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Influence of Punch Trough Stop Layer and Well Depths on the robustness of bulk FinFETs to Heavy Ions impact

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ABSTRACT This study analyzes the effects of the punch-through stop (PTS) layer and well depth in a bulk FinFET SRAM cell on the fraction of charge generated by an ion impact that is collected by the FinFET channel. More than 1700 3D TCAD simulations have been performed to obtain a detailed map of the sensitivity areas in a full cell 6-T SRAM 22 nm bulk-FinFET process. The influence of the well depth on the charge collected by the drain devices of the SRAM cell has been studied, and it has been concluded that the collected charge can be reduced down to 300% simply by modifying the depth of the well, without affecting the performance of the cell. Different PTS layer depths have been analyzed in order to calculate which value minimizes the impact of the charge generated by an ion during its track along the FinFET body. The simulations carried out allow to conclude that the incorporation of a PTS layer not only reduces the leakage current, but also reduces the amount of charge, delivered by the ion, that reaches the drain region. Simulation results also show that the fraction of the charge generated by the ion impact, which is collected by the drain, mainly depends on the depth of the wells, whereas the PTS layer hardly modifies the collected charge.

INDEX TERMS Charge collection, single event cross section, radiation hardening, soft error, single event transient (SET), single event upset (SEU), FinFET, 3D TCAD modeling

I. INTRODUCTION

Single Event Effects (SEE) are due to prompt collection by the circuit of the charge originated in the substrate by ionizing radiation. Because CMOS ICs memory cells store information in two discrete voltage levels, VDD and VSS, the collected charge can upset the stored state if the induced transient voltage exceeds the logic margins, either momentarily, which is known as a Single Event Transient (SET) or the upset of a storage element. While the bit would eventually recover to its original value as the charge is collected if it is meanwhile sensed, it could lead to a permanent flip of contents of that storage, which is known as a Single Event Upset (SEU).

Each circuit has a sensitive volume in which the charge deposited on the substrate is collected. SRAM cells and latches are characterized by the critical charge Q_{crit}, which, if collected by one of the two storage nodes, will flip the cell state.

Although the scaling down of individual transistors and memory cells tends to reduce the probability of a particle crossing a sensitive volume and triggering an upset event, smaller individual cells also present decreasing values of the critical charge, which eventually increases the overall sensitivity. This makes storage cells the most sensitive and vulnerable elements of an electronic circuit.

FinFETs have replaced planar CMOS as the device of choice because of their many superior attributes, especially in the areas of performance, leakage power, intra-die variability, low voltage operation (lowering dynamic power), and minimal retention voltage for SRAMs. It offers excellent solutions to the problems of subthreshold leakage, poor short-channel electrostatic behavior, and high device parameters variability, which plagued planar CMOS as it scaled down to 20 nm. Furthermore, its ability to operate at a much lower supply voltage allowed a more aggressive

voltage scaling down, which contributed to additional savings in static and dynamic powers.

With the development of high-k/metal gate technology and the application of low supply voltage, punch through leakage current has become one of the primary components of the OFF state current in FinFETs [1]–[3]. The scaling-down of FinFETs has led to improved junction isolation below the channel to suppress the source-to-drain punch through the leakage current. To the best of our knowledge, only the effects of the Total Ionizing Dose (TID) when the Punch-Through Stop (PTS) layer is implanted in bulk FinFET devices have been analyzed [4].

The dynamics of the charge generated by a radiation particle in a device was properly evaluated in [5]. After the ion reaches the silicon surface, it generates a track that leaves a dense plasma of electron-hole pairs along its path. If the electron-hole plasma is generated in a region with an electric field, electrons and holes are separated and a current spike can be observed at sensitive circuit nodes where free carriers are collected. This current spike has two components: a prompt component due to charge collection in the original depletion region and the funnel region [5], and a delayed component due to carrier diffusion up to the depletion region where it is quickly collected by the junction electric field.

The change in device structure from planar to FinFET modifies the sensitive area and the charge collection process after an ion strike [6]. In conventional CMOS devices all the area under the device collects the charge produced by the ion, but in the bulk FinFET it is only collected in the area under the fin.

To date, several approaches to build the well of the transistor which mitigates the effect of ionizing radiation in planar CMOS have been implemented [7]–[9]. However, the results are inconclusive, as they lead to contradictory conclusions. In the case of bulk FinFETs, no previous studies have investigated the effect of the well depth on the impact of ionizing radiation on the device performance have been found.

The spot defects, some of them modelled at the electrical level as resistors can exacerbate the memory susceptibility to SEUs. A good fault coverage can avoid the use of these SRAM cells in critical missions as suggested in [10]. The influence of these types of defects has already been previously studied in [11].

A previous study [12] proposed the creation of an internal structure to generate an electrical field that drives the charge generated by the ion track in the FinFET channel, thus satisfactorily mitigating the effect of ionizing radiation. However, this solution is very expensive from a technological point of view because it requires the insertion of complementarily doped regions near the active region of the device, which increases the total area of the circuit.

In this context, the present work analyzes the impact of the PTS layer and the choice of the depth well as mechanisms to harden a FinFET SRAM cell against ionizing radiation without affecting its performance.

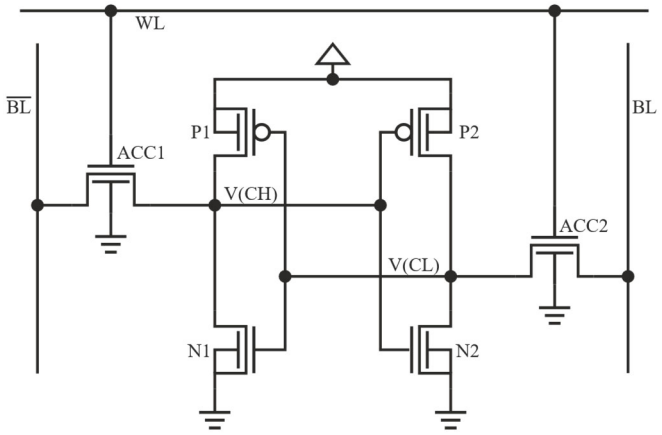

FIGURE 1. Schematic of the 6T SRAM cell.

The structure of the manuscript is as follows. Section II outlines the simulation procedures. In Section III, the sensitivity of the full SRAM cell is analyzed. A total of 1700 simulations of the entire memory cell have been performed. In Section IV, the effects of an ion strike on the Pfin and Nfin devices, with and without a PTS layer, are evaluated. In Section V, a set of Pwell and Nwell depths are evaluated to determine how to improve the hardening of the overall SRAM cell. In section VI, the combined effect of the PTS layer position and wells depth is considered. Finally, in Section VII, the main conclusions of this study are presented.

II. SIMULATION ENVIRONMENT

Technology Computer-Aided Design (TCAD) [13] is an ideal tool for studying the effects of ionizing radiation on integrated circuits (ICs), and in particular to explain the influence of ionizing radiation on a bulk FinFET SRAM cell under SEEs.

The cell studied is a classic 6T SRAM cell. It employs a regenerative feedback loop between two opposite inverters to hold the latched data (Fig. 1). It is susceptible to SEU when the upset causes the voltage level of the struck inverter to cross the tripping point of the opposite inverter, causing the flip of the stored data. More importantly, the SEU rate increases with the technological advancement.

This 6T SRAM cell is formed using two pull-down Nfin devices (N1 and N2), two Pfin pull-up devices (P1 and P2), and two Nfin pass-gate (ACC1 and ACC2). A previous work [14] evaluated several configurations for the number of fins (PU:PD:PG), and the combination (1:2:2) was observed to improve the cell transient current and writing capability of the cell, with the remaining configurations presenting poor writing margins.

The layout and 3-D structure of the simulated SRAM cell are illustrated in Fig. 2 and in Fig. 3, respectively. The transistors considered are from a 22 nm bulk-FinFET process, with High-k/Metal gate scheme and nominal VDD of 1 V. FinFET doping profiles and dimensions have been obtained from [15], a case that is based on process emulation, and from [16]. Both devices (Pfin and Nfin) have been calibrated to

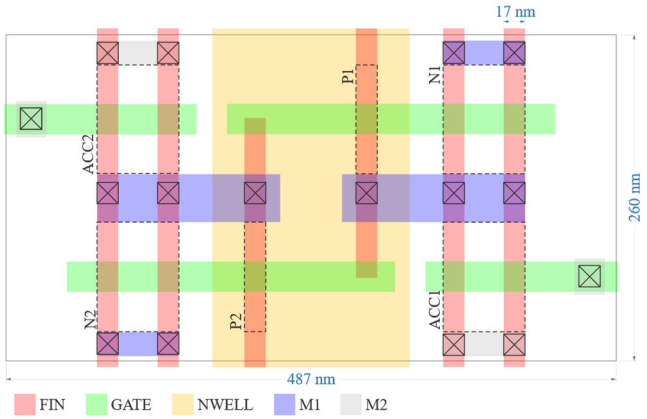

FIGURE 2. Layout of the bulk-FinFET 6T SRAM bulk-FinFET cell studied in this work. All dimensions are in nm.

fulfil the ITRS high-performance requirements for the technology node evaluated in this study [17].

Electrical characteristics such as drain current vs. gate voltage (I_D–V_G), drain current vs. drain-source voltage (I_D–V_{DS}), and threshold voltage (V_T) were also calibrated to achieve the performance published in [18], where both the ITRS and designed I-V curves were compared. The substrate thickness has been chosen to be 0.5 µm. Dodd et al. [19] studied the impact of substrate thickness in CMOS technology and concluded that the best results are obtained with a lower substrate thickness, due to the reduction in the length of the ion path. Consequently, the amount of charge deposited, which diffuses up to the depletion region decreases. We have demonstrated that these conclusions are also true for FinFETs.

In all the simulations in the present work, the following models are used: impact ionization, drift-diffusion transport, concentration dependent Shockley-Read-Hall (SRH) statistics, high-field mobility degradation, density-gradient quantum corrections, and Coulomb scattering.

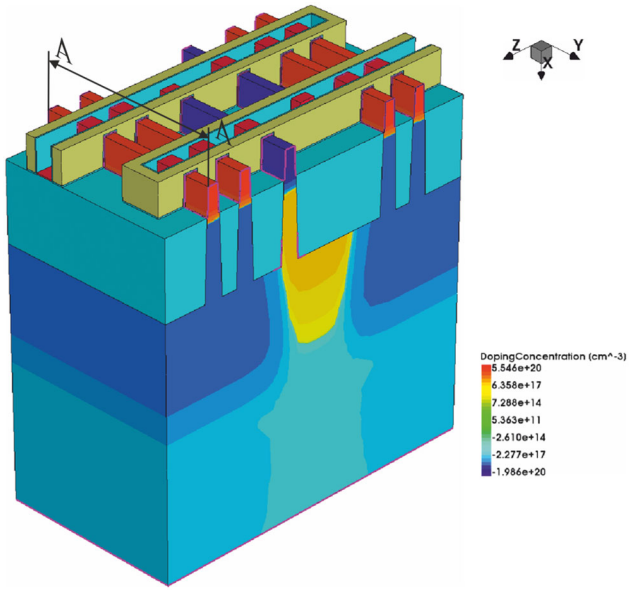

FIGURE 3. Three-dimensional TCAD model of the SRAM cell simulated in this study. The cell has been designed according a 22nm bulk trigate FinFET process.

The spatial and temporal ion track parameters have been selected from [12], with a constant Linear Energy Transfer (LET) along the track, Gaussian spatial distribution, characteristic ion-track radius of the Gaussian function of 10 nm, and for best fit with this technology, the characteristic width, t_{hi}, of the temporal evolution of 0.8 ps has been chosen. The incident angle of the ion has been chosen normal to the surface of silicon, which is the worst-case scenario [20].

III. SRAM CELL CHARACTERIZATION

In this section, we characterize the robustness of the SRAM cell versus ion impact with normal incidence over the entire cell surface.

Standard single-point 3-D mixed-level simulations are known to predict upset thresholds in very good agreement with the measured thresholds.

In these simulations, the most sensitive strike location was assumed based on past experiences. However, error rates in ICs are dependent not only on the threshold but also on the sensitive area, which cannot be obtained from a single-point simulation, and, the sensitive area is fitted by the LET of the ion.

The unit cell area is 0.26 µm x 0.487 µm and transient 3-D simulations were performed for particle ion strikes incident every 4 nm (maximum distance) throughout the SRAM cell surface. An additional 0.3 µm of silicon was added around the unit cell to minimize the nonphysical reflections of carriers at the boundaries. The simulation results provide a map of the degree of sensitivity to SEU of the SRAM unit cell for each evaluated point. The angle of ion particle strike is normal to the surface, and the LET chosen (0.4 MeV-cm^2/mg) has been enough lower enough in order to avoid the change of the cell state. Upon increasing the LET, all the results shifts up proportionally, until they reach the switch of the cell [12].

The SRAM cell is considered to be in the hold state, with V(CH) at high level and V(CL) at low level; that is, devices N1 and P2 are in OFF state, and devices N2 and P1 are in ON state. The devices ACC1 and ACC2 are also in OFF state, with BL and $\overline{\text{BL}}$ lines at high value level, and WL line at low level.

In Fig. 4, the minimum value of the V(CH) voltage after an ion impact is plotted. For the sake of clarity, the contour plot is shown in Fig. 5. Because V(CH) is at high level, the minimum value peak represents the maximum change in this voltage when an ion impacts the selected SRAM point. At points where the value of V (CH) is 1V or close to this value, the effect of the ion impact is practically null. However, the lower the value of V (CH), the larger the effect of ion impact at that point, and a lower LET could potentially change the stored bit in the SRAM.

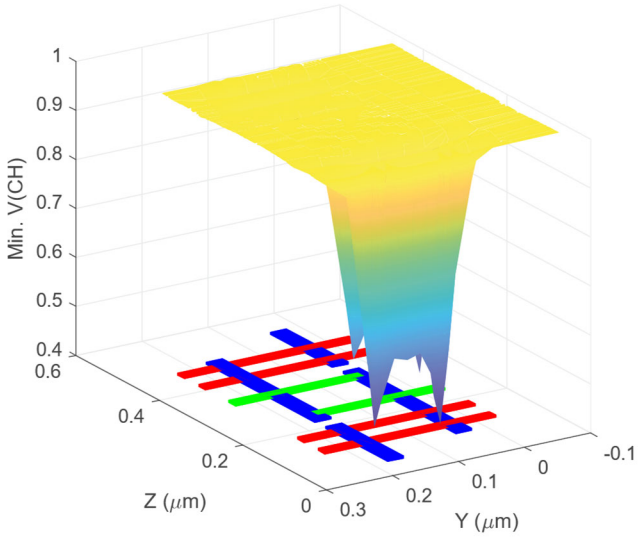

FIGURE 4. Map of V(CH) minimal value reached in the SRAM after an ion impact. Below, the NFin layer (red bar), PFin layer (green bar) and gate layer (blue bar) are plotted.

For reference, the layout of SRAM is plotted at the bottom of the figure. Red bars represent the NFin layer, green bars represent the PFin layer, and blue bars represent the gate layer (see Fig. 2 for the device reference).

As observed, the most sensitive area is the two fins of the N1 FinFET drain (in OFF state), which agrees with results already published in the literature [21]. However, the area occupied by the two fins of the ACC1 drain are similarly affected. For this SRAM design, the NFin pull-down transistors and the NFin access transistors share a common fin, and the ACC1 device is in OFF state when the ion reaches their drain. The effect of the ion impact decreases quasi linearly with the distance to the reverse-biased NFin drain, and its maximum value is reached at the drain-body junction, with a peak value of -0.4355 V, which is very close to the switching voltage (0.39 volts, approximately). A smaller effect was observed in the drain of the N2-ACC2 region.

Unlike in MOS transistors, in Bulk FinFET devices when a dense plasma of electron-hole pairs is generated by the ion, the only path to reach the fin from the substrate is the narrow sub-

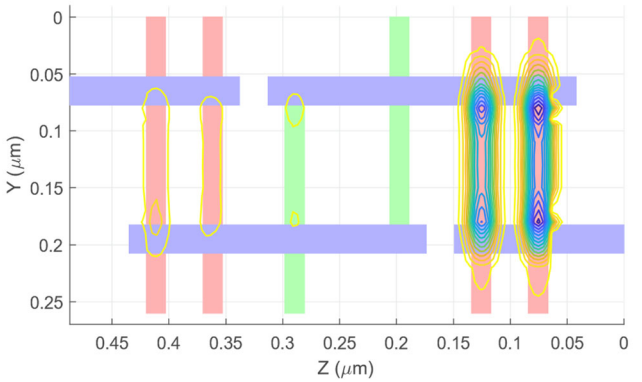

FIGURE 5. Contour map of V(CH) peak values reached in the SRAM after an ion impact. Overprinted are the NFin layer (red bar), PFin layer (green bar) and gate layer (blue bar).

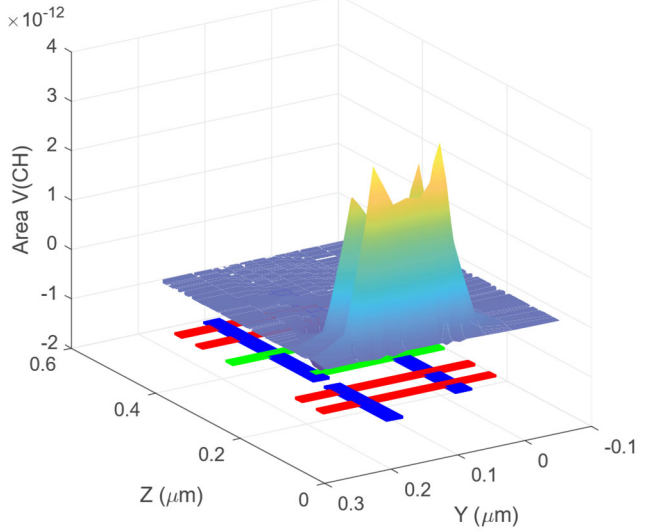

FIGURE 6. Map of the modified area of V(CH) in the SRAM after an ion impact. In the lower part, the NFin layer (red bar), PFin layer (green bar) and gate layer (blue bar) are plotted.

fin region [12]. Reverse-biased pn junctions are among the most efficient regions in collecting charge, thanks to the large depletion region and the high electric field.

As an example, consider that an ionizing particle strikes one of the reverse-biased drain junctions, for instance the drain of the OFF NFin in the cross-coupled inverter pair in the cell. As a consequence, the electron-hole pairs will be generated and collected by the depletion region of the drain junction. This will cause a transient current which will flow through the struck junction, while the restoring transistor (the ON PFin of the same inverter) will source current in an attempt to balance the particle-induced over-current. However, since the restoring PFin has a finite amount of current drive and a finite channel conductance, the voltage will drop at the struck node.

As the distance from depletion region increases, the e-h pairs will recombine and reduce the excess charge before reaching the drain terminal via the sub-fin region. The points where V(CH) does not almost decrease are the points where the electric field is small enough to allow most of the e-h recombination.

The area change of the V(CH) voltage under the nominal value (1 V) has been evaluated after ion impact and is plotted in Fig. 6. To obtain the area, the integral of V(CH) minus their nominal voltage has been calculated. The trapezoidal rule was applied to obtain the integral, and the transient simulation time was increased to account for all the voltage changes. Note that the area under the nominal voltage in the most sensitive section (the drain region of the N1 and ACC1 devices) follows the map of the V(CH) minimal value reached when an ion impacts this area. However, when the ion impacts P1 device (in ON state), the area is negative. The negative area of V(CH) indicates an increase in V(CH) voltage. In the worst case, this voltage reaches up to 20% of the nominal VDD value.

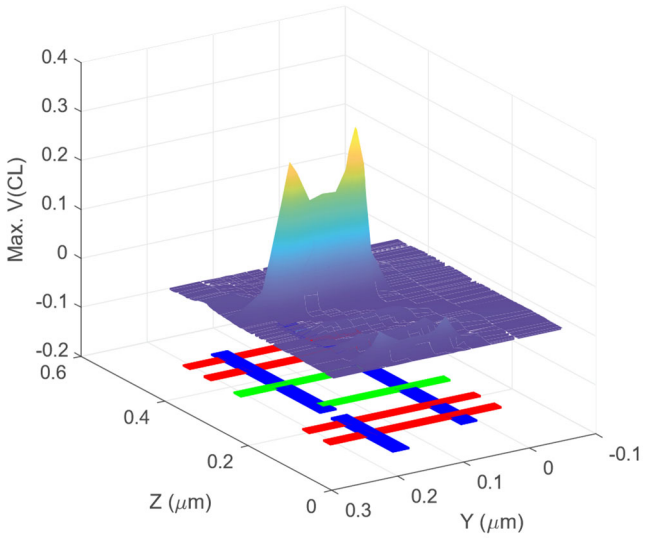

FIGURE 7. Map of V(CL) maximum value reached in the SRAM after an ion impact. Below the plot the NFin layer (red bar), PFin layer (green bar) and gate layer (blue bar).

The effects on the V(CL) node are plotted in Fig. 7 and Fig. 8. In this case, V(CL) is at low level, and the 3D map monitors the maximum voltage reached after an ion impact. Similar behavior has been observed for this node. The most sensitive region is around the P2 Pfin device, which is in OFF state. However, the most sensitive region extends to the drain of Nfin ACC2, which is also in OFF state. As before, the cause is found in both devices sharing the drain in the same fin.

The maximum voltage reached 0.3461V after an ion impact is obtained at the edge between the drain area and the area under the gate (similar to V(CH)), owing to the highest electrical field in this area.

Addition, we calculated the modified area of the V(CL) voltage after the ion impact (Fig. 9). The most sensitive region for the maximum value is where we found the maximum change in the area, which is similar to the effects in the V(CH). An impact in the drain regions of N2 (in on state) and ACC2

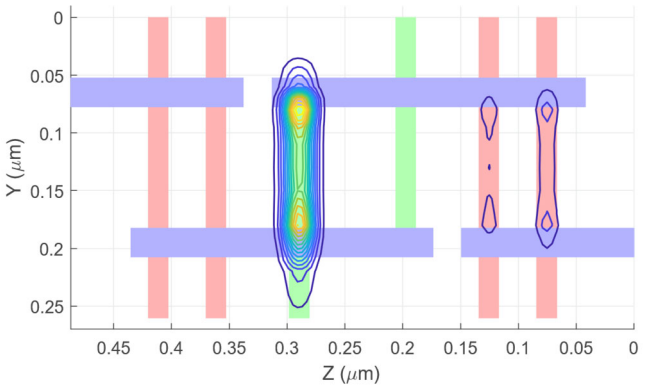

FIGURE 8. Contour map of V(CL) peak values reached in the SRAM after an ion impact. Overprinted are the NFin layer (red bar), PFin layer (green bar) and gate layer (blue bar).

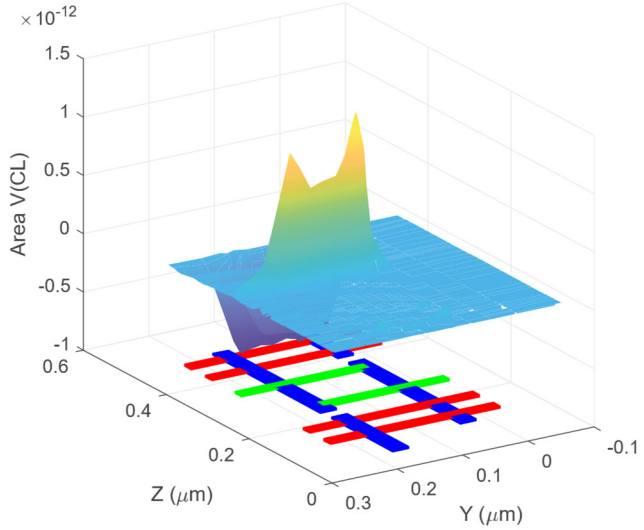

FIGURE 9. Map of the modified area of V(CL) in the SRAM after an ion impact. In the lower part are plotted the NFin layer (red bar), PFin layer (green bar) and gate layer (blue bar).

devices generates a negative value in the V(CL) voltage. This value can reach -20% of the nominal VDD value.

Simulations have been performed with N1 and P2 devices in OFF state and N2 and P1 devices in ON state, that is, V(CH) and V(CL) are at high and low levels, respectively, which corresponds to storing a low-level bit. In this situation, the most sensitive regions are the drain regions of N1, P2, and ACC1, whereas for a stored high logical value, the most sensitive regions are the drain regions of N2, P1, and ACC2.

The critical charge Q_{crit} is the minimum charge that must be deposited by a particle strike to cause a circuit malfunction. Because the relationship between the voltage peak value and LET follows a linear rule [12], the critical charge for each point in the previous results can be obtained easily using linear extrapolation.

In the simulations carried out previously, a metastable state of the SRAM cell was observed for LET (0.6 MeV-cm^2/mg) below the Q_{crit} value before flipping the stored bit (see Fig. 10).

The simulated switching time for this cell is approximately 9.5 ps, but in the case of Fig. 10, both nodes V(CH) and V(CL) remain for a large period of time (approximately 25ps) at an undefined logical value after an ion strike, which produces a charge in the cell near their critical charge. This undefined value can induce incorrect values if the cell is read in this period; therefore, the definition of the critical charge must include the effect of metastability in memory cells.

Effects of track angular incidence

In previous works, the charge collected by a bulk-FinFET device after an ionizing particle hit, has demonstrated a great dependence on the angular incidence of the ion trajectory [20], [22]. But, a priori, contradictory results have been found regarding the influence of the angle on the charge collected by the terminals of active devices. In [20], the angle of incidence

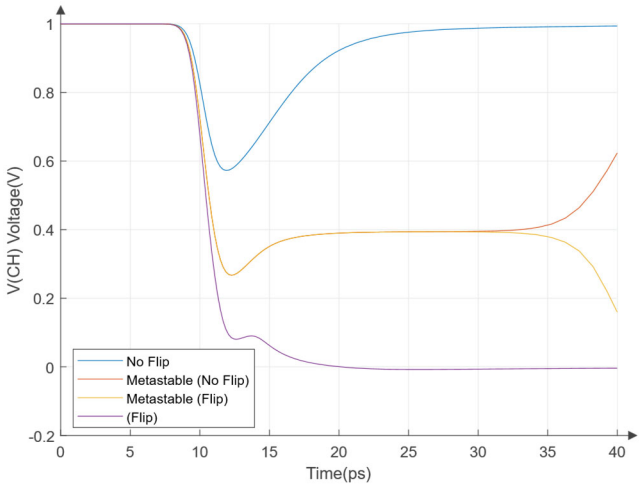

FIGURE 10. Metastability of the cell when an ion impact generates a lower charge than the critical charge. Both lines, V(CH) and V(CL) remains in an undefined value, for a large period of time compared with the switching time of the cell.

that mostly affects the operation of storage elements (in their case flip flops) is the normal incidence angle of the track to the bulk. On the contrary, in [22] the authors conclude that the largest Multiple Bit Upset (MBU) effect occurs for angles perpendicular to the fin direction.

We have carried out an exhaustive analysis of the effect of the incidence angle of the ionizing particles assuming a track length equal to that used with normal incidence (0.5 μm) and the same characteristics as in the previous section in order to make a correct comparison.

The results show that in order to obtain a higher variation of the SRAM cell voltages compared to normal incidence, the trajectory of the ion should maximize the match of the drain depletion region. The more the ion track path coincides with the drain depletion region, the greater the effect on the voltages V(CH) and V(CL). Thus, not only the angle of the track has an impact on the collected charge, but also the depth of the ion track. That is, in the SRAM studied, the maximum variation of the voltage corresponds to a trajectory with an incidence direction parallel to the fins and an angle of 90 degrees, and a depth of 0.05 μm.

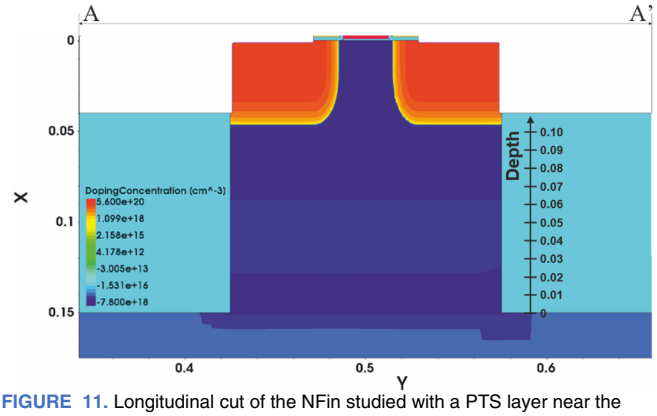

FIGURE 11. Longitudinal cut of the NFin studied with a PTS layer near the base of the Fin. All the dimensions are in μm.

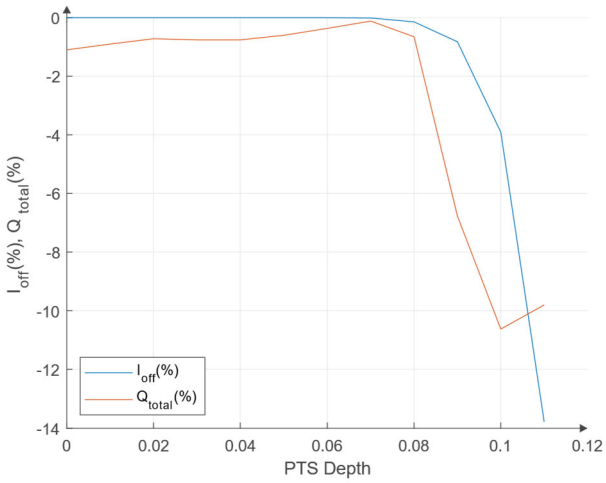

FIGURE 12. Leakage current I_{OFF} and charge collected in the NFin as a function of the PTS layer depth relative to the case without PTS layer.

To corroborate the previous result, we have varied the points of incidence of the track, moving them out from the drain junction. Lower variations of the cell voltages for both V(CH) and V(CL) were obtained.

The main reason for the larger effect in the SRAM voltage is the increase in the drift component due to the charge collection in the original depletion region.

The results in [20] and [22] are not contradictory. They correspond to devices with different geometries (with the available information), in such a way that, in their respective cases, the maximum values match when the ion trajectory crosses the major area of the drain depletion region.

IV. EFFECTS OF THE PUNCH TROUGH STOP LAYER

In this section, only the individual devices (Pfin and Nfin) have been simulated, with Pwell and Nwell depth of 0.17 μm and 0.2 μm, respectively. First, we calculated the basic parameters of the device (leakage current I_{off}, maximum current I_{dsat}, transconductance gain g_m, and threshold voltage V_t) without PTS layer, and compared them with those obtained for several values of the PTS layer depths. The reference point for the depth of the PTS layer is the Shallow Trench Isolation (STI), the bottom position of which is shown in Fig. 11.

Fig. 12 shows the leakage current, I_{OFF}, and charge collected, Q_{total}, by the drain of the Nfin device for different depths of PTS relative to the same device without PTS. The selected range of values do not degrade the I_{dsat} and g_m. The nearest value to the device channel of the PTS layer is 0.11 μm in the range simulated.

As expected, the best result is achieved for a depth closer to the bottom region of the drain-source doping area, which is where the punch trough current flows. For depth values greater than 0.1 μm, I_{dsat} degrades considerably, worsening the performance of the device. The charge collected by the device after an ion impact in the drain is smaller with the proximity of the PTS layer to the channel, but for a depth value greater than 0.1 μm the collected charge increases significantly. Note

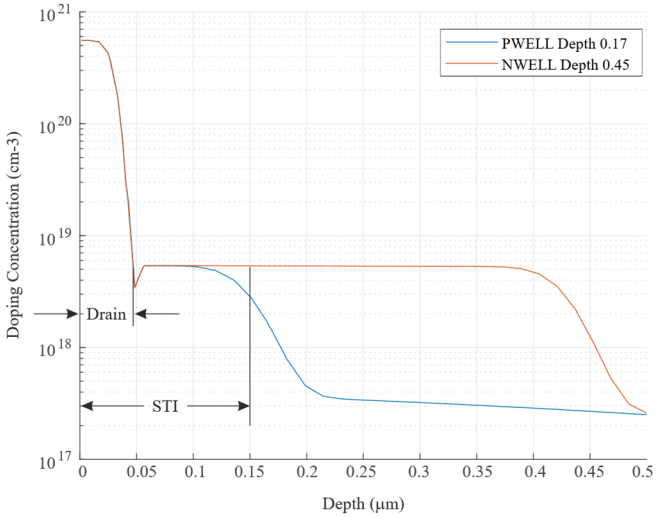

FIGURE 14. Doping profile under the Pfin drain terminal with a Pwell depth of 0.17 μm, and Nwell of 0.45 μm.

that this depth limit matches the maximum PTS current knee point of fig. 12.

The simulation results for the Pfin device are shown in Fig. 13. The behaviors of the collected charge and leakage current are similar to those of the Nfin device. Depths greater than 0.1 μm impair the device characteristics and increase the charge collected by the device.

The presence of a PTS creates a small electric field that blocks the diffusion of charge towards the active terminals of the device.

The selected depth for the PTS layer in the next sections is 0.1 μm for all the devices in the SRAM cell.

V. EFFECTS OF THE WELL DEPTH

In this section, we evaluate the effect of the Pwell and Nwell depths on the collected charge in the Pfin and Nfin devices without PTS layer in the SRAM cell of Fig. 3. The cell has an additional silicon area around it to avoid loss of charge generated by the ion track. The SRAM cell is in hold state with V(CH) at high level and V(CL) at low level; that is, N1 and P2 devices are in OFF state, and N2 and P1 are in ON state. The ion impacts have a normal trajectory to the surface of the drain area of the P2 and N1 devices.

The values of the Pwell and Nwell depths are modified, from 0.17 μm to 0.45 μm.

Nwell (and also Pwell) needs good biasing and well-taps to prevent latch-up. Choosing a value for the Nwell (or Pwell) close to the depth of the STI (0.15 μm) can cause the isolation of the well around each fin and the need for additional well-taps because the well under the STI is not sufficiently thick to allow correct biasing between adjacent fins. Silicon is 0.5 μm thick, so the deepest well evaluated is 0.45 μm.

An example of the doping profile under the drain area of the Nfin device is shown in Fig. 14 for a Nwell depth of 0.45 μm, and Pwell of 0.17 μm.

In all these simulations, we check the Static Noise Margin (SNM) in hold, read, and write operations using the butterfly method and the device parameters (leakage current I_{off}, maximum current I_{dsat}, transconductance gain g_m, and the threshold voltage V_t). No modifications or degradation of the SNM or device parameters have been observed for the entire set of values.

The effects of the ion track crossing the drain of N1 are illustrated in Fig. 15. A low LET value (0.4 MeV-cm^2/mg) has been chosen to avoid flipping the stored value in the SRAM cell. An increase in the LET causes the entire shape of the graph to shift proportionally to the LET value. The minimum voltage V(CH) that causes switching of the value stored in this cell is approximately 0.39 Volts with VDD = 1V.

As shown, a clear dependence exits between the well depth and the V(CH) minimal peak value. Lower values of Pwell and higher values of Nwell yield lower V(CH) peak values, when the heavy ion impacts on the N1 drain area. It should be noted that the static value of V(CH) is high.

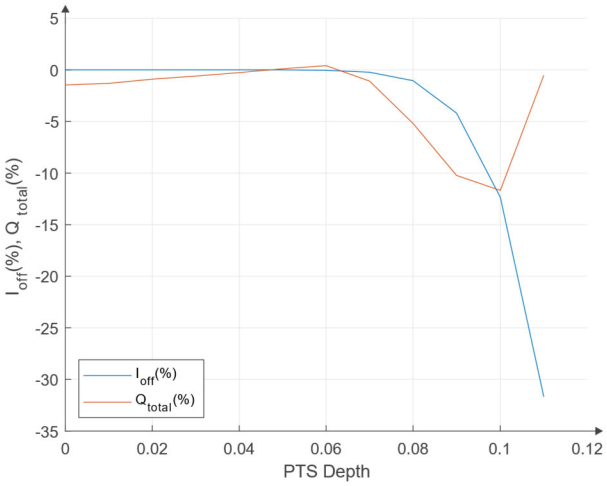

FIGURE 13. Relative charge collected in the drain of the PFin and leakage current compared with no PTS layer, and changing the PTS layer depth.

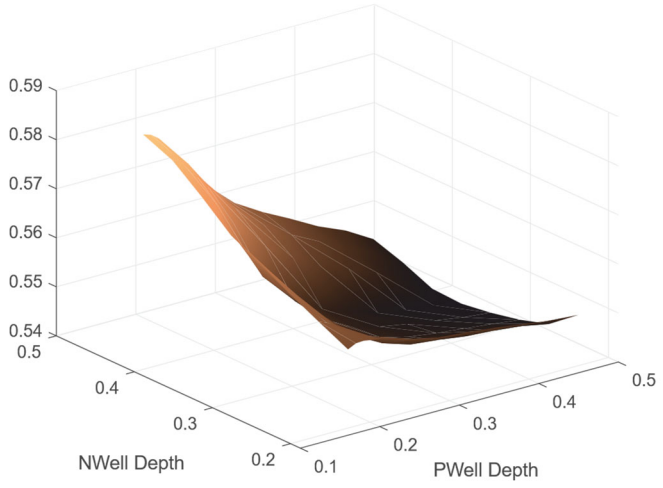

FIGURE 15. Minimum peak value of the V(CH) voltage when an ion impacts in the drain area of N1 device of the SRAM, vs the Nwell and Pwell depths.

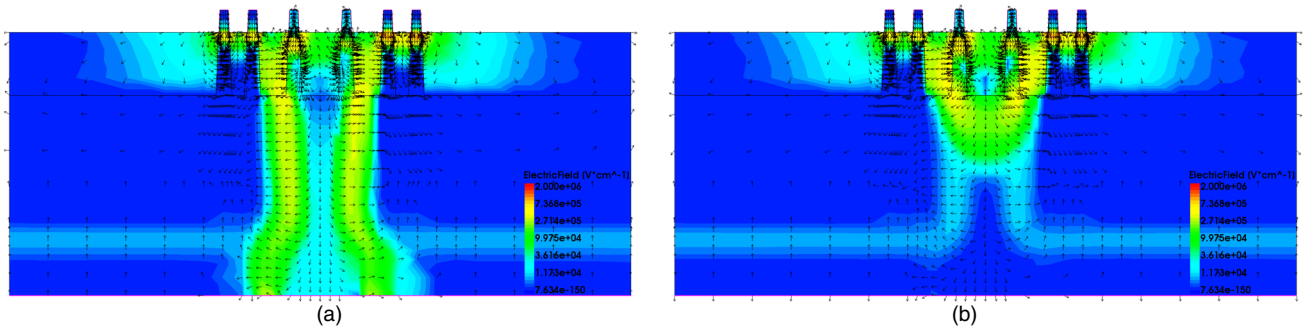

FIGURE 17. Electric field in the cross section of the SRAM (perpendicular to fin direction). (a) PWELL depth of 0.4 μm, NWELL depth 0.4 μm; (b) PWELL depth of 0.4 μm, NWELL depth 0.176 μm

We evaluate the area under the nominal value (VDD) caused by the ion in the V(CH) voltage, and the relationship follows the same shape as V(CH) peak.

The same set of well depths have been evaluated for an ion impact on the P2 device, and the results are shown in Fig. 16. In this case, the plotted parameter is the peak value of V(CL) because the static value of this voltage is low. The Pwell depth has a minimal effect on the peak value of V(CL).

Comparing the results of Fig. 15 and Fig. 16, assuming the same LET in both experiments, it can be concluded that the Pfin devices are more influenced by the well depths than the N devices. This is because in this SRAM cell, the Pfin device is formed by only a single fin, whereas the Nfin device uses two fins. The best results are found for shallower wells; however, Nfin has the most sensitive region, and after an ion impact, there is a higher probability of flipping the data.

A previous study [12] proposed the creation of an internal structure to generate an electrical field that drives the charge generated by the ion track out of the FinFET channel, thus satisfactorily mitigating the effect of the ionizing radiation.

In fig. 17, the electric field distribution in the cross section of the modified SRAM structure proposed in Ref [12] is shown at 0.4 μm depth in the PWELL and at 0.4 μm depth in the NWELL in the left figure, and at 0.4 μm depth in the PWELL and at 0.176 μm depth at the NWELL in the right figure. The shape of the electric field with a shallower NWELL (right figure) prevents the diffusion of the charges created by the ion towards the Pfin device.

Previous studies concluded that multiple-cell-upset events are due to charge sharing among adjacent cells [23], [24] . The presence of an electric field in the region under the device allows reducing the charge that reaches the device and thus reduces the number of MBU events.

VI. PTS LAYER AND WELL DEPTHS

The effects of the wells and PTS layer depths have been evaluated separately in previous sections. In this section, we combine the previous results and compare them to validate the combined effects of the PTS layer and well depth.

The selected Pwell and Nwell depths are 0.176 μm and 0.40 μm. The selected PTS layer depth is 0.1 μm for both Nfin and Pfin devices, which according to Section IV is the depth of the PTS layer, which provides greater robustness of the SRAM cell versus ion impacts.

Simulations for all the possible combinations of well depth values have been performed, and compared the cases with and without PTS layer. A shallow Nwell provides good hardening for the Pfin devices, whereas no improvement in hardening is

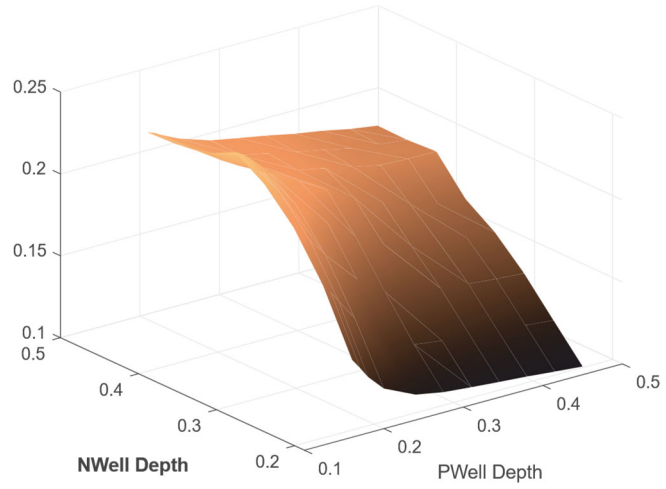

FIGURE 16. Maximum peak value of the V(CL) voltage when an ion impacts in the drain area of P2 device of the SRAM, in function of the Nwell and Pwell depths.

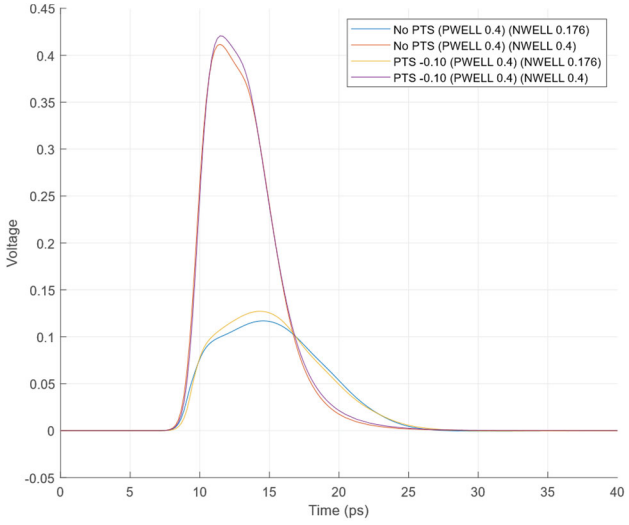

FIGURE 18. Shape of V(CL) voltage when an ion impact in the drain area of P2 device. The simulations correspond to a PWELL depth of 0.4 μm, and NWELL of 0.176 μm and 0.4 μm, with and without PTS layer.

found in the Nfin devices. The best results for the Nfin devices were obtained for a deep Nwell and a shallow Pwell.

A summary of the most significant simulation results is presented in Fig. 18, when an ion impacts in the P2 drain region. The predominant effect to harden the Pfin device was achieved with shallow Nwell. It should be noted that the insertion of the PTS layer has a minor effect. The reduction achieved in the V(CL) voltage is almost a factor of three times.

Because of the shallow Nwell, the junction formed by the Nwell and the substrate doping overlaps the PTS layer. This modifies the profile in this region and boosts the shielding of the PTS layer by improving the hardening of the Pfin device. The leakage current remains unchanged.

In Fig. 19, a summary of the simulation results when an ion impacts the Nfin device is shown. In this case, the depth of Pwell and Nwell hardly modifies the effect on voltage V(CH). The best results are obtained with the insertion of a PTS layer, with an improvement of approximately 5%, compared with no insertion of the PTS layer. The improvement in the leakage current is maintained.

The low effect on V(CH) is due to the fact that the PWELL profile is not as abrupt as the NWELL, causing a weaker electric field which attenuates its effects.

VII. CONCLUSIONS

This study evaluates the sensitivity versus the ionizing radiation of a 6T SRAM FinFET cell designed in a 22 nm bulk-FinFET process using 3D TCAD Sentaurus tools.

A sensitivity map to SEU has been generated, which shows that the area reduction techniques used for SRAM cell design decrease the robustness under heavy ions strikes. This is mainly caused by the sharing of the fins between some transistors. When the ion hits the drain region, the effects propagate beyond the transistor through the shared fins, which adversely affects the performance of the exposed cell.

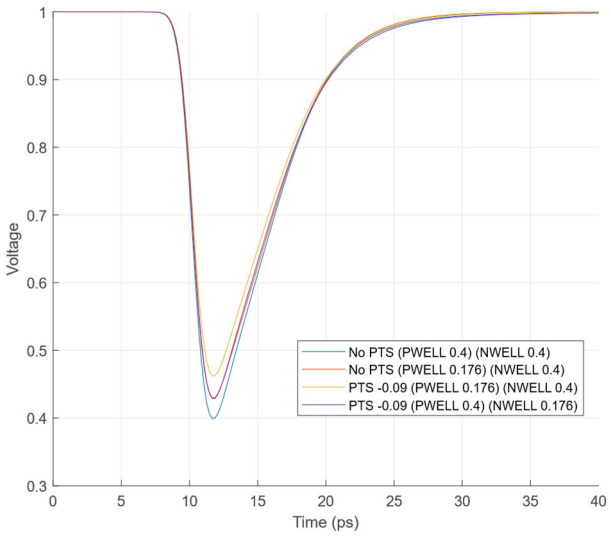

FIGURE 19. Shape of V(CH) voltage when an ion impact in the drain area of N1 device. The simulations correspond to a PWELL depth of 0.4 μm and 0.176 μm, and NWELL of 0.176 μm and 0.4 μm, with and without PTS layer.

The influence of the position of the PTS layer and depth of the wells on the ionizing radiation effects on bulk FinFETs are also investigated. It is observed that if the PTS layer is placed under the transistor channel, the effects of SEU are significantly reduced. In the case of the wells depth, the influence of the ionizing radiation on the robustness of the SRAM cell is analyzed. It is observed that the lowest sensitivity to ion is achieved when the depths of the Pwell and Nwell are maximum and minimum, respectively, achieving an increase in hardening of up to three times higher. Furthermore, depth tuning does not change the performance of the cell.

This improvement has been evaluated using 22 nm twin-well technology. This improvement must be evaluated for other types of wells.

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