An Approach to Dynamic Power Consumption Current Testing of CMOS ICs

J.A. Segura, M. Roca

Physics Dept.
Balearic Islands University
07071 Palma de Mallorca, SPAIN

D. Mateo, A. Rubio

Electronic Engineering Dept.
Polytechnic University of Catalonia
08034 Barcelona, SPAIN

Abstract

I_{DDQ} testing is a powerful strategy for detecting defects that do not alter the logic behavior of CMOS ICs. Such a technique is very effective especially in the detection of bridging defects although some opens can be also detected. However, an important set of open and parametric defects escape quiescent power supply current testing because they prevent current elevation. Extending the consumption current testing time, from the static period to the dynamic one (i.e. considering the transient current), defects not covered with I_{DDQ} can be detected. Simulations using an on-chip sensor show that this technique can reach a high coverage for defects preventing current and also for those raising the static power consumption.

1 Introduction

In early integrated circuits (fabricated in bipolar technology), logic fault models were developed as effective tools for detecting defects. Later, those fault models were used in the verification of CMOS ICs. During the last decade several works from different authors reported that the behavior of CMOS defective circuits could not be efficiently modeled with a logic based description [1, 2]. As a solution, testing strategies based on other observables than the logic circuit outputs were investigated. A high percentage of defective circuits in CMOS technology show a static power consumption (I_{DDQ}) many orders of magnitude higher than non defective ones, providing a valid observable to determine its goodness [3, 4]. The advantage of I_{DDQ} vs. logic testing is based upon a higher coverage and observability, providing the detection of a greater number of defects with a simplified test vector generation process. A detailed analysis of I_{DDQ} and Boolean test capabilities for defects in CMOS circuits was presented at the 1994 ITC [5]. Although I_{DDQ} testing significantly increases the coverage when combined with logic testing, some defects may not be detected. Open defects that do not raise the static current consumption and some parametric defects causing signal delays may escape a combination of I_{DDQ} and Boolean tests. This paper analyzes the possibilities of dynamic current testing ($i_{dd}(t)$) on the detection of such defects. Dynamic power supply current testing has been previously applied to the study of SRAMs [6].

2 The principles of $i_{dd}(t)$ testing

The power consumption current signature of a CMOS static circuit consists of a sequence of sharpen peaks appearing during the input/output transitions. During the quiescent period, the current consumption is negligible. Power consumption current peaks are mainly due to two factors: 1) the simultaneous conduction of n-MOS and p-MOS transistors during the transition, and 2) the charge/discharge of circuit internal capacitances. Defects appearing in CMOS circuits may change the current consumption signature by eliminating some current peaks or causing elevated current during the quiescent periods. Figure 1 shows the dynamic current consumption of a CMOS NAND gate for three different cases, obtained measuring the potential drop at a 100 Ω resistor connected between the ground node of the circuit and the power supply ground terminal. Figure 1.a corresponds to the input voltage transition, while in 1.b the current peak for a fault-free gate is reported. Figure 1.c shows the same measurement when an open is present at the gate of one n-MOS transistors of the NAND. Such an open occurs far away from the transistor resulting in a high gate capacitance that induces a voltage at this node below the threshold of the device. Because the open prevents the device conduction, the peak of fig. 1.b is missing. The quiescent current of the circuit is not changed so an I_{DDQ} test cannot detect the defect. For

0-8186-7000-2/95 $04.00 © 1995 IEEE

Authorized licensed use limited to: UNIVERSITAT POLITECNICA DE CATALUNYA. Downloaded on September 13,2022 at 06:34:42 UTC from IEEE Xplore. Restrictions apply.

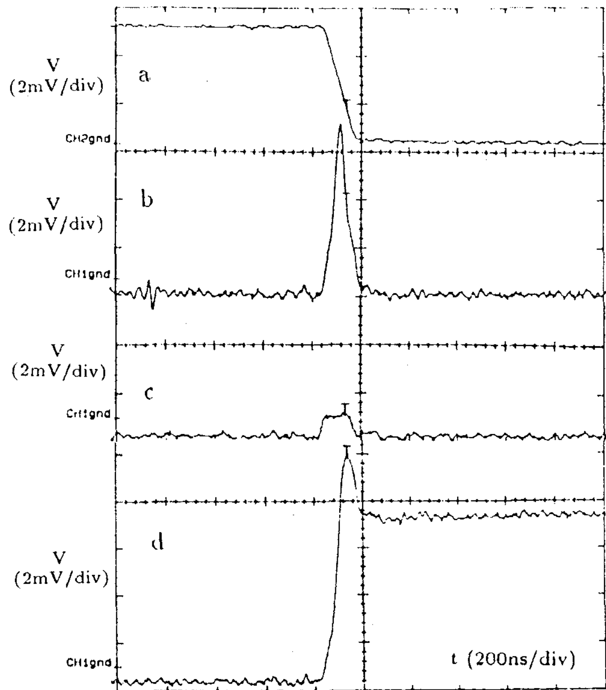

Figure 1: *Input transition (a), and dynamic current consumption for a NAND gate. The measurement shown in (b) was obtained from a non-defective circuit, while (c) corresponds to a NAND with an open and (d) to a gate with a short.*

this simple gate a logic test is effective, but in general opens resulting in an off transistor cannot be 100% detected with a Boolean test [5]. The effectiveness of $i_{dd}(t)$ testing is related to quantifying changes of the current peaks shape provoked by defects in the circuit. This can be done by monitoring the amount of charge driven into the circuit during and after the transition. The value of this charge can be expressed as:

$$Q = \int_{clk} i_{dd}(t)\, dt \quad (1)$$

where clk denotes an integral during a clock period. For a non defective circuit the value of the charge at a given transition ($Q_{no\,def}$) will range within a given margins that are characteristics of the circuit ($Q^{min}_{no\,def} < Q_{no\,def} < Q^{max}_{no\,def}$). $Q^{min}_{no\,def}$ is the minimum charge driven into the non defective circuit during any transition and $Q^{max}_{no\,def}$ is the maximum value it can reach. The amount of charge driven into the circuit when a defect preventing current is sensitized will be smaller than the value registered for the same transition when defect is not present ($Q_{def\,no\,leak} < Q_{no\,def}$). The detection of the defect with $i_{dd}(t)$ testing will be possible if the obtained charge lies out of the normal circuit operation values ($Q_{def\,no\,leak} < Q^{min}_{no\,def}$).

Defects raising the static current of the circuit can be also detected by monitoring the charge. Figure 1.d shows the current behavior of a NAND gate when a short between the drain and the source of a n-MOS transistor is present. Because of the elevated quiescent current, the value of the charge driven into the circuit while the defect remains sensitized is much higher than when the defect is not present $Q_{def\,leak} > Q_{no\,def}$. The short will be detected if the obtained value is beyond the maximum ($Q_{def\,leak} > Q^{max}_{no\,def}$).

Some opens and parametric defects do not raise the current consumption of the circuit. They do not affect its logic behavior but may change the timing of the circuit. Generally those defects are hard to detect and delay test techniques have to be adopted. Small opens, slow transistors, or high capacitance nodes provoke a slow transition that result in big (wide) current peaks. The value of the charge driven into the circuit during this transition may be beyond the maximum limit for the normal operation. If this happens the defect can be detected with $i_{dd}(t)$.

3 A sensor for $i_{dd}(t)$ testing

Built-in current sensors (BICs) are an effective way of detecting defects and they have been proposed as a tool for I_{DDQ} testing [7]. The effectiveness of on-chip circuit sensors is expected to increase when considering dynamic measurements. External monitoring of high-speed signals present noise problems caused by the inductances inherent in the power distribution lines [8]. The induced voltage glitch is proportional to the effective inductance of the power lines (related to its length) and other effects that may limit the off-chip sensor efficiency. Built-in sensors can be placed very close to the device under test reducing these effects.

The function of the sensor proposed here is to provide a voltage value proportional to the charge driven into the circuit during a given period of time. Sensor operation is based on a modification of the Keating and Meyer principle where the current is integrated into a capacitor. The proposed circuit surveys the $i_{ss}(t)$ current although a version for $i_{dd}(t)$ can be derived. During sensor operation the ground of the device under test is connected to a virtual ground.

Because the Keating-Meyer approach considers the parasitic DUT capacitor (C_P) for measurement, the dependence of this capacitor with process deviations and the electrical state of the circuit has to be taken into account. To avoid this dependence the DUT cur-

Authorized licensed use limited to: UNIVERSITAT POLITECNICA DE CATALUNYA. Downloaded on September 13,2022 at 06:34:42 UTC from IEEE Xplore. Restrictions apply.

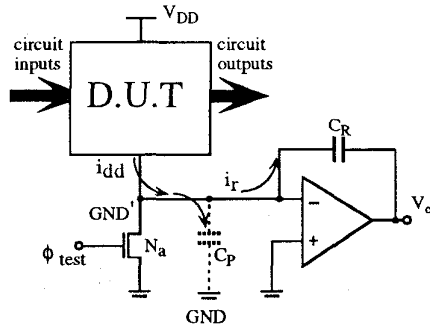

Figure 2: *Scheme of the proposed sensor.*

rent is not integrated into C_P but into a separate smaller capacitor. The value of this element is multiplied by a factor using the Miller effect so that most of the current goes into the small capacitor and not into the DUT parasitic. A major difference between a DBIC and a quiescent BIC is that the integration of dynamic current peaks occurs without raising the circuit ground voltage. In the proposed sensor, the ground induced noise is divided by the same factor that multiplies the small capacitor allowing the integration of dynamic peaks with a very small increase of the DUT GND.

3.1 Sensor operation

Figure 2 shows the scheme of the sensor. Its operation and internal structure can be found in [9]. The maximum voltage at the ground node GND$'$ in a fault free circuit during an input/output transition is $V_{GND'} = Q_{no\ def}/(1+A)C_R$. Assuming that A, the gain of the amplifier of figure 2, is high ($A >> 1$) the sensor output will range between the values [9]

$$V_{dd} - \frac{Q^{max}_{no\ def}}{C_R} < V_o^{no\ def} < V_{dd} - \frac{Q^{min}_{no\ def}}{C_R} \quad (2)$$

A defect will be detected when the output voltage of the sensor lies out of the limits defined for $V_o^{no\ def}$ in (2).

3.2 Timing considerations

In the derivation of the sensor output voltage, a high value for the op amp gain was assumed ($A >> 1$). Because of the gain dependency with the frequency ($A(w)$) a given sensor will be efficient up to a given working frequency. The value of w is not related to the clock period but to the rise and falltime of inputs and the clock signal. For high values of w the op amp gain can eventually drop to values next to 1 degrading the circuit operation. The sensor efficiency can be quantified defining the efficiency coefficient $E(w)$ as

$$E(w) = \frac{A(w)}{1+A(w)} \quad (3)$$

The value of $E(w)$ ranges between 0 and 1, the closer its value to 1 the higher the sensor efficiency. The output voltage of the sensor can be expressed as

$$V_o = V_{DD} - \frac{E(w)}{C_R}Q \quad (4)$$

When $E(w)$ is close to zero the second term in (4) remains small even when the value of the charge is big, and the output voltage of the sensor remains close to V_{DD}. The effect of a small $E(w)$ can be compensated in design by choosing a low value for C_R, but its minimum value is determined by the maximum noise induced at the DUT ground node during the test mode.

The time required by the sensor to reach a steady value after the integration of each current peak is related to the op amp switching speed defined by its slew rate (SR). A delay time for the sensor (t_{sen}) can be defined as:

$$t_{sen} = \frac{V_{DD} - \frac{Q^{max}_{no\ def}}{C_R}}{SR} \quad (5)$$

3.3 Sensor Operation Testing Modes

In this section we present two different testing modes depending on the DUT speed operation and the sensor efficiency. The proposed techniques are the *Single Period Testing Mode* (SPTM) and the *Average Period Testing Mode* (APTM).

3.3.1 Single Period Testing Mode (SPTM)

In this mode a charge evaluation within each clock period is performed. This is possible when the sensor efficiency is high ($A(w) >> 1$) and the DUT testing speed is within a given margin defined below. SPTM allows an on-line test so that no TPG effort is required. An additional circuit to process the value of the sensor is connected to its output. Such a module can be an ADC if the numeric value of the charge is required, or a simple circuit providing a pass/fail signal. In this work we use a small circuit with a reduced delay, a Level Comparator Block (LCB) which determines if V_o remains into the correct circuit operation margins. Figure 3 shows the internal configuration of the LCB. The output of the sensor V_o is connected to two smith

Authorized licensed use limited to: UNIVERSITAT POLITECNICA DE CATALUNYA. Downloaded on September 13,2022 at 06:34:42 UTC from IEEE Xplore. Restrictions apply.

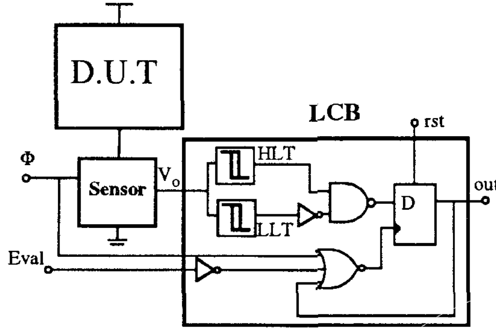

Figure 3: *Internal configuration of the LCB circuit.*

trigger circuits, HLT and LLT. The function of HLT (High Level Trigger) is to detect when the sensor output goes below V_o^{max}. If $V_o > V_o^{max}$ after the signal $Eval$ goes to 1 (i.e. after the sensor output has reached its steady value), then the output of the sensor is out of the specified limits. In this case the output of HLT is zero and the D-latch captures the high level output of the NAND gate indicating that a defect has been sensitized. The function of LLT is similar detecting when the sensor output is below the minimum limit V_o^{min}. The maximum DUT testing speed for SPTM is determined by the sensor and LCB delays (t_{sen} and t_{LCB}) and also the time required to set the sensor output to V_{DD} (t_{rst}). The following relation has to hold for t_{clk}, the clock period of the DUT

$$t_{sen} + t_{LCB} + t_{rst} \leq \frac{t_{clk}}{2} \tag{6}$$

Figure 4 illustrates the sensor timing operation for SPTM. After each clock transition the current peak is integrated. The sensor output V_o is stable for a time t_{sen} after the clock transition. The signal $Eval$ is activated and the LCB block processes the data. At a time t_{rst} before the next clock transition arrives Φ goes high setting the sensor output to V_{DD}. A feedback from the LCB output is added so that when a defect is detected the test fail signal does not go low until the reset is activated.

3.3.2 Average Period Testing Mode (APTM)

When the sensor efficiency is low ($A(w) \simeq 1$) the change in V_o after a single peak has been integrated is too small to be detected by the LCB. In this case instead of quantifying the charge of a single peak, the integration of a set of peaks is considered. The sensor remains in the test mode ($\Phi = 0$) while a sequence of

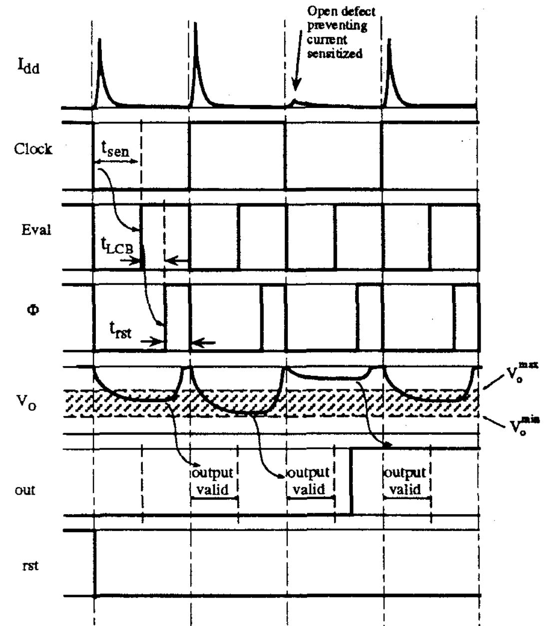

Figure 4: *Timing diagram of the sensor and LCB.*

test vectors is applied to the circuit. If n is the number of test vectors applied to the circuit, the output of the sensor for a non defective circuit at the end of the test sequence will be:

$$V_o = V_{DD} - \frac{E(w)}{C_R} \sum_{i=1}^{n} Q_i \tag{7}$$

where Q_i is the value of the charge driven into the circuit when the ith test vector (T_i) is applied. The sensor output will be considered correct if the voltage is within the interval $V_o \pm \Delta V_{tol}$, ΔV_{tol} being the output margin related to process variations.

Test vectors have to be derived trying to sensitize the defect as many times as possible. If a defect driving a charge Q_i^{def} is sensitized by the vector T_i, the difference in the charge value between the fault free circuit (Q_i) and the defective one will be $\Delta Q_i^{def} = Q_i - Q_i^{def}$. This value will be negative when the defect causes a leakage and positive if the defect prevents current. If a defect is not sensitized then $\Delta Q_i^{def} = 0$. The difference between the output voltage in a fault free circuit and a defective one ΔV_o will be

$$\Delta V_o = -\frac{E(w)}{C_R} \sum_{i=1}^{n} \Delta Q_i^{def} \tag{8}$$

the defect will be detected if $| \Delta V_o | > \Delta V_{tol}$.

Authorized licensed use limited to: UNIVERSITAT POLITECNICA DE CATALUNYA. Downloaded on September 13,2022 at 06:34:42 UTC from IEEE Xplore. Restrictions apply.

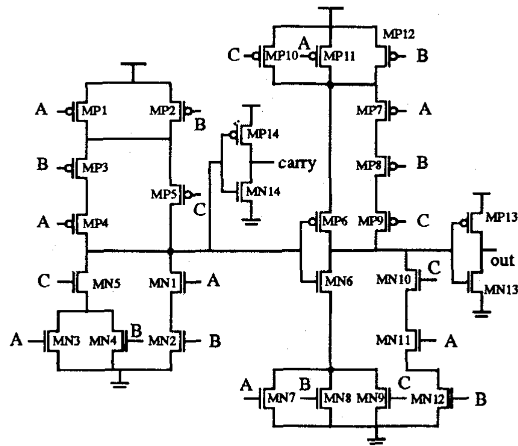

Figure 5: *Full-adder circuit used for $i_{dd}(t)$ testing.*

When using APTM the evaluation of the sensor output (signal *Eval*) has to be activated after all the test vectors have been applied to the circuit.

4 A case study

In this section we apply the proposed sensor to the full-adder of figure 5. An exhaustive study for preventing current defects (PCD) and raising current defects (RCD), by simulating the behavior of the circuit surveyed by the sensor with HSPICE was carried out for a SPTM. For PCDs we considered open defects in single transistors that prevent the device from turning on. The open defect was simulated by substituting the device with an ideal current source having a zero current value. In the simulation of RCDs we considered single transistor shorts, that were modeled using a 200 Ω resistor. The effect of opens raising the quiescent current will be similar to that induced by shorts with a different quiescent current value.

4.1 PCD Results

Testing PCDs is related to the detection of missing current peaks. Because current peaks appear during the input/output transitions, test vectors are calculated in order to induce a given transition into the circuit rather than setting determined nodes to DC values. For this reason we will refer to *State Transition Test Vectors* (STTV). A STTV will be effective if during the transition it induces a current path in the fault free circuit that is missing in the defective one because of the open. For the full-adder circuit

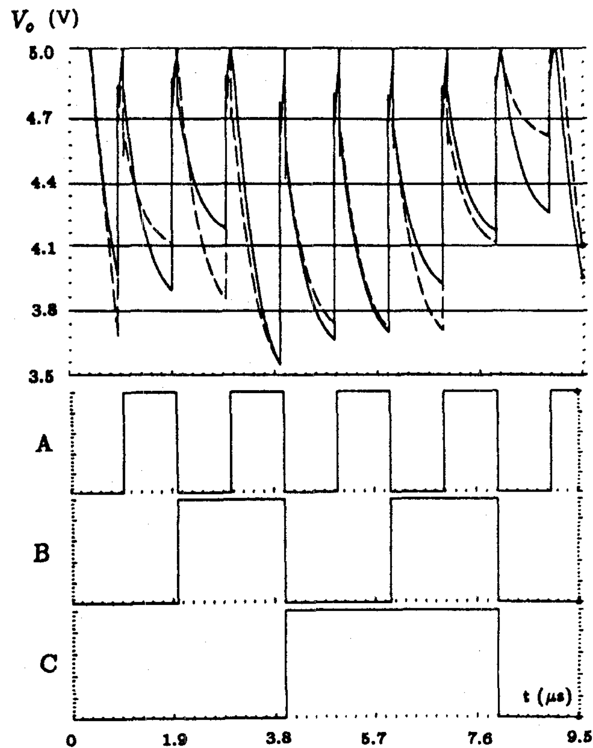

Figure 6: *Comparison of the sensor output for a defect-free full-adder (solid line) and with an open in transistor MP8 (dashed line). The defect is detected after STTV 8.*

we have considered the eight STTVs shown in figure 6 (each transition of A corresponds to a single STTV). The sensor limits for a non defective behavior are $3.50V < V_o < 4.40V$.

A comparison of the sensor output for a good circuit (solid line) and when an open at MP8 is present (dashed line) is also shown in fig. 6. For the defective case the sensor output remains out of the specified limits after STTV 8. Table 1 reports the results for all single transistor opens, showing which STTV detects each open. Six of the 28 considered defects (12 %) remain undetected: transistors MN2, MN3, MN4, MN8, MP3 and MP12. From the circuit schematic it is clear that an open in MN8 should be detectable because MN7 is detected (its relative position depends on the circuit layout). The same occurs for the device pairs MN2 and MN1, MP3 and MP4, MP11 and MP12. The reason why MN7 is detected and MN8 not is that the considered sequence does not properly sensitize it. Choosing an appropriated STTV that open was detected, and extending this to the other cases, the coverage was raised from 88 % to 91 %.

Authorized licensed use limited to: UNIVERSITAT POLITECNICA DE CATALUNYA. Downloaded on September 13,2022 at 06:34:42 UTC from IEEE Xplore. Restrictions apply.

Op.\STTV	N 1	N 2	N 3	N 4	N 5	N 6	N 7	N 8	N 9	N 10	N 11	N 12	N 13	N 14
1														
2							x							
3						x								x
4	x													
5														
6							x		x				x	
7	x				x									
8										x	x	x		

Op.\STTV	P 1	P 2	P 3	P 4	P 5	P 6	P 7	P 8	P 9	P 10	P 11	P 12	P 13	P 14
1														
2														
3	x	x		x		x	x		x		x		x	x
4					x									
5														
6		x			x					x	x		x	
7														
8						x	x	x						

Table 1: Detection of the opens using the considered STTV

4.2 RCD Results

The condition required to detect RCDs is the same for $i_{dd}(t)$ and I_{DDQ}. For the considered circuit all the shorts may be sensitized and the quiescent current is increased in all the cases, so a 100 % coverage is achieved. Figure 7 illustrates the sensor output behavior when the static current is elevated, V_o goes below the nominal circuit operation levels. For RCDs the coverage achieved with I_{DDQ} and $i_{dd}(t)$ is the same because both methodologies survey the same observable.

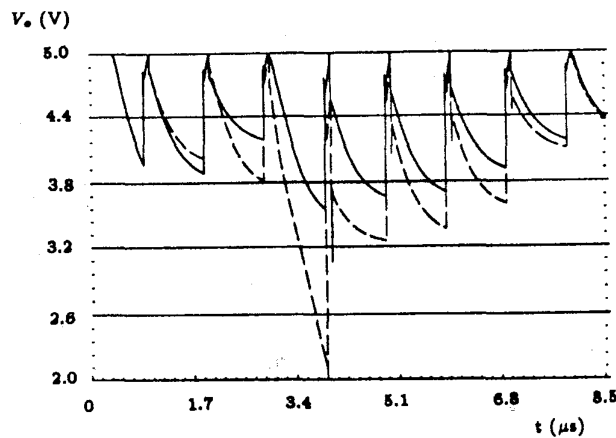

Figure 7: *Comparison of the sensor output behavior between a non defective circuit (solid line) and when the quiescent current is elevated (dashed line).*

5 Conclusions

An approach to $i_{dd}(t)$ testing has been presented, showing the principles and possibilities of such technique. By surveying the consumption current of a circuit not only in the quiescent period but during the input/output transitions, the detection of some defects not covered with I_{DDQ} can be achieved. In particular, open defects preventing current are susceptible of being detected by surveying the absence of current peaks.

A case study for a full adder circuit has been presented showing that dynamic current test vector generation allows detection levels ranging between 80-90 % while a 100% coverage is achieved for defects raising the quiescent consumption of the circuit.

Acknowledgments

We would like to express our gratitude to Charles Hawkins from the University of New Mexico for his comments and to Jim Morra from Philips Semiconductors for his support in our measurements. This work was partially supported by the CICYT project TIC-92-0666.

References

[1] S. Al-Arian, D.P. Agrawal. "Physical failures and fault models of CMOS circuits". *IEEE Tran. on Circ. and Systems*, 34(3):269–279, March 1987.

[2] C. Hawkins, J. Soden. "Electrical characteristics and testing considerations for gate oxide shorts in CMOS ICs". *Int. Test Conf.*, Nov. 1985.

[3] C. Hawkins, J Soden, R. Fritzemeier, L. Horning. "Quiescent power supply current measurement for CMOS IC defect detection". *IEEE Tran. on Ind. Electronics*, 36(2):211–218, May 1989.

[4] P. Nigh, W. Maly. "Test generation for current testing". *IEEE Design and Test of Computers*, 7(2):26–38, Feb 1990.

[5] C. Hawkins, J. Soden, A. Righter, J. Ferguson. "Defect classes - An overdue paradigm for CMOS IC testing". *Int. Test Conf.*, October 1994.

[6] S.T. Su, R.Z. Makki. "Testing of static random acces memories by monitoring dynamic power supply current". *JETTA*, 3(3):265–278, Aug. 1992.

[7] W. Maly and P. Nigh. "Built-in current testing: feasibility study". *IEEE Int. Conf. on Computer-Aided Design*, pages 340–343, November 1988.

[8] H.B. Bakoglu. *"Circuits, interconnections and packaging for VLSI"*. Addison Wesley, 1990.

[9] J.A. Segura, M. Roca, D. Mateo, and A. Rubio. "Built-in dynamic current sensor circuit for digital VLSI CMOS testing". *IEE Electronics Letters*, 30(20):1668–1669, Sept. 1994.

Authorized licensed use limited to: UNIVERSITAT POLITECNICA DE CATALUNYA. Downloaded on September 13,2022 at 06:34:42 UTC from IEEE Xplore. Restrictions apply.