Constant Common-Mode Voltage Strategies Using Sigma-Delta Modulators in Five-Phase VSI

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***Abstract*—This paper proposes and studies different sigma-delta ($\Sigma\Delta$) modulation strategies for obtaining a constant common-mode voltage (CMV) by eliminating the CMV level transitions in a five-phase voltage source inverter (VSI). These techniques are based on choosing vectors that generate a constant CMV with values of 0.1V_{dc} or –0.1V_{dc}. Because of the high-switching frequencies used with wide-bandgap semiconductors, pulse-width modulation (PWM) techniques continually generate high dv/dt values. Therefore, the proposal to combine a $\Sigma\Delta$ modulation strategy with vector selections achieves: 1) a constant CMV level due to the elimination of its level transitions; 2) a reduction in conducted electromagnetic interference; and 3) a high-efficiency converter operation. The average number of switching per transistor of the VSI is analyzed using the results from Matlab/Simulink and PLECS simulations. Experimental results are obtained by applying the proposed $\Sigma\Delta$ modulation strategies on a VSI with silicon carbide (SiC) MOSFETs. The results demonstrate the achievement of the aforementioned features.**

***Index Terms*—Common-mode Voltage, Five-phase VSI, Power Losses, Sigma-Delta Modulation, Total Harmonic Distortion, Wide-bandgap devices.**

I. Introduction

NOWADAYS, multiphase systems have become an attractive option in high-power industrial applications, electric traction, and renewable energy generation [1], [2]. Compared to conventional three-phase systems, multiphase systems offer more degrees of freedom, higher reliability, lower current per phase, and better fault tolerance [3], [4].

Voltage source inverters (VSIs) are frequently used to drive multiphase systems. Fig. 1 shows the basic structure of a five-phase VSI based on wide-bandgap (WBG) semiconductors. In recent years, the use of WBG semiconductors has enabled engineers to design VSIs with high power density, high efficiency, and fast operating dynamics, due to the fact that WBG semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) can operate at high temperatures, high frequencies, and high voltages [5], [6].

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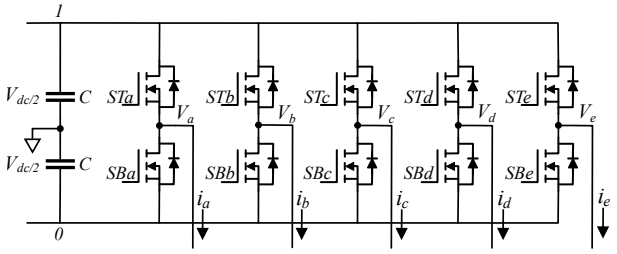


Fig. 1: Five-phase voltage source converter.

Common-mode voltage (CMV) is affected by the switching frequency. High-frequency space vector modulation (SVM) and PWM techniques affect CMV by causing a large number of level transitions, which are linked to high dv/dt values [7], [8]. Depending on the application, high-frequency CMV can cause several issues. In motors, it can cause bearing currents, mechanical vibrations, shaft voltages, and insulation damage [9], [10]. In photovoltaic (PV) systems, because of their large capacitances, CMV can generate high-frequency common-mode currents (CMC) that lead to additional power losses, EMI issues, and distortion of output voltages and currents [11], [12].

Several research studies have been conducted to reduce or eliminate CMV. These studies include the use of advanced inverter topologies [13]–[15], filters [16] or specific modulation techniques [17], [18].

Some modulation techniques allow for reducing CMV without employing filters or advanced converter topologies, thus reducing costs and design time. In multiphase VSI, as the number of phases increases, the number of CMV levels and their transitions also increases. In the case of a five-phase VSI, the CMV has two more levels and four more transitions than those of a three-phase VSI.

Modulation techniques for reducing the CMV amplitude in a five-phase VSI can be classified into three groups, based on whether the number of CMV level transitions are: kept the same, reduced, or eliminated.

Among the modulation techniques that reduce CMV amplitude while maintaining the same number of level transitions, there are the active zero-state PWM (AZSPWM) techniques [19]; carrier-based modulations with reduced CMV (RCMV-CBM1 and RCMV-CBM2) [20], and phase-shifted PWM (PS-PWM) [21]. To achieve this reduction, AZSPWM replaces

the zero vectors with active vectors. The RCMV-CBM1 and RCMV-CBM2 techniques use two carriers of opposite phases, whereas PS-PWM uses phase-shifted carriers.

Regarding the techniques known as SVM common-mode voltage reduction 3 (SVM-CMVR3) [22], hybrid active zero-state L5M5-PWM (HAZSL5M5-PWM) [23], and sawtooth carrier-based PWM (SCPWM) [24], reduce the peak-to-peak amplitude of CMV and additionally reduce the number of level transitions. To achieve this performance, the SVM-CMVR3 technique uses the five large vectors closest to the reference vector. HAZSL5M5-PWM uses a combination of five large vectors and five medium vectors, and SCPWM uses two variants of sawtooth carriers with changing positions and phases. The discontinuous modulation techniques in [25] allow for decrementing the peak-to-peak CMV amplitude, thus reducing the number of level transitions and improving the converter efficiency as a result of eliminating one zero vector operation. The previously mentioned modulation techniques manage to reduce the peak-to-peak amplitude of CMV by 40% to 80%, regardless of whether or not the number of level transitions is reduced. However, their total harmonic distortion (THD) is higher than that of standard five-phase modulation techniques.

Techniques that eliminate CMV level transitions achieve a constant or null CMV amplitude. In [26], this performance is achieved by implementing a five-phase three-level VSI (FPTHL-NPC) and a specific switching sequence. Besides, [27] additionally applies a speed-sensorless predictive torque control (PTC-S) to a five-phase three-level VSI, whereby a CMV value of 0 V is achieved. On the other hand, implementing a predictive current control technique while applying specific vectors allows eliminating CMV level transitions and obtaining a constant CMV with a value of $0.1V_{dc}$ [28]. It is important to note that these techniques make use of advanced topologies such as multilevel converters and specific control techniques that need closing the control loop in order to achieve this behavior.

Spectrum spread modulation techniques are used in order to reduce the amplitude of high-frequency components, thus achieving low EMI content [29], [30]. The sigma-delta ($\Sigma\Delta$) modulation technique is a spread-spectrum technique implemented in power converters to achieve low EMI content [31].

In [32] and [33], the $\Sigma\Delta$ modulation technique was implemented in three-phase multilevel converters to achieve a reduction in the high-frequency components due to spreading the harmonic content across the frequency spectrum. In addition, the overall number of switching operations was reduced, leading to a decrease in switching losses.

The use of $\Sigma\Delta$ modulation is recommended for high sampling frequencies. Low sampling frequencies lead to an increase in the modulator error, thereby affecting its resolution and thus generating an output signal with low-order harmonics [34]. Another approach for increasing the resolution of $\Sigma\Delta$ modulations is using additional integrator loops. However, increasing the number of integrators can lead to destabilization of the system [35].

The performance of the hexagonal $\Sigma\Delta$ modulation technique in a three-phase converter is analyzed in [36], which shows that low-order harmonics are mitigated by the hexagonal $\Sigma\Delta$ technique operating at high switching frequencies (100 and 200 kHz) using a double-loop modulator. Furthermore, despite switching at high frequencies, the high-efficiency operation of the converter is validated.

In [37], the use of $\Sigma\Delta$ modulation for a five-phase VSI is proposed. The authors further analyze the double-loop five-phase all vector $\Sigma\Delta$ modulation technique (DL-5P-AV-$\Sigma\Delta$). This work validates the high efficiency of the converter at high frequencies while also achieving a low THD. The number of CMV level transitions during a switching period is reduced, thus also reducing the amplitude of conducted EMIs. Compared with the performance of the two large and two medium SVM technique (2L+2M SVM) [25], the results are significantly better.

The literature has so far not yet addressed the use of $\Sigma\Delta$ modulation techniques for reducing or eliminating CMV effects in five-phase converters. As mentioned before, four $\Sigma\Delta$-based modulation strategies, that can eliminate CMV level transitions thus obtaining a constant CMV level without resorting to implementing control techniques or using multilevel converters, are proposed in this paper. These strategies are applied to a five-phase converter based on SiC devices. As these devices can operate at high switching frequencies, good resolution in the $\Sigma\Delta$ modulator loops can be achieved. Each proposed modulation strategy implements a set of vectors (switching states) that generate the same CMV level. In [37], a reduction in the number of level transitions was achieved. However, the amplitude of CMV level transitions is not constant due to the fact that it depends on the applied vector. In the proposed modulation strategies, the CMV level transitions are completely eliminated, thus achieving a constant CMV amplitude. This feature allows for an improved performance of the proposed modulation strategies concerning conducted EMI and CMC. Regardless of the reduction in the number of vectors used by each modulation strategy, high-efficiency converter operation and low THD voltage are achieved. To summarize, the proposed modulation strategies allow for:

- A constant CMV value by eliminating level transitions.
- A decrease in conducted EMI and CMC amplitudes.
- High efficiency converter operation.

The obtained simulation results allow for analyzing the average number of switching operations per SiC MOSFET when using single-loop and double-loop $\Sigma\Delta$ modulators. The experimental results have been used for the analysis of THD, efficiency, CMV waveform, and conducted EMI of the converter under each proposed modulation strategy.

The rest of this paper is organized as follows. Section II introduces the basis of the decision algorithm and describes the set of chosen vectors in each of the modulation strategies. Section III shows the simulation and experimental results obtained from a five-phase SiC VSI. Section IV discusses the obtained results. Finally, Section V summarizes the conclusion of this paper.

II. $\Sigma\Delta$ MODULATION TECHNIQUES WITH CONSTANT CMV

SVM techniques are frequently implemented to drive five-phase systems because they facilitate choosing the proper

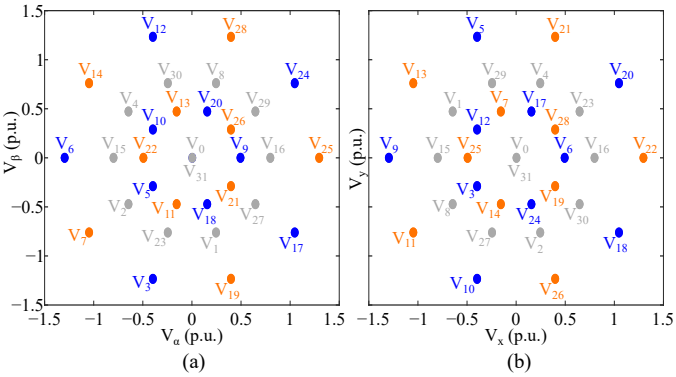


Fig. 2: Five-phase 2-D subspaces: (a) α-β, and (b) x-y subspace. The orange vectors generate a CMV value of $0.1V_{dc}$, and the blue vectors generate a CMV value of -$0.1V_{dc}$.

vectors (switching states) and the switching sequence that will provide the system with the required performance. However, to simplify the choice of vectors and switching sequence, decoupling transformations such as the Clarke transformation (1) are applied. These transformations generate two 2-D subspaces, as shown in Fig. 2.

$$C_{T5} = \frac{2}{5}\begin{bmatrix} 1 & \cos(\varphi) & \cos(2\varphi) & \cos(3\varphi) & \cos(4\varphi) \\ 0 & \sin(\varphi) & \sin(2\varphi) & \sin(3\varphi) & \sin(4\varphi) \\ 1 & \cos(3\varphi) & \cos(\varphi) & \cos(4\varphi) & \cos(2\varphi) \\ 0 & \sin(3\varphi) & \sin(\varphi) & \sin(4\varphi) & \sin(2\varphi) \\ 1/2 & 1/2 & 1/2 & 1/2 & 1/2 \end{bmatrix} \quad (1)$$

where $\varphi = 2\pi/5$.

The two subspaces are composed of 32 vectors divided into 10 small, 10 medium, 10 large, and 2 zero vectors. The first subspace, called α-β, contains the harmonics of order $10k \pm 1$ ($k = 0, 1, 2, 3, \ldots$). The second subspace, called x-y, contains the harmonics of order $10k \pm 3$ ($k = 0, 1, 2, 3, \ldots$). The large vectors in the α-β subspace are represented as small vectors in the x-y subspace. On the other hand, the small vectors in the α-β subspace are represented as large vectors in the x-y subspace. Each vector is represented by a five-digit binary code. The leftmost bit corresponds to the switching state of VSI leg a, whereas the rightmost bit corresponds to the switching state of VSI leg e. Each leg's switching state is represented by 0 or 1, indicating the output voltage levels $\frac{-V_{dc}}{2}$ and $\frac{V_{dc}}{2}$, respectively, in terms of the midpoint of the DC bus, as shown in Fig. 1.

The value of CMV can be understood as a function of the switching states of each leg of the inverter, as follows [19]:

$$V_{CM} = \frac{V_{dc}}{5}(S_a + S_b + S_c + S_d + S_e) - \frac{V_{dc}}{2} \quad (2)$$

where V_{CM} is the CMV value; S_i is the inverter leg's switching states, being $i = \{a, b, c, d, e\}$; and V_{dc} is the DC bus voltage. Table I summarizes the CMV values according to the applied vector. Thus, by applying specific vectors, a constant CMV level is achieved as the level transitions are eliminated. The modulation strategies proposed in this work are based on using large and small vectors that generate constant CMV values of –$0.1V_{dc}$ and $0.1V_{dc}$. Fig. 2 shows the vectors implemented in the proposed modulation techniques. The vectors in orange generate a CMV with a value of $0.1V_{dc}$, while the vectors in blue generate a CMV of –$0.1V_{dc}$. Because of the use of large vectors, the range of the linear operation will be wider than when using medium vectors.

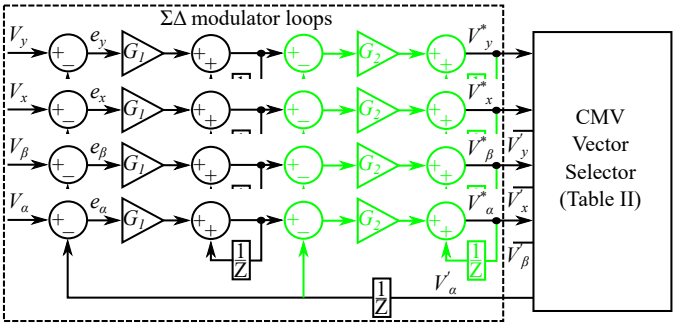


Fig. 3: ΣΔ modulator loops. The green line shows the second integrator-loop for the double-loop ΣΔ modulator. The value of both G_1 and G_2 is 0.9.

TABLE I: CMV value according to the applied vector.

Vectors,V_j (switching states)	CMV value
V_{31}(11111)	$+0.5V_{dc}$
V_{15}(01111), V_{23}(10111), V_{27}(11011), V_{29}(11101), V_{30}(11110)	$+0.3V_{dc}$
V_7(00111), V_{11}(01011), V_{13}(01101), V_{14}(01110), V_{19}(10011), V_{21}(10101), V_{22}(10110), V_{25}(11001), V_{26}(11010), V_{28}(11100)	$+0.1V_{dc}$
V_3(00011), V_5(00101), V_6(00110), V_9(01001), V_{10}(01010), V_{12}(01100), V_{17}(10001), V_{18}(10010), V_{20}(10100), V_{24}(11000)	$-0.1V_{dc}$
V_1(00001), V_2(00010), V_4(00100), V_8(01000), V_{16}(10000)	$-0.3V_{dc}$
V_0(00000)	$-0.5V_{dc}$

A. Five-phase ΣΔ modulation technique

The operations of the ΣΔ modulation strategies proposed in this paper are based on those applied to a five-phase VSI in [37]. Four ΣΔ modulating loops are implemented to track the reference vector in the α-β and x-y subspaces. The output of the ΣΔ modulator loops is connected to a quantizer, which uses a nearest-vector algorithm to select the vector to be applied in order to follow the reference vector.

First, ΣΔ modulator loops compare the position of the reference vector in both subspaces (V_α, V_β, V_x, and V_y) with the current output of the quantizer (V'_α, V'_β, V'_x, and V'_y). The resulting error is integrated and then introduced into the quantizer (V^*_α, V^*_β, V^*_x, and V^*_y). Fig. 3 shows the ΣΔ modulator structure. The values of gains G_1 and G_2 are both 0.9.

Second, the quantizer uses a nearest-vector algorithm to calculate the distance between the quantizer inputs (V^*_α, V^*_β, V^*_x, V^*_y) and the position of the vectors in the α-β and x-y (V'_α, V'_β, V'_x, V'_y) subspaces as follows:

$$D^2_{\alpha\beta j} = (V'_{\alpha j} - V^*_\alpha)^2 + (V'_{\beta j} - V^*_\beta)^2 \quad (3)$$

$$D^2_{xyj} = (V'_{xj} - V^*_x)^2 + (V'_{yj} - V^*_y)^2 \quad (4)$$

where $D^2_{\alpha\beta j}$ and D^2_{xyj} are the squared distances from the $\Sigma\Delta$ modulator loop outputs (V^*_α, V^*_β, V^*_x, V^*_y) to each j vector position ($V'_{\alpha j}$, $V'_{\beta j}$, V'_{xj}, V'_{yj}). $D^2_{\alpha\beta j}$ and D^2_{xyj} are calculated instead of $D_{\alpha\beta j}$ and D_{xyj} in order to simplify the implementation of the nearest-vector algorithm by avoiding the square root operation.

Third, the quantizer calculates the total distance as follows:

$$D_j = D^2_{\alpha\beta j} + D^2_{xyj} \tag{5}$$

where D_j is the sum of the squared distances for each vector.

Finally, the vector with the minimum total distance is selected as follows:

$$V_j = min\{\hat{D}_j\} \tag{6}$$

where V_j is the vector with the minimum distance value. In addition, the algorithm feeds back the $\Sigma\Delta$ modulator loops with the coordinates of the chosen vector (V'_α, V'_β, V'_x, and V'_y).

The switching frequency marks a notable difference between SVM techniques and $\Sigma\Delta$ modulations. Because the switching frequency is variable in $\Sigma\Delta$ modulation techniques, it is necessary to set a maximum switching frequency (f_{max}) parameter in order to compare the performance of $\Sigma\Delta$ and SVM modulation techniques, which is done as follows:

$$f_{max} = \begin{cases} f_{sw} & \text{for 2L+2M SVM} \\ f_s/2 & \text{for } \Sigma\Delta \text{ modulations} \end{cases} \tag{7}$$

where f_{sw} is the switching frequency and f_s is the sampling frequency.

B. Constant CMV strategies

These four proposed $\Sigma\Delta$ modulation strategies are based on choosing the vectors that eliminate the CMV level transitions and keep the CMV amplitude constant, thus achieving a reduction in CMV peak-to-peak amplitude of 100%. The positive five-phase five-large vector $\Sigma\Delta$ modulation and the positive five-phase five-large five-small vector $\Sigma\Delta$ modulation (5P-5L-POS-$\Sigma\Delta$ and 5P-5LS-POS-$\Sigma\Delta$, respectively) generate a continuous CMV shape with a value of $0.1V_{dc}$. The negative five-phase five-large vector $\Sigma\Delta$ modulation and the negative five-phase five-large five-small vector $\Sigma\Delta$ modulation (5P-5L-NEG-$\Sigma\Delta$ and 5P-5LS-NEG-$\Sigma\Delta$, respectively) generate a continuous CMV shape with a value of $-0.1V_{dc}$. Fig. 4 shows the Voronoi diagram. The Voronoi diagram gives a graphical view of the vectors used by the proposed $\Sigma\Delta$ modulation strategies. Geometrically, for the vectors chosen in each proposed strategy, the maximum value of m is $(4/5)*2*cos^2(\pi/5) = 1.047$. However, due to the performance of the $\Sigma\Delta$ modulation, it is not possible to reach this value of m. As shown in the Voronoi diagram in Fig. 4, the red dashed line shows the linear operation region of the proposed modulation techniques (m = 0.8). Working outside this area of operation generates a discontinuity at the voltage output because of the fact that the number of vectors that can be applied is limited.

Depending on the operating point, using small vectors improves the quality of the output waveform because the number of switching states is increased, thus allowing a better resolution. However, in the proposed modulation techniques, using small vectors slightly decreases the efficiency of the converter because for each change between neighboring small vectors, four legs have to change their state simultaneously.

Table II summarizes the main characteristics of these modulation strategies.

TABLE II: Summary of the characteristics of the proposed five-phase constant CMV $\Sigma\Delta$ modulation techniques.

Modulation techniques	Switching states (Vectors)	CMV level	Max. number of level transitions[1]	Linear region
5P-5L-POS-$\Sigma\Delta$	V_7, V_{14}, V_{19}, V_{25}, V_{28}	$0.1V_{dc}$	0	m $\leq$ 0.8
5P-5LS-POS-$\Sigma\Delta$	V_7, V_{11}, V_{13}, V_{14}, V_{19}, V_{21}, V_{22}, V_{25}, V_{26}, V_{28}	$0.1V_{dc}$	0	m $\leq$ 0.8
5P-5L-NEG-$\Sigma\Delta$	V_3, V_6, V_{12}, V_{17}, V_{24}	$-0.1V_{dc}$	0	m $\leq$ 0.8
5P-5LMS-NEG-$\Sigma\Delta$	V_3, V_5, V_6, V_9, V_{10}, V_{12}, V_{17}, V_{18}, V_{20}, V_{24}	$-0.1V_{dc}$	0	m $\leq$ 0.8

[1] Per switching period.

III. Results

Simulation and experimental results were obtained to assess the performance of the proposed modulation strategies. The simulation results were obtained through simulations performed in Matlab/Simulink and PLECS Blockset [40], [41]. The five-phase VSI was modeled in PLECS using the thermal model of the SiC MOSFET module FS45MR12W1M1_B1. This model uses a junction temperature of 125°C and external gate resistances R_{on} = 10 Ω and R_{off} = 5.1 Ω. These simulations have been used for analyzing the effects of using single-loop (SL) or double-loop (DL) $\Sigma\Delta$ modulators on the number of switching operations per MOSFET. Additionally, an overall power-loss analysis was performed.

On the other hand, THD, efficiency, CMV, and EMI of the proposed modulation strategies were experimentally evaluated using a five-phase VSI prototype. The results were obtained by varying the modulation index value from 0.2 to 0.7 and using 100 and 200 kHz as f_{max} values. Fig. 5 shows the experimental setup. This prototype consists of SiC MOSFET modules FS45MR12W1M1_B1. The VSI was fed by a 300 V_{dc} source connected through a LISN (10 kHz to 30 MHz frequency range). At the output of the VSI, there is an R-L load with R = 34 Ω and L = 470 μH. The modulation techniques were implemented on a dSPACE platform. The voltages and currents were measured with a high-resolution oscilloscope (1 GHz bandwidth and 4 GS/s sampling rate), a high voltage differential probe (400 MHz bandwidth), and a current probe (100 MHz bandwidth). VSI efficiency was measured using a digital power meter (1 MHz bandwidth). CMC and conducted EMIs were measured using an RF current probe (9 kHz to 30 MHz range) and an EMI receiver (9 kHz to 3 GHz range). These measurements were performed according to the standard CISPR-16-1-1 [39]. The performance of the proposed modulation techniques was compared with that of the 2L+2M SVM [25], and DL-5P-AV-$\Sigma\Delta$ [37] modulation techniques.

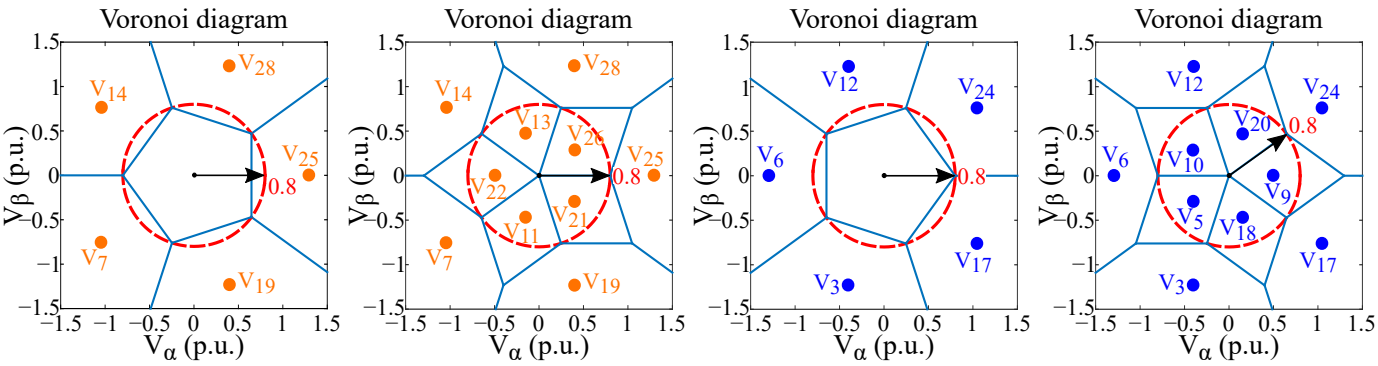


Fig. 4: Voronoi diagram: (a) 5P-5L-POS-ΣΔ, (b) 5P-5LS-POS-ΣΔ, (c) 5P-5L-NEG-ΣΔ, and (d) 5P-5LS-NEG-ΣΔ.

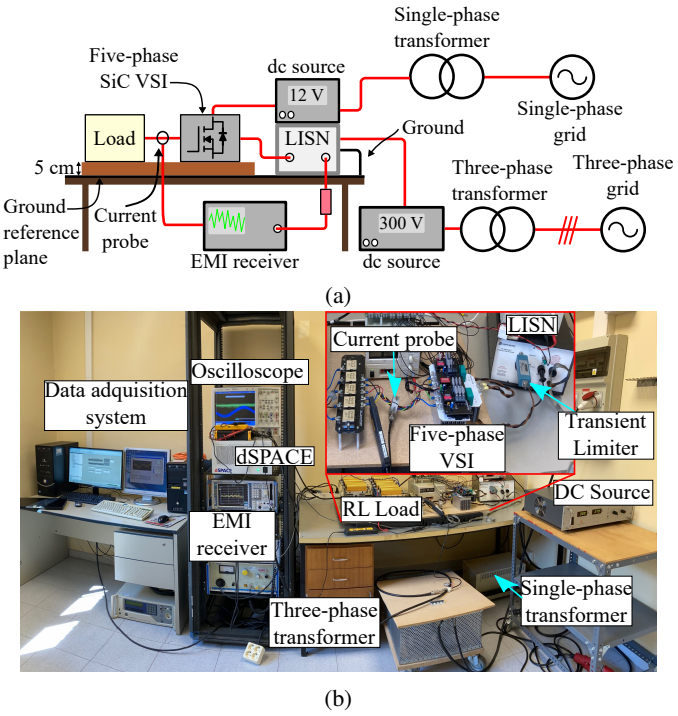


Fig. 5: Experimental setup: (a) setup schematic, and (b) implemented setup.

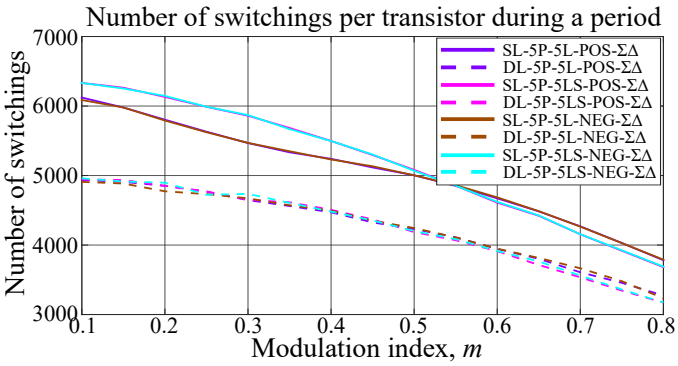


Fig. 6: Comparison of transistor switching operations during a fundamental period using single-loop and double-loop ΣΔ modulators at f_{max} of 200 kHz.

A. Study of the number of switching operations under single-loop and double-loop ΣΔ modulators.

The use of single-loop and double-loop ΣΔ modulators was analyzed on the basis of the number of MOSFET's switching operations per fundamental period. The values for G_1 and G_2 gains in the simulations are 0.9. In [37], double-loop ΣΔ modulation techniques generated more switching operations than single-loop ΣΔ modulation techniques for values of $m \leq 0.65$. In contrast, for values of $m > 0.65$, the number of switching operations for both types of modulation techniques were very similar. However, comparing to single-loop ΣΔ modulators, the use of double-loop ΣΔ modulators in the proposed modulation strategies brings a decrease in the number of switching operations between 13.4% and 22%, as shown in Fig. 6. In addition, as m increases, the number of switching operations decreases. Therefore, due to this reduction in the number of switching operations, the VSI will be more efficient when using the proposed modulation strategies with double-loop ΣΔ modulators. In order to prove the aforementioned, an overall power-loss analysis was performed through simulation by using a 12.5 A current, varying its phase angle, and a 600 V dc bus, as shown in Fig 7. It is demonstrated that the total losses decrease when double-loop ΣΔ modulators are applied due to the decrease in the number of switching operations. Therefore, the double-loop ΣΔ modulation strategies proposed have from 4 to 15% less power losses than those of single-loop ΣΔ modulation strategies.

B. THD and efficiency analysis

The line voltage THD and the inverter efficiency performance are shown in Table III, for which the first forty harmonics have been computed, as detailed in the standard EN 50160 [38]. At an f_{max} of 100 kHz, all the techniques show low THD. However, the THD for the 2L+2M SVM modulation gets worse as f_{max} increases, whereas the THD for the ΣΔ modulation techniques remains low. The resolution of the ΣΔ modulator loops increases on account of the increment of f_{max}. Furthermore, the THD improves because of the combined use of double-loop ΣΔ modulators and the increase of f_{max}. For values of $m \geq 0.7$, DL-5P-5L-POS-ΣΔ and

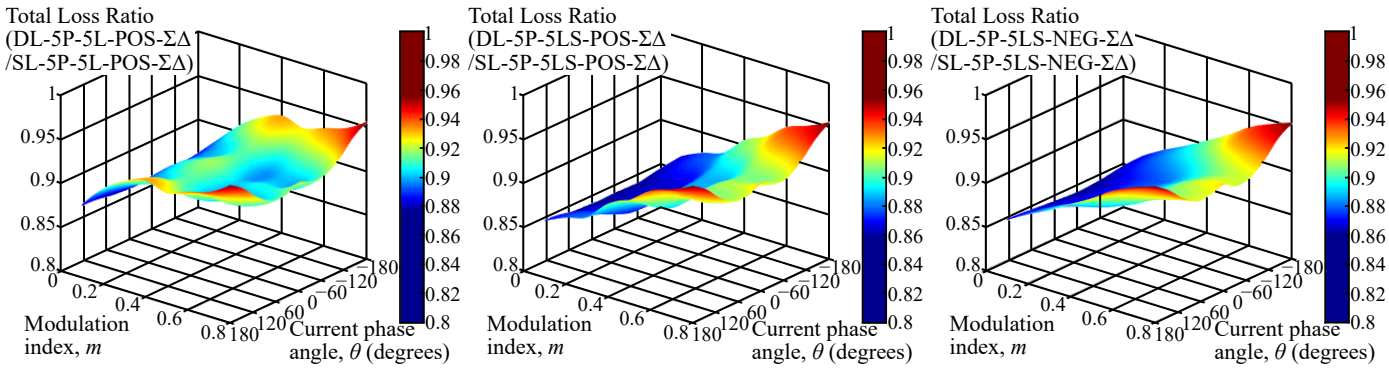


Fig. 7: Simulation ratio of total losses at 200 kHz f_{max} and 12.5 A: (a) DL-5P-5L-POS-ΣΔ and SL-5P-5L-POS-ΣΔ ratio (b) DL-5P-5LS-POS-ΣΔ and SL-5P-5LS-POS-ΣΔ ratio, and (c) DL-5P-5LS-NEG-ΣΔ and SL-5P-5LS-NEG-ΣΔ ratio.

DL-5P-5L-NEG-ΣΔ techniques yield worse THD values, as shown in Table III. However, DL-5P-5LS-POS-ΣΔ and DL-5P-5LS-NEG-ΣΔ strategies overcome this drawback by using small vectors, and generate a THD that, at high values of m, is eight times lower than that of the DL-5P-5L-POS-ΣΔ and DL-5P-5L-NEG-ΣΔ. On the other hand, using small vectors in the DL-5P-5L-POS-ΣΔ and DL-5P- 5L-NEG-ΣΔ strategies slightly reduces the efficiency of the VSI as changing between neighboring small vectors implies that four legs of the VSI must change their state simultaneously. This behavior has a significant impact on efficiency for low m values. DL-5P-5LS-POS-ΣΔ and DL-5P-5LS-NEG-ΣΔ techniques have been used to obtain the remaining experimental results in order to improve the THD in spite of the decrease in the converter efficiency. The comparison of the experimental results in terms of output voltage THD and inverter efficiency between the proposed modulation strategies and those of the 2L+2M SVM and DL-5P-AV-ΣΔ modulation techniques can be seen in Figs. 8 and 9. Table IV shows the amplitude of the low-order harmonics. ΣΔ modulation strategies present a lower amplitude of these harmonics compared to those of the 2L+2M SVM technique. This demonstrates that the proposed ΣΔ modulation strategies mitigate the presence of low-order harmonics, thus yielding a low THD.

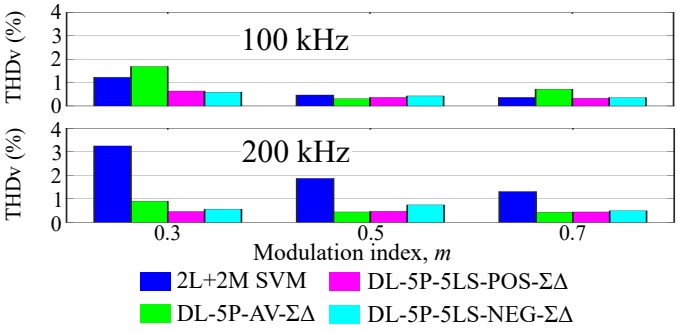


Fig. 8: Experimental line voltage THD at f_{max} of 100 and 200 kHz.

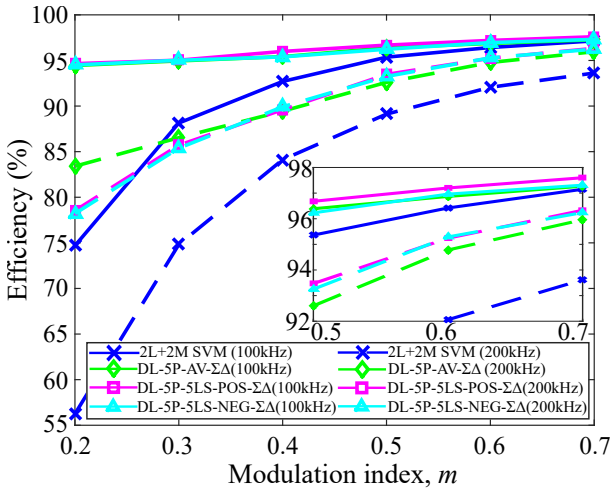


Fig. 9: Experimental converter efficiency at f_{max} of 100 and 200 kHz.

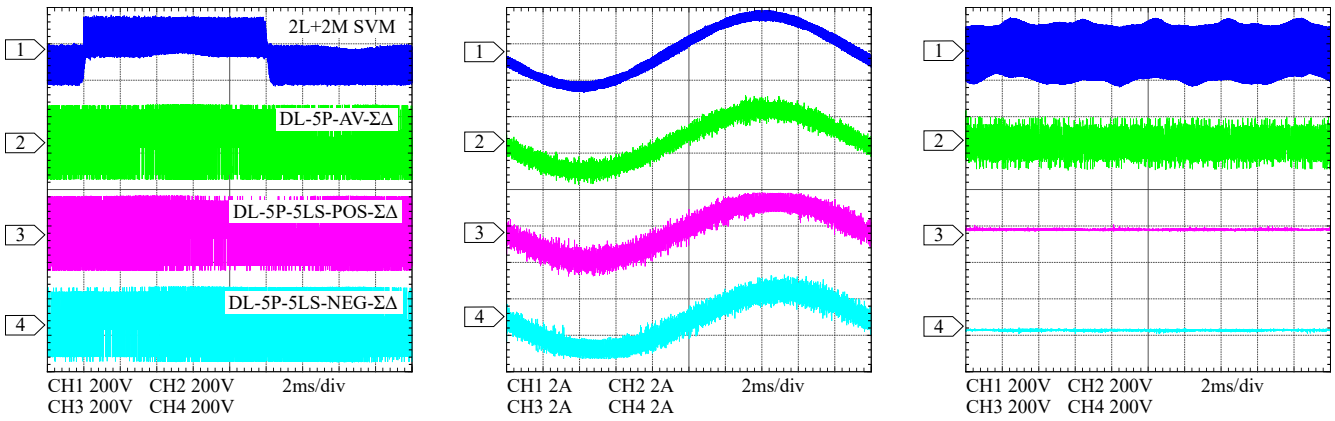
C. CMV, CMC and Conducted EMI analysis

Fig. 10 shows the line voltage, currents, and CMV waveforms of the 2L+2M SVM, DL-5P-AV-ΣΔ, DL-5P-5LS-POS-ΣΔ, and DL-5P-5LS-NEG-ΣΔ modulation techniques. Although each modulation technique has a different line voltage waveform, the output current is sinusoidal in all of them, as shown in Figs. 10a and 10b. However, DL-5P-AV-ΣΔ, DL-5P-5LS-POS-ΣΔ, and DL-5P-5LS-NEG-ΣΔ have more current ripple than 2L+2M SVM due to the increase of the mid-order harmonics.

Their most important difference can be seen in the CMV waveform, as shown in Fig. 10c. The 2L+2M SVM [25] and DL-5P-AV-ΣΔ [37] techniques have a similar CMV waveform, although the 2L+2M SVM CMV waveform presents more level transitions than the DL-5P-AV-ΣΔ modulation. On the other hand, the DL-5P-5LS-POS-ΣΔ and DL-5P-5LS-NEG-ΣΔ techniques generate a constant CMV with a value of 30 V and −30 V, respectively. These values are achieved because of the fact that the vectors used by each of these techniques generate the same CMV amplitude, and therefore, the level transitions are eliminated.

TABLE III: Experimental line voltage THD and efficiency performance.

Switching frequency (f_{max})	Modulation technique	Line voltage THD (%) Modulation index, m			Efficiency (%) Modulation index, m					
		0.3	0.5	0.7	0.2	0.3	0.4	0.5	0.6	0.7
100 kHz	2L+2M SVM [25]	1.23	0.47	0.37	74.69	88.14	92.70	95.361	96.42	97.15
	DL-5P-AV-ΣΔ [37]	1.69	0.31	0.72	94.45	94.95	95.42	96.39	96.87	97.27
	DL-5P-5L-POS-ΣΔ	1.30	1.33	3.99	94.98	95.56	96.44	97.06	97.37	97.71
	DL-5P-5LS-POS-ΣΔ	0.64	0.37	0.33	94.65	95.03	95.99	96.68	97.20	97.60
	DL-5P-5L-NEG-ΣΔ	1.33	3.46	3.82	94.79	95.10	95.99	96.63	97.08	97.46
	DL-5P-5LS-NEG-ΣΔ	0.59	0.43	0.36	94.51	95.02	95.39	96.23	96.96	97.31
200 kHz	2L+2M SVM	3.25	1.87	1.31	56.25	74.82	84.12	89.12	92.06	93.62
	DL-5P-AV-ΣΔ	0.90	0.44	0.43	83.40	86.53	89.44	92.60	94.78	95.96
	DL-5P-5L-POS-ΣΔ	0.61	0.71	3.58	80.57	86.99	90.85	93.81	95.52	96.50
	DL-5P-5LS-POS-ΣΔ	0.46	0.47	0.44	78.53	85.71	89.60	93.47	95.24	96.33
	DL-5P-5L-NEG-ΣΔ	0.66	0.45	3.51	79.79	86.14	90.46	93.51	95.43	96.43
	DL-5P-5LS-NEG-ΣΔ	0.56	0.74	0.49	78.21	85.38	89.92	93.25	95.29	96.24



(a) (b) (c)

Fig. 10: Experimental output waveforms at f_{max} = 200 kHz and m = 0.7 for 2L+2M SVM (CH1), DL-5P-AV-ΣΔ (CH2), DL-5P-5LS-POS-ΣΔ (CH3), and DL-5P-5LS-NEG-ΣΔ (CH4) : (a) line voltage, (b) current, and (c) CMV waveform.

TABLE IV: Amplitudes of low order harmonics at m = 0.7 and f_{max} = 200 kHz.

Harmonic order	2L+2M SVM	DL-5P-AV-ΣΔ	DL-5P-5LS-POS-ΣΔ	DL-5P-5LS-NEG-ΣΔ
3rd	0.56 V	0.27 V	0.25 V	0.26 V
7th	0.24 V	0.19 V	0.09 V	0.05 V
9th	0.19 V	0.11 V	0.09 V	0.10 V
11th	0.26 V	0.11 V	0.07 V	0.05 V
13th	0.18 V	0.10 V	0.06 V	0.05 V
17th	0.21 V	0.05 V	0.08 V	0.11 V
19th	0.07 V	0.05 V	0.06 V	0.06 V
21th	0.20 V	0.08 V	0.11 V	0.11 V
23th	0.11 V	0.02 V	0.09 V	0.10 V
27th	0.03 V	0.06 V	0.14 V	0.10 V
29th	0.19 V	0.05 V	0.07 V	0.13 V
31th	0.36 V	0.04 V	0.05 V	0.11 V
33th	0.14 V	0.03 V	0.04 V	0.10 V
37th	0.14 V	0.10 V	0.03 V	0.10 V
39th	0.11 V	0.04 V	0.09 V	0.06 V

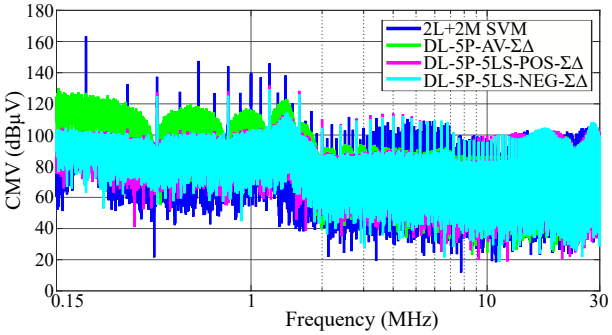


Fig. 11: Experimental CMV spectrum at f_{max} = 200 kHz and m = 0.7.

Fig. 11 shows the frequency analysis of CMV. For frequency components below 2 MHz, the proposed modulation techniques manage to reduce the amplitude of the frequency components between 5 and 30 dBμV when compared to those of the DL-5P-AV-ΣΔ, and up to a 60 dBμV reduction when compared to those of the 2L+2M SVM. However, for components whose frequencies are higher than 2 MHz, the peaks generated at multiples of f_s lead the proposed modulation techniques to still have a better performance than that of the 2L+2M SVM and similar to DL-5P-AV-ΣΔ.

Fig. 12 shows the experimental analysis of the EMIs. The ΣΔ modulation techniques reduce the maximum CMC

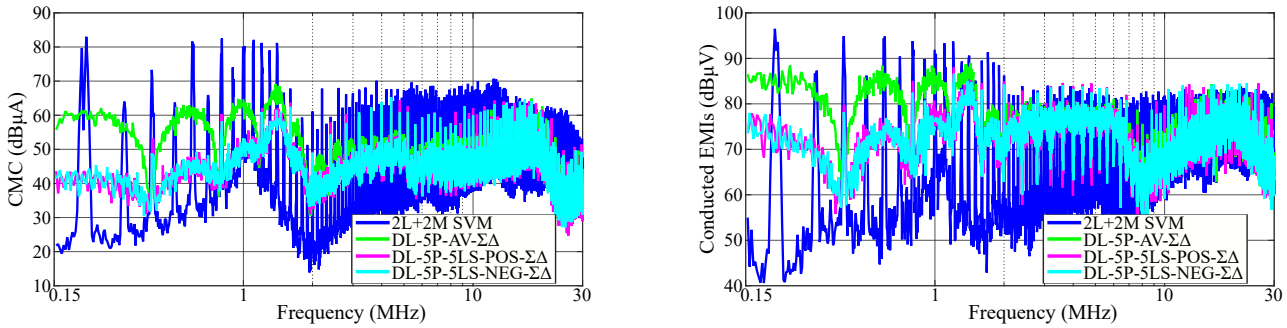


Fig. 12: Experimental EMIs analysis at f_{max} = 200 kHz and m = 0.7: (a) CMC spectrum, and (b) Conducted EMIs.

frequency components' amplitude up to 19 dBμA compared to the 2L+2M SVM technique, as shown in Fig. 12a. On the other hand, because of the CMV is constant and its level transitions are eliminated, the proposed modulation techniques have lower CMC (up to 20 dBμA less) compared to DL-5P-AV-$\Sigma\Delta$, especially for frequency components below 2 MHz. However, the DL-5P-5LS-POS-$\Sigma\Delta$ and DL-5P-5LS-NEG-$\Sigma\Delta$ CMC frequency components above 2 MHz have higher amplitude than those of the DL-5P-AV-$\Sigma\Delta$, whereas their performance is still better than the 2L+2M SVM technique. This same performance can be observed in the analysis of conducted EMIs, as shown in Fig. 12b. The DL-5P-5LS-POS-$\Sigma\Delta$ and DL-5P-5LS-NEG-$\Sigma\Delta$ techniques present better performance in the range of 150 kHz to 2 MHz, with lower EMI values. However, their performance becomes similar to that of DL-5P-AV-$\Sigma\Delta$ at frequency components above 2 MHz.

Simulation results of the implementation of the DL-5P-5LS-POS-$\Sigma\Delta$ strategy for a motor drive application are shown in Fig. 13. A five-phase permanent magnet synchronous machine (PMSM) was simulated. The control of the PMSM included field-oriented control (FOC) with a speed reference of 1500 rpm and a load torque of 1 Nm, as shown in Fig. 13a. The currents in the d_1q_1 and d_3q_3 planes (first and third-order harmonic planes, respectively) have been plotted in Fig. 13b; the currents in the x-y subspace (I_{d3} and I_{q3}) can hardly be noticed as they are zero. Fig. 13c shows the stator currents and a zoomed version of them. These currents are sinusoidal with a THD of 0.0824%. The accomplishment of a constant CMV value of 30 V (0.1 V_{dc}), thanks to the set of vectors implemented by DL-5P-5LS-POS-$\Sigma\Delta$ modulation strategy, can be observed in Fig. 13d. In Fig. 13e, the stator current spectrum is displayed. The mitigation of low-order harmonics can be noticed. This mitigation is achieved by nulling the reference values in the x-y subspace (V_x and V_y), so the DL-5P-5LS-POS-$\Sigma\Delta$ modulation strategy drives the inverter towards having an output with zero voltage in the x-y subspace. The voltage in the x-y subspace is a cause for concern in motor drive applications, as it is not opposed by the back-EMF thus causing the circulation of large harmonic currents.

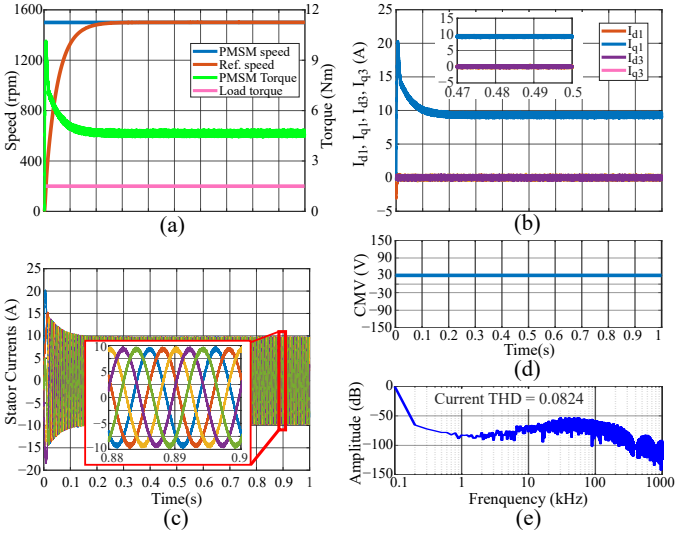


Fig. 13: Five-phase PMSM drive simulation: (a) speed and torque, (b) d_1q_1 and d_3q_3 currents, (c) stator currents, (d) CMV, and (e) stator current spectrum.

IV. Discussion

The use of double-loop $\Sigma\Delta$ modulators reduces the switching operations compared to those obtained with single-loop $\Sigma\Delta$ modulators, thus achieving less power losses and improving the converter efficiency. However, the DL-5P-5L-POS-$\Sigma\Delta$ and DL-5P-5L-NEG-$\Sigma\Delta$ techniques can compromise THD when used with m values close to 0.8 (maximum value in the linear region). To avoid this problem, DL-5P-5LS-POS-$\Sigma\Delta$ and DL-5P-5LS-NEG-$\Sigma\Delta$ techniques can be used instead, thus achieving low THD due to the use of small vectors for these m values. Apart from having better THD, their THD does not get worse when the switching frequency increases as it happens with the 2L+2M SVM technique. Therefore, when compared to the 2L+2M SVM, the DL-5P-5LS-POS-$\Sigma\Delta$ and DL-5P-5LS-NEG-$\Sigma\Delta$ modulation techniques have 3 to 4 times better THD and 2.7% to 19% better efficiency, depending on the value of m.

By eliminating CMV level transitions and generating a constant CMV, CMC and conducted EMI amplitudes decrease when DL-5P-5LS-POS-$\Sigma\Delta$ or DL-5P-5LS-NEG-$\Sigma\Delta$ modulations are used with regards to those of the DL-5P-AV-

$\Sigma\Delta$. However, at switching frequencies above 2 MHz, their conducted EMI performance is similar to that of DL-5P-AV-$\Sigma\Delta$, due to the peaks generated at the sampling frequency multiples. Therefore, according to the experimental results, the DL-5P-5LS-POS-$\Sigma\Delta$ and DL-5P-5LS-NEG-$\Sigma\Delta$ modulation strategies allow the converter to perform significantly better than standard modulation techniques do. In addition, the adverse effects generated by CMC and other conducted EMIs are reduced. Futhermore, the problems caused by CMV level transitions are eliminated.

V. Conclusion

The proposed modulation strategies implement a vector selector that generates constant CMV values of $0.1V_{dc}$ or $-0.1V_{dc}$, thereby eliminating the CMV level transitions and thus reducing the EMIs. The vector selector, combined with the use of double-loop $\Sigma\Delta$ modulators and SiC MOSFETs, allows the converter to operate at higher efficiency and lower THD than standard modulation techniques at high switching frequencies. However, the maximum linear region of operation is limited ($0 \leq m \leq 0.8$). The proposed modulation strategies demonstrate better performance than the 2L+2M SVM and the DL-5P-AV-$\Sigma\Delta$ techniques in the following aspects:

- THD improves as f_{max} increases. At 200 kHz, the THD is 3 to 5 times lower compared to that of the 2L+2M SVM strategy.
- VSI operation is between 2.7% and 19% more efficient, depending on the operating point.
- The maximum amplitude of the CMV frequency components is lowered (up to 60 dBμV reduction).
- A constant CMV with no level transitions is achieved, thus lowering the amplitude of CMC frequency components (up to 20dBμA reduction).
- Conducted EMI amplitude is reduced.

The most significant drawback of the proposed techniques is that the maximum value of m is 0.8, which is lower than with the 2L+2M SVM and DL-5P-AV-$\Sigma\Delta$ techniques (m = 1.0515). Therefore, the DC bus voltage must be increased when a higher output voltage is required.

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