POLITECNICO DI MILANO

School of Industrial and Information Engineering
Master of Science in Automotive and Industrial Engineering

POLITECNICO
MILANO 1863

ANALYSIS AND OPTIMIZATION OF THE HARDWARE DESIGN OF A SIC MOSFET BASED POWER CONVERTER WITH SIC SCHOTTKY DIODES UTILIZING A SPLIT OUTPUT TOPOLOGY

Supervisor: Prof. Francesco CASTELLI DEZZA

Co-supervisor: Ing. Nicola TOSCANI

Ing. Matteo SPOSITO

Master Thesis dissertation of:

Mikel ACELDEGUI BERNAL

Academic Year 2021-2022

Abstract

In recent years, the use of power electronic devices for energy conversion with semiconductors such as silicon carbide (SiC) or gallium nitride (GaN) are replacing silicon due to their high thermal conductivity, efficiency, resistance, and the possibility of smaller and thinner designs. For this reason, in order to evaluate the improvement potential of these systems, it is beneficial to realize experimental setups that emulate real operating conditions in order to verify the correct performance of these systems.

In this context and based on the previous work done by Giorgio Ferrara, this thesis focuses on the analysis and identification of improvements of a SiC MOSFET-based power electronic converter with the aim of suggesting and studying different solutions that ensure a high-performance operation that allows its correct implementation in motor traction and grid-connected applications.

During the thesis work, it is carried out an in-depth analysis of the voltage peaks between drain and source originated by the fast switching of the MOSFET to evaluate the use of Snubber capacitors and it is made a new hardware design of the gate driver board using isolated gate drivers to improve the dynamic behaviour in the switching transients of the SiC transistors and provide safety and robustness to the system.

Finally, maintaining the original design of the converter, it implements the split output topology to evaluate possible solutions to the problems of electromagnetic interference (EMI) and the crosstalk effect that occurs with high frequency switching.

Sommario

Negli ultimi anni, l'uso di dispositivi elettronici di potenza per la conversione dell'energia con semiconduttori come il carburo di silicio (SiC) o il nitruro di gallio (GaN) sta sostituendo il silicio grazie alla sua elevata conducibilità termica, all'efficienza, alla resistenza e alla possibilità di realizzare disegni più piccoli e sottili. Per questo motivo, al fine di valutare il potenziale di miglioramento di questi sistemi, è utile realizzare set-up sperimentali che emulino le condizioni operative reali, in modo da poter eseguire diversi test per verificare il corretto comportamento di questi sistemi.

In tale contesto e a partire dal precedente lavoro effettuato per Giorgio Ferrara, la presente tesi si concentra nell' analisi e nidentificazione di miglioramenti di un convertitore di potenza DC-AC a commutazione, al fine di proporre e studiare diverse soluzioni che garantiscano le elevate prestazioni che assicurano la sua corretta implementazione in applicazioni di trazione a motore e di connessione alla rete.

Durante il lavoro di tesi, si analizza in dettaglio il fenomeno di picchi di tensione tra drain e source causato per la commutazione veloce del MOSFET e si valuta l'utilizzo di condensatori snubber; in più si realizza un nuovo disegno hardware della board di gate driver utilizzando gate driver isolati per migliorare il comportamento dinamico nei transitori di commutazione dei transistor SiC e per fornire sicurezza e robustezza al sistema.

Per finire, mantenendo il disegno originale del convertitore, implementa la topologia di uscita Split Output per valutare possibili soluzioni ai problemi di interferenza elettromagnetica (EMI) e all'effetto diafonia che si produce con la commutazione ad alta frequenza.

Info

This master thesis has been developed at the Laboratory of Electrical Drives and Power Electronics located at the Department of Mechanical Engineer- ing.

The laboratory is managed by the Electrical Machines, Drives, and Power Electronics Research Group lead by Prof. Francesco Castelli Dezza (francesco.castellidezza@polimi.it)

Politecnico di Milano

ELECTRICAL MACHINES, DRIVES,

AND POWER ELECTRONICS RESEARCH GROUP

Department of Mechanical EngineeringBuilding B23

Campus La Masa (Bovisa)via La Masa 1

20156 Milan, Italy

https://www.mecc.polimi.it

https://www.polimi.it

The student Mikel Aceldegui BERNAL worked in the new design of the converter, being supervised by Ing. Nicola Toscani (nicola.toscani@polimi.it) and Ing. Matteo Sposito (matteo1.sposito@polimi.it). The thesis contents were studied using the hardware provided by the Electrical Machines, Drives, and Power Electronics Research Group and the university start-up ePEBB^S Srl which is sponsoring the laboratory materials to this thesis.

Thesis summary:

Author Name:	Mikel ACELDEGUI BERNAL
Title:	ANALYSIS AND OPTIMIZATION OF THE HARDWARE DESIGN OF A SIC MOSFET BASED POWER CONVERTER WITH SIC SCHOTTKY DIODES UTILIZING A SPLIT OUTPUT TOPOLOGY
Supervisor:	Prof. Francesco CASTELLI DEZZA
Co-Supervisor:	Ing. Nicola TOSCANI
	Ing. Matteo SPOSITO
Location:	Department of Mechanical Engineering
Time Duration:	9 months
Language:	English
Master of Science:	Automotive and Industrial Engineering

CONTENTS

1. INTRODUCTION……..3

1.1. Problem framing…….. 3

1.2. Main Purpose……... 5

2. SIC BASED INVERTER WITH SPLIT OUTPUT TOPOLOGY…….7

2.1. Half-bridge topology limitations……...7

2.2. Analysis of the split output converter……... 10

2.2.1. Operation of Split Output Converter……10

2.2.2. Benefits and drawbacks of the Split Output Converter……. 14

3. ANALYSIS AND OPTIMIZATION OF THE HARDWARE DESIGN……... 15

3.1. Previous Hardware Design……... 15

3.2. Analysis of the Power Unit……...17

3.2.1. DC-Link……... 17

3.2.2. Snubber Capacitors……...24

3.2.3. PSIM Model of the Power Unit…… 30

3.2.4. New Proposed PSIM Model of the Power Unit……40

3.2.5. PMDC Simulation with New Model…… 43

3.3. Analysis of the Gate Driver Unit…….. 49

3.3.1. Hardware design mistakes in the Gate Driver unit……... 50

3.3.2. Bootstrap vs Isolated Gate Driver……51

3.3.3. Selection of New Component to the Gate Driver Unit…….. 55

4. NEW HARDWARE DESIGN OF THE GATE DRIVER BOARD……...59

4.1. Schematics……59

4.2. Power calculations……77

4.3. PCB Layout Design……..80

4.4. Bill Of Materials (BOM) ……. 87

5. CONCLUSION……...91

5.1. Total Cost of the Project……... 92

5.2. Future Work…… 93

1. INTRODUCTION

This section explains the framework of the thesis, explaining the advantages of using silicon carbide semiconductors in comparison to silicon, and the main objectives to be achieved during the development of the project.

1.1. Problem framing

Power electronic devices are replacing silicon semiconductors by wide bandgap semiconductors because of their significantly improved performance. Two typologies of semiconductors are currently used in the industry, Gallium nitrate (GaN) and Silicon Carbide (SiC), both typologies are good choices but the selection of between them depends on the application where they will operate.

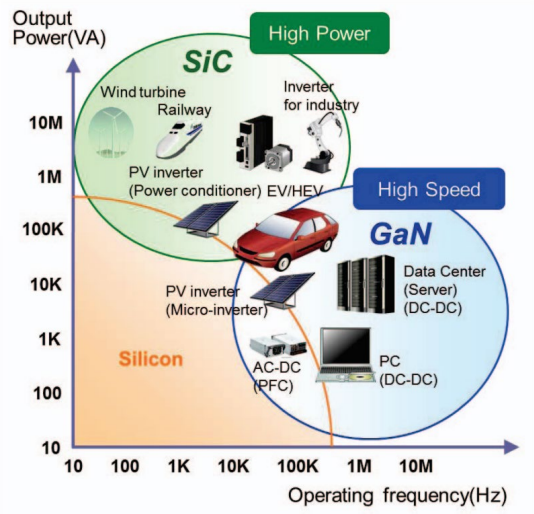


Figure 1: Potential applications of GaN and SiC power switching transistors.

The GaN typology is oriented to low power and low voltage applications, while SiC is oriented to high power and high voltage applications. Moreover, the frequency range of GaN devices is much higher due to their high electron mobility compared to SiC, which can reach up to 300 kHz. Currently GaN devices tend to be smaller than SiC, and their manufacturers are improving their performance to meet high power and high voltage applications.

This thesis focuses on the use of silicon carbide power semiconductors and their remarkable improvement in comparison to silicon (Si) based homologues. The SiC type is capable of blocking higher voltages, operating at higher junction temperatures, and obtaining lower switching and conduction losses. In addition, the frequencies achievable by SiC switches sufficiently fulfil the requirements of motor drive or grid-connected applications. On the other hand, given their high-power density and high frequency, they present problems of electromagnetic interference and crosstalk, which must be controlled and treated.

Properties	Si	4H-SiC	GaN
Crystal Structure	Diamond	Hexagonal	Hexagonal
Energy Gap : E_G (eV)	1.12	3.26	3.5
Electron Mobility : μ_n (cm^2/Vs)	1400	900	1250
Hole Mobility : μ_p (cm^2/Vs)	600	100	200
Breakdown Field : E_B (V/cm) X10^6	0.3	3	3
Thermal Conductivity (W/cm°C)	1.5	4.9	1.3
Saturation Drift Velocity : v_s (cm/s) X10^7	1	2.7	2.7
Relative Dielectric Constamt : ε_S	11.8	9.7	9.5

Figure 2: Comparison of some electrical and material properties of Si, 4H-SiC and GaN for power device applications.

The power converter to be analysed and improved is an experimental six-phase split output inverter that mounts 3 Vincotech modules with SiC MOSFETs and incorporates Schottky SiC diodes in antiparallel. This inverter topology is used to provide the necessary flexibility to test different inverter configurations with and without split output in order to show the improvements and drawbacks when a three-phase load is connected.

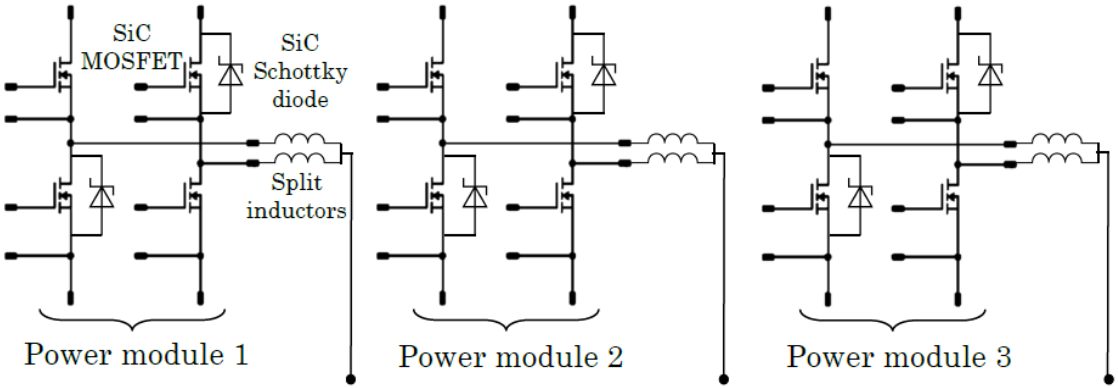


Figure 3: Six-phase Split-Output configuration with SiC Schottky diodes in antiparallel.

1.2. Main Purpose

The SiC power inverter with split output mounted in the lab was not operating correctly during the tests realized in the previous thesis project of Giorgio Ferrara. The reasons for this were a bad design of the printed circuit boards which was not designed for high power applications with SiC MOSFETs, a failure on the mechanical assembly between the board connectors and the lack of Snubber capacitors to avoid high voltage peaks which can cause device failures.

In order to improve this behaviour, the analysis and improvement of the inverter is carried out by monitoring the following points during the development of the thesis:

- Analysis and calculations of the inverter's DC bus to verify that it is correctly dimensioned. Proposal to replace the current bus DC with electrolytic capacitors, which reduce the efficiency of the system, with a MKP capacitor bus DC that provides higher performance and also reduces the system's dimensions.

- Study on the integration of Snubber capacitors in order to reduce the voltage peaks between the source-drain terminals of the MOSFETs. Different calculations are performed and the simulation software PSIM is used to validate the results and see the improvements in the inverter performance.

- Comparison between the current converter and the converter with the proposed changes using the tests realized in the previous thesis and the new PSIM simulations.

- Redesign of the gate driver board from a 2-layer to a 4-layer board. Bootstrap circuit is replaced by the integration of isolated gate drivers with multiple functionalities to provide protection and including their respective DCDC converters with positive and negative outputs. The traces were redesigned using polygons in order to decrease the parasitic inductances of the traces, avoid high temperatures and reduce electromagnetic interference (EMI) and the crosstalk effect. The position of the connectors was changed to ensure the correct mechanical assembly between the power board and the gate driver board.

- A checking of the new designed board is carried out using Eurocircuit's PCB Checker tool in order to apply changes in the design of the PCB to reduce the level of technology required to manufacture it and also to reduce its cost.

- Analysis of the cost of manufacturing and assembling all the possible changes, including the changes already made and the proposed ones.

2. SIC BASED INVERTER WITH SPLIT OUTPUT TOPOLOGY

As previously discussed, silicon carbide (SiC) power devices have great advantages in terms of material properties and are commonly used in power electronic systems to achieve high power density and high efficiency. Because of the low switching and conduction losses of these devices, they can reach frequencies of the order of kHz. These high frequencies can be interesting in applications where it is important to obtain a good wave quality and minimize THD (Total Harmonic Distortion). In other applications, such as renewable energies, where the aim is to minimize converter losses, their use is also very common.

However, SiC MOSFETs have some limitations when used in a standard half-bridge topology at high switching frequencies or when low switching and conduction losses are sought.

2.1. Half-bridge topology limitations

The standard half-bridge configuration is a classic configuration used in many power electronics applications for the realization of DC-DC converters or DC-AC inverters. This configuration is formed from two switches connected in series where, in case of using MOSFET devices, the drain of the low side switch is connected to the source of the high side switch (Figure 4).

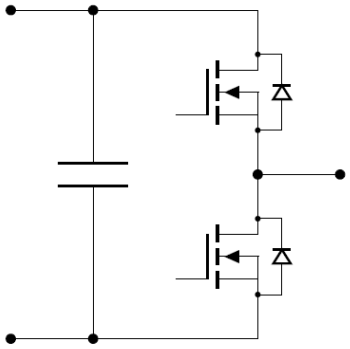


Figure 4: Standard half-bridge topology.

The main limitations of the standard half-bridge topology are switching and conduction losses due to the poor performance of the SiC MOSFET body diode, EMI problems at high frequencies and the crosstalk effect due to the high switching speed (dv/dt).

Poor-performing Body Diode

The body diode of SiC MOSFETs produces a high forward voltage drop during conduction and also does not have a very good reverse recovery charge. These poor characteristics result in high losses when using this diode as a freewheeling path: high conduction losses due to the high forward voltage drop and increased switching losses at turn-on caused by the reverse recovery charge.

To overcome these losses, the manufacturers of this type of devices suggest the use of external diodes connected in antiparallel with the SiC MOSFET. That is why SiC Schottky diodes, which have superior characteristics than the body diode, have a great relevance in this function. However, this solution of connecting diodes in antiparallel has some drawbacks: the addition of an external diode increases the total junction output capacitance (higher switching losses) and also there is no guarantee that the body diode will not conduct the freewheeling current for example in switching transients due to the effect of some leakage inductance.

A typical application to avoid conduction of the body diode of the SiC MOSFET is shown in Figure 5, where two external diodes are used: A D1 diode connected in series and a D2 diode connected in antiparallel.

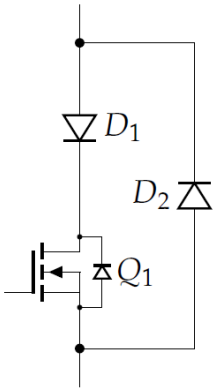


Figure 5: Typical solution to avoid the conduction of the MOSFET body by using two external diodes

This presented solution effectively avoids the body diode conduction of the SiC MOSFET, but, due to having more semiconductor devices, it increases the cost, complexity and area of the system.

Electromagnetic Interference (EMI)

One of the main limitations of SiC MOSFETs devices is the electromagnetic interference (EMI) that is caused due to the high switching speed (dv/dt) of the devices resulting in high frequency currents (di/dt) across the parasitic components of the converter. These high frequency currents produce electromagnetic interference which affects to other devices connected to the converter generating problems and system failures.

Crosstalk Effect

The high switching speed of SiC MOSFETs which cause high dv/dt can result in the crosstalk effect. This effect produces the interaction in the turn-on between MOSFETs of the same leg: when one MOSFET turns on, spurious gate voltages can be induced in the other MOSFET causing it to turn on as well. This misfire results in a simultaneous conduction of both switches that leads to a failure of the converter.

In order to avoid the conduction of the MOSFET body diode, decrease EMI and crosstalk problems, the topology of six-phase SiC MOSFET based converter with split output and external SiC Schottky diodes is used.

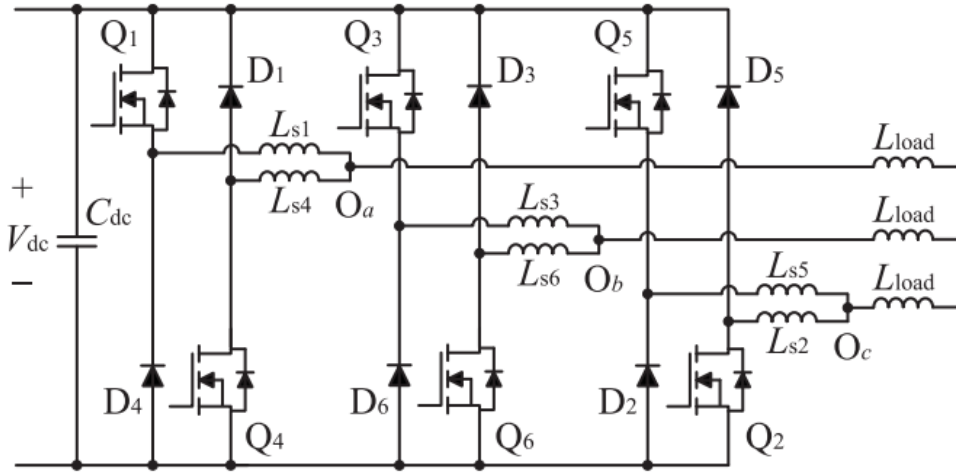
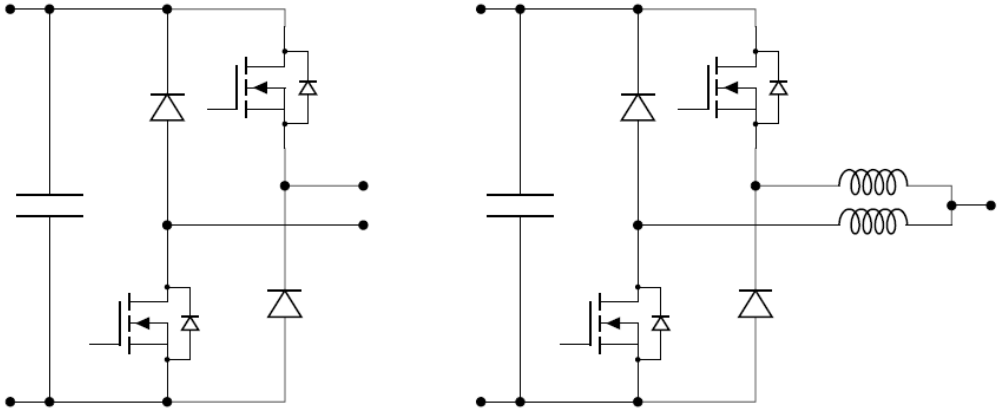


Figure 6: Six-phase split output inverter

2.2. Analysis of the split output converter

The split output topology for a half-bridge converter is shown in Figure 7.a. Instead of connecting the two MOSFETs directly in series, they are divided into two different legs by adding two diodes which results in two output terminals. On the other hand, Figure 7.b shows how to obtain a single output terminal from two inductors called split inductors connecting the two MOSFETs on the high and low side of the converter.



(a) One-leg configuration.

(b) Connection of the two switches with split inductors.

Figure 7: Half-bridge converter with split output topology

In this topology it is possible to decouple the two MOSFETs by using split inductors and provide a path for the freewheeling current through the external diodes in order to improve the converter performance.

2.2.1. Operation of Split Output Converter

To analyse the operation and the current flow in a half-bridge split output converter, the circuit in Figure 8 is considered. This circuit consists of a high value inductance connected to the output terminal L_{load}, two split inductors that decouple the MOSFETs L_{s1}, L_{s2}, two ideal external diodes for driving the freewheeling currents D_H, D_L and the MOSFETs transistors with their respective output capacitances Q_H, Q_L. Also, the converter is supplied by a constant V_{DC} voltage source, which is parallel-connected to a DC-link capacitor C_{DC}.

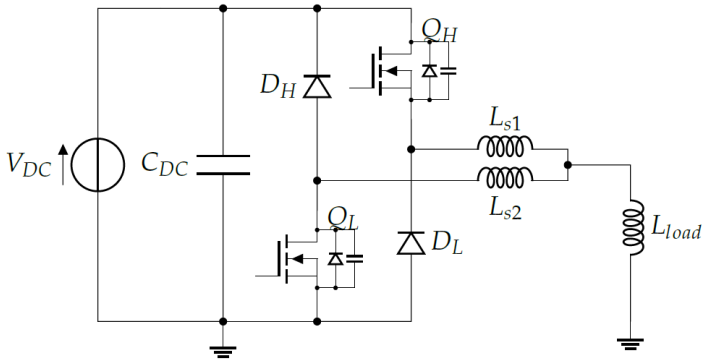


Figure 8: Half-bridge split output converter with load

In order to perform the analysis of the different converter states, the control signals S_H and S_L that drive the switching of the high side MOSFET (Q_H) and low side MOSFET (Q_L) are taken into account following the typical form of a double pulse test (DPT), a technique commonly used to validate the transient responses of power converters where is interesting to highlight the current flow in the turn-on and turn-off transitions of the switches, and also during the dead times, when both the transistors are off.

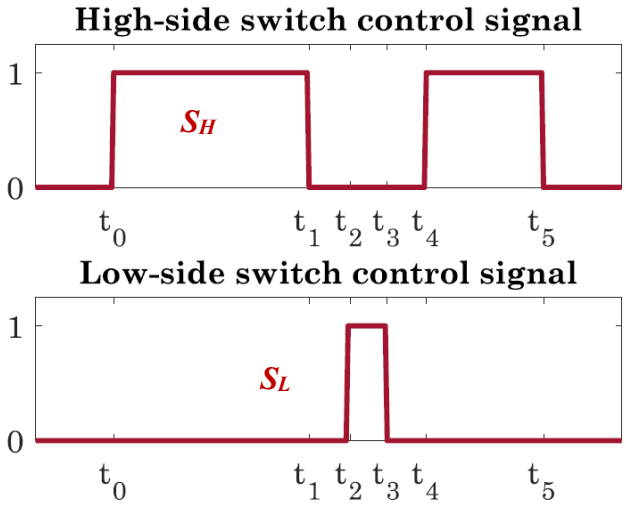


Figure 9: Control signals applied to the SiC MOSFETs (Double Pulse Test, DPT)

The double pulse test gives seven possible different states shown in the Figure 10, which are analysed in more detail to know the current flow during transients of the converter. During switch-off and switch-on transients of the switches the states are subdivided due to the charging and discharging of the output capacitors of the MOSFETs, these intermediate states are shown with an asterisk *.

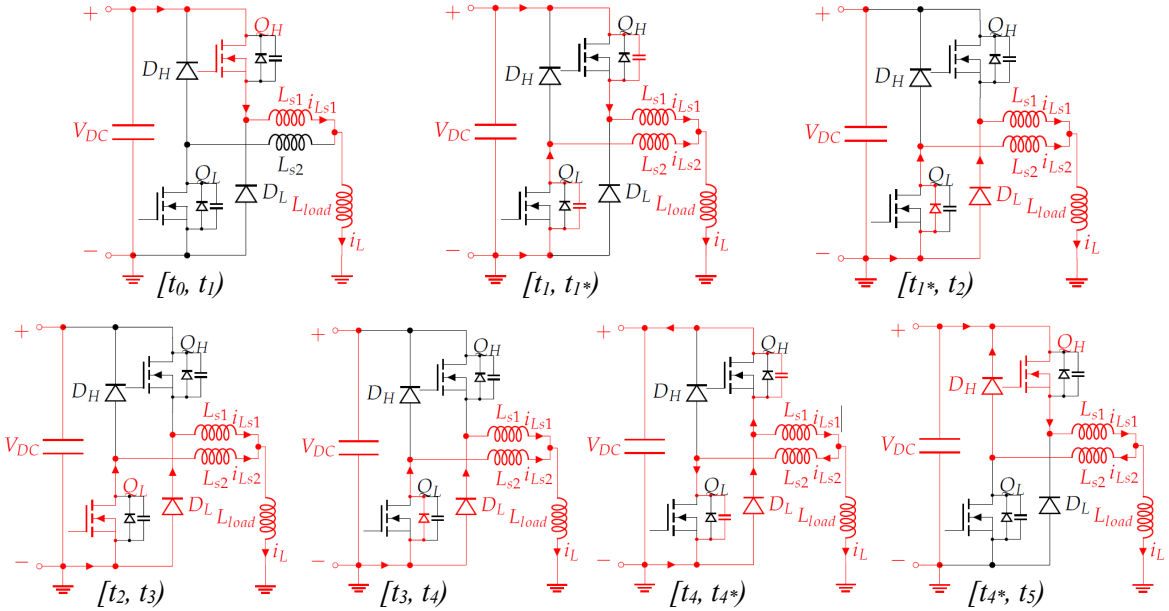
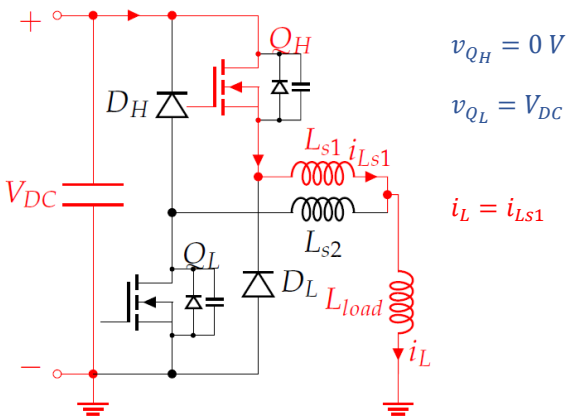


Figure 10: States of a Half-bridge split output converter in a Double Pulse Test (DPT)

Initial State [t_0; t_1)

The initial state occurs between instants t_0 and t_1. In this state the upper switch Q_H is on while the lower switch Q_L is off blocking the DC-Link voltage. Current flows from the input to the output load through the high side MOSFET and the split inductance L_{S1}. This current increases linearly until reach the desired output current.

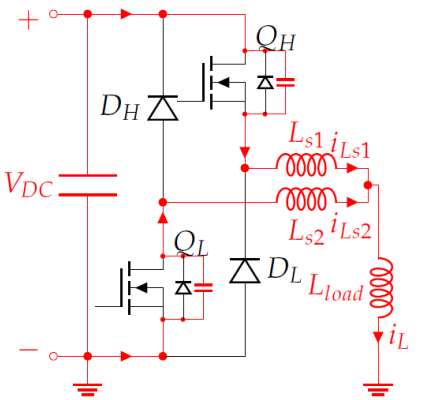


(a) Starting condition: $t \in [t_0, t_1)$

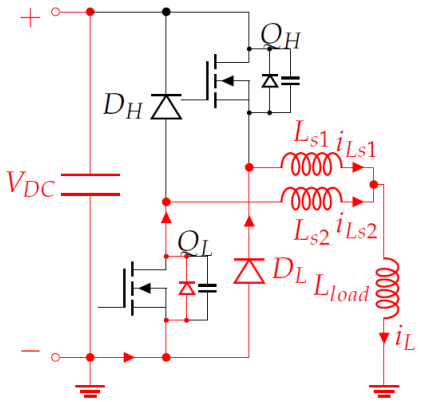
Turn off transient of QH [t_1; t_2)

At instant $t = t_1$, the control signal S_H of the high side MOSFET changes to logic 0 state initiating the turn-off transient of the MOSFET Q_H. At the beginning of the transient the output capacitance of the MOSFET Q_H which is initially discharged starts to charge through the split inductance L_{S1} and the switch voltage goes from $0\ V$ to V_{DC}. At the same time, the output capacitance of the MOSFET Q_L which was initially charged begins to discharge through the split inductance L_{S2} and the switch voltage goes from V_{DC} to $0\ V$. It should be noted that due to the small output capacitances of the MOSFETs, the charge and discharge transients are very fast.

When the processes of charging and discharging of the output capacitances of the MOSFETs are completed, the D_L diode begins to conduct the i_{Ls1} current, while the i_{Ls2} current is commutated to the low-side MOSFET Q_L body diode.



(b) Initial part of the turn off transient of Q_H: $t \in [t_1, t_1^*)$



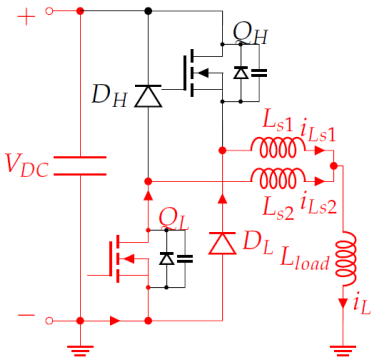
(c) Final part of the turn off transient of Q_H: $t \in [t_1^*, t_2)$

Turn on and turn off of QL [t_2; t_4)

At instant $t = t_2$, the control signal of the low side switch S_L changes to the high logic state 1, so the MOSFET Q_L starts to conduct with a soft switching of the current i_{Ls2}.

At instant $t = t_3$, the control signal of the low-side switch S_L changes to logic low state 0, so the MOSFET Q_L starts to turn off, and a soft-switching of current i_{Ls2} starts again, which the current returns to flow through the body diode of the MOSFET.

In both states, the output i_L current decreases linearly due to the application of the 0 voltage at the split inductance terminals.

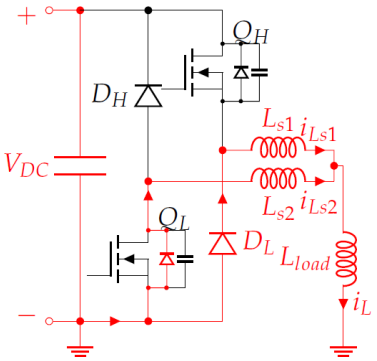


(d) Turn on of Q_L: $t \in [t_2, t_3)$

$$v_{Q_H} = V_{DC}$$

$$v_{Q_L} = 0\ V$$

$$i_L = i_{Ls1} + i_{Ls2}$$

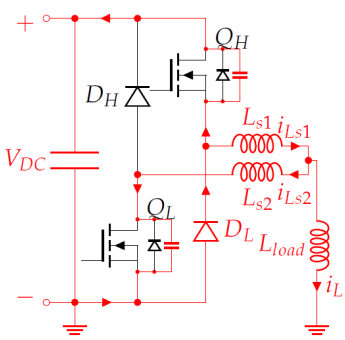


(e) Turn off of Q_L: $t \in [t_3, t_4)$

Turn on transient of QH [t_3; t_4]

In this state the high side switch control signal S_H at $t = t_4$ changes to logic 1 state initiating the turn-on transient of the MOSFET Q_H. The output capacitance of the MOSFET Q_H which initially had a voltage V_{DC} begins to discharge, and the switch voltage goes from V_{DC} to $0\ V$. Similarly, the output capacitance of the MOSFET Q_L which was initially at $0\ V$ starts to charge by reversing the current iLs2 and the switch voltage goes from $0\ V$ to V_{DC}.

When the charge/discharge processes of the output capacitances of the MOSFETs are completed, the D_L diode stops conducting and a soft switching of the current i_{Ls1} though the MOSFET Q_H is realized. Otherwise, the diode D_H starts conducting with a soft switching of the current i_{Ls2} until the energy stored in the split inductance L_{S2} is dissipated, returning to the initial state in Figure 10.a. If this dissipation does not occur due to the application of another S_H signal pulse for the MOSFET Q_H turn-off, the converter starts to operate in the state of Figure 10.b.

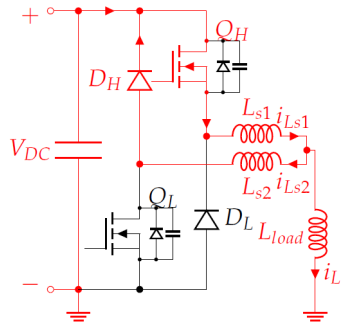


(f) Initial part of the turn on transient of Q_H: $t \in [t_4, t_4^*)$

$$v_{Q_H} = V_{DC} \rightarrow 0\ V$$

$$v_{Q_L} = 0\ V \rightarrow V_{DC}$$

$$i_L = i_{Ls1} - i_{Ls2}$$



(g) Final part of the turn on transient of Q_H: $t \in [t_4^*, t_5)$

2.2.2. Benefits and drawbacks of the Split Output Converter

The development of a new converter with the split output topology implies a series of benefits and drawbacks which are shown below (these benefits and drawbacks are studied in more depth in Giorgio Ferrara's thesis).

Benefits:

☺ The split output topology provides a path for freewheeling current through the external SiC Schottky diodes, avoiding the conduction of the MOSFET body diode and increasing the efficiency of the converter.

☺ Decoupling of the high and low side MOSFET switches by the split inductances, mitigating crosstalk effects and allowing the achievement of higher switching frequencies of the converter.

☺ Reduced generation of electromagnetic interference (EMI) thanks to the incorporation of split inductances which limit the high-frequency harmonic components of the output.

Drawbacks:

☹ The split inductors support high current pulses and large voltage drops produced by the switching of the MOSFET Q_H, furthermore, when the split inductance decreases, the amplitude of the current pulses becomes larger, and the width of the voltage pulses becomes smaller $\left(v_L = L \cdot \frac{di}{dt}\right)$. Due to this, large conduction losses are generated in the inductors at high switching frequencies.

☹ Due to the decoupling of the MOSFET switches, the synchronous rectification disappears, leading to a negative influence on the converter's conduction losses.

☹ When the converter operates in continuous conduction mode, the overall efficiency of the converter with split inductors can be lower than without them. This is because the conduction losses generated by the current pulses and voltage peaks in the split inductors can overcome the reduction in switching losses. The loss efficiency is increased at higher switching frequencies.

3. ANALYSIS AND OPTIMIZATION OF THE HARDWARE DESIGN

In this section, the previous design of the split output power converter is presented, identifying its possible failures, and proposing new improvement alternatives in order to optimize the converter's performance.

3.1. Previous Hardware Design

The previous split output converter was designed to offer flexible operating performance to test the silicon carbide technology for different circuit configurations. The design conditions followed for the inverter hardware design were as follows:

- Maximum DC voltage: $V_{DC,máx} = 1000\ V$
- Rated DC voltage: $V_{DC,N} = 700\ V$
- Rated current: $I_N = 32\ A$
- Switching frequency: $f_{sw} > 10\ kHz\ (max\ 100\ kHz)$
- Flexible topology: Allowing for different hardware configurations, including the ones featuring a split output.

The specifications for voltage and current of the system were chosen based on testing for high-performance DC-AC motor drive and AC-DC grid connection applications.

A maximum switching frequency of 100 kHz was set according to the characteristics of the silicon carbide-based semiconductors and the hardware control system's computational power.

Finally, the flexibility of the converter allows to test it in different load scenarios and also evaluate and compare the possible improvements when using or not using the split output topology.

The six-phase SiC MOSFET based converter with split output designed by Giorgio Ferrara is shown in the figure. This system shows three different units:

1. The power unit
2. The gate drive unit
3. The split inductor unit.

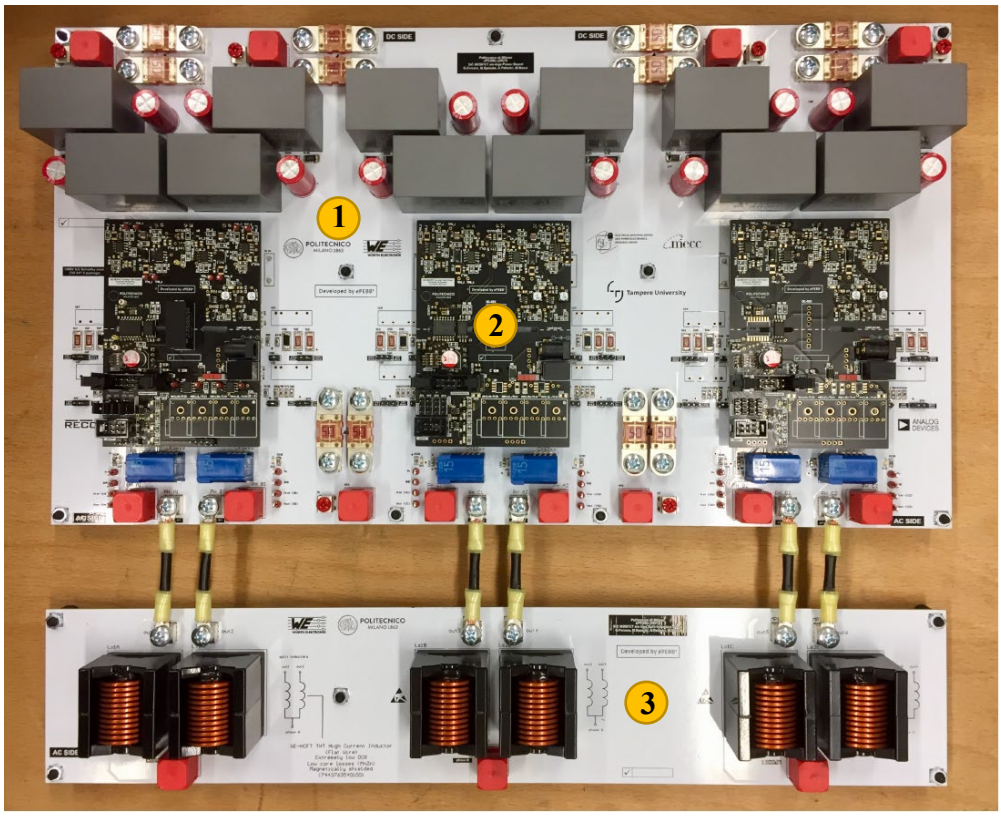


Figure 11: Split Output SiC-Based Power Converter

Additionally, a LauchPad F28069M Piccolo is used to control the inverter, which executes the main switching algorithm of the MOSFETs, monitors all the control signals and acts when it is necessary to ensure that the system is operating properly and safely.

Power Unit

The power unit is composed by the DC-link capacitor bank, the three Vincotech MOSFET SiC modules connected by press-fit technology and the different systems for measuring and signal processing of current and voltage.

Gate Drive Unit

The gate drive unit is responsible for switching of the different MOSFETs by the PWM signals that it receives from the control unit with optical fiber technology. Also provides the connection for other signals (temperature, current, voltage…) to the control unit and makes the isolation between the low voltage part (control unit) and the high voltage part (power unit).

Split Inductor Unit

Consists of the inductors to realize the split output topology, also providing the connections to the power unit.

3.2. Analysis of the Power Unit

In order to make the appropriate improvements in the converter, the first step is to identify the current malfunctions. For this purpose, an exhaustive analysis of the power unit in the previous design is carried out, including the study of new design methods for the converter hardware, which result in different proposals that are verified by the use of calculations and simulations.

The list of the different points that were followed to improve the performance of the power unit of the converter are shown below.

DC-Link

- Calculations to verify the correct sizing of the DC-Link capacitance of the inverter.
- Selection of new DC-Link capacitor bank with MKP technology to optimise space, cost, and performance.

Snubber Capacitors

- Study of the integration of Snubber capacitors together with SiC MOSFET devices in order to reduce the voltage peaks caused by the parasitic inductances of the hardware design and the fast current pulses (di/dt).
- Simulation using PSIM software and comparison between the new proposal hardware with snubber capacitor and the transient response captured in previous tests of the existing inverter.

3.2.1. DC-Link

It is necessary a properly dimensioning of the DC-Link capacitors for the power inverter to comply with the established requirements, trying to ensure that its occupied volume is the minimum possible.

The capacitor bank of the DC-Link mainly performs two functions:

- *Provides a low impedance path for high frequency currents.* When the frequency goes up, the stray inductances of the battery and cables cause the impedance increase ($X_L = j\omega L$). Inversely, the impedance of the DC-Link capacitor bank decreases according to the equation $X_C = \frac{1}{j\omega C}$, so becomes the preferred path for high-frequency AC Ripple Current.
- *Stiffen the DC bus.* The DC-Link capacitors decouple the effects of parasitic inductance from the DC voltage source to the power bridge. Voltage ripple on the DC bus manifests as ripple in the phase current of the inverter, which is undesirable and must be prevented by having a rigid DC bus. For the dimensioning of the capacitors, it is necessary to specify the maximum permissible voltage ripple on the DC bus.

After describing the functionalities of the DC-Link, the dimensioning is determined based on the analysis of four parameters that it must satisfy.

1. DC Voltage Rating:

The DC voltage rating of the capacitor should be rated based on the average maximum bus voltage multiply by a safety factor of 10%.

$$V_{cap} > V_{DC,N} \cdot 1{,}1$$

$$\boxed{V_{cap} > 700\ V \cdot 1{,}1 = \mathbf{770\ V}}$$

2. Ripple Current Rating:

An analytical method for calculating ripple current based on inverters which use Space Vector Modulation (SVM) is used for dimensioning of the DC-Link capacitor bank. The ripple current refers to the AC current that the capacitors must supply to the power bridges and the motor.

The inverter input current $i(t)$ can be expressed by the following three components:

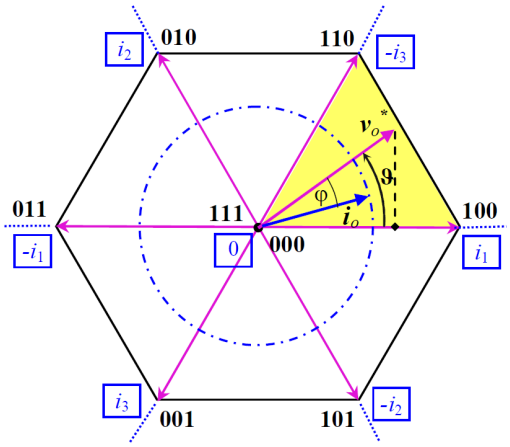
$$i(t) = I_{dc} + \tilde{\imath}(t) + \Delta i(t)$$

Being I_{dc} the average dc component, $\tilde{\imath}(t)$ the alternating double fundamental frequency component and $\Delta i(t)$ the switching frequency component.

In a system with balanced load the component $\tilde{\imath}(t)$ is zero and the inverter input current only contains of average dc current and high frequency harmonics around the switching frequency and its multiplies.

$$i(t) = I_{dc} + \Delta i(t) \qquad \textit{Balanced Load}$$

The input current $i(t)$ is the sum of three bridge leg current and is dependent on the inverter switching state. Considering three switching leg states $S_k = [0,1]$, $k = 1,2,3$, the input current of inverter bridge leg can be expressed as:



$$i(t) = S_a i_a + S_b i_b + S_c i_c$$

Figure 12: Space vector diagram of a three-phase inverter output voltage.

The inverter phase currents over the switching period for the worst case correspond to three reference signals with 120º phase shift and whose amplitude is the maximum phase current given in the system specifications ($I_{ph,max} = I_N = 32\ A$).

$$i_a = I_{ph,max} \cdot \sin(\omega t)$$

$$i_b = I_{ph,max} \cdot \sin\left(\omega t - \frac{2}{3}\pi\right)$$

$$i_c = I_{ph,max} \cdot \sin\left(\omega t + \frac{2}{3}\pi\right)$$

To calculate the average bus current I_{dc}, the average value of the input current $i(t)$ in a switching period is calculated.

$$I_{DC} = \frac{1}{T_e}\int_0^{Te} i(t) \cdot dt$$

By regrouping the above equations, the value of switching frequency input current component is obtained.

$$\Delta i(t) = i(t) - I_{dc} = i(t) - \frac{1}{T_e}\int_0^{Te} i(t) \cdot dt$$

It is assumed that the battery supplies only DC current and the capacitor must supply all AC current because as the frequency goes up, the impedance of the battery increases while the impedance of the capacitor decreases. This includes the AC components of the fundamental, harmonics and current ripple at the switching frequency. By calculating the RMS component of the AC current, it is possible to obtain the peak current value to be supplied by the capacitor bank of the DC-Link.

$$I_{DC\_link,RMS} = \Delta i_{RMS}(t) = \sqrt{\frac{1}{T_e}\int_0^{Te} (i(t) - I_{DC})^2 \cdot dt}$$

The current required by the capacitor bank due to the use of SVM modulation depends on the phase current, the modulation index, and the power factor. Assuming a unity power factor, the RMS current is plotted for the entire modulation index range [0 ; 1.1547] using the SIMULINK simulation tool in MATLAB.

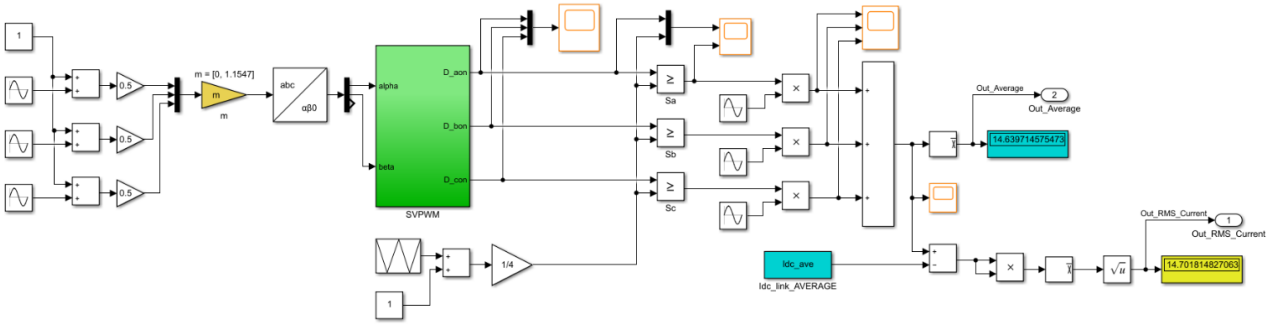


Figure 13: Simulation of the RMS current of the DC-Link in a three-phase inverter with SVM for a PM Motor

After the simulation is completed, the DC-Link capacitor bank has a maximum RMS current to be supplied of **14,7019 A** for a modulation index of **m = 0,6126**.

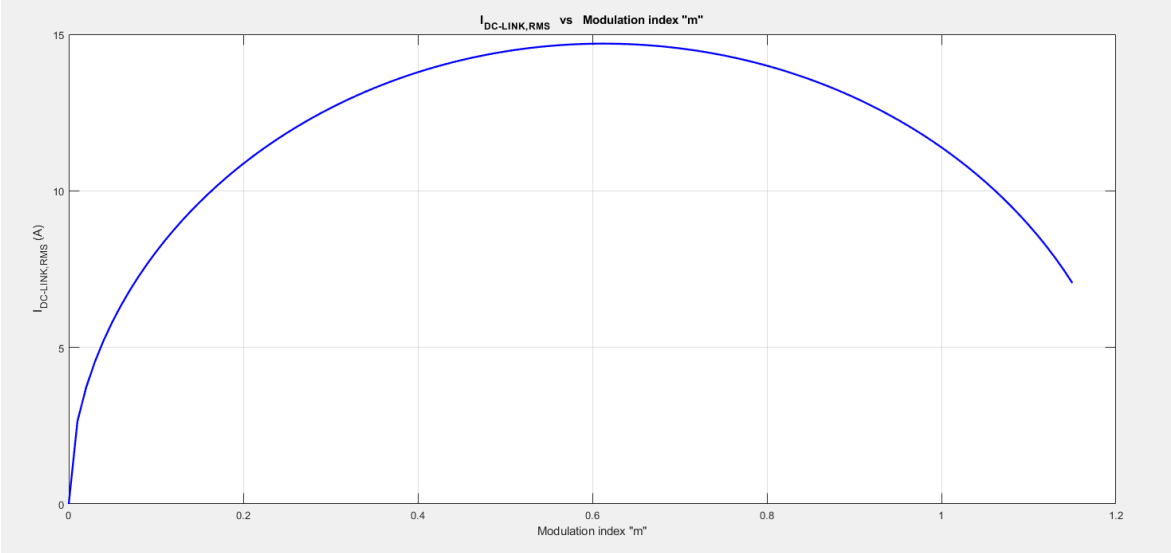


Figure 14: DC-Link RMS Current vs Index Modulation in a three-phase inverter with SVM for a PM Motor

$$I_{DC_{link},RMS}(m = 0{,}6126) = \mathbf{14{,}7019\ A}$$

Another way to calculate the value of the maximum RMS current for PM motors using an approximate but simpler calculation method is to multiply the maximum RMS phase current by a factor of 0,65.

$$I_{DC\_link,RMS}{}' = 0{,}65 \cdot I_{ph,RMS} = 0{,}65 \cdot \frac{32\ A}{\sqrt{2}} = \mathbf{14{,}7078\ A}$$

The maximum RMS current of the DC-Link capacitor bank is decisive to ensure the lifetime of the capacitors. The ripple current rating of a capacitor is derived from its temperature and depends on the ESR and thermal resistance. When a capacitor is exposed to high frequency charge and discharge cycles, the conductors heat up, which causes the internal temperature of the capacitor to increase. It is necessary to limit this internal temperature of the capacitor in order to prevent its deterioration, for this reason manufacturers specify the maximum value of the RMS ripple current at an ambient temperature to ensure its proper operation.

For the selection of the capacitor bank in a conservative way, a safety factor of 10% is applied to the ripple current rating.

$$I_{cap,RMS} > 1{,}1 \cdot 14{,}7019 = \mathbf{16{,}172\ A}$$

3. Ripple Voltage Rating:

The DC Link capacitor smooth DC voltage fluctuations and stiffen the DC bus. This is important because any voltage ripple on the DC bus shows up as current ripple in the phase currents, and that leads to torque ripple.

Assuming that the current flowing through the capacitors in a switching period remains constant, the current-voltage relationship of a capacitor over a one switching period is as follows.

$$i_{cap} = C \cdot \frac{dv}{dt} \quad \rightarrow \quad i_{cap} = C \cdot \frac{\Delta v}{\Delta t} \quad \rightarrow \quad C > \frac{I_{cap,MAX}}{\Delta v \cdot f_{sw,min}} = \frac{\sqrt{2} \cdot I_{cap,RMS\_MAX}}{\Delta v \cdot f_{sw,min}}$$

The capacitance is inversely proportional to switching frequency. When the switching frequency increase , the capacitance of the DC-Link bus required decreases. Also, the capacitor volume is proportional to the capacitance, so by increasing the switching frequency, higher power densities can be achieved. This is one of the reasons why SiC and GaN-based converters can achieve higher power densities than IGBT-based converters.

For the design of the capacitor bank of the DC-Link ,the maximum allowable voltage ripple assumed is 3% of the maximum voltage of the DC-Link.

$$C > \frac{\sqrt{2} \cdot \ 16{,}172\ A}{(1000\ V \cdot 0{,}03)\ \cdot 10\ kHz} = \mathbf{76{,}236\ uF}$$

4. Resonant Frequency Rating:

The capacitor has a frequency at which it is self-resonant by the ESL. Beyond this point, the capacitor behaves as an inductor and does not work correctly. To avoid this, the capacitor must have a resonant frequency 2 times higher than the switching frequency. The maximum switching frequency achievable by the inverter is 100 kHz, higher frequencies make the SiC MOSFET less efficient.

$$f_{cap,Res} > 2 \cdot f_{sw} = 2 \cdot 100\ kHz = \mathbf{200\ kHz}$$

In summary, the characteristics to be fulfilled by the DC-Link capacitor bank are shown in the following table (Table 1).

DC-Link capacitor bank Requirements	
DC Voltage	V_{DC} > 770 V
Ripple Current RMS	I_{RMS} > 16,172 A
Capacitance	C > 76,236 uF
Resonant Frequency	f_{Res} > 200 kHz

Table 1: DC-Link capacitor bank Requirements

The DC-Link capacitor bus of the laboratory power board consists of two electrolytic capacitors and two ceramic capacitors per leg. The characteristics and connections of the capacitors are shown below.

Model	860241478004	C4AF7BW4680T3JK
Supplier	Würth Elektronik	KEMET
Capacitance	22 uF	6.8 uF
Rated Voltage	450 V	700 V
RMS Current	0.632 A	18.3 A
ESR	0.7 Ω	2.8 mΩ
ESL	11 nH	10 nH
$f_{resonance}$	-	-
Dielectric	Polypropylene metallized	Metallized Polypropylene
Size	25mm x 13 mm (ØD)	42 mm x 37 mm x 28 mm

Table 2: DC-Link capacitors specifications of the laboratory power board design

The two capacitors of each type are connected in series and the two branches are connected by the neutral point N. This configuration results in a total DC-Link capacitance of 86.4 uF

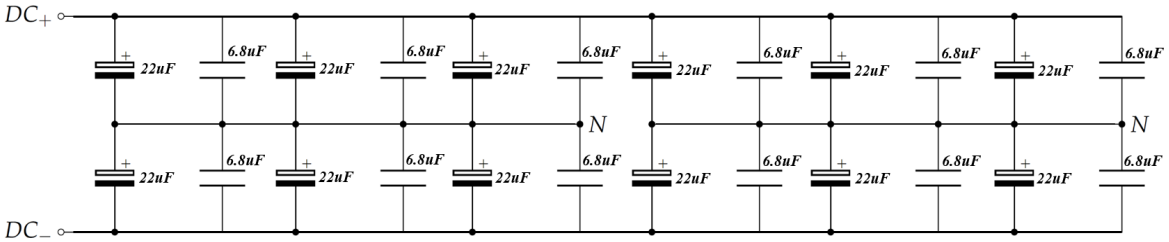


Figure 15: DC-Link capacitor connections from the lab power board design

$$V_{DC\_link} = \min(450\ V \cdot 2\ ;\ 700\ V \cdot 2) = 900\ V > \mathbf{770\ V}$$

$$I_{RMS,DC\_link} = (0{,}632\ A + 18{,}3\ A) \cdot 6 = 113{,}592\ A > \mathbf{16{,}172\ A}$$

$$C_{DC_{link}} = \left(\frac{22\ uF}{2} + \frac{6{,}8\ uF}{2}\right) \cdot 6 = 86{,}4\ uF\ > \mathbf{76{,}236\ uF}$$

$$Vol_{DC_{link}} = \left(\frac{\pi \cdot 13^2}{4} \cdot 25\right) mm^3 \cdot 12 + (42 \cdot 37 \cdot 28) mm^3 \cdot 12 = \mathbf{561{,}964\ cm^3}$$

$$€_{DC_{link}} = 1{,}73\ € \cdot 12 + 7{,}06\ € \cdot 12 = \mathbf{105{,}48\ €}$$

The DC-Link capacitor bus meets the system requirements. It is recommended to connect the neutral point "N" of all capacitors in order to avoid voltage unbalance between legs. In addition, the volume occupied by the DC-Link is too high and could be reduced.

The use of film capacitors is highly recommended instead of using electrolytic capacitors due to their higher ripple current capability because of their low ESR and ESL. In addition, the volumetric efficiency is usually much higher when using film capacitors and they have a lifetime of approximately 100,000 hours compared to 10,000 hours for an electrolytic.

A new proposal of the DC-Link capacitor bus design is made by using only film capacitors in order to meet the system requirements and to optimise the volume and the cost. The capacitors chosen for this design are shown in the Table 3.

Model	MKP1848C62090JP4	C4AQOBW5200M3HJ
Supplier	Vishay	KEMET
Capacitance	20 uF	20 uF
Rated Voltage	900 V	900 V
RMS Current	14 A	18.9 A
ESR	5 mΩ	4.3 mΩ
ESL	35 nH	13 nH
$f_{resonance}$	250 kHz	-
Dielectric	Metallized Polypropylene	Metallized Polypropylene
Size	24 mm x 44 mm x 42 mm	24 mm x 44 mm x 41,5 mm

Table 3: New proposal DC-Link capacitors specifications for the power board design

The capacitors meet the voltage requirements of the DC-Link, so their connection would be done by interconnecting 4 in parallel to reach a resulting capacitance of 80 uF.

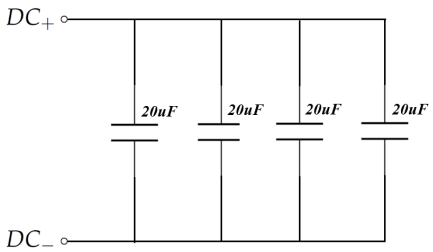


Figure 16: New proposal DC-Link capacitors connections for the power board design

Considering the two capacitor models, it was decided to choose the C4AQOBW5200M3HJ from KEMET, which have better ESR, ESL and RMS peak current performance and are also cheaper in terms of market price.

$$V_{DC\_link} = 900\ V > \mathbf{770\ V}$$

$$I_{RMS,DC\_link} = 18{,}9\ A \cdot 4 = 75{,}6\ A > \mathbf{16{,}172\ A}$$

$$C_{DC_{link}} = 20\ uF \cdot 4 = 80\ uF\ > \mathbf{76{,}236\ uF}$$

$$Vol_{DC_{link}} = (24 \cdot 44 \cdot 41{,}5)mm^3 \cdot 4 = \mathbf{175{,}296\ cm^3}$$

$$€_{DC_{link}} = 6{,}64\ € \cdot 4 = \mathbf{26{,}56\ €}$$

The new DC-Link capacitor bank meets the necessary requirements by achieving a size reduction of 68.80 % and a price reduction of 74.82 % using the MKP technology.

3.2.2. Snubber Capacitors

The use of SiC MOSFETs in power applications where fast and efficient switching is required leads to high voltage peaks due to the combination of the high dv/dt and di/dt with the stray inductances of the modules and the surrounding circuit.

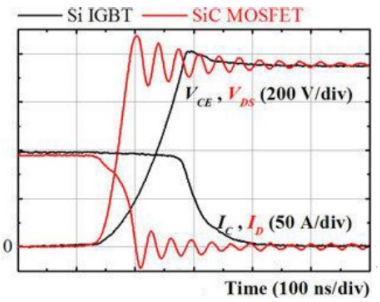


Figure 17: Comparison of voltage and current transients during switching of an Si IGBT and a SiC MOSFET

When the MOSFET turns on, current stores energy in the stray inductance of the wire on the PCB layout. This stored energy resonates with the parasitic capacitance of the MOSFET producing a surge current that follows the current ring path illustrated in Figure 18.

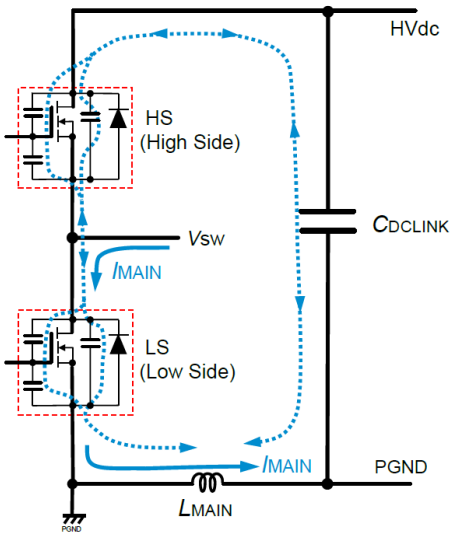


Figure 18: Current path when turn-off surge occurs

In a half-bridge typology when *LS* is turned on, the current I_{MAIN} flows from V_{SW} through the stray inductance L_{MAIN}. When *LS* is turned off, I_{MAIN} flows through the loop formed by L_{MAIN}, C_{DCLINK} and parasitic capacitance of the *HS* and *LS* switches. During the turn-off of *LS*, a surge voltage occurs at the Drain-Source terminals of *LS* due to the resonance phenomenon between the L_{MAIN} inductance and parasitic capacitance of the C_{OSS} MOSFET (C_{DS}+C_{DG}).

The maximum voltage V_{DS_SURGE} is calculated from the following equation.

$$V_{\mathrm{DS\_SURGE}} = \frac{V_A * e^{-(a/\omega)[\tan^{-1}(a/\omega)+\Phi]}}{1+(a/\omega)^2} + V_{\mathrm{HVDC}}$$

Where:

$$V_{\mathrm{A}} = \sqrt{{V_{\mathrm{HVDC}}}^2 + (a/\omega)^2 * \left(2 * R_{\mathrm{OFF}} * I_{\mathrm{MAIN}} - V_{\mathrm{HVDC}}\right)^2}$$

$$\Phi = tan^{-1} \frac{V_{\mathrm{HVDC}}}{(a/\omega)*(2*R_{\mathrm{OFF}}*I_{\mathrm{MAIN}}-V_{\mathrm{HVDC}})}$$

$$a = \frac{1}{2*R_{\mathrm{OFF}}*C_{\mathrm{OSS}}}$$

$$\omega_{SURGE} = \frac{1}{\sqrt{L_{\mathrm{MAIN}}*C_{\mathrm{OSS}}}} * \sqrt{1 - \left(\frac{\sqrt{L_{\mathrm{MAIN}}/C_{\mathrm{OSS}}}}{2R_{\mathrm{OFF}}}\right)^2}$$

- V_{HVDC} = Voltage applied on the DC-Link
- I_{MAIN} = RMS current at the output
- R_{OFF} = Resistance in the branch when a transistor turns off
- C_{oss} = Output parasitic capacitance of the transistor (datasheet).
- L_{MAIN} = Stray inductance of the transistor and the branch.

Roff is an approximation of the value of the equivalent resistance when the transistor is turned off and Lmain is the sum of the inductances of the DC-Link (Obtained by simulation in 0), the cable that connects the boards, the possible stray inductance of the snubber capacitor and finally, the inductance of the MOSFET itself (oversized in order to have a safety factor).

The calculations for the Vincotech module 10-PC124PA040MR-L638F18Y with a DC-Link bus voltage of 700 V and a maximum current of 32 A give the maximum peak drain-source voltage of the SiC MOSFET.

Data	
V_{HVDC}	700V
C_{oss}	76 pF
L_{MAIN}	16 nH
I_{MAIN}	32 A
R_{OFF}	12.5 Ω

$$V_{DS\_SURGE} = 805{,}06\ V$$

Table 4: Values for the calculation of the peak voltage at the drain-source terminals of the MOSFETs

The next step is to introduce a Snubber C_{SNB} capacitor (Figure 13) to reduce the peak voltage generated by the switching of the MOSFET, which is higher than 800 V and could damage the system. This capacitor has the function of neglecting LMAIN in order to reduce the energy stored in the current ring and consequently decrease the peak voltage generated between the drain and source of the MOSFET.

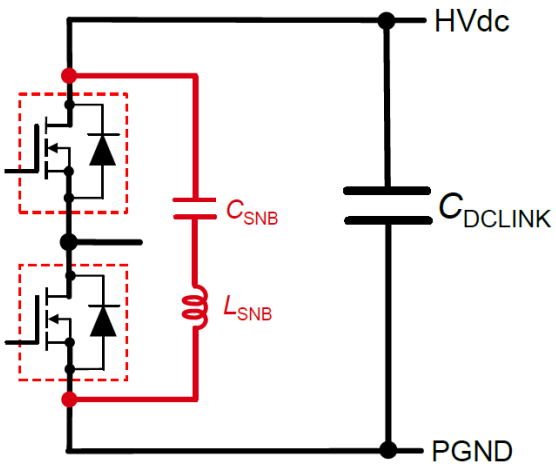


Figure 19: C Snubber capacitor in a MOSFET leg

The reduction of the peak voltage is due to the fact that C_{SNB} is placed very close to the switches in order to reduce the inductance involved in the switching path (L_{SNB}). The behaviour of the system will be better if the stray inductance is minimised as much as possible. However, this reduction is not always realistic and might make the heat dissipation worse. Instead, placing the snubber capacitor as close as possible to the MOSFET minimize the stray inductance of the circuit. The snubber capacitor C_{SNB} also absorbs the energy stored by the L_{SNB} inductance and clamp surge voltage while the MOSFET is turned off.

For the calculation of the Snubber capacitor needed to reduce the peak voltage generated in the Drain Source of the MOSFET there are two methods: **passive snubber**, which consists of passive components such as resistor, inductor, capacitor, and diodes; and **active snubber**, which utilize semiconductor switch.

Focusing on passive snubber, four different examples of commonly used Snubber capacitors are shown in the figure.

(a) *C snubber*, where the capacitor C_{SNB} is connected in parallel to the MOSFET bridge

(b) *RC snubber*, where the resistor R_{SNB} and capacitor C_{SNB} are connected in parallel to each MOSFET

(c) *Discharge RCD snubber*, where a diode is added to RC snubber; and

(d) *Non-discharge RCD snubber*, where the discharging path is changed from the discharge RCD snubber presented in (c).

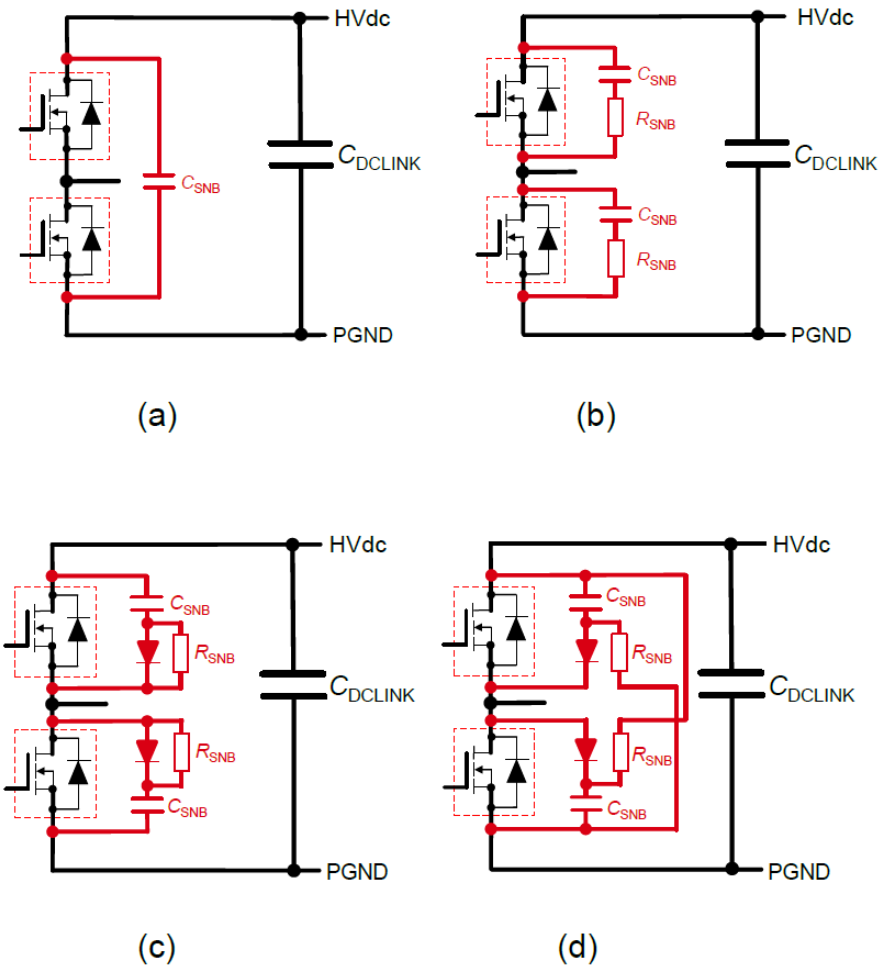


Figure 20: Passive snubber circuits. (a) C snubber, (b) RC snubber, (c) Discharge RCD snubber, (d) Non-discharge RCD snubber

During the development of the project, it was decided to design the passive snubber C implementation, given its layout simplicity, the reduction in the number of components and because it is more suitable for 2 in 1 module rather than circuit discrete components.

C Snubber Design

The C snubber circuit absorbs the energy stored in LMAIN. It is important that the parasitic inductance of the snubber path LSNB has to be smaller than LMAIN. A higher CSNB capacitance of the snubber makes it more efficient because it is not discharged, but it should be noted that the higher the capacitance, the higher the parasitic inductance (ESL) it will present.

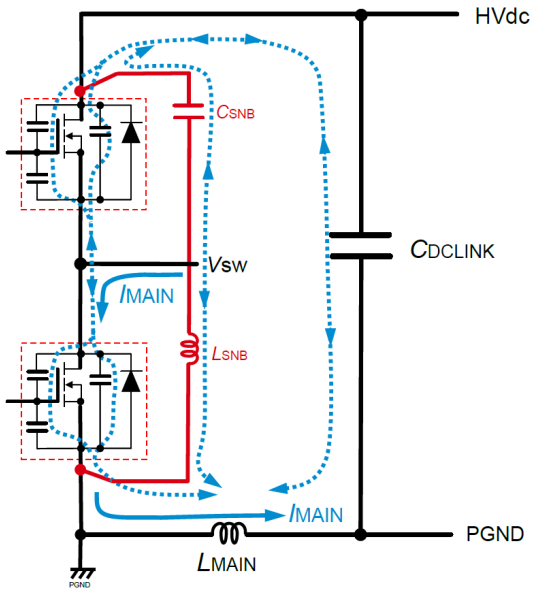


Figure 21: C snubber with the I_{MAIN} path

Assuming that all the energy stored in L_{MAIN} is transferred to the C_{SNB} capacitance, the following equation is used to select the required electrostatic capacitance of the snubber using the maximum peak voltage V_{DC_SURGE}.

$$C_{SNB} > \frac{L_{MAIN} \cdot {I_{MAIN}}^2}{{V_{DS\_SURGE}}^2 - {V_{HVDC}}^2}$$

$$\boldsymbol{C_{SNB} > \frac{16\,nH \cdot (32\,A)^2}{(805{,}06\,V)^2 - (700\,V)^2} = 0{,}1036\,nF}$$

For this application, the use of film capacitors has been abandoned in preference to a new generation of ceramic dielectric capacitors, which allow a considerable reduction in volume and weight without losing other features such as rated voltage or low ESL and ESR.

The capacitors selected are *B58031U9254M062* from the manufacturer *EPCOS / TDK* with a CSNB snubber capacitance of 0,25uF. This capacitance is oversized in order to allow the capacitor to withstand the maximum 1000 V of the design conditions and also to allow it conduct higher RMS currents.

Model	B58031U9254M062
Supplier	EPCOS / TDK
Capacitance	0,25 uF
Rated Voltage	900 V
RMS Current	7 A
ESR	24 mΩ
ESL	3 nH
$f_{resonance}$	9 MHz
Dielectric	Ceramic Lead Lanthanum Zirconate Titanate
Size	7,14 mm x 7,85 mm x 4 mm
Price	7,30 €

Table 5: C Snubber capacitor specifications

The snubber characteristics meet the system requirements, maintaining a low ESL below LMAIN to decrease the voltage peaks between the Drain-Source terminals of the MOSFETs. The converter will incorporate three snubber capacitors, one for each module, which results in an associated cost of 21,90 €, that is not a very high value for the improvement in the system performance in terms of durability and reliability.

$$€_{snubber} = 7{,}30\ € \cdot 3 = \mathbf{21{,}90\ €}$$

3.2.3. PSIM Model of the Power Unit

PSIM is a simulation software that is focused on power electronics. It offers very high simulation speed and at the same time produces high quality simulation results at the system level. Using the PSIM software tool, a simulation model of the laboratory inverter is generated in order to reproduce the behaviour as accurately as possible and to evaluate the improvements from the proposed hardware changes.

In order to adjust the simulation model to the behaviour in the real conditions, previous tests of the laboratory inverter in different configurations were used. The experimental test setup consisted of the following hardware components:

- Device under test (DUT), which is the power device to be studied, depending on the configuration, it's the lower or upper SiC MOSFET of one leg of the power converter.
- Freewheeling diode, the external SiC Schottky diode that allows the freewheeling current flow, or the internal antiparallel diode of the SiC MOSFET.
- Split Inductors, if required, to study the change in the converter's behaviour
- DC power supply, at a voltage $V_{DC} = 20V$
- DC-Link, consists of the capacitors assembled on a leg of the designed converter, with a capacitance value $C_{DC} = 28{,}8\ uF$
- Load inductor, a *700 uH* inductor with *0.21 Ω* parasitic series resistance
- Gate Driver Circuit, board which is responsible for switching the different MOSFETs according to the signals of the control board
- Control signal generator, a *LaunchPad F28069M Piccolo micro-controller board* is used to generate the control signals with the standard procedure of a *double pulse test (DPT)*
- Oscilloscope, to capture signals of interest.

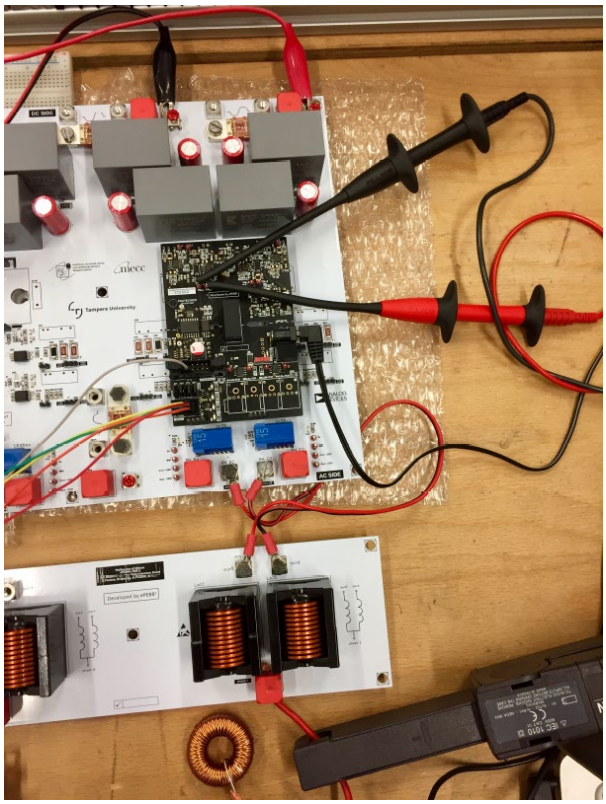


Figure 22: Test setup used for the Double Pulse Test

Double Pulse Test

The test procedure is the same for all experiments done on the inverter hardware of the laboratory using the double pulse test method.

This type of test starts by charging the capacitor bank of the DC-Link to the desired value of 20 V. When this value is reached, the DC-Link is disconnected from the power supply. Furthermore, the control signals of the gates generated by the micro-controller consist of three different periods time periods (**¡Error! No se encuentra el origen de la referencia.**).

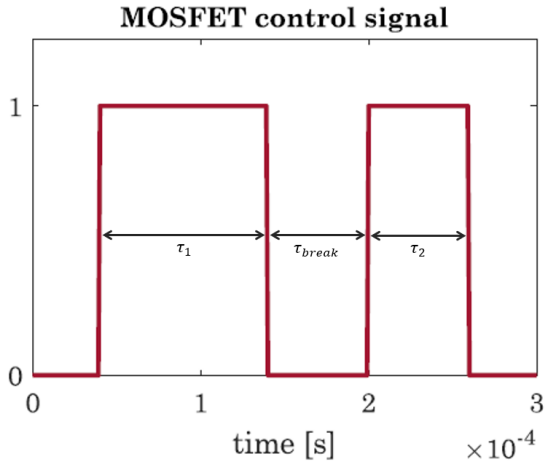


Figure 23: Double Pulse Test MOSFET control signal

1. ***First Pulse with duration τ_1***, defined considering that the voltage overload is governed by the equation

$$v_{load} = L_{load} \cdot \frac{di_{load}}{dt}$$

with initial conditions $v_{load}(t = 0) = V_{dc}$ and $i_{load}(t = 0) = 0$. Also, it is assumed that the DC-Link voltage during τ_1 is constant and $i_{load}(t = \tau_1) = I_{test} = 3A$

$$V_{dc} = L_{load} \cdot \frac{I_{test}}{\tau_1} \rightarrow \quad \tau_1 = L_{load} \cdot \frac{I_{test}}{V_{dc}}$$

$$\tau_1 = 700\ \mu H \cdot \frac{3\ A}{20\ V} \approx \mathbf{100\ \mu s}$$

2. ***Pulse break with duration τ_{break}***, during this time the switch under test is off, the load is not connected to the DC-Link and the currents flows through the freewheeling diode and the load. The conducting diode has a forward voltage of $V_F = 1{,}5\ V$ and the current decrease during this period a maximum value of $\Delta I_{max} = 5\% \cdot I_{test} = 0{,}15\ A$.

$$\Delta I = \frac{V_F}{L_{load}} \cdot \tau_{break} \rightarrow \quad \tau_{break,max} = \frac{\Delta I_{max} \cdot L_{load}}{V_F}$$

$$\tau_{break,max} = \frac{0{,}15\ A \cdot 700\ \mu H}{1{,}5\ V} = 70\ \mu s\ (\mathbf{60\ \mu s\ limited\ by\ micro})$$

The sampling time of the micro-controller is $T_s = 1/f_s = 20\ \mu s$, as a consequence τ_{break} is set to $60\ \mu s$.

3. ***Second pulse with duration τ_2***, this pulse has the role of turning on the switch. During this period, the load is again connected to DC-Link, thus the load current increase. The duration of this pulse has to be selected to remain the current load under acceptable levels. For these reasons, τ_2 is set to $60\ \mu s$.

$$\tau_2 = 60\ \mu s$$

PSIM schematic

After defining the Double Pulse Test to be used in the simulation of the converter hardware, the schematic design has to be defined in PSIM by introducing the simulation models of the different components in order to emulate the behaviour as accurately as possible. The Figure 24 shows the PSIM schematic of the converter system for a single module in Half-Bridge configuration.

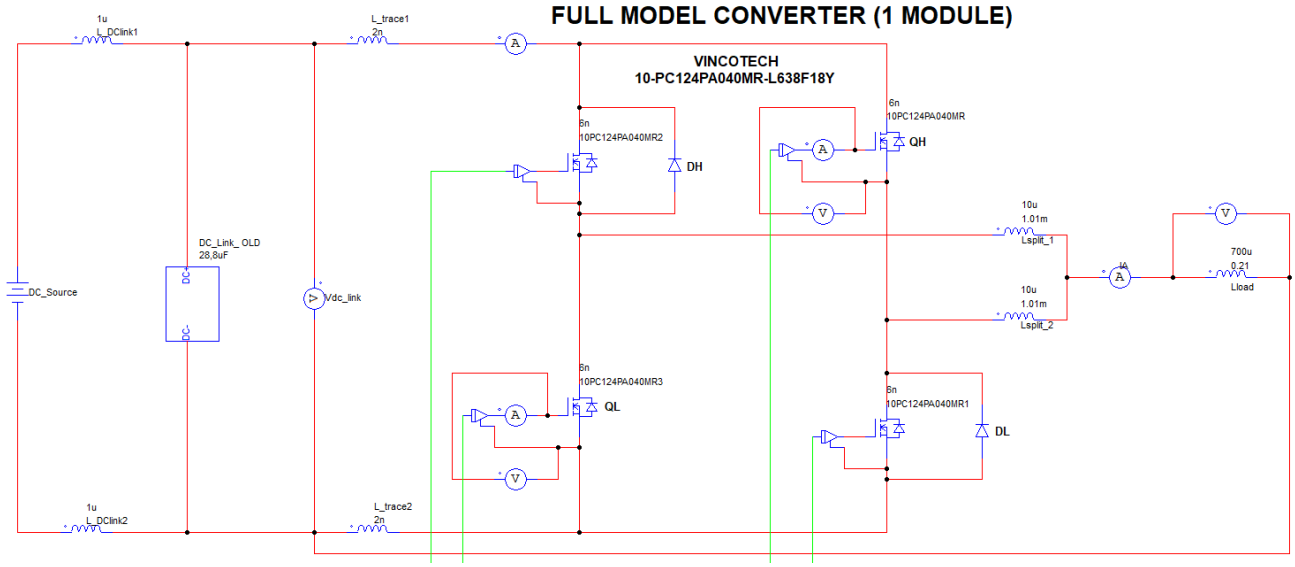


Figure 24: Simulation Model of a single leg of the converter in PSIM

Where the DC-link subcircuit is composed of the following.

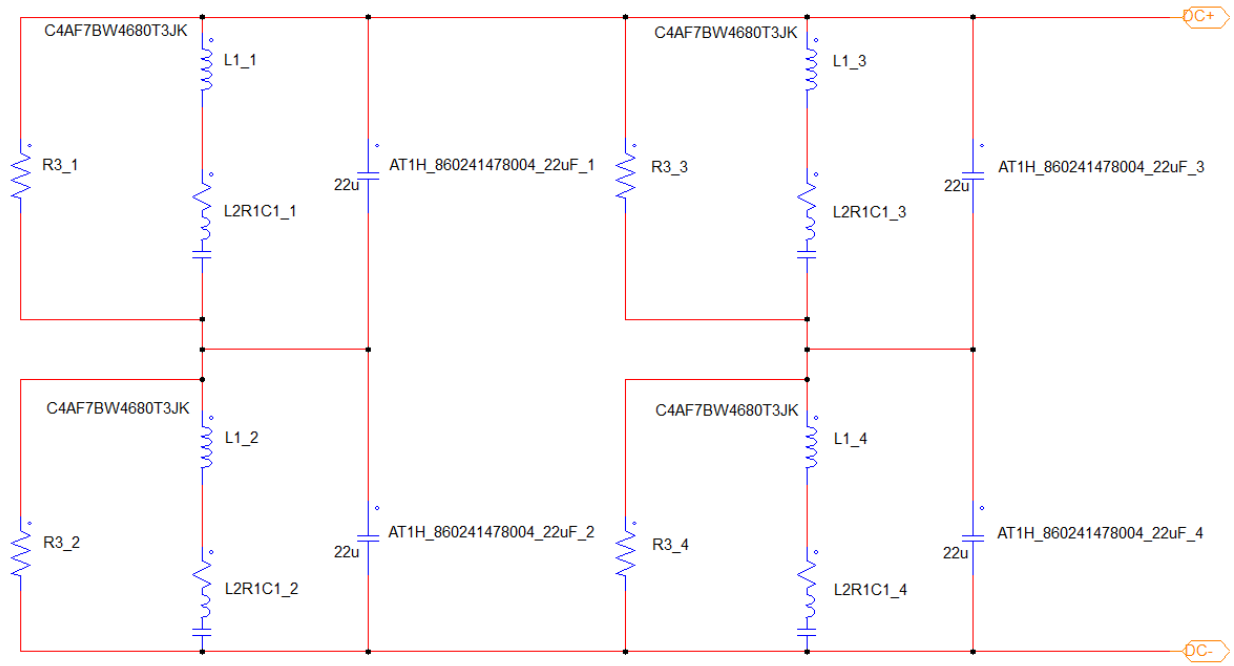


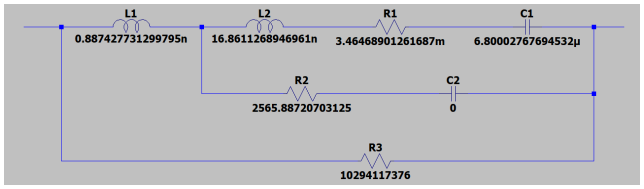
Figure 25: DC-Link Subcircuit of the converter in PSIM

Simulation models of both DC-Link capacitors were made from the manufacturer's information given in the PSPICE files of the components.

Capacitor C4AF7BW4680T3JK:

```
.SUBCKT C4AF7BW4680T3JK 1 6
*Temp = 25Â°C, Bias = 0VDC, Center Frequency = 10000 Hz
*KEMET Model RLC Cerm
R1 3 4 0.00346468901261687
R2 2 5 2565.88720703125
R3 1 6 10294117376
L1 1 2 8.87427731299795E-10
L2 2 3 1.68611268946961E-08
C1 4 6 6.80002767694532E-06
C2 5 6 0
.ENDS
```

PSpice



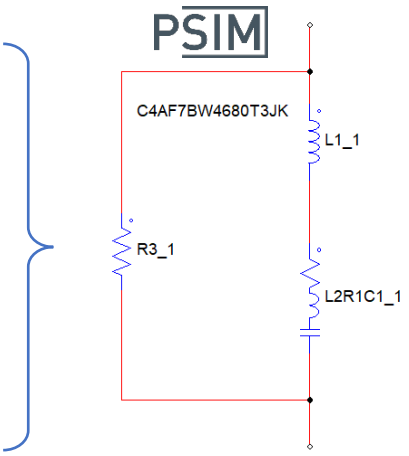
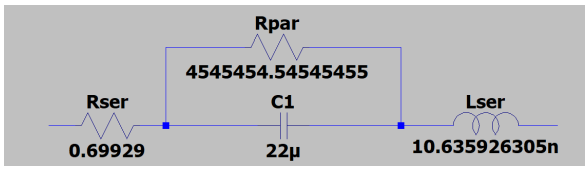


Figure 26: C4AF7BW4680T3JK PSPICE parameters and its model in PSIM

Capacitor AT1H 860241478004:

```
* AT1H_860241478004_22uF 1 2 "MACROMODEL" SUBCIRCUIT
.subckt AT1H_860241478004_22uF 1 2
*
Rser 1 3 0.69929
Lser 2 4 1.0635926305E-08
C1 3 4 0.000022
Rpar 3 4 4545454.54545455
.ends AT1H_860241478004_22uF
```

PSpice



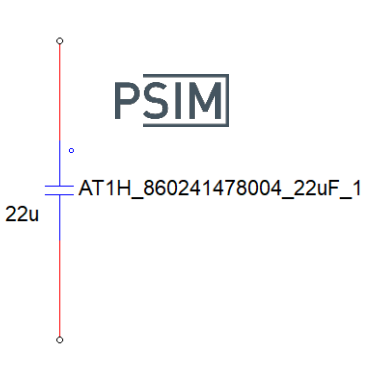
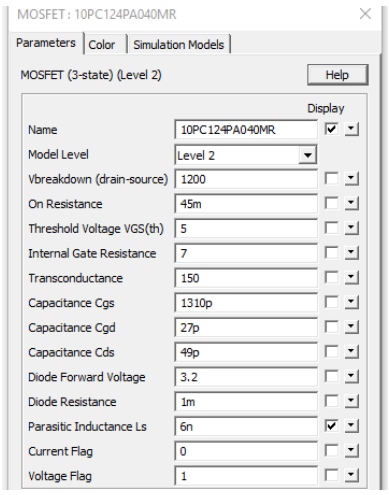
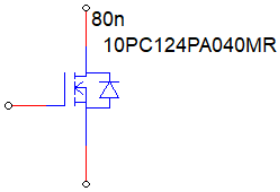
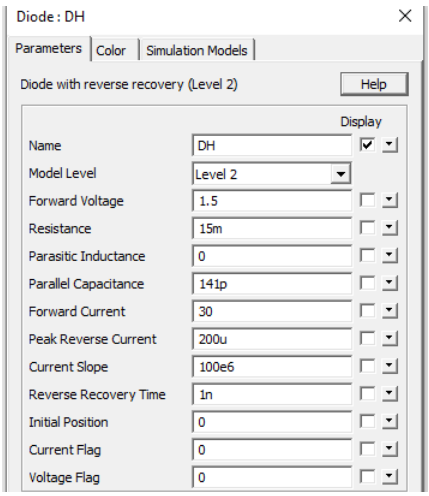


Figure 27: AT1H 860241478004 PSPICE parameters and its model in PSIM

The parameters of the MOSFETs and diodes were set according to their respective datasheet. For the configuration parameters of the SiC MOSFETs and SiC Schottky diodes, level 2 parameters of the PSIM software were used.







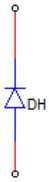


Figure 28: PSIM level 2 configuration parameters of the SiC MOSFET and SiC Diode

The values of the parasitic inductances were selected by performing successive simulations of the system to adjust the response with the values captured by the oscilloscope of the laboratory converter tests. The values of the DC-Link parasitic inductances were set between the realistic values of 1-5 uH while the SiC MOSFET module between 10-100 nH. In addition, based on the PCB design of the power board, the parasitic inductance was estimated as a function of the length, width, and thickness of the trace, obtaining values of nH. The values used in the simulation are shown in Table 6.

Stray Inductances	
L_{DC_Link}	1 µH (Symmetrical)
$L_{trace\_DC\_bus}$	2 nH (Symmetrical)
L_{SiC_MOSFET}	6 nH (per Module)
$\mathbf{L_{MAIN}} = 2 \cdot L_{trace\_DC\_bus} + 2 \cdot L_{SiC\_MOSFET} = \mathbf{16\ nH}$	

Table 6: Stray Inductances of the PSIM model of the converter

It should be noted that the MOSFET gate circuit is configured according to the converter hardware explained in section 3.3.2. This hardware incorporates the bootstrap technique in the gate switching circuit design and generates PWM switching signals between 0V and 18V with a gate resistance of 6 Ohm.

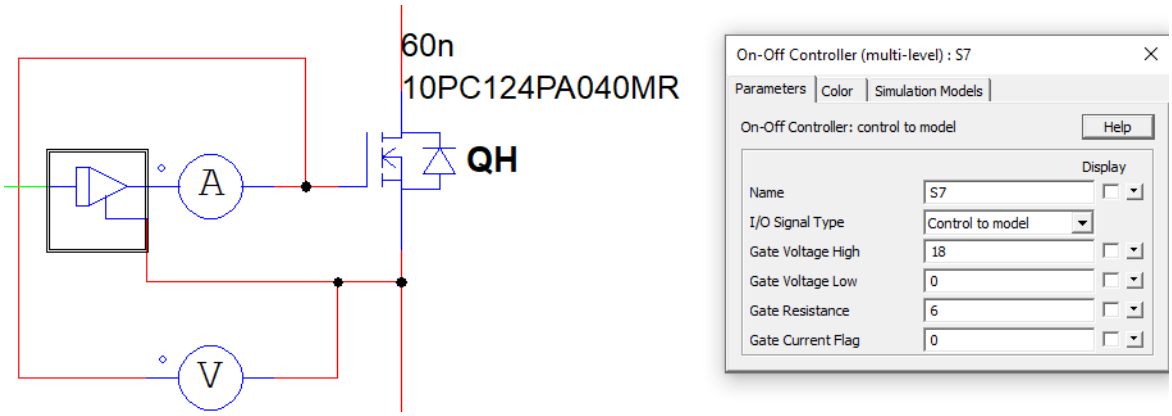


Figure 29: Bootstrap circuit configuration in PSIM

PSIM Simulations

When the different elements of the system have been integrated into PSIM and their parameters have been adjusted, the model simulations are carried out and compared with the tests of the real laboratory converter to validate the model.

➢ *Half bridge configuration.*

To perform the parameter adjustment, the converter is tested with the Half-bridge configuration. In this configuration, both legs of the SiC MOSFET module are used, connecting the load between both output terminals, and applying the control signal of the double pulse test DPT to the high-side MOSFET.

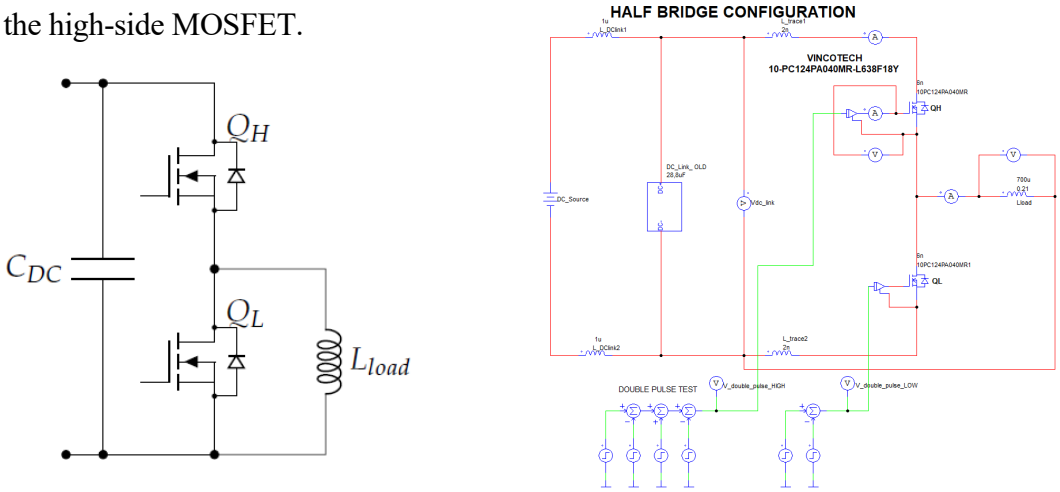


Figure 30: Half Bridge configuration of the converter and its Model in PSIM

The model is simulated in PSIM for a simulation time of 300 µs to obtain firstly the Double Pulse Test graphs. To do this, the voltage applied to the gate-source of the MOSFET and current of the load connected between the output terminal and the DC- are monitored (Figure 31).

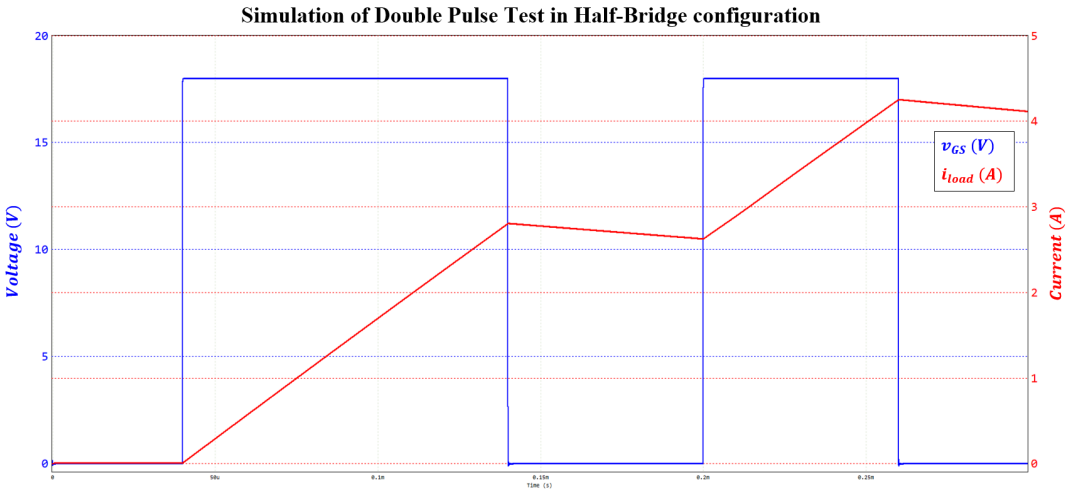


Figure 31: Simulation of the Double Pulse Test in Half-Bridge configuration using PSIM

The results are as expected, when the top side MOSFET is closed at τ_1 the current starts to increase until it reaches a value close to 3A, then with the opening of the MOSFET the current decreases slightly during τ_{break} and finally with the new switching of the MOSFET at τ_2 the current increases again to 4,25A.

To verify the correct selection of the stray inductances and their effect on the voltage spikes caused by the fast switching of the SiC MOSFETs, the voltage between the drain-source terminals of the high-side MOSFETs in Half Bridge configuration is monitored and compared with the real test of the converter in the laboratory (Figure 32).

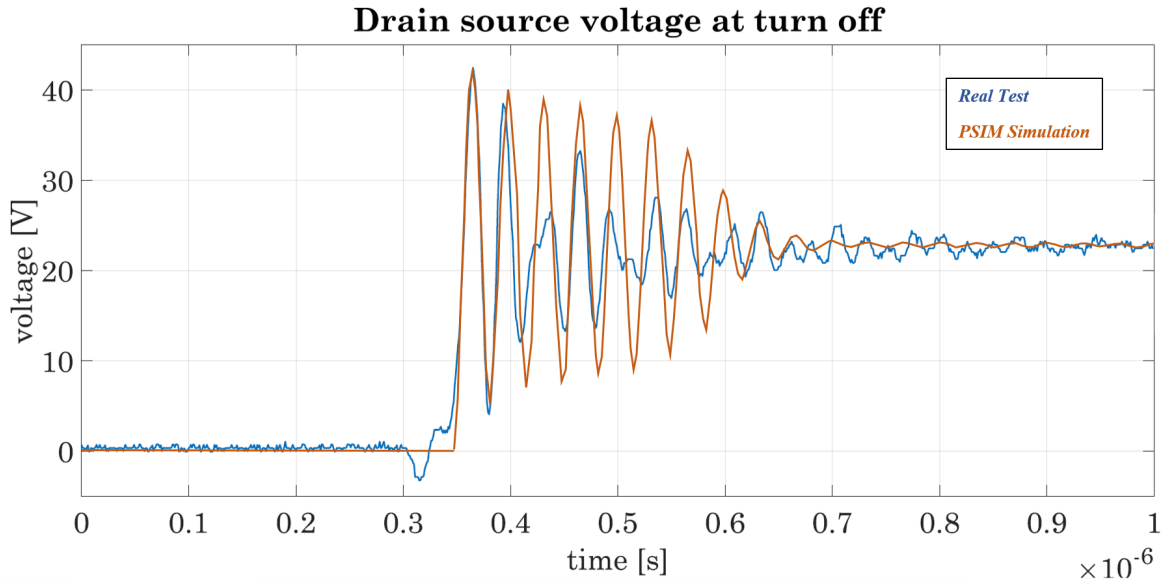


Figure 32: Comparison of the Drain-Source voltage at turn-off between real test and PSIM Simulation (Half Bridge)

It is observed that the simulation obtained by PSIM of the drain-source voltage of the MOSFET is very similar to the real behaviour of the system, especially in the maximum peak voltage. This peak voltage has a maximum value of 43 V approximately, which exceeds by far the value of 20 V established in the DC-Link capacitor bank.

➢ *Split Output configuration.*

The next configuration that is simulated from the PSIM model is the split output configuration (Figure 33), that allows to observe if the response obtained is in accordance with the results of the converter tests done in the laboratory with this topology.

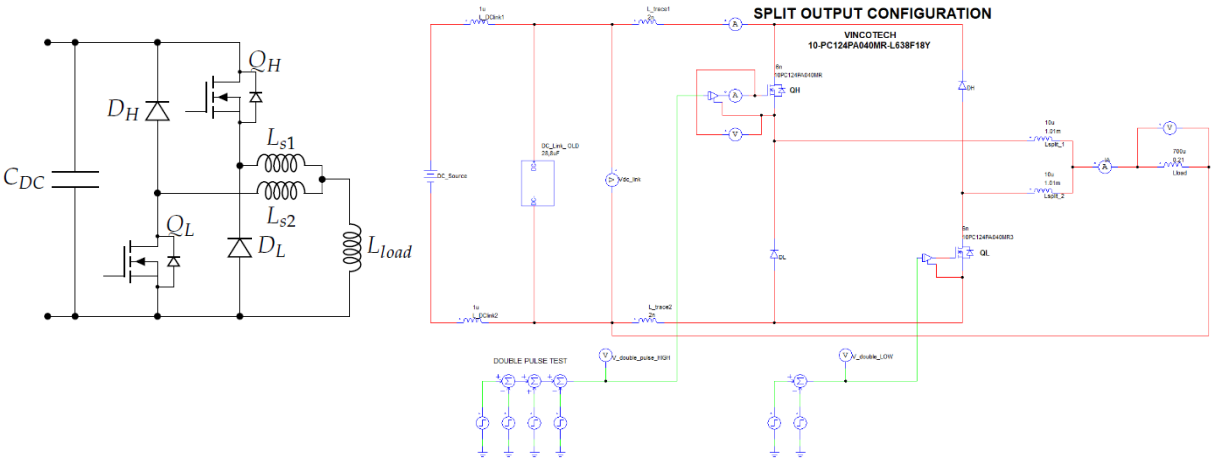


Figure 33: Split Output configuration of the converter and its Model in PSIM

In this configuration two inductors *7443763540100* from Wurth Elektronik, with an inductance of 10 µH, are added on both legs of the converter resulting in a single output terminal. The load is connected between this single output terminal and the DC- of the DC-Link bus. The high side MOSFET is selected as the device under test by applying the double pulse test signal and the same simulation period is maintained (300 µs).

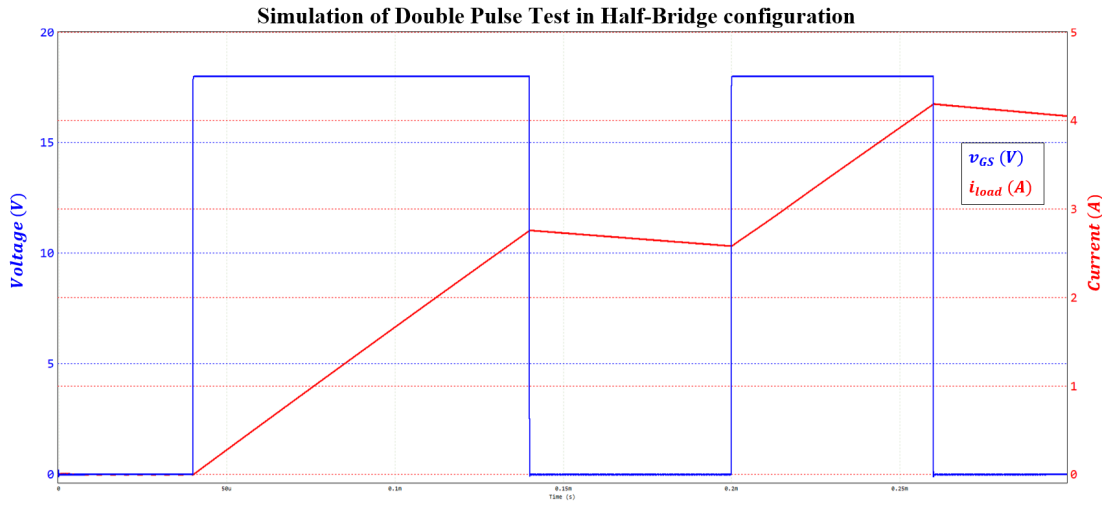


Figure 34: Simulation of the Double Pulse Test in Split Output configuration using PSIM

The signals obtained from the double pulse test in the Split output configuration are very similar to the Half bridge configuration. The difference is that the output load is increased by connecting the splitting inductors and therefore the current is slightly lower, reaching a maximum of 4.18V.

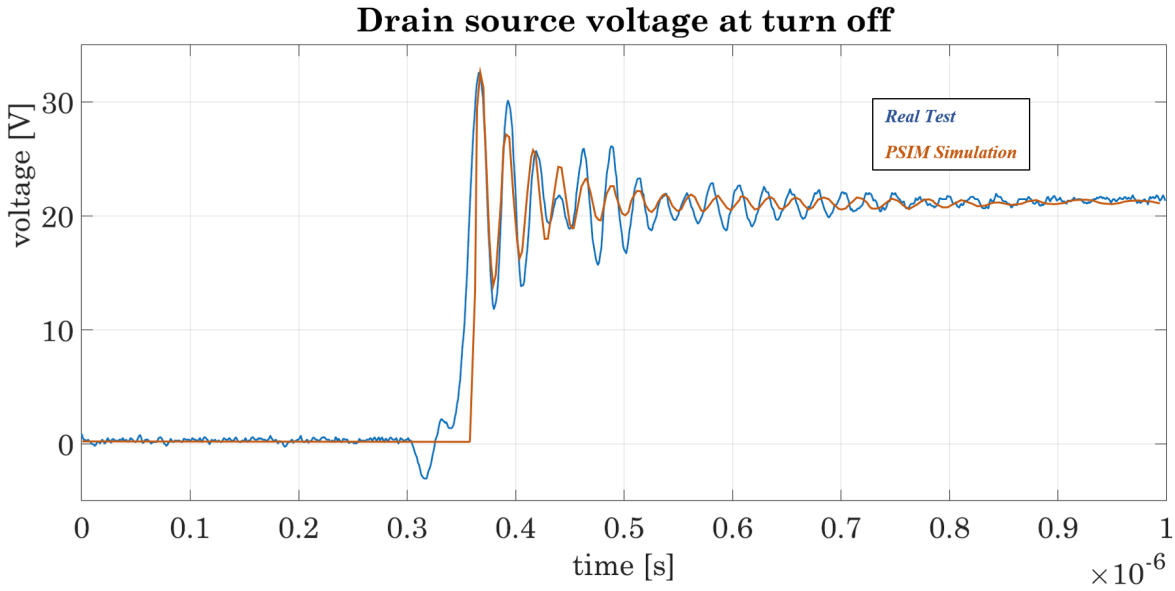


Figure 35: Comparison of the Drain-Source voltage at turn-off between real test and PSIM Simulation (Split Output)

The simulation model fits perfectly to the real behaviour of the converter with the split output topology. It can be seen that when the split output configuration is used, the peak voltage generated is reduced to a value of 33V and the turn-off transient of the MOSFET is shortened as it stabilises earlier.

After the simulations in half-bridge and split-output configurations to adjust the parameters of the model, a new simulation is carried out with the most restrictive design conditions, connecting the system to a 700 V power supply, and switching the MOSFET when the load current is 32 A. For this reason, the double pulse test periods are recalculated to obtain the required voltage and current conditions in the simulation.

$$\tau_1 = 700\ \mu H \cdot \frac{32\ A}{700\ V} \approx \mathbf{32\ \mu s}$$

After the period τ_1 is over, the high-side MOSFET begins to turn off and the load current with the value of approximately 32 A begins to decrease slowly. No more switching periods are carried out because the discharge slope of the coil current is very small, which would cause the maximum current of the system to be exceeded when the high-side MOSFET is switched on again without waiting enough time.

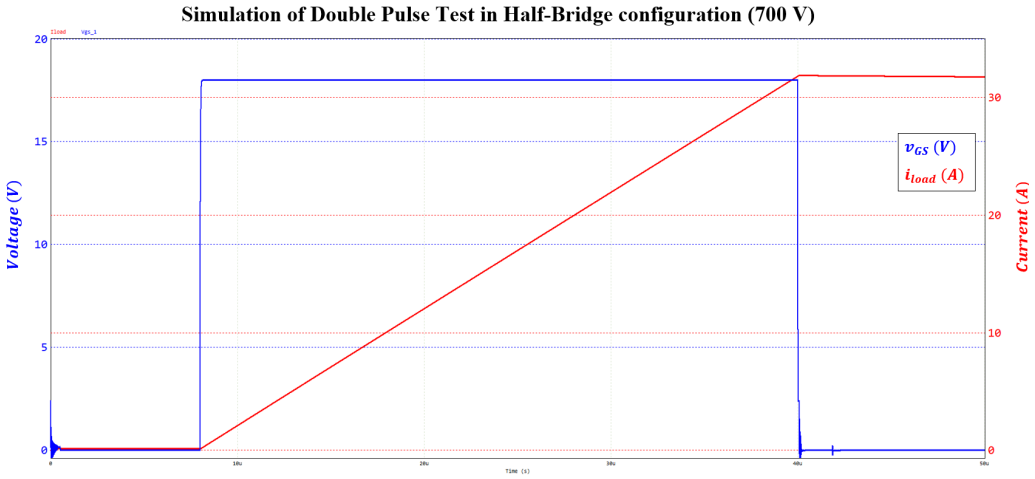


Figure 36: Simulation of the Double Pulse Test (τ_1) in Split Output configuration using PSIM (700V)

Similarly to the simulation of the converter connected to the 20V power supply, the new simulation is executed with the 700V Half-bridge and Split output configuration monitoring the drain-source voltage of the high-side MOSFET in order to see the maximum peak voltage.

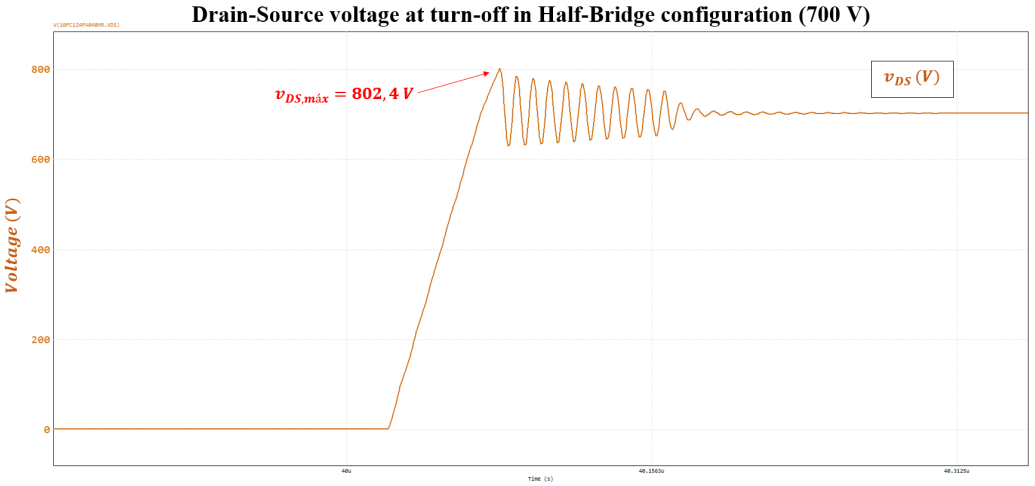


Figure 37: Drain-Source voltage at turn-off in Half bridge configuration PSIM Simulation (700V Supply)

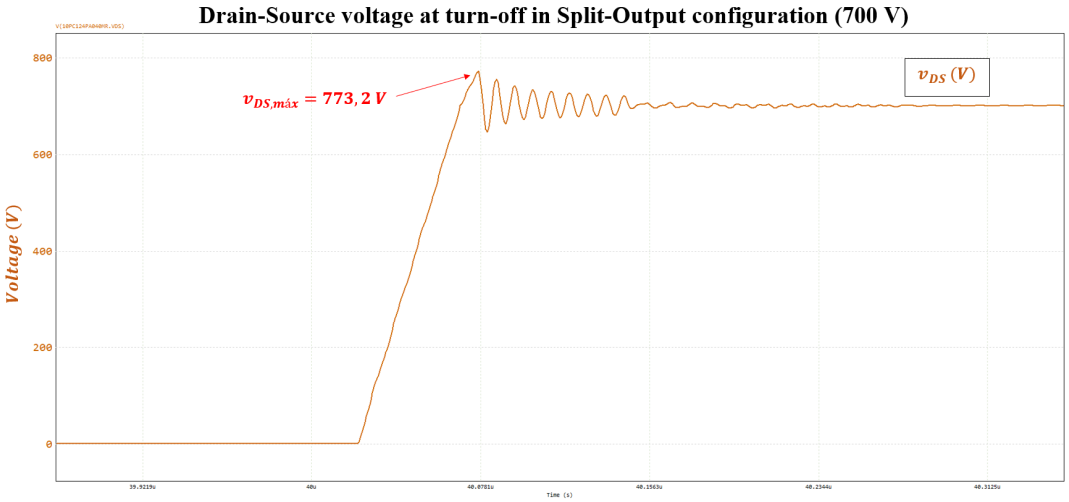


Figure 38: Drain-Source voltage at turn-off in Split output configuration PSIM Simulation (700V Supply)

The half bridge and split output configurations produce high peak voltages when the MOSFET turns off. In the half bridge configuration, a voltage between the Drain-Source terminals of 802,4 V is reached, while in the split output it is reduced to 773,2 V due to the advantages of this configuration. These high voltages can cause problems in the converter, leading to failures that compromise the durability and reliability of the system, so it is important to mitigate them.

3.2.4. New Proposed PSIM Model of the Power Unit

The proposed new model of the power unit (Figure 39) aims to improve the operating performance of the laboratory converter. For this, the new DC-Link capacitor bank proposed in section 3.2.1 is incorporated to minimise the volume occupied with a lower total cost. In addition, this new model also incorporates the snubber capacitors proposed in section 3.2.2 to reduce the peak voltage at the MOSFET Drain-Source terminals when the turn-off occurs.

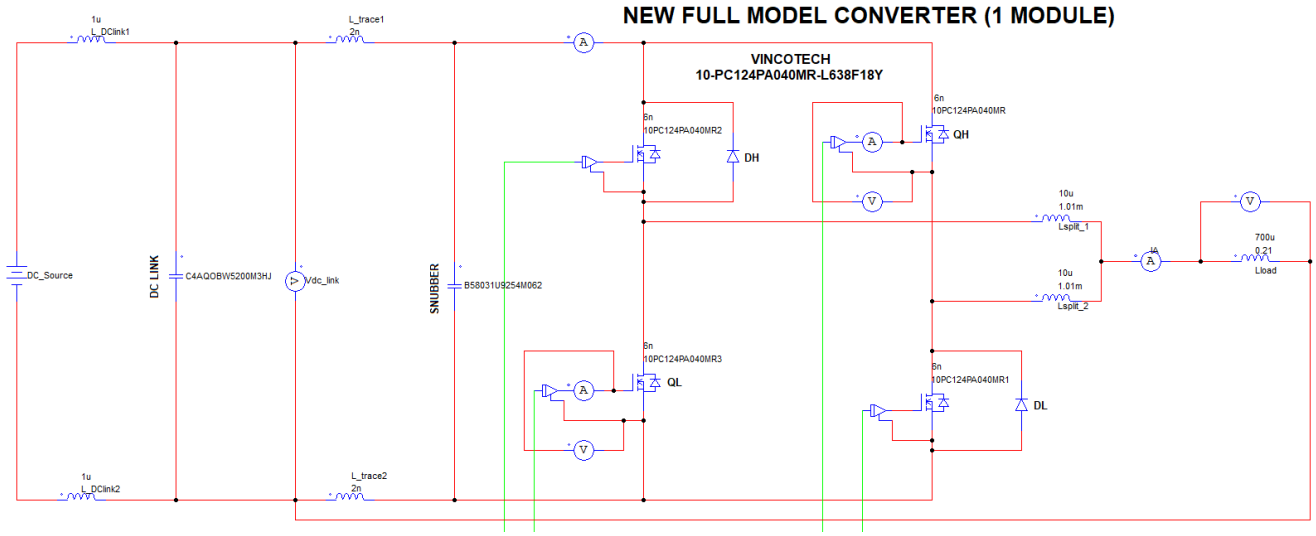


Figure 39: New Simulation Model of a single leg of the converter with snubber in PSIM

Simulations of the new proposed converter in half bridge and split output configurations are carried out in order to check the improvements in the voltage peaks at the Drain-Source terminals of the MOSFET when the DC-Link is connected to the 700V power source (Design condition).

➢ *New proposed Half bridge configuration.*

The simulated model of the proposed new half bridge configuration is shown in Figure 39. In this model, the old DC-Link is replaced by a single MKP capacitor (*C4AQOBW5200M3HJ*) and also the ceramic snubber capacitor (*B58031U9254M062*) is incorporated.

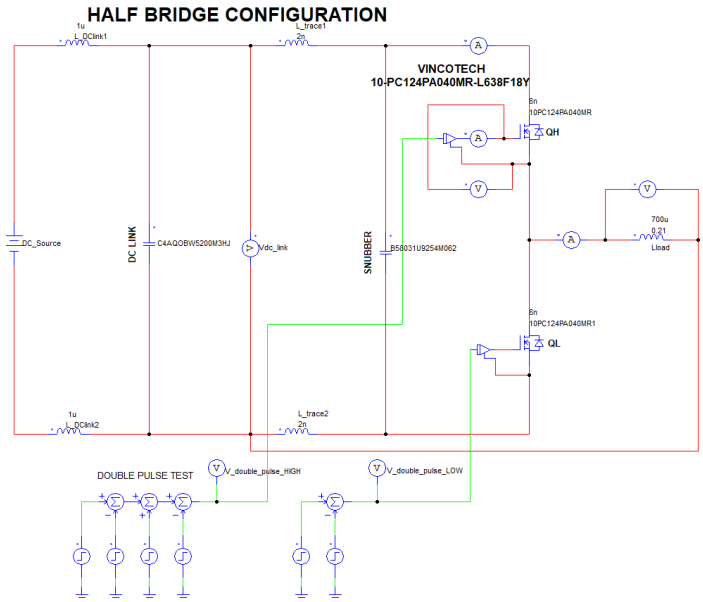


Figure 40: New Proposed Half bridge model in PSIM

Simulating the model and monitoring the voltage between the drain-source terminals of the high-side MOSFET the following plot is obtained.

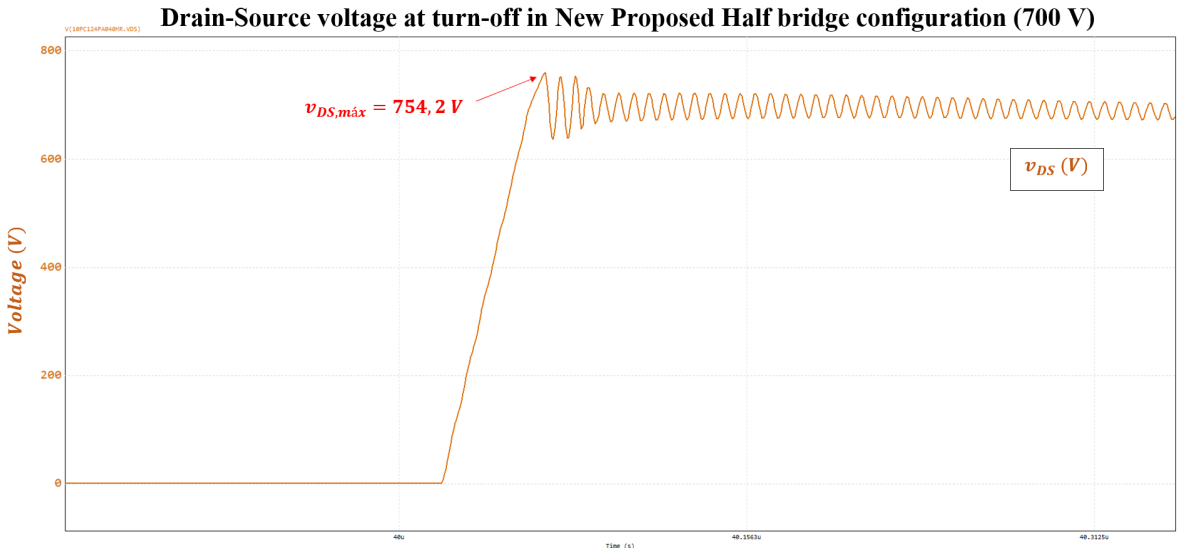


Figure 41: Drain-Source voltage at turn-off of the New proposed half bridge configuration PSIM Simulation (700V Supply)

➢ *New proposed Split Output configuration.*

The simulated model of the proposed split output configuration is shown in Figure 39. Again, the DC-Link is replaced with one MKP capacitor and the snubber is added.

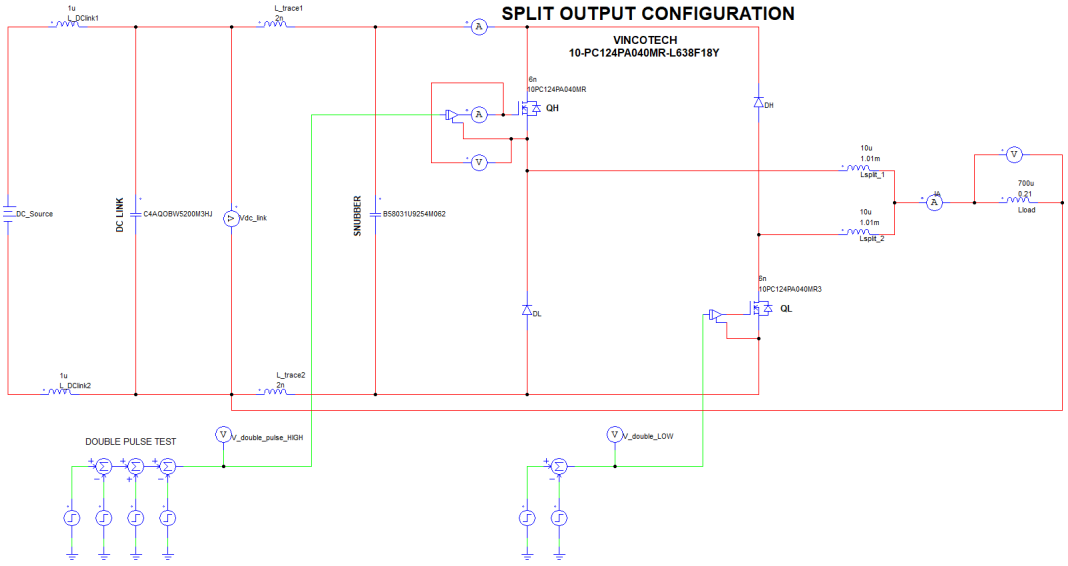


Figure 42: New Proposed Split output model in PSIM

Simulating the new model, the voltage plot of the drain-source terminals of the high-side MOSFET in the split output configuration is obtained.

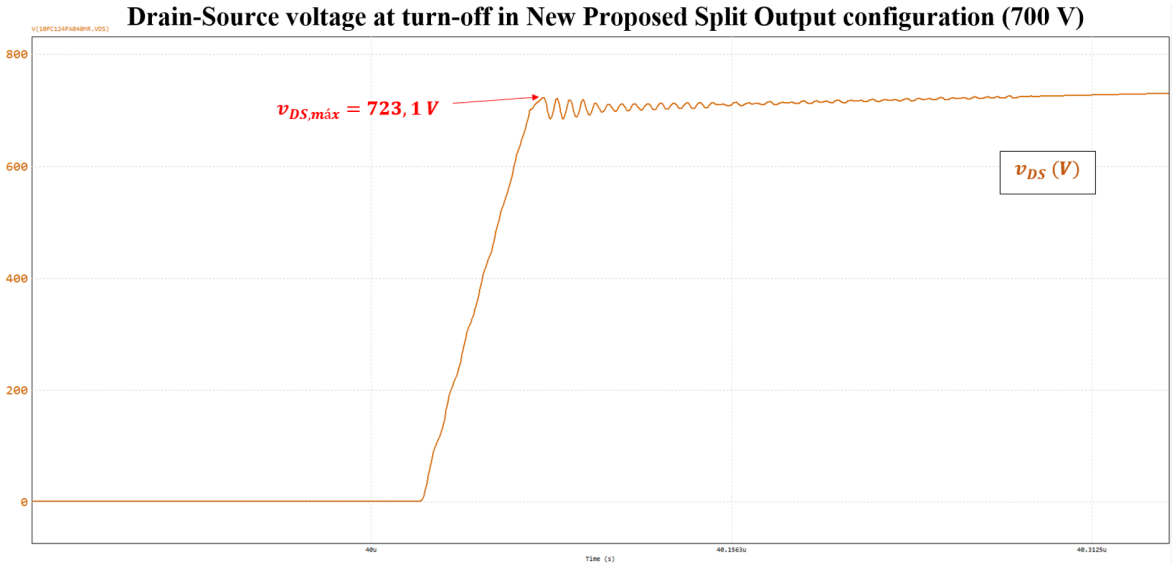


Figure 43: Drain-Source voltage at turn-off of the New proposed split output configuration PSIM Simulation (700V Supply)

Finally, it can be concluded that the addition of the snubber diode improves the system behaviour during power switching of the MOSFETs , reducing the maximum voltage peaks between their Drain-Source terminals and therefore making the system more reliable and safer. In addition, the new DC-Link, which occupies less volume and is cheaper, acts efficiently without changing the system response and keeps the voltage stable.

3.2.5. PMDC Simulation with New Model

Finally, to test the functionalities of the new models proposed in Half bridge and Split output configurations, simulations are realized for the closed-loop control of a permanent magnet DC motor (PMDC) using the unipolar modulation strategy. For this purpose, Simulink software is used for the design of the testing control algorithms and the interconnection through the PSIM SimCoupler block, which allows the co-simulation with the PSIM models of the new proposed power converter (Figure 44).

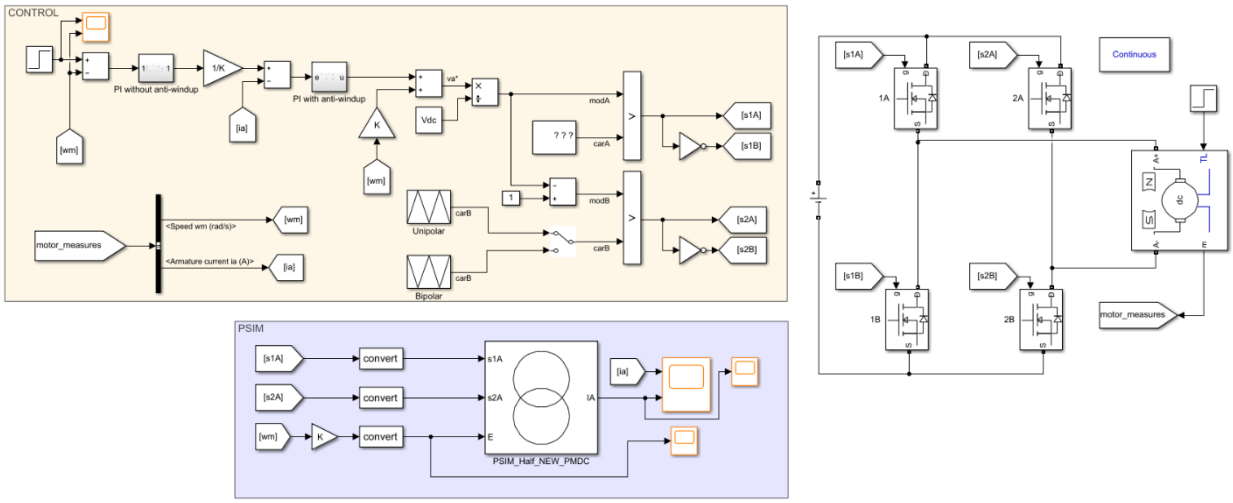


Figure 44: PMDC Control Simulink model for testing the new proposed models by the SimCoupler block

The MOSFETs are driven according to a pulse width modulation (PWM) scheme using unipolar modulation strategy, whose working principle is represented in Figure 45. A constant signal representing the desired duty cycle (Vref), is compared with a 20 kHz triangular waveform (Vtri). If, at a given discrete time instant k, the modulator signal is higher than the carrier, then the high-side switch is driven with a positive gate control signal s1A = 1; otherwise, a zero control signal s1A = 0 is provided. The low side switch, instead, is driven by a complementary control signal with respect to the high-side one.

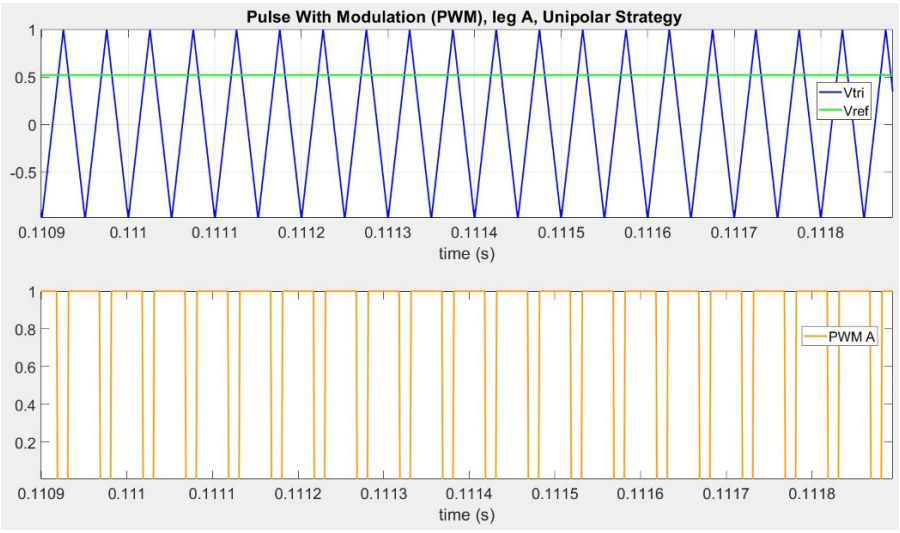


Figure 45: Working Principle of PWM for the PMDC Control using unipolar modulation strategy (leg A).

Similarly, the PWM signal using the unipolar modulation strategy that activates the MOSFET on the high side of the leg B of the new proposed converter is represented in the Figure 46.

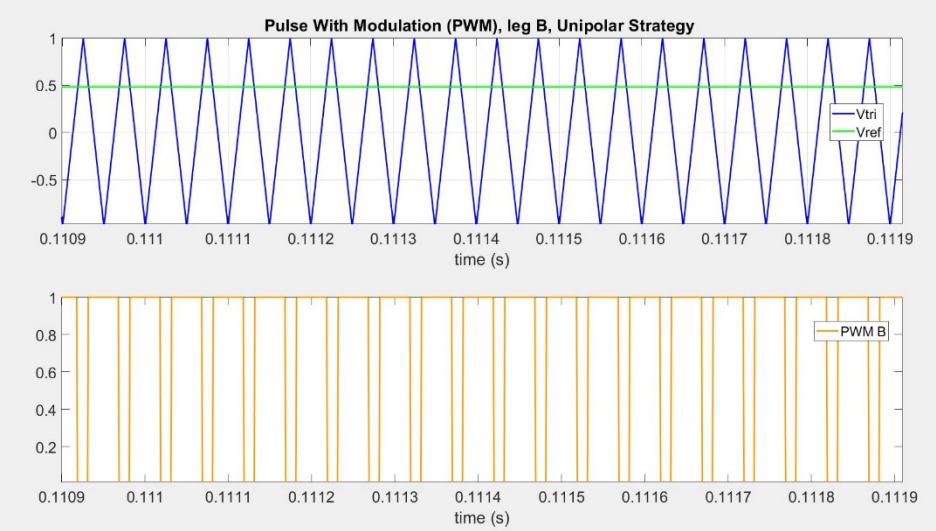


Figure 46: Working Principle of PWM for the PMDC Control using unipolar modulation strategy (leg B).

➢ *New proposed Half bridge configuration for PMDC Control.*

The new model proposed in PSIM for the control of the PMDC motor using the Half bridge configuration is shown in Figure 47. For the Co-simulation with Simulink, IN-Link and Out-Link nodes are used, in addition, the PMDC is modelled from a 0,529 H inductor with a series resistance of 0,86507 mΩ and a controlled voltage source E for the Back Electromotive Force.

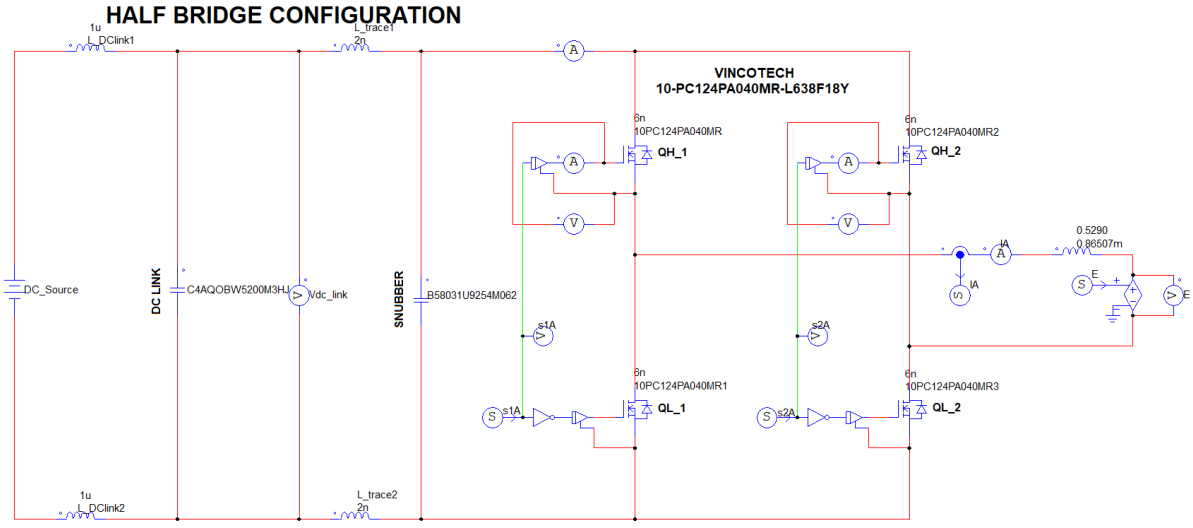


Figure 47: New Proposed Half bridge model for the PMDC Control in PSIM

The signals obtained in the simulation of the model in half bridge configuration during the control of the PMDC motor are shown in the figures below.

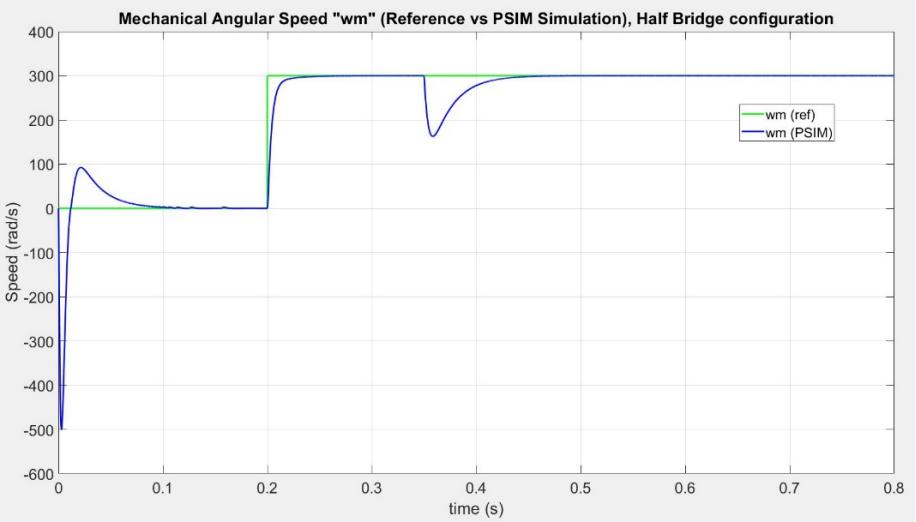


Figure 48: Mechanical Angular Speed "ω_m" (Reference vs PSIM simulation) in a Half bridge configuration

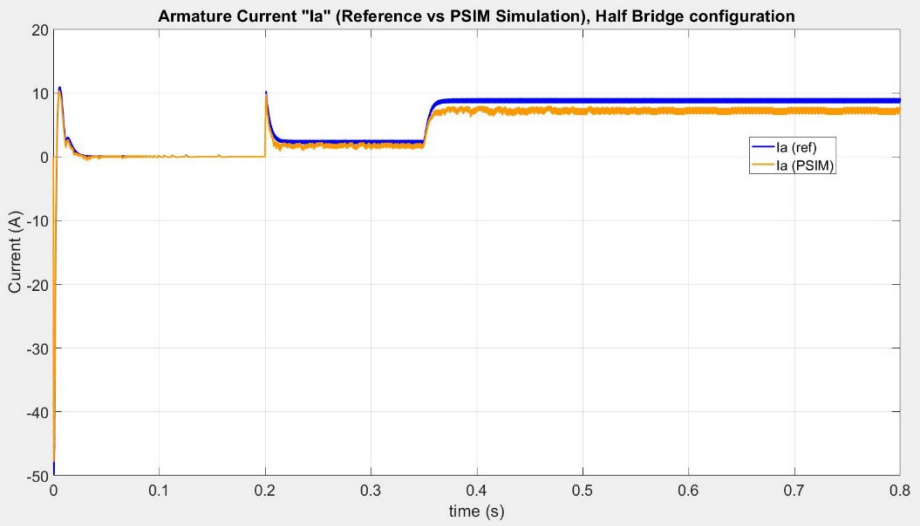


Figure 49: Armature Current "I_A" (Reference vs PSIM simulation) in a Half bridge configuration

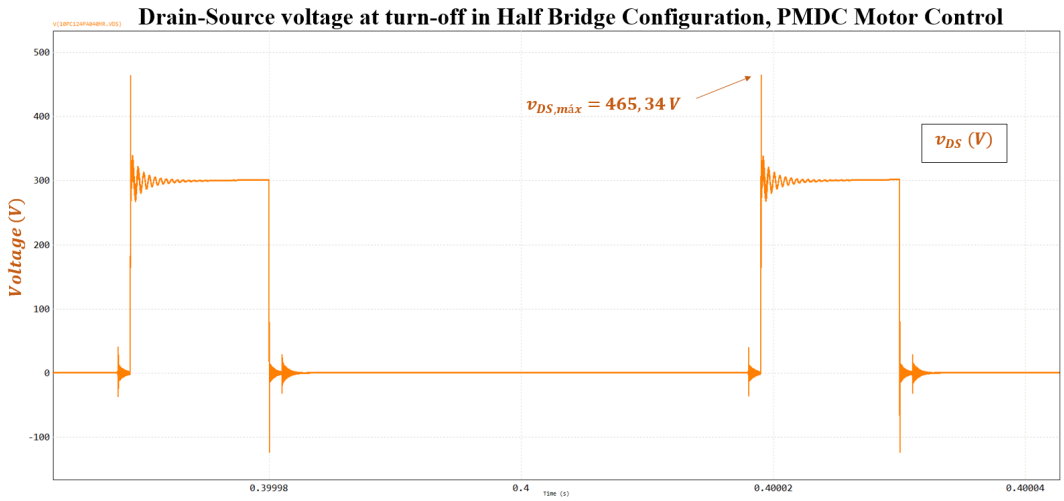


Figure 50: Drain-Source voltage at turn-off in a Half bridge configuration, PMDC Motor Control

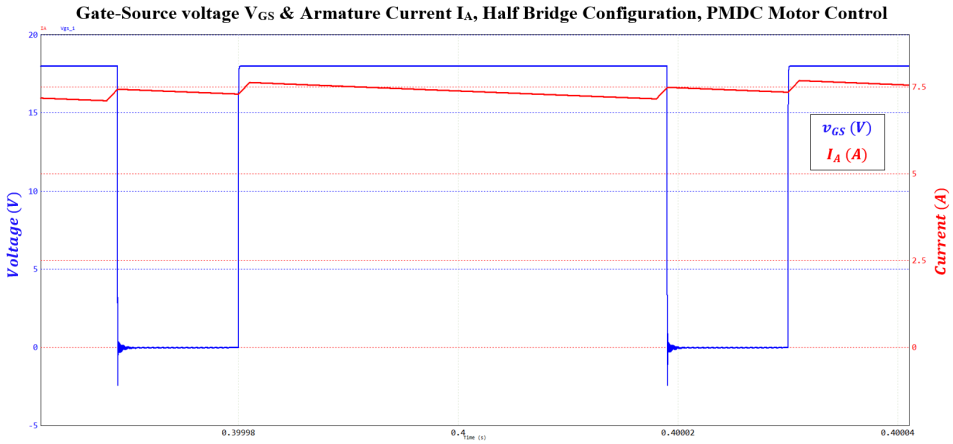


Figure 51: Gate-Source voltage "V_{GS}" & Armature Current "I_A" at turn-off in a Half bridge configuration, PMDC Control

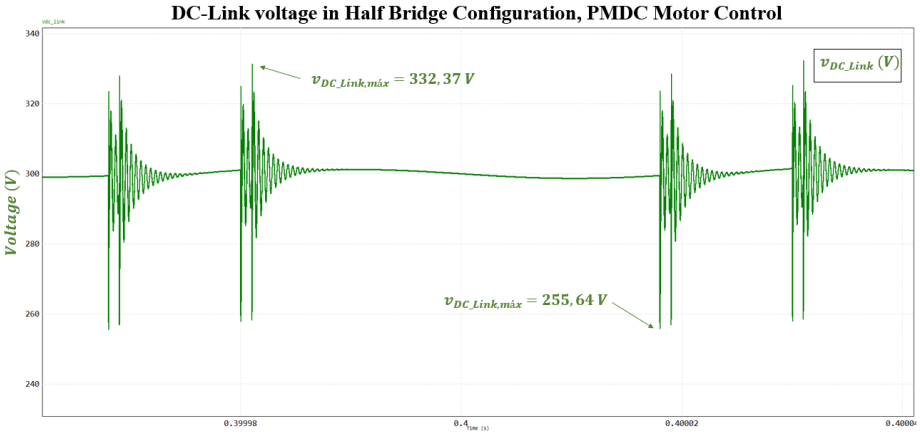


Figure 52: DC-Link voltage in a Half bridge configuration, PMDC Motor Control

➢ *New proposed Split Output configuration for PMDC Control.*

The new model proposed in PSIM for the control of the PMDC motor using the Split Output configuration is shown in Figure 53Figure 47. The split output configuration for PMDC control requires the use of two SiC MOSFET modules connected in parallel. Similarly as in the half bridge configuration for co-simulation with Simulink, the IN-Link and OUT-Link nodes are used.

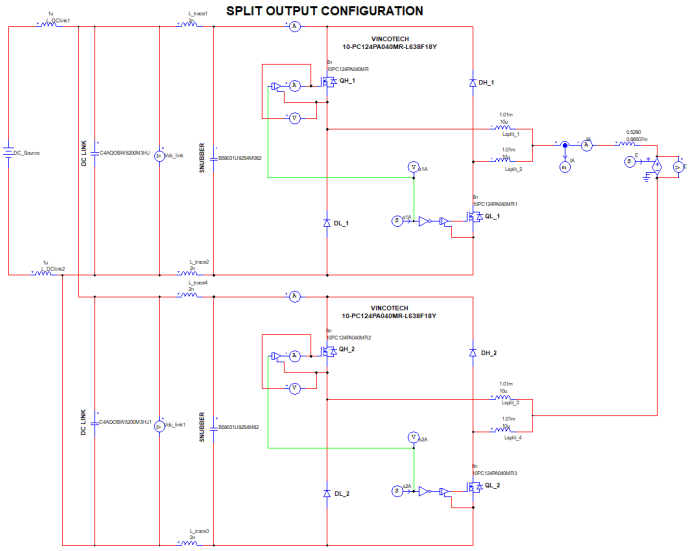


Figure 53: New Proposed Half bridge model for the PMDC Control in PSIM

The signals obtained in the simulation of the model in split output configuration during the control of the PMDC motor are shown in the figures below.

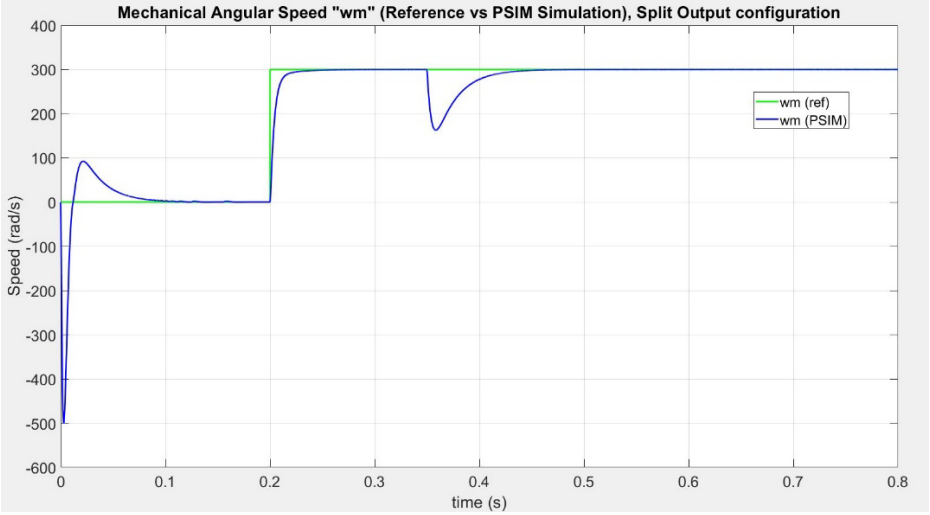


Figure 54: Mechanical Angular Speed "ω_m" (Reference vs PSIM simulation) in a Split Output configuration

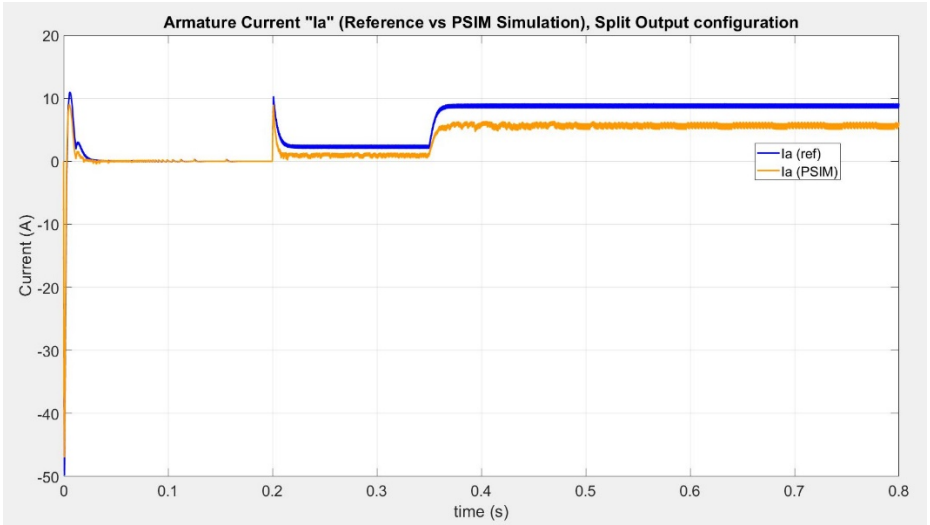


Figure 55: Armature Current "I_A" (Reference vs PSIM simulation) in a Split Output configuration

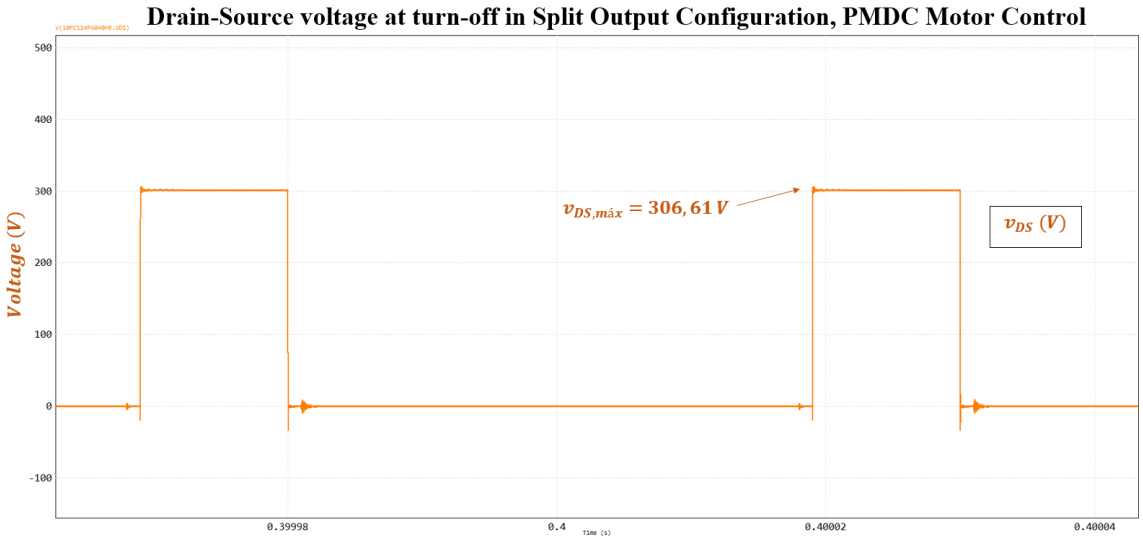


Figure 56: Drain-Source voltage at turn-off in a Split Output configuration, PMDC Motor Control

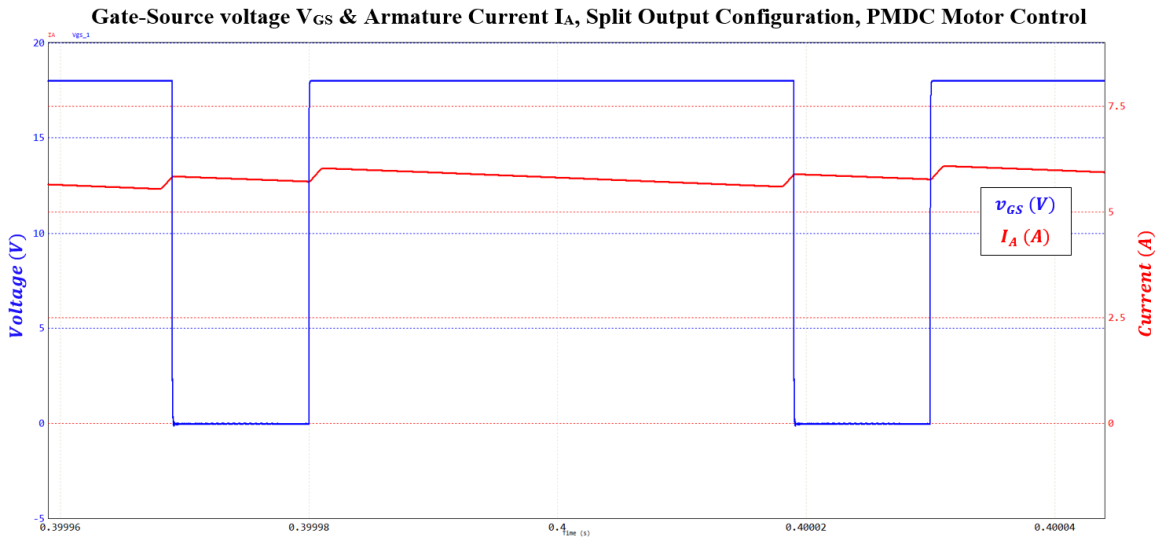


Figure 57: Gate-Source voltage "V_{GS}" & Armature Current "I_A" at turn-off in a Split Output configuration, PMDC Control

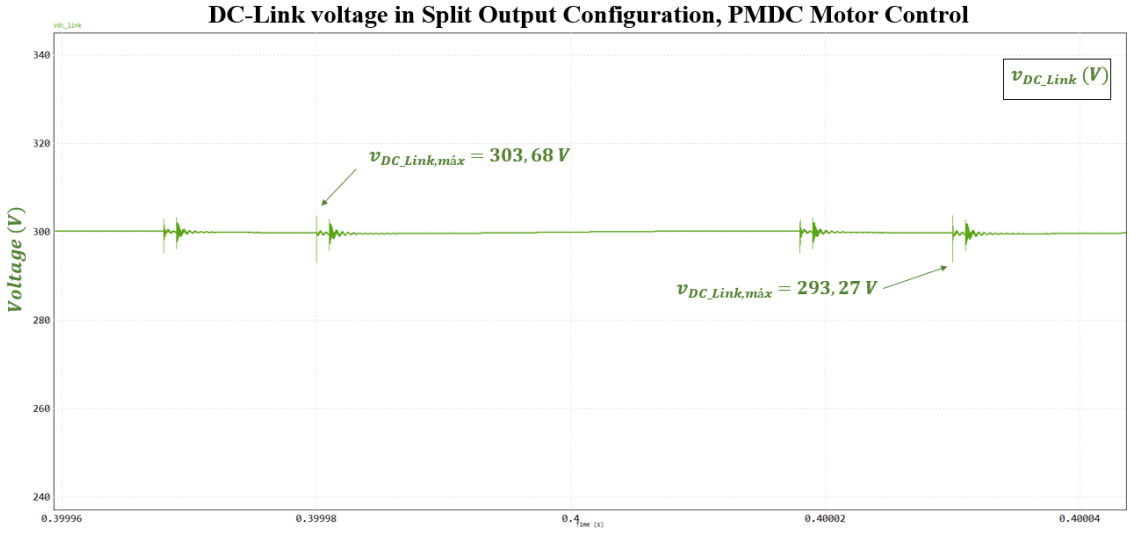


Figure 58: DC-Link voltage in a Split Output configuration, PMDC Motor Control

The figures show that the signals obtained in the simulation with the Split Output configuration have less voltage peaks in the drain-source voltage of the MOSFET and in the DC-Link voltage. This is because the PMDC motor control algorithm is not taking into account the dead times of the MOSFET, which causes phase shortages in the converter. Due to this, high voltage peaks occur in the drain-source of the MOSFETs in the half-bridge configuration. In the split output configuration, the two MOSFETs are decoupled, so this effect is avoided, and the voltage signals are much less distorted also have shorter stabilisation times.

Moreover, it can be seen that the reference angular velocity tracking is obtained by lower currents in the Split Output configuration than in the Half bridge configuration. This decrease in current is due to the improvement in conduction and switching losses in the Split Output configuration of the converter due to the incorporation of SiC Schottky diodes that conduct the free-wheeling currents.

3.3. Analysis of the Gate Driver Unit

The gate driver unit is the board that is mainly responsible for switching the different MOSFETs according to the PWM control signals it receives. In order to improve it with respect the previous design, this section analyses the gate driver unit with the aim of identifying and resolving the different faults to obtain a better system behaviour.

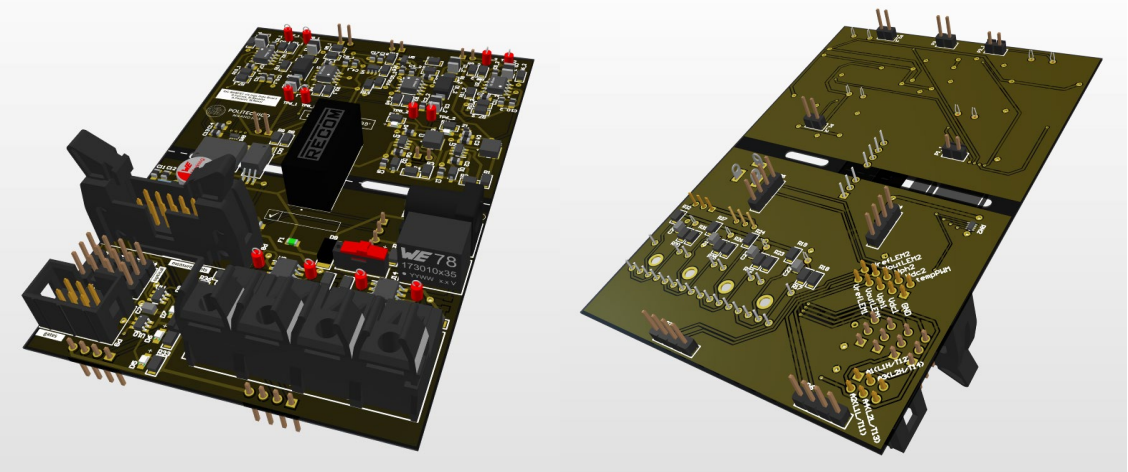


Figure 59: 3D Renders of the Gate Drive Unit in Altium

The list of the different points that were followed in this analysis to improve the performance of the gate driver unit are shown below. This list includes malfunctions of the converter with their respective solutions, as well as studies of new proposals components to improve the system and suggestions of changes from the professors who supervised the thesis work.

Gate Driver PCB

- Elimination of the optical fiber PWM control signals which are not necessary by adding signals in connector cable sets.
- Rectification of the mechanical connection between the connectors of the gate driver board and the power board
- Replacement of bootstrap technology by using isolated drivers with isolated power supply which offer multiple protection functions (Desaturation Protection, Active Miller Clamp).
- Selection of new components for the gate driver board with several alternatives in order to solve the current stock shortage problem due to the semiconductor crisis.

3.3.1. Hardware design mistakes in the Gate Driver unit

The two main mistakes in the hardware design of the gate driver board were the use of optical fiber for the PWM signals of the control and a mechanical failure between the connection boards due to an error in the position of a connector.

Fiber optic cable vs Copper wire

The use of optical fiber for the control signal transmission is not necessary in this type of application. Although the data transmission is faster when using optical fiber, its use is more recommended in network applications with long distances, but in this type of application where the connections to the control board are short, the use of copper cables for electrical connections meets the requirements of the system.

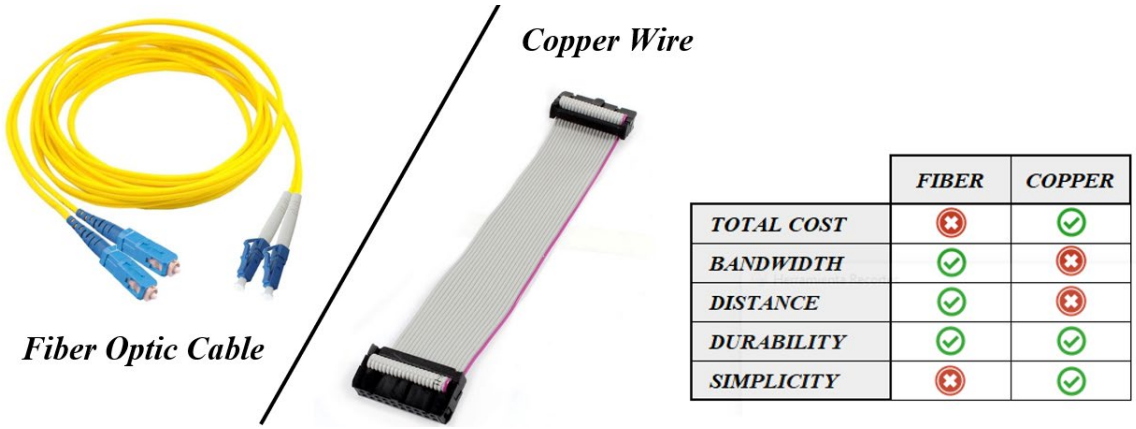


Figure 60: Fiber Optical Cable vs Copper Wire

Another property of optical fiber is that it is impervious to electromagnetic interference (EMI), which ensures that there is no coupling or distortion of the signals coming from the control board. However, by a good design and placement of the different boards with the use of copper wires for the electrical connections, the magnetic fields from the power lines that cause the electromagnetic interference can be avoided. It is recommended to position the control board in the perpendicular plane to the power plate of the converter.

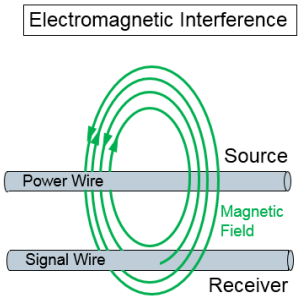
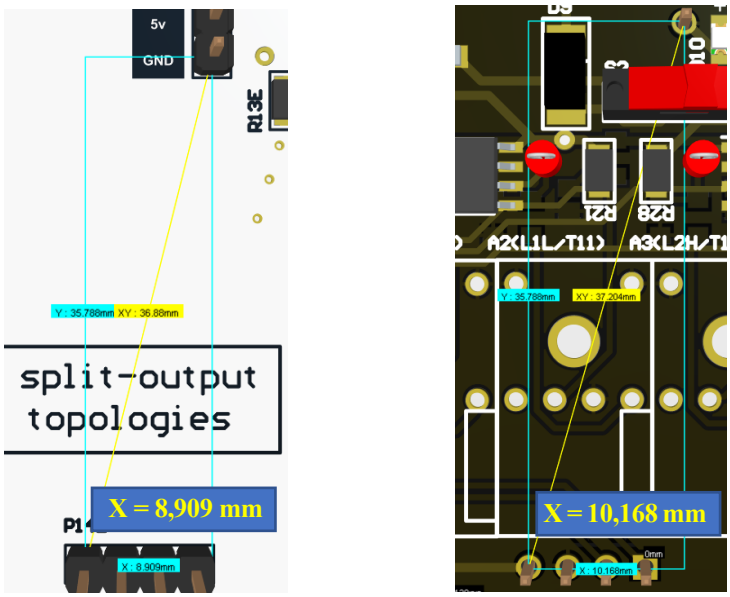


Figure 61: Electromagnetic Interference from a Power Wire to a Signal Wire

Moreover, the use of optical fiber increases the complexity and the cost of the gate driver unit. This is why it was decided to redesign the new PCB of the gate driver unit with only copper electrical connections.

Mechanical connection between gate driver board and power board

During the design of the gate driver board, the distance between the connectors on the power board and the gate driver board was incorrectly measured (Figure 62Figure 62). The two boards must be perfectly connected to each other because one is placed above the other, so this error must be corrected in the future design of the gate driver board.



a) Power Board Connector *b) Gate Driver Board connector*

Figure 62: Distances between connectors in the Power Board and the Gate Driver Board

3.3.2. Bootstrap vs Isolated Gate Driver

The gate (G) of the MOSFETs generally is driven at voltages between 10 and 15V higher than the source voltage (S). When the high-side MOSFET is turned on, voltage of the source is equal to the high voltage supplied by the DC-Link (V_{BB}). Consequently, for gate drive of the high-side MOSFET, a power supply with an even higher voltage value is required, this voltage being equal to the sum of the DC-Link voltage and the voltage required between the drain source terminals of the switch ($V_{BB} + V_{GS}$).

To realise the driving of the high-side MOSFETs one of the most popular and cost-effective ways is the bootstrap circuit, which consists of a capacitor, a diode, and a resistor (Figure 63).

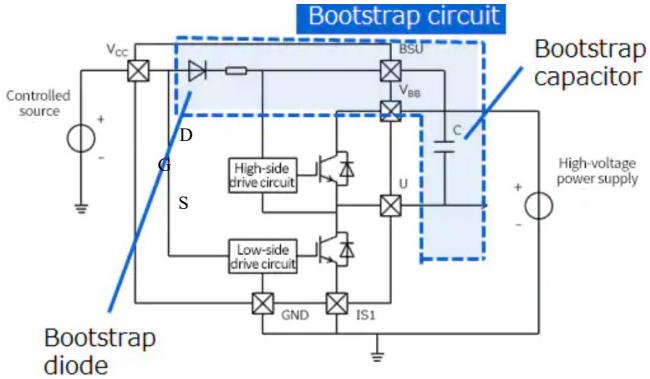


Figure 63: Example of a bootstrap circuit

When the low-side MOSFET device turns on, the bootstrap capacitor (C) stores charge, which is used to drive the gate of the high-side device (Figure 64).

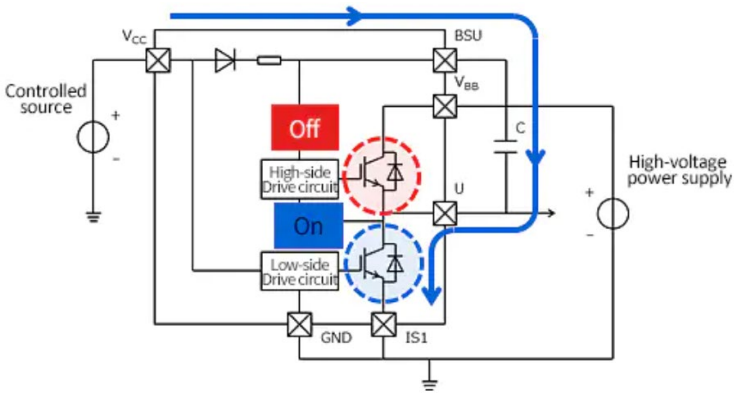


Figure 64: Bootstrap operation, low-side MOSFET turn on

In the same way when it is desired to turn on the high-side MOSFET, the charge stored in the bootstrap capacitor is used to drive this device (Figure 65).

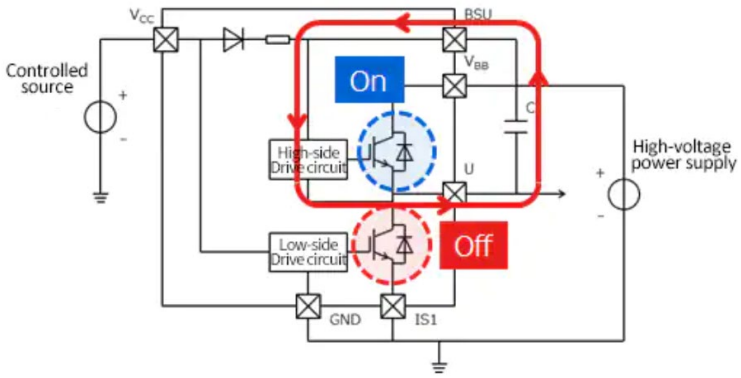


Figure 65: Bootstrap operation, high-side MOSFET turn on

The previous design of the gate driver unit board incorporates the bootstrap circuit to realise the turn-on of the MOSFETs. This circuit also implements a bypass capacitor in order to avoid voltage spikes in the power supply between the gate-source terminals of the MOSFET. The bootstrap circuit as its two modes of operation are shown in the figures below (Figure 66 and Figure 67).

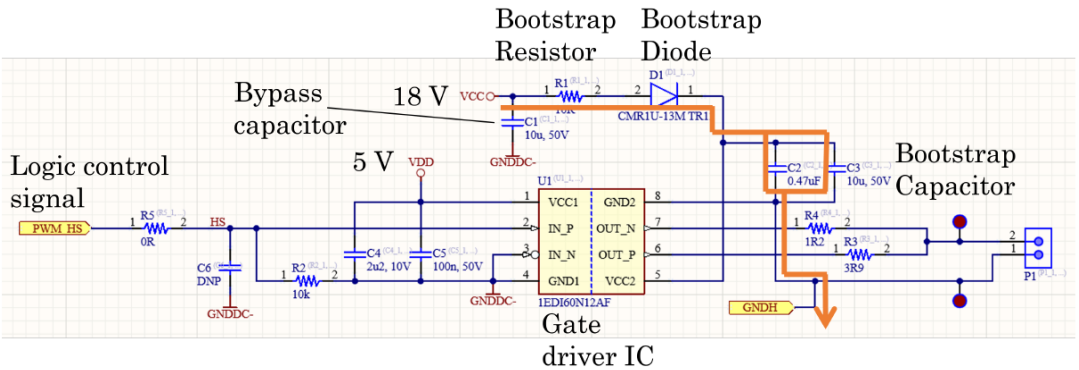


Figure 66: Bootstrap of the Gate Driver Board, charging path of the bootstrap capacitor

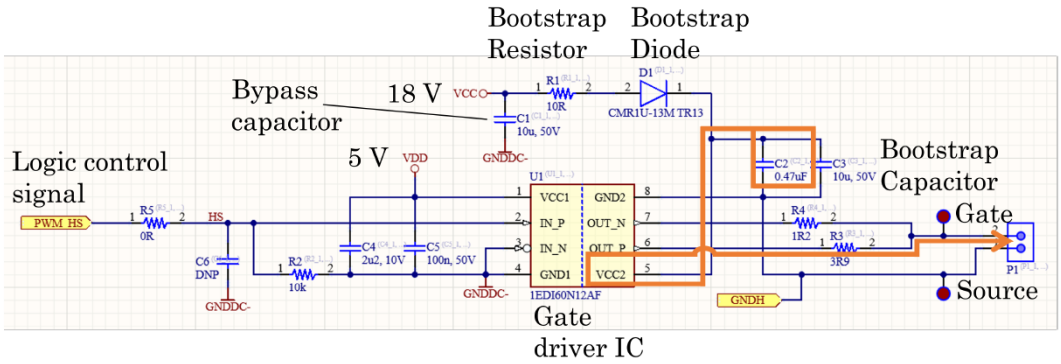


Figure 67: Bootstrap of the Gate Driver Board, discharging path of the bootstrap capacitor

The bootstrap circuit has the advantage of being simple and low cost but has some limitations. One of the limitations is that Duty-cycle and on time is limited by the requirement to refresh the charge in the bootstrap capacitor, C. This causes that 100% duty cycle is not possible on the high side drive voltage, only the low side drive voltage can work at 100% duty cycle.

The biggest difficulty with this circuit is that it is not allowed to produce negative gate voltages during turn off. The stray inductance (L_{SI}) caused by the connections between the switch and the controller reference (COM in Figure 68**¡Error! No se encuentra el origen de la referencia.**), causes a negative gate-source voltage when the MOSFET is turned off. This negative voltage present at the source of the switching device causes load current to suddenly flow in the low-side freewheeling diode, as shown in Figure 68.

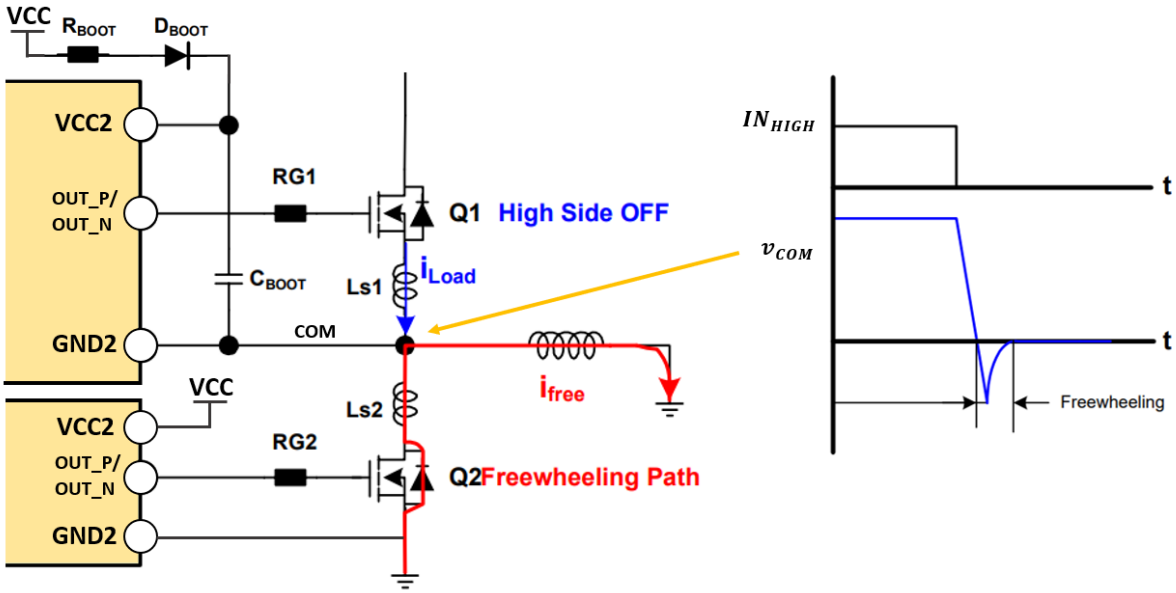


Figure 68: Freewheeling current path and Waveforms in a Half bridge application with bootstrap circuit at turn-off

This negative voltage can be trouble for the gate driver's output stage because it directly affects the GND2 pin of the high-side driver or PWM control IC and might pull some of the internal circuitry significantly below ground. The other problem caused by the negative voltage transient is the possibility to develop an over-voltage condition across the bootstrap capacitor.

Another configuration that allows MOSFETs to be driven and mitigates the limitations of the bootstrap circuit is the use of isolated DCDC converters for gate driver applications with bipolar voltage output (Figure 69).

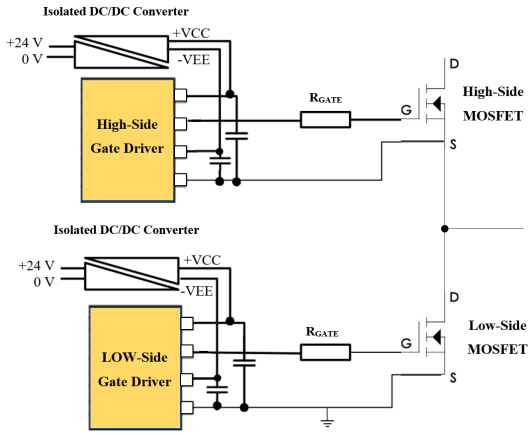


Figure 69: Isolated Gate Driver in a Half bridge configuration with Isolated DCDC Converters (Bipolar Output)

The isolated DCDC converters provides good immunity to the high dV/dt of the switch node and has a very low coupling capacitance. The isolation barrier of the drive circuit is robust and has a slow degradation over the design lifetime due to the effects of partial discharges.

The bipolar output of the isolated DCDC converters is an advantage since it enables rapid switching controlled by a gate resistor during turn-on and turn-off transients. Moreover, an appropriate negative drive ensures that the gate-source turn-off voltage is always actually zero or less and also helps to overcome the effect of drain to gate 'Miller' capacitance (C_{GD}) which works to inject current into the gate drive circuit on device turn-off.

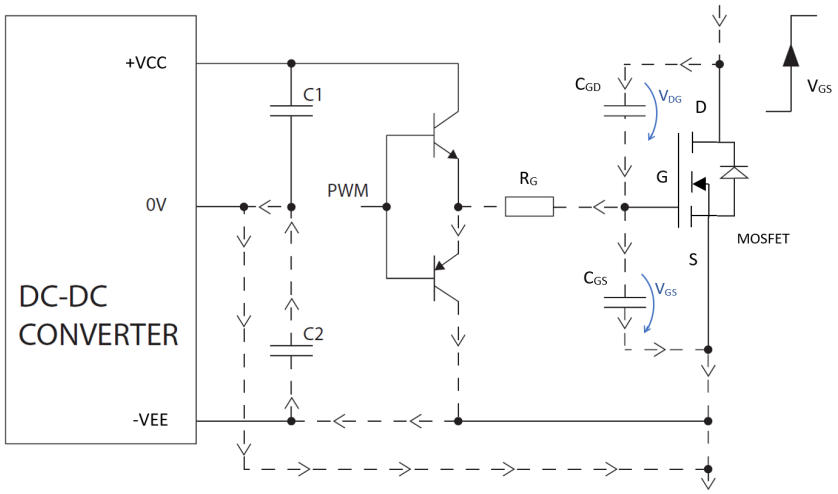


Figure 70: Current Through "Miller" capacitance (C_{GD}) opposes switch off

When an MOSFET is driven off, the drain-gate voltage (V_{DG}) rises and current of value $C_{GD} \cdot dV_{DS}/dt$ flows through the Miller capacitance into the gate to source capacitance C_{GS} and through the gate resistor to the driver circuit. The resulting voltage V_{GS} on the gate can be sufficient to turn the device on again with possible shoot-through and damage. Driving the gate of the MOSFET to a negative voltage mitigates this effect.

3.3.3. Selection of New Component to the Gate Driver Unit

Finally, a selection of components is required to improve the design of the new gate driver board in order to achieve a better performance during the operation of the converter. This selection replaces the bootstrap method through the incorporation of isolated DCDC converters with bipolar voltage output in a distributed architecture (Figure 71) and changes the current isolated gate drivers by more advanced ones in terms of functionalities and performance.

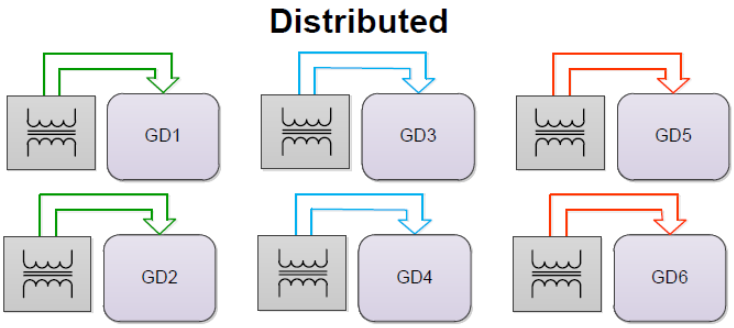


Figure 71: Distributed gate driver architecture

The new components are selected focusing on the optimal operation of the board, minimising the waiting periods in stock due to the silicon crisis and with the possibility of using multiple options for not to depend only on one product.

Murata DCDC Isolated *MGJ2D*:

The MGJ2D of Murata is a series of isolated DCD converters ideal for the powering high-side and low-side gate drive circuits for MOSFETs in bridge circuits (Figure 72). A choice of asymmetric output voltages allows optimum drive levels for best system efficiency and EMI. The MGJ2 series is characterised for high isolation and dV/dt requirements commonly seen in bridge circuits used in motor drives and inverters, while the MGJ2 industrial grade temperature rating and construction gives long service life and reliability.

Figure 72: Isolated DCDC Converter MGJ2D series from Murata

The MGJ2 is the only series which provides bipolar voltage outputs in the +22V/-5V range and allows 24V input voltages. For this reason, it perfectly meets the hardware requirements which implements the Vincotech module that supports a range of V_{GS} voltages between +22V/-4V and has an external power supply of 24V input.

The model of the series chosen for the isolated DCDC converter was the "*MGJ2D241802SC"* whose main characteristics are shown in the Table 7. Other model options that are also valid: *MGJ2D241503SC, MGJ2D242003SC.*

Model	MGJ2D241802SC
Supplier	Murata Power Solutions
Nominal Input Voltage	24 V
Output Voltage 1 / 2	+18 V / -2,5V
Output Current 1 / 2	80 mA / 80 mA
Efficiency (Typ)	80 %
Isolation Capacitance	4 pF
Isolation Voltage (Hi Pot Test)	5,2 kVDC
Common Mode Transient Immunity (CMTI)	> 200 kV/us

Table 7: MGJ2D241802SC main characteristics

Driver Infineon *EiceDRIVER 1ED34x1Mc12M*:

The EiceDRIVER 1ED34x1Mc12M series from Infineon (Figure 73) are a series of single-channel high-voltage isolated gate driver ICs with integrated coreless transformer (CLT) technology. The ICs are designed for use with 650 V, 1200 V, 1700 V, and 2300 V IGBTs, silicon and silicon-carbide MOSFETs.

Figure 73: Isolated Gate Driver 1ED34x1Mc12M series from Infineon

The 1ED34x1Mc12M series also implements numerous functionalities that provide security for the correct switching of the SiC MOSFETs. These functionalities are the Desaturation Protection, Active Miller clamp, Undervoltage lockout protection and more.

The model of the series chosen for the isolated gate driver was the "*1ED3431MC12MXUMA1"* whose main characteristics are shown in the Table 8. Other model options that are also valid: *1ED3461MC12M, 1ED3491MC12M, 1ED3431MU12M, 1ED3461MU12M, 1ED3491MU12M.*

Model	1ED3431MC12MXUMA1
Supplier	Infineon
Supply Voltage Input Side	3.3 V or 5 V
Positive supply Voltage Output	+13 V / +25 V
Negative supply Voltage Output	-25 V / 0 V
Supply Voltage Difference Output	13 V (min.) / 35 V (max.)
Peak Output Current	± 3 A
Maximum switching frequency	fsw = 250 kHz
Isolation Capacitance	1,7 pF
Isolation Voltage	5,2 kVDC
Common Mode Transient Immunity (CMTI)	200 kV/us

Table 8: 1ED3431MC12MXUMA1 main characteristics

The *MGJ2D241802SC* isolated DCDC converter and the gate driver *1ED3431MC12MXUMA1* are compatible with each other. The voltage and current ranges are within the hardware requirements and the isolation characteristics are very similar so both will provide good performance. The connection scheme of the gate drivers and the DCDC power supplies is the half bridge configuration that will be followed, is shown in the Figure 74.

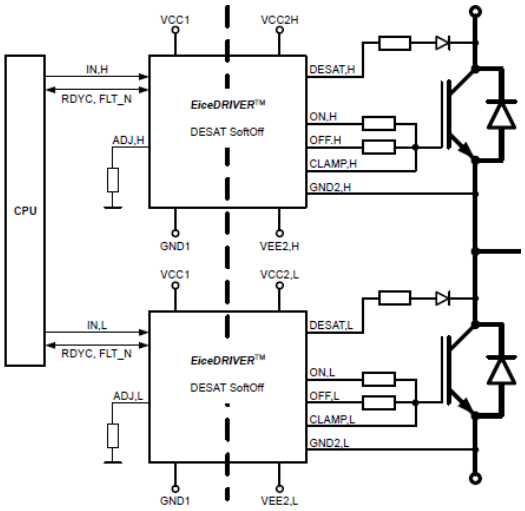


Figure 74: Connections of the EiceDriver in a typical Half bridge configuration

4. NEW HARDWARE DESIGN OF THE GATE DRIVER BOARD

In this section, the gate driver board is redesigned. This new design solves the different mistakes of the previous gate driver board and implements the new isolated DCDC converter technologies with new improved gate drivers to increase the performance of the three-phase split output converter with SiC MOSFETs and SiC Schottky diodes.

4.1. Schematics

Before starting with the hardware design, it is important to be clear about all the input and output signals of the gate driver board. Selecting the signals of interest, choosing a connector that complies with the established conditions and showing a brief description of its purpose if required. To do this, the signals have been distributed into inputs and outputs and, at the same time, according to their origin and destination. This organisation can be seen in the table below.

Connector	Pin	Label	Origin	Destination	Type	Range	Description
Power Jack (J1)	1	V_BAT	Battery	Gate Drivers	Analog	24 V	-
	2/3	GND_LOW	Battery	Gate Drivers	Analog	REF	-
Molex 14 (P8)	1	GND_LOW	Gate Drivers	Control Board	Analog	REF	-
	2	TEMP_PWM_OUT	Gate Drivers	Control Board	APWM	0 – 5 V	Temperature of the SiC MOSFET module
	3	VDClink1	Gate Drivers	Control Board	Analog	0 – 3,3 V	Measurement of DC-Link voltage
	4	VDClink2	Gate Drivers	Control Board	Analog	0 – 3,3 V	Measurement of DC-Link voltage
	5	VPH1	Gate Drivers	Control Board	Analog	0 – 3,3 V	Measurement of the phase of the DC-Link
	6	VPH2	Gate Drivers	Control Board	Analog	0 – 3,3 V	Measurement of the phase of the DC-Link
	7	VrefLEM1	Control Board	Gate Drivers	Analog	0 – 4 V	Reference voltage of the current sensor
	8	VoutLEM1	Gate Drivers	Control Board	Analog	0 – 5 V	Measurement of the phase current
	9	VrefLEM2	Control Board	Gate Drivers	Analog	0 – 4 V	Reference voltage of the current sensor
	10	VoutLEM2	Gate Drivers	Control Board	Analog	0 – 5 V	Measurement of the phase current
	11	IN_H1	Control Board	Gate Drivers	Digital	0 – 3,3 V	PWM Signal MOSFET H1
	12	IN_L1	Control Board	Gate Drivers	Digital	0 – 3,3 V	PWM Signal MOSFET L1
	13	IN_H2	Control Board	Gate Drivers	Digital	0 – 3,3 V	PWM Signal MOSFET H2
	14	IN_L2	Control Board	Gate Drivers	Digital	0 – 3,3 V	PWM Signal MOSFET L2

Connector	Pin	Label	Origin	Destination	Type	Range	Description
Molex 4 (P1)	4	+5V_LOW1	Gate Drivers	Power Board	Analog	5 V	-
	3	GND_LOW	Gate Drivers	Power Board	Analog	REF	-
	2	VoutLEM1	Power Board	Gate Drivers	Analog	0 – 5 V	Measurement of the phase current
	1	VrefLEM1	Gate Drivers	Power Board	Analog	0 – 4 V	Reference voltage of the current sensor
Molex 4 (P2)	4	VDClink1	Power Board	Gate Drivers	Analog	0 – 3,3 V	Measurement of DC-Link voltage
	3	VPH1	Power Board	Gate Drivers	Analog	0 – 3,3 V	Measurement of the phase of the DC-Link
	2	+5V_LOW1	Gate Drivers	Power Board	Analog	5 V	-
	1	GND_LOW	Gate Drivers	Power Board	Analog	REF	-
Molex 4 (P9)	4	+5V_LOW2	Gate Drivers	Power Board	Analog	5 V	-
	3	GND_LOW	Gate Drivers	Power Board	Analog	REF	-
	2	VoutLEM2	Power Board	Gate Drivers	Analog	0 – 5 V	Measurement of the phase current
	1	VrefLEM2	Gate Drivers	Power Board	Analog	0 – 4 V	Reference voltage of the current sensor
Molex 4 (P10)	4	VDClink2	Power Board	Gate Drivers	Analog	0 – 3,3 V	Measurement of DC-Link voltage
	3	VPH2	Power Board	Gate Drivers	Analog	0 – 3,3 V	Measurement of the phase of the DC-Link
	2	+5V_LOW2	Gate Drivers	Power Board	Analog	5 V	-
	1	GND_LOW	Gate Drivers	Power Board	Analog	REF	-
Molex 1 (P11)	1	D1_1	Power Board	Gate Drivers	Analog	700 V	Drain terminal of the MOSFET
Molex 2 (P3)	1	S1D2_1	Power Board	Gate Drivers	Analog	REF	Source/Drain terminal of the MOSFET
	2	G1_1	Gate Drivers	Gate Drivers	Analog	-2,5 V – 18 V	Gate terminal of the MOSFET
Molex 2 (P4)	1	G2_1	Gate Drivers	Gate Drivers	Analog	-2,5 V – 18 V	Gate terminal of the MOSFET
	2	S2_1	Gate Drivers	Gate Drivers	Analog	REF	Source terminal of the MOSFET
Molex 1 (P12)	1	D1_1	Gate Drivers	Gate Drivers	Analog	700 V	Drain terminal of the MOSFET
Molex 2 (P6)	1	S1D2_1	Power Board	Gate Drivers	Analog	REF	Source/Drain terminal of the MOSFET
	2	G1_1	Power Board	Gate Drivers	Analog	-2,5 V – 18 V	Gate terminal of the MOSFET
Molex 2 (P7)	1	G2_1	Power Board	Gate Drivers	Analog	-2,5 V – 18 V	Gate terminal of the MOSFET
	2	S2_1	Power Board	Gate Drivers	Analog	REF	Source terminal of the MOSFET
Molex 2 (P5)	1	NTC-	Power Board	Gate Drivers	Analog	REF	NTC Terminal of the MOSFETs Module
	2	NTC+	Power Board	Gate Drivers	Analog	0 – 5 V	NTC Terminal of the MOSFETs Module

Table 9: Gate driver board input and output signals and properties

Isolated DCDC Converter (MGJ2D241802SC)

For the MGJ2D241802SC isolated DCDC converter, the manufacturer's recommendations have been followed to ensure good performance of the component (Figure 75). It is recommended to place an LC filter at the input, with the values shown in the figure below, to reduce the common mode current and at the same time reduce the possible interference with the circuits on the primary side. Also on the input side, it can be seen the protection with a fuse to ensure that there are no overcurrents higher than 1 A that could damage the device.

At the output of the converter a decoupling capacitor bank can be observed. These capacitors are used to prevent voltage peaks in the output signal of the circuit, making the signal as flat as possible. This avoids any possible negative effects that could have an undesired impact on the operation of the gate driver. For the dimensioning of its capacitance, calculations are made with the aim of ensuring that the output voltage does not drop more than 0.5V.

$$E = Q_g \cdot (V_{DD} - V_{EE}) = 107\ nC \cdot 20{,}5\ V = 2{,}194\ uJ$$

$$E_1 = \frac{18}{20{,}5} \cdot 2{,}194\ uJ = 1{,}926\ uJ = \frac{1}{2} \cdot C_1 \cdot (18^2 - 17{,}5^2) \rightarrow \boldsymbol{C_1 = 0.217\ uF}$$

$$E_2 = \frac{2{,}5}{20{,}5} \cdot 2{,}194\ uJ = 0{,}268\ uJ = \frac{1}{2} \cdot C_2 \cdot (2{,}5^2 - 2^2) \rightarrow \boldsymbol{C_2 = 0.238\ uF}$$

After calculating the necessary output capacitors, the manufacturer recommends to keep the capacitance values below 220uF, because the higher the capacitance, the higher the start-up time. Following this recommendation, capacitors with different output values are selected to filter different frequencies without exceeding this limit.

Finally, at the output of the circuit, it can be seen the fuses of 1A breaking current that protect the components that the DCDC converter supplies. To visually check the general status of the system and these fuses, a series of different coloured LEDs have been installed, one for each bipolar output voltage.

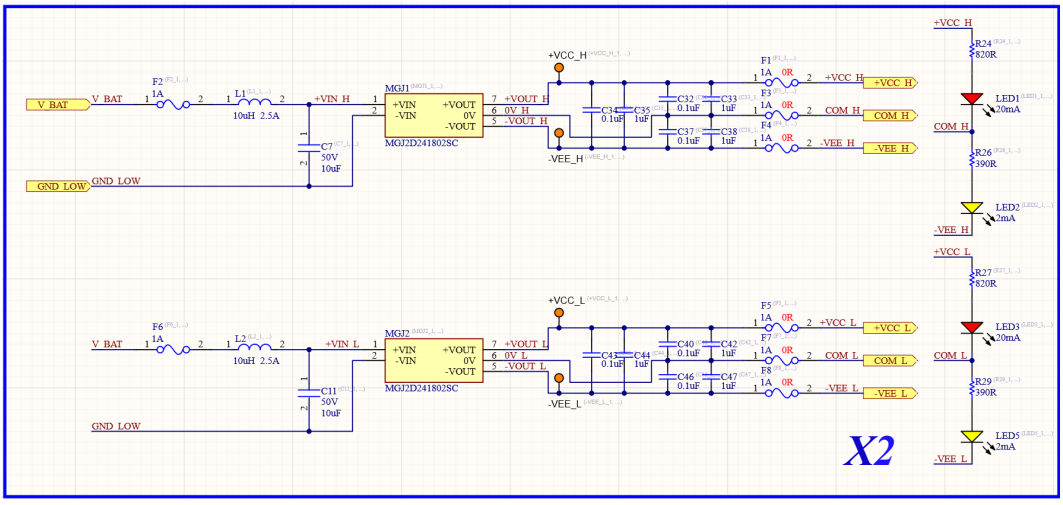


Figure 75: Schematic circuit diagram of the Isolate DCDC converter MGJ2D241802SC

5V voltage regulator (LM2937IMP-5.0)

A 5V regulator *LM2937IMP-5.0* is installed for each phase of the SiC MOSFET module (Figure 76) and another regulator for the power supply of the low voltage part in the isolated part of the NTC circuit (Figure 77). It has been decided to use many 5V voltage regulators because the power that they can supply is quite low (2,5 W) and this solution avoids problems when supplying power to the different systems.

The regulators on the low voltage side are directly supplied from the input battery while the regulator for the isolated NTC is supplied through the isolated MURATA DCDC converter on the low side.

For the correct operation of the regulator circuit, the manufacturer Texas Instruments recommends the use of a 0.1 uF decoupling capacitor at the input and a 10 uF capacitor at the output. In addition, a fuse is placed at the output to protect the component from higher currents than it can withstand.

In order to know if it is working correctly and 5 V are set at the output, an LED has been positioned to visually indicate the status of the regulator.

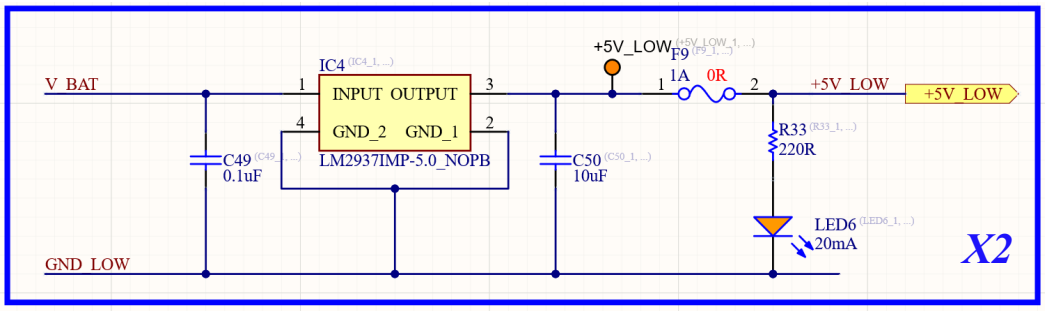


Figure 76: Schematic circuit diagram of the 5V regulator LM2937IMP-5.0, SiC Module phase supply

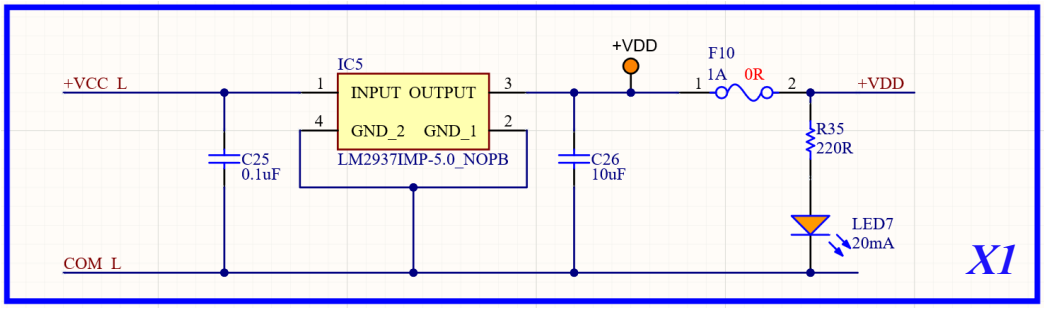


Figure 77: Schematic circuit diagram of the 5V regulator LM2937IMP-5.0, NTC isolated supply

Single-channel Isolated Gate Driver (1ED3431MC12MXUMA1)

In order to explain in detail the schematic design of the gate driver 1ED3431MC12MXUMA1, it is necessary to have a detailed description of its pinout and functionalities of its pins. Figure 78 shows the component package with its pinout, which includes the pin names and a table showing the functionality of each pin.

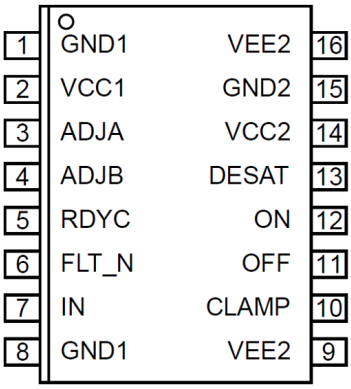


Table 3 Pin configuration

Pin no.	Pin name	Pin type	Buffer type	Pull device	Function
1	*GND1*	GND	–	–	Ground input side
2	*VCC1*	PWR	–	–	Positive power supply input side
3	*ADJA*	AI	special	CS	Parameter adjust set A
4	*ADJB*	AI	special	CS	Parameter adjust set B
5	*RDYC*	I/O	OD, CMOS	–	Combined ready output, high active and fault clear input and soft-off input, low active
6	*FLT_N*	I/O	OD, CMOS	–	Fault output, low active and soft- off input, low active
7	*IN*	I	CMOS	PD, 40 kΩ	Non inverted driver input
8	*GND1*	GND	–	–	Ground input side
9	*VEE2*	GND	–	–	Negative power supply output side
10	*CLAMP*	PWR	OD	–	Active Miller clamping, open drain to VEE2 (1ED3431M only)
10	*CLAMPDRV*	PWR	PP	–	Active miller clamping, clamp driver for external MOSFET (1ED3461M, 1ED3491M)
11	*OFF*	PWR, AI	OD	–	Driver sink output
12	*ON*	PWR, AI	OD	–	Driver source output
13	*DESAT*	AI	special	CS, 500 µA	Enhanced desaturation protection
14	*VCC2*	PWR	–	–	Positive power supply output side
15	*GND2*	AI	–	–	Signal ground output side
16	*VEE2*	GND	–	–	Negative power supply output side

Figure 78: Pinout and functionalities of the isolated gate driver 1ED3431MC12MXUMA1

For the power supply of the driver logic, a protective zener diode has been installed which will maintain a certain voltage between its terminals. Additionally, in order to maintain constant supply voltages without voltage peaks or interference on both sides of the device, it incorporates different decoupling capacitors (Figure 79).

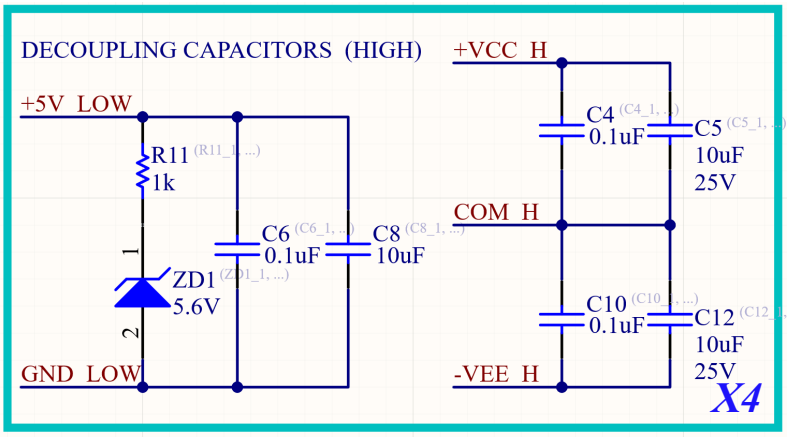
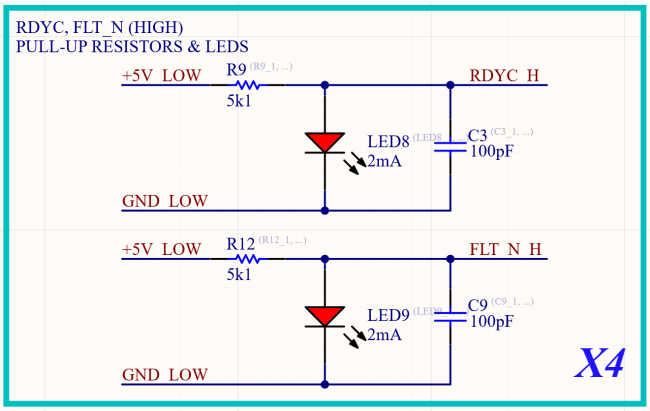


Figure 79: Schematic of the supply circuit of the Isolated gate driver 1ED3431MC12MXUMA1

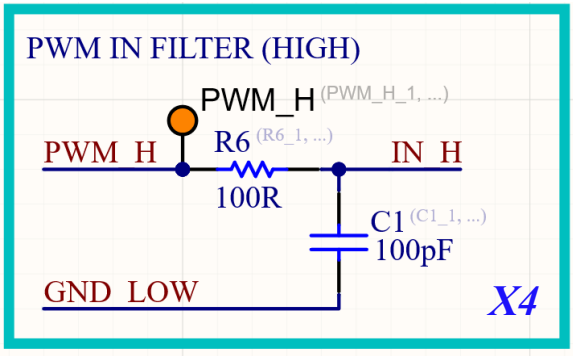
The pins are 5 and 6 correspond to the RDYC and FLT_N signals respectively. This open-drain output requires the use of pull-up resistors in order to use them. These pull-up resistors have been used to form low-pass filters cut-off frequency of 312,07 kHz and to incorporate a LED for visualize the status of both signals, that describe if the driver is working correctly or if there are failures (Figure 80).



$$f_c = \frac{1}{2\pi RC} = 312{,}07\ kHz$$

Figure 80: Schematic of the RDYC_H & FLT_N circuits of the Isolated gate driver 1ED3431MC12MXUMA1

The control signal for the driving of the different MOSFETs arrives at the driver by the IN input. In order to provide a cleaner signal, an RC filter is incorporated, taking into account that the switched signal can have a maximum frequency of up to 100 kHz according to the design requirements. A 100 Ω resistor and a 100 pF capacitor are chosen to provide a cut-off frequency of 15,915 MHz.



$$f_c = \frac{1}{2\pi RC} = 15{,}915\ MHz$$

Figure 81: Schematic of the pin IN circuit of the Isolated gate driver 1ED3431MC12MXUMA1

To explain the schematic of the DESAT pin of the gate driver, first of all it is necessary to understand the different operating zones of the MOSFET. The normal operating range of a SiC MOSFET in the ON-state is in the linear region, but in case of a short circuit the device may enter into the saturation range.

Due to the silicon carbide chemistry, the linear region of SiC MOSFET devices is larger and the transition from the linear region to the saturation region occurs for higher DS voltages (Figure 82). During the transition period the Drain current increases at the same time as VDS increases and the device is destroyed before even reaching the transition point.

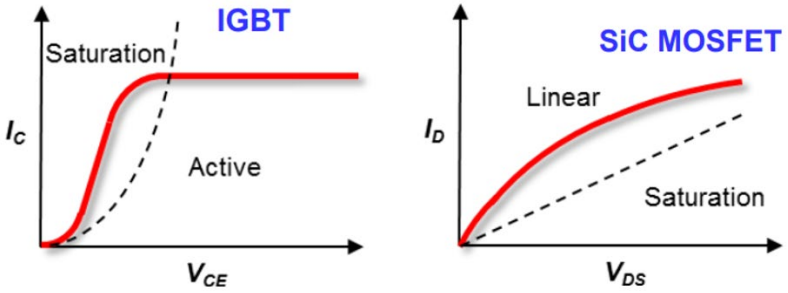


Figure 82: Comparison between the Linear region of an IGBT and a MOSFET

To avoid this behaviour, the 1ED3431MC12MXUMA1 gate driver incorporates the DESAT pin, which acts by turning off the device when it detects that the SiC MOSFET is initiating the transition from the linear zone to the Saturation zone ($V_{DS} > V_{DS\_threshold}$) when the device is driving in HIGH state. The internal desaturation circuit of the driver is shown in Figure 83.

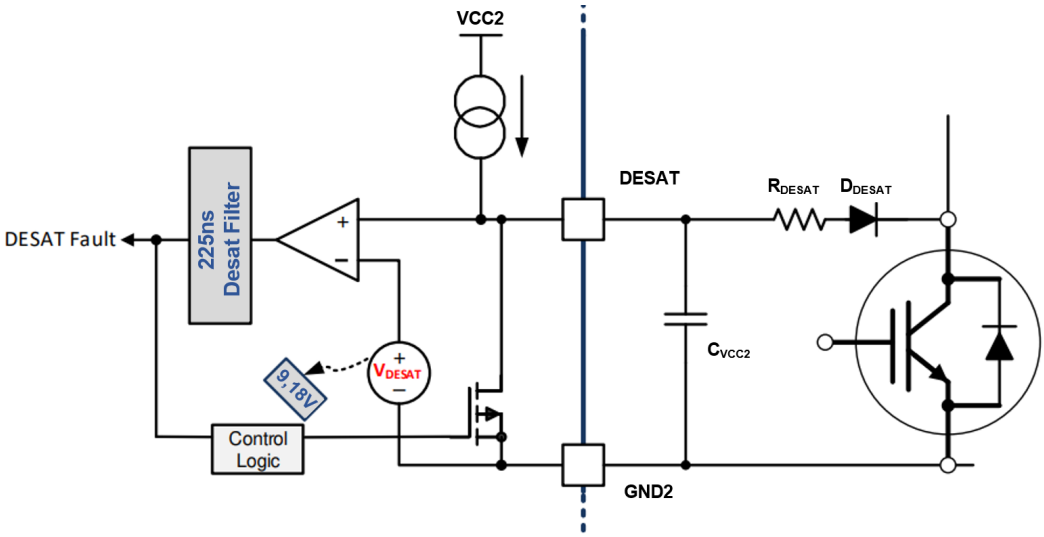


Figure 83: Desaturation protection circuit of the 1ED3431MC12MXUMA1 isolated gate driver

The protection circuit consists of a resistor (R_{DESAT}), a blanking capacitor (C_{VCC2}) and diodes placed in series (D_{DESAT}). In addition, it injects a current of 500 uA into the DS terminals of the MOSFET according to the Infineon driver datasheet.

- Normal operation (ON-State): The capacitor voltage acquires the value determined from the sum of the V_{DS} voltage for a given I_D current with the voltage established by the resistors and diodes. This voltage must be configured to be lower than 9V to prevent the desaturation fault. For the Vincotech module *10-PC124PA040MR-L638F18Y* with $R_{DS}(on) = 60\ m\Omega$ and a maximum current of 32A, a $V_{DS} = 1{,}92V$ is obtained. Furthermore, given that the driver injects a current of 500 uA, the voltage drop for a 1k resistor is 0,5V and the forward voltage of the *STTH112A* diodes from Texas instruments is 1,5V each.

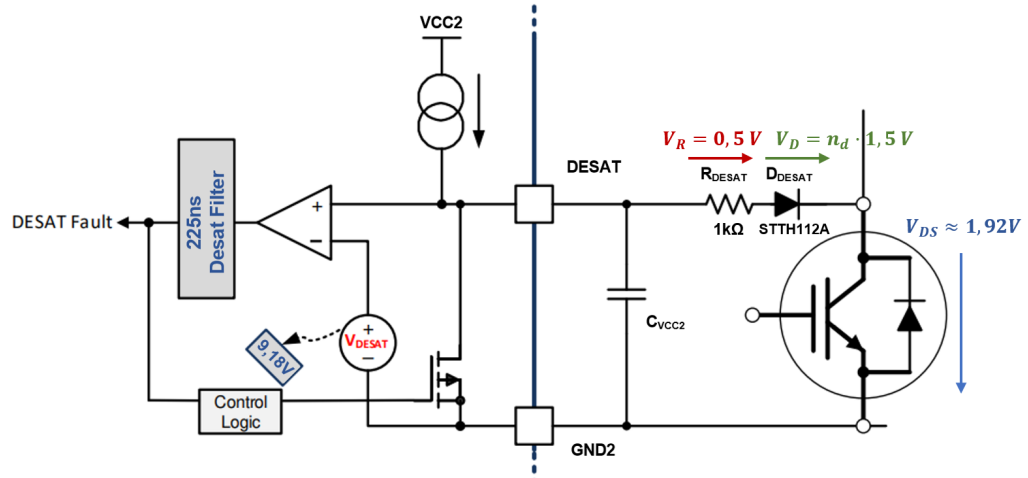


Figure 84: Desaturation protection circuit in Normal Operation

- Saturation operation: When a short circuit occurs the voltage V_{DS} increases rapidly and causes the capacitor to charge exceeding the threshold voltage of 9.18 V set in the internal comparator of the driver. At this point a desaturation failure is detected and controlled shutdown of the MOSFET begins.

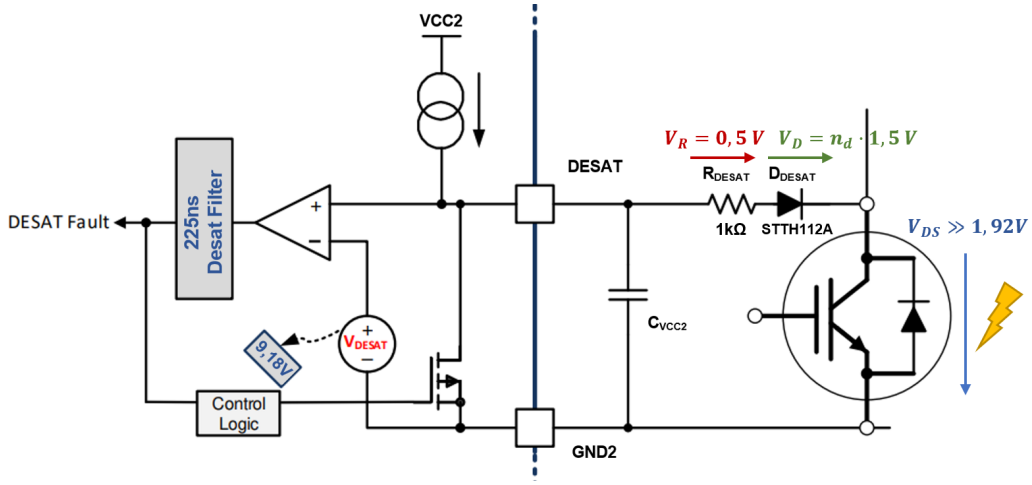


Figure 85: Desaturation protection circuit in Saturation Operation

The blanking capacitance of the desaturation must be dimensioned to be charged fast in order to start the controlled shutdown of the device as soon as possible. This charge has to be slower than the turn-on transient of the SiC MOSFET to avoid false activation of the DESAT pin.

The Infineon driver takes into account this delay by incorporating a typical waiting time of 400 ns ($t_{DESATleb}$) before starting to measure the saturation of the device. The Vincotech SiC MOSFET has a turn-on time much lower than 400 ns, so this delay covers the waiting time needed for not activate the desaturation at turn-on.

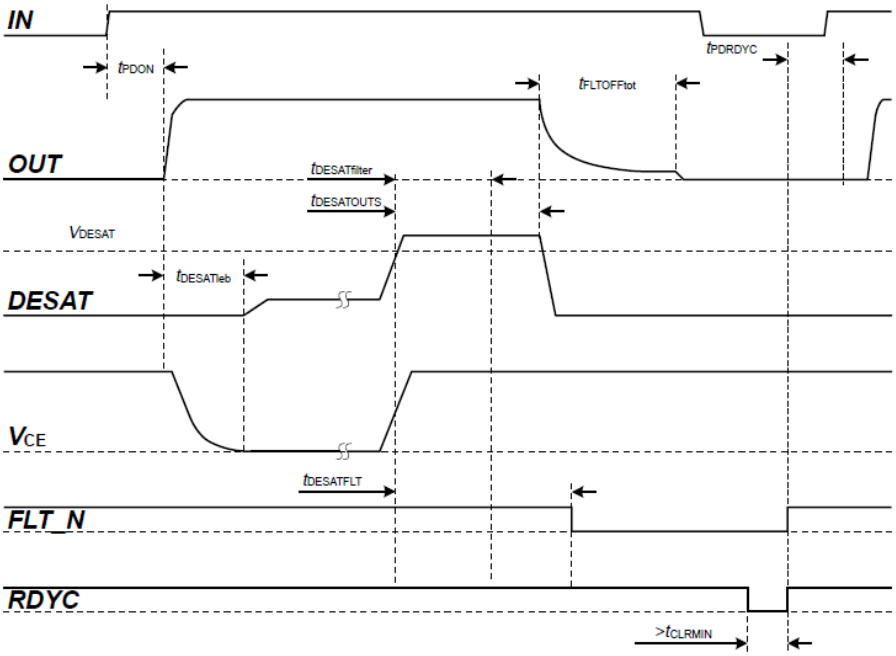


Figure 86: DESAT timing with leading edge blanking, filter, and reaction times

The datasheet of the Infineon driver shows the operation. When the SiC MOSFET starts to conduct after waiting for the delay $t_{DESATleb}$, the C_{VCC2} capacitor starts to charge. In case of short circuit the capacitor voltage exceeds the threshold limit of 9,18 V and after that the fault is detected and the MOSFET turn-off is begins (Soft Turn-Off).

The capacitor charging time is determined by the following formula:

$$t_{BCAP} = \frac{C_{BLK} \times V_{DESAT}}{I_{CHG}}$$

The schematic design of the desaturation circuit is shown in Figure 87. This circuit also incorporates some extra components that give more protection to the driver avoiding high voltages in the system.

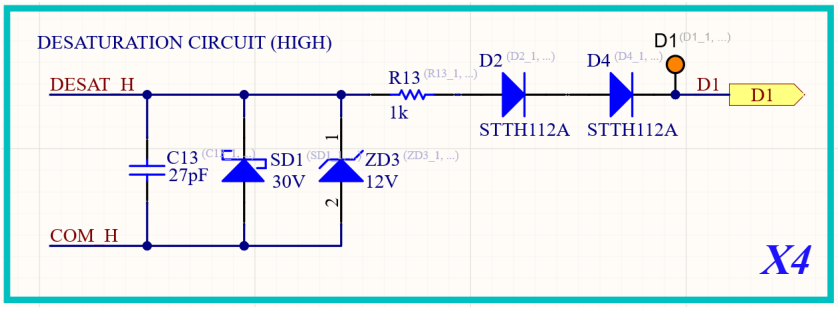


Figure 87: Schematic of the Desaturation circuit of the Isolated gate driver 1ED3431MC12MXUMA1

For the desaturation circuit calculations, the spreadsheet provided by Texas Instruments for their Isolated gate driver with desaturation functionalities (Figure 88) is used. Obtaining a charging time of the blanking capacitor C_{VCC2} of 0,5 us and a threshold at the Drain-Source terminals of the MOSFET of 5,68 V.

User Input			
System Parameters			
RDESAT (Ω)	Vfw (V)	# of diodes	CBLK (nF)
1000	1,5	2	0,027

Fixed Value	
Driver Parameters	
VDESAT (V)	ICHG (µA)
9,18	500

Calculator Output	
VDESAT_Actual (V)	tBLK (µs)
5,68	0,50

Parameter	Definition
VDD-VEE	VDD to VEE voltage (Total drive output voltage)
RDESAT	Resistor in series with HV blocking diode to limit current
Vfw	Forward voltage drop across HV blocking diode
# of diodes	Number of HV blocking diodes in series
CBLK	Blanking capacitor to control DESAT blanking time
VDESAT	Driver IC internal DESAT threshold voltage
ICHG	Driver IC internal DESAT charging current
VDESAT_Actual	Actual DESAT threshold based on external components
tBLK	Blanking time to charge CBLK to DESAT threshold voltage

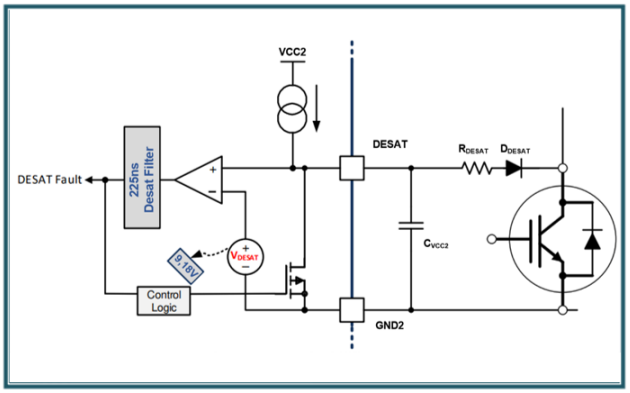


Figure 88: Spreadsheet for desaturation calculations by Texas Instruments

The 1ED34x1Mc12M isolated gate drivers allows the parameters configuration of the Soft-off current and Desaturation functionalities through the ADJA and ADJB pins respectively. For their configuration, it is necessary to connect resistors with values between 1.33 k and 28k with tolerances of 1% and whose opposite end is grounded. The tables for parameter setting according to the values of the resistors connected to the ADJA and ADJB pins of the driver are shown below.

Soft-off adjustment with *ADJA*

Soft-off set up	default	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	stopped
Resistance from *ADJA* to *GND1*	< 1.05 kΩ or tied to *GND1*	1.33 kΩ	1.58 kΩ	1.91 kΩ	2.26 kΩ	2.74 kΩ	3.32 kΩ	4.02 kΩ	4.87 kΩ	5.90 kΩ	7.15 kΩ	8.66 kΩ	10.7 kΩ	13.7 kΩ	17.4 kΩ	23.2 kΩ	28.0 kΩ	>45.3 kΩ or tied to *VCC1*
typ. I_{CSOFF} 1ED3431M	146 mA	15 mA	29 mA	44 mA	58 mA	73 mA	87 mA	102 mA	116 mA	131 mA	146 mA	160 mA	175 mA	189 mA	204 mA	218 mA	233 mA	inhibit gate driver operation
typ. I_{CSOFF} 1ED3461M	291 mA	29 mA	58 mA	87 mA	116 mA	146 mA	175 mA	204 mA	233 mA	262 mA	291 mA	320 mA	349 mA	379 mA	408 mA	437 mA	466 mA	
typ. I_{CSOFF} 1ED3491M	437 mA	44 mA	87 mA	131 mA	175 mA	218 mA	262 mA	306 mA	349 mA	393 mA	437 mA	480 mA	524 mA	568 mA	612 mA	655 mA	699 mA	

Table 11: Soft-off adjustment with ADJA in 1ED34x1Mc12M isolated gate drivers

DESAT filter timing ADJB adjustment

DESAT filter time set up	stopped	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	default
Resistance at *ADJB* to *GND1*	< 1.05 kΩ or tied to *GND1*	1.33 kΩ	1.58 kΩ	1.91 kΩ	2.26 kΩ	2.74 kΩ	3.32 kΩ	4.02 kΩ	4.87 kΩ	5.90 kΩ	7.15 kΩ	8.66 kΩ	10.7 kΩ	13.7 kΩ	17.4 kΩ	23.2 kΩ	28.0 kΩ	>45.3 kΩ or tied to *VCC1*
typ. $t_{DESATleb}$	inhibit gate driver operation	650 ns	650 ns	650 ns	650 ns	650 ns	650 ns	650 ns	650 ns	1150 ns	1150 ns	1150 ns	1150 ns	1150 ns	1150 ns	1150 ns	1150 ns	400 ns
typ. $t_{DESATfilter}$		1575 ns	1775 ns	1975 ns	2375 ns	2775 ns	3175 ns	3575 ns	3975 ns	3975 ns	3575 ns	3175 ns	2775 ns	2375 ns	1975 ns	1775 ns	1575 ns	*225* ns

Table 10: Desat filter time adjustment with ADJB in 1ED34x1Mc12M isolated gate drivers

In the schematic circuit of the pins ADJA and ADJB the adjustment of resistors is performed to set the parameters as follows (Figure 89):

***ADJA → GND**, default parameters*

***ADJB → 100 kΩ**, parameters at minimum values.*

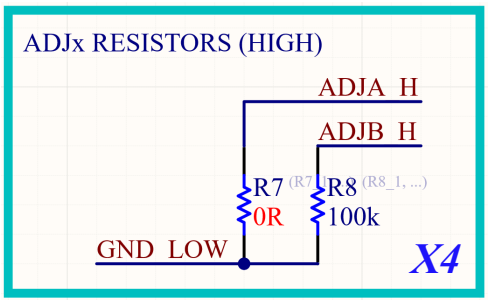


Figure 89: Schematic of the pin ADJA & ADJB circuit of the Isolated gate driver 1ED3431MC12MXUMA1

The MOSFET gate driver circuit (Figure 90) is composed of gate resistors to control the current injected into the gate and some protection systems such as a transient-voltage-suppression (TVS) diode to avoid overvoltages, an external capacitor between the Gate-Source to lower the impedance for suppressing rises in the gate potential and a pull-down resistor to avoid floating pins of the driver, this resistor has to be much bigger than the gate resistor for not affecting the gate voltage of the MOSFET.

This circuit also implements the CLAMP pin connected directly to the gate of the MOSFET with a 0 Ω resistor. This pin prevents false turn-on of the MOSFETs due to Miller currents.

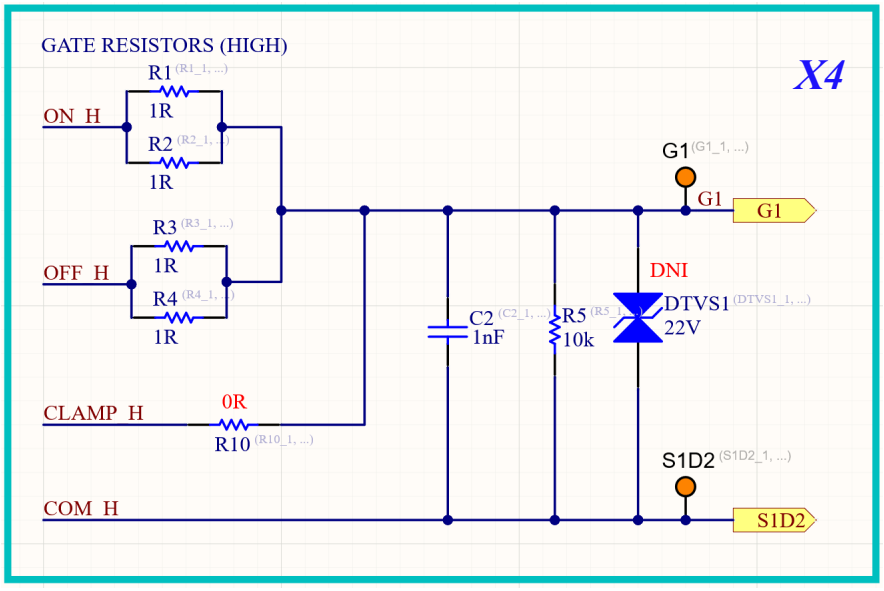


Figure 90: Schematic of the MOSFET gate driver circuit of the Isolated gate driver 1ED3431MC12MXUMA1

It is important to know which gate resistors are appropriate for the gate activation circuit. These resistors are responsible for limiting the current peaks supplied by the driver for switching the MOSFETs by charging and discharging the parasitic capacitance between its Gate-Source terminals and therefore have a significant influence on the turn-on and turn-off transient times.

The internal gate activation circuit of the driver 1ED3431MC12MXUMA1 is shown in the Figure 91. This circuit incorporates two internal resistors $R_{DS,source}$ and $R_{DS,sink}$ whose values can be found in the driver datasheet (Table 12) and the parasitic resistance R_{G_INT} of Vincotech SiC MOSFET module which has a value of 7 Ω.

Driver type	$R_{DS,source}$ output resistance		$R_{DS,sink}$ output resistance	
	typ [Ω]	max [Ω]	typ [Ω]	max [Ω]
1ED3431Mc12M, 1ED3830Mc12M	1.12	4.0	0.82	6.0

Table 12: Internal Gate Driver resistor driver 1ED3431MC12MXUMA1

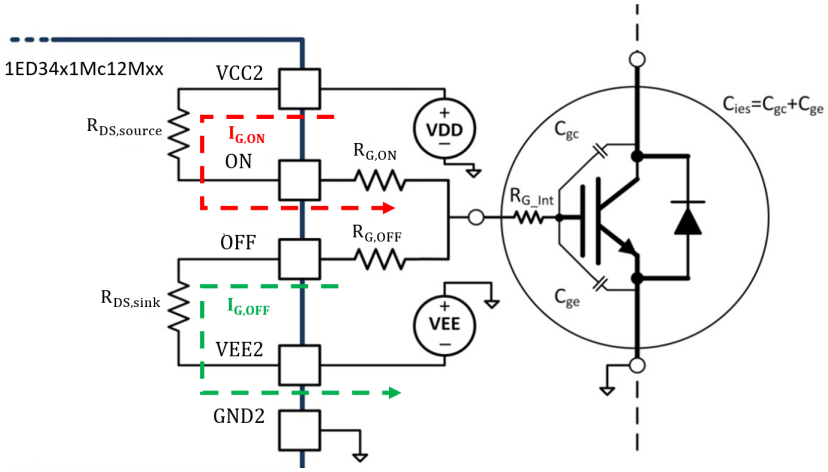


Figure 91: Gate Driver Circuit of the driver 1ED3431MC12MXUMA1

The minimum gate resistance is obtained from the maximum current that the driver "1ED3431MC12MXUMA1" is capable of supplying, which is 3A.

$$I_{G,ON} = \frac{V_{DD} - V_{EE}}{R_{DS,source} + R_{G,ON} + R_{G,int}} = \frac{20{,}5\ V}{1{,}12 + R_{G,ON} + 7} = 3\ A\ (Driver) \rightarrow \boldsymbol{R_{G,ON} > 0\ \Omega}$$

$$I_{G,OFF} = \frac{V_{DD} - V_{EE}}{R_{DS,sink} + R_{G,OFF} + R_{G,int}} = \frac{20{,}5\ V}{0{,}82 + R_{G,OFF} + 7} = 3\ A\ (Driver) \rightarrow \boldsymbol{R_{G,OFF} > 0\ \Omega}$$

$$\boldsymbol{I_{G,ON\_máx} = \frac{20,5}{1,12\ \Omega + 0 + 7\ \Omega} = 2,525\ A}$$

$$\boldsymbol{I_{G,OFF\_máx} = \frac{20,5}{0,82\ \Omega + 0\ \Omega + 7\ \Omega} = 2,621\ A}$$

Since the internal resistance of the Vincotech module is very big, the maximum ON and OFF current would not exceed the maximum current of the driver even if no fate resistor is implemented.

The maximum Gate resistance is calculated from the charging and discharging time of the parasitic capacitance of the CGS module during turn-on and turn-off. This charge and discharge time has to be much shorter than the switching period of the module (20 times shorter).

$$C_{GS} = C_{iss} - C_{rss} = 1337pF - 27pF = 1310\,pF$$

$$t_r = 5 \cdot R_G \cdot C_{GS} << T_s = \frac{1}{100\,kHz} = 10\,us$$

$$R_G = R_{DS,source} + R_{G,ON} + R_{G_{int}}$$

$$R_G = R_{DS,sink} + R_{G,OFF} + R_{G_{int}}$$

$$R_G < \frac{T_s}{20} \cdot \frac{1}{5 \cdot C_{GS}} = \frac{10\,us}{20} \cdot \frac{1}{5 \cdot 1310\,pF} = 76{,}336\,\Omega$$

$$R_{G,ON} < R_G - R_{DS,source} - R_{G_{int}} = 76{,}336\,\Omega - 4\,\Omega - 7\Omega \rightarrow \boldsymbol{R_{G,ON} < 65{,}34\,\Omega}$$

$$R_{G,OFF} < R_G - R_{DS,sink} - R_{G_{int}} = 76{,}336\,\Omega - 6\,\Omega - 7\Omega \rightarrow \boldsymbol{R_{G,OFF} < 63{,}34\,\Omega}$$

$$\boldsymbol{I_{G,ON\_máx} = \frac{20{,}5\,V}{1{,}12\,\Omega + 65{,}34\,\Omega + 7\,\Omega} = 0{,}279\,A}$$

$$\boldsymbol{I_{G,OFF\_máx} = \frac{20{,}5\,V}{0{,}82\,\Omega + 63{,}34\,\Omega + 7\,\Omega} = 0{,}288\,A}$$

Taking into account the calculated maximum and minimum ON and OFF gate resistances, the following ranges are obtained:

$$\boldsymbol{0\,\Omega < R_{G,ON} < 65{,}34\,\Omega}$$

$$\boldsymbol{0\,\Omega < R_{G,OFF} < 63{,}34\,\Omega}$$

In order to limit the gate current and ensure fast switching of the MOSFETs, a gate resistance of $R_{G,ON} = R_{G,OFF} = 1\,\Omega$ is chosen.

Temperature measurement circuit (LTC6992CS6-1, LM4040B50FTA, ACPL-W61L-000E)

These types of power converters suffer from warm up due to the high currents and power that they drive. In order to avoid overheating that can affect the lifetime of the converter, Vincotech modules implement an NTC thermistor (Figure 92) to monitor the temperature and take appropriate actions to ensure the correct operation of the converter.

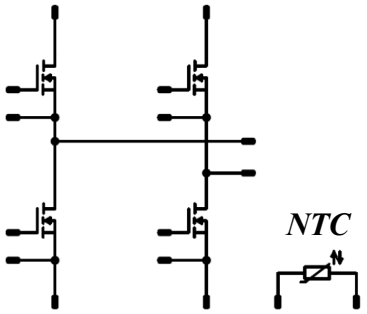


Figure 92: Schematic of 10-PC124PA040MR-L638F18Y , Vincotech module

This temperature sensor is a resistor whose resistance has relevant variations when the temperature changes; the relation describing its first order behaviour is:

$$\Delta R = k\Delta T$$

with k = -273,5 Ω/K and the resistance at 25 ºC is R_{25} = 22 kΩ as can be found in the power module datasheet. In order to take advantage of this temperature sensor, a measurement circuit is designed on the gate drive board; the schematic of this circuit is displayed in Figure 93. The circuit is placed on the gate drive board and is connected to the thermistor pins of the power module through a board to board connector P5.

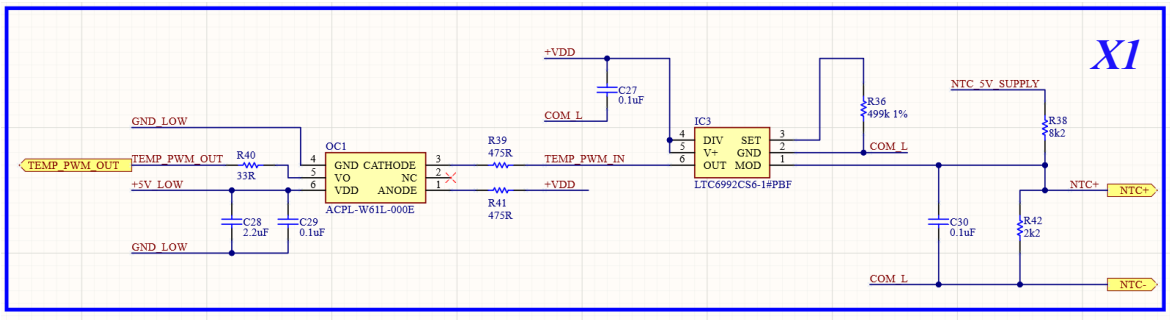


Figure 93: Schematic of the Temperature measurement circuit

This circuit of the consists of a voltage controlled PWM (*LTC6992CS6-1*) and a digital optocoupler (*ACPL-W61L-000E*) which provides isolation to the circuit.

The temperature measurement circuit is based on the generation of a PWM signal which represents the junction temperature of the SiC power module by its duty cycle. To do this, the PWM voltage controlled integrated circuit *LTC6992CS6-1* has to be configured correctly.

There are many ways to configure the PWM voltage controller, for this application its parameters are set to obtain a PWM signal with a frequency of 100 kHz and whose duty cycle decreases if the voltage at its Vmod terminal increases.

This configuration implies that its polarity flag (POL) has to be "1", and its divider (N_{DIV}), which has a range of [1, 16384], is set to the minimum value which is "1". For this purpose, the resistors R1 and R2 shown in Figure 94 are used, where in this case according to Table 13, R1 is short-circuited and R2 is open.

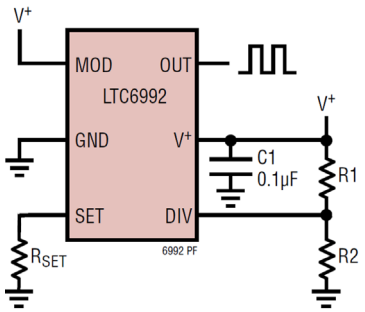


Figure 94: Typical application of the LTC6992CS6-1

DIVCODE	POL	N_{DIV}	RECOMMENDED f_{OUT}	R1 (kΩ)	R2 (kΩ)	V_{DIV}/V^+
15	1	1	62.5kHz to 1MHz	Short	Open	≥0.96875 ±0.015

Table 13: DIVCODE Programming of the LTC6992CS6-1

Una vez ajustados los parámetros del DIVCODE, se calcula la resistencia RSET para ajustar la frecuencia de la PWM de voltaje a partir de la siguiente ecuación.

$$R_{SET} = \frac{1\,MHz \cdot 50k}{N_{DIV} \cdot f_{OUT}} = \frac{1\,MHz \cdot 50k\Omega}{1 \cdot 100kHz} = \mathbf{500\ k\Omega}$$

The modulator signal Vmod instead, that sets the duty cycle of the PWM signal, is generated through the voltage divider circuit in Figure 95. In this circuit the modulator voltage is the voltage applied over the parallel connection between the NTC thermistor and the 2.2 k resistor.

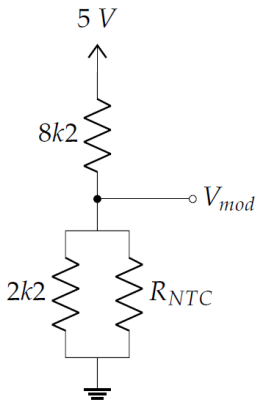


Figure 95: Voltage divider circuit for the generation of the modular signal

Where the modulator voltage Vmod is given by the following equation of the voltage divider circuit.

$$V_{mod} = 5\ V \cdot \frac{R_{NTC}//2.2\ k\Omega}{R_{NTC}//2.2\ k\Omega + 8.2\ k\Omega}$$

and

$$R_{NTC} = R_{25} + k \cdot (T - 25)$$

where T [ºC] is the junction temperature.

According to the equations, a voltage of 1V at the modulator , resulting in a 100% duty cycle, corresponds to the lowest measurable temperature of −4,5 ºC, while the upper temperature limit is 105 ºC, corresponding to a 0 V modulator and a 0% duty cycle. The sensitivity of the modulator voltage with respect to temperature variations increases with temperature, and it is the highest for temperature closer to the upper bound.

To route the PWM voltage signal to the low voltage side, the *ACPL-W61L-000E* integrated is used, which is a digital optocoupler that provides voltage isolation to the circuit (Figure 96). The manufacturer also recommends the use of bypass capacitors between the VDD and GND pins.

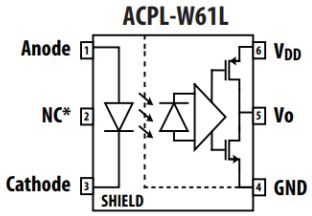


Figure 96: Functional diagram of the ACPL-W61L-000E

Finally, a shunt reference *LM4040B50FTA* voltage is used for the 5V supply to the temperature measurement circuit (Figure 97). This circuit works as a Zener voltage whose value is set via the resistor RS and allows a wide range of input voltages.

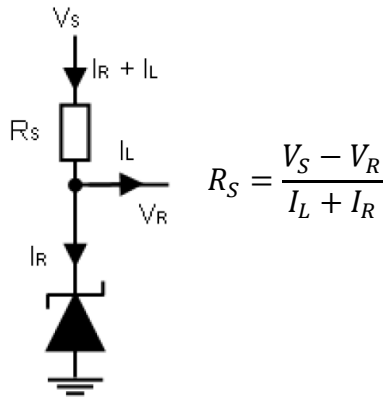


Figure 97: Operation of the shunt reference voltage

For the dimensioning of the Rs resistor, the manufacturer recommends the analysis of two situations. The first is when the Vs voltage is at its minimum and the load current is at its maximum, this circuit should be able to supply at least the minimum IR current (87 mA according to datasheet). The minimum voltage of the isolated DCDC converter *MGJ2D241802SC* is 3% less than its normal output voltage (18V·97% = 17,46 V).

$$R_{S,max} = \frac{V_{S,min} - V_R}{I_{L,max} + I_{R,min}} = \frac{17{,}46\ V - 5V}{609{,}75\ uA + 83\ uA} = 17986\ \Omega$$

where

$$I_{L,max} = \frac{5}{8k2 + (2k2 // R_{NTC,max})} = \frac{5}{8k2 + 0} = 609{,}75\ uA$$

The second situation is that when the voltage Vs is at its maximum and the load current is at its minimum, the chosen resistor RS limits the maximum current IR to a value less than 15 mA. The minimum voltage of the isolated DCDC converter *MGJ2D241802SC* is 10% more than its normal output voltage (18V ·110% = 19,8 V).

$$R_{S,min} = \frac{V_{S,max} - V_R}{I_{L,min} + I_{R,max}} = \frac{19{,}8\ V - 5V}{490{,}20\ uA + 15\ mA} = 955\ \Omega$$

where

$$I_{L,min} = \frac{5}{8k2 + (2k2 // R_{NTC,min})} = \frac{5}{8k2 + (2k2 // 22k)} = 490{,}20\ uA$$

$$955\ \Omega < R_S < 17986\ \Omega$$

Finally, a normalised value of Rs = 10 kΩ is chosen. This value is within the calculated resistance range and meets the requirements of the circuit. The schematic of the shunt reference voltage circuit is shown in Figure 98.

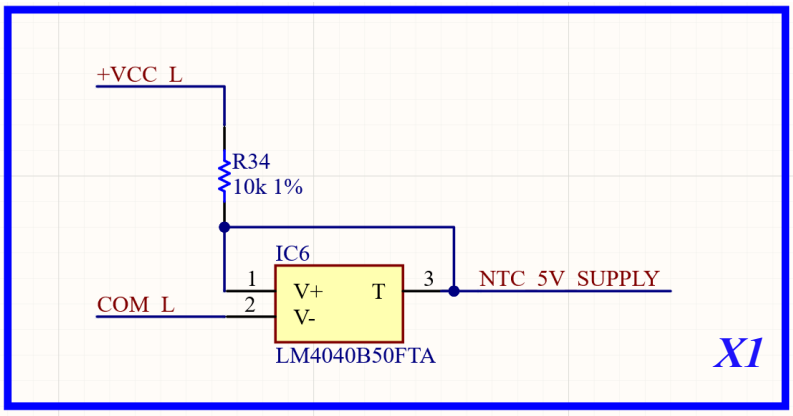


Figure 98: Schematic of the 5V shunt reference voltage circuit for supply

Since most of the circuits on the gate driver board are replicated for each of the Vincotech modules, Altium Designer "Sheet Symbols" are used. The Sheet Symbols contain the schematics of the circuits to be replicated and give access to the inputs/outputs of the circuit. In this way, the design is simpler, and the input and output connections of the gate driver board, explained at the beginning of this section ,can be seen more clearly. Figure 99 shows all gate driver connections including the Sheet Symbols required for the design.

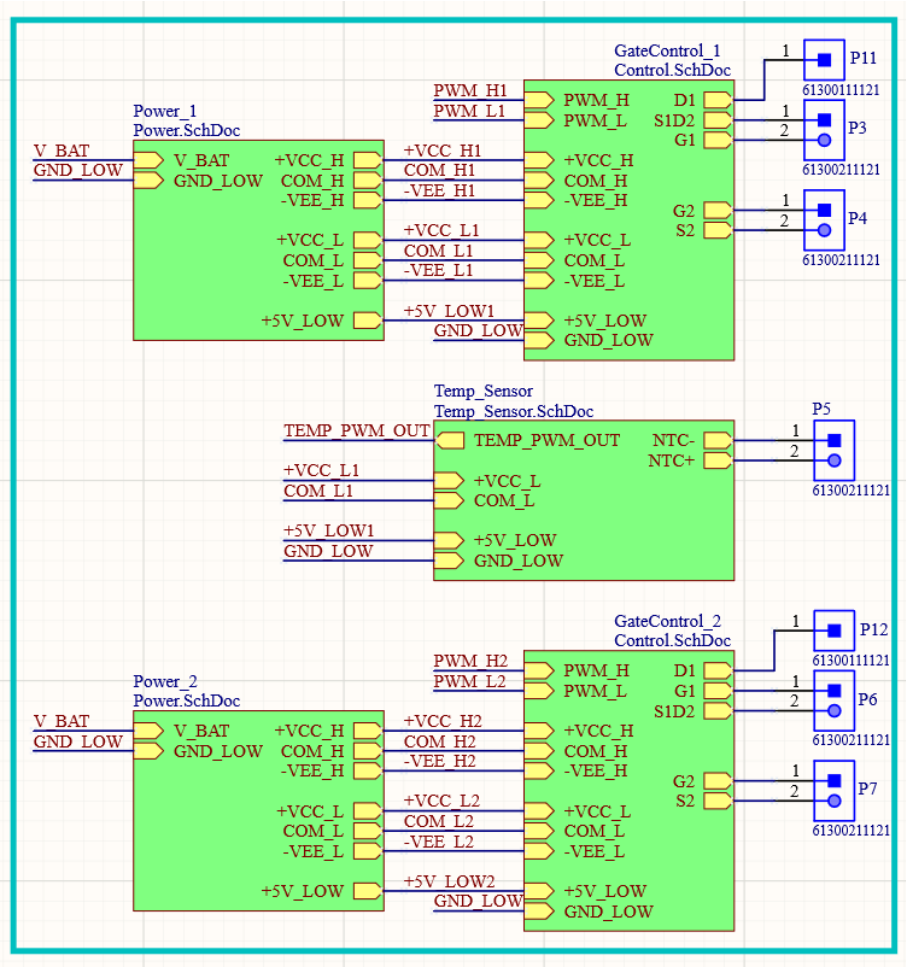


Figure 99: Sheet symbols connections of the new gate driver board design

4.2. Power calculations

To verify that the power supplies of the different systems are correctly dimensioned, the power calculations of the most important integrated components of the gate driver board are made.

In order to schematise the power calculation process, a block diagram with the power consumption and the connections of the different components was created for a single module.

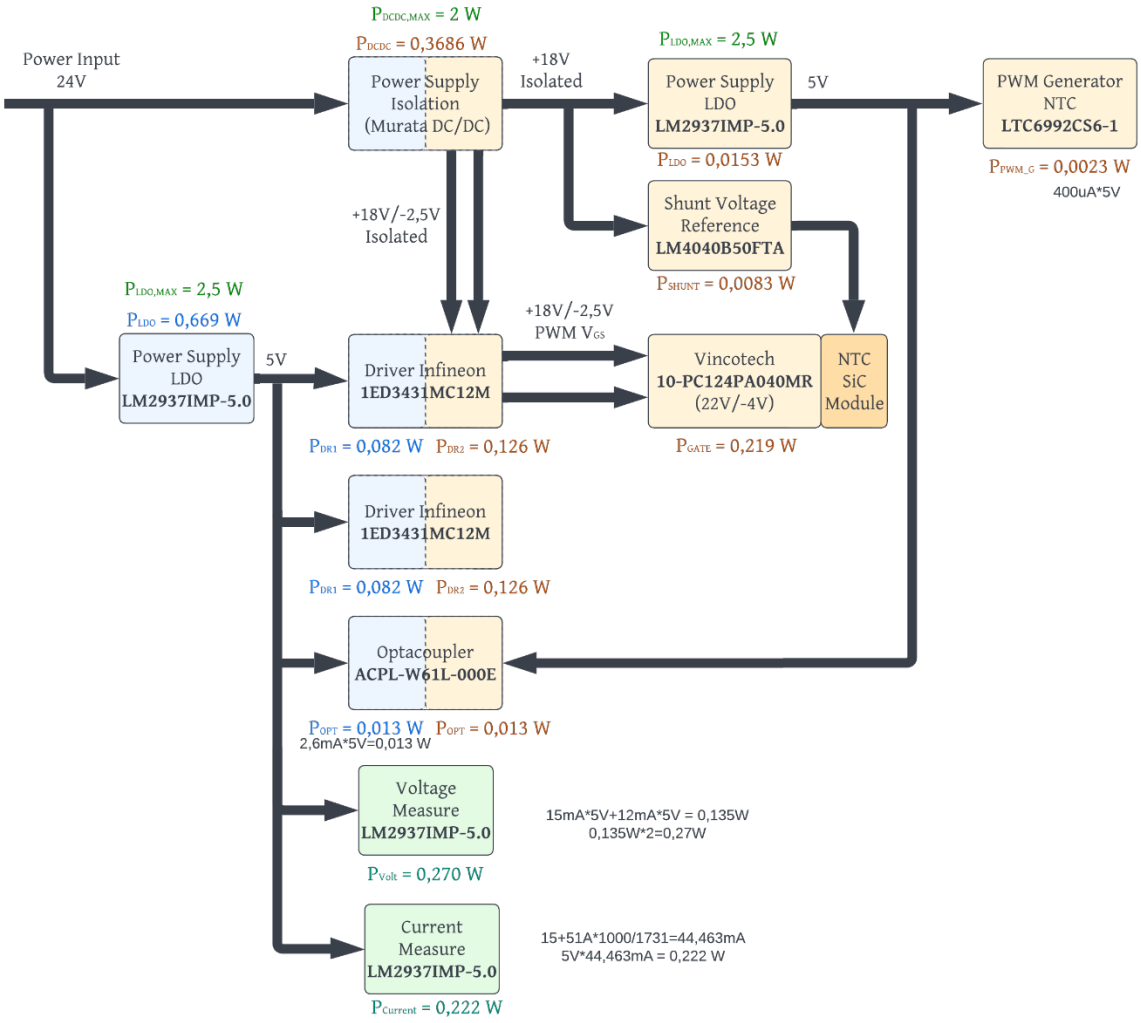


Figure 100: Block Diagram of the power consumptions in the new gate driver board

Looking at Figure 100, it is shown how the power that can be supplied by the different components is within the limits. The simpler calculations are shown directly in the block diagram while the more complex calculations are explained in more depth throughout this section.

Power calculation of the gate of the Vincotech 10-PC124PA040MR-L638F18Y

The power lost during the gate charging can be calculated from the following equation, taking into account that the Vincotech module has a Q_G = 107 nC.

$$P_{GATE} = (V_{DD} - V_{EE}) \cdot f_{SW} \cdot Q_G = 20{,}5\ V \cdot 100\ kHz \cdot 107\ nC = \mathbf{0{,}219\ W}$$

Where the product $f_{SW} \cdot Q_G$ gives the average bias current required to drive the gate. In addition, the selected gate resistors must be able to dissipate this calculated power.

Power calculation of the driver 1ED3431MC12MXUMA1

The power dissipated in the driver must be considered in order to keep it below its thermal limit. These gate driver losses include quiescent loss and switching loss.

$$\boldsymbol{P_{DR} = P_Q + P_{SW}}$$

The quiescent loss power of the driver can be calculated from the quiescent currents in the driver datasheet, in this case we only focus on the power part I_{Q2} supplied by the DCDC.

$$P_{Q2} = I_{Q2} \cdot (V_{DD} - V_{EE}) = 5\ mA \cdot 20.5\ V = \mathbf{0{,}1025\ W}$$

VCC2 quiescent current	I_{Q2}	–	3.9	5	mA	V_{VCC2} = 15 V, V_{VEE2} = -8 V, *OUT* = High, *DESAT* = Low
VCC2 operating current	I_{Q2}	–	3.9	5	mA	V_{VCC2} = 15 V, V_{VEE2} = -8 V, *OUT* = 16 kHz, 50%, *DESAT* = Low, C_{LOAD} = 100 pF

Figure 101: Quiescent and operating currents for the 1ED3431MC12MXUMA1 driver

The series resistors of the gate drive path are used to calculate the losses during switching. In each switching operation, the load required for the gate passes through the output resistor of the driver, the gate resistor (R_G = 1 Ω) and the internal gate resistor of the MOSFET.

$$P_{SW} = \frac{1}{2} \cdot \left(\frac{R_{DS,source}}{R_{DS,source} + R_{G,ON} + R_{G_{int}}} + \frac{R_{DS,sink}}{R_{DS,sink} + R_{G,OFF} + R_{G_{int}}} \right) \cdot (V_{DD} - V_{EE}) \cdot f_{SW} \cdot Q_G$$

$$P_{SW} = \frac{1}{2} \cdot \left(\frac{1{,}12}{1{,}12 + 1 + 7} + \frac{0{,}82}{0{,}82 + 1 + 7} \right) \cdot 20{,}5\ V \cdot 100\ kHz \cdot 107\ nC = \mathbf{23{,}665\ mW}$$

Finally, the power dissipated by the gate driver is obtained.

$$P_{DR} = 0{,}1025\ W + 23{,}665\ mW = \mathbf{0{,}126\ W}$$

Assuming a board temperature of 125 ºC (T_B) and a thermal resistance of $R_{thJB} = 66\ K/W$, the junction temperature of the component is calculated.

$$T_J = T_B + R_{thJB} \cdot P_{DR} = 133{,}33\ ºC < 150\ ºC$$

It is observed that the junction temperature on the board does not exceed the maximum temperature specified in the driver datasheet, which means it is working correctly.

Power calculation of the 5V shunt reference voltage LM4040B50FTA

Based on the maximum current and resistor Rs calculated previously, the power of the 5V shunt reference voltage is obtained.

$$P_{SHUNT} = \left(I_{L,max} + I_R\right) \cdot V_R + \left(I_{L,max} + I_R\right)^2 \cdot R_S$$

$$P_{SHUNT} = (609{,}75\ uA + 83\ \text{uA}) \cdot 5\ \text{V} + (609{,}75\ uA + 83\ \text{uA})^2 \cdot 10\ \text{k}\Omega = 0{,}0083\ \text{W}$$

Power calculation of the Isolated DCDC Converter MGJ2D241802SC

The power to be supplied by the Isolated DCDC Converter is equal to the sum of the powers from the driver, the gate, the shunt reference voltage and the 5V voltage regulator on the isolated part of the circuit.

$$P_{DCDC} = P_{DR} + P_{GATE} + P_{SHUNT} + P_{LDO}$$

$$P_{DCDC} = 0{,}126\ W + 0{,}219\ W + 0{,}0083\ W + 0{,}0153\ W = 0{,}3686\ W$$

4.3. PCB Layout Design

The good design of the PCB layout of the gate driver unit will define the proper functioning of the board. This design is complicated, especially in high-power and high-frequency applications such as SiC chemistries. For this reason, a number of guidelines have to be followed which define how this design is going to be done.

- Redesign of the printed circuit board of the gate driver unit from 2 layers to 4 layers maintaining the size of the previous design.
- Use of measurement points to facilitate signal monitoring in the converter laboratory tests.
- Redesign of the Drain-Gate-Source tracks of the SiC MOSFETs by integrating them in different layers to reduce the effect of EMI and trying to keep them as short as possible. These tracks have to follow the same routing by using the intermediate layers in order to reduce the area susceptible to electromagnetic couplings from the power tracks.
- Use of polygons in the design of the gate driver board tracks to optimise heat dissipation and minimise parasitic inductances. It is important to round the edges to avoid sharp points that create an antenna effect.
- Provide an adequate isolation distance between the low voltage side and the high voltage side. Applying different cut-offs on critical parts of the board.
- Check of the gate driver board using Eurocircuits "PCB Visualizer" software for reducing the technology needed to manufacture the PCB and reducing its cost.

4 layer design

For the design of this printed circuit board, a 4-layer layout has been chosen. This type of configuration allows the use of the top and bottom layers for the routing of the signal traces, and the middle layers are used for the power supply signals.

In a 4-layer design, there are different possibilities in the order chosen. In high power designs where it is important to have good immunity to electromagnetic interference (EMI), the positive power +VDC layer is usually placed in a higher position than the ground GND layer. The full layer configuration of the PCB is shown in Figure 102.

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.01016mm	3.5	
1	Top Layer		Signal	1oz	0.03556mm		
	Dielectric 2	FR-4	Core		0.254mm	4.2	0.02
2	VCC/GATE		Signal	1oz	0.035mm		
	Dielectric 1		Prepreg		0.127mm	4.2	
3	GND/GATE		Signal	1oz	0.035mm		
	Dielectric 3	FR-4	Core		0.254mm	4.2	0.02
4	Bottom Layer		Signal	1oz	0.03556mm		
	Bottom Solder	Solder Resist	Solder Mask		0.01016mm	3.5	
	Bottom Overlay		Overlay				

Figure 102: Layer Stack Manager of the gate driver PCB

Furthermore, after routing the signal tracks of the PCB, the top and bottom layers of the PCB must be grounded by using copper ground planes. This also applies to the insulated parts of the PCB with their respective grounds.

In order to achieve a good connection between the different ground layers, the use of vias is essential. as many vias as necessary have to be placed to keep all areas connected.

Figure 103: Placement of vias in the gate driver PCB layers

Measurement Points

In order to verify the correct operation of the new gate driver board during laboratory tests, it is necessary to use measurement points. These points allow easy coupling of the oscilloscope instruments, giving access to signals that are difficult to measure without an external connection and avoiding measurements directly on the board, which can cause undesired short-circuits.

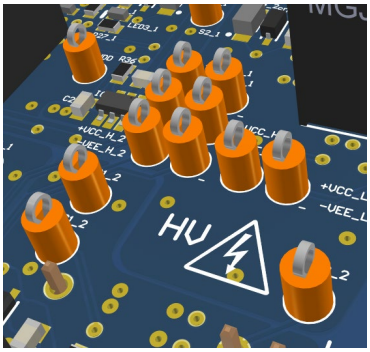


Figure 104: Measurement Point of the gate driver PCB

Another way to realise measurement points in a more economical way and to avoid drilling holes in the board, is by using traces which connect the signals to be measured with vias located at the edges of the board (Figure 105). However, given the limited space of the design, it was decided to use measurement points with holes to save space and avoid long traces .

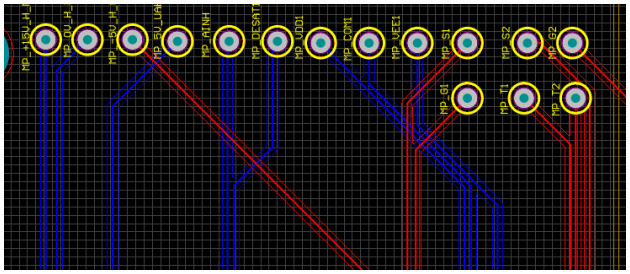


Figure 105: Measurement Points by using traces and vias in other PCB design

Drain-Gate-Source tracks

The magnetic fields generated in the power lines of the Power Unit can generate interferences in the signal lines of the gate driver board. These types of interferences are critical in the case of the drain, gate, and source signals of the circuit because they can cause spurious turn-on of the MOSFETs or false activation of the driver desaturation which can result in system failures.

To avoid these effects, the board must be designed to reduce the area where magnetic field signals can interfere. To do this, the routing of the Gate-Source and Drain-Source tracks should be as close together as possible. When using a 4-layer design, it is most useful to route these tracks through the different layers one above the other as follows.

Top Layer (1) → High speed signals, Positive Supply Signals

+VCC Layer (2) → Gate Signals, Positive Supply Signals

GND Layer (3) → Source Signals, Negative Supply Signals, GND

Bottom Layer (4) → Drain Signals, Noncritical Signals

Figure 106 shows a part of the layout design where it can be seen how the gate and source signals have the same routing in different layers.

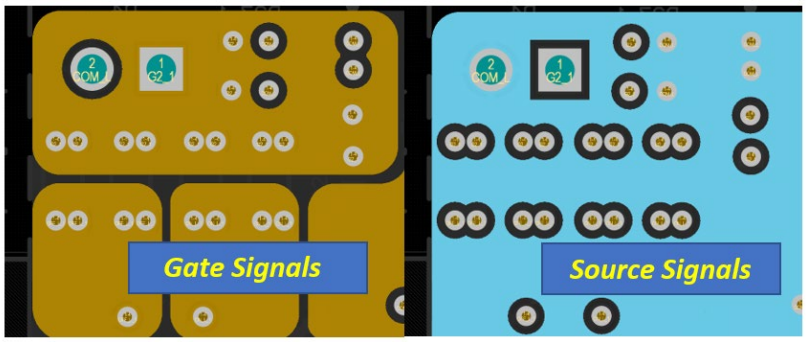


Figure 106: Routing of the Gate and Source signals in the gate driver PCB

Another example is the routing of drain and source traces in different layers shown in .

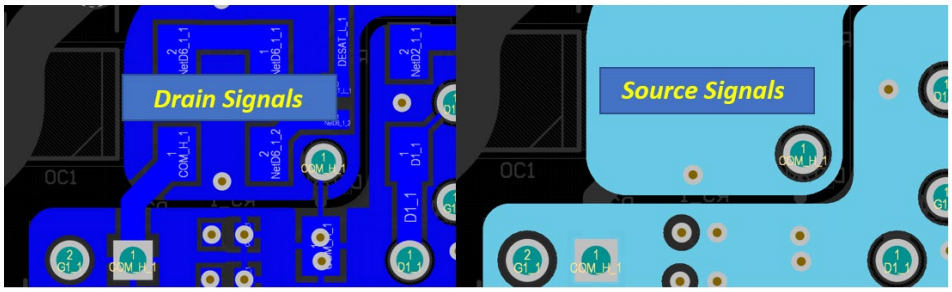


Figure 107: Routing of the Drain and Source signals in the gate driver PCB

Polygon Pour Design

One of the important changes from the previous design is the use of polygons for the layout of the power tracks. This technique is useful to reduce the heating of the plate by increasing the heat dissipation area and to reduce the parasitic inductances by increasing the track width.

On the other hand, it is essential to avoid sharp edges on the polygons, because they act as antennas and can affect to the performance of the board by generating more interference. For this reason, the edges should be rounded as much as possible. The design technique with polygons can be seen in the.

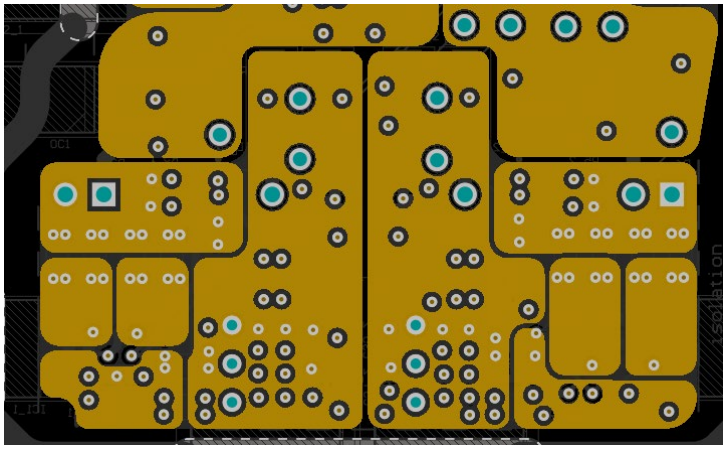


Figure 108: Polygon Pour Design of the VCC layer from the Gate Driver PCB

Isolation

The board design is divided into two sides, the low voltage side (LV), and the high voltage side (HV). This division is intended to ensure good isolation between the two parts in order to reduce possible coupling and interference generated by the power tracks in the low part where the control signals are located.

As can be seen in Figure 109, in order to guarantee the insulation distance, a copper-free area must be left. This insulation distance is in many cases is determined by the manufacturers of the different components, and it is very important to respect it in order to ensure that the insulation characteristics given in the datasheet are not affected.

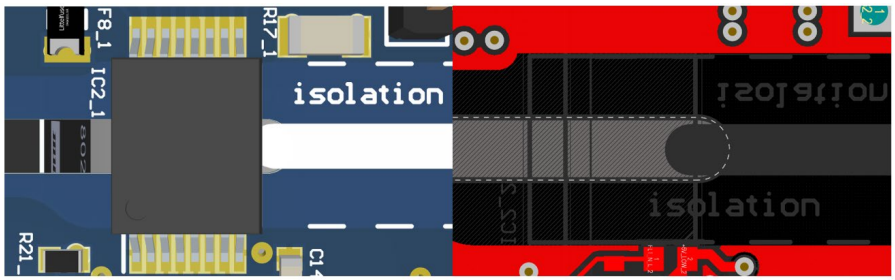


Figure 109: Isolation Barrier of the Gate Driver PCB

In addition, due to the superior isolation characteristics of the air, it is recommended to make cut-outs in the critical points of the board, for example, under the devices to be isolated. It should be noted that these cut-outs are usually free of any cost in the PCB manufacturing process.

PCB Visualizer by Eurocircuits

Eurocircuits is a leading manufacturer of printed circuit boards (PCB) which has a very high quality of the PCBs that they make. Moreover, Eurocircuits also incorporates a board checking system called "PCB Visualizer" which runs directly from their website and has the main function of verifying the correct layout of the PCB designed and providing information about the type of technology and price needed to manufacture it. This tool is shown in Figure 110.

In order to verify the board using the PCB Visualizer tool, it is necessary to generate its Gerber Files and NC Drill Files. Once the PCB is loaded, the tool automatically detects all the characteristics of the board and allows you to configure the different manufacturing parameters.

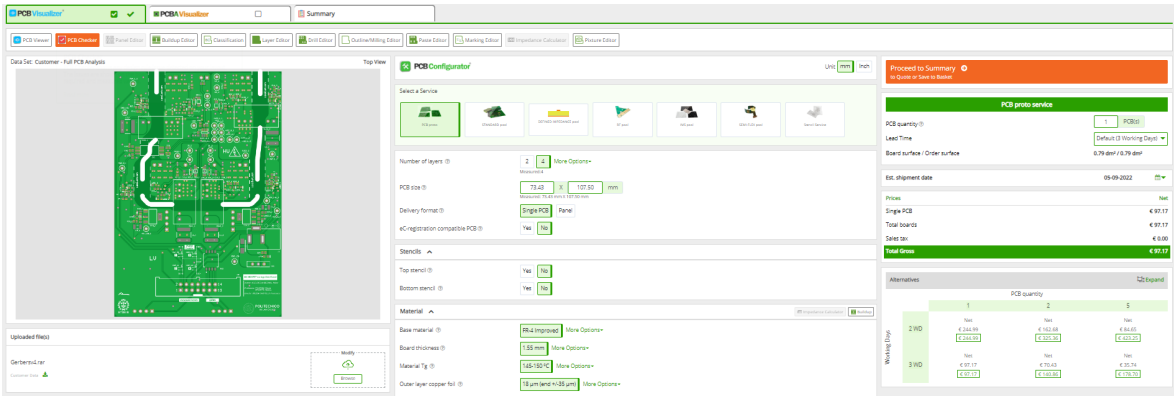


Figure 110: PCB Visualizer Tool of Eurocircuits for the Gate Driver PCB

After setting the parameters, you can visualise any errors in the layout design using the "*PCB Checker*" (Figure 111). This tool provides a view of the different layers indicating any design mistakes that cannot be done with the selected manufacturing technology and have to be fixed.

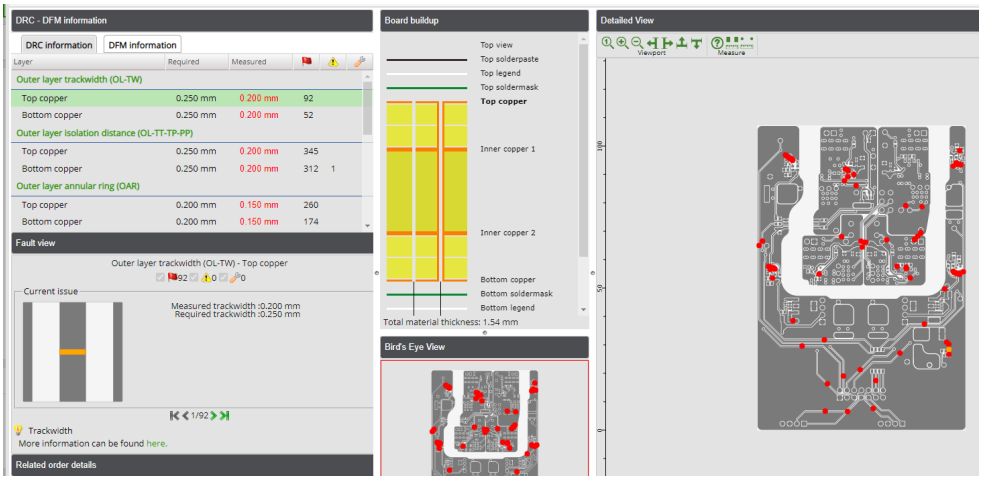


Figure 111: PCB Checker Tool of Eurocircuits for the Gate Driver PCB

The different pattern classes and drill class that define the manufacturing technology depend on the required board accuracies in terms of board widths, annular rings, drill sizes and isolation distances. All the classes are listed in Figure 112.

Pattern class

	Design values	Pattern class 3	4	5	6	7	8	9
Outer layer trackwidth (OL-TW)	0.2	≥ 0.250 mm	≥ 0.200 mm	≥ 0.175 mm	≥ 0.150 mm	≥ 0.125 mm	≥ 0.100 mm	≥ 0.090 mm
Outer layer isolation distance (OL-TT-TP-PP)	0.2	≥ 0.250 mm	≥ 0.200 mm	≥ 0.175 mm	≥ 0.150 mm	≥ 0.125 mm	≥ 0.100 mm	⚠ ≥ 0.100 mm
Outer layer annular ring (OAR)	0.15	≥ 0.200 mm	≥ 0.150 mm	≥ 0.150 mm	≥ 0.125 mm	≥ 0.125 mm	≥ 0.100 mm	≥ 0.100 mm
Inner layer trackwidth (IL-TW)	0.200	≥ 0.250 mm	≥ 0.200 mm	≥ 0.175 mm	≥ 0.150 mm	≥ 0.125 mm	⚠ ≥ 0.125 mm	⚠ ≥ 0.125 mm
Inner layer isolation distance (IL-TT-TP-PP)	0.3	≥ 0.250 mm	≥ 0.200 mm	≥ 0.175 mm	≥ 0.150 mm	≥ 0.125 mm	⚠ ≥ 0.125 mm	⚠ ≥ 0.125 mm
Inner layer annular ring (IAR)	0.15	≥ 0.200 mm	≥ 0.150 mm	≥ 0.150 mm	≥ 0.125 mm	≥ 0.125 mm	≥ 0.125 mm	≥ 0.100 mm

⚠ The selected outer copper foil thickness (18 µm) requires a minimum outer layer isolation of 0.100 mm.
⚠ The selected inner copper foil thickness (35 µm) requires a minimum inner layer isolation of 0.125 mm and a minimum inner layer trackwidth of 0.125 mm.

Drill class

	Design values	Drill class A	B	C	D	E
Smallest final hole	0.35	≥ 0.50 mm	≥ 0.35 mm	≥ 0.25 mm	≥ 0.15 mm	≥ 0.10 mm

Figure 112: Pattern classes and Drill classes of Eurocircuits for the Gate Driver PCB

It is important to adjust the PCB layout design to the lower precision classes in order to reduce the cost of board manufacturing. In the case of the gate driver board, after making several changes to the layout, a manufacturing technology 4B was achieved. This type of technology implies a manufacturing cost of 97€ (Figure 113) which is acceptable for this type of application with high performance boards.

Eurocircuits also offers different prices depending on the quantity of PCBs to be manufactured and the working days of delay. In this case, given that three gate driver PCB are required to the setup, the most economical option is to order five boards with a unit price of 35,74 €.

Prices	Net
Single PCB	€ 97.17
Total boards	€ 97.17
Sales tax	€ 0.00
Total Gross	**€ 97.17**

Alternatives — Expand

Working Days	PCB quantity 1	2	5
2 WD	Net € 244.99 / € 244.99	Net € 162.68 / € 325.36	Net € 84.65 / € 423.25
3 WD	Net € 97.17 / € 97.17	Net € 70.43 / € 140.86	Net € 35.74 / € 178.70

Figure 113: Gate Driver PCB Manufacturing Price

Finally, the 3D renders of the new gate driver PCB to be manufactured is shown in Figure 114 and Figure 115. Annotations are incorporated into the overlay layers to make board assembly and testing more user-friendly.

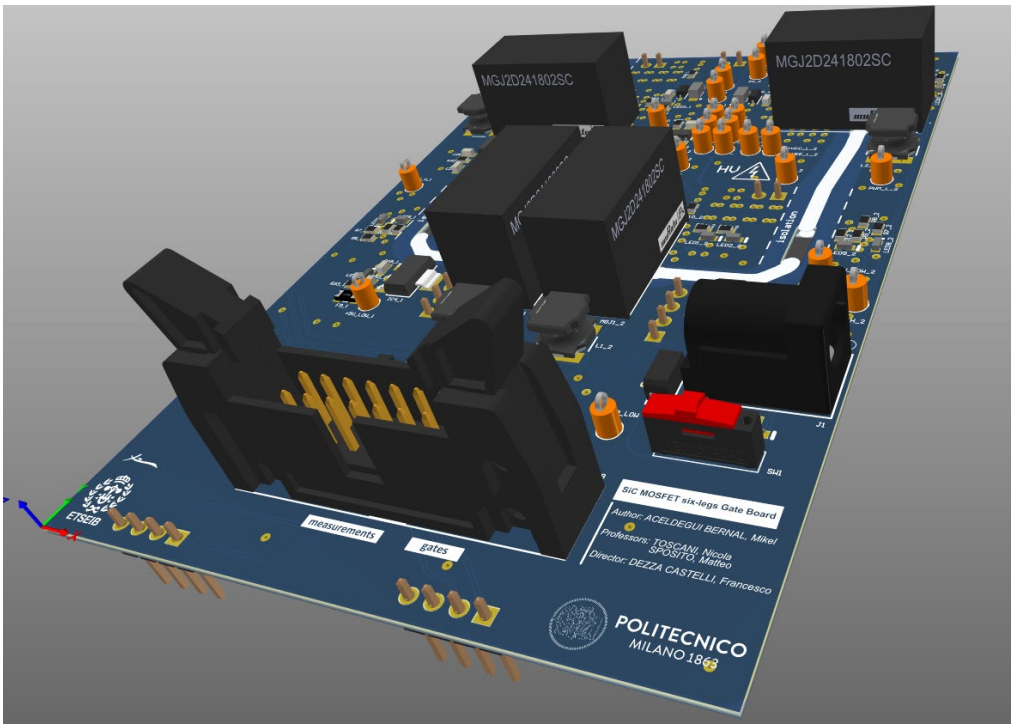


Figure 114: Top Render of the New Gate Drive Unit in Altium

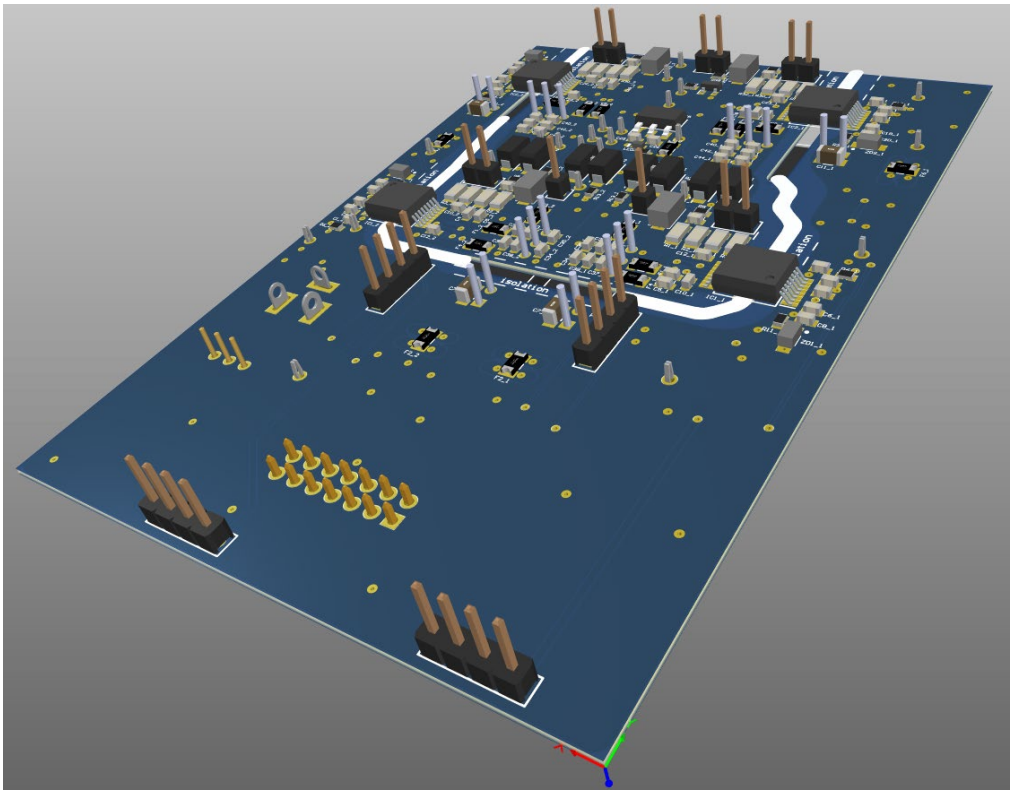


Figure 115: Bottom Render of the New Gate Drive Unit in Altium

4.4. Bill Of Materials (BOM)

The components used in the design of the new gate driver board are used to make the "Bill Of Materials" (BOM) table, , which lists the prices and quantities of all the necessary components in order to determine the total cost of the material.

Part Number	*Description*	*Quantity*	*Unit Price*	*Total Price*
61201422021	Male Box Header 14pins	1	1,77 €	1,77 €
61300111121	Vertical Pin Header 1pins	2	0,13 €	0,26 €
61300211121	Vertical Pin Header 2pins	5	0,13 €	0,65 €
61300411121	Vertical Pin Header 4pins	4	0,19 €	0,76 €
450301014042	SWITCH SLIDE POWER	1	2,26 €	2,26 €
694106301002	DC Power Jack Connector	1	1,02 €	1,02 €
C0603C104K5RAC3121	Capacitor 0.1uF	30	0,09 €	2,76 €
C0603X102K5RAC3316	Capacitor 1nF	4	0,31 €	1,24 €
C1608X7R1V105M080AE	Capacitor 1uF	12	0,16 €	1,93 €
C0603C225K4PACTU	Capacitor 2.2uF	1	0,14 €	0,14 €
C0603C106M9PACTU	Capacitor 10uF	7	0,27 €	1,90 €
GRM188R61E106KA73D	Capacitor 10uF, 25V	8	0,17 €	1,39 €
C0603C270J5GACAUTO7411	Capacitor 27pF	4	0,18 €	0,72 €
C0603C101J2GACAUTO	Capacitor 100pF	12	0,23 €	2,78 €
598-8070-107F	LED GREEN	1	0,31 €	0,31 €
STTH102A	High Efficiency Ultrafast Diode STTH102A	1	0,45 €	0,45 €
STTH112A	High Voltage Ultrafast Rectifier STTH112A	8	0,50 €	4,00 €
BAT54WS-TP	Schottky Diode 30V	4	0,36 €	1,44 €
0466001.NR	FUSE 1A	19	0,64 €	12,16 €
416131160804	SWITCH SLIDE 4pins	1	5,25 €	5,25 €
GRT31CR61H106ME01L	Capacitor 10uF, 50V	4	0,44 €	1,76 €
NR6045T100M	Inductor 10uH	4	0,41 €	1,64 €

5003	Test Point Orange	27	0,35 €	9,37 €
MGJ2D241802SC	DCDC Isolated Power Supply	4	8,42 €	33,68 €
MMSZ5232BT1G	Zener Diode 5.6V	4	0,24 €	0,96 €
MMSZ5242BT1G	Zener Diode 12V	4	0,25 €	1,00 €
CRCW06030000Z0EAHP	Resistor 0R	8	0,15 €	1,20 €
RCC06031K00FKEA	Resistor 1k	8	0,14 €	1,12 €
CRCW06031K20FKTA	Resistor 1k2	1	0,15 €	0,15 €
CRCW06032K20FKEAHP	Resistor 2k2	1	0,15 €	0,15 €
CRCW06035K10JNTA	Resistor 5k1	8	0,14 €	1,12 €
CRCW06038K20JNTA	Resistor 8k2	1	0,13 €	0,13 €
CRCW060310K0FKEAC	Resistor 10k	5	0,07 €	0,36 €
CRCW060333R0FKEAC	Resistor 33R	1	0,11 €	0,11 €
CRCW0603100KFKEAC	Resistor 100k	4	0,10 €	0,39 €
CRCW0603100RFKEAHP	Resistor 100R	4	0,16 €	0,64 €
RCG0603220RJNEA	Resistor 220R	3	0,11 €	0,33 €
CRCW0603390RFKEA	Resistor 390R	4	0,11 €	0,44 €
CRCW0603475RFKEAC	Resistor 475R	2	0,16 €	0,32 €
CRCW0603499KFKEBC	Resistor 499k	1	0,10 €	0,10 €
CRCW0603820RJNEA	Resistor 820R	4	0,09 €	0,34 €
RCWE0612R100JNEA	Resistor 1R	16	0,50 €	8,07 €
ACPL-W61L-000E	Digital Optocoupler	1	4,13 €	4,13 €
1ED3431MC12MXUMA1	Infineon Gate Driver	4	6,38 €	25,52 €
LTC6992CS6-1#TRMPBF	PWM Voltage Controlled	1	5,54 €	5,54 €
LM4040B50FTA	5V Shunt Reference Voltage	1	0,97 €	0,97 €
LM2937IMP-5.0/NOPB	5V DCDC Voltage Regulator	3	2,71 €	8,13 €
SMAJ22CA-E3/5A	Transient Voltage Suppressor 22V	4	0,52 €	2,08 €

TLMS1000-GS08	Low Current LED RED	8	0,43 €	3,44 €
TLMO1100-GS08	LED ORANGE	3	0,42 €	1,26 €
TLMS1100-GS08	LED RED	4	0,43 €	1,72 €
TLMY1000-GS08	Low Current LED YELLOW	4	0,43 €	1,72 €
				161,08 €

Table 14: Bill Of Material of the New gate drive PCB

Adding the total prices of each component, we get a material cost of the New gate driver PCB of 161,08 €. This price is given by the electronic components distributor "Mouser electronics".

Moreover, taking into account the manufacturing cost of the board by Eurocircuits, leads the total cost of the board. The calculation is made for the case of manufacturing only 1 board or manufacturing the 3 boards.

$$€(1\ PCB) = 97{,}17€ + 161{,}08€ = \mathbf{258{,}25}\ €$$

$$€(3\ PCB) = 178{,}70€ + 161{,}08€ \cdot 3 = \mathbf{661{,}94}\ €$$

The cost of the components in case of 3 boards can be reduced because the product distributors reduce the unit price of the components in case of ordering in lots. In addition, for PCB fabrication, it is possible to opt for options from Chinese manufacturers which have a lower cost, although the lead time for receiving the product increases.

5. CONCLUSION

First of all, the fact of studying and designing a six-phase SiC MOSFET based power converter with split output typology, provides a better understanding about the development of high power and high performance electronic boards.

Following the order of the sections in the report, several conclusions can be taken. The use of SiC chemistry for high-power applications is complicated but at the same time has a variety of advantages over normal silicon chemistry. On the other hand, gallium nitride (GaN) is interesting in higher switching frequency applications where its performance with respect to SiC starts to increase, and also, given that its control can be achieved higher frequencies, a better synthesizing of the output voltages can be performed, reducing the total harmonic distortion (THD) of the waveforms.

The use of split-output topology requires the use of a higher number of components but involves a number of significant improvements in inverter losses and the transient duration. Also, decoupling the high-side and low-side switches of the leg avoids short-circuit problems and incorporates free-wheeling diodes that improve the characteristics of the system.

The design of the DC-Link is very important, in many applications where its use is required, it occupies a large percentage of the system volume. For this reason, it should not be oversized and its connections to the SiC MOSFETs should be as short as possible to avoid stray inductance. This type of parasitic inductance must be taken into account because it produces voltage peaks due to the fast switching of the MOSFETs and can lead to a multitude of failures. The use of snubber reduces the possible unwanted effects of these stray inductances and makes the system safer.

Due to the increasing demand for silicon-based electronic devices, a semiconductor crisis is currently occurring. This crisis makes it difficult to find material in stock within the project deadlines, and for this reason the design of components with several options can solve the impossibility of finding stock for the manufacturing of the inverter.

It is important to select components designed for SiC-based high-power device systems, so in this way the inverter has a greater number of functionalities that provide robustness and extend the lifetime of the system. Desaturation protection or Active Miller Clamp in the drivers are functionalities designed for this type of devices and are relatively easy to apply with great advantages, therefore they should not be ignored and drivers with these features are recommended.

To realise a good hardware design for this type of high power applications, previous experience is required. Applications based on SiC devices that drive high power require a design that can avoid all the electromagnetic interference (EMI) that it generates, as well as reduce the crosstalk effect. Reading scientific papers and examining the layout design of other SiC-based applications can help in this task.

Design verification using software tools provided by electronic board manufacturers is key to ensure that the PCB is producible and to adjust the layout design to a technology that involves a lower manufacturing cost.

5.1. Total Cost of the Project

In order to have a more global vision of the estimated budget for the development of this project, a total sum of the costs associated with each part is calculated, including the engineering cost. This cost means the salary that would hypothetically have been paid to a worker for doing this work.

First, the cost of all proposed hardware changes and the manufacture of the new gate driver board is calculated. This calculation is made for the case of only modifying one leg of the converter or making changes to all three legs.

	Manufacturing **1 PCB**	Manufacturing **3 PCB**
Components New DC-Link	8,85 €	26,56 €
C Snubber Capacitors	7,30 €	21,90 €
Manufacturing Gate Driver Board	97,17 €	178,70 €
Component Gate Driver Board	161,08 €	483,24 €
	274,40 €	**710,40 €**

Table 15: Hardware cost of the new gate driver PCB (1 board & 3 boards)

On the other hand, the engineering cost is calculated by analysing the hours spent during the development of the project for each of the activities. With the corrected work plan (Figure 116), the following hours are obtained.

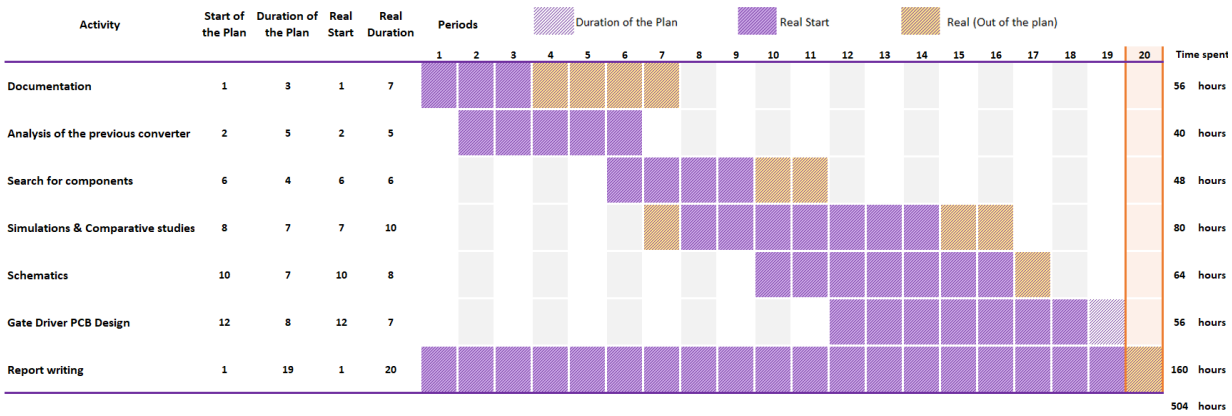


Figure 116: Planning and Hours spent in the project

Considering that an electronic design engineer receives €15 for each hour of work, the result of the engineering cost is as follows. In addition, to be more realistic with the cost of the project, it is assumed that the assembly of the components into a single board takes four working days (32 hours).

	Total Hours	€/h	
Hours spent in the project	504	15,00 €	7.560,00 €
Assembly of the components (x3 PCB)	96	15,00 €	1.440,00 €
			9.000,00 €

Finally, the total cost of the project can be calculated by adding the hardware and engineering costs (Table 16).

	Manufacturing **3 PCB**
Components New DC-Link	26,56 €
C Snubber Capacitors	21,90 €
Manufacturing Gate Driver Board	178,70 €
Component Gate Driver Board	483,24 €
Cost of Engineering	9.000,00 €
	9.710,40 €

Table 16: Total cost of the project for manufacturing and assembling 3 PCB of the gate driver unit

5.2. Future Work

It is important to define the next steps of the project in order to meet and improve the objectives to be achieved. In addition, the fact that the new designed gate driver board has not yet been manufactured and assembled in itself leaves a lot of work to be done.

One of the most important points of this future work is to reduce the distance between the DC-Link and the current MOSFETs modules on the power board since, as can be seen on the laboratory board, it is excessive. Because of this, the stray impedances that are created result in a negative system behaviour and suggest a redesign of a new power board, which implies a significant cost and could damage the MOSFETs devices with press-fit technology. To avoid this, the incorporation of snubber capacitors without modifying the original board can be a great solution to these unwanted phenomena, although it would mean an external assembly.

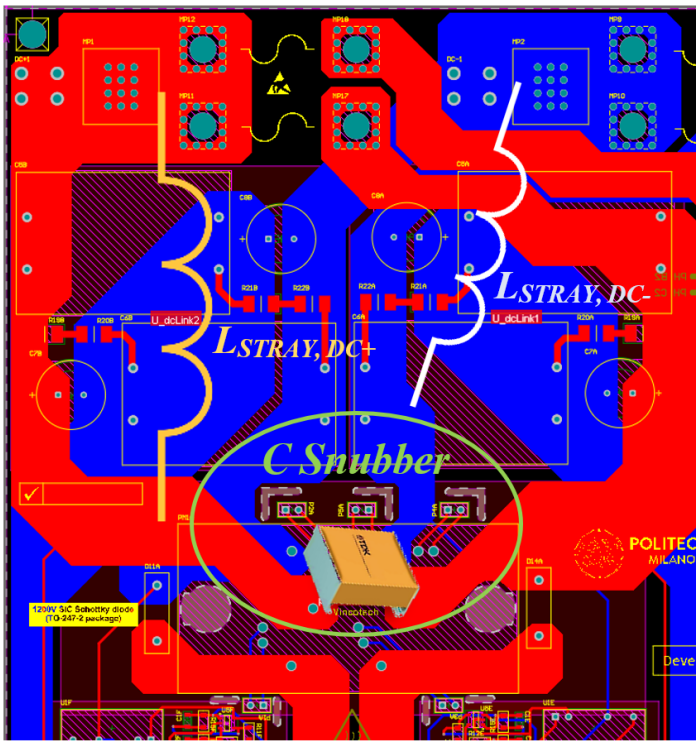


Figure 117: Layout design of the Power unit PCB with stray inductances and the capacitor C Snubber

Furthermore, the protection diodes (zener, schottky) of the DESAT circuit, which are incorporated in most of the drivers for the switching of high power IGBTs and MOSFETs, must be incorporated in the power board. When the Drain signal of the MOSFETs is carried from the power board to the gate driver board, the connector has to withstand switching voltages of 1000 V because when the device is switched off it blocks the DC-Link voltage. For this reason, in order to avoid the destruction of the connector and system failure, it is necessary to incorporate protection diodes that limit this voltage to an acceptable value before the connector and avoid high voltages on the gate driver board.

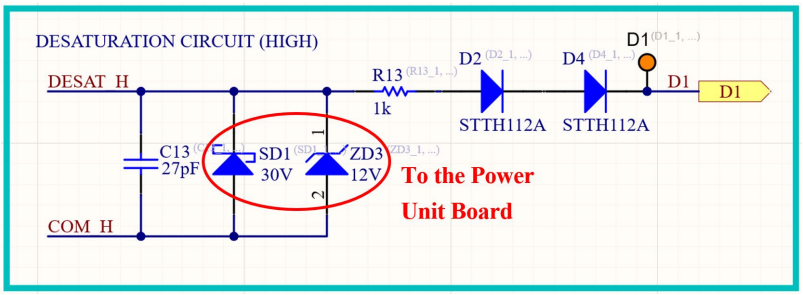


Figure 118: Desaturation protection circuit highlighting the protection diodes to be moved to the power unit board

The old board design does not incorporate a high side Drain terminal connector because the previous gate driver did not provide MOSFET desaturation control functions. As a result, it is necessary to incorporate an external connection and could be used to add the protection diodes of the DESAT circuit in parallel.

Regarding to the control algorithm in Simulink, the dead time treatment of the MOSFETs is not incorporated in the generation of the PWM signals, causing high voltages in the switching transients when the device is working in the half-bridge configuration when the two legs are not decoupled. Figure 118 shows a possible solution to this problem through the incorporation of a transport delay block and a logic AND block. This solution provides a time delay before the MOSFETs are switched on, thus avoiding possible simultaneous switching of both devices in the leg.

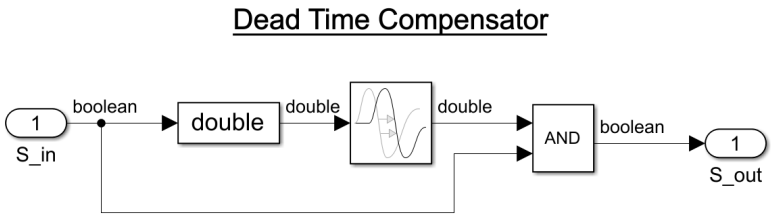


Figure 119: Dead time compensator solution for the switching of the SiC MOSFETs

Finally, by applying the improvements and propositions described in this thesis, the total space of the power converter could be reduced, decreasing its cost, and increasing its relations kW/kg and kW/m^3. Also, the option of using a semi-distributed configuration for the isolated DCDC converters should be studied (Figure 120). This type of configuration is based on sharing the same DCDC converter for the low-side MOSFETs since they have the same source reference, this reduces the components required and the space used, but makes fault monitoring more difficult.

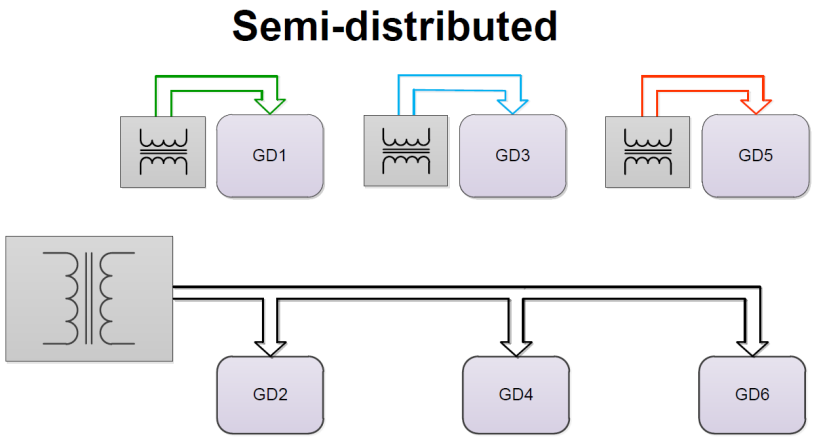


Figure 120: Semi-distributed gate driver architecture

List of Figures

Figure 1: Potential applications of GaN and SiC power switching transistors.

Figure 2: Comparison of some electrical and material properties of Si, 4H-SiC and GaN for power device applications.

Figure 3: Six-phase Split-Output configuration with SiC Schottky diodes in antiparallel.

Figure 4: Standard half-bridge topology.

Figure 5: Typical solution to avoid the conduction of the MOSFET body by using two external diodes

Figure 6: Six-phase split output inverter

Figure 7: Half-bridge converter with split output topology

Figure 8: Half-bridge split output converter with load

Figure 9: Control signals applied to the SiC MOSFETs (Double Pulse Test, DPT)

Figure 10: States of a Half-bridge split output converter in a Double Pulse Test (DPT)

Figure 11: Split Output SiC-Based Power Converter

Figure 12: Space vector diagram of a three-phase inverter output voltage.

Figure 13: Simulation of the RMS current of the DC-Link in a three-phase inverter with SVM for a PM Motor

Figure 14: DC-Link RMS Current vs Index Modulation in a three-phase inverter with SVM for a PM Motor

Figure 15: DC-Link capacitor connections from the lab power board design

Figure 16: New proposal DC-Link capacitors connections for the power board design

Figure 17: Comparison of voltage and current transients during switching of an Si IGBT and a SiC MOSFET

Figure 18: Current path when turn-off surge occurs

Figure 19: C Snubber capacitor in a MOSFET leg

Figure 20: Passive snubber circuits. (a) C snubber, (b) RC snubber, (c) Discharge RCD snubber, (d) Non-discharge RCD snubber

Figure 21: C snubber with the I_{MAIN} path

Figure 22: Test setup used for the Double Pulse Test

Figure 23: Double Pulse Test MOSFET control signal

Figure 24: Simulation Model of a single leg of the converter in PSIM

Figure 25: DC-Link Subcircuit of the converter in PSIM

Figure 26: C4AF7BW4680T3JK PSPICE parameters and its model in PSIM

Figure 27: AT1H 860241478004 PSPICE parameters and its model in PSIM

Figure 28: PSIM level 2 configuration parameters of the SiC MOSFET and SiC Diode

Figure 29: Bootstrap circuit configuration in PSIM

Figure 30: Half Bridge configuration of the converter and its Model in PSIM

Figure 31: Simulation of the Double Pulse Test in Half-Bridge configuration using PSIM

Figure 32: Comparison of the Drain-Source voltage at turn-off between real test and PSIM Simulation (Half Bridge)

Figure 33: Split Output configuration of the converter and its Model in PSIM

Figure 34: Simulation of the Double Pulse Test in Split Output configuration using PSIM

Figure 35: Comparison of the Drain-Source voltage at turn-off between real test and PSIM Simulation (Split Output)

Figure 36: Simulation of the Double Pulse Test (τ_1) in Split Output configuration using PSIM (700V)

Figure 37: Drain-Source voltage at turn-off in Half bridge configuration PSIM Simulation (700V Supply)

Figure 38: Drain-Source voltage at turn-off in Split output configuration PSIM Simulation (700V Supply)

Figure 39: New Simulation Model of a single leg of the converter with snubber in PSIM

Figure 40: New Proposed Half bridge model in PSIM

Figure 41: Drain-Source voltage at turn-off of the New proposed half bridge configuration PSIM Simulation (700V Supply)

Figure 42: New Proposed Split output model in PSIM

Figure 43: Drain-Source voltage at turn-off of the New proposed split output configuration PSIM Simulation (700V Supply)

Figure 44: PMDC Control Simulink model for testing the new proposed models by the SimCoupler block

Figure 45: Working Principle of PWM for the PMDC Control using unipolar modulation strategy (leg A).

Figure 46: Working Principle of PWM for the PMDC Control using unipolar modulation strategy (leg B).

Figure 47: New Proposed Half bridge model for the PMDC Control in PSIM

Figure 48: Mechanical Angular Speed "ω_m" (Reference vs PSIM simulation) in a Half bridge configuration

Figure 49: Armature Current "I_A" (Reference vs PSIM simulation) in a Half bridge configuration

Figure 50: Drain-Source voltage at turn-off in a Half bridge configuration, PMDC Motor Control

Figure 51: Gate-Source voltage "V_{GS}" & Armature Current "I_A" at turn-off in a Half bridge configuration, PMDC Control

Figure 52: DC-Link voltage in a Half bridge configuration, PMDC Motor Control

Figure 53: New Proposed Half bridge model for the PMDC Control in PSIM

Figure 54: Mechanical Angular Speed "ω_m" (Reference vs PSIM simulation) in a Split Output configuration

Figure 55: Armature Current "I_A" (Reference vs PSIM simulation) in a Split Output configuration

Figure 56: Drain-Source voltage at turn-off in a Split Output configuration, PMDC Motor Control

Figure 57: Gate-Source voltage "V_{GS}" & Armature Current "I_A" at turn-off in a Split Output configuration, PMDC Control

Figure 58: DC-Link voltage in a Split Output configuration, PMDC Motor Control

Figure 59: 3D Renders of the Gate Drive Unit in Altium

Figure 60: Fiber Optical Cable vs Copper Wire

Figure 61: Electromagnetic Interference from a Power Wire to a Signal Wire

Figure 62: Distances between connectors in the Power Board and the Gate Driver Board

Figure 63: Example of a bootstrap circuit

Figure 64: Bootstrap operation, low-side MOSFET turn on

Figure 65: Bootstrap operation, high-side MOSFET turn on

Figure 66: Bootstrap of the Gate Driver Board, charging path of the bootstrap capacitor

Figure 67: Bootstrap of the Gate Driver Board, discharging path of the bootstrap capacitor

Figure 68: Freewheeling current path and Waveforms in a Half bridge application with bootstrap circuit at turn-off

Figure 69: Isolated Gate Driver in a Half bridge configuration with Isolated DCDC Converters (Bipolar Output)

Figure 70: Current Through "Miller" capacitance (C_{GD}) opposes switch off

Figure 71: Distributed gate driver architecture

Figure 72: Isolated DCDC Converter MGJ2D series from Murata

Figure 73: Isolated Gate Driver 1ED34x1Mc12M series from Infineon

Figure 74: Connections of the EiceDriver in a typical Half bridge configuration

Figure 75: Schematic circuit diagram of the Isolate DCDC converter MGJ2D241802SC

Figure 76: Schematic circuit diagram of the 5V regulator LM2937IMP-5.0, SiC Module phase supply

Figure 77: Schematic circuit diagram of the 5V regulator LM2937IMP-5.0, NTC isolated supply

Figure 78: Pinout and functionalities of the isolated gate driver 1ED3431MC12MXUMA1

Figure 79: Schematic of the supply circuit of the Isolated gate driver 1ED3431MC12MXUMA1

Figure 80: Schematic of the RDYC_H & FLT_N circuits of the Isolated gate driver 1ED3431MC12MXUMA1

Figure 81: Schematic of the pin IN circuit of the Isolated gate driver 1ED3431MC12MXUMA1

Figure 82: Comparison between the Linear region of an IGBT and a MOSFET

Figure 83: Desaturation protection circuit of the 1ED3431MC12MXUMA1 isolated gate driver

Figure 84: Desaturation protection circuit in Normal Operation

Figure 85: Desaturation protection circuit in Saturation Operation

Figure 86: DESAT timing with leading edge blanking, filter, and reaction times

Figure 87: Schematic of the Desaturation circuit of the Isolated gate driver 1ED3431MC12MXUMA1

Figure 88: Spreadsheet for desaturation calculations by Texas Instruments

Figure 89: Schematic of the pin ADJA & ADJB circuit of the Isolated gate driver 1ED3431MC12MXUMA1

Figure 90: Schematic of the MOSFET gate driver circuit of the Isolated gate driver 1ED3431MC12MXUMA1

Figure 91: Gate Driver Circuit of the driver 1ED3431MC12MXUMA1

Figure 92: Schematic of 10-PC124PA040MR-L638F18Y , Vincotech module

Figure 93: Schematic of the Temperature measurement circuit

Figure 94: Typical application of the LTC6992CS6-1

Figure 95: Voltage divider circuit for the generation of the modular signal

Figure 96: Functional diagram of the ACPL-W61L-000E

Figure 97: Operation of the shunt reference voltage

Figure 98: Schematic of the 5V shunt reference voltage circuit for supply

Figure 99: Sheet symbols connections of the new gate driver board design

Figure 100: Block Diagram of the power consumptions in the new gate driver board

Figure 101: Quiescent and operating currents for the 1ED3431MC12MXUMA1 driver

Figure 102: Layer Stack Manager of the gate driver PCB

Figure 103: Placement of vias in the gate driver PCB layers

Figure 104: Measurement Point of the gate driver PCB

Figure 105: Measurement Points by using traces and vias in other PCB design

Figure 106: Routing of the Gate and Source signals in the gate driver PCB

Figure 107: Routing of the Drain and Source signals in the gate driver PCB

Figure 108: Polygon Pour Design of the VCC layer from the Gate Driver PCB

Figure 109: Isolation Barrier of the Gate Driver PCB

Figure 110: PCB Visualizer Tool of Eurocircuits for the Gate Driver PCB

Figure 111: PCB Checker Tool of Eurocircuits for the Gate Driver PCB

Figure 112: Pattern classes and Drill classes of Eurocircuits for the Gate Driver PCB

Figure 113: Gate Driver PCB Manufacturing Price

Figure 114: Top Render of the New Gate Drive Unit in Altium

Figure 115: Bottom Render of the New Gate Drive Unit in Altium

Figure 116: Planning and Hours spent in the project

Figure 117: Layout design of the Power unit PCB with stray inductances and the capacitor C Snubber

Figure 118: Desaturation protection circuit highlighting the protection diodes to be moved to the power unit board

Figure 119: Dead time compensator solution for the switching of the SiC MOSFETs

Figure 120: Semi-distributed gate driver architecture

List of Tables

Table 1: DC-Link capacitor bank Requirements

Table 2: DC-Link capacitors specifications of the laboratory power board design

Table 3: New proposal DC-Link capacitors specifications for the power board design

Table 4: Values for the calculation of the peak voltage at the drain-source terminals of the MOSFETs

Table 5: C Snubber capacitor specifications

Table 6: Stray Inductances of the PSIM model of the converter

Table 7: MGJ2D241802SC main characteristics

Table 8: 1ED3431MC12MXUMA1 main characteristics

Table 9: Gate driver board input and output signals and properties

Table 10: Desat filter time adjustment with ADJB in 1ED34x1Mc12M isolated gate drivers

Table 11: Soft-off adjustment with ADJA in 1ED34x1Mc12M isolated gate drivers

Table 12: Internal Gate Driver resistor driver 1ED3431MC12MXUMA1

Table 13: DIVCODE Programming of the LTC6992CS6-1

Table 14: Bill Of Material of the New gate drive PCB

Table 15: Hardware cost of the new gate driver PCB (1 board & 3 boards)

Table 16: Total cost of the project for manufacturing and assembling 3 PCB of the gate driver unit

Bibliography

[1] Giorgio Ferrara, Prof. Francesco Castelli Dezza, Ing. Mattia Rossi, Prof. Iustin Radu Bojoi. Control and hardware design of a SiC MOSFET-based power converter with SiC Schottky Diodes utilizing a split output topology for superior dynamic behaviour. *Politecnico di Milano, Master Thesis in Automation and Control Engineering, Academic year 2020-2021.*

[2] Andrea Polastri, Matteo Sposito, Prof. Francesco Castelli Dezza, Ing. Mattia Rossi. Model Predictive Voltage Control of Step Down DC-DC Converters: Implementation and Hardware Design. *Politecnico di Milano, Master Thesis in Automation and Control Engineering, Academic year 2018-2019.*

[3] Tetsuzo Ueda. Reliability issues in GaN and SiC power devices. *Power Electronics Development Center, Automotive & Industrial System Company, Panasonic Corporation 3-1-1 Yagumo-nakamachi, Moriguch-shi, Osaka 570-8501, Japan. IEEE Explore, 21 July 2014.*

[4] Specter engineering. Inverter DC Link Capacitor Selection. *10 September 2019*

[5] ROHM Semiconductor. Snubber circuit design methods. *ROHM Application Note, April 2020.*

[6] Joachim Lamp. IGBT Peak Voltage Measurement and Snubber Capacitor Specification. *Semikron Application Note AN-7006, 17 March 2008.*

[7] Fairchild Semiconductor Corporation. Design and Application Guide of Bootstrap Circuit for High-Voltage Gate-Driver IC. *Fairchild Application Note AN-6076, 30 September 2008.*

[8] Texas Instruments. UCC21750 10-A Source/Sink Reinforced Isolated Single Channel Gate Driver for SiC/IGBT with Active Protection, Isolated Analog Sensing and High-CMTI. *Texas Instruments Datasheet, December 2019.*

[9] TI Live! India Automotive Seminar, Bing Lu. Isolated Bias Supply Solutions for Isolated Gate Drivers. *Texas Instruments Seminar, 10 December 2021.*

[10] Pedro Miguel Batista de Sousa Correia da Costa. Compact three-Phase SiC Inverter for the IST Formula Student Prototype. *Técnico Lisboa, Thesis to Obtain the Master of Science Degree in Electrical and Computer Engineering, November 2018.*

[11] M. Vujacic, M. Hammami, M. Srndovic, G. Grandi. Evaluation of DC Voltage Ripple in Three-Phase PWM Voltage Source Inverters. *Dept. of Electrical, Electronic and Information Engineering, University of Bologna, (Italy). 09 June 2022.*

[12] Felix Kaiser, Julian Klein (Tufast e.V.). Electric Power Conversion in Formula Student Cars. *Power Electronics, FSG Academy 2020/2021, 16 April 2021.*

[13] Pan Hao Company. How to operate IGBT modules in parallel properly. *Pan Hao Application Note.*

Agradecimientos

El trabajo de investigación de esta tesis ha sido posible gracias a la universidad politécnica de Milán, la cual me ha acogido durante mi programa de movilidad internacional Erasmus+ y me ha brindado todas las facilidades necesarias para llevar a cabo el proyecto. Agradecer también al profesor Frascesco Castelli Dezza por hacer posible mi investigación en temas relacionados con conversión de energía, electrónica de potencia y a los profesores Nicola Toscani, Matteo Sposito por realizarme el seguimiento y dedicar su tiempo para ayudarme con cualquier dificultad.

Por otro lado, gracias a la universidad politécnica de Catalunya pude pertenecer durante 3 años al equipo de Formula Student BCN eMotorsport donde he podido adquirir mis conocimientos sobre control y diseño de inversores de alta potencia para aplicaciones de tracción eléctrica. Gran parte de estos conocimientos vienen gracias a la ayuda de otros miembros del equipo como Santi Prats, amigo y un gran ingeniero de sistemas electrónicos, Quim Pérez, ayudante durante el diseño del layout del primer inversor, Daniel Montesinos, tutor durante toda mi estancia en Formula Student y otras muchas personas que siempre han estado ahí dando su apoyo desde el punto de vista ingenieril.

Finalmente y no menos importante, este trabajo de tesis y toda mi trayectoria se la debo a mi familia y amigos. Sin su apoyo, no hubiera sido posible terminar mis estudios de master y desarrollarme tanto a nivel personal. No toda la gente tiene la misma suerte y facilidades, es por ello que hay que valorar donde estamos y siempre que sea posible dar el máximo de sí mismo.

A todos ellos lectores que lleguen a esta página de agradecimientos, agradezco su tiempo y espero que esta tesis haya sido de ayuda para obtener un mayor conocimiento el cual compartir con otros.