Development and Testing of the 3U+ CubeSat PCDU for SOURCE

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Abstract
SOURCE (Stuttgart Operated University CubeSat for Evaluation and Education) is a 3U+ research CubeSat that is being developed by students at the University of Stuttgart in cooperation with the Institute for Space Systems and the Small Satellite Student Society KSat e.V.. The objectives include technology demonstrations, atmospheric research and the investigation of satellite demise while also serving as an educational program. SOURCE was selected by ESA's "Fly your Satellite" program and is currently in Phase D.

The electrical power supply system combines commercial off-the-shelf parts with self-developed units to meet the requirements of the payloads. The solar array configuration and Power Conditioning and Distribution Unit (PCDU) are self-developed, while the battery is a commercial product.

A total of 56 solar cells provides up to 32W under ideal conditions, which can be stored in a 75Wh space-qualified lithium-ion battery. To maximise the power output of the solar cells, maximum power point tracking is performed by the PCDU. This is controlled by a radiation hardened microcontroller.

The PCDU provides regulated 3.3V, 5V and unregulated battery voltage to the subsystems with 32 switchable outputs, 27 of which are latch-up current protected. The microcontroller controls these individual output channels and the switching between the various CubeSat modes as commanded by the on-board computer. Additionally, every output channel power consumption is monitored for overcurrents. The PCDU functions as a watchdog by checking the health of the on-board computer, rebooting it in case of a failure. High priority commands can be sent directly to the PCDU from the ground via the communication system, bypassing the on-board computer. These can reset either the communication subsystem, the on-board computer or the entire satellite.

Four hybrid inhibits, using a combination of mechanical switches and FETs are integrated in the PCDU, replacing the usual fully mechanical design. Three are used to deactivate the satellite in the deployer configuration and the fourth is a remove-before-flight inhibit.

An engineering model was manufactured during phase C and is being tested functionally, environmentally and for performance. This paper presents the detailed design of the PCDU, the acquired test results and outlines issues encountered during the tests.

Keywords
CubeSat, EPS, PCDU, SOURCE

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Acronyms/Abbreviations

CSA	*Current Sense Amplifier*
DPS	*Deployment Switch*
EMC	*Electromagnetic Compatibility*
FET	*Field-Effect Transistor*
IRS	*Institute for Space Systems*
LCL	*Latch-up Current Limiter*
MPPT	*Maximum Power Point Tracking*
MRAM	*Magneto resistive Random-Access Memory*
OBC	*On Board Computer*
PCDU	*Power Conditioning and Distribution Unit*
PV	*Photovoltaic*
PWM	*Pulse Width Modulation*
RBF	*Remove Before Flight (pin)*
SOURCE	*Stuttgart Operated University Research CubeSat for Evaluation and Education*
UR	*unregulated (voltage rail)*

1. Introduction

Practical projects are an important part of university education. At the University of Stuttgart, the Small Satellite Student Society KSat e.V. and the Institute of Space Systems (IRS) are working together on a student CubeSat with the help of several industry partners to provide such a project. The Stuttgart Operated University Research CubeSat for Evaluation and Education (SOURCE) is a 3U+ CubeSat with many in-house developments designed and built by bachelor and master students under supervision of PhD students of the IRS [1]. The SOURCE project is currently in phase D preparing for the manufacturing readiness review as part of ESA's *Fly Your Satellite!* program.

The primary objective is to develop a reproducible CubeSat platform and verification of new technologies provided by industry partners. The secondary objective is the study of the re-entry of natural and man-made objects. The re-entry of SOURCE itself is also part of the mission [1]. For these purposes, the electrical power supply subsystem has to provide power over a wide range of mission phases and for a wide range of subsystems and payload components. There are several other student projects with custom Power Conditioning and Distribution Units (PCDU) like PW-Sat [2] or UpSat [3] and commercial products available by companies like GomSpace, ISISpace. Acquiring commercial components offers the benefit of already tested and validated hardware. However, none of the available products could satisfy the educational and technical requirements set by the objectives of SOURCE.

The PCDU was therefore self-developed to provide a comprehensive educational overview of a PCDU. Additionally, it could be tailored to the specific mission of SOURCE and at the same provide a base for future CubeSats projects. This paper will focus on the design of the PCDU, the findings made during testing and performances which were determined.

2. Functional Architecture

The general hardware architecture can be seen in Figure 1. The PCDU has two power inputs, and three voltage channels, 3.3 V, 5 V and an unregulated (UR) output. The UR output is directly connected to the 75 Wh lithium-ion battery, with the voltage depending on the charge level, varying from around 12 V to 16.8 V. The GomSpace BPX battery is a commercial component. The rad-hard microcontroller VA10820 from Vorago Technologies, controls the Maximum Power Point Tracking (MPPT) as well as collecting data and communicating with the On-Board-Computer (OBC), which includes a watchdog function, to restart the OBC.

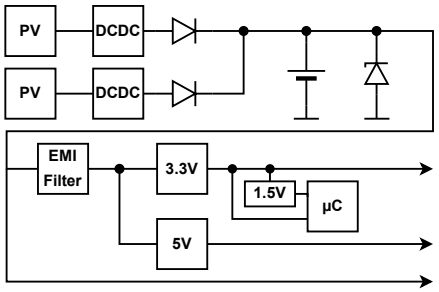

Figure 1. PCDU functional architecture.

The program code is stored on a hardware write-protected Magneto resistive Random-Access Memory (MRAM) chip. Measurement data and other non-volatile parameters are stored on a second MRAM chip. High priority commands to reset the PCDU, OBC or even the entire satellite are independent from the OBC. These commands are directly forwarded to the PCDU from the communication system by a simple high-low signal for maximum simplicity. In the following a brief overview of the key elements of the hardware design is given.

2.1. Power Input

2.1.1. Photovoltaic Arrays

A Photovoltaic (PV) string has seven solar cells (Azurspace 3G30C-Advanced) connected in series, with each individual cell having a bypass diode. The strings are arranged according to Figure 2, forming two large PV arrays made of carbon fibre reinforced polymer laminate.

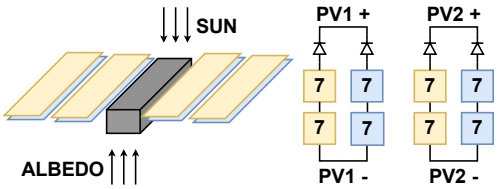

Figure 2. Solar-Cells Array configuration.

Two strings each are connected in series, with a string diode to prevent any reverse currents. The results in an open clamp voltage of 37.8 V and a maximum power point voltage of around 33.75 V. The DC-converters connected to the PV array were chosen to be buck-converters and therefore the input voltage must be higher than the output, which is determined by the battery (max. 16.8 V). In addition to this, the solar cells orientated to the albedo side, will be connected in parallel to the cells orientated towards the sun. This increases the total current and thus the efficiency of the DC-converters. The PV array provides up to 32 W under ideal conditions. The dual side PV array setup also improves power generation during tumbling.

2.1.2. Input Conditioning

A schematic of the input paths plus the interface with the microcontroller is shown in Figure 3.

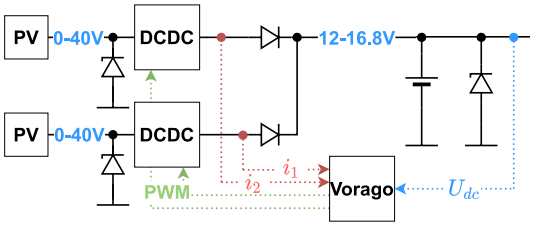

Figure 3. Schematic of input rails.

Each PV array is connected to redundant DC-converters which are controlled by an MPPT algorithm. Zener- or rather transient voltage suppressor diodes protect the input for voltage peaks, that will likely occur during the transition between the shadow and sun phases. In this situation, the solar cells are cold and the open clamp voltage is increased due to the lower temperature. The controlling of the DC-converter output is done by applying an external voltage at the feedback pin of the converter. The resistor and the capacitor form a low pass filter, which outputs the mean value (DC voltage) of the Pulse Width Modulated (PWM) input. By changing the duty cycle of the PWM signal, the control voltage changes, which then leads to a different output voltage. The PWM method was chosen for its simplicity and robustness since the rad-hard microcontroller is used to generate the PWM signal.

2.2. Power output

The power output is designed redundantly. The 3.3 V, as well as the 5 V rail, are supplied by three parallel non-synchronised Buck-Converters, each with a fixed voltage. Not synchronising the DC-converters usually decreases efficiency, due to unequal load sharing and by operating at lower loads on average. However, synchronised converters would not be fully redundant. Each voltage rail connects to the individual subsystem switches. A latch-up-current protection is also integrated for most switches. There are a total of 32 switchable channels, 27 of which integrate the latch-up current limiters (LCLs). Five protected and all five unprotected channels are on the UR voltage rail. The 5 V voltage rail supplies eight channels and the 3.3 V voltage rail is connected to 14 channels.

2.2.1. Output channel switches and Latch-Up Current protection

The switching circuit, with the LCL, can be seen in Figure 4. The microcontroller activates and deactivates the redundant high-side switches.

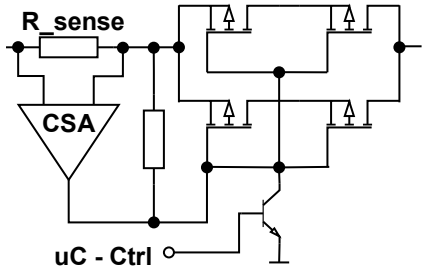

Figure 4. Switching circuit with current limiting.

The additional protection for latch-up events is handled in a hybrid configuration of hardware and software. The microcontroller monitors the current of the output and deactivates it in an overcurrent event. To avoid any damage due to the delay of the microcontroller processing, a hardware current limit is implemented. This is achieved by connecting the output of the Current Sense Amplifier (CSA) to the gate of the FETs. If the current reaches a certain value, the

resistance of the FETs increases, thus leading to a limitation of the current. Then the microcontroller deactivates the output.

2.3. *Inhibits*

The configuration in Figure 5 of the deployment switches represents the standard configuration to fulfil the requirements from ESA and launcher companies like Nanoracks [4].

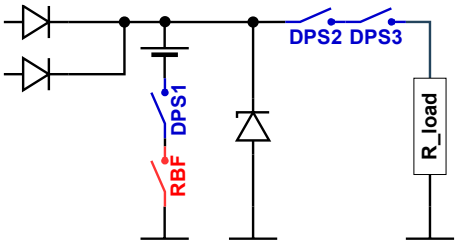

Figure 5. General inhibit configuration.

Usually, these inhibits are large mechanical switches, in the structure of the CubeSat, that are being actuated while they are in the deployer. Due to lack of space in the structure of SOURCE, small switches had to be used instead. These cannot handle the high currents of the main bus, which is why an electro-mechanical approach was developed. This consists of replacing the large mechanical switches with FETs which are activated by the smaller mechanical switches. This also improves overall magnetic cleanliness since it reduces major current loops through the satellite. Figure 6 shows the functional architecture.

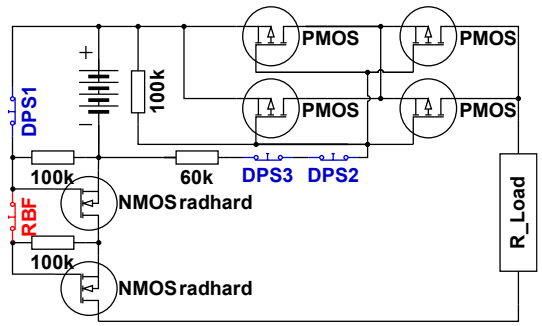

Figure 6. Inhibit configuration for the electro-mechanical solution.

3. Test Results

Figure 7. PCDU engineering model.

Part of the development process is the functional testing campaign. For this purpose, an engineering model (see Figure 7) was manufactured in phase C.

Testing began in March 2021 and is still ongoing. Since SOURCE is a student project, testing campaigns were intermittent and had to be paused during exam periods. Overall, all functions of the PCDU could be verified, however not without some troubleshooting and iteration. At the time of writing, the thermal-vacuum tests and full system efficiencies measurements are still to be conducted.

3.1. *Anomalous component tests*

3.1.1. *Inhibits*

During the development of the inhibits it was discovered that the battery could still be charged while all Deployment Switches (DPS) were actuated. This could lead to overcharging of the battery, since the control logic is disabled by the inhibits. Therefore, the enable pins of the input DC-converters were integrated in the design, actively enabling and disabling the converters together with the DPS FETs. This however requires the battery voltage at the enable pins of the converter to enable charging with the solar panels. This prevents solar-only operation, without the battery.

3.1.2. *Latch-up Current Limiters*

For testing the maximum current before current-limiting, a DC load in constant resistance mode was used to emulate a high current draw on the LCLs. During testing highly anomalous behaviour occurred with LCLs on all output voltages. Figure 8 shows the oscilloscope measurement of the 5 V output during current limiting operation. Similar behaviour could be observed with the 3.3 V and unregulated (UR) LCLs.

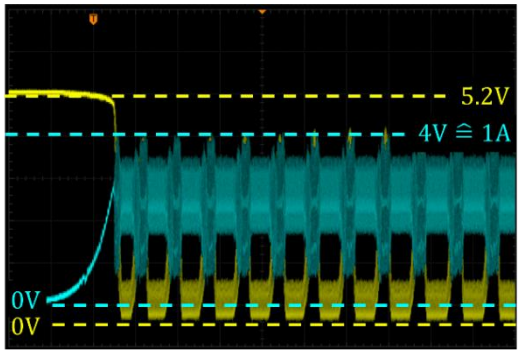

Figure 8. Anomalous behaviour of a 5V LCL during current limiting operation over 6ms. Yellow is the output voltage; Blue is the voltage of the CSA and corresponds to the current.

Extreme oscillations can be seen and no stable current limiting could be established.

The first assumption was an instability in the feedback circuit, mainly due to high resistor values, insufficient smoothing capacitance and due to the large amplification of 500x by the CSA. New simulations in LTSpice did not provide any new findings, neither did additional tests with new configurations with different resistors and CSAs. The test setup was re-evaluated and an additional test was conducted using fixed load resistors instead of the DC-load (using the same resistance values).

The result can be seen in Figure 9. Apart from some ripple, stable current limiting could be achieved and the DC-load was determined as the cause for the initial anomalous behaviour.

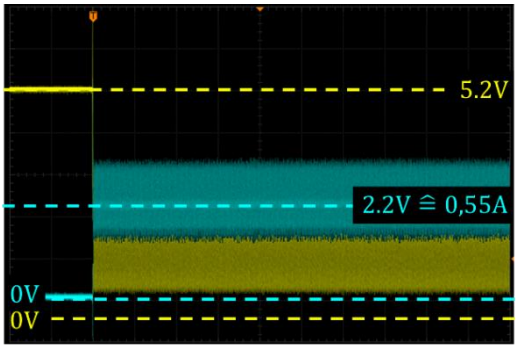

Figure 9. Stable current limiting of a 5V LCL during current limiting operation over 6ms.

The original design of the LCL circuit was concluded to be functional as intended as the anomalous behaviour was solely caused by the initial test setup.

3.1.3. MRAM chips

It was discovered that the initially selected Everspin 128 kB MRAM chip could not be flashed properly. This was because the smaller chips of Everspin's MRAM chip range have a smaller address width and therefore cannot be used with the VA10820. The 1 Mb version on the other hand could be flashed without issues.

3.1.4. Electromagnetic compatibility tests

In addition to the functional testing, a radiating emission test has been performed to verify conformal emission of the PCDU, especially in the S-band range. This range is relevant because most of SOURCE's communication is done via S-band [1]. A horn antenna was positioned at 1 m distance from the PCDU. Both polarizations were measured. The results showed some peaks in the S-band (up to 50 dBµV/m). Future measurements will involve sniffing tests to localize the emitting element. However, the result is not necessarily critical since it has to be compared with the sensitivity of the S-band module.

3.2. Performance

3.2.1. Inhibits

The hybrid design of the inhibits has the disadvantage that a small leakage current is always present. The results for different combination of active inhibits switches are seen in Table 1. The leakage is minimal and acceptable for a required state of charge of 80 % at deployment.

Table 1. Leakage of hybrid inhibits. Time t until battery is discharged to 80% state of charge.

	U / V	I / mA	P / mW	t / d
RBF	14.28	0.250	3.57	175
DPS1/2/3	14.28	0.020	0.29	2156
DPS1/2/3 + RBF	14.28	0.001	0.02	36473

Additionally, during operation losses also occur due to the on-resistance of the FETs. These losses are listed in Table 2 and are not negligible for higher currents.

Table 2. Losses of hybrid inhibits. Current and voltage on the main bus.

I / A	U / V	P_IN / W	P_loss / W
0.50	13.95	6.97	0.04
1.00	13.90	13.90	0.11
2.00	13.80	27.59	0.41
2.50	13.73	34.33	0.67

3.2.2. Input DCDC converter

Lower performance due to unequal load sharing was reproduced in the tests. One converter delivered the main load up until 1 A output current. After that both converters delivered the same amount of power, raising efficiency to that of a single converter. The input converter can be operated in a large range of operation. This includes an input voltage range of 20 – 38 V, an output voltage range of 12 – 18 V (set by PWM duty cycle between 0 – 100 %) and a load current range of 0 - 2.5 A. Over the whole range an average input efficiency of 88% was achieved.

3.2.3. Output DCDC converter

The output converters also are not synchronised and do not share the load equally. A 12 – 18 V main bus voltage and 0 – 2.5 A output current was used for both 3.3 V and 5 V. Full load

sharing between all three converters was only reached at 2 A output current for both voltage rails. In this case this proved to be beneficial, as the higher efficiency of a single converter was achieved during lower load operation. An average efficiency of 89 % was achieved on the 5 V rail and an average 87 % on the 3.3 V rail. The most efficient operating range was between 0.5 A and 1 A output current for both voltage rails.

3.2.4. Latch-up Current Limiters

Hardware current limiting could be achieved in 2 µs for the 3.3 V LCLs, 10 µs for the 5 V LCLs and 20 µs for the UR LCLs.

4. Discussion

Many Student projects face the decision whether to purchase a commercial product or to build their own PCDU. The experience made in SOURCE, shows that the added complexity and manpower necessary for the entire development and testing must be considered carefully. However, the benefits in education and for future developments have proven to be valuable.

One of the lessons learned during the testing was recognising the role of measurement and testing equipment and their ability to interfere with the measurements. Another lesson was, that power converters are often portrayed in their optimal operating conditions in their datasheets, with real-world applications performing differently, especially when converters are used in parallel. Additionally, testing the PCDU with wide-ranging operating conditions, leads to numerous tests and drastically increases testing time. For example, the input converters were first to be tested, following the logical paths of the PCDU from the PV cells to the switches. In hindsight, these initial tests, which covered the entire range of operating conditions and were conducted manually, only provided limited benefit and the testing could have been reduced to simple functional testing for a selection of operating conditions. A better way of conducting full operational tests would have been to use automated data acquisition combined with the internal logging capabilities of the PCDU at a later date.

The hybrid inhibit design provides great benefits for the size and mass constraints of CubeSats, however the higher losses need to be considered in the power budget and the added complexity must be taken into account as well.

5. Conclusion

For SOURCE, a custom PCDU was developed. The functionalities were all successfully tested and their performances were determined to be as expected. Further tests yet to be conducted are the thermal vacuum chamber test and radiation sniffing tests to find and assess the source of the radiated emission in the S-band spectrum, and tests of the MPPT algorithm using the PCDU and solar cells.

The testing of the PCDU will continue and likely provide further educational value. The next milestone of SOURCE is the mission readiness review mid-2022, at which point functional testing of the PCDU must be completed. Afterwards, the flight hardware will be manufactured and FlatSat system testing will begin. There are still several test campaigns to be conducted until the PCDU is fully flight worthy and can be considered for future projects. However, the design, development, and lessons learned are already being applied.

Acknowledgements

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