Analysis of ISSQ/IDDQ Testing Implementation and Circuit Partitioning in CMOS Cell-Based Design

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Abstract

Difference between ISSQ and IDDQ testing strategies is presented, discussing the dependency of area overhead and sensing speed on the technology. The current sensor implementation style suitable for cell-based design methodology or semi-custom design style is proposed. Experimental results for each strategy are discussed. Finally, different types of partitioning strategies are showed, taken into account the parallelism of the gates.

1 Introduction

IDDQ testing has emerged as an efficient technique for the detection of realistic faults in static CMOS circuits [1]. IDDQ testing has been also accepted by the test community as a complementary methodology to the logic testing in order to achieve a higher fault coverage [2]. Built-in-current (BIC) techniques were proposed to monitor the amount of quiescent current in internal power lines using current sensors introduced into the circuit [3, 4, 5, 6, 7, 8, 9].

In this paper, we present an approach to ISSQ and IDDQ testing design based on the application of BIC sensors to a cell library design methodology [10], and a discussion and experimentation about the effect of circuit partitioning [8, 11, 12, 13, 14].

2 The impact of the technology type

The efficiency of an on-chip current sensor depends on the technology type used to implement the circuit. By technology type we mean whether the technology CMOS used is p-well or n-well.

Due to the fact that in a n-well technology, the p-type substrate is common to the whole IC, and due to the usual design practice to bias locally substrate with the same line used for the source transistors of the logic, the sensing circuit is shunted by the substrate, degrading the behaviour of the sensor. The problem can be solved by using two possible techniques:

- to implement an IDDQ sensor (instead of ISSQ), because due to the possibility to use different n-well zones for circuit and sensor, the shunt effect is avoided;
- to make a special design of the CUT circuit, in such a way that the biasing Vss and the n-mos source electrode Vss be implemented by using different rails.

We can conclude that for a n-well technology, the faster strategy is to place the current sensor in the Vss rail (ISSQ) however this strategy implies the need of a design of the CUT oriented to ISSQ test (independent rail for substrate biasing). To locate the sensor in the VDD rail (IDDQ) implies a simpler design of the CUT, but a slower monitoring. In the case of a p-well technology the faster monitoring corresponds to a location of the sensor in the VDD rail (IDDQ) and the implementation on the Vss rail means the simpler design.

3 ISSQ/IDDQ testable cell-library

In a standard cell-library design the cells are regularly distributed in a set of rows and columns according to the functional interconnections. Then, to achieve IDDQ or ISSQ testable designs, a sensor per row ratio may be considered in order to reduce sensing speed and also minimize the routing area due to interconnections between sensors.

In this work we use two different strategies over a standard cell library (1μm n-well ES2 technology): ISSQ sensor and IDDQ sensor. In each case, we will show the integrator sensor and its behaviour, the different modifications that have to be introduced in the design of the cell library and the main results obtained over a set of five circuits.

Finally, we will compare the area overhead and the test frequency obtained in each strategy.

The main parameters that qualify an on-chip ISSQ/IDDQ implementation are:

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- the voltage drop in VSS or VDD due to ISS/IDD current. This drop occurs when the sensor is in the non-measuring state and usually is due to the sensing element. In any case, $Vdrop_{max}=Rs \cdot ISS_{max}$ ($Vdrop_{max}=RD \cdot IDD_{max}$) where Rs (RD) is the resistance of the sensor and ISS (IDD) is the current consumption of the circuit. The value Rs (RD) is the responsible in a significant way of the area of the sensor and this means that for a given Vdrop, the maximum peak of current consumption deals with the area of the sensor.
- the sensing time, that it is proportional to the parasitic capacitance Cequ of the CUT, and consequently it is dependent on the size of the circuit under test.
- the silicon area overhead due to the sensor implementation.
- the defective current discriminability, that it is the relation between the ISSQ/IDDQ current due to a defect and the fault-free leakage current.

4 ISSQ strategy

4.1 ISSQ current sensor

In this work, we use an integrator sensor, whose structure is shown in Figure 1.

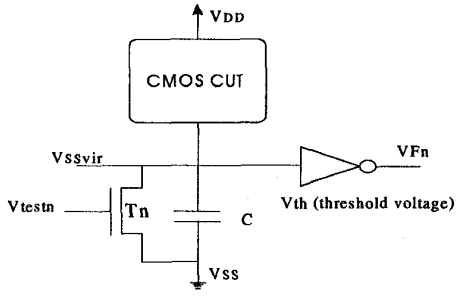

Figure 1: ISSQ integrator current sensor

Its simplicity is obvious because it only needs a pass transistor (to discharge the capacitance after the current measurement) and an inverter which integrates the current [9]. In order to reduce the Vdrop of the supply voltage, we will use a modular design of the sensor (paragraph 4.2). The relation between the capacitor C, the threshold voltage of the inverter and the test frequency will determinate the current level (ISSQ) detectable on the circuit.

To introduce ISSQ testing technique in a cell library, a virtual ground (Vssvir) is added in each cell for current monitoring by the sensor. Both, virtual ground and main ground flow in parallel through the row of cells into the circuit. In consequence, the height of the cell is increased due to the size of the ground lines and the spacing that the grounds must keep between them, due to the design rules. In our case, we have obtained a 14% of area overhead of our cells (1 µm n-well ES2 technology).

4.2 Modular current ISSQ sensor

In a standard cell approach, the size of the rows of a circuit depends on the amount of cells of the circuit. The capacitance (C) associated with the Vssvir layer depends on the length of the cell row. To respond to this fact, we propose a flexible and modular design a of current sensor (modular current sensor, MCS) composed of two parts (Figure 2):

- The inverter module (MINV) is a fixed part, that is designed to obtain a good time of integration
- The module MTN, a pair of discharge transistors, that reset the capacitance associated to Vssvir line after the ISSQ measurement (transistor Tn in Figure 1).

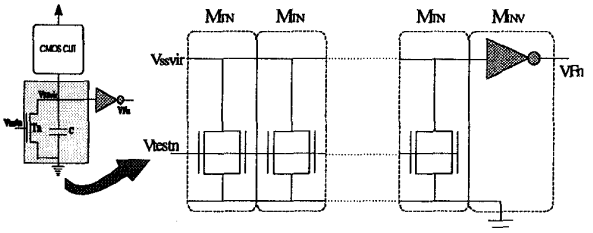

Figure 2: Strategy ISSQ of modular current sensor

The number of this MTN modules depends on the maximum voltage transition peak of the row, where the MCS has to be added, which depends on the number of simultaneous logical transitions.

The input of the inverter is the Vssvir line and the output VFAn is a boolean value corresponding with the detection a fault. All the discharge transistors are controlled externally with the same signal called Vtest.

In order to obtain the optimal relationship between maximum voltage transition peak of the row and the size of the MCS the following relation is obtained:

$$K = \text{number of modules} = ISS \cdot Rs / Vdrop$$

where Rs is the resistance of the module MTN. So, the size S of the modular sensor will be:

$$S = K \cdot S_{MTN} + S_{MINV}$$

where S_{MTN} is the size of the module MTN and S_{MINV} is the size of MINV.

4.3 ISSQ results

In order to obtain the optimal relationship between the length of the row and the size of the MCS, different

lengths of cell rows have been built and in each case, different sizes of MCS has been added. The number of modules MTN is a function dependent on the voltage drop in VSSvir, that occurs during the cell transitions. Our objective has been to maintain that value under 500 mV (around the 10% of the supply voltage value).

To obtain different row sizes we have integrated 5 circuits composed of 1, 2, 4, 8 and 16 full-adders. In these circuits we have included the correspondent MCS.

Table I summarizes the simulated (HSPICE) parameters of each circuit: voltage drop, number of MTN, sensing time (the VFAn response time), and the area overhead. In all of these circuits, a fault of 144µA current injection is introduced by means of a fault-injector cell.

# full-adders	# cells	Vdrop	# MTN used	VFAn sensing time	Area overhead
1 FA	13	436 mV	1	21 ns	35 %
2 FA	26	470 mV	2	38 ns	28 %
4 FA	52	460 mV	5	75 ns	27 %
8 FA	104	450 mV	11	145 ns	26 %
16 FA	208	445 mV	23	295 ns	26 %

Table I: Simulated results with ISSQ strategy.

From the table we can conclude that:

- The number of modules MTN increases linearly with the size of the row.
- The sensing time also increases linearly with the size of the row, and there isn't relation with the number of the MTN.
- For small row lengths, the area overhead is relatively important (due to the fixed part). However, as row lengths increase, area overheads decreases quickly around 26 %.

5 IDDQ strategy

5.1 IDDQ current sensor

In this section, we present the same integrator sensor but designed to be compatible with the IDDQ strategy (Figure 3). In this case, the clock is called Vtestp.

In this strategy, the main disadvantage is the additional capacitance due to n-well, necessary for the transistor P used in the sensor. So, as the sensing time is proportional to the equivalent capacitance, IDDQ sensor responses will be slower than ISSQ sensor responses. In another way, the main advantage is also related to the use of n-well.

However, different n-well zones (for the circuit and for the sensor) are used in order to avoid the shunt effect. If we apply this strategy in a standard cell library, no modification has to be introduced in the library, and sensors are added by adjacency to the cell-rows.

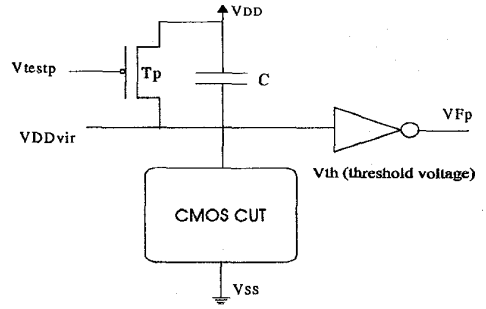

Figure 3: IDDQ integrator current sensor

5.2 Modular current IDDQ sensor

In this strategy, we also use a modular design of a current sensor composed of two parts (Figure 4):

- The inverter module, that is designed to obtain a good time of integration
- The module MTP, a pair of charge transistors, that preset the capacitance associated to VDDVIR line after the IDDQ measurement (transistor Tp in Figure 3).

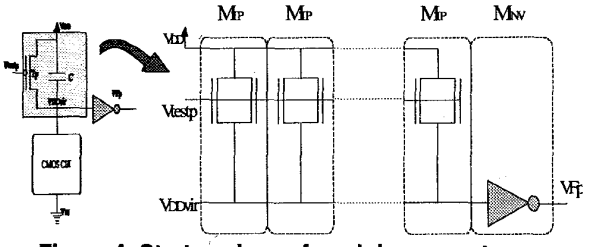

Figure 4: Strategy IDDQ of modular current sensor

5.3 IDDQ results

In order to compare with the results obtained in section 4.3, the circuits integrated are the same full-adders and we summarize the different results obtained for each circuit in table II.

# full-adders	# cells	Vdrop	# MTP used	VFAp sensing time	Area overhead
1 FA	13	495 mV	2	55 ns	36 %
2 FA	26	494 mV	4	90 ns	24 %
4 FA	52	450 mV	9	192 ns	19 %
8 FA	104	440 mV	20	384 ns	17 %
16 FA	208	440 mV	40	730 ns	15 %

Table II: Simulated results with IDDQ strategy.

6 Comparison between ISSQ/IDDQ strategies.

From sections 4.3 and 5.3 we can conclude that time integration using ISSQ sensor is faster than IDDQ sensor (Figure 5) but ISSQ strategy cause bigger area overhead (Figure 6). It is important to emphasize that for a small length of a row, the area overhead is high but it tends towards 26% (in a ISSQ strategy) and 15% (in a IDDQ strategy). On the other hand, IDDQ strategy has the advantage that no modification has to be introduced in the library. This is a great advantage for designers because they do not have to spend any effort in order to redesign the library cells.

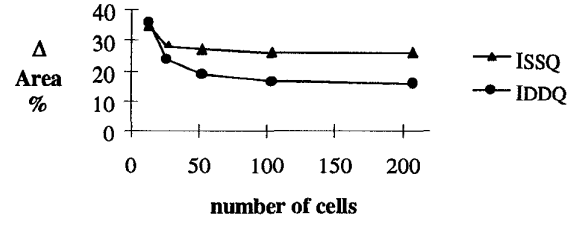

Figure 5: Overhead versus number of cells in ISSQ and IDDQ strategies.

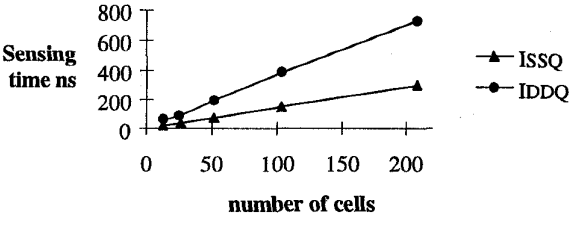

Figure 6: Sensing time versus number of cells in ISSQ and IDDQ strategies.

7 Analysis of the circuit partitioning.

This section deals with how a partitioning technique influences response delays and area overheads parameters of the global circuit. We will apply this technique only to ISSQ strategy because it is faster than IDDQ strategy (when n-well technology is applied).

The main reasons to use circuit partitioning are related with the defective current discriminability (in order to improve this parameter, the solution is to partition the CUT) and also with the capacitance of the CUT. If the CUT is partitioned, each partition will have lower Cequ, and sensing time decreases. This section deals with how a partitioning technique influences response delays and area overheads parameters of the global circuit. We will apply this technique only to ISSQ strategy because it is faster than IDDQ strategy. The range of influence for different partitioning techniques is considered for a set of ISCAS circuits [15].

7.1 Partitioning a circuit: two limit cases

Two aspects have to be taken into account when a partitioning for ISSQ is intended: the size of the partitioning and the partitioning strategy.

The size of the partitioning deals with an increment of area overhead and a reduction of the sensing time (it is important to find an equilibrium between these trade-offs). The partition strategy, this means the selection of gates forming each partition, deals with an increment of overhead but does not affect sensing time in a significant way. From the point of view of sensor overhead, two limit partitioning strategies, can be considered:

- A worst-case, from the point of view of overhead, corresponding to a partitioning strategy of maximum parallelism of gates. That is, maximum parallel switching and relative maximum (Iss)max. So in this case we find the highest overhead.
- A best-case, from the point of view of overhead, corresponding to a partitioning strategy of maximum serial gates. The gates of every partition switch at different time, with minimum parallel switching and minimum (Iss)max. So the sensor area decreases.

For any other partitioning strategy the overhead is bounded by the two previous cases. Figure 7 shows, for C432 ISCAS circuit, the area overhead introduced by ISSQ testing under the assumption of using a sensor like the indicated in section 5.3 and a maximum voltage drop of 250 mV.

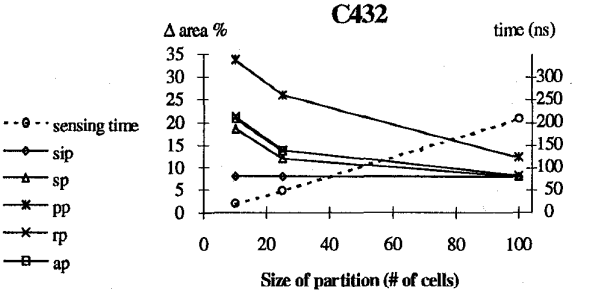

Figure 7: Overhead and sensing time versus size of partition, for different partition strategies (C432).

Figure 7 and 8 shows the results for the area overhead and sensing time using different strategies: single partition (sip), serial partition (sp), parallel partition (pp), random partition (rp) and automatic partition (ap)

strategies. Observe than the results for random and automatic partition (based on commercial placement tool) strategies are nearer to the best-case, this means that the parallel strategy is really a worst limit.

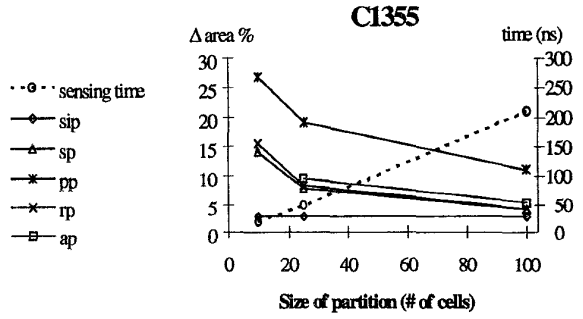

Figure 8: Overhead and sensing time versus size of partition, for different partition strategies (C1355).

Different scenarios have been taken into account: single partition (use of a single sensor for the whole circuit), and partition for 10, 25 and 100 equivalent NOT gates. This analysis has been performed using the ISSQ testable library shown in section 4.2.

This data has to be considered together with the speed of response (Figure 7-8). We can conclude that the sensing time only depends on the size of the partition (Cequ) and it is independent of the partitioning strategy.

8 Conclusions

Rules for on-chip ISSQ/IDDQ rail selection has been presented. When a fast option is selected, using n-well (p-well) technology, it makes sense to consider in a standard cell design style a family of ISSQ (IDDQ) testable cells. If better area overheads have to be obtained, then IDDQ (ISSQ) testable cells should be used. The concept of modular sensor has been introduced. A simple stack of modular cells allows the synthesis of sensor ISSQ/IDDQ adequate for the characteristic of the circuit.

When the circuit is complex a partitioning in ISSQ/IDDQ testable domains can be considered. This technique increases the speed of the current sensing and improves the sensor resolution discriminability required for the circuit. For a given partition size the overhead depends on the law of selection of gates for each partition. This overhead is in-between a margin corresponding to two limit strategies. The margin of area overhead for a set of ISCAS circuits have been calculated.

In the future, these results would be applied to implement automatically multiple partition ISSQ/IDDQ testable circuits by using an oriented placement and routing tool.

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