Received: 16 August 2021 | Revised: 21 September 2021 | Accepted: 11 October 2021

DOI: 10.1049/tje2.12099

The Journal of Engineering

The Institution of Engineering and Technology WILEY

ORIGINAL RESEARCH PAPER

SiC MOSFET switching – Lower losses without increased EMI – A technique to evaluate and achieve this goal

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Funding information
Deutsche Forschungsgemeinschaft; University of Bayreuth

Abstract

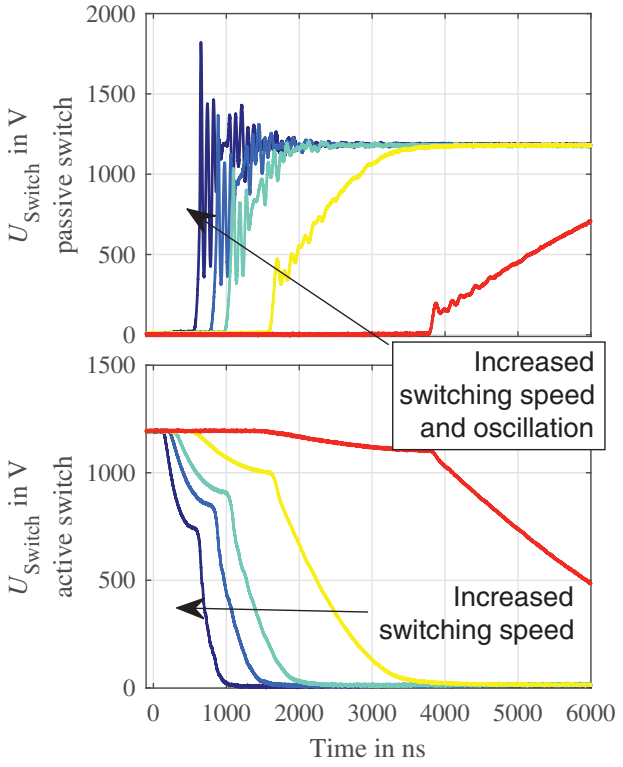
With increasing switching speed of new power semiconductors like the SiC MOSFET, special attention has to be paid on the electromagnetic interference and its limitations. In this work, an evaluation criterion is developed as an optimisation tool for maximum exploitation of conducted electromagnetic interference limit by optimizing the switching process of a SiC MOSFET. The switching losses of power semiconductors can be reduced by increasing their switching speed. Unfortunately, at the same time, the electromagnetic interference will increase due to higher voltage and current slopes and higher switching oscillations. The electromagnetic interference caused by the switching process can be reduced by decreasing the switching speed. This also reduces the switching oscillation but inevitably increases the switching losses. The electromagnetic interference criterion developed in this paper will help to identify the proper switching speed for minimum losses under compliance with switching process related electromagnetic interference. It can be used to evaluate the benefit of more advanced gate control methods that allow increasing the switching speed without increasing the switching oscillation amplitude. The proposed method will not replace the final electromagnetic interference testing, but it will help determine the proper gate control method for lowest possible switching losses without violating the electromagnetic interference restrictions in an early development state. Measurements show that the switching losses can be reduced by 75% with a proper gate control method, where the proposed method assures the compliance with the electromagnetic interference limit.

1 | INTRODUCTION

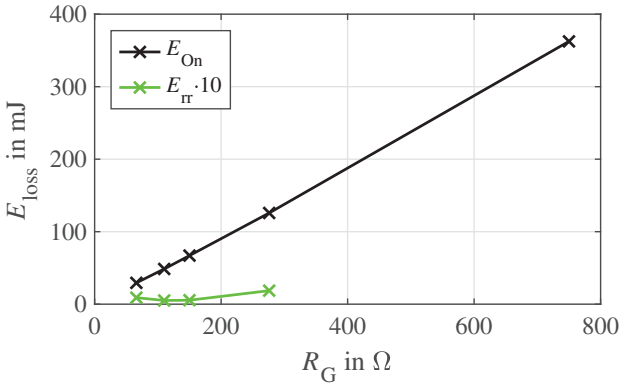
The electromagnetic compatibility (EMC) or electromagnetic interference (EMI) topic is typically handled relatively late in the development process. For clarification, it will be spoken of EMI for the electromagnetic emission to be distinguished from the electromagnetic susceptibility. In the literature, it can be found that the development cost for EMI solving entities will increase with the development state it is implemented in [1].

Addressing the EMI topic from the perspective of adjusting the semiconductor switching process, there is the consent that increasing the slopes of a switching process and the occurrence of oscillations in the switching waveforms deteriorate the EMI [2–5]. In the literature, there are mainly two different approaches to investigate several effects on the EMI. An important tool for EMI investigation is simulation. Some models are developed to simulate the EMI within a given system [4, 6]. These models implement the functional and parasitic elements of the circuit and simulate the EMI that is present at the line impedance stabilisation network (LISN). The investigations mostly simplify the semiconductor's switching waveform to a trapezoidal course with different slopes. Another approach is the investigation of the spectral energy in a given semiconductor switching waveform [7, 8]. The influence of parasitic elements on the switching waveforms and their spectral energy is evaluated. The combination of both is addressed in some publications [5, 9]. The semiconductor switching waveform is inserted in a system simulation model and the spectral energy is evaluated.

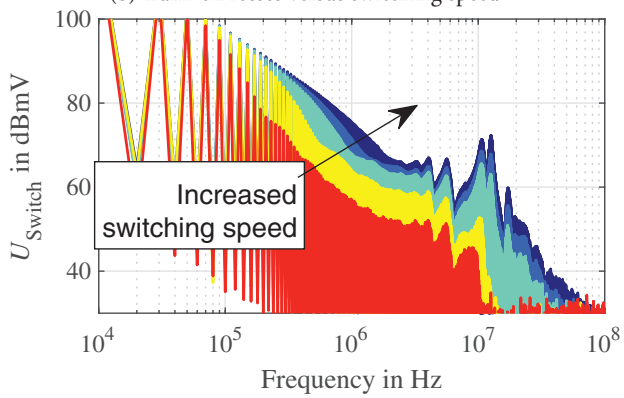
Methods to reduce the EMI always increase the losses or need big and heavy filters. So it is necessary to reduce the EMI as much as needed but to reduce the switching speed as little as



(a) Switching waveforms of SiC MOSFET turn-on process (active switch) and corresponding Body-Diode (passive switch) turn-off process with different switching speed.



(b) Turn-on losses versus switching speed



(c) Passive switch voltage spectral content for different switching speed.

FIGURE 1 Evaluation of the losses (integral, one parameter) and EMI (spectral content, frequency dependent waveform) in terms of switching speed

possible. Publications can be found that investigate the effect of several switching parameters on the spectral amplitudes of the semiconductor switching waveform [10]. Others identify several propagation paths from the semiconductor to the LISN [11]. Methods of switching process control to reduce the EMI are addressed in [12, 13].

One important task to be treated by the EMI simulation model is to determine the lowest possible switching losses while maintaining the accordance with EMI limitations. To the author's knowledge, there is no publication inspecting this topic. In this paper, a method is proposed to investigate the switching process of a semiconductor in the well-known double pulse test and simultaneously evaluate the violation of an EMI limit. With this proposed method, it is possible to minimise the semiconductor switching losses without deteriorating the EMI emission.

In [13], an active gate drive method is proposed that is capable of reducing the voltage and current oscillations that arise in the switching process and increase the voltage slope at the same time. The method proposed in the present paper will evaluate the highest permitted oscillation and voltage slope to maintain compliance with an exemplary EMI limit. Utilizing the highest permissible values for these parameters will ensure the lowest achievable switching losses.

Figure 1 shows the turn-on switching process for the SiC MOSFET as active switch and the body-diode turn-off process

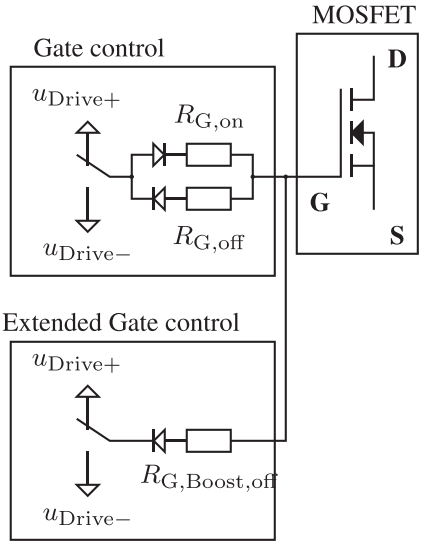


FIGURE 2 Schematic depiction of simple gate resistor controlled gate driver. The 'Extended Gate Control' refers to an additional turn-off switching optimisation according to [13]

of the complementary device in a half bridge as passive switch. The switching process is based on a typical simple gate control with a gate resistor that controls the switching speed (see Figure 2). In the implementation, two resistors are used for indi-

vidual setup for the turn-on and turn-off process. The switching process that is shown is based on a high power application for railway traction purposes. The precise operating conditions can be found in [14]. One peculiarity of the application's switching conditions is a high product of switched current and commutation cell stray inductance. The nominal current of a full module is 2000 A and the stray inductance in the application is 50 nH. In Figure 1(a), the time signals of the turn-on measurements performed with different values for the gate resistance are shown. It can be seen that the active switch does not have a voltage oscillation in the switching process. In contrast, the passive switch (the SiC MOSFET body-diode) shows a very high voltage oscillation at high switching speed. The voltage gradient of the passive switch increases simultaneously with the oscillation in this typical example.

Figure 1(b) shows the influence of the switching speed (expressed by the used gate resistor) on the switching losses. The figure shows that a comparative evaluation of the losses is easily implemented with the total energy loss. The complete time signal can be narrowed down to one comparative parameter that allows an easy performance comparison for different gate control methods. Figure 1(c) shows the spectral content of the passive switch voltage signal. This is a typical representation that can be found in several publications dealing with the effect of a switching process on the EMI of an application.

From the mathematical investigation of ideal trapezoidal signals, it is known that an increased gradient will also increase its spectral content for high frequencies [15]. On the other hand, an oscillation causes an increase of the signal's spectral energy at the specific oscillation frequency. Although an increased voltage gradient of a switching process is preferable for the switching loss reduction [16], the switching oscillation increases as an unintended side-effect. Considering EMI limitations, a superior gate control method should therefore manage to increase the voltage slope of a switching process and mitigate the switching oscillations at the same time.

In contrast to the integral evaluation of the switching losses, there is no such comparison method for the evaluation of different switching waveforms in terms of EMI. Such an evaluation method would be desirable to evaluate the performance benefit for several gate control methods.

With the method developed in this paper, it will be possible to compare several switching processes in terms of EMI by one comparative parameter and point out the best switching losses in compliance with the EMI regulation. The parameter will show a margin to the chosen EMI limit. This will enable the user to conduct a comparative margin evaluation.

The present work is organised as follows. In Section 2, the calculation of the spectral content of a measured switching signal is described.

In Section 3, the development of the comparative margin EMI criterion is discussed. The criterion has to be adjusted for the relevant application. In this work, a simple implementation serves as example to demonstrate the usage of the proposed comparison criterion. The simulation model included in this section is kept radically fundamental without a claim to be complete.

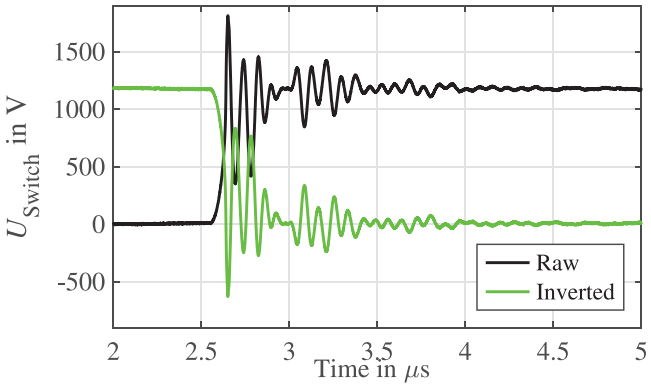


FIGURE 3 Raw and inverted time signals of an exemplary switching waveform. The inverted signal is used to prepare the calculation of the spectral content via the FFT

The developed EMI criterion is used in Section 4 to evaluate the optimisation of the turn-off process of a SiC MOSFET with an advanced gate control method called 'boost-method'. The method presented in [13] uses a switchable gate resistance to optimise the turn-on and turn-off switching process. A time duration is defined, where a low gate resistance, the so-called boost resistor, is active. After this time duration (within the same switching process), the boost resistor is deactivated and the switching process is slowed down. With this method, the switching process can be accelerated and the oscillation can be reduced at the same time. The schematic implementation of this method is shown in Figure 2 as combination of the 'Gate control' and the 'Extended Gate control' element.

In Section 5, the development and the utilisation of the proposed EMI criterion is discussed. The benefits of the criterion are outlined.

Section 6 gives a short summary and finishes the work.

2 | SPECTRAL CONTENT OF A SWITCHING PROCESS

When dealing with the topic EMI, there is no way around the mathematical description of the spectral content of a given time signal. This mathematical process, however, is treated very well in many academic publications and textbooks [15, 17]. For numerical signals, the transformation in the frequency domain is typically performed via the Fast Fourier Transformation (FFT).

Even though the FFT method is discussed very well in literature, there are some precautions to be taken to properly calculate the spectral content of a switching waveform. In this work, the EMI spectral content of one particular switching process is to be analyzed. The waveforms are measured in the commonly known double pulse test. The fastest switching waveform shown in Figure 1 is used to demonstrate the signal preparation to calculate the spectral content via the FFT.

Figure 3 shows the measured (Raw) and an inverted switching voltage signal from the body diode (passive switch) switching process. The DC link voltage in this example is set to 1200 V. The inverted signal is generated from the raw signal via

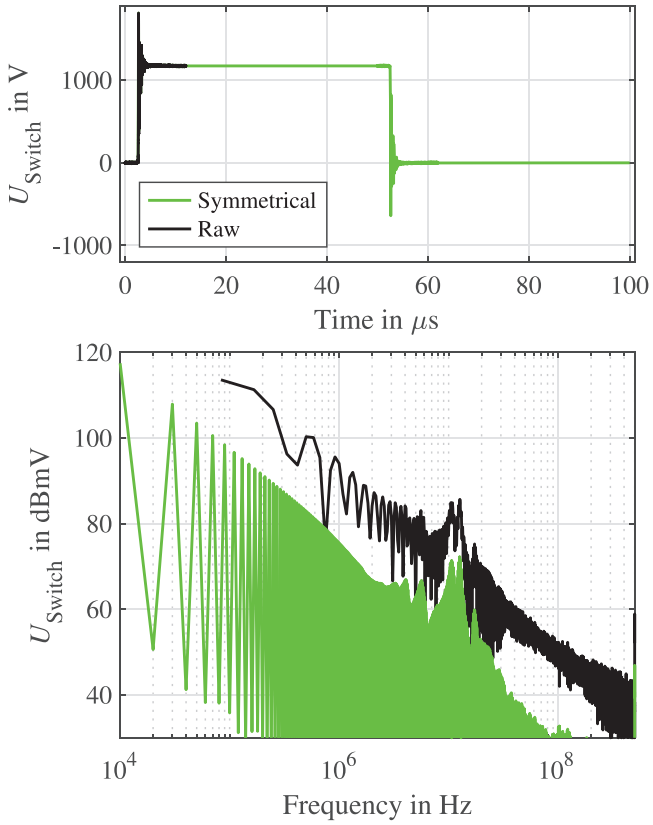


FIGURE 4 Spectral content of switching voltage. The double pulse test measurement signal (Raw) is prepared to derive a proper spectral content via FFT (Symmetrical). The upper diagram shows the signals in time domain. The bottom diagram shows the signals in frequency domain

Equation (1).

$$u_{\text{Switch,Inverted}} = U_{\text{DC}} - u_{\text{Switch,Raw}} \tag{1}$$

The inverted signal is necessary to properly calculate the spectral content of the switching waveform. In Figure 4, the spectral content of the prepared signals is shown. The raw signal and its spectral content is inserted to demonstrate the necessity of a proper signal preparation to calculate the FFT. Both signals show the same transient signal, but the spectral content significantly diverges between both signals. This evaluation shows that for the comparison of the spectral content of different switching processes, these signals have to be prepared properly and, most importantly, equally prior to the transformation in the frequency domain via the FFT.

For the preparation of the symmetrical signal, the raw waveform is inverted as it is demonstrated in Figure 3. Subsequently, the inverted signal is placed at the end of the raw signal. The signal is extended to the time duration of one period of the considered switching frequency. In this case, the switching frequency is set to 10 kHz. With a proper signal extension, the modulation index of the signal is set to 50%. The FFT executed for the properly prepared signal gives the relevant spectral content of the specific switching process.

3 | EMI COMPARATIVE MARGIN CRITERION FOR SWITCHING PROCESS EVALUATION

The spectral content calculated by FFT from the semiconductor switching waveform cannot be compared with the limit given by the application's applicable standard. Standards like the IEC 61000-3 for industrial devices operated at public grid or the CISPR standard for vehicles, components and industrial devices limit the spectral emission that is measured at an LISN [18]. The EMI test is conducted with the complete system at the end of the development process. In this section, a tool is discussed that allows the evaluation of the switching process in terms of EMI with a comparative margin evaluation.

The EMI criterion developed in this paper aims to simplify the communication process between the top level system design and the low level semiconductor switching process control design. In conventional EMI treatment, a time-consuming iteration is necessary for optimal exploitation of the switching process in terms of EMI. With the proposed EMI criterion, the communication between system design and semiconductor switching control design will be simplified and standardised. This enables a fast evaluation of the switching process in terms of EMI and therefore an optimisation of the switching process for low switching losses while maintaining EMI compliance.

3.1 | Simplified system simulation with trapezoidal waveforms

The proposed comparison criterion is based on a simplified system simulation. The propagation path from the noise source (the semiconductor switching process) to the noise sink (the measurement port of the LISN) has to be considered when dealing with the EMI issue.

As a simplification, especially by separation of the switching process optimisation and the system level engineering, the proposed method uses simple trapezoidal waveforms for the system simulation. With this simplification, the system simulation can be conducted totally independent from the switching process optimisation.

Figure 5 shows an exemplary schematic for the system simulation. Using a simulation model with higher details than the exemplary, one will increase the precision of the switching process optimisation. However, the method is proposed to simplify the EMI treatment. It is assumed that even with a low-quality system simulation the proposed method will enable a qualitative switching process evaluation in regard to EMI. Furthermore, the present work aims to develop the tool for a proper link between the system simulation and the semiconductor switching optimisation and therefore does not treat the system simulation in detail.

A simple implementation of the system simulation is shown in Figure 6. The model does not claim to be complete. For example, there are no filters inserted in the model. The parasitic coupling capacitors are estimates. The model is used to

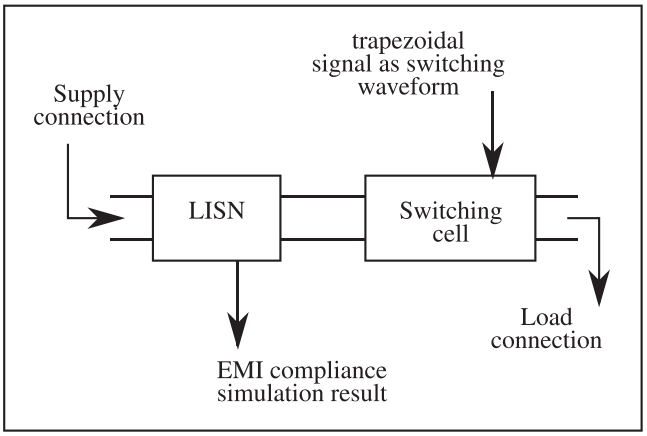


FIGURE 5 Exemplary schematic of a system simulation

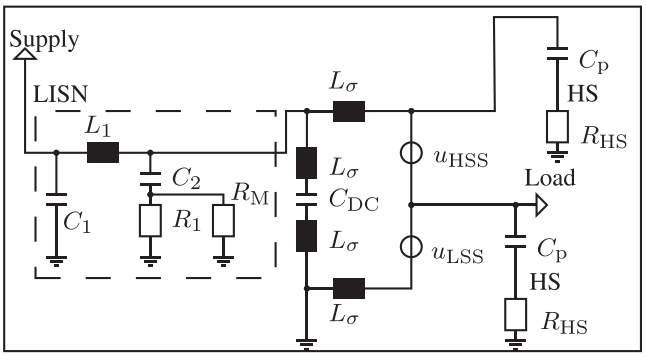


FIGURE 6 Exemplary implementation of a system simulation. The connection 'HS' indicates the heat sink connection. The simulation does not claim to be complete or representative. The values used in the simulation are given in Table 1

clarify the implementation of the EMI criterion. The 50 µH LISN is typical for many conducted EMI measurements. The LISN schematic and the applicable values can be found in [1, 18].

Table 1 shows the parameters that are used for the elements of the system simulation. For the stray inductance L_σ, a total value of 48 nH is adopted for a high power traction application (see [14]). The value is distributed equally in the switching cell to the DC-link capacitor connection and the common path from the supply to the semiconductor. The values for the parasitic capacitance C_p and the damping resistor R_{HS} (which

TABLE 1 Parameter values used in the simulation model in Figure 6. The parameters du/dt, U_{DC} and f_{SW} define the trapezoidal signals u_{HSS} and u_{LSS}

Parameter	C_1	C_2	R_1	R_M
Value	1 µF	100 nF	1 kΩ	50 Ω
Parameter	L_1	L_σ	C_p	R_{HS}
Value	50 µH	12 nH	10 nF	2 Ω
Parameter	du/dt	U_{DC}	f_{SW}	
Value	10 V/ns	1200 V	10 kHz	

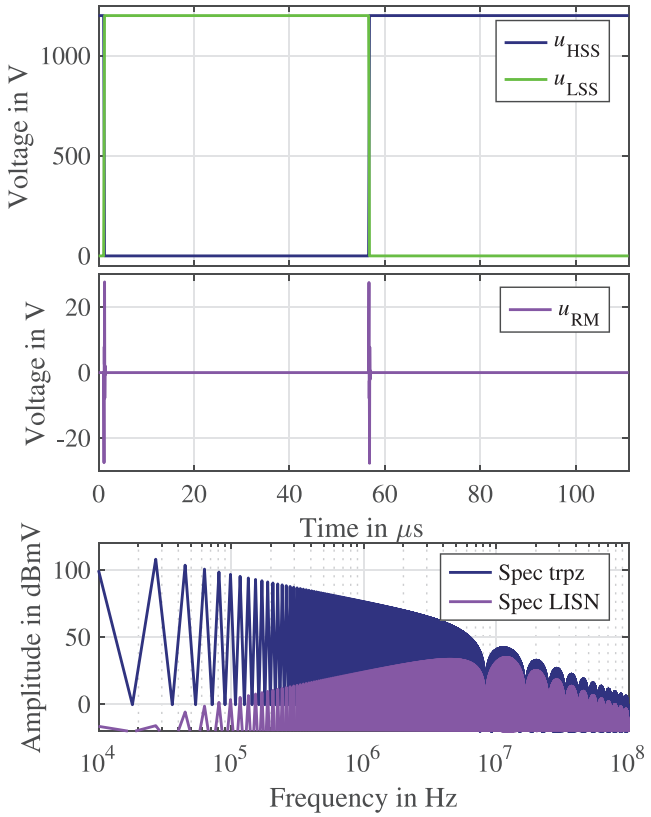


FIGURE 7 System simulation result

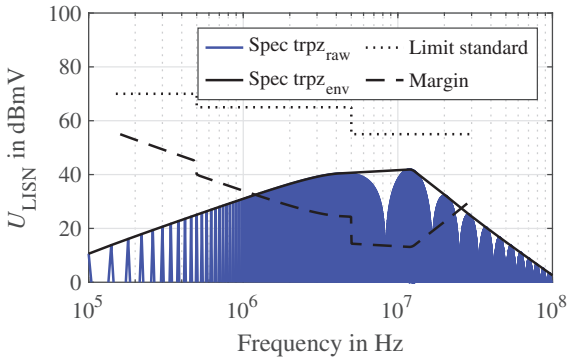
is the electrical resistance of the grounded heat sink connection) are estimated. Of course, in a real application, the parasitic elements are highly complex. However, it is not the scope of this investigation to generate a realistic simulation model but to develop a method for the EMI consideration in the semiconductor switching process optimisation.

Figure 7 shows exemplary results with the simulation model given in Figure 6. Simplified trapezoidal switching waveforms are fed in the simulation, where u_{HSS} and u_{LSS} are inverted to each other (similar to Equation 1). The signals are shown in dark blue and light green lines in the upper diagram. The signal evaluated at the LISN is the voltage u_{RM} or u_{LISN} measured at the measurement resistance R_M. It is drawn in the middle diagram. Via the FFT, the voltage is transformed in the frequency domain representing the spectral content of the electromagnetic emission. The spectral content is shown in the lower diagram as FFT from u_{HSS} (= Spec trpz) and from u_{RM} (= Spec LISN).

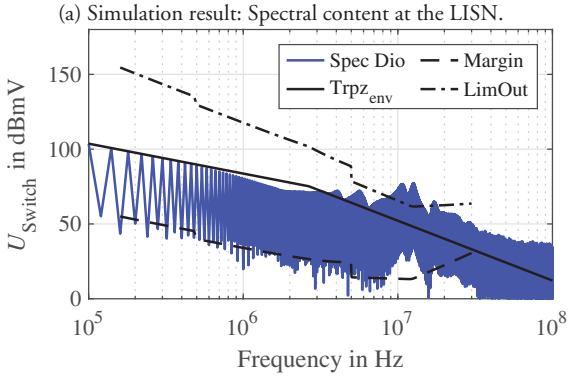
3.2 | Reference signal for the switching process spectral comparison

As result of the simulation, the spectral content of the signal simulated at the LISN can be compared with the applicable standard. Figure 8 shows the signals used to develop the EMI criterion based on simulation results.

The solid blue line 'Spec $trpz_{raw}$' in Figure 8(a) shows the spectral content of the voltage waveform u_{RM} simulated at the



(a) Simulation result: Spectral content at the LISN.



(b) Calculated results without influence of the LISN or propagation path from the source of switching noise to the measurement unit. The figure explains the derivation of the comparison limit "LimOut".

FIGURE 8 Development of the EMI criterion. The index 'env' indicates the envelope of the spectral content. As 'Limit standard', an exemplary value is chosen. For a quantitative comparison, the simulation model has to be strengthened and the limit from the applicable standard has to be used here

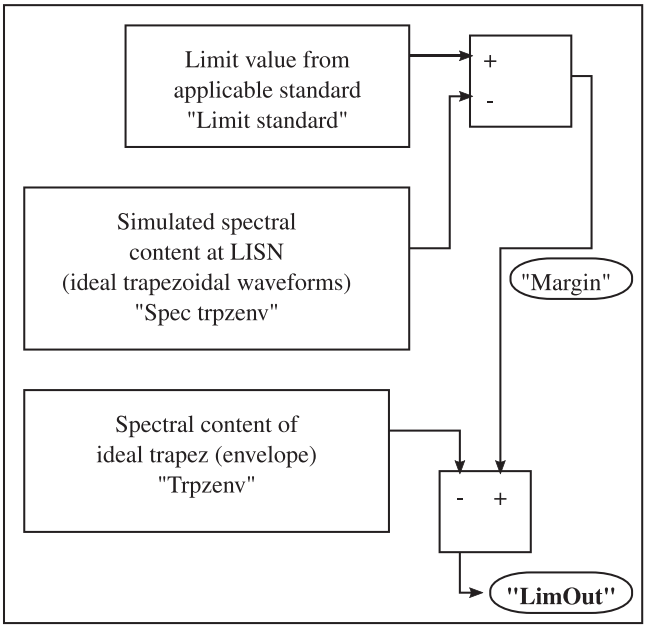


FIGURE 9 Schematic depiction of the calculation process for the signal 'LimOut'. The signals used for the calculation are shown in Figure 8

TABLE 2 Definition for evaluated diode switching waveforms

Label	R_G	Δ dB	E_{On}
Dio A	78 Ω	+15.6	15.6 mJ
Dio B	150 Ω	+7.4	67.0 mJ
Dio C	210 Ω	−0.5	94.5 mJ
Dio D	380 Ω	−9.1	175.5 mJ

LISN. As a typical course for short time signal transformation, the signal shows a strong saw tooth character. For the calculation of a generally applicable Limit, the envelope of the signal has to be calculated. The calculated envelope is shown as 'Spec Env_{trpz}'. With this envelope and the signal "Limit standard", the remaining margin between ideal trapezoidal switching waveform and the EMI limit 'Margin' can be calculated with Equation (2).

$$\text{Margin}(f) = \text{Limit standard}(f) - \text{Spec trpz}(f). \quad (2)$$

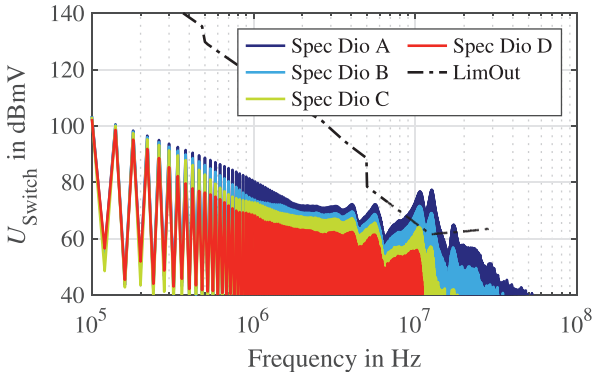
Figure 8(b) demonstrates the calculation of the reference signal 'LimOut' that is necessary for the proposed EMI criterion. The black line '$Trpz_{env}$' shows the envelope spectrum of an ideal trapezoidal signal. The amplitude and switching gradient have to be equivalent to the trapezoidal signal that is used in Figure 8(a) to derive the EMI level at the LISN. The margin, calculated in Figure 8(a) is added to the idealised trapezoidal signal spectrum to generate the applicable comparison criterion LimOut, see Equation (3). As an example, the spectral content of a diode switching waveform signal 'Spec Dio' is added in Figure 8(b).

$$\text{LimOut}(f) = \text{Trpz}_{\text{env}}(f) + \text{Margin}(f). \quad (3)$$

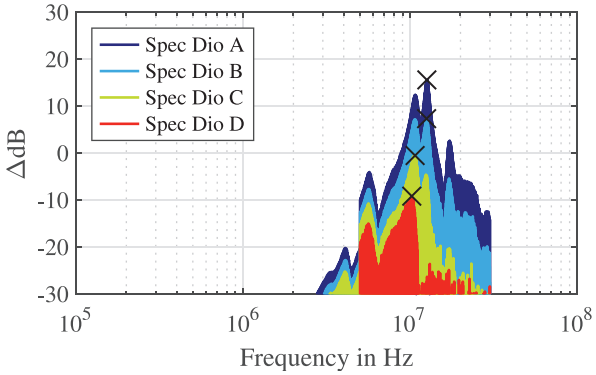
Figure 9 shows a flowchart of the calculation of the signal 'LimOut' that is developed as comparison benchmark in this work.

With the developed EMI limit 'LimOut', the spectral content of the switching process can be compared with the exemplarily chosen limit 'Limit standard'. The standard typically gives a limit for the spectral content measured at the LISN. This cannot be applied directly to the spectral content of the switching waveform that is calculated by the FFT.

Figure 10 shows an exemplary use case of the EMI criterion. For turn-on switching process, the voltage waveform of the complementary body diode is evaluated with different gate resistance values. Table 2 gives an overview over the measurement parameters and specifies the used labels 'Dio A' to 'Dio D'. Figure 10(a) shows the spectral content of different diode switching waveforms as it is calculated in Section 2. The EMI limit is also shown in the diagram. It can be seen that for lower frequency, the switching waveform spectral content by far does not reach the calculated limit. For fast switching process, the diode switching voltage shows an oscillation at approximately 10 MHz (see Figure 1a). At this frequency, the diode voltage spectral contents 'Dio A' and 'Dio B' exceed the



(a) Diode switching waveform spectral content and reference signal LimOut.



(b) Margin between switching signal spectral content and derived reference signal "LimOut". The cross marker indicate the margin's maximum which is the proposed EMI criterion.

FIGURE 10 Determining the optimum switching speed for turn-on process by using the EMI criterion

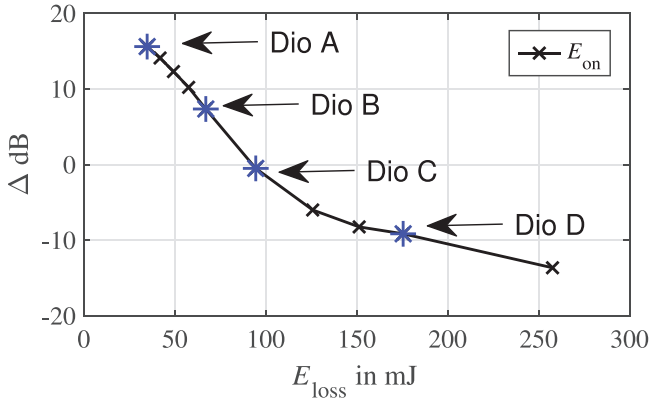


FIGURE 11 Comparative margin evaluation of turn-on losses and developed EMI criterion

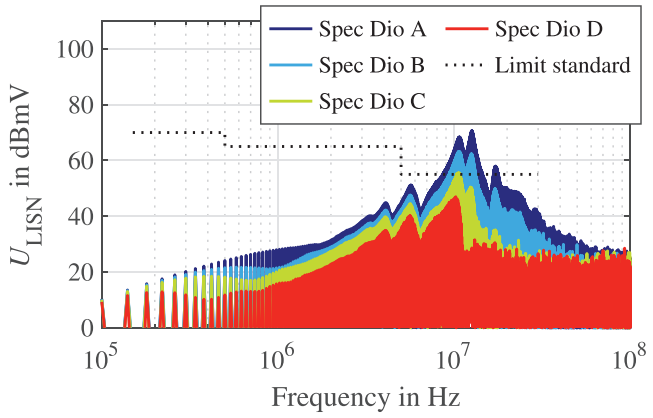


FIGURE 12 Spectral content at the LISN simulated with diode voltage signals. The result verifies the proposed EMI criterion

EMI limit. This representation still does not allow a comparative evaluation of the EMI content with a single value.

Figure 10(b) shows the difference of the switching process' spectral content and the signal LimOut. The unit is referred to as ΔdB. Each value of ΔdB that exceeds 0 means the switching process violates the exemplary chosen EMI limit. Furthermore, the magnitude of the violation can be given by one single, comparative value. Equation (4) gives the mathematical representation for the single value evaluation, which is the maximum of the difference between the signal LimOut and the spectral content of the specific switching waveform, shown by the black cross markers per waveform.

$$\Delta\text{dB} = \max\left(\text{Spec Dio} - \text{LimOut}\right). \tag{4}$$

This comparative margin value as EMI criterion allows an easy comparison for different switching processes and even for different gate control strategies. Figure 11 shows the comparative margin value in respect to the active switch's turn-on switching losses. The diagram shows that the lowest switching losses that can be reached without violation of the EMI criterion is $E_{\text{on}} = 94.5$ mJ. Further increase of the gate resistance will increase the switching losses, while a decrease of the resistance will lead to violation of the EMI criterion. The blue star markers highlight the switching processes that are shown in Table 2.

3.3 | Validity evaluation with system simulation

By using the developed criterion, it can be seen from Figures 10(b) and 11 that the optimal switching is achieved with configuration 'Dio C'. The switching process with this setup has the lowest switching losses while still maintaining compliance with the EMI limit. To evaluate the validity of the proposed method, the diode waveforms described in Table 2 are fed into the system simulation given in Figure 6. The spectral content measured at the LISN for the four signals is shown in Figure 12.

The diagram shows that the simulated LISN spectral content for signal 'Dio C' is in compliance with the standard EMI limit. However, at approximately 10 MHz, the limit is completely exploited. This result verifies the validity of the proposed EMI criterion.

For further comparison in this exemplary application, no additional system simulation has to be conducted. Every

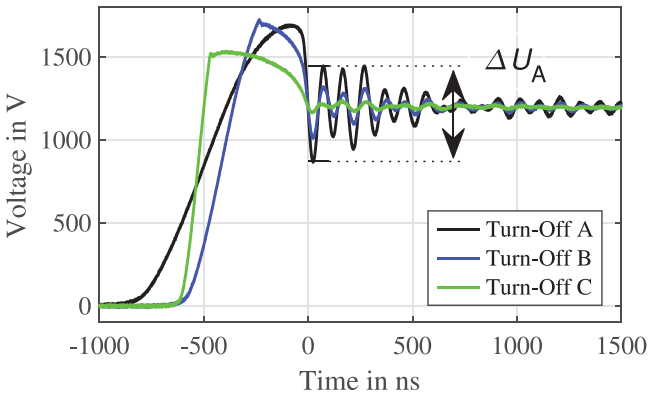


FIGURE 13 SiC MOSFET turn-off process with boost-method gate control. The switching process is scaled to high power module application. Table 3 gives a description for the different switching waveforms. The oscillation amplitude ΔU is exemplarily shown for Turn-Off A waveform as ΔU_A

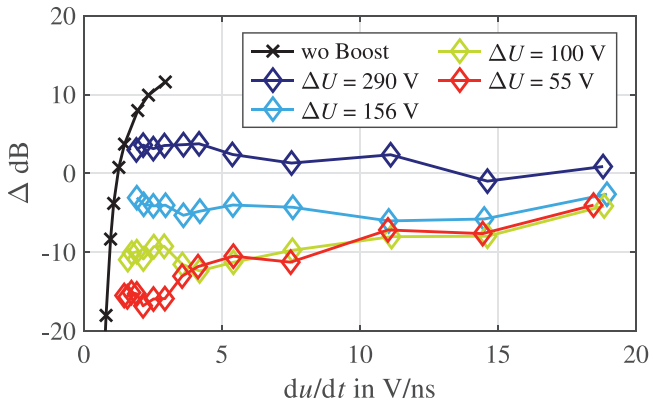


FIGURE 14 Margin evaluation of voltage slope versus EMI criterion. Different gate control settings are compared to derive low losses while maintaining compliance with the EMI standard limit

TABLE 3 Definition for evaluated turn-off switching waveforms

Label	Description
Turn-Off A	Without boost-method—low du/dt and high oscillation
Turn-Off B	Medium du/dt and medium oscillation
Turn-Off C	High du/dt and low oscillation

switching waveform to be investigated can be compared with the derived signal 'LimOut'.

4 | EMI COMPLIANT SWITCHING PROCESS OPTIMIZATION

Reducing the gate resistance for a SiC MOSFET switching process simultaneously increases the voltage slope and the oscillation. In Figure 10(b), it can be seen that the spectral content at the oscillation frequency of the semiconductor switching process shows the critical value in terms of EMI compliance. In literature, several gate control methods are investigated that allow the reduction of SiC MOSFET switching oscillation [12, 13, 19]. The proposed EMI criterion facilitates the performance evaluation and comparison between different gate control strategies. The boost-method proposed in [13] is a promising method to reduce the turn-off switching oscillation amplitude without increasing the switching losses. Using this active gate driver allows a separate adjustment of the voltage gradient and the switching oscillation magnitude. The developed EMI criterion allows the determination of an optimal combination of both these parameters realizing lowest possible losses while maintaining the EMI limit.

The boost-method itself is already presented in [13]. As it is a promising technique to adjust the switching process, it is used to demonstrate the advantage of the developed EMI criterion.

Figure 13 shows three different voltage waveforms of the SiC MOSFET turn-off switching process. Table 3 gives a short description of the switching conditions of the turn-off waveforms. 'Turn-Off A' is derived without the boost-method. As it can be seen, the maximum transient turn-off voltage completely exploits the semiconductor maximum blocking voltage of 1700 V. A further reduction of the gate resistance without separate measures would lead to a harmful electrical stress to the semiconductor.

The waveforms 'Turn-Off B' and 'Turn-Off C' are derived with the boost-method gate control presented in [13]. In Figure 2, the 'extended gate control' shows the hardware setup used for the turn-off boost-method. Figure 13 shows that with this method it is possible to adjust the voltage slope and the oscillation amplitude of the switching process independently from each other. The figure additionally shows a definition of an oscillation amplitude ΔU. This parameter is used as simple value to quantify the turn-off oscillation amplitude. With a proper setting of the boost-method, it is possible to adjust this amplitude to a desired value.

The proposed EMI criterion discussed in this paper is used to evaluate an optimal setting for lowest switching losses while maintaining the accordance with the EMI limit. For this investigation, the voltage slope du/dt and the oscillation amplitude ΔU are adjusted separately via the boost-method. The results are compared with the simple resistor controlled gate control.

Figure 14 shows the comparative margin evaluation of the voltage slope for several measurements with different gate control setups. For the simple gate resistor controlled switching, the voltage slope and the switching oscillation are linked. With the boost-method, these parameters can be decoupled. For $\Delta U =$ 290 V and 156 V, the EMI criterion is relatively constant with the voltage slope. This indicates that the relatively high oscillation dominates the spectral content of the switching process. With $\Delta U =$ 290 V, the spectral amplitude exceeds the standard limit. For $\Delta U =$ 100 V and 55 V, there is a plateau for voltage slopes lower than 3 V/ns. For higher values, the EMI criterion is equal for both curves which means that in this region the EMI criterion is dominated by the voltage slope and not by the oscillation.

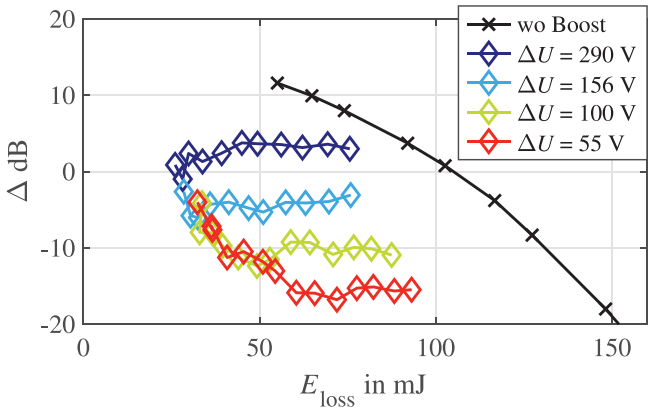


FIGURE 15 Comparative margin evaluation of switching losses versus EMI criterion. Different gate control settings are compared to derive low losses while maintaining compliance with the EMI standard limit

The goal of the EMI criterion is to provide a tool to determine an optimal setup for the switching process giving low switching losses and EMI compliance at the same time. In Figure 15, the EMI criterion is drawn in respect to the switching losses for the same measurements as in Figure 14. The gate resistor controlled measurement with lowest switching losses maintaining the EMI standard limit has turn-off losses of approximately 120 mJ. With the boost-method the switching losses can be reduced to 30 mJ. This value can be reached with different settings. Switching with high du/dt and low oscillation (red line, ΔU=55 V) causes equivalent losses as switching with comparably higher oscillation but reduced du/dt. In Figure 15, two aspects are covered. The lowest possible switching loss while maintaining the EMI criterion can be found to be approximately 30 mJ. Furthermore, the diagram shows that for the losses it is indifferent if the EMI criterion is matched by reducing the oscillation amplitude while maintaining high du/dt or by reducing the du/dt while maintaining the oscillation amplitude.

The lowest possible switching losses under the given boundary conditions can be read in Figure 15. The diagram also shows that there is no trade-off between the voltage slope and the oscillation amplitude. With the proper setting, for each limited oscillation amplitude ΔU = 55 V to ΔU = 156 V, there is a setup to reach the low losses. However, it might be advantageous for handling purposes to have a switching process with lower voltage slope which maintains the same losses as a switching process with higher voltage slope.

5 | DISCUSSION

In this work, a newly developed semiconductor switching process criterion is discussed that allows a one parameter evaluation for EMI compliance. The so-called EMI criterion allows a comparative margin evaluation of the EMI spectral amplitude of a semiconductor switching process. With this criterion, the complex frequency dependent electromagnetic emission can be narrowed down to one single comparative value. The parameter is developed as a tool to include the complex topic of electromagnetic interference in an early stage of development. It is possible to optimise the switching process based on double pulse measurements and even to evaluate the benefit of active gate driving techniques in terms of switching loss reduction without violating the EMI.

The EMI criterion is based on a system simulation which simulates the conducted electromagnetic emission of a given system at a line impedance stabilisation network. Simple trapezoidal waveforms can be used for the switching process in the simulation. The difference of the applicable EMI limit and the results of the simulation serve as basis for the EMI criterion.

The EMI criterion enables a comparative margin evaluation and allows a direct comparison of different switching processes in terms of EMI. With this tool, several gate control mechanisms can be compared and the optimum control strategy can be identified leading to low losses while maintaining compliance with EMI limits.

The developed criterion is used to optimise the turn-off switching process of a SiC MOSFET in a high power application. The result of this optimisation shows the benefit of the propose method. The turn-off losses can be reduced by 75% with the application of the so called boost-method in comparison with simple gate resistor controlled switching. In the comparison, both methods exploit the EMI limit.

6 | CONCLUSION

The developed EMI criterion can be used for the semiconductor switching process optimisation. It gives a one parameter evaluation to compare the EMI caused by the switching process with its switching losses. With a proper system simulation model, it is possible to evaluate the lowest switching losses achievable while maintaining the EMI compliance given by the applicable standard. Furthermore, the criterion can be used to compare sophisticated gate driving methods in terms of the resulting switching loss reduction and their influence on the EMI caused by the optimised switching process.

ACKNOWLEDGEMENTS

The authors would like to thank Dr.-Ing D. Domes and Dr.-Ing F.-J. Niedernostheide from Infineon AG for many fruitful discussions and their feedback to this work. This publication was funded by the German Research Foundation (DFG) and the University of Bayreuth in the funding programme Open Access Publishing.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

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How to cite this article: Maier, R.W., Bakran, M.-M.: SiC MOSFET switching – Lower losses without increased EMI – A technique to evaluate and achieve this goal. J. Eng. 2022, 76–85 (2022). https://doi.org/10.1049/tje2.12099