Gate-Tunable Superconductivity

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To my family.

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1 Introduction

"Kurz zusammengefaßt kann ich die ganze Tat als einen Akt der Verzweiflung bezeichnen. Denn von Natur bin ich friedlich und bedenklichen Abenteuern abgeneigt. [...] Im übrigen war ich zu jedem Opfer an meinen bisherigen physikalischen Überzeugungen bereit."

Max Planck (1858-1947)
on introducing quantization as an act of despair

Thirty years ago, the processor of a typical desktop computer featured $\sim 3 \cdot 10^6$ transistors[1], ten thousand times less than the transistor count on a modern CPU[2]. If a global pandemic had hit the world during that time, video conference calls and working from home would have hardly been possible. The digital revolution impacts all aspects of the modern world and was enabled mainly by the tremendous achievements in miniaturizing integrated circuits, famously predicted by Gordon Moore in 1965 [1]. Ever since, the end of the exponential growth of circuit complexity has been anticipated, but the development of new manufacturing tools, techniques and materials [2] has allowed this exponential trend to continue. While a fundamental limit to the downscaling of transistors appears to be the atomic limit [3], recent accomplishments in vertical design and 3D integration [4] will likely enable continued miniaturization for many years to come.

Despite the rapid increase in compute power enabled by these advancements, certain computational problems are intrinsically hard to solve on classical computers and would require excessive computing time and energy even on future machines [5, 6]. This barrier has fueled the quest for specialized hardware, such as on-chip AI accelerators[3], and the release of the first commercially available quantum computer[4]. While today's quantum computers cannot yet outperform their classical counterparts in practical computing tasks, in the future they are expected to enable speedup in several areas, e.g. factoring of large numbers [7], in chemistry [8] for the development of new drugs and vaccines, and in materials science [9] for next-generation batteries with high energy density.
The promise of the quantum era incentivizes big technology companies like IBM, Google, Intel, and Microsoft to work towards large-scale, universal quantum computers. The

[1] Intel Pentium
[2] Apple M1 Pro
[3] e.g. IBM z16
[4] IBM Quantum System One

most mature solid state qubit platform to date is based on superconducting transmons [10], but other qubit types like spin qubits and topologically protected qubits might prove advantageous in the future due to their compatibility with established manufacturing techniques and relaxed temperature constraints (spin qubits) [11], or long expected coherence times (topological qubits) [12]. Despite the fundamental differences between these approaches, building a large-scale quantum computer capable of solving real-world problems is a challenging task on all platforms and has not yet been achieved [13].
In this context, two main challenges are evident. First, scaling the number of qubits requires exceptional fabrication control [14] with much narrower margins for imperfections than in transistor fabrication for classical processors. Even small perturbations like coupling to random two-level systems [15] or to nuclear spins [16] are sources of decoherence for the fragile quantum states in superconducting qubits and spin qubits, respectively. This makes reliable and reproducible qubit manufacturing a complicated undertaking. A class of qubits that might overcome such challenges are topological qubits [17] which are expected to be protected against local perturbations, but an experimental demonstration of a single qubit is still lacking.
The second main obstacle towards practical quantum computers is the scaling of the infrastructure around a quantum processor, which requires the development of new components like cryogenic switches and amplifiers for a closely integrated quantum-classical interface at cryogenic temperatures. While important milestones in this direction have been achieved [18], compatibility with operation at mK temperatures and monolithic integration for true scalability are still missing. Reaching these goals will likely require novel manufacturing techniques, beyond the capabilities of silicon complementary metal-oxide-semiconductor (Si-CMOS) fabrication.

The work presented in this thesis was performed in the alternative qubits group at IBM Research Europe - Zurich. This group was newly established at the start of this thesis and therefore we explored a plethora of projects that could advance quantum technologies and help address the challenges outlined above, instead of limiting our focus to a single material or device platform. Three of these projects are presented in the following.
In **chapter 2** we review important concepts which are fundamental for understanding the subsequent results. Our discussion ranges from BCS theory and quasiparticle disequilibrium in superconductors to hybrid superconductor-semiconductor interfaces, templated semiconductor epitaxy and the Aharonov-Bohm effect. **Chapter 3** introduces the various fabrication methods used in this work, with special focus on patterning of superconducting nanowires, indium arsenide (InAs) epitaxy in hybrid templates, and device fabrication on selective-area-grown lead telluride (PbTe) structures. In **chapter 4** we investigate gated metallic superconducting nanowire switches. We explain the mechanism for triggering the transition from the superconducting to the normal state, an effect that was controversially discussed in literature and could find use in superconducting signal routers and multiplexers in the near future. **Chapter 5** presents a novel method for semiconductor-superconductor hybrid device fabrication which relies on InAs

epitaxy inside superconducting, CMOS compatible templates. After further optimization, this method might enable the monolithic integration of classical cryogenic CMOS control electronics into scalable quantum processors. In **chapter 6** we present the first transport experiments on selective-area-grown lead telluride (PbTe) structures on InP. High electron mobility and phase coherence length, together with extreme material properties, make PbTe a promising building block for topological qubits. In **chapter 7** we summarize our findings and propose future directions for all three projects.

2 Theoretical Background

2.1. Superconductivity

The dependence of electrical resistivity in metals as a function of temperature was a heavily debated topic in the early 20th century. In 1911, H. K. Onnes successfully cooled down a sample of Hg below liquid helium temperature and made a remarkable discovery: the sample became a perfect conductor below a threshold temperature, which is now known as the critical temperature T_C [19]. In the following years, a plethora of metals and alloys were found to exhibit a similar superconducting state. Further important insights included the finding that superconductors are perfect diamagnets (Meißner-Ochsenfeld effect) and phenomenological models describing superconductivity emerged [20]. However, developing a microscopic description of superconductivity remained an open challenge for many years.

2.1.1. Microscopic Description

Experiments on different isotopes of Hg indicated that the atomic lattice of a material plays a crucial role in the emergence of superconductivity. Specifically, it was found that $T_\mathrm{C} \propto M^{-\alpha}$ where M is the atomic mass and $\alpha \approx 1/2$ [21, 22]. With this result in mind, J. Bardeen, L. N. Cooper, and J. R. Schrieffer (BCS) were able to develop a microscopic description of superconductivity in 1957 [23, 24].
At the heart of BCS theory is an attractive interaction between electrons. This interaction causes the Fermi sea to become unstable at low temperatures and electrons within an energy window 2Δ around the Fermi energy E_F to form bosonic Cooper pairs [25]. The attractive potential between electrons can intuitively be understood as being mediated by the lattice: a first electron traveling through a material distorts its lattice, leaving behind a locally increased positive charge density which in turn attracts a second electron. Considering the Fermi velocity of electrons ($v_\mathrm{F} \sim 10^6$ m/s) and the time constant associated with the lattice distortion (10^{-14} to 10^{-13} s), one finds a lower limit for the spatial extent of the interaction of 10 to 100 nm [20]. The BCS Hamiltonian reads [20]

$$H_\mathrm{BCS} = \sum_{\mathbf{k},\sigma} \xi_\mathbf{k} n_{\mathbf{k},\sigma} + \sum_{\mathbf{k},\mathbf{k'}} V_{\mathbf{k},\mathbf{k'}} \underbrace{c^\dagger_{\mathbf{k}\uparrow} c^\dagger_{-\mathbf{k}\downarrow}}_{P^\dagger_\mathbf{k}} \underbrace{c_{-\mathbf{k'}\downarrow} c_{\mathbf{k'}\uparrow}}_{P_\mathbf{k'}} \tag{2.1}$$

where the first term describes the kinetic energy and $n_{\mathbf{k},\sigma} = c^\dagger_{\mathbf{k}\sigma} c_{\mathbf{k}\sigma}$ is the particle number operator. The single particle kinetic energy $\xi_\mathbf{k}$ is defined relative to the chemical

potential μ and reads

$$\xi_{\mathrm{k}} = \frac{\hbar^2 k^2}{2m} - \mu. \tag{2.2}$$

The second term in equation 2.1 describes the s-wave pairing of electrons with opposite momentum and spin into Cooper pairs ($\mathbf{k}\uparrow, -\mathbf{k}\downarrow$) for negative pair potential $V_{\mathbf{k},\mathbf{k}'}$. $P^{\dagger}_{\mathbf{k}}$ and $P_{\mathbf{k}'}$ are the pair creation and annihilation operators, respectively.

2.1.2. Quasiparticles in Superconductors

In the following we discuss excitations from the BCS ground state. Such excitations are described by the Bogoliubov-de Gennes (BdG) equation [26]

$$\begin{pmatrix} H(\mathbf{r}) & \Delta(\mathbf{r}) \\ \Delta^*(\mathbf{r}) & -H(\mathbf{r}) \end{pmatrix} \Psi_{\mathbf{k}}(\mathbf{r}) = E_{\mathbf{k}} \Psi_{\mathbf{k}}(\mathbf{r}) \tag{2.3}$$

with the wave function in electron-hole space

$$\Psi_{\mathbf{k}}(\mathbf{r}) = \begin{pmatrix} u_{\mathbf{k}}(\mathbf{r}) \\ v_{\mathbf{k}}(\mathbf{r}) \end{pmatrix}. \tag{2.4}$$

The single-electron Hamiltonian is

$$H(\mathbf{r}) = -\frac{\hbar^2 \nabla^2}{2m^*} + U(\mathbf{r}) - \mu \tag{2.5}$$

where m^* is the effective electron mass and $U(\mathbf{r})$ is a scalar potential. The probability amplitudes $u_{\mathbf{k}}(\mathbf{r})$ and $v_{\mathbf{k}}(\mathbf{r})$ determine the character of the quasiparticle. We call an excitation electron-like if $|u_{\mathbf{k}}(\mathbf{r})|^2 > |v_{\mathbf{k}}(\mathbf{r})|^2$ and hole-like in the opposite case. Without superconductivity, i.e. if $\Delta(\mathbf{r}) = 0$ in equation 2.3, we obtain two decoupled Schrödinger equations for electrons and holes. $\Delta(\mathbf{r}) > 0$ couples $u_{\mathbf{k}}(\mathbf{r})$ and $v_{\mathbf{k}}(\mathbf{r})$, highlighting that excitations in superconductors are a coherent mixture of electron-like and hole-like states. Assuming a homogeneous superconductor with $U(\mathbf{r}) = 0$ and $\Delta(\mathbf{r}) = \Delta$, we can separate the spatial dependence of the wave function and find a solution to equation 2.3 of the form [26]

$$\Psi(\mathbf{r}) = e^{i\mathbf{k}\mathbf{r}} \cdot \begin{pmatrix} u_0 \\ v_0 \end{pmatrix} \tag{2.6}$$

with eigenvalues

$$E_{\mathbf{k}} = \pm\sqrt{\xi_{\mathbf{k}}^2 + \Delta^2} \tag{2.7}$$

and electron and hole coherence factors

$$|u_{\mathbf{k}}|^2 = \frac{1}{2}\left(1 + \frac{\xi_{\mathbf{k}}}{E_{\mathbf{k}}}\right), \quad |v_{\mathbf{k}}|^2 = \frac{1}{2}\left(1 - \frac{\xi_{\mathbf{k}}}{E_{\mathbf{k}}}\right). \tag{2.8}$$

We gain important insights into the formation of the superconducting state by considering the hole coherence factor $|v_{\mathbf{k}}(\mathbf{r})|^2$ which we plot in Fig. 2.1a as a function of the

single particle kinetic energy $\xi_{\mathbf{k}}$. We can understand $|v_{\mathbf{k}}(\mathbf{r})|^2$ as the probability to find a state $\mathbf{k}$ occupied, or equivalently that an excitation at $\mathbf{k}$ is hole-like [20, 26]. Crucially, $|v_{\mathbf{k}}(\mathbf{r})|^2$ at $T = 0$ (Fig. 2.1a) closely resembles the Fermi function at $T = T_{\mathrm{C}}$ [27]. The smeared out nature of $|v_{\mathbf{k}}(\mathbf{r})|^2$ indicates that the system increases its kinetic energy (first term in equation 2.1) compared to the noninteracting Fermi gas. This allows the system to form Cooper pairs, since the gained pairing energy (second term in equation 2.1) overcompensates for the invested kinetic energy. Figure 2.1a further plots the coherence factor $|u_{\mathbf{k}}|^2$ which describes the electron character of an excitation. An interesting situation is reached at $\xi_{\mathbf{k}} = 0$, where an excitation is similarly electron-like and hole-like. In Fig. 2.1b we compare the single particle excitation spectrum of a normal metal (green dashed lines) to that of a superconductor (solid blue/red line). The quasiparticle (QP) spectrum of a superconductor features an energy gap Δ which originates from the coupling of electron and hole states (equation 2.3). Consequently, no QP states exist within the energy gap. QP excitations with $\xi_{\mathbf{k}} > 0$ have electron character, excitations with $\xi_{\mathbf{k}} < 0$ are hole-like (Fig. 2.1b). For $\xi_{\mathbf{k}} \gg 0$ or $\xi_{\mathbf{k}} \ll 0$, excitations are pure electrons or holes, because at these points $|v_{\mathbf{k}}|^2 = 0$ and $|v_{\mathbf{k}}|^2 = 1$, respectively.
Finally, we compare the superconducting density of states D_{S} to the normal metal density of states D_{N} (Fig. 2.1c). Since we require that no states are lost when the normal metal transitions to the superconducting state, we can equate $\int D_{\mathrm{S}}(E_{\mathbf{k}})\,\mathrm{d}E_{\mathbf{k}} = \int D_{\mathrm{N}}(\xi_{\mathbf{k}})\,\mathrm{d}\xi_{\mathbf{k}} = \int D_{\mathrm{N}}(\xi_{\mathbf{k}})\,(\mathrm{d}\xi_{\mathbf{k}}/\mathrm{d}E_{\mathbf{k}})\,\mathrm{d}E_{\mathbf{k}}$. Assuming D_{N} is constant around E_F we obtain

$$D_{\mathrm{S}}(E_{\mathbf{k}}) = D_{\mathrm{N}}(\xi_{\mathbf{k}})\frac{\mathrm{d}\xi_{\mathbf{k}}}{\mathrm{d}E_{\mathbf{k}}} = \begin{cases} D_{\mathrm{N}}(E_F)\frac{E_{\mathbf{k}}}{\sqrt{E_{\mathbf{k}}^2-\Delta^2}} & \text{for } E_{\mathbf{k}} > \Delta \\ 0 & \text{for } E_{\mathbf{k}} < \Delta. \end{cases} \tag{2.9}$$

In Fig. 2.1c we plot both D_{S} and D_{N}. At $E_{\mathbf{k}} = \Delta$ the superconducting density of states diverges, at $E_{\mathbf{k}} \gg \Delta$ it approaches D_{N}.

2.2. Out-of-Equilibrium Phenomena

After introducing the concept of excitations in superconductors in the previous section, we discuss how such excitations are created. For this purpose, we first consider a superconductor at finite temperature in equilibrium. Then we move to systems which are out of thermal equilibrium. We will distinguish between energy-mode (even) and charge-mode (odd) disequilibrium and focus on systems in steady state disequilibrium. Finally, we comment on important relaxation mechanisms and their time scales.

2.2.1. Finite Temperature

A superconductor at finite temperature $0 < T < T_{\mathrm{C}}$ hosts quasiparticle excitations. In thermal equilibrium their occupation is described by the Fermi distribution

$$f_0(E_{\mathbf{k}}/k_{\mathrm{B}}T) = \frac{1}{e^{(E_{\mathbf{k}}/k_{\mathrm{B}}T)}+1} \tag{2.10}$$

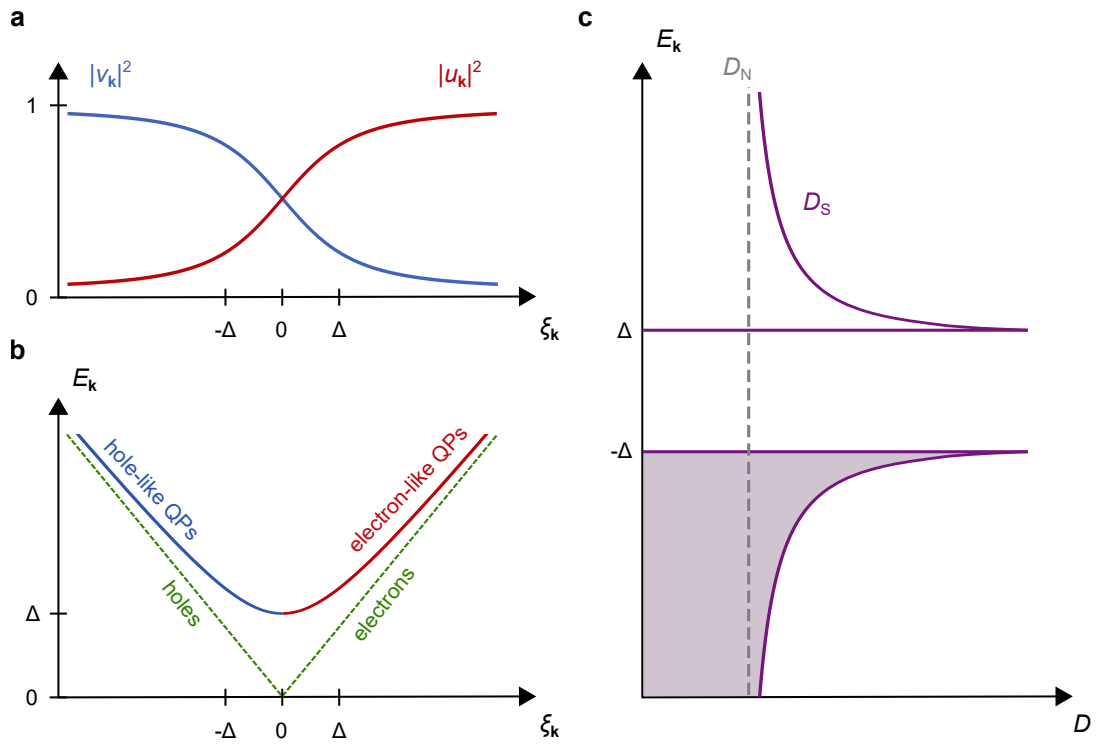

Figure 2.1. Fundamental characteristics of superconductors. **a** Probability $|v_{\mathbf{k}}(\mathbf{r})|^2$ to find a state $\mathbf{k}$ occupied or, equivalently, for an excitation to be hole-like. The function is smeared out even at zero temperature. $|u_{\mathbf{k}}(\mathbf{r})|^2$ is the probability for an excitation with electron-like character. **b** Excitation spectrum of electrons and holes in a normal metal (green) and of hole- and electron-like quasiparticles in a superconductor (blue and red solid line). No quasiparticle states exist at $|E < \Delta|$ due to the coupling of electron and hole states. **c** Density of states of a normal metal (dashed line) and of a superconductor (solid purple line). D_S is zero for $|E < \Delta|$. Figure inspired by [28] and [20].

where k_B is the Boltzmann constant. This situation is sketched in Fig. 2.2a where red (blue) dots indicate electron-like (hole-like) excitations.[1] By simplifying the pair potential of equation 2.1 to $V_{\mathbf{k},\mathbf{k}'} = -V$, with V a positive constant, the condition for self-consistency at thermal equilibrium reads [28]

$$1 = \frac{V}{2}\sum_{\mathbf{k}}\frac{1-2f_0}{E_{\mathbf{k}}} = \frac{V}{2}\sum_{\mathbf{k}}\frac{1-2f_0}{\sqrt{\xi_{\mathbf{k}}^2+\Delta^2}}. \tag{2.11}$$

[1] In the two-fluid model of superconductivity, such quasiparticle excitations are regarded as normal electrons.

The self-consistency equation allows us to relate the energy gap Δ to temperature. At $T \approx T_\mathrm{C}$, where a relevant number of quasiparticles are excited, one finds [28]

$$\frac{\Delta(T)}{\Delta(0)} \approx 1.74 \left(1 - \frac{T}{T_\mathrm{C}}\right)^{1/2}. \tag{2.12}$$

The energy gap at zero temperature is related to the critical temperature by

$$\Delta(0) = 1.764\ k_\mathrm{B} T_\mathrm{C}. \tag{2.13}$$

In out-of-equilibrium systems the quasiparticle occupation in equation 2.11 is generally $f_\mathbf{k} \neq f_0$, i.e. non-thermal. The origin and implications of such distributions are discussed in the following sections.

2.2.2. Energy-Mode Disequilibrium

A superconductor can be driven into a disequilibrium state by impinging phonons (see section 2.5) or photons. Quasiparticles excited by such neutral perturbations (in addition to thermally excited quasiparticles) are schematically depicted in Fig. 2.2b. It is important to recognize that quasiparticles are distributed equally on both particle and hole branch of the excitation spectrum in this so-called energy-mode disequilibrium. Due to its symmetric quasiparticle excitation, in literature this situation is also referred to as the even mode [29, 30].[2] We can associate an energy-mode disequilibrium state with an effective quasiparticle temperature T^*. Importantly, this parameter is not to be misunderstood as a thermodynamic temperature, instead it allows us to intuitively describe the (reduced) superconducting gap in disequilibrium as $\Delta_\mathrm{BCS}(T^*) = \Delta(f_\mathbf{k})$, where the right-hand side is calculated by plugging the out-of-equilibrium distribution $f_\mathbf{k} \neq f_0$ into Eq. 2.11 [28].

2.2.3. Charge-Mode Disequilibrium

If charged particles are injected into or extracted from a superconductor, the system obtains a net quasiparticle charge Q^* and is said to be in charge-mode disequilibrium, also referred to in literature as the odd mode or branch imbalance. We can write the imbalance as [28, 30]

$$Q^* = \sum_\mathbf{k} \underbrace{\left(u_\mathbf{k}^2 - v_\mathbf{k}^2\right)}_{q_\mathbf{k}} \delta f_\mathbf{k} = \sum_\mathbf{k} \frac{\xi_\mathbf{k}}{E_\mathbf{k}} \delta f_\mathbf{k} \tag{2.14}$$

where we describe the quasiparticle charge Q^* in terms of the deviation from thermal equilibrium $\delta f_\mathbf{k} = f_\mathbf{k} - f_0$ and the BCS coherence factors (see equation 2.8). We identify the term $u_\mathbf{k}^2 - v_\mathbf{k}^2 = q_\mathbf{k}$ as the effective charge of a single quasiparticle excitation. Importantly, $q_\mathbf{k}$ is a function of the energy $\xi_\mathbf{k}$ and ranges from -1 for $\xi_\mathbf{k} \ll -\Delta$ to 1

[2] The even mode can also be excited by charged perturbations, however, they will additionally excite the odd mode which is discussed below.

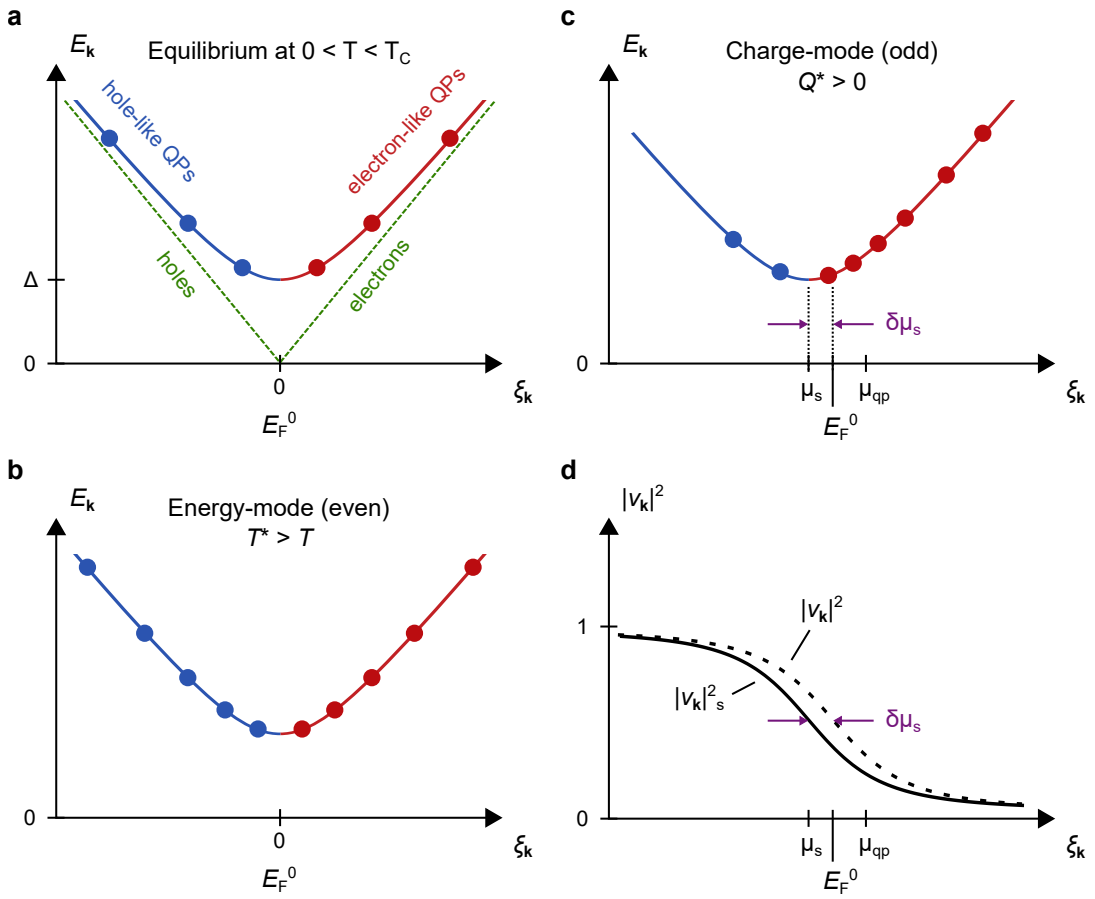

Figure 2.2. Quasiparticle excitations in out-of-equilibrium superconductors. Quasiparticle excitations are indicated as dots. **a** In thermal equilibrium, symmetric electron-hole excitations are Fermi distributed. **b** The superconductor is driven into energy-mode disequilibrium via neutral perturbations. Hole-like and electron-like branches are still occupied equally, however, the excitations are no longer Fermi distributed. **c** Charged perturbations drive the superconductor into charge-mode disequilibrium where excitation branches are no longer occupied evenly. To account for charge neutrality, the superfluid and quasiparticle chemical potentials are shifted to μ_s and μ_{qp}, respectively. **d** The distribution $|v_\mathbf{k}|^2$ is shifted accordingly to $|v_\mathbf{k}|^2_s$. Figure inspired by [30] and [28].

for $\xi_\mathbf{k} \gg \Delta$.[3] We now focus on the case of electron injection (where $Q^* > 0$), but the discussion is equivalently valid for electron extraction.
To ensure overall charge neutrality, an additional quasiparticle charge Q^* must be com-

[3]This is intuitively clear if we consider an electron impinging on a superconductor with energy much larger than Δ. The probability for it to enter into the superconductor as an electron-like excitation is given by the electron coherence factor $|u_\mathbf{k}(eV \gg \Delta)|^2 = 1$.

pensated by Cooper pairs with equivalent charge leaving the injection region. The removal of Cooper pairs decreases the superfluid chemical potential by $\delta\mu_s$ to μ_s. Figure 2.2c exemplifies this situation for $Q^* > 0$. Note that in contrast to energy-mode disequilibrium, hole-like and electron-like excitations are now no longer balanced (Fig. 2.2c). Since the minimum of the quasiparticle excitation spectrum is pinned to the superfluid chemical potential, it is shifted by $\delta\mu_\mathrm{s}$ and Eq. 2.2 becomes $\xi_\mathrm{k} = \frac{\hbar^2 k^2}{2m} - \mu_\mathrm{s}$. This preserves the meaning of the single effective quasiparticle charge $q_\mathbf{k} = \xi_\mathbf{k}/E_\mathbf{k}$ but also implies that $q_\mathbf{k}$ of an excitation with $E_\mathbf{k} \gtrsim \Delta$ might change sign as another quasiparticle is added. The shift of the superfluid chemical potential is also reflected in the new Cooper pair distribution $|v_\mathbf{k}|^2_\mathrm{s}$. This is depicted in Fig. 2.2d, together with an increased quasiparticle chemical potential $\mu_\mathrm{qp} > E^0_\mathrm{F}$, larger than the equilibrium Fermi energy E^0_F to compensate for the lower μ_s.

2.2.4. Relaxation Mechanisms and Time Scales

We now discuss how equilibrium can be restored after perturbation events. Finding a generalized description for the mechanisms and time scales associated with such relaxation is a challenging task, since both depend on the superconducting material, the device geometry and its coupling to its surroundings, defects and impurities in the superconductor, the anisotropy of the superconducting gap, temperature gradients in the device, the nature and energy of the perturbations, and temperature [30]. Due to these complications, an exhaustive discussion of all parameters goes beyond the scope of this introduction. Instead, we will focus on general trends and typical values found in experiments. The reviews [29, 30] and references therein provide further details.

Energy-mode disequilibrium, which is characterized by equal occupation of quasiparticle branches (Fig. 2.2b), equilibrates in a two step process for $k_\mathrm{B}T \ll \Delta$ [29, 31]. First, quasiparticles which can assume energies $E_\mathbf{k} \gg \Delta$ for high-energy perturbations relax within the thermalization time τ_th to lower energy states close to the gap edge under phonon emission. The thermalization time τ_th can be on the order of a few ps (e.g. in Nb [30]) and was found to decrease exponentially as $E_\mathbf{k}$ increases [29]. In a second step, the excitations which now have energies $E_\mathbf{k} \gtrsim \Delta$ recombine into Cooper pairs, again by phonon emission. The time scale associated with the second step is the recombination time τ_R which is inversely proportional to the number of quasiparticles. It is often found that the recombination time τ_R dominates the overall relaxation time (e.g. in Al and Sn). Experiments on Al thin films yielded $\tau_\mathrm{R} \approx 10^{-7}$ s at $\Delta = k_\mathrm{B}T$ and τ_th at least an order of magnitude smaller than τ_R [31]. An exception to this finding is e.g. Pb at low temperature, where cooling and recombination occur on a similar time scale [29]. As pointed out in Ref. [32], if phonons emitted in the thermalization and recombination step have energies $\geq 2\Delta$, they themselves can break Cooper pairs again, thereby increasing the effective recombination time.

In the case of charge-mode disequilibrium, an additional timescale, namely the branch

mixing time τ_{Q^*}, also called branch relaxation time, has to be considered. The branch mixing time τ_{Q^*} indicates the time in which charge balance, i.e. $Q^* = 0$, is restored. A detailed study of τ_{Q^*} in Sn was performed in [29, 33]. In these experiments, a superconducting segment consisting of a Sn thin film was contacted by two superconducting contacts and two tunneling contacts [33, 34]. The latter are formed by a thin insulating layer between the superconductor and normal metal leads (see discussion on superconductor/normal metal tunnel junctions in section 2.3). Quasiparticles with energies much larger than Δ were injected via the first tunnel junction, thus creating charge imbalance in the Sn film.[4] The quasiparticle chemical potential was measured with the second tunneling junction on the reverse side of the Sn segment and the superfluid chemical potential was measured with the superconducting lead contacting the Sn segment. The voltage V that must be applied between the two junctions to zero the current was shown to be proportional to τ_{Q^*} [34]. For injected quasiparticles with energies much larger than Δ and at $T \lesssim T_\mathrm{C}$, the authors of Refs. [29, 33] found that $\tau_{Q^*}^{ph} \sim 10^{-10}\Delta(0)/\Delta(T)$ s for inelastic electron-phonon scattering. At lower temperature, elastic scattering events were found to become important with $\tau_{Q^*}^{el}$ ranging from $1.4 \cdot 10^{-10}$ s to 10^{-9} s. The precise values strongly depend on the details of the superconductor: fastest branch mixing occurs in dirty superconductors with anisotropic Δ [35], where elastic scattering mechanisms may dominate [28].
The charge imbalance relaxation length λ_{Q^*} is typically measured using long nanowire devices along which quasiparticle diffusion is one-dimensional [28]. Q^* decays in space as $\exp(-x/\lambda_{Q^*})$ [28] where in the diffusive case

$$\lambda_{Q^*} = \sqrt{D\tau_{Q^*}} = \left(\frac{1}{3} v_\mathrm{F} l \tau_{Q^*}\right)^{\frac{1}{2}}. \tag{2.15}$$

Here, D is the diffusion constant, v_F is the Fermi velocity, and l is the mean free path. More recent experiments on Al nanowires [36] revealed λ_{Q^*} of a few μm. Additionally, the superconducting gap was affected significantly only if the energy of injected electrons exceeded Δ. We will discuss the regime of small injection energies (smaller than Δ) in section 2.4.

2.3. Tunnel Junctions

In the previous section, we mentioned the concept of quasiparticle injection via a normal metal/insulator/superconductor (NIS) junction. Here, we review the properties of NIS junctions in more detail and discuss typical applications. Our description is based on the semiconductor model [37] from which we gain an intuitive picture of the tunneling processes. However, this model should be used with caution as it greatly simplifies the description of superconductors. In particular, it does not accurately account for the

[4] Since the Sn segment is a thin film and quasiparticles are injected via a large interface, quasiparticle diffusion is not important in this configuration. Steady-state charge imbalance is reached when the injection rate equals the average relaxation rate, i.e. $\dot{Q}^*_\mathrm{inj} = Q^*/\tau_{Q^*}$.

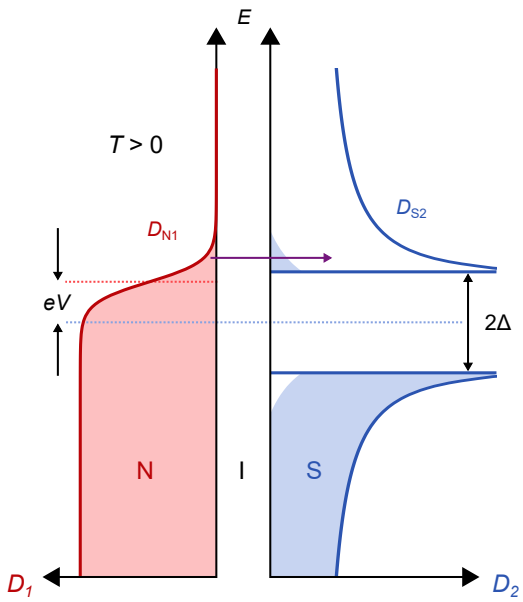

Figure 2.3. NIS tunnel junction. Semiconductor model of an NIS tunnel junction at finite temperature $T > 0$. Shaded areas indicate occupied states. Electrons elastically tunnel from the normal metal into the superconductor when a bias voltage V is applied. Figure inspired by [20] and [38].

mixed electron-like and hole-like nature of excitations in superconductors (see section 2.1.2) but instead treats them as electrons and holes, respectively.
Figure 2.3 schematically depicts an NIS junction in the semiconductor model. Occupied states are shaded in red and blue for the normal metal and superconductor, respectively. At finite temperature $T > 0$, the Fermi distribution in the normal metal is smeared out and the superconductor features electron-like and hole-like excitations. As we apply a bias voltage V across the junction, electrons start to tunnel from the tail of the Fermi distribution of the normal metal to unoccupied states in the superconductor. This is indicated by the horizontal purple arrow in Fig. 2.3 under the assumption of elastic tunneling.

The elastic tunneling current I is proportional to the product of occupied initial states and unoccupied final states and reads as a function of bias V [20]:

$$\begin{aligned} I_{\mathrm{NS}}(V) =& C\,|t|^2\, D_{\mathrm{N1}}\left(E_{\mathrm{F}}\right) D_{\mathrm{N2}}\left(E_{\mathrm{F}}\right) \int_{-\infty}^{\infty} \frac{D_{\mathrm{S2}}\left(E\right)}{D_{\mathrm{N2}}\left(E_{\mathrm{F}}\right)} \left(f(E) - f(E+eV)\right) \mathrm{d}E \\ =& \frac{G_{\mathrm{NN}}}{e} \int_{-\infty}^{\infty} \frac{D_{\mathrm{S2}}\left(E\right)}{D_{\mathrm{N2}}\left(E_{\mathrm{F}}\right)} \left(f(E) - f(E+eV)\right) \mathrm{d}E. \end{aligned} \tag{2.16}$$

Here, C is a constant, t is the constant tunneling matrix element, and $D_{1,2}$ is the density of states on the left and right-hand side of Fig. 2.3 in the normal (N) and superconducting (S) state, respectively. G_{NN} is the conductance with both metals in the normal state and

is a characteristic value of the junction. In equation 2.16 we further assumed a constant normal density of states $D_{\mathrm{N}}(E+eV) \approx D_{\mathrm{N}}(E_{\mathrm{F}})$. At zero temperature and $e|V| < \Delta$, the current is $I_{\mathrm{NS}} = 0$ due to the energy gap in D_{S2}. At higher bias $e|V| > \Delta$, the current rapidly increases due to the high number of unoccupied states in the superconductor. At finite temperature this transition is smeared out (Fig. 2.3).
In experiments one often measures the differential conductance G_{NS}, which yields the convenient relation [20]

$$G_{\mathrm{NS}}(V) = \frac{\mathrm{d}I_{\mathrm{NS}}}{\mathrm{d}U} = G_{\mathrm{NN}} \int_{-\infty}^{\infty} \frac{D_{\mathrm{S2}}(E)}{D_{\mathrm{N2}}(E_{\mathrm{F}})} \left[-\frac{\partial f(E+eV)}{\partial (eV)} \right] \mathrm{d}E. \tag{2.17}$$

The term in square brackets is a bell-shaped function with peak at $-eV$, unit area, and width $\sim 4k_{\mathrm{B}}T$. Therefore, we obtain for low temperature $T \to 0$ [20]

$$G_{\mathrm{NS}}(V) = G_{\mathrm{NN}} \frac{D_{\mathrm{S2}}(eV)}{D_{\mathrm{N2}}(E_{\mathrm{F}})}. \tag{2.18}$$

In other words, the differential tunneling conductance is proportional to the superconducting density of states D_{S2}. In sections 5.1.6 and 5.3.1 we will use this finding to measure the induced superconducting gap of titanium nitride (TiN) in InAs via a gate-defined tunnel junction.
Besides their use as quasiparticle injectors, detectors, and as tools to measure the superconducting density of states, NIS junctions are utilized in other interesting applications. Assume a junction is biased at $e|V| \lesssim \Delta$ as sketched in Fig. 2.3. Owing to the energy gap and the diverging density of states at $E = \Delta$, the superconductor effectively operates as an energy filter and only the highest-energy electrons tunnel from the normal metal into the superconductor. The extraction of hot electrons cools the normal metal [39]. This phenomenon was recently used to demonstrate cooling of a degenerately doped Si sub-chip in an elegant experiment [40]. This idea can be further expanded to sandwiched SINIS junctions [41] where hot electrons are extracted into one tunnel contact, while at the same time cold electrons are injected into the normal metal from the second tunnel junction.
Finally, superconducting tunnel junctions can be used as phonon generators and detectors [42]. Such junctions typically have SIS geometry where the tunnel barrier separates two superconductors of the same material. To detect phonons, SIS junctions are biased to $e|V| < \Delta$. Quasiparticles are excited in the first electrode by phonons with energy $E_{\mathrm{phon}} \geq 2\Delta$ and extracted through the tunnel barrier into the second superconductor, where the flow of a current is measured [43]. For phonon generation, a voltage $e|V| > 2\Delta$ is applied such that a current of quasiparticles flows through the junction into the second superconductor. There, quasiparticles relax and recombine as described in section 2.2.4. The maximum energy of phonons generated during relaxation is $E_{\mathrm{phon}} = eV - 2\Delta$, while phonons emitted during recombination have energy $E_{\mathrm{phon}} \approx 2\Delta$ [43].

2.4. Andreev-Reflection

In section 2.2.3 we investigated charge-mode disequilibrium assuming electrons with energies $|E| > \Delta$ are injected or extracted. We described quasiparticles excited by such large perturbations as predominantly electron-like or hole-like. We now turn our attention to the case of charged perturbations with energies smaller than the superconducting gap. Figure 2.4a schematically shows an interface formed by a normal metal and a superconductor. We consider an electron with energy $E_\mathrm{F} < E < \Delta$ to be incident on the superconductor. Since D_S has a gap at this energy, the incident electron cannot propagate in the superconductor. Additionally, let us assume the N-S interface is perfectly transparent. This excludes reflection of the incident electron, but if we allow a second electron to be taken from the Fermi sea of the normal metal, a Cooper pair can be formed in the superconductor. This process is called Andreev reflection [44].
If the electron incident on the interface is in the state $(+\mathbf{k}, \uparrow)$, then the electron extracted from the normal metal must have $(-\mathbf{k}, \downarrow)$ for the two electrons to form a Cooper pair. The wave vector of the Fermi sea with one missing electron is therefore $+\mathbf{k}$. Equivalently, the electron vacancy can be regarded as a hole at $-E$ with positive charge and wave vector $+\mathbf{k}$ (Fig. 2.4a). For electrons the group velocity $\mathbf{v_k} = \frac{1}{\hbar}\nabla_\mathbf{k} E$ points in the same direction as $\mathbf{k}$, but for holes $\mathbf{v_k}$ and $\mathbf{k}$ point in opposite directions [26]. Consequently, the incident electron and the retroreflected hole travel in opposite direction, despite the fact that they both have wave vector $+\mathbf{k}$. This is schematically depicted in the real space representation of Andreev reflection in Fig. 2.4b. The opposite trajectory and charge of electron and hole on the normal metal side further imply that the conductance is doubled as the normal current is converted into a supercurrent [26]. Furthermore, the injected electrons do not cause charge-mode disequilibrium in the superconductor, since we assumed perfect conversion of electrons into Cooper pairs.
We should keep in mind that, in a more rigorous picture of Andreev reflection at a perfect interface, one would describe injected electrons with $|E| < \Delta$ as evanescent quasiparticle states that enter in the superconductor and decay on a length scale $\xi(T)$ into Cooper pairs [45]. $\xi(T)$ is typically much shorter than the charge imbalance relaxation length λ_{Q^*} [28].

Owing to interface degradation such as oxide formation and interface disorder, as well as Fermi velocity mismatch in the case of a semiconductor/superconductor device, a realistic hybrid interface will differ from the ideal situation described so far. Blonder, Tinkham, and Klapwijk (BTK) formulated a successful model to describe such imperfect interfaces [45]. The model assumes the pairing potential to increase at the interface as $\Delta(x) = \Theta(x)\Delta_0$ where $\Theta(x)$ is the step function. The interface (located at $x = 0$) is modeled by introducing a potential in equation 2.3 of the form [26]

$$U(x) = U_0\Theta(-x) + \frac{\hbar^2 k_\mathrm{FS}}{m_\mathrm{e}} Z\delta(x) \tag{2.19}$$

where the first term represents the Fermi velocity mismatch and the second term describes the transparency of the interface. $k_\mathrm{FS} = \sqrt{2m_\mathrm{e}\mu/\hbar^2}$ and m_e are the wave number

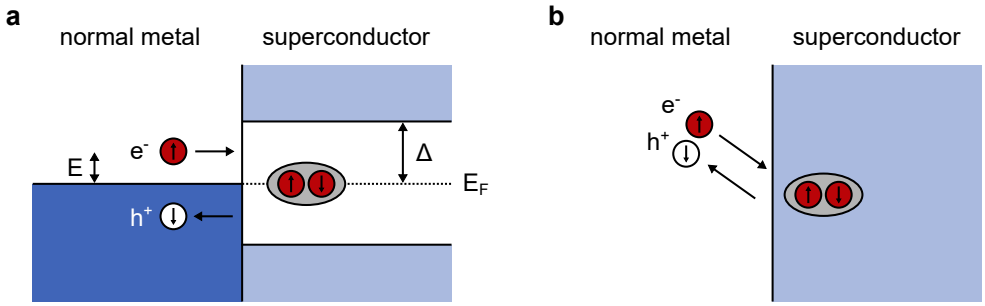

Figure 2.4. Andreev reflection at a perfect normal metal/superconductor interface. a Energy representation of a first electron with energy $|E| < \Delta$ impinging on the superconductor. Together with a second electron of opposite momentum (equivalent to a hole traveling away from the interface) it forms a Cooper pair in the superconductor. **b** Real space representation of the process in **a**. The retroreflected hole takes the same path as the impinging electron but has opposite group velocity. Figure inspired by [26] and [46].

in the superconductor and the electron mass, respectively. Z is a dimensionless parameter characterizing the interface barrier. $Z = 0$ implies perfect Andreev reflection, $Z > 0$ indicates a finite probability of normal reflection.
Using a plane-wave ansatz [26] we can describe the scattering of an incident electron wave

$$\Psi_{\mathrm{in}}(x) = \begin{pmatrix} 1 \\ 0 \end{pmatrix} e^{ik_{\mathrm{e}}x} \tag{2.20}$$

into reflected holes or electrons in the normal metal

$$\Psi_{\mathrm{refl}}(x) = a \begin{pmatrix} 0 \\ 1 \end{pmatrix} e^{ik_{\mathrm{h}}x} + b \begin{pmatrix} 1 \\ 0 \end{pmatrix} e^{-ik_{\mathrm{e}}x} \tag{2.21}$$

and electron-like and hole-like quasiparticles in the superconductor

$$\Psi_{\mathrm{qp}}(x) = c \begin{pmatrix} u_0 \\ v_0 \end{pmatrix} e^{ik'_{\mathrm{e}}x} + d \begin{pmatrix} u_0 \\ v_0 \end{pmatrix} e^{-ik'_{\mathrm{h}}x}. \tag{2.22}$$

In Fig. 2.5 the terms of $\Psi_{\mathrm{in}}(x)$, $\Psi_{\mathrm{refl}}(x)$, and $\Psi_{\mathrm{qp}}(x)$ are illustrated, with arrows pointing in the direction of the group velocity. The wave numbers k_{e}, k_{h}, k'_{e}, and k'_{h} (for electrons, holes, electron-like quasiparticles and hole-like quasiparticles, respectively) read [26]

$$k_{\mathrm{e,h}} = \sqrt{k_{\mathrm{FN}}^2 \pm (2m^*/\hbar^2)\, E} \quad \text{and} \quad k'_{\mathrm{e,h}} = \sqrt{k_{\mathrm{FS}}^2 \pm (2m_{\mathrm{e}}/\hbar^2)\, \xi} \tag{2.23}$$

where $k_{\mathrm{FN}} = \sqrt{2m_{\mathrm{e}}\,(\mu - U_0)\,/\hbar^2}$ in the normal metal and ξ is given by Eq. 2.7.

Using the boundary conditions of the above wave functions, one can now calculate the probabilities $A(E) = a^*a$ for Andreev reflection and $B(E) = b^*b$ for normal reflection at

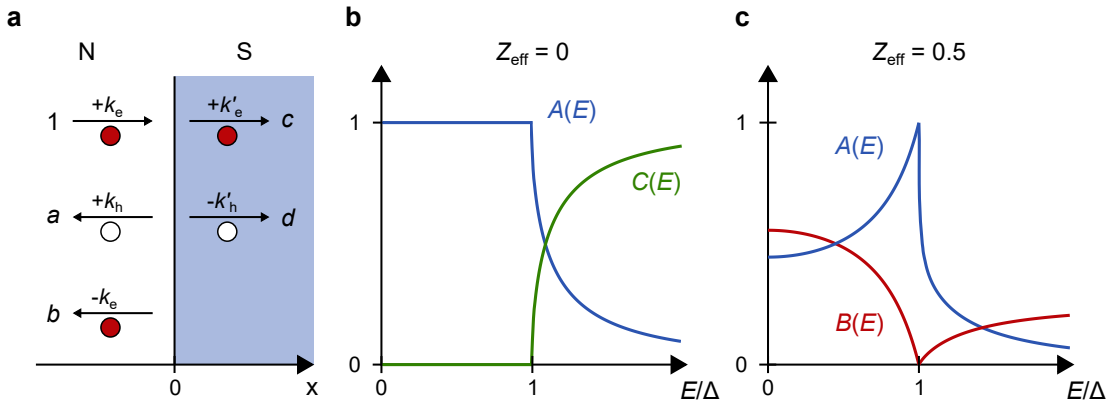

Figure 2.5. Andreev reflection at a normal metal/superconductor interface with barrier. a An electron impinging on a normal metal/superconductor interface can be Andreev reflected as a hole, reflected as an electron, or transmitted as an electron-like or hole-like quasiparticle. Arrows indicate the direction of the group velocity. Details are discussed in the text. **b** Probabilities $A(E)$ and $C(E)$ for Andreev reflection and transmission as an electron-like quasiparticle, respectively, at an interface without barrier ($Z_{\text{eff}} = 0$). **c** Probabilities $A(E)$ and $B(E)$ for Andreev reflection and normal reflection, respectively, at an interface with barrier $Z_{\text{eff}} = 0.5$. Figure inspired by [26] and [45].

the interface. Their general form reads [45]

$$A(E) = \begin{cases} \frac{\Delta^2}{E^2+(\Delta^2-E^2)(1+2Z^2)^2} & \text{for } E < \Delta \\ \frac{u_0^2 v_0^2}{\left(u_0^2+Z^2\left(u_0^2-v_0^2\right)\right)^2} & \text{for } E > \Delta \end{cases}$$
$$B(E) = \begin{cases} 1 - A(E) & \text{for } E < \Delta \\ \frac{\left(u_0^2-v_0^2\right)^2 Z^2\left(1+Z^2\right)}{\left(u_0^2+Z^2\left(u_0^2-v_0^2\right)\right)^2} & \text{for } E > \Delta. \end{cases} \tag{2.24}$$

In these relations we can account for the Fermi velocity mismatch $r = v_{\text{FN}}/v_{\text{FS}}$ at the interface by shifting the Z parameter to a higher effective value $Z_{\text{eff}} = \sqrt{Z^2 + (1-r)^2/4r}$ [47]. The probabilities $A(E)$ and $B(E)$ substantially simplify for $Z_{\text{eff}} = 0$ to $A(E < \Delta) = 1$, $A(E > \Delta) = v_0^2/u_0^2$, and $B = 0$. This case is plotted in Fig. 2.5b together with the probability for normal transmission $C(E < \Delta) = 0$ and $C(E > \Delta) = 1 - A$. We recognize the effects discussed above, that is, perfect Andreev reflection for $E < \Delta$ and injection of electron-like quasiparticles for $E > \Delta$ which cause charge-mode disequilibrium in the superconductor (see section 2.2.3).
For a barrier $Z_{\text{eff}} > 0$, the probability of Andreev reflection is decreased whereas the probability of normal reflection becomes finite. This is exemplified in Fig. 2.5c for $Z_{\text{eff}} = 0.5$. A special case is reached at $E = \Delta$, where the superconducting density of states diverges. Here, $A = 1$ and $B = 0$ for all Z_{eff} [45].

2.5. Phonons in Silicon

In section 2.2.2 we introduced the concept of out-of-equilibrium superconductivity and indicated that phonons can excite energy-mode disequilibrium, in which case quasiparticles have a non-thermal distribution. In section 4.3 we experimentally investigate the quench of superconductivity in nanowires coupled to a Si substrate which can host high-energy phonons. It is therefore instructive to review the phononic properties of Si in the following.

Figure 2.6a shows the dispersion relation of phonons in Si along high-symmetry directions. Solid lines correspond to calculations performed in Ref. [48] using the bond charge model [49]. Markers in Fig. 2.6a are data obtained from neutron scattering experiments [50]. Si has a two atom basis, hence, three optical and three acoustic phonon modes can be excited. In [100] direction (Γ to X) and [111] direction (Γ to L) the branches are partially degenerate. Along the [110] direction (Γ to K) all degeneracies are lifted. Figure 2.6b plots the corresponding phononic density of states (DOS) in Si. The maximum lattice frequency in Si is $\sim$ 16 THz [48, 51], corresponding to a maximum phonon energy of $\sim$ 66 meV for transverse and longitudinal optical phonons. No phononic states exist above this energy. Calculations of Si surface phonons revealed additional low energy modes in the spectrum, but details of their dispersion curves depend on the surface orientation and surface reconstruction. The maximum energy of surface phonons is similar to that of bulk phonons [52, 53]. Experiments showed that details of the Si surface reconstruction can also alter the phonon DOS [54] and chemical surface treatments such as removal of native SiO_2 [55] as well as roughening of Si surfaces [56] can lead to enhanced phonon scattering. Finally, the phononic spectrum of Si can be deliberately engineered by surface patterning [57].

In chapter 4 we investigate the impact of phonons in a Si substrate on superconducting nanowires. Phonons are produced due to the decay of high energy electrons injected into the substrate. As electrons relax, optical and acoustic phonons are emitted [58]. Moreover, electron-phonon scattering is enhanced at high electric fields [59]. Many details of hot electron relaxation in Si such as the role of optical phonons, their subsequent decay into acoustic modes (which govern thermal conductance [60]), and the dependence on electron energy and lattice temperature are currently still under debate [58].

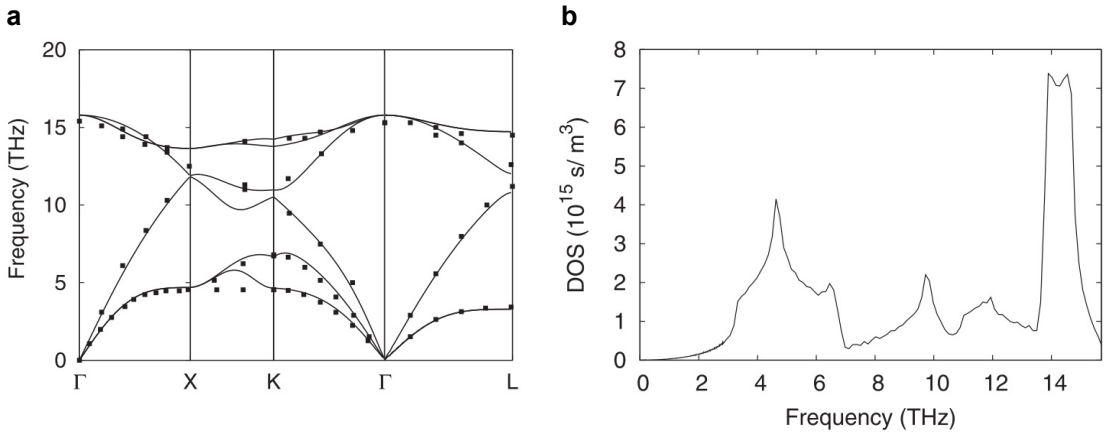

Figure 2.6. Phonon dispersion relation and DOS in Si. a Calculated phonon dispersion relations for Si (lines) together with experimental data from neutron scattering experiments (markers). **b** Calculated phononic density of states in Si. No states are available above 16 THz. Reprinted from [48], with the permission of AIP Publishing.

2.6. Epitaxy of Semiconductor Nanowires

Semiconductor nanowires, due to their unique properties, are widely used in research [61] e.g. in solar cells [62], for force sensing [63], or as tips in scanning tunneling microscopy [64]. Throughout this thesis, we study semiconductor nanowires for their electronic properties. In particular, we investigate nanowires with a diameter d similar to the Fermi wavelength $\lambda_\mathrm{F} = 2\pi/k_\mathrm{F}$, the regime where quantization effects become important at low temperature. The Fermi wavelength depends on the electron density n_e via the Fermi wavevector, which reads $k_\mathrm{F} = \left(3\pi^2 n_e\right)^{1/3}$ in the three-dimensional case [20]. With a typical carrier density on the order of $n_e \sim 10^{18}$ cm^{-3}, we aim for nanowires with a diameter of a few tens of nm. For high-quality material and at low temperature, d can be smaller than the electron mean free path l_e and the electron phase coherence length l_φ. The length L of nanowires investigated in this work is typically on the order of 1 μm, where often $d \lesssim l_\mathrm{e} < L < l_\varphi$ (see chapter 6). However, these relations crucially depend on the scattering mechanisms in the nanowire, which strongly depend on details of the system such as the material, device geometry, doping, interfaces, and temperature.

A versatile platform that allows growth of semiconductor nanowires with the specifications outlined above is the vapor-liquid-solid (VLS) method [65]. VLS growth is typically Au-catalyzed, however Au-free self-catalyzed growth of vertical nanowires has been demonstrated. In the latter case, the catalytic droplet is formed by one constituent of the nanowire material, e.g. In [66], or Ga [67]. The VLS method allows out-of-plane nanowire growth with high yield and aspect ratio, as well as exceptional control over nanowire diameter and crystal phase [68]. Furthermore, complex geometries such as core shell nanowires [69], modulation doping [70], heterostructures [71], and nanowire

networks [72] have been demonstrated. This flexibility makes VLS growth often the method of choice when demonstrating epitaxy of novel materials [73] and many pioneering transport experiments were performed on VLS-grown wires [74–77].
Despite these favorable properties, fabrication of contacts and multiple gates for transport experiments on individual vertical nanowires would be extremely challenging. Hence, to enable top-down fabrication, VLS nanowires are often placed manually on substrates, a process that severely limits scalability. For this reason, tremendous effort has recently been put into the development of deterministic in-plane growth of high-quality nanowires. In the following, we introduce the selective-area-growth and template-assisted selective epitaxy methods. They both enable in-plane nanowire growth and we will use them in the experiments of chapters 5 and 6.

2.6.1. Selective-Area-Growth

Selective-area-growth (SAG) of nanowire structures uses dielectric masks (typically SiO_2 or SiN_x) on which openings are lithographically defined. InP is often used as the substrate and locally exposed after top-down etching of the mask. SAG relies on the diffusion of precursors in vapor and on the mask surface towards the mask openings where they nucleate and fill the pre-defined trenches. Since the growth interface is directly exposed on the chip surface, complex structures such as branched geometries and networks can be realized. The required precursor diffusion lengths are sufficiently small to enable growth both via molecular beam epitaxy (MBE) [78] and metal-organic vapor phase epitaxy (MOVPE) [79]. The cross-section of one-dimensional SAG structures is mainly determined by the growth time and the substrate and trench crystal orientation [78, 80], as well as the ratio of group V and group III precursors (V/III ratio) [81]. To obtain conformal single crystalline structures, the trench orientation must point along high-symmetry directions [78]. As the crystal exceeds the trench it can laterally expand beyond the lithographically defined mask, further modifying the cross-section.
Recently, SAG of InAs [80, 82] and InSb [79, 83] on InP was demonstrated. Due to the substrate/nanowire lattice mismatch (see Tab. 2.1), misfit dislocations form at the interface to relieve the strain. Additionally, twin planes parallel to the (111)B substrate may form close to the interface [79]. To reduce scattering at such hetero-interfaces, buffer layers can be introduced to allow elastic strain relaxation. A recent study on buffered InAs nanowires on InP found a mobility $\mu > 5000$ cm^2/(Vs) and phase coherence length $l_\varphi > 10$ μm [84]. In section 3.3 we discuss device fabrication on selective-area-grown PbTe structures and transport experiments are detailed in chapter 6.

Hybrid semiconductor/superconductor devices based on in-plane SAG can be realized by deposition of a superconductor on the entire chip and subsequent etching [79, 82] or alternatively by fabrication of lithographically defined vertical pillars and shadow epitaxy of superconductors [85].
Going forward it has to be noted that InP is a piezo-electric material which limits on-chip integration of RF components [86]. Furthermore, InP is incompatible with established complementary metal–oxide–semiconductor (CMOS) techniques. For rapid scaling, in-

plane SAG on Si substrates would be highly desirable. However, owing to the large lattice mismatch, current approaches require growth of multiple global buffer layers and exhibit limited selectivity [87].

2.6.2. Template-Assisted Selective Epitaxy

In template-assisted selective epitaxy (TASE), III-V semiconductors nucleate on a small crystalline Si seed surface and expand into a SiO_2 template. The key difference between TASE and SAG lies in the aspect ratio of the template and the size of the seed surface. Templates used in this thesis have a typical length of ~ 1 μm and both width and height between 50 nm and 100 nm. The lithographically defined TASE templates determine the cross-section of grown structures, while the length of nanowires is tuned by the growth time. A small Si seed surface area on the order of 50 nm $\times$ 50 nm inside the template together with the high aspect ratio allows monolithic integration of III-V semiconductors directly on Si, since strain from lattice mismatch is relieved in a dislocation network localized at the hetero-interface [88, 89]. Furthermore, TASE growth can be free of planar stacking faults [90], though deliberate tuning between pure zinc-blende and wurzite phase has so far only been shown for InP [91].
The fabrication of TASE templates is CMOS compatible and out-of-plane growth [92, 93], in-plane growth [94, 95], stacked geometries [94], cross-junctions [96] and nano-sheets [97] have been demonstrated.

The high aspect ratio of TASE templates brings about crucial implications which must be considered in device design. First, precursor species must reach the nanowire growth interface which might be located deep (~ 1 μm) inside a template. This necessitates high growth selectivity and long precursor diffusion lengths, requirements which can be fulfilled in MOVPE [93]. Second, the template geometry plays an active role in the local V/III ratio at the growth interface. This is a consequence of the distinct group-III and group-V precursor diffusion mechanisms, which we will consider now using the specific example of InAs following the model proposed in [93].

Figure 2.7a schematically shows a vertical SiO_2 template together with a seed (green cylinder) and a segment of an InAs nanowire (blue cylinder). The top facet of the nanowire is colored red. At a growth temperature $T \gtrsim 520$ °C, the nanowire growth rate is limited by mass transport into the template and towards the growth interface. The group-V precursor tertbutylarsine (TBAs) and its products after (partial) decomposition are transported to the growth surface via vapor diffusion with a mean free path of up to $l_{\mathrm{V}}^{\mathrm{max}} \approx 2$ μm [93]. For templates with length $L < l_{\mathrm{V}}$ and high aspect ratios, the molar flow of group-V species scales linearly with the template diameter d and pressure gradient but is inversely proportional to L [93]. The same relations hold for the vapor diffusion of the group-III precursor trimethylindium (TMIn) and its products after (partial) pyrolysis, with maximum diffusion length $l_{\mathrm{III}}^{\mathrm{max}} \approx l_{\mathrm{V}}^{\mathrm{max}}$ [93].
For high aspect templates, group-III precursors diffuse predominantly via surface diffusion. This diffusion mechanism does not solely depend on the template geometry as in the case of vapor diffusion, instead, the surface chemistry of the template plays an

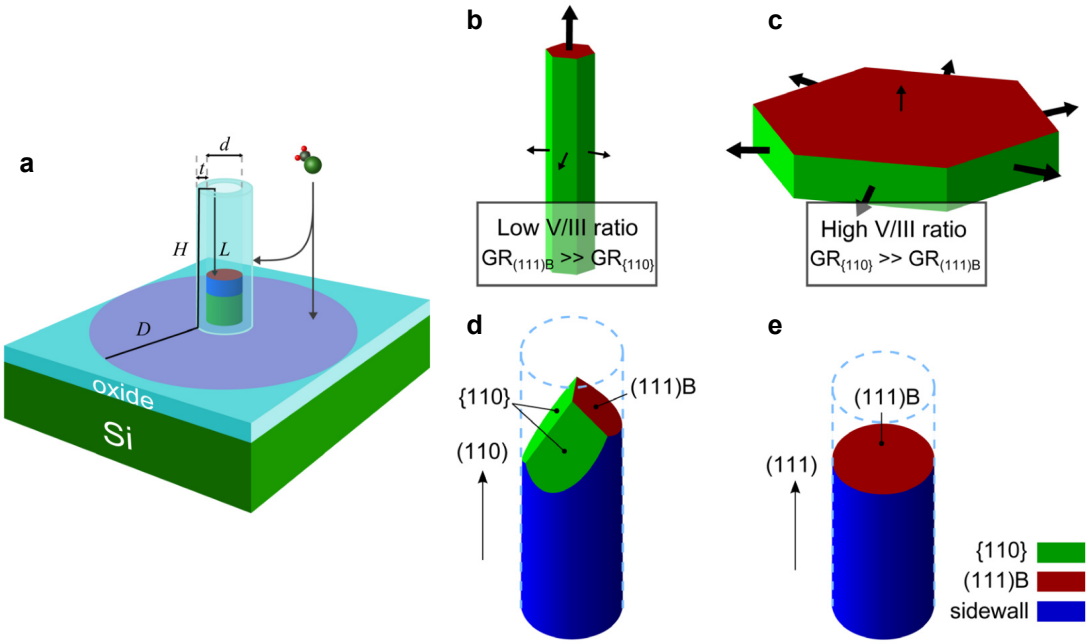

Figure 2.7. Growth mechanisms of TASE. a Schematic of a vertical TASE template with Si seed (green cylinder) and InAs nanowire stem (blue cylinder). Precursors reach the growth surface (red) via vapor diffusion (group III and V) and surface diffusion (group III). **b** Morphology of a nanowire grown at low V/III precursor ratio or high temperature. **c** Nanowire grown at a high V/III material ratio or low temperature. Growth of {110} facets dominates if the wire is not restricted by a template. **d,e** Typical facet morphology of wires grown at balanced conditions inside ⟨110⟩ and ⟨111⟩ aligned templates, respectively. Details are described in the text. Reprinted from [93], with the permission of AIP Publishing.

integral role. Precursor surface diffusion is characterized by an adsorption rate a_{ads} of a molecule onto the surface and a precursor surface migration length λ_{SD}. The latter translates into an effective precursor collection area $A(\lambda_{\mathrm{SD}})$ (purple circle in Fig. 2.7a). A precursor molecule that adsorbs to the surface within $A(\lambda_{\mathrm{SD}})$ can reach the growth front by means of surface diffusion [98, 99]. Hence, large a_{ads} and λ_{SD} increase the molar flow per area Φ_{SD} which reads [93]

$$\Phi_{\mathrm{SD}} = \frac{4a_{\mathrm{ads}}p}{RT}\left(\frac{A(\lambda_{\mathrm{SD}})}{d^2} + \frac{\lambda_{\mathrm{SD}}}{d}\right) \tag{2.25}$$

with $A = D^2 + 2(D+H)t + t^2$ and $\lambda_{\mathrm{SD}} = D + H + t + L$. The template dimensions are indicated in Fig. 2.7a. In the case of lateral templates, we can set $H = 0$. R, T, and p are the gas constant, temperature, and precursor species partial pressure in the vapor, respectively. The partial pressure p can be assumed constant outside the template but decreases inside the tube. From Eq. 2.25 we find that surface diffusion becomes more important as the template diameter d decreases. We stress that the opposite relation is

true for vapor diffusion discussed above. From these considerations we can summarize that:

- The effective V/III ratio inside high aspect ratio templates is lower than outside the templates and decreases further for longer and thinner templates (higher aspect ratio).
- The effective V/III ratio at the growth surface gradually increases as the nanowire progressively fills the template, because the effective aspect ratio decreases.

Figures 2.7b and c highlight the influence of the V/III ratio on the morphology of a nanowire grown in ⟨111⟩ direction without restriction by a template. At low V/III ratio (Fig. 2.7b), the growth rate of the (111)B facet exceeds that of {110} facets, resulting in a long and thin nanowire. This is attributed to low As-trimer formation (i.e. high number of In adsorption sites) on the (111)B facet while growth of {110} facets is limited by the As species flow [99, 100]. For high V/III ratio the situation is reversed and the lateral growth rate exceeds the axial one (Fig. 2.7c). The suppression of growth in ⟨111⟩ direction is caused by a high surface coverage with As trimers [101–103]. Similar morphology changes as shown in Fig. 2.7b and c are found for high and low growth temperature, respectively [93].
In templated growth where the wire diameter is restricted, such changes in V/III ratio are reflected in the top facet morphology. Balanced growth of (111)B and {110} facets (Fig. 2.7d) is typically observed for ⟨110⟩ aligned templates and a moderate V/III ratio of ~ 70. Lowering the V/III ratio (or increasing temperature) promotes growth of the (111)B facet and distinct {110} terminating facets are observed. Conversely, the {110} facets grow out at high V/III ratio (or low temperature) and a (111)B facet remains. Rotating the nanowire axis e.g. to ⟨111⟩ (Fig. 2.7e) changes this picture and a single (111)B facet often dominates for a wide growth parameter space.

In chapter 5 we will investigate in detail TASE growth of InAs as a function of crystal direction and implications of introducing metallic template segments, which give rise to intriguing epitaxy dynamics.

2.7. Properties of Lead Telluride

In the projects throughout this thesis we utilized a range of semiconductors. In this section we highlight the fundamental properties of lead telluride (PbTe), as its characteristics differ significantly from more established semiconductors like Si, InAs and InP. These properties will be elemental for the interpretation of our experimental results in chapter 6. Table 2.1 serves as a summary and point of comparison to Si, InP, and InAs.

PbTe is a relatively unexplored semiconductor that has recently received considerable attention from both experimental and theoretical side [73, 104–107], mainly due to its extreme material properties, which might prove advantageous in hybrid semiconductor-superconductor structures for quantum computing applications.

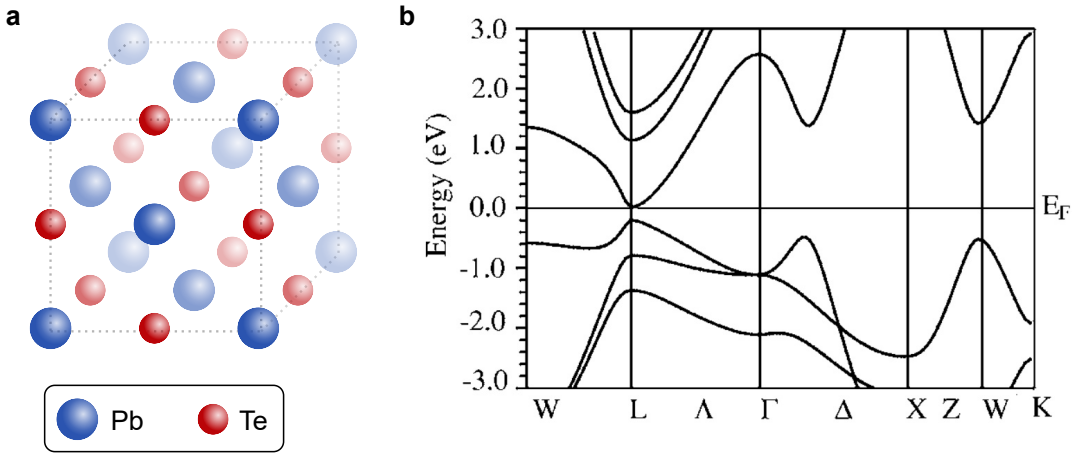

Figure 2.8. Properties of the PbTe crystal. **a** Rocksalt crystal structure of PbTe. **b** Dispersion relation of PbTe. Note the direct band gap of PbTe at the L-point of the Brillouin zone. Panel **b** reprinted with permission from [115]. Copyright (2006) by the American Physical Society.

PbTe is a group IV-VI semiconductor with a lattice constant of 6.439 Å [108]. Due to its rocksalt crystal structure (Fig. 2.8a), PbTe is mechanically softer than tetrahedrally bonded semiconductors and is chemically attacked by solvents routinely used in nano fabrication [109]. Both of these characteristics put important constraints on device fabrication (see section 3.3). Given that PbTe is composed of heavy elements in an inversion symmetric crystal lattice (Fig. 2.8a), strong Rashba and negligible Dresselhaus spin-orbit coupling is expected [107].
PbTe has a direct band gap [110] with four-fold degeneracy of the valence band valley, located at the L-point of the Brillouin zone (Fig. 2.8b), corresponding to the outer edge of the Brilloin zone in $\langle 111 \rangle$ direction. The valley degeneracy is lifted in strained PbTe epilayers and quantum wells [111] as well as in nanowires grown along specific crystal directions [107]. Compared to other semiconductors in Tab. 2.1, PbTe has a small band gap of $E_g = 0.19$ eV at low temperature [108, 112, 113] with a positive temperature coefficient $\mathrm{d}E_g/\mathrm{d}T > 0$ [114], opposite to the behavior observed in common semiconductors (see Tab. 2.1). Due to its small and direct band gap, PbTe finds use in opto-electronic applications such as infrared photon detectors and emitters [114]. The Fermi surfaces of PbTe are ellipsoids of revolution elongated along the $\langle 111 \rangle$ directions and the effective electron mass m^* is highly anisotropic with $m_L^* \gg m_T^*$ [113] (see Tab. 2.1). The valence and conduction bands of PbTe are almost mirror symmetric, consequently the effective longitudinal and transverse hole masses have values similar to their electron counterparts.

PbTe features an extraordinarily large dielectric constant with strong temperature dependence (Tab. 2.1). At low temperature it reaches $\varepsilon_r\,(T = 4\ \mathrm{K}) = 1350$ [114]. This behavior can be understood as a consequence of the rocksalt crystal structure of PbTe

Table 2.1. Bulk properties of important semiconductors. Comparison of material parameters of semiconductors used in this thesis. Values are cited from [125–127] (Si), [125, 127, 128] (InP), [125, 127] (InAs), and [108, 112–114, 117, 124, 129] (PbTe).

Parameter	**Si**	**InP**	**InAs**	**PbTe**
Group	IV	III-V	III-V	IV-VI
Crystal structure	diamond	zinc blende	zinc blende	rocksalt
Lattice constant a_0 (Å)	5.43	5.87	6.04	6.44
Position of band extrema				
valence band max.	Γ	Γ	Γ	L
conduction band min.	X	Γ	Γ	L
Energy gap E_g (eV)				
at 300 K	1.12	1.35	0.35	0.31
at 4 K	1.17	1.42	0.43	0.19
Dielectric constant ε_r				
at 300 K	11.9	12.6	15.2	414
at 4 K	12.1	11.8	14.6	1350
Effective electron mass				
m_L^*/m_e	0.91	0.080	0.026	0.223
m_T^*/m_e	0.19	(isotropic)	(isotropic)	0.027
g-factor	2.0	1.3	-15.3	15 to 60

which approaches a rhombohedral modification with ferroelectric properties at low temperature [116]. It is important to stress, however, that PbTe remains paraelectric without reaching the phase transition to ferroelectic behavior. We can illustrate this behavior by describing the temperature dependence of $\varepsilon_r(T)$ in terms of the Curie-Weiss law $\varepsilon_r(T) \propto C/(T-\theta)$. Here, C is a material specific constant and θ can be interpreted as an extrapolated negative Curie temperature of $\theta = -70$ K [117]. The unphysical negative value of θ is testament to the incomplete phase transition.
The large dielectric constant of PbTe has important implications for its transport properties. Scattering at ionized impurities is reduced compared to conventional III-V semiconductors, since random potential fluctuations are screened effectively [107, 111]. This allows for high electron mobilities reaching $\mu > 10^6$ cm^2/(Vs) in bulk-like PbTe epilayers on BaF_2 substrates [118, 119], without the need for elaborate modulation doping [120, 121]. Moreover, conductance quantization in PbTe quantum wells was observed despite high background impurity density, again due to reduced backscattering in the junction area [122]. A detailed discussion focused on the properties of PbTe nanowires can be found in a recent theoretical study [107]. The authors find that all valley degeneracies of bulk PbTe at the L-point are lifted for nanowires grown along certain crystallographic directions, and axial Landé g-factors range from 15 to 59, similar to findings in quantum wells [123] and bulk [124].

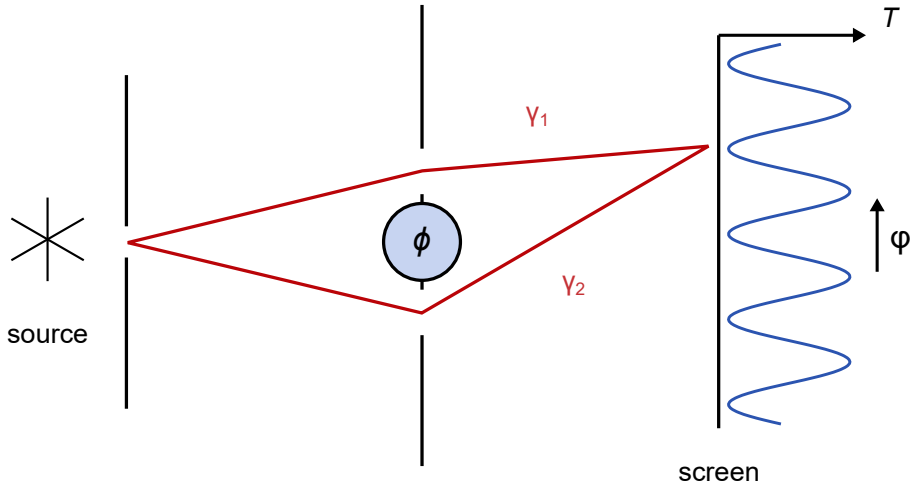

Figure 2.9. Schematic setup of the Aharonov-Bohm experiment. An electron is emitted from a source and reaches the screen via paths γ_1 and γ_2. The paths enclose a magnetic flux ϕ, but the electron travels on magnetic field-free trajectories. Figure inspired by [131].

2.8. Aharonov-Bohm Effect

The Aharonov-Bohm (AB) effect was theoretically predicted in 1959 [130] and constitutes the electronic analog to the double slit experiment in optics, highlighting the particle-wave duality of electrons. A schematic representation of the setup is shown in Fig. 2.9, where an electron traveling from a source to the screen can take two alternative paths denoted γ_1 and γ_2. The two paths enclose a localized magnetic flux ϕ. The electron trajectories lie in magnetic-field-free regions, therefore, electrons do not experience a Lorentz force. According to the prediction by Aharonov and Bohm, the electron picks up a phase difference $\Delta\varphi_{\mathrm{AB}}$ which is proportional to the line integral along the closed path $\gamma_1 - \gamma_2$ of the vector potential $\vec{A}$ [131]

$$\Delta\varphi_{AB} = -\frac{|e|}{\hbar}\oint \vec{A}\, d\vec{s} = -\frac{|e|}{\hbar}\int_{\vec{S}} \vec{\nabla}\times\vec{A}\, d\vec{S} = -\frac{|e|}{\hbar}\int_{\vec{S}} \vec{B}\, d\vec{S} = -\frac{|e|}{\hbar}\phi = -2\pi\frac{\phi}{\phi_0} \quad (2.26)$$

with the magnetic flux quantum $\phi_0 = h/e$. As indicated in Fig. 2.9, changing the magnetic flux is equivalent to moving the position of the detector on the screen, as both parameters modulate the phase difference between the paths γ_1 and γ_2.

To observe the AB effect experimentally, a few changes are made with respect to the theoretical proposal. First, γ_1 and γ_2 are defined by a confining potential, for example a semiconductor ring structure. Second, ohmic contacts on either side of the ring serve as electron source and detector. Third, a homogeneous magnetic field is applied perpendicular to the semiconductor ring such that the ring encloses a magnetic flux

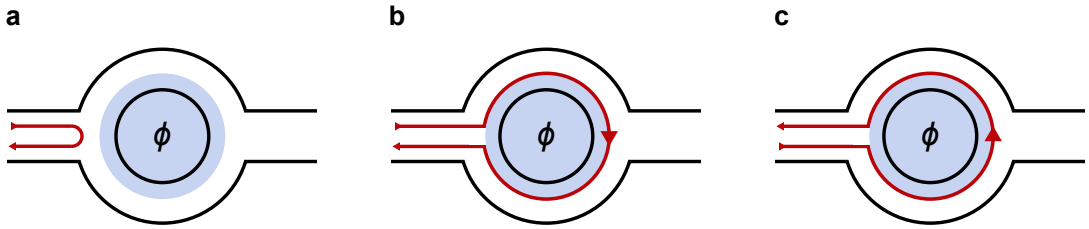

Figure 2.10. Lowest-order reflection terms in an Aharonov-Bohm loop. The loop is threaded by a flux ϕ and an incoming electron is reflected **a** at the entrance of the ring, **b,c** after traveling through the ring in clockwise or anticlockwise direction. Figure inspired by [131].

$\phi = S \cdot B$, where S is the ring area. The third condition causes the electrons to experience a Lorentz force when traversing the ring. We can neglect this contribution if we limit ourselves to a small magnetic field range, i.e. if the cyclotron radius $R_{\mathrm{cyc}} = \hbar k_F / eB$ is large compared to the ring radius.[5]
In the following, we assume that the leads are strongly coupled to the ring, i.e. that the transmission probability $T(E_{\mathrm{F}}) = 1 - R(E_{\mathrm{F}})$ is high because the reflection probability is $R(E_{\mathrm{F}}) \ll 1$. In this scenario we can describe the AB effects in terms of the three electron paths depicted in Fig. 2.10. In Fig. 2.10a the electron is reflected at the entrance of the ring. In Fig. 2.10b and c, the electron is reflected after traveling through the ring once in clockwise and anticlockwise direction, respectively. Considering only these three paths, we can express the reflection probability as [131]

$$\begin{aligned} R &= \left| r_0 + r_1 e^{i \cdot 2\pi\phi/\phi_0} + r_1 e^{-i \cdot 2\pi\phi/\phi_0} + \ldots \right|^2 \\ &= |r_0|^2 + 2\,|r_1|^2 + 4\,|r_0|\,|r_1| \cos\delta \underbrace{\cos\left(2\pi \frac{\phi}{\phi_0}\right)}_{\mathrm{AB}} + 2\,|r_1|^2 \underbrace{\cos\left(4\pi \frac{\phi}{\phi_0}\right)}_{\mathrm{AAS}} + \ldots \end{aligned} \tag{2.27}$$

where r_0 and r_1 are reflection probability amplitudes and δ is the phase that the electron wave accumulates when exploring the ring once at $B = 0$. The term denoted AB in equation 2.27 is modulated with the flux ϕ and has a periodicity of h/e. The AB term arises from interference between the path shown in Fig. 2.10a and the path of either Fig. 2.10b or c. The amplitude of AB oscillations may be reduced by the prefactor $|\cos\delta| \leq 1$. The phase δ depends e.g. on the microscopic details of the devices such as impurities and temperature. Owing to the prefactor, AB oscillations can show a maximum or a minimum at $B = 0$. The fourth term in equation 2.27 are the so-called Altshuler-Aronov-Spivak (AAS) oscillations [132]. They are $h/2e$-periodic and arise due to interference of the time reversed paths shown in Fig. 2.10b and c.

[5] With typical values from chapter 6 ($n_{\mathrm{e}} = 3 \cdot 10^{18}$ cm^{-3} and $B_\perp = 100$ mT) we obtain $R_{\mathrm{cyc}} = 2.9$ μm.

The AAS effect was experimentally confirmed [133] before the AB effect was observed [134–137], since AAS oscillations are more robust than AB oscillations against ensemble and energy (temperature) averaging as well as averaging due to multiple channels in the ring. This robustness is a consequence of time reversal symmetry of the interfering paths, which implies that the AAS amplitude does not depend on δ and consequently, the waves always interfere constructively at $B = 0$, resulting in a peak in resistance.
We make use of the robustness of AAS oscillations in our experiments discussed in chapter 6.

3 Sample Fabrication

3.1. Fabrication of Superconductor Nanowire Devices

In this section we review the fabrication of superconducting nanowire devices which we discuss in chapter 4. Parts of this section have been adapted from the methods sections of Refs. [138] and [139]. TiN layers used in this thesis were deposited by Amy Bowers, Dr. M. A. Mueed, Dr. Benjamin Madon, and Dr. Aakash Pushp at the IBM Almaden Research Center. Ti and Nb layers were deposited by Dr. Sean Hart and Dr. Pat Gumann at the IBM T. J. Watson Research Center.

Titanium Nitride Devices on Silicon

Gated TiN nanowires (NWs) were fabricated from 20 nm thick films of TiN which were deposited by DC reactive magnetron sputtering. The layers were sputtered on 1 inch Si wafers from which native oxide was stripped prior to metallization using a buffered hydrofluoric acid solution. The wafers were dehydrated at 180 °C for 5 minutes, then a 50 nm thick layer of hydrogen silsesquioxane (HSQ) based negative tone resist was spun, followed by exposure of both NW and gate structures using electron beam lithography (EBL). Wafers were immersed in AZ351B:H_2O (1:3) diluted developer for 150 s. The reaction was quenched by further diluting the developer with H_2O. Samples were swiftly transferred into acetone while still covered in water to avoid HSQ residues on the chip and then finally rinsed in isopropanol (IPA) and blow dried with N_2. TiN areas not protected by the HSQ mask were removed by inductively coupled plasma (ICP) etching for 12 s in an HBr plasma. After etching of TiN, HSQ was removed by immersion in a diluted hydrofluoric acid solution (20:1) for 12 s. After the TiN layer was structured, Ti/Au bonding pads were defined using optical lithography. For this purpose, the wafer was dehydrated at 180 °C for 5 min, a thin layer of HMDS adhesion promoter was deposited, structures were exposed on a double layer of LOR5B and AZ1505 resist, and development was performed in AZ400K:H_20 (1:4) for 45 s. Then, 10 nm of Ti plus 150 nm of Au were evaporated and lift-off was performed in hot DMSO ($T \approx 120$ °C), followed by rinsing in acetone and IPA. To ensure good electrical contact between Au bonding pads and devices, the wafers were immeresed in BHF for 5 s prior to evaporation to etch potential surface oxides formed on TiN.

Each 1 inch wafer hosted 144 NW devices. The optical image in Fig. 3.1a shows an array of 4 fully processed devices, a zoom-in on a device similar to that of Fig. 4.11a is shown in Fig. 3.1b. The device features four contact and three gate pads. Wafers were diced into 5.5 mm × 5.5 mm chips, glued onto a QDevil daughter board with polymethyl

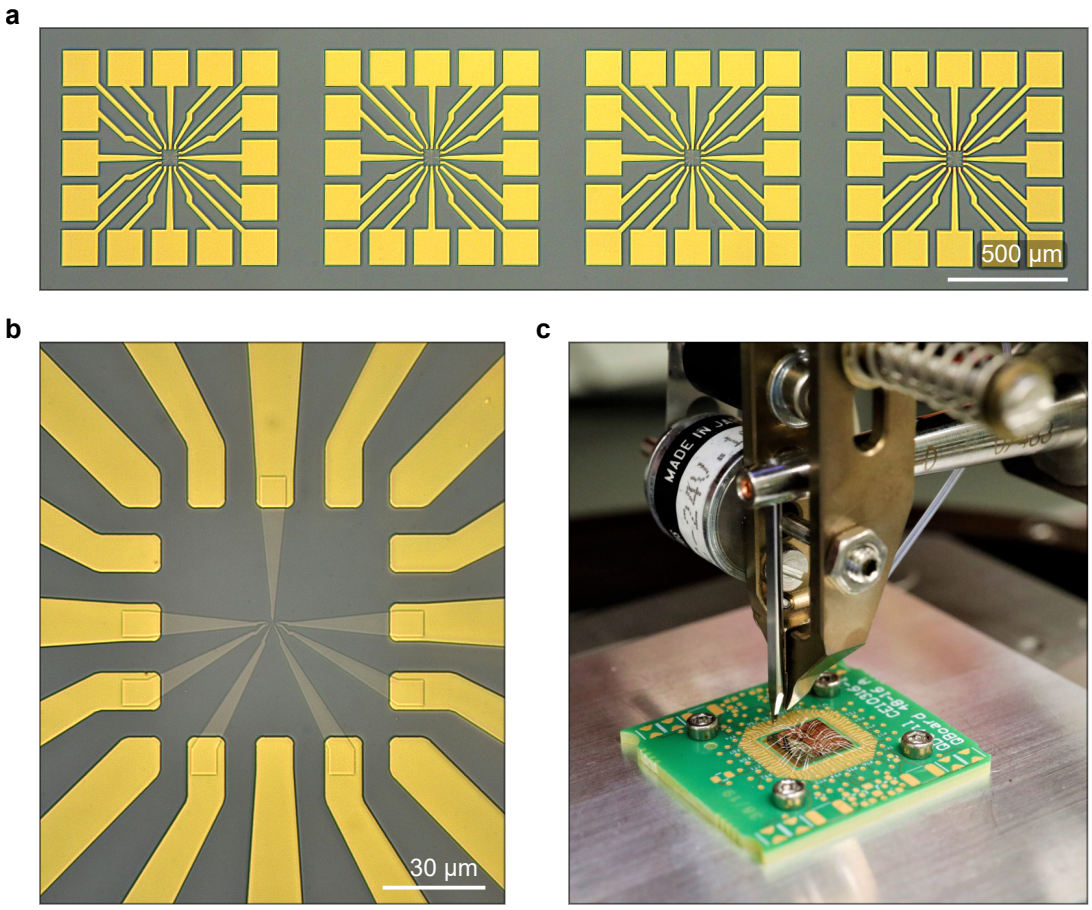

Figure 3.1. Superconducting nanowire device fabrication. a Optical microscopy image of four nanowire devices (center), surrounded by Au bonding pads (yellow). **b** Detailed view of a nanowire with four contact pads, two pads for remote gates and one pad for a direct injection gate. All pads are contacted using optical lithography, Ti/Au evaporation and lift-off. **c** Device bonding after the chip was diced and mounted onto a daughter board.

methacrylate (PMMA) and wire-bonded using a wedge to wedge semi-automatic wire bonder (see Fig. 3.1c).
The above fabrication procedure was performed on both high resistivity ($\sim$ 10 kΩ cm) and low resistivity ($\sim$ 10 Ω cm) Si. At temperatures below 100 K, device performance in terms of gate currents vs. gate voltages was similar for both substrates.
Characterization of the TiN film gave a resistivity of 68 Ω per square, a critical temperature of 3.5 K and a critical out-of-plane magnetic field of 3.5 T. These properties remained unchanged in the completed devices.
Measurements presented in Fig. 4.3a and b were performed on TiN wires that were fabricated on a Si substrate with a 25 nm thermally grown SiO_2 top layer. All other

processing steps remained the same as outlined above.

Trench Fabrication

Some devices (e.g. Fig. 4.12a) were further processed after deposition of the Au bonding pads. In this case, a 2 nm SiN_x layer was first deposited by atomic layer deposition (ALD) to protect TiN structures from consecutive processing steps (see discussion in section 5.2.7). Second, a 210 nm SiO_2 hard mask was deposited with plasma enhanced chemical vapor deposition (PECVD). A 190 nm layer CSAR AR-P 6200.09 positive tone resist was then spun and trench structures were exposed with electron beam lithography. Patterns needed to be aligned manually using nearby devices, since no alignment markers were fabricated in previous steps. After standard development in AR600-546, rinsing in IPA and post bake at 130°C for 1 min, the SiO_2 hard mask was patterned using reactive ion etching (RIE) with CHF_3 and Ar (etch rate 16 nm/min). Structures were overetched by 50% to account for both the high aspect ratio of the resist pattern and the thin SiN_x layer. Without removing the resist, a 510 nm deep trench was etched into the Si substrate using ICP etching in an HBr plasma (etch rate 120 nm/min). The etching removed the CSAR resist and thinned down the hard mask. The latter was stripped together with the SiN_x protection layer by immersion in BHF for 90 s.

Titanium Device Fabrication

Titanium wires were defined by EBL on a positive tone PMMA double layer mask, electron beam evaporation of a 30 nm thick Ti film and lift-off. Ti evaporation was performed at a base pressure of 10^{-9} mbar and at a deposition rate of 1 nm s^{-1}. The high deposition rate was chosen to minimize contamination of the Ti film during evaporation [140]. The Ti wire of Fig. 4.3(c) had a critical temperature of 220 mK, a normal state resistance of 74 Ω and a retrapping current of 560 nA.

Niobium Device Fabrication

Nb wires were obtained by sputtering of a 13.5 nm film on intrinsic Si substrates and device patterning similar to that described above for TiN. ICP etching of regions not protected by the HSQ mask was performed using an Ar/Cl_2 plasma. The Nb wire of Fig. 4.3(e) had a normal state resistance of 655 Ω and a retrapping current of 7.6 μA. Since Nb forms a non self-terminating oxide in air [141] and several days passed between deposition and device measurement, the actual thickness of the Nb devices was likely lower than the nominally sputtered thickness.

3.2. Hybrid-TASE Device Fabrication

In this section we focus on some aspects of hybrid-TASE fabrication that were not described in detail in Ref. [142] (see also sections 5.1.3 and 5.1.9). In particular, we review the marker fabrication procedure and discuss details of InAs epitaxy.

3.2.1. Marker Fabrication

InAs epitaxy experiments performed in the framework of this thesis were based on 8 inch (100) and (110) silicon-on-insulator (SOI) wafers. The thickness of the Si top layers ranged between 30 nm and 70 nm. Results discussed in chapter 5 were obtained on 70 nm Si layers with (110) orientation. 8 inch wafers were diced into five 6.2 cm×6.2 cm wafers, schematically indicated in Fig. 3.2a together with the main crystal directions. A schematic cross-section is shown in Fig. 3.2b. In the first fabrication step (Fig. 3.2c), a 30 nm SiO_2 layer was deposited using PECVD at 300°C, followed by sputtering of a 100 nm thick W layer and exposing the marker pattern on an AR-N 7520.17 negative tone resist (Fig. 3.2d). The detailed parameters of the resist development were crucial, since the alignment accuracy of all following exposures relied on this pattern. Development for 14 min in AR 300.47:H_2O (4:1) diluted developer under continuous agitation of the solution resulted in the most sharply defined resist structures.[1] To ensure that small structures in the 430 nm thick resist were not washed off during development, a surpass adhesion promoter was applied prior to resist spinning. The marker pattern was transferred into the W layer via RIE using N_2/SF_6 plasma (etch rate 18 nm/min). The SiO_2 layer served as etch stop and protected the thin Si layer. The resist mask was stripped in acetone and IPA, the wafer was thoroughly rinsed in H_2O and exposed to an aggressive 600 W O_2 plasma to remove organic residues (Fig. 3.2e). The W markers were then encapsulated in a 300 nm thick SiO_2 layer deposited via PECVD at 400°C using tetraethyl orthosilicate (TEOS) as precursor. Wafers were annealed for 30 s at 750 °C in Ar/H_2 atmosphere and optical lithography was performed with AZ6612 resist and development in AZ400K:H_2O (1:4) to define device areas (Fig. 3.2f). After etching unprotected regions of the 330 nm SiO_2 layer in BHF (etch rate 1.7 nm/s), the resist was stripped in acetone and IPA. Finally, wafers were cleaned in 600 W O_2 plasma and hot concentrated piranha $H_2SO_4 : H_2O_2$ (2:1) ($T \approx 120$°C) for 10 min. A schematic of the encapsulated W markers together with the exposed Si regions (device areas) is presented in Fig. 3.2g.

The photograph of a wafer with markers and exposed device areas is shown in Fig. 3.3a. Each wafer consisted of nine 2 cm × 2 cm chips and a 1 mm frame to facilitate wafer handling. Figure 3.3b is an optical microscopy image of the bottom-right corner of one 2 cm × 2 cm chip. Indicated are (i) dice marks, (ii) alignment markers for optical lithography, and (iii) arrays of EBL markers. A large area of the thick SiO_2 layer was etched in the center of each chip (iv). This allowed us to perform ellipsometry measurements on processed wafers and chips. The chips consisted of four quadrants, each with an array of 32 device areas (v). Figure 3.3c shows a magnified view of such an array. The top Si layer is exposed in the blue regions, devices were fabricated in small squares (v) in the centers of the structures. Orange regions are covered by the 330 nm SiO_2 layer protecting the alignment markers.

We discuss all consecutive steps of the hybrid-TASE process, such as fabrication of

[1] Development in concentrated developer for 210 s gave similar results but was less controlled due to the rapid development.

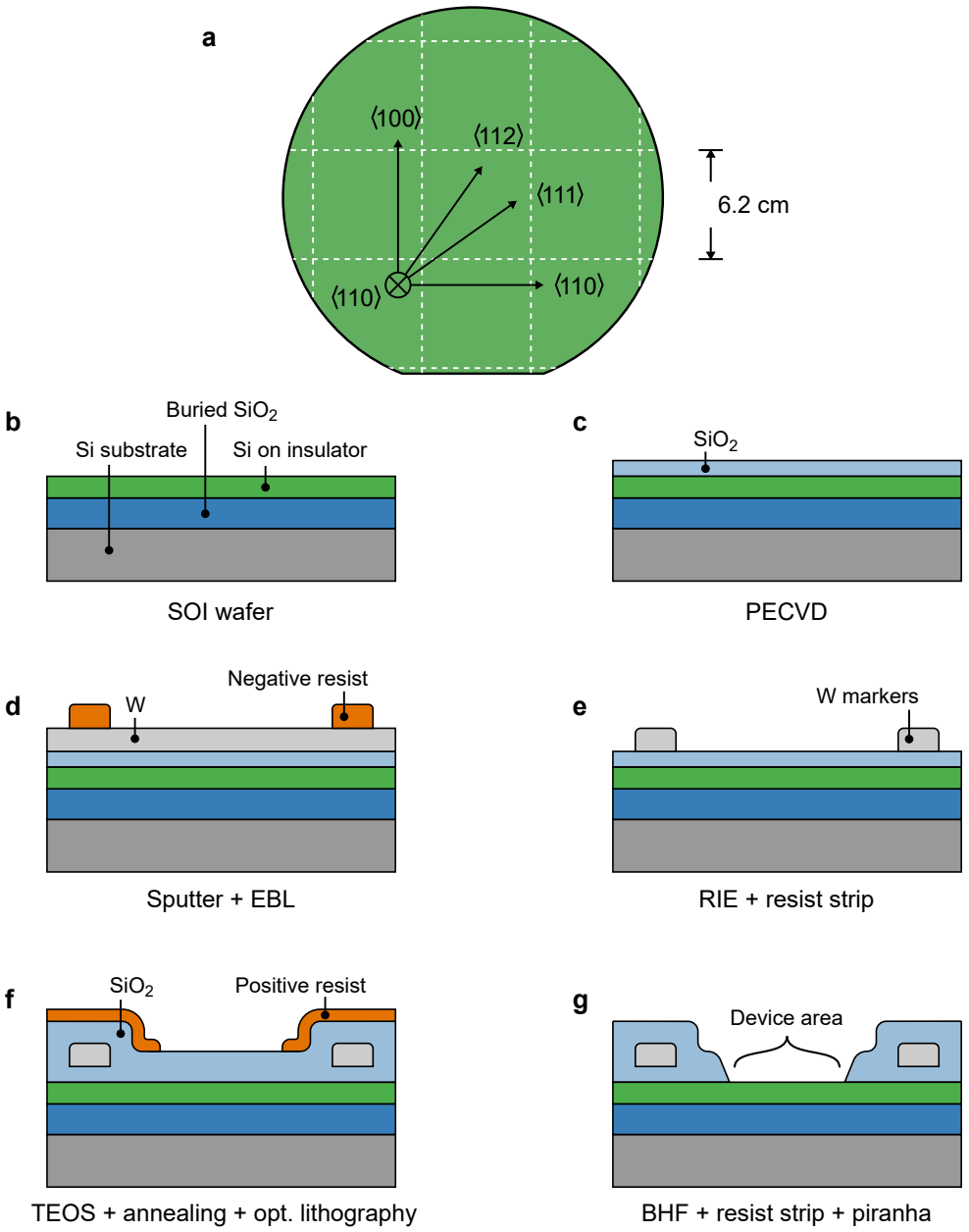

Figure 3.2. Marker fabrication for hybrid-TASE. **a** Schematic of an 8 inch (110) wafer with dice lines indicated. **b** Schematic cross-section of a 6.2 cm×6.2 cm wafer after dicing. **c** Deposition of a 30 nm SiO_2 etch stop layer. **d** Sputtering of a 100 nm W film and patterning of markers into a negative resist using EBL. **e** Transfer of marker pattern into W with RIE etching. **f** Encapsulation of markers in SiO_2 and definition of device areas via optical lithography. **g** BHF etching of SiO_2 to expose the top Si layer in device areas.

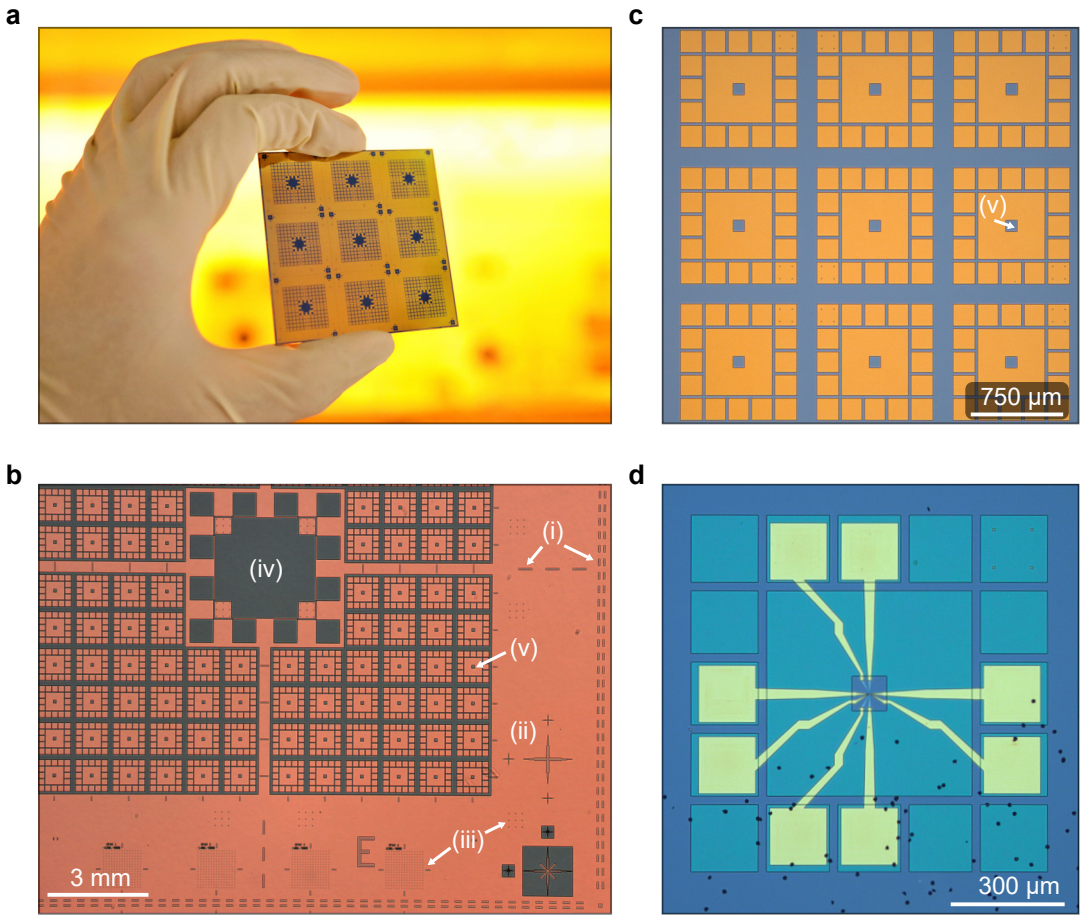

Figure 3.3. Lithography markers for hybrid-TASE and device contacting. a Photograph of a wafer after marker patterning and exposing device areas. Each wafer hosts nine 2 cm×2 cm chips. **b** Optical microscopy image of the corner of a 2 cm×2 cm chip with (i) dice marks, (ii) optical alignment markers, (iii) EBL alignment markers, (iv) large exposed Si area in the center of the chip, and (v) device areas. **c** Zoom-in on an array of nine structures that can host devices (in the centers) and bonding pads (surrounding squares). Regions where the top Si layer is exposed appear blue, areas covered with a 330 nm SiO_2 layer are orange. **d** Optical microscopy image of a final hybrid-TASE QPC (see Fig. 5.5a) including Au contacts, gates, and bonding pads. Black spots are parasitic InAs crystals.

templates in the predefined device areas, as well as InAs epitaxy in our publication [142], which we reprint in chapter 5. The (macroscopic) device geometry of a completed device is highlighted in the optical microscopy image of Fig. 3.3d showing a device similar to that of Fig. 5.5a. Gates and contacts were fabricated with EBL, Ti/Au evaporation and lift-off. Note that the large bonding pads sit on top of squares of 330 nm thick SiO_2. This geometry prevented unintentional contacting of the Si handle wafer during

bonding. Black spots in Fig. 3.3d are parasitic InAs crystals. Important aspects of the growth selectivity are discussed in section 5.3.2.

3.2.2. Metal-Organic Chemical Vapor Phase Epitaxy

MOVPE was performed in a Veeco P-125 system (Fig. 3.4a) operated at a pressure of 80 mbar. Precursors trimethylindium (TMIn) and tertbutylarsine (TBAs) were extracted from temperature controlled bubblers and using hydrogen as carrier gas. Epitaxy experiments were performed in a temperature range from 540 °C to 600 °C, placing growth in the mass transport limited regime (see section 2.6.2). Temperature was controlled by manually setting heater currents as this was found to give the most reproducible results. Precursor material flows ranged from 1.9 to 4.6 μmol/min (TMIn) and 137 to 704 μmol/min (TBAs) with V/III ratios between 70 and 150. Chips were annealed at 600 °C for 300 s in As atmosphere before epitaxy was initiated. Higher temperatures were avoided to minimize TiN degradation in hybrid templates (see section 5.2.7). Growth times to obtain $\sim$ 1 μm long nanowires ranged from 500 s to over 2 hours. This large range underlines the high growth rate dependence on template aspect ratio and template material. SiO_2 templates with highest aspect ratios fabricated from wafers with 30 nm SOI layer required the longest growth time (see discussion on aspect ratio dependent growth rate in section 2.6.2). Growth rates were highest inside templates based on 70 nm SOI wafers (see e.g. section 5.1.5) and further increased in templates with integrated TiN elements. A detailed discussion of this observation can be found in section 5.2.2.
During growth, chips were mounted on a rotating susceptor plate. In early experiments, chips were lost in the reactor because the graphite sample holders used to accomodate 2 cm $\times$ 2 cm chips in 2 inch susceptor pockets were not suitable for 740 μm thick samples. We solved this issue by designing a thicker graphite holder (Fig. 3.4b) with additional flaps (yellow arrows) to lock chips in place on the spinning susceptor.

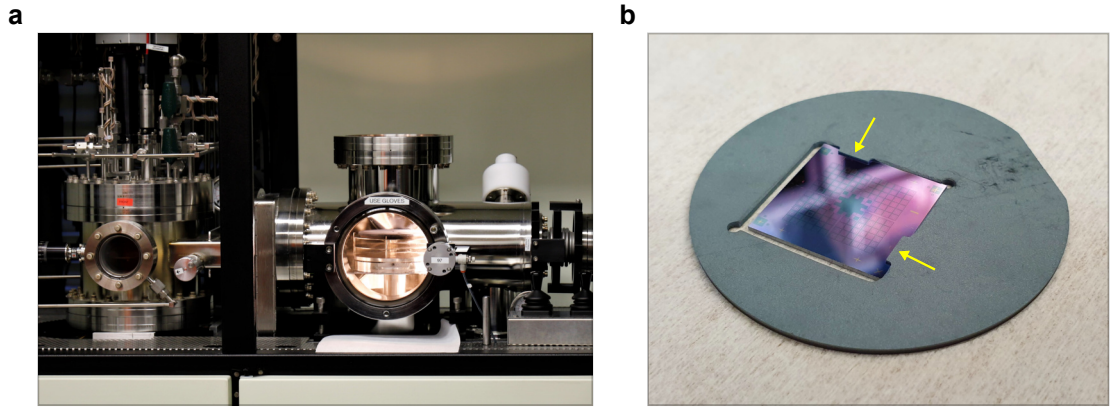

Figure 3.4. Growth reactor and graphite sample holder. a MOVPE growth chamber (left) and sample load lock (right, illuminated). **b** Custom graphite sample holder to accommodate 2 cm×2 cm chips in 2 inch wafer pockets. Slightly overlapping flaps (yellow arrows) were designed to lock chips in place on the rotating susceptor.

3.3. Fabrication of Lead Telluride Devices

In chapter 6 we discuss transport measurements on PbTe nanostructures selective-area-grown on InP (111)A. The growth was developed and performed by Jason Jung and Alexander G. Schellingerhout in the group of Prof. Erik P.A.M. Bakkers at TU Eindhoven. Figure 3.5 gives a brief overview of wires grown with this method. Amorphous SiN_x served as a growth mask and PbTe nanowires were grown with MBE inside trenches along the $\langle 110 \rangle$ and $\langle 112 \rangle$ directions (Fig. 3.5a). Figure 3.5b shows a bright-field HRTEM cross-sectional view of a nanowire grown along the $[01\bar{1}]$ direction. The crystal exhibits distinct faceting and a flat InP/PbTe interface. Devices investigated in this thesis were grown within a short time of 10 minutes, in which case the crystal did not laterally expand significantly beyond the mask openings (Fig. 3.5b). Further details about the selective-area-growth of PbTe can be found in [143, 144].

In the collaboration between the Eindhoven group and our team at IBM, we investigated PbTe nanowires and networks grown on 5 mm × 5 mm chips (Fig. 3.6a). A major challenge of the project consisted in handling and processing of the chips without damaging PbTe. In particular, wires were repeatedly damaged during shipping and standard chemicals such as H_2O, HF, TMAH, and DMSO were found to damage the wires. To reduce the risk of material degradation, chips were shipped in Ar atmosphere and stored in vacuum-sealed bags in a freezer at $T = -20$ °C.
The fabrication recipe for device contacts and gates was developed with these constraints in mind. For contacts fabrication, a PMMA double layer resist (AR-P 669.04, 206 nm and AR-P 672.02, 54 nm) was spun and baked at 180 °C. Contacts were exposed using EBL, followed by development in MIBK:IPA (1:2) and rinsing in IPA. Figure 3.6b shows the optical microscopy image of a chip at this fabrication stage. Chips featured 6 device

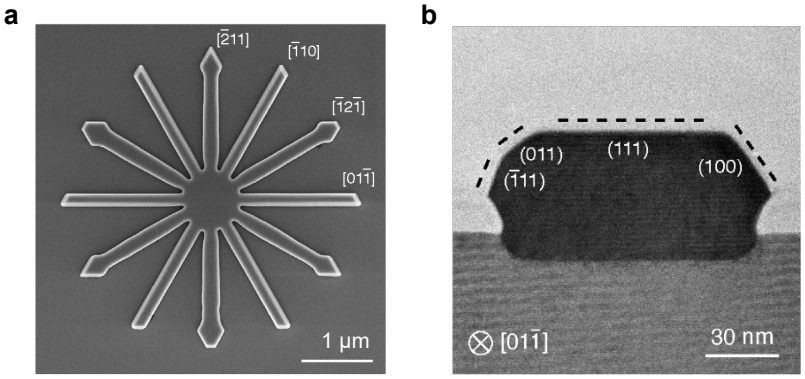

Figure 3.5. Selective-area-growth of PbTe on InP. a SEM micrograph of a selective-area-grown PbTe network on InP (111)A. Crystal directions are indicated. **b** HRTEM cross-section of a PbTe nanowire after 10 minute growth. The nanowire axis points along the $[01\bar{1}]$ direction. Image credit: Jason Jung and Alexander G. Schellingerhout, TU Eindhoven. Figure adapted from [144].

areas hosting 25 devices each and sufficiently spaced to accommodate bonding pads. Native oxides of PbTe were etched by *ex-situ* RIE Ar sputtering at a power of 100 W for 12 s. After swiftly transferring the chip into an electron-beam evaporation chamber, 5 nm Ti and 50 nm Au were evaporated.[2] Lift-off was performed in acetone for ∼8 hrs at room temperature. On devices featuring top gates, a 23 nm Al_2O_3 layer was deposited using thermal atomic layer deposition at 110 °C, followed by EBL, evaporation, and lift-off with the same parameters as for contacts fabrication. Figure 3.6c shows an optical microscopy image of a device area after contacts and gates fabrication. A zoom-in on the device array is presented in Fig. 3.6d. The array hosts 5×5 devices with wires along $[01\bar{1}]$ and $[\bar{1}2\bar{1}]$ directions in the first two columns, ring structures in the third column, and Hall bar structures along $[01\bar{1}]$ and $[\bar{1}2\bar{1}]$ directions in the fourth and fifth column, respectively. Continuous wires without obvious defects were selected by SEM imaging, then contacts and gates were designed specifically for the selected devices. In the example of Fig. 3.6d, contacts and a top gate were fabricated on two nanowires and one Hall bar. High-resolution SEM images of finished devices are presented in chapter 6 alongside the corresponding transport data.

[2]Initially, sputter-cleaning was performed using an Ar gun fitted to the chamber of our evaporator. On devices processed in this way, lift-off of small features was prevented by extensive formation of lift-off ears. By performing tests with a plethora of substrates, lift-off parameters, and seven different (double layer) resist stacks, we verified that lift-off ears were correlated to the *in-situ* sputtering step. Cross-sectional SEM imaging of resist gratings revealed that resist side-walls were rounded during etching, causing the evaporated metal layers to be continuous across the resist step. This finding can be attributed to the shallow incidence angle of Ar ions with respect to the substrate in our evaporator. The vertical *ex-situ* sputtering approach described in the text was chosen to avoid such complications.

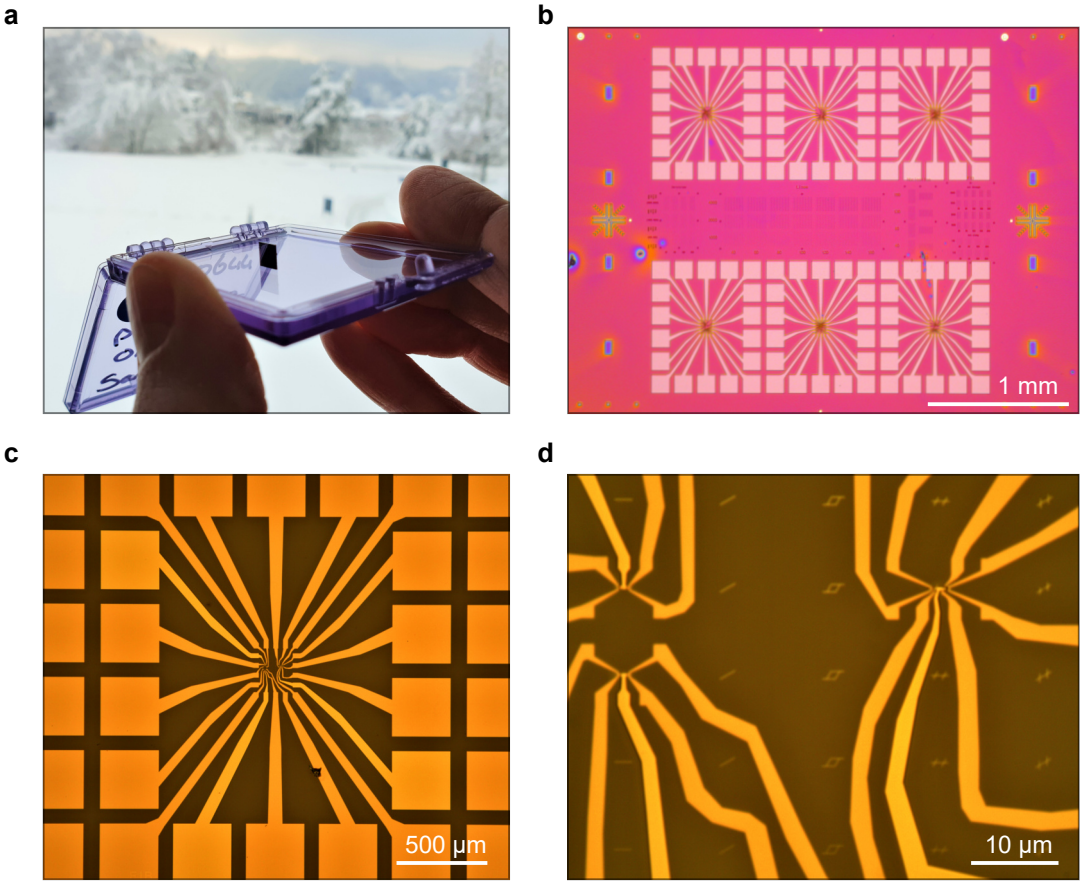

Figure 3.6. PbTe device fabrication. a 5 mm×5 mm InP chip with selective-area-grown PbTe structures arriving in our lab literally 'on the edge'. Snowy Albis mountains in the background. **b** Optical microscopy overview image of the chip after development of a PMMA double layer resist for contacts patterning. The chip features six device areas surrounded by bonding pads. **c** Optical microscopy image of one device area after fabrication of contacts and top gates via lift-off. **d** Detailed view of the device array in the center of **c**. Contacts and gates are patterned on selected devices after screening the chip using SEM. Details are described in the text.

4 Gated Superconducting Nanowire Switches

"You will observe with concern how long a useful truth may be known, and exist, before it is generally received and practiced on."

Benjamin Franklin (1706-1790)

The conductivity of metals subject to high electric fields has been studied for more than a century [145, 146]. Since metals have a high electron density of $n_e \sim 10^{23}$ cm^{-3} [20], the space charge region formed at the metal surface in high electric field is only a few atomic layers thin [147]. In bulk samples, this change in electron density is immeasurably small [146]. Therefore, gating experiments are typically performed on metal thin films [145–150] where the surface area is maximized while the number of bulk electrons is minimized. This approach, in combination with ionic liquid gating [147, 151, 152] which is used to create sufficiently high electric fields (>150 GVm^{-1}), can result in a measurable change in conductivity [151].
A range of normal metals [145–150] and superconductors [150–152] was investigated using these methods. In normal metals, a field-induced resistance change on the order of one percent was typically found and the critical temperature in superconductors could be tuned by a similar magnitude. Important characteristics of the small gating effect depended on details of the gate interface [149] and, crucially, on the metal used. Some metals exhibited an increase in resistance when a negative voltage was applied to the gate, while others showed opposite behavior [148, 150]. Similar material dependent effects were observed in superconducting devices, since the direction of T_C change for a given gate polarity depended on the superconductor used [150].
These findings led to the conclusion that the observed gating was dominated by interface effects such as scattering at the thin depletion layer [147], while the bulk remained unaffected by high electric fields.
This generally accepted notion was called into question by a recent study [153] where superconducting nanowires were switched to the normal state by application of a modest side gate voltage. The authors assigned this tunability of I_C to a novel gating effect in superconductors. Owing to the wide range of applications for such simple, all-metallic, and field-resilient superconducting switches, a large number of experimental [153–167] and theoretical [168–173] studies followed. The effect was reproduced on a wide range of device geometries and materials; however, key observations such as the ambipolar

suppression of I_C and spatial dependence of the effect were not explained.

At the time of this debate, our interest in the topic was sparked while working with high-quality TiN thin films on Si substrates for the project that will be presented in chapter 5. We fabricated TiN nanowires and found a similar phenomenology. However, our experiments revealed that the quench of superconductivity is not related to electrostatic gating. Instead, superconductivity is effectively quenched by few high-energy electrons and phonons.
In sections 4.1 to 4.4 we present our publications [138, 139] which elucidate these mechanisms in detail. In section 4.5 we directly compare our results to work claiming electrostatic gating and review recent publications that support our interpretation. Finally, we summarize our conclusions and discuss their implications for future device applications in section 4.6.

Sections 4.1, 4.2, 4.3, and 4.4 are adapted from the publications:

A superconducting switch actuated by injection of high-energy electrons
M. F. Ritter, A. Fuhrer, D. Z. Haxell, S. Hart, P. Gumann, H. Riel, and F. Nichele
Nature Communications **12**, 1266 (2021).

Author contributions: F.N. conceived the experiments. A.F. and F.N. designed the samples. S.H and P.G. deposited the Ti and Nb films. M.F.R. and D.Z.H. fabricated the devices. M.F.R., A.F., D.Z.H. and F.N. performed the measurements. M.F.R., A.F., D.Z.H, H.R. and F.N. interpreted and analyzed the data. A.F. and F.N. wrote the manuscript.

Out-of-equilibrium phonons in gated superconducting switches
M. F. Ritter, N. Crescini, D. Z. Haxell, M. Hinderling, H. Riel, C. Bruder, A. Fuhrer, and F. Nichele
Nature Electronics **5**, 71-77 (2022).

Author Contributions: A.F. and F.N. conceived the experiments. M.F.R. and A.F. designed and fabricated the samples. N.C. and A.F. performed simulations of the electric field magnitude. M.F.R., M.H., and F.N. performed the measurements. D.Z.H. and C.B. fitted the switching probability data. All authors analyzed and interpreted the data and contributed to the writing of the manuscript.
This publication was featured on the cover of Nature Electronics, Volume 5, Issue 2, February 2022 (see Appendix A).

4.1. Publication I: A Superconducting Switch Actuated by Injection of High-Energy Electrons

4.1.1. Abstract

Recent experiments with metallic nanowire devices seem to indicate that superconductivity can be controlled by the application of electric fields. In such experiments, critical currents are tuned and eventually suppressed by relatively small voltages applied to nearby gate electrodes, at odds with current understanding of electrostatic screening in metals. We investigate the impact of gate voltages on superconductivity in similar metal nanowires. Varying materials and device geometries, we study the physical mechanism behind the quench of superconductivity. We demonstrate that the transition from the superconducting to resistive state can be understood in detail by tunneling of high-energy electrons from the gate contact to the nanowire, resulting in quasiparticle generation and, at sufficiently large currents, heating. Onset of critical current suppression occurs below gate currents of 100 fA, which are challenging to detect in typical experiments.

4.1.2. Introduction

Superconducting circuits, thanks to their ultra-low power consumption and high speed, offer great promise as building blocks for quantum computing architectures and related cryogenic control electronics. In this context, it is especially intriguing to develop switching devices that can be electrically tuned between a superconducting and a resistive state at high frequency. Ultimately, such a three-terminal device would enable novel functionalities for which no semiconducting counterpart exists, such as cryogenic switches, ultra sensitive detectors, amplifiers, circulators, multiplexers and frequency tunable resonators [174–181]. Several electrically controlled superconducting switches based on the injection of out-of-equilibrium quasiparticles in Josephson junctions have been realized [182–185]. However, Josephson junctions typically come with limited source-drain critical currents and the requirement to operate in magnetic field free environments. Consequently, architectures which do not rely on Josephson junctions are subjected to intense study. Such pioneering approaches are based on three or four terminal devices where electrical currents [186], locally generated Oersted fields [187] or heat [188–190] drive a superconducting channel normal. Finally, recent experiments suggest that moderate electric fields might affect superconductivity in metallic nanowires [153, 157]. Controlling superconductivity in metallic devices via gate voltages would be appealing, however a satisfactory explanation for the observed phenomena was not yet provided.

Here we report an experimental investigation of metallic nanowires subjected to electric fields. Our findings rule out any variation of superconducting properties as a direct consequence of the applied electric field, as suggested in Refs. [153, 157]. On the other hand, we highlight the importance of tunneling and field emission from the gate electrode. Detailed measurements indicate that relatively few electrons, injected at energies several orders of magnitude higher than the superconducting gap, trigger the genera-

tion of a large number of quasiparticles and weaken superconductivity. This is in stark contrast to previously demonstrated devices actuated by quasiparticle injection at low energy [183, 188, 190], where gate currents comparable to the device critical current (a few μA) were needed for switching. For larger gate currents, injected electrons locally increase temperature and drive the nanowires normal. We characterize the effect of electron injection into nanowires in terms of their critical current and its dependence on gate voltage, temperature and magnetic field. This basic characterization is performed with different substrates and superconductors. We then investigate how injected quasiparticles influence superconductivity along the length of the channel in a region free of electric fields. After presenting the experimental observations, we will elaborate on their physical origins.

4.1.3. Basic Characterization

A typical device is shown in Fig 4.1a together with its measurement setup: it consists of a 2 μm long, 80 nm wide TiN wire (blue) with a TiN side gate (red). Wire and side gate are separated by an 80 nm wide gap. Gates and nanowires were defined by electron beam lithography and dry etching of a TiN film deposited on an intrinsic Si substrate (gray). Measurements were performed by low-frequency lock-in techniques by passing a source-drain current I_{SD} in the nanowire and recording the resulting voltage V. A gate voltage V_{G} was applied via a source-measure unit, which also recorded the current I_{G} entering the gate contact. A second side gate (gray) was not operated in this work and left grounded. Further details on materials, samples fabrication and measurement techniques are reported in sections 3.1 and 4.1.8. At $V_{\mathrm{G}} = 0$, the nanowire showed a critical current $I_{\mathrm{C}} = 45$ μA, measured sweeping I_{SD} in either direction starting in the superconducting state. In contrast, when sweeping I_{SD} from the normal state towards zero, superconductivity was re-established below the retrapping current $I_{\mathrm{R}} = 1$ μA. Figure 4.1b shows the nanowire differential resistance dV/dI_{SD}, measured while sweeping I_{SD} in the positive direction. The inset gives the temperature dependence of I_{C} and I_{R}. The large difference between I_{C} and I_{R}, especially marked at low temperature, is likely due to self-heating when the nanowire is in the normal state, together with the difficulty in extracting heat via the substrate or the leads [191]. Figures 4.1c and d show I_{C} and I_{G}, respectively, as a function of V_{G}. For $V_{\mathrm{G}} \sim \pm 2.5$ V, just before I_{G} reached detection level (~ 100 fA in our setup), I_{C} started decreasing. At $V_{\mathrm{G}} = \pm 5.5$ V, where $I_{\mathrm{G}} \approx \pm 1.5$ nA, I_{C} vanished and the nanowire reached its normal state resistance $R_{\mathrm{N}} = 1.6$ kΩ. The parametric plot of I_{C} vs. I_{G} shown in Fig. 4.1e indicates an extremely sharp suppression of I_{C} for small values of I_{G} (about 50% of the suppression took place within the noise level for I_{G}), followed by a slower decay which persisted up to $I_{\mathrm{G}} \sim 1.5$ nA.

4.1.4. Temperature and Magnetic Field Dependence

Figure 4.2a and b show the gate voltage dependence of I_{C} for various temperatures T and out-of-plane magnetic fields $B_{\perp}$, respectively. Neither temperature nor field affected the I_{G} vs. V_{G} characteristics of Fig. 4.1d (see section 4.2.2), and resulted in identical

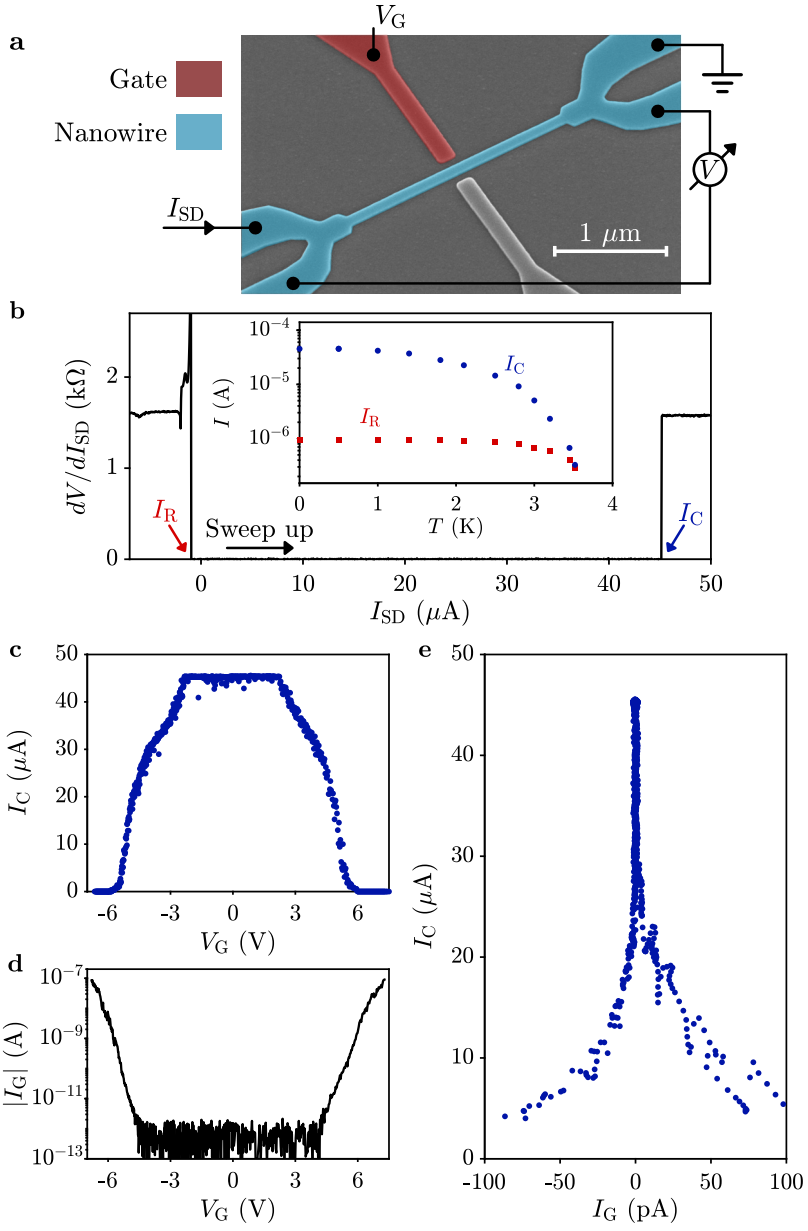

Figure 4.1. Operation of a metallic nanowire superconducting switch. **a** False color scanning electron micrograph of a device identical to that under study, together with a schematic of the measurement setup. The silicon substrate is gray, the TiN nanowire blue and the gate electrode red. A second gate electrode (gray) was left grounded. **b** Differential resistance dV/dI_{SD} of the nanowire as a function of I_{SD}, measured by sweeping up I_{SD} starting from -50 μA. Critical current I_C and retrapping current I_R are indicated. Inset: temperature dependence of I_C (blue dots) and I_R (red squares). **c** Critical current I_C in the nanowire as a function of gate voltage V_G. **d** Absolute value of the gate current I_G flowing between gate and nanowire as a function of V_G. A linear component $I_G \sim 1$ TΩ, attributed to leakage in the measurement setup, was subtracted from the data (see section 4.2.1). **e** Parametric plot of I_C vs. I_G. Obtained from the data in c and d. Figure adapted from Ref. [138].

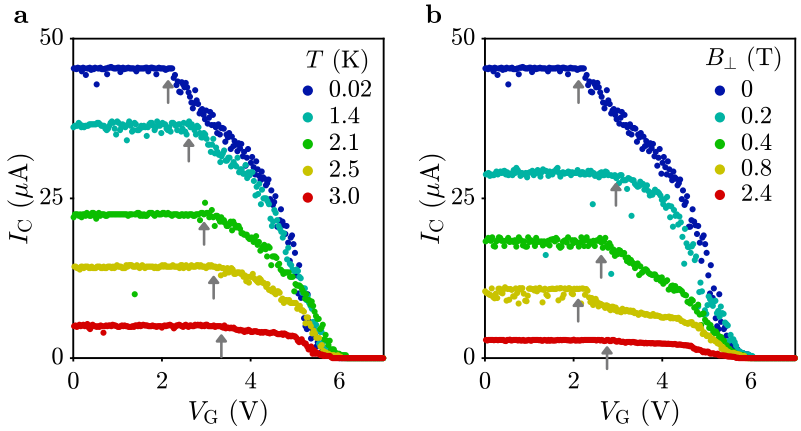

Figure 4.2. Temperature and magnetic field dependence. a Critical current I_C of the device presented in Fig. 4.1 as a function of gate voltage V_G for various temperatures T. **b** Critical current I_C of the device presented in Fig. 4.1 as a function of out-of-plane magnetic fields $B_\perp$. Gray arrows indicate the gate voltage where I_C starts to decrease. Figure adapted from Ref. [138].

V_G values for complete suppression of superconductivity in the nanowires, up to the critical temperature and critical field. On the other hand, the increase of I_C suppression systematically moved to higher V_G for higher temperatures (see gray arrows). A more complicated dependence was observed as a function of $B_\perp$.

4.1.5. Critical Current Suppression in Various Superconductors

Suppression of I_C concomitant to, or slightly anticipating, the onset of I_G above detection level was confirmed for over 20 TiN devices, characterized by various gate shapes, nanowire widths (40, 80 and 200 nm), nanowire lengths (650 nm, 1 and 2 μm), and gate-to-wire separations (80 and 160 nm, see section 4.2.3). Similar behavior was also observed on devices with a different substrate than Si or with a different superconductor than TiN. Figures 4.3a and b show measurements performed on a TiN device as that of Fig. 4.1a, but deposited on a 25 nm SiO_2 layer thermally grown on Si. Despite the vastly different operational range of V_G with respect to that of Fig. 4.1, suppression of I_C still coincided with the onset of I_G. Devices with a SiO_2 interlayer further showed a characteristic asymmetry of the I_C vs. V_G curve, with a sharper suppression of I_C for negative than for positive V_G. Given the sharp termination of the gate electrode, and the large electric field reached on SiO_2 substrates, emission of electrons from the gate is expected to be easier for negative gate biases. In the present case, detection of small gate current asymmetries is hindered by spurious current leakage in the measurement setup for high gate biases. Figures 4.3c and d show I_C and I_G, respectively, as a function of V_G for a Ti nanowire as that of Fig. 4.1a, but with 200 nm width and 30 nm thickness. In this case, the normal state was reached for I_G as low as 30 pA for positive V_G.

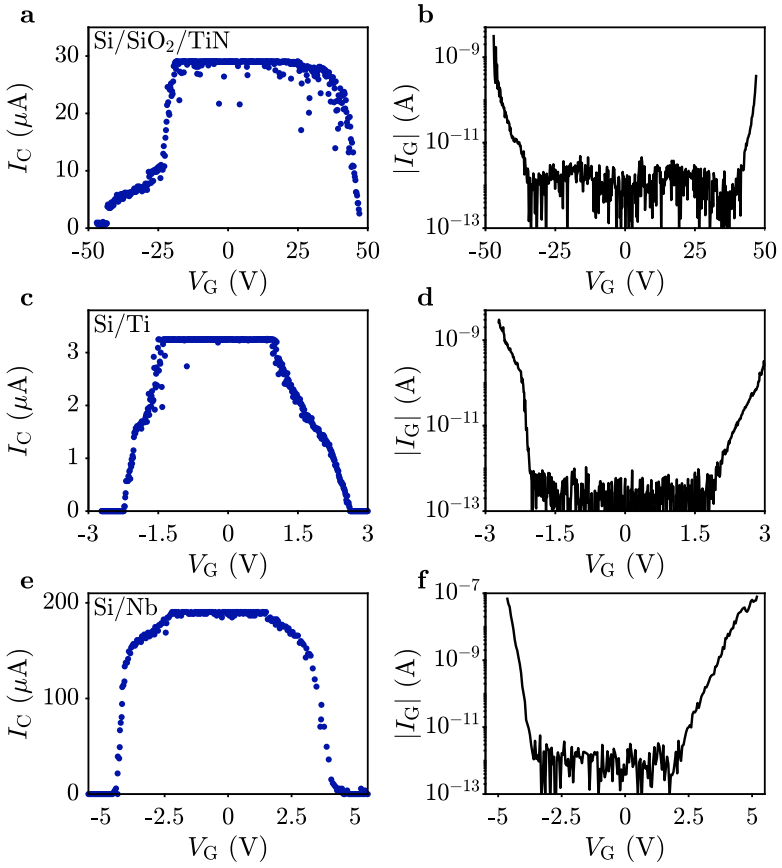

Figure 4.3. Critical current suppression in various superconductors. a,b Critical current I_C and gate current I_G as a function of gate voltage V_G for a TiN wire on a 25 nm thick SiO_2 film thermally grown on Si substrate. The wire is 2 μm long, 80 nm wide and 20 nm thick. **c,d** Critical current I_C and gate current I_G as a function of gate voltage V_G for a Ti wire on Si substrate. The wire is 2 μm long, 200 nm wide and 30 nm thick. **e,f** Critical current I_C and gate current I_G as a function of gate voltage V_G for a Nb wire on Si substrate. The wire is 2 μm long, 200 nm wide and 13 nm thick. Figure adapted from Ref. [138].

Figures 4.3e and f show I_C and I_G, respectively, as a function of V_G for a Nb nanowire as that of Fig. 4.1a but with 13 nm thickness. Similarly to the previous cases, I_C started to decrease with I_G still below 100 fA. However complete suppression of I_C required $I_G \geq 20$ nA. Overall, these results indicate that the switching mechanism presented here is generic, and not linked to specific superconductors or substrates. On the other hand, data also suggests that small gap superconductors (e.g. Ti) require considerably less gate current for switching to occur compared to superconductors with larger gaps (e.g. TiN or Nb).

4.1.6. Spatially Resolved Suppression of the Critical Current

Measurements presented so far were conducted in relatively short nanowires, where sharp transitions from zero resistance to the normal state were observed. We complement these observations with measurements on a long, multi-terminal nanowire, which allow us to investigate how superconductivity is affected away from the electron injection point, along the nanowire length. The device shown in Fig. 4.4a consists of six TiN segments of 1 μm length and 80 nm width (named A to F). Each segment j is controlled by a nearby gate, with gate voltage V_{G}^{j} and corresponding gate current I_{G}^{j}. In a first measurement configuration (Configuration 1), schematically shown in Fig. 4.4b, I_{SD} was passed between contacts 1 and 9, that is the DC current is the same for every segment. As I_{SD} was ramped, voltages V_j across the six segments were simultaneously recorded. Critical currents I_{C}^{j}, defined as the values of I_{SD} where segment j turned resistive, are reported in Fig. 4.4b as a function of $V_{\mathrm{G}}^{\mathrm{A}}$, with the corresponding gate current I_{G}^{j} shown in Fig. 4.4d. Configuration 1 highlights two regimes. For $I_{\mathrm{SD}} > I_{\mathrm{R}}$, switching in all the segments happened simultaneously. For $I_{\mathrm{SD}} < I_{\mathrm{R}}$, switching was sequential: the further away a segment was from the biased gate, the larger was the gate current required to suppress its critical current. We contrast this behavior with the results obtained using Configuration 2, schematically shown in Fig. 4.4c. In this case, I_{SD} is routed in one segment only. The critical currents of the six segments were extracted in six separate measurements as $V_{\mathrm{G}}^{\mathrm{A}}$ was biased (see Fig. 4.4c). Routing I_{SD} far from the electron injection point avoids the simultaneous switching observed in Fig. 4.4b, highlighting instead spatial dependence of the critical current also for $I_{\mathrm{SD}} > I_{\mathrm{R}}$. In Fig. 4.4e we plot the critical current suppression factor S as a function of distance Δx between injection point and segment. The suppression factor for a segment j is defined as $S^j = (I_0^j - I_{\mathrm{C}}^j)/I_0^j$, where I_0^j is the critical current of a segment for zero gate voltage. A fit to an exponentially decaying function $\exp(-\Delta x/\lambda)$ (solid line in Fig. 4.4f), yields a characteristic decay length $\lambda \sim 1.8$ μm.

4.1.7. Discussion

After presenting the experimental results, we now discuss the origin of the observed phenomena. Injected electrons reach the superconductor in a deeply out-of-equilibrium state, with energies of the order eV_{G}, much larger than the superconducting gap Δ ($\Delta = 500$ μeV for TiN [192]). As each electron relaxes to the gap edge by inelastic scattering with other electrons and phonons, up to $eV_{\mathrm{G}}/\Delta \sim 10^5$ quasiparticles are generated within the nanowire. A sufficiently high concentration of quasiparticles drives the nanowire into the normal state by quenching the superconducting gap [193], leading to a suppression of the depairing critical current [194]. The closer I_{SD} is to I_{C}, the more sensitive the device becomes, so that relatively few injected electrons can trigger a normal state transition. Indeed, half of the suppression of I_{C} takes place for gate currents below the noise floor of our setup, where the power provided by the gate voltage source is less than 300 fW and unlikely to result in any relevant temperature increase. Indeed, a temperature increase above 1.5 K would be needed for an appreciable vari-

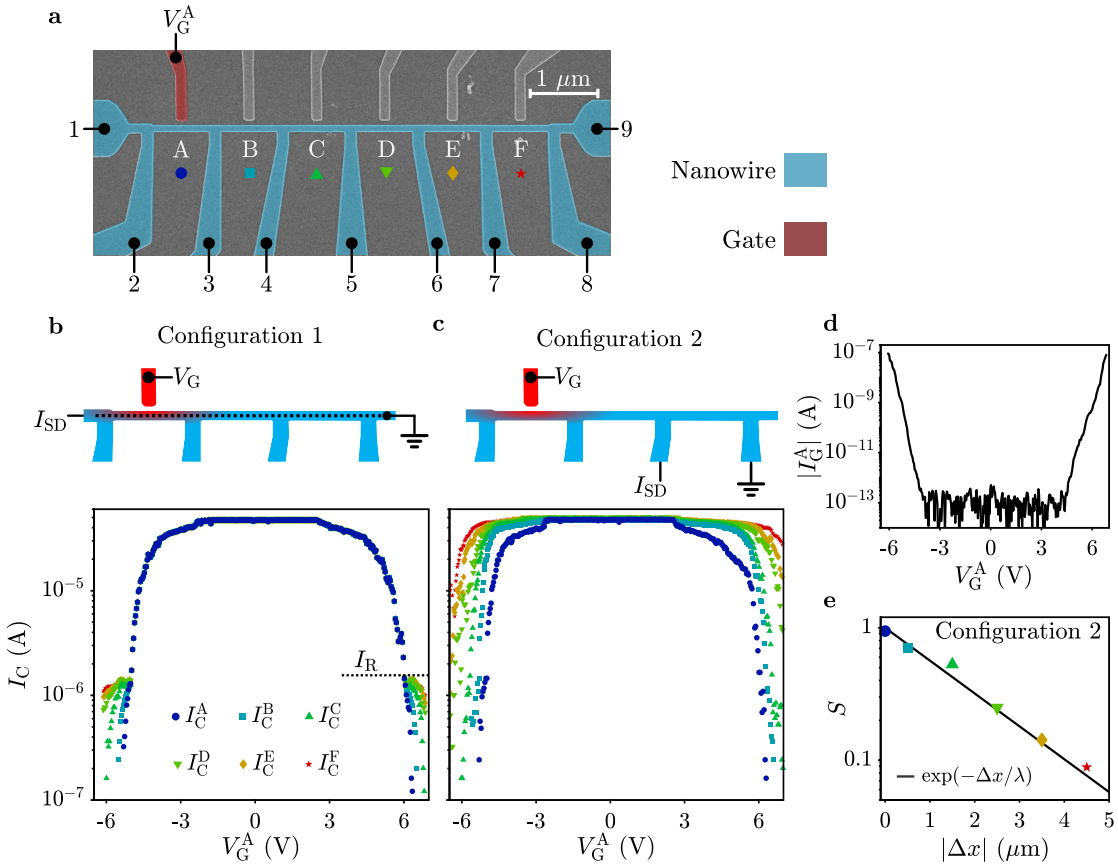

Figure 4.4. Spatially resolved suppression of the critical current. **a** False color scanning electron micrograph of a device as that under study. Colors are as in Fig. 4.1a. **b** Top: schematics of measurement configuration 1, where I_{SD} always intersects the point of electron injection. Bottom: critical currents of the six segments as a function of gate voltage $V_G^A = 6$ V. **c** Top: schematics of measurement configuration 2, where I_{SD} does not necessarily intersect the point of electron injection. Bottom: critical currents of the six segments as a function of gate voltage $V_G^A = 6$ V. **d** Absolute value of gate current I_G^A as a function of gate voltage V_G^A. **e** Suppression factor S as a function of the distance between gate and nanowire segment, calculated from the data in c for $V_G^A = 6$ V. The solid line is a fit to an exponential, resulting in a characteristic length scale $\lambda = 1.8$ μm. Figure adapted from Ref. [138].

ation of I_C to be detected (see Fig. 4.1b). This can be excluded at such small gate currents. Such behavior is reminiscent of superconducting nanowire single photon detectors (SNSPDs) [195, 196], where the strike of a visible or infrared photon promotes a single electron to high energy, which in turn triggers the generation of a large amount of quasiparticles as it relaxes. In the present case, high energy charge carriers are provided directly by the gate current. Due to their close proximity, gate and nanowire are coupled

by phonons, so that dissipation of the injected energy and generation of quasiparticles occurs on both sides. Figures 4.2a and b show rich physics at low values of V_G, with the initial suppression of I_C moving to higher and higher gate voltages as temperature increases (see gray arrows). This behavior presumably reflects the increase of quasiparticle density in the wire with temperature, requiring more electrons to be injected before a sizable effect on I_C is observed. Systematic studies of the more complicated variations of I_C vs. V_G as a function of $B_\perp$ could shed light on the physics of field repulsion and vortex penetration in nanowires [197].

For gate currents several orders of magnitude larger, the power provided to the device is significant and likely to result in an increase of the local lattice temperature. We estimate the minimum power required for keeping the nanowire in the normal state as $P_R = I_R^2 R_N$, that is Joule heating in the normal state and at the retrapping current. For the device of Fig. 4.1 we obtain $P_R = 1.6$ nW. This power is similar to the one provided by the gate voltage source at the point where superconductivity is suppressed $P_G = V_G I_G$. For the device of Fig. 4.1, we obtain $P_G = 6.1$ nW. The difference between P_R and P_G is readily accounted for by considering that a significant fraction of P_G is not dissipated in the nanowire but in the gate electrode and in the surrounding environment. Furthermore, quasiparticles generated withing the nanowire spread over a distance longer than the nanowire length, so that a fraction of them thermalizes in the leads (see following discussion). The relation $P_G \approx 4P_R$ is closely followed also for the devices of Fig. 4.3. The consistency is remarkable considering that dissipated power in the Nb wire ($P_R = 29$ nW) is three orders of magnitude larger than for the Ti wire ($P_R = 23$ pW).

After determining that small currents of high energy electrons are responsible for weakening of the superconducting properties, we discuss in more detail how the transition to the normal state takes place. The device of Fig. 4.1 showed a sharp transition from superconducting to its normal state resistance for any gate voltage. This behavior might appear surprising considering that the gate acts on a short portion of the nanowire. With reference to Fig. 4.4, we demonstrated that the sharp transition to the normal state resistance is a result of the measurement configuration. Indeed, I_C is first reduced in a region close to the point of electron injection. As I_{SD} is increased, that region switches to the resistive state and becomes a hotspot due to the large I_{SD} flowing in the nanowire. For $I_{SD} > I_R$ the hotspot warms up the surrounding metal via Joule heating, resulting in a further spreading of the normal region. This process rapidly turns the entire nanowire length normal along the path of I_{SD}. For $I_{SD} < I_R$ the power dissipated in the hotspot is insufficient to trigger the transition to the normal state in the nearby metal. In this case, considerable gate currents are needed to influence regions of the nanowire which are furthest away via diffusion of energetic quasiparticles and heat. In Configuration 2, I_{SD} does not intersect the point of electron injection (except for segment A) and simultaneous switching is prevented and the critical current is lowest at the point of injection and restored at large distances. The characteristic length scale of 1.8 μm is presumably related to the diffusion length of long lived quasiparticles. A framework for calculating quasiparticle density profiles has been put forward for SNSPDs in Ref. [197]

and is compatible with our experimental results.

Recent work argued on the effect of electric fields on the critical current of metallic nanowires, using a similar device as that of Fig. 4.1a [153, 157]. From a qualitative standpoint, the modulation of I_C we observe strongly resembles data in Refs. [153, 157], including ambipolar behavior, response to temperature and magnetic field and spatial suppression of the supercurrent reduction. We note that electric field modulation of superconductivity has been previously demonstrated in metallic thin films [151, 152], but changes of critical temperature by less than one percent required significantly stronger electric fields than those applied here. Investigating multiple material combinations and comparing local and non-local measurement configurations allow us to readily exclude any electric field induced suppression of superconductivity in our devices. First, gate voltages are too small to generate a sizable electric field (see section 4.2.3 for a different gate design leading to identical results). Second, suppression of superconductivity is always correlated to the onset of gate currents, irrespective of the applied gate voltage. Third, non-local responses extend far beyond the gate induced electric field, to a distance where only phonons and quasiparticle diffusion is relevant (see Fig. 4.4). We further note that the gate current needed for affecting superconductivity is especially low for small gap superconductors on highly insulating substrates, the platform used in Refs. [153, 157]. For large gap superconductors on semi-insulating substrates, i.e. the main focus of this work, the lower energy of emitted electrons, together with the requirement for higher quasiparticle density to suppress superconductivity, make required gate currents larger and their detection more feasible.

Injection of high energy electrons in superconducting elements might be employed for realization of fast and electrically controlled superconducting switches. As devices properly function also in the limit of $I_{SD} = 0$, self-resetting from normal to superconducting state is not inhibited by self-heating [190], a limitation of other superconducting devices. The quasiparticle relaxation length limits the extent of the segment that can be switched, and consequently the largest normal state resistance of the device. Alternatively, nanowires of arbitrary length can be operated by choosing $I_{SD} > I_R$ [186, 188]. We expect the switching time to be fast, presumably limited by quasiparticle recombination (less than 100 ps) [188]. In our case, we measured a switching time below 100 ns, limited by the setup in use (see section 4.2.4).

In conclusion, we demonstrated quenching of superconductivity in metallic nanowires via gate currents several orders of magnitude smaller than the source-drain critical current and described the physical mechanisms responsible for this behavior. Devices studied here could serve as tools for novel studies of quasiparticle physics at unprecedented energy scales and in the limit of no current flowing in the nanowire. Furthermore, combining length dependence studies as in Fig. 4.4 with time-resolved measurements, will provide a novel tool to investigate quasiparticle dynamics and thermal effects.

Acknowledgments

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4.1.8. Methods

Electrical Measurements

Unless specified differently, measurements were performed in a dilution refrigerator at the base temperature of 20 mK. Low-pass RC filters and microwave pi-filters were installed along each line. A DC source-drain current I_{SD}, superimposed to a small AC component of 30 nA and 113 Hz was applied to the nanowire via large bias resistors. The AC differential voltage V across the nanowire was then recorded with lock-in amplifiers with 10 MΩ input impedance and used to calculate the differential resistance dV/dI_{SD}. Measurements were recorded with I_{SD} as the fast axis, sweeping from zero to positive values. This allowed initializing the wires to the superconducting state before each sweep started. Gate voltages were applied with a Keysight B2902A source-measure unit, which also recorded the current entering the gate contact. To avoid damaging the devices, a compliance of ±95 nA was chosen. A linear contribution of about 1 pAV^{-1}, associated with spurious leakage paths in our setup, was subtracted from the I_G measurements shown in the Main Text (see section 4.2.1). To avoid potential contributions from displacement currents or hysteresis, I_G values were recorded by sweeping V_G from 0 V towards either positive or negative voltages and waiting times in excess of 30 s were allowed. Plots as that of Figs. 4.1c and d were then obtained by merging two data sets at $V_G = 0$ V. In case a second gate was present and left grounded, as for the device in Fig. 4.1a, it was verified that most of the gate current was flowing from the energized gate to the nanowire and not to the grounded gate.

In a standard measurement configuration, I_{SD} is sourced on one side of the sample by applying a voltage to a large resistor, while the other side of the sample is connected to ground. This asymmetric configuration results in lifting of the nanowire potential by $I_{SD}R_L$, where R_L is the resistance of the line connecting the nanowire to ground (2.2 kΩ in our case). This effect is typically negligible, except for samples where a large I_{SD} is required (see Fig. 4.3e). A first approach is to use a symmetric current biasing configuration, as shown in Fig. 4.8. Alternatively, this effect can be accounted for by representing critical currents on the virtual voltage axis $V_G^* = V_G - I_{SD}R_L$.

4.2. Publication I: Supporting Information

4.2.1. Processing of the Gate Current

Measurements of the gate current I_G, flowing between gate and nanowire channel were obtained with a Keysight B2902A source-measure unit and processed by the numerical technique described below. The source-measure unit applied a voltage V_G to the gate contact and read the current I_G flowing into the setup. An example of an I_G vs. V_G curve measured with this technique, referred to as Method 1, is shown in Fig. 4.5 (green dots). When measuring with Method 1, we describe the DC current flowing into the electrical setup as sum of two components: the current that actually flows into the gate electrode and reaches the nanowire, and the current that is lost before reaching the gate by spurious leakage paths present in the cryostat. The first current component is expected to depend exponentially on V_G, the second was found to be approximately linear. That is, for small gate voltages, the current flowing to spurious paths and not reaching the gate voltage is dominating. The following numerical procedure was applied to extract the current contribution that actually reaches the nanowire. First, a current offset related to the measurement device is subtracted from the data (typically within ± 5 pA), so that $I_G = 0$ for $V_G = 0$. Second, a line is fit to the experimental $I_G(V_G)$ curve for small values of V_G (dotted black line in Fig. 4.5). Third, the obtained line is subtracted from the experimental curve in the entire V_G range, resulting in the red triangles in Fig. 4.5. This procedure typically results in gate currents which are within the noise level of our setup at low V_G, and then increase exponentially at large V_G. The linear component that we subtracted corresponds to a resistance of about 1 TΩ. Testing different parts of our setup individually showed that this spurious resistance is predominantly associated with the low frequency twisted pair wires that bring the signal from room temperature to the mixing chamber stage, and is present also when no device is connected. In our experience, such a high value of resistance to ground is indicative of a good DC measurement setup.

To verify the validity of this numerical procedure, we measured the current with a second technique, referred to as Method 2. In Method 2, all contacts to the nanowire channel are left floating except for one, which is grounded via a low impedance IV converter (Basel Physics SP 983, with feedback resistance set to 1 GΩ). The gate current I_G injected into the nanowire channel flows into the IV converter and gives rise to voltage output of $I_G \times 1$ GΩ. The current I_G simultaneously measured with Method 2 is also shown in Fig. 4.5 (blue squares) and is essentially identical to that processed with the numerical technique described above. Adopting Method 2 throughout this work would however not be possible, as the large source-drain currents needed to reach the critical current would result in overloading of the IV converter. For example, the current to voltage gain of 1 GΩ allows for a maximum input current of 10 nA, while typical source-drain critical currents extend up to 200 μA. Operating with lower current-to-voltage conversion gain, such as 100 kΩ, would not provide enough resolution to detect small gate currents.

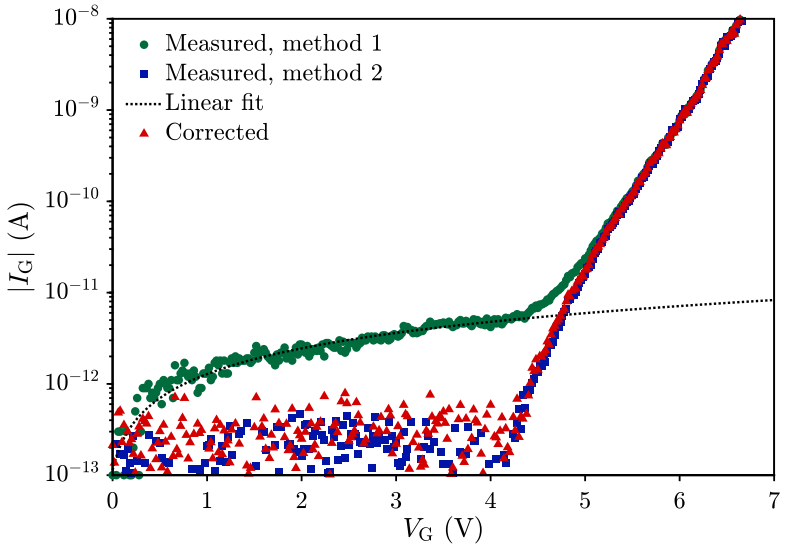

Figure 4.5. Processing of the gate current. Measurement and processing techniques for the gate current I_G as a function of gate voltage V_G. Green dots are measured by Method 1 (see text), blue squares by Method 2 (see text). The dotted black line is a linear fit to the green dots for $V_G \leq 3.5$ V. Red triangles are obtained by subtracting the dotted line from the green dots. Figure adapted from Ref. [138].

4.2.2. Temperature and Field Dependence of the Gate Current

Figure 4.2 shows the critical current I_C as a function of gate voltage V_G for the device of Fig. 4.1 measured at various temperatures and fields. In Fig. 4.6a and b we show the simultaneously measured gate currents I_G. Data indicate that I_G is unaffected by both temperatures and magnetic fields.

4.2.3. Measurement of a Device with Large Gates

Data shown in section 4.1 was obtained on nanowires where gates were relatively narrow (on the order of 100 nm or less) and terminated with a sharp tip. In Fig. 4.7 we present measurements obtained on a nanowire as that of Fig. 4.1, but with 2 μm wide gates. A false colored scanning electron micrograph of the device is shown in Fig. 4.7a, together with the measurement setup. The nanowire is colored in blue and the two gates in red. The gates are separately operated with gate voltages V_{G1} and V_{G2}, respectively. The response to a source-drain current was characterized in Fig. 4.7b by sweeping I_{SD} up from the resistive state. As for the wire in Fig. 4.1, the critical current was $I_C = 47$ μA and the retrapping current $I_R = 1$ μA. The source-drain critical current I_C as a function of gate voltage V_{G1} is shown in Fig. 4.7c, with the corresponding gate current I_{G1} shown in Fig. 4.7d. Equivalent measurements performed as a function of gate voltage V_{G2} are shown in Figs. 4.7e and f. For both V_{G1} and V_{G2}, full suppression of I_C was reached at

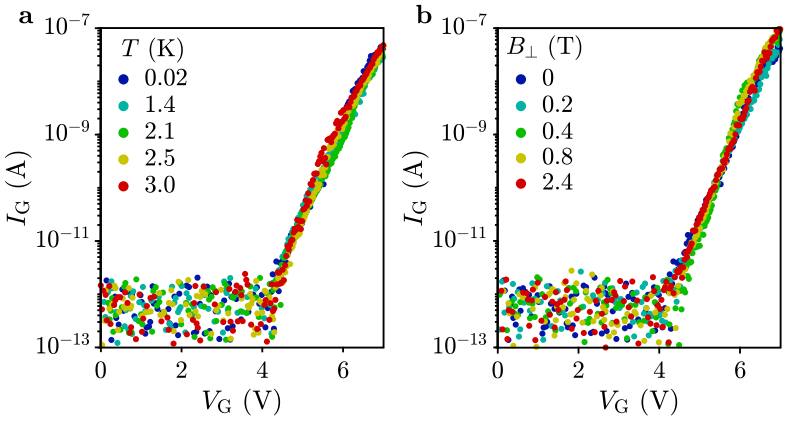

Figure 4.6. Temperature and magnetic field dependence of the gate current. a Gate current I_C as a function of gate voltage V_G simultaneously measured as in Fig. 4.2a. **b** Gate current I_C as a function of gate voltage V_G simultaneously measured as in Fig. 4.2b. Figure adapted from Ref. [138].

about ±4 V, corresponding to gate currents of about ±1 nA.

4.2.4. Time-Resolved Measurements

Here we present time-dependent measurements, indicating fast switching operation as a function of V_G and the ability of the device to self-reset from normal to superconducting state. A schematic of the electrical setup used for those measurements is shown in Fig. 4.8a, which allows for the simultaneous application of low frequency and high frequency signals (colored blue and red, respectively). The device was mounted on a sample holder with resistive bias-Ts (resistance $R_T = 50$ kΩ and capacitance $C_T = 22$ nF). The low frequency lines (resistive twisted pairs) passed through RC low pass filters on the sample holder (LP in Fig. 4.7a) and additional RC filters and high frequency pi-filters at the mixing chamber level (not shown), resulting in an additional line resistance $R_L = 2.5$ kΩ. A voltage bias V_{SD}, symmetrically applied between two low frequency inputs, resulted in a source-drain current of approximately $I_{SD} = V_{SD}/(2R_T + 2R_L)$. Application of a symmetric bias ensured the nanowire potential was constant with respect to the gate potential as I_{SD} varied. Low frequency voltage signals V^+ and V^- were used to calculate the nanowire four terminal resistance as $R = (V^+ - V^-)/I_{SD}$.

The device transmission was measured via a lock-in amplifier (Zurich Instruments UHFLI, with input and output set to 50 Ω impedance) by applying a voltage V_{in} through a −80 dB attenuator (A) and recording the resulting voltage V_{out}. The ratio V_{out}/V_{in} is shown in Fig. 4.8b as a function of frequency f for three situations. In orange is the situation where the wire was superconducting, meaning $I_{SD} = 0$ and $V_G = 0$. In blue is the situation in which the wire was turned normal by means of a DC current $I_{SD} = 60\mu$A, larger than the nanowire critical current $I_C = 50$ μA. In green is the situation in which the nanowire was turned normal by the application of a DC gate

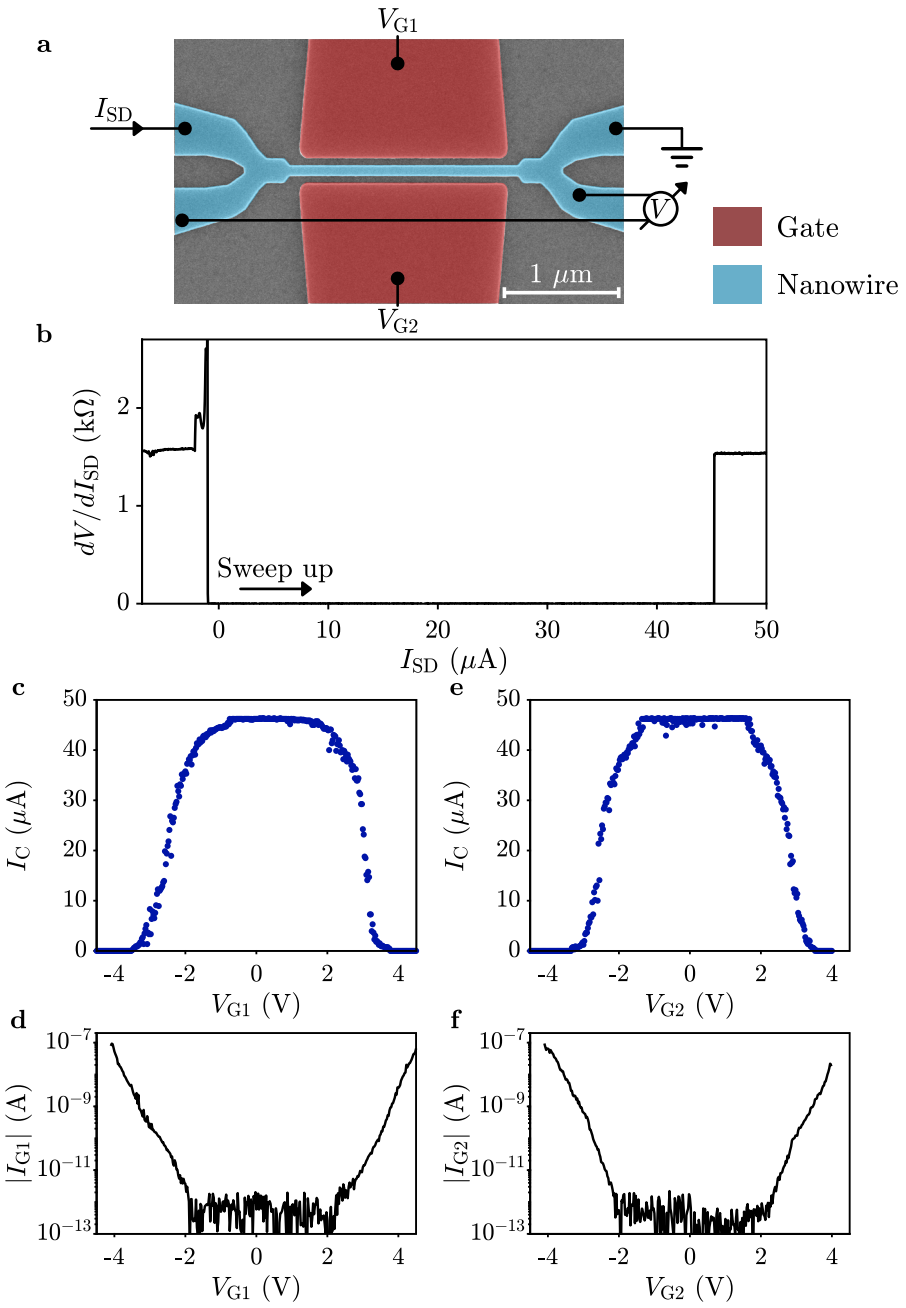

Figure 4.7. Measurements of a device with wide side gates. **a** False colored scanning electron micrograph of the device under study and schematics of the measurement setup. The nanowire is colored blue and the side gates red. **b** Nanowire resistance dV/dI_{SD} as a function of source-drain bias current I_{SD}. The measurement highlights the critical current $I_C = 47$ μA and the retrapping current $I_R = 1$ μA. **c** Critical current I_C as a function of gate voltage V_{G1}. **d** Gate current I_{G1} as a function of gate voltage V_{G1}. **e** Critical current I_C as a function of gate voltage V_{G2}. **f** Gate current I_{G2} as a function of gate voltage V_{G2}. Figure adapted from Ref. [138].

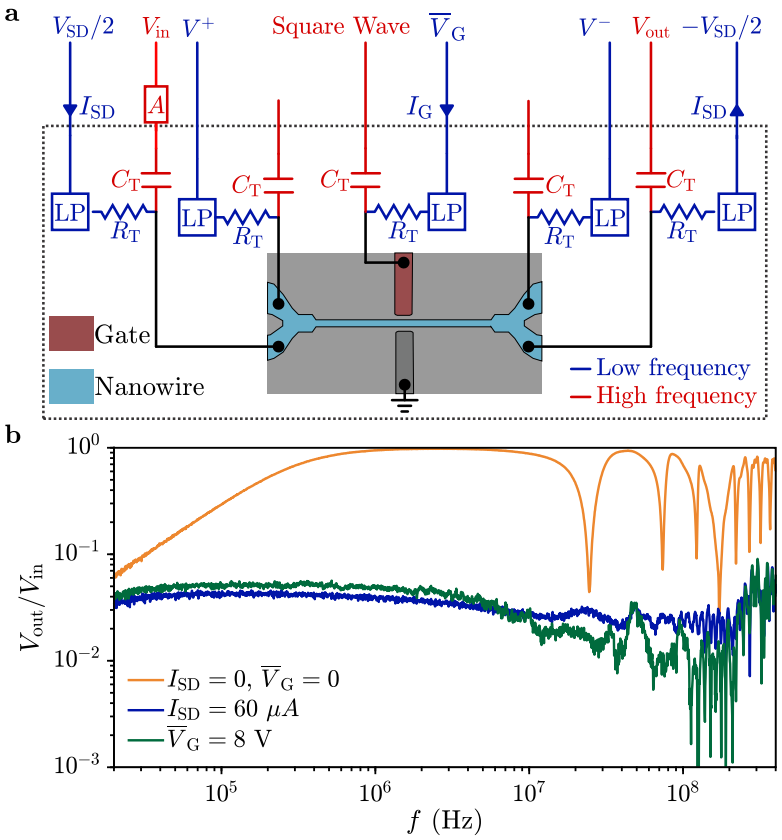

Figure 4.8. High frequency measurements. **a** Schematic measurement setup for the high frequency experiment presented in Fig. 4.9. The dashed box divides the 20 mK (inside) and room temperature (outside) apparatus. Lines for low and high frequency signals are indicated in blue and red, respectively. Low temperature bias-Ts with components R_T and C_T were connected to the four leads of the wire and a side gate. Low frequency cables were filtered by low-pass (LP) filters. Symmetric application of low frequency voltage $\pm V_{SD}/2$ results in the flow of a current I_{SD}. Fast signals V_{in} and V_{out} are applied and recorded, respectively, thorough 50 Ω ports. **b** Frequency dependent V_{out}/V_{in} signal measured with the nanowire in the superconducting state (orange), in the normal state as a consequence of a large source-drain current (blue), and in the normal state as a consequence of a large gate voltage (green). Figure adapted from Ref. [138].

voltage $\overline{V}_G = 8$V. As expected, for sufficiently high frequency the device transmission in the superconducting state approaches unity. Deviations however occur at specific frequencies, presumably due to the fact that the device was not designed to operate at high frequencies. Measurements shown below were performed at a frequency of 250 MHz.

Using the low temperature bias-Ts, a square wave signal was superimposed to the low frequency gate voltage $\overline{V}_G$. The ratio between the transmitted voltage V_{out} and the voltage input to the measurement setup V_{in} is shown in Fig. 4.9a as a function of

time t and $\overline{V}_G$, with the time-averaged gate current shown in Fig. 4.9b. Clear switching operation was achieved within a 500 mV interval around $\overline{V}_G = 6.7$ V, corresponding to a gate current of 1 nA. Figure 4.9c shows a line cut of Fig. 4.9a for $\overline{V}_G = 6.7$ V, demonstrating fast and reproducible switching between two impedance states. A zoom-in close to a rise point is shown in Fig. 4.9d, with dashed lines marking the transition between 10% and 90% of the step height, which takes place in 90 ns (similar results are obtained for the decay time). Such transient equals three times the time constant of the lock-in amplifier used for these measurements (30 ns) and is taken as the shortest switching time measurable with the setup in use, and as the upper limit for the device response time. Future work will take advantage of samples specifically designed for microwave measurements [186] and correlation techniques [188] to test the ultimate switching speed of the device.

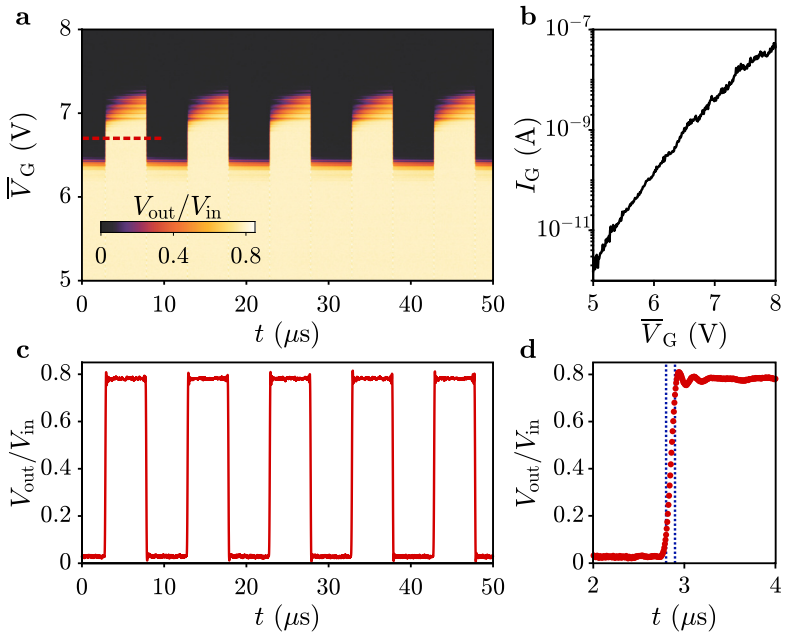

Figure 4.9. Fast switching in a metallic nanowire. a Time-dependent switching characteristics of a device as that of Fig. 4.1a as a function of DC gate voltage $\overline{V}_G$. A 100 kHz square wave with peak-to-peak amplitude of 1 V was added to $\overline{V}_G$. **b** Gate current I_G as a function of $\overline{V}_G$ measured simultaneously to the data in **a**. **c** Line-cut of the data in **a** for $\overline{V}_G = 6.7$ V (see red line). **d** Zoom-in of the data in **c** in proximity to a normal to superconducting state transition. Dashed vertical lines indicate the 10% to 90% amplitude transition, corresponding to 90 ns. This value is limited by the measurement bandwidth of the setup in use and serves as upper limit for the device switching time. Figure adapted from Ref. [138].

Our superconducting switch has the remarkable property to operate without the need of a DC current I_{SD} flowing in it. Measurements shown in Fig. 4.9 were obtained with $I_{SD} = 0$, where latching mode is not required. As expected, similar behavior

was obtained for $|I_{SD}|$ smaller than the retrapping current I_R ($I_R = 1.1$ μA in the present device). Figure 4.10 demonstrates switching operation as a function of I_{SD}. For $|I_{SD}| < 1$ μA clear and fast switching operation was obtained, without the need of self-resetting the device at every gate cycle. On the contrary, for $|I_{SD}| > I_R$ no switching was observed.

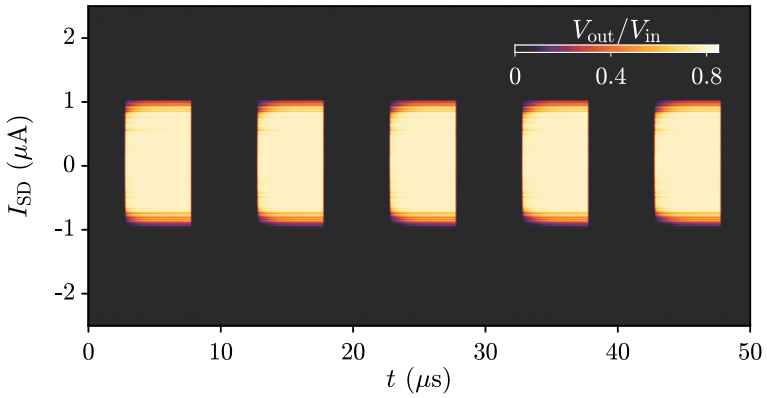

Figure 4.10. Demonstration of self-resetting. Switching operation as a function of the DC source-drain current I_{SD}. Self-resetting was possible for I_{SD} values smaller than the nanowire retrapping current. Figure adapted from Ref. [138].

4.3. Publication II: Out-of-Equilibrium Phonons in Gated Superconducting Switches

4.3.1. Abstract

Recent experiments have suggested that superconductivity in metallic nanowires can be suppressed by application of modest gate voltages. The source of this gate action has been debated and either attributed to an electric field effect or to small leakage currents. Here we show that suppression of superconductivity in titanium nitride nanowires on silicon substrates does not depend on the presence or absence of an electric field at the nanowire, but requires a current of high-energy electrons. The suppression is most efficient when electrons are injected into the nanowire, but similar results are obtained when electrons are passed between two remote electrodes. This is explained by the decay of high-energy electrons into phonons, which propagate through the substrate and affect superconductivity in the nanowire by generating quasiparticles. By studying the nanowire switching probability distribution, we also show that high-energy electron emission leads to a much broader phonon energy distribution compared to the case where superconductivity is suppressed by Joule heating near the nanowire.

4.3.2. Introduction

It is generally thought that metallic nanostructures are not affected by electric fields, as long as their size is larger than the corresponding screening length, which is typically below 1 nm. Recent experiments [153–156, 160, 162] have, however, shown that gate voltages can have a dramatic impact on the superconducting properties of metallic devices, including the ambipolar quenching of the critical current. The microscopic mechanism responsible for this behaviour has sparked debate. First, it was suggested that an electric field can penetrate a superconducting film up to the London penetration depth [153]. Second, it was proposed that an electric field might perturb the polarization of atomic orbitals at the metal surface, and this would affect the superconducting properties in the bulk [158, 168]. Third, studies of the switching probability distribution in metallic nanowires suggested an interplay between an electric field and superconducting phase slips [160].

We have previously reproduced the most distinctive features of these experiments using titanium nitride (TiN), niobium and titanium nanowires [138]. In our samples, the critical current suppression was always accompanied by a current flowing between gate and nanowire. In these experiments the gate current is carried by electrons with energies of several eV, which is orders of magnitude larger than the superconducting energy gap in the nanowires. We concluded that the emission of relatively few electrons lead to an avalanche of quasiparticles, which effectively quench the critical current [197]. This hypothesis was supported by tunnelling spectroscopy experiments [198], which highlighted a non-thermal increase in quasiparticle population as a gate voltage was applied.
Further work also demonstrated a correlation between onset of gate currents and suppression of superconducting properties [199, 200]. However, open questions remain. For

example, in a scenario where injection of high-energy electrons controls the critical current suppression, a marked asymmetry would naively be expected between injecting high-energy electrons into the nanowire (negative gate voltage) and extracting electrons from the nanowire at the Fermi energy (positive gate voltage), and having them relax either in the substrate or in the gate electrode. Unravelling the microscopic mechanisms behind these observations could prove valuable in the development of technological applications of the phenomenon, such as the realization of voltage-controlled superconducting switches and resonators.

In this Article, we show that the quenching of superconductivity in metallic nanowires can be linked to the relaxation of high-energy electrons, and not to the presence of electric fields at the superconductor surface. In particular, we examine the effect of high-energy electrons flowing into the nanowire, out of the nanowire, and between two remote gate electrodes in the vicinity of the nanowire. Detailed measurements reveal that superconductivity is most efficiently suppressed when a current is injected into the nanowire. However, a qualitatively similar critical current suppression is observed when high-energy electrons flow near the nanowire, without any current or electric field directly reaching the nanowire itself.

The non-local nature of the observed effect is consistent with energy relaxation of electrons by phonon emission in the substrate. Due to their relatively high energy, phonons generate quasiparticles in the superconductors and efficiently quench the critical current in our devices. At cryogenic temperatures phonons can propagate over considerable distances in the crystalline silicon substrate before thermalizing. The effect is thus distinct from the situation where a local temperature increase is produced by a resistive heater. Our observations question existing interpretations and theories based on electric fields, and provide insight into the complex interactions between out-of-equilibrium phenomena in solids and the performance of superconducting hardware.

4.3.3. Critical Current Suppression and Electric Fields

Seven TiN nanowires on Si substrates were investigated during this work. All nanowires had a length of 2 μm, a width of 80 nm and a height of 20 nm. At low temperature, devices showed critical currents I_C between 42 and 45 μA, a retrapping current $I_R = 1.0$ μA and a normal state resistance $R_N \sim 1750$ Ω, consistent with previous work [138]. The uniformity of these values demonstrates that the nanowires were homogeneous and not characterized by accidental weak links. The large difference between I_C and I_R indicates significant self-heating in the normal state, together with limited heat extraction via the leads or the substrate, typical of metallic nanowires [191, 201]. Further details on sample fabrication and basic characterization are reported in section 3.1. Here, we present results from four devices, referred to as Device A1, A2, B and C, respectively. Extended data and three additional devices, used as references, are shown in more detail in the Supplementary Material (Figs. 4.15, 4.16, and 4.17).

Figure 4.11a shows a false colored scanning electron micrograph of Device A1, together with a schematics of the measurement configuration. Device A1 consists of a nanowire (blue) and three gates (red). Gate 1, controlled by the voltage V_{G1}, was separated from

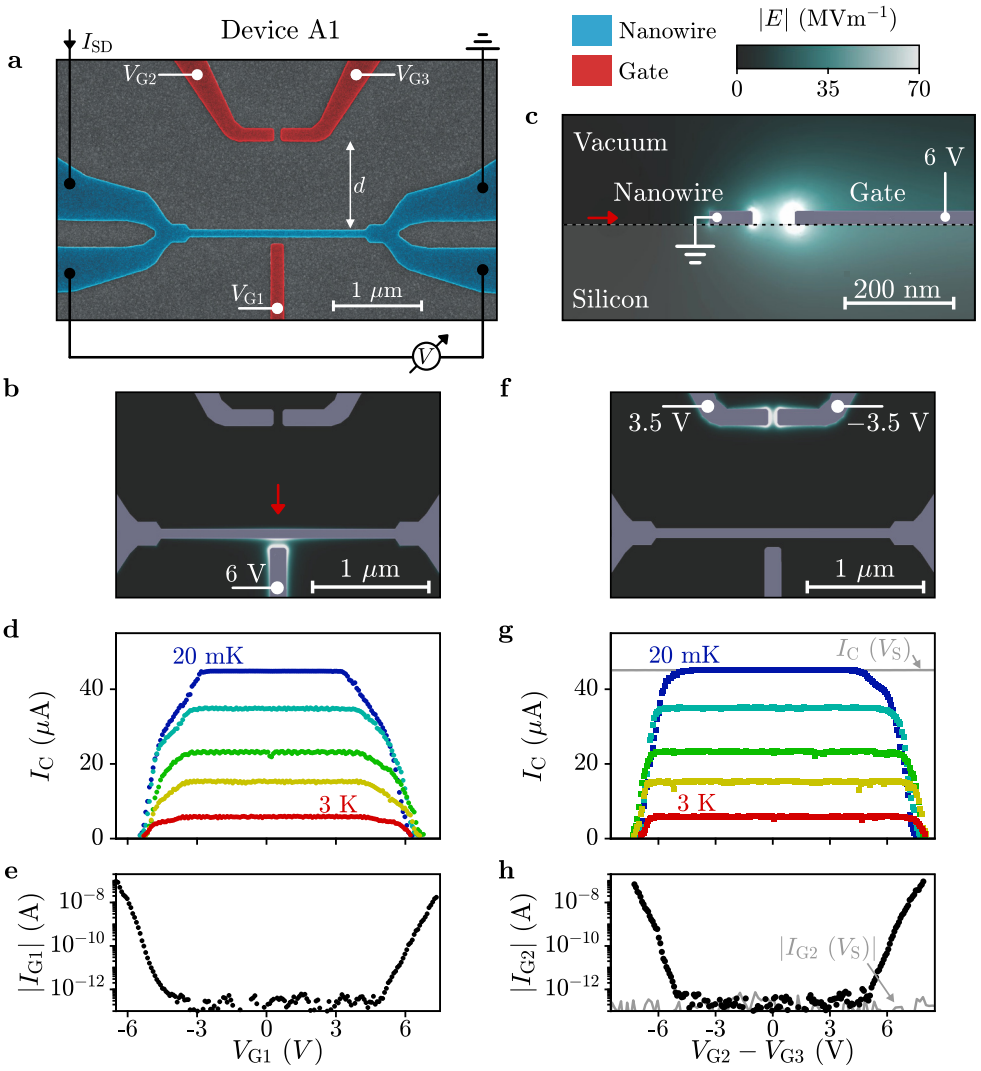

Figure 4.11. Basic device characterization and electric field simulation. **a** False color scanning electron micrograph of Device A1, with simplified measurement configuration. The nanowire under investigation is depicted in blue and the gates in red. **b** Finite element simulation of the electric field magnitude $|E|$ for $V_{G1} = 6$ V. We show a slice of the three dimensional simulation on a plane elevated 10 nm from the Si substrate. **c** Same as in **b**, but for a plane perpendicular to the substrate and intersecting gate 1. The red arrow indicates the direction of the cut in **b**. **d** Critical current I_C in Device A1 as a function of gate voltage V_{G1} for temperatures T of 20 mK (blue), 1.5 K, 2.1 K, 2.5 K and 3 K (red). **e** Gate current I_{G1} as a function of V_{G1} measured at $T = 20$ mK simultaneously to the data in **d**. **f** Finite element simulation as in **b**, but calculated for gate voltage difference $V_{G2} - V_{G3} = 7$ V. **g** Critical current I_C in Device A1 as a function of $V_{G2} - V_{G3}$ for temperatures as in **d** (markers), together with I_C as a function of $V_S = 2V_{G2} = 2V_{G3}$, representing twice the voltage applied to both gates simultaneously (gray line). **h** Current I_{G2} flowing from gate 2 as a function of voltage difference $V_{G2} - V_{G3}$. In this configuration $I_{G2} = -I_{G3}$ within experimental error. Gate current I_{G2} as a function of V_S is shown in gray. Figure adapted from Ref. [139].

the nanowire by a gap of 80 nm. Gates 2 and 3, controlled by voltages V_{G2} and V_{G3} respectively, were separated from each other by 80 nm and from the nanowire by a distance $d = 1$ μm. A similar device, named Device A2, had $d = 80$ nm and is presented in section 4.4.1.

We first discuss the response of Device A1 to a side gate voltage V_{G1}, similar to previous work [138, 153, 198]. The electric field distribution in this configuration was calculated using three-dimensional finite element simulations (see section 4.3.8).[1] Figure 4.11b shows the field magnitude $|E|$ on a plane 10 nm above the substrate for $V_{G1} = 6$ V. Figure 4.11c represents $|E|$ on a plane perpendicular to both the substrate and the wire axis, and intersecting the gate (see red arrow in Fig. 4.11b). To better highlight the field distribution, the color scale was saturated to $|E| = 70$ MVm^{-1}. The highest $|E|$ in our simulations was below $|E| = 500$ MVm^{-1}, which is several orders of magnitude smaller than typical electric fields required to perturb superconductivity in a metallic device [151, 152]. Figure 4.11d shows the experimentally measured I_C as a function of V_{G1}, for temperatures ranging from 20 mK (blue) to 3 K (red). Figure 4.11e shows the gate current I_{G1} measured simultaneously to the data in Fig. 4.11d. Consistent with previous observations [138, 199], the decrease of I_C was correlated to the onset of I_{G1}, and the initial decrease in I_C took place for $I_{G1} < 1$ pA. Furthermore, $|I_{G1}|$ was found to increase exponentially with V_{G1} and to be approximately symmetric around $V_{G1} = 0$.

We now discuss the dependence of I_C on a differentially applied voltage $V_{G2}-V_{G3}$, with $V_{G2} = -V_{G3}$. Figure 4.11f shows the numerically computed electric field for $V_{G2} - V_{G3} =$ 7 V. As expected, $|E|$ is strongly confined between Gates 2 and 3. If superconductivity in the nanowire were controlled by the electric fields, this configuration should result in negligible effects on I_C. Strikingly, quenching of the supercurrent occurred also in this situation, as shown in Fig. 4.11g. Figure 4.11h shows the current I_{G2} flowing from Gate 2 (we found $I_{G2} = -I_{G3}$ within experimental error). Remarkably, the suppression of I_C was strongly correlated to the onset of I_{G2}, despite no measurable gate current reached the nanowire and electric fields between gate and nanowire were negligible.

To test whether residual electric fields were relevant, we also measured I_C with Gate 2 and 3 biased at the same voltage ($V_{G2} = V_{G3}$). In Fig. 4.11g we plot I_C as a function of the quantity $V_S = 2V_{G2} = 2V_{G3}$ (solid gray line in Fig. 4.11g) as, at any one point in this plot, the absolute voltages $|V_{G2}|$ and $|V_{G3}|$ on the gate electrodes are identical and the absolute value of the electric field $|E|$ reaching the nanowire is similar. More specifically, we estimate $|E(V_{G2} = V_{G3})| \gtrsim |E(V_{G2} = -V_{G3})|$ at the nanowire surface. Nevertheless, no current was detected between gates and nanowire for symmetrically applied gate voltages (see gray curve in Fig. 4.11h) and I_C was not perturbed. These results further corroborate our findings that high-energy electrons, and not electric fields, are responsible for the suppression of I_C. Similar results obtained with Device A2 are presented in section 4.4.1.

Overall, experiments and numerical simulation presented in Fig. 4.11 demonstrate that the suppression of superconductivity takes place irrespective of electric fields at the nanowire surface. Instead it requires the flow of high-energy electrons in the surroundings

[1] Electric field simulations presented in this work were performed by Dr. N. Crescini and Dr. A. Fuhrer

of the device. This is the first conclusion of our work.

4.3.4. Role of the Substrate

The remote action of $V_{G2}-V_{G3}$ on I_C points to the existence of an efficient energy transfer mechanism triggered by the flow of I_{G2}. We now analyze the origin of this remote action more carefully using Devices B and C, shown in Fig. 4.12a and b, respectively. Device B is identical to Device A1, except for the presence of a 510 nm deep, 200 nm wide and 80 μm long trench etched into the substrate between the remote gates and the nanowire. Device C consists of two parallel TiN nanowires separated by a distance of 80 nm. Each nanowire was controlled by a nearby gate (red). We measured the critical current of one of the two nanowires (blue) while the second one (purple) was set in the resistive state and was traversed by a DC current I_H, resulting in Joule heating, similar to Ref. [202].

Figure 4.12c and d summarize the behavior of our devices in terms of I_C as a function of I_{G1} and I_{G2}, respectively. The full dataset is presented in Figs. 4.15 and 4.16. The dependence on I_{G1} (see Fig. 4.12c) is similar in all devices, with a faster suppression of I_C for $I_{G1} < 0$. Due to the exponential dependence of I_{G1} on V_{G1}, this asymmetry is hard to spot in Figs. 4.11d and e. We further notice that Device B (gray diamonds) exhibited a particularly slow decay of I_C for $I_{G1} > 0$. We will discuss possible causes for this asymmetry below. Figure 4.12d reveals that I_{G2} is significantly less effective in suppressing I_C than I_{G1}. Furthermore, Device A2 (blue squares, $d = 80$ nm), was six times more efficient than Device A1 (red circles, $d = 1$ μm), which was six times more efficient than Device B (gray diamonds, $d = 1$ μm plus an etched trench). In the case of Device B, the maximum I_{G2} allowed in our setup (100 nA) was not sufficient to reach $I_C = 0$. Altogether, these results demonstrate that most of the remote action of I_{G2} on I_C is mediated by the substrate, i.e. the high-energy electrons relax by emitting phonons, which travel through the substrate and affect superconductivity in the nanowire. This is the second main conclusion of our work.

4.3.5. Comparison to Joule Heating

We now discuss the properties of the generated phonons in more detail. In particular, we compare their effect on I_C to that of heat generated by a resistive conductor placed 80 nm from the superconducting nanowire. These experiments were performed with Device C, shown in Fig. 4.12b. The dependence of I_C on the heater current I_H is shown in Fig. 4.12e for various temperatures. As expected, Joule heating eventually resulted in the suppression of I_C. However, the current required to reach $I_C = 0$ was several orders of magnitude higher than in the configurations where a gate voltage was applied.

Figure 4.13 provides a comparison between the devices presented above in terms of the suppression of normalized critical currents I_C as a function of dissipated power. For each measurement configuration, we distinguish the case of positive and negative voltage bias with full and empty markers, respectively. The critical current is more efficiently suppressed when a voltage bias V_{G1} is applied to a gate directly facing the nanowire (red dots). In this case, the dissipated power is calculated as $I_{G1}V_{G1}$. When a remote

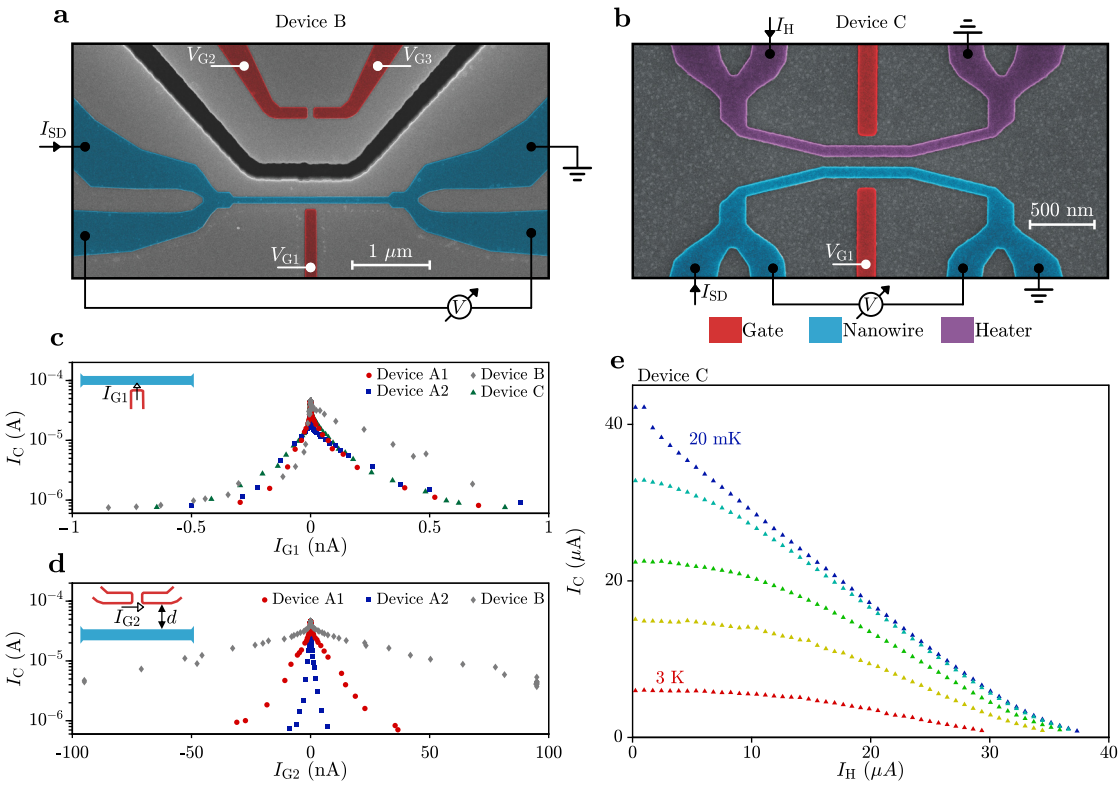

Figure 4.12. Additional devices. a False color scanning electron micrograph of Device B. The nanowire is depicted blue, the gates red and the trench appears black. The trench is 510 nm deep, 200 nm wide and has a total length of 80 μm. **b** False color scanning electron micrograph of Device C. The nanowire under investigation is depicted blue, the gates red and the heater nanowire purple. **c** Plot of critical current I_C as a function of gate current I_{G1} for all the devices presented in this section. **d** Plot of I_C as a function of the remote gate current I_{G2} for Devices A1 ($d = 1$ μm), A2 ($d = 80$ nm) and B ($d = 1$ μm plus a trench). **e** Critical current in Device C as a function of heater current I_H for temperatures as in Fig. 4.11d. Figure adapted from Ref. [139].

current I_{G2} flows, the power is calculated as $I_{G2}(V_{G2} - V_{G3})$. Suppressing I_C by means of Joule heating with a resistive conductor (purple line) required a significantly higher power $I_H^2 R_N$ than in the other configurations. As noted above, the dependence on I_{G1} (red circles) shows a difference between positive and negative gate polarity, with the negative polarity being 2.5 times more power efficient in suppressing I_C compared to the positive one.

We have shown that Joule heating is orders of magnitude less efficient in suppressing I_C of our nanowires than a current of high-energy electrons. In addition to these quantitative differences, we gain further insight from the switching probability distributions (SPDs) of our devices. The SPD is the probability for a switch from superconducting to resistive state to occur per unit of source-drain current. The SPD has proven to be a pow-

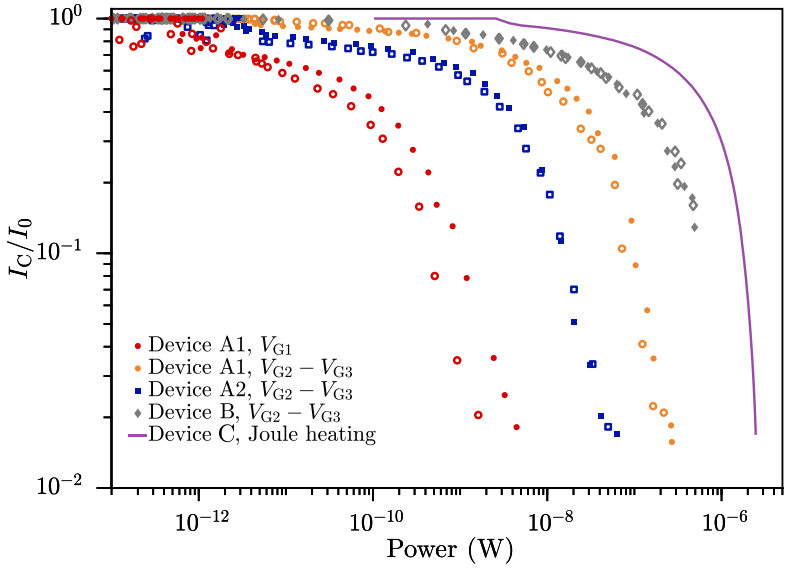

Figure 4.13. Comparison of switching power. Normalized critical current I_C/I_0 as a function of input power for various devices and experimental configurations (see legend). Full and empty markers define positive and negative gate polarity, respectively. The solid purple line indicates the dependence as a function of Joule heating in Device C. Figure adapted from Ref. [139].

erful tool to study Josephson junctions and metallic nanowire properties that are hard to access with standard transport measurements [160, 203]. Figures 4.14a and b show the SPDs of Devices A1 and C, respectively, under various experimental conditions. For these experiments, the source-drain current was swept 20,000 times from zero to 49 μA. For each sweep, the source-drain current value at which a switch to the resistive state occurred was recorded. At low temperature and zero gate voltage, Device A1 exhibited a sharp SPD (blue markers), with a standard deviation $\sigma_I = 47$ nA. At a temperature of 2.2 K (green markers) the SPDs had their maximum at half of the low temperature I_C value, with $\sigma_I = 100$ nA. More detailed analysis, reported in section 4.4.4, revealed that the switching mechanisms at 20 mK and 2.2 K are consistent with quantum phase slips and thermal fluctuations, respectively. Much broader SPDs were obtained by applying a gate leakage current $I_{G1} = 10$ pA (red markers), with $\sigma_I = 2.0$ μA. The finding that the application of a gate voltage results in much broader SPDs than increasing the bath temperature (for equal suppression of I_C) is consistent with the observations in Ref. [160]. However, we show that a similarly broad SPD is also obtained by applying a remote current $I_{G2} = 2.5$ nA (orange circles in Fig. 4.14a, $\sigma_I = 1.2$ μA), that is without any electric field or current reaching the nanowire. Using Device C (Fig. 4.14b), we compare the SPD obtained when I_C is suppressed by 50% either by Joule heating (solid purple line) or by increasing the bath temperature to 2.1 K (green triangles). The two results are indistinguishable, indicating that a resistive heater indeed affects superconductivity

in the same way as an increase in bath temperature, but in a totally different manner than a current of high-energy electrons (gray triangles). The difference between SPDs obtained at high temperature (green markers) and finite gate voltage (red markers) led the authors of Ref. [160] to exclude the presence of electrical currents. This conclusion was however reached under the assumption that a gate current causes heating similar to an increase of the bath temperature. Our results demonstrate instead that a current of high-energy electrons perturbs the superconducting properties of nanowires in a way that is qualitatively and quantitatively distinct from a bare temperature increase, even if the current does not flow into the nanowire but only in its surroundings. This is the third main conclusion of our work.

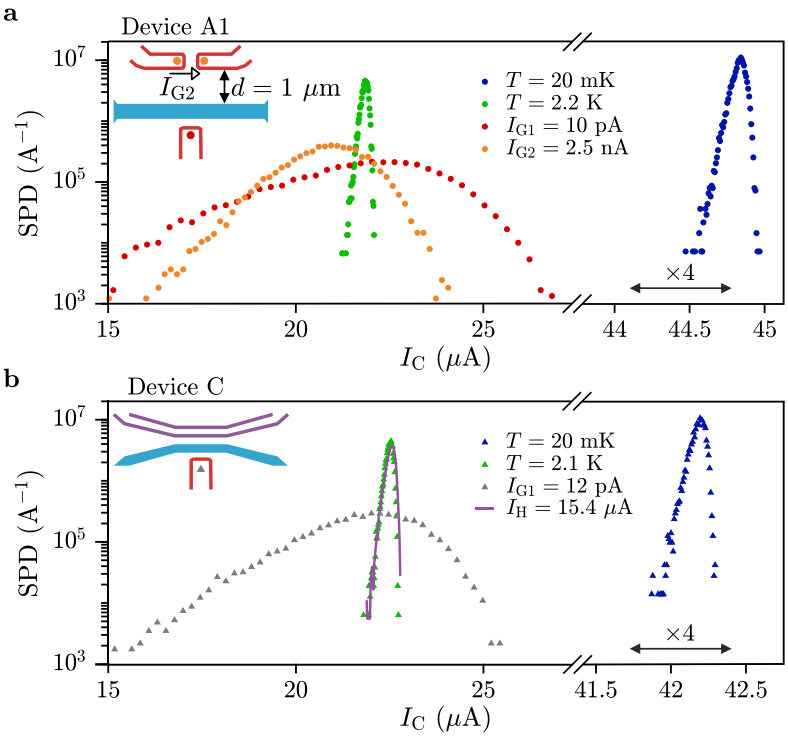

Figure 4.14. Comparison of switching probability distribution. a Switching probability distribution (SPD) in Device A1 as a function of source-drain current I_{SD}. Blue and green circles are obtained at zero gate voltage and for $T = 20$ mK and $T = 2.2$ K, respectively. Red circles are obtained for gate current $I_{G1} = 10$ pA, ($V_{G1} = 5.85$ V), orange dots for remote gate current $I_{G2} = 2.5$ nA ($V_{G2} - V_{G3} = 7.25$ V). Note that the horizontal axis is interrupted and the high current region is horizontally expanded by a factor 4. **b** As in **a**, but for Device C. Blue and green triangles are obtained at zero gate voltage and for $T = 20$ mK and $T = 2.1$ K, respectively. Gray triangles are obtained for $I_{G1} = 12$ pA ($V_{G1} = 5.2$ V), the purple line is obtained for a heater current $I_H = 15.4$ μA. Figure adapted from Ref. [139].

4.3.6. Nature of Generated Phonons

Our observations are consistent with the phenomenology of phonon generation by hot electrons in the substrate. First, we note that phonons with energies above the superconducting gap (500 μeV for TiN [192]) are well known to affect superconducting devices [42, 204–206] (see discussion in section 2.2). Second, electrons accelerated by high electric fields in Si undergo a series of relaxation events over time scales below 1 ns and on mean free paths below 10 nm. Such relaxation most likely happens by emission of optical and acoustic phonons [59, 207–209] (see discussion in section 2.5). Phonons in Si have a maximum energy of the order of 50 meV, which means that a single electron with energies of a few eV can generate a large amount of phonons [210, 211] as it travels between two metallic electrodes. At temperatures below 3 K phonons in Si have long mean free paths (up to 1 μm [212, 213]) and even longer thermalization lengths. It is therefore expected that the emitted phonons reach the nanowire in an out-of-equilibrium state [214, 215].

The electronic mean free path in Si decreases as $|E|$ increases [59, 207], resulting in intense phonon emission close to the metal electrodes, independent of gate voltage polarity (see simulation in Fig. 4.11c) [210]. This may be the reason for the more efficient suppression of I_C when a current is either injected or extracted from the nanowire (see Fig. 4.12c) compared to the case where a current flows between two gates near the nanowire (see Device A2 in Fig. 4.12d). Furthermore, suppression of I_C by a fixed factor requires 2.5 times less power for $V_{G1} < 0$ (Fig. 4.13) compared to $V_{G1} > 0$. This could indicate that electrons reaching the nanowire are not completely thermalized, and can still generate a sizeable number of quasiparticles via electron-electron interaction in the nanowire [197, 216, 217]. Assuming the phononic contribution is similar for both gate polarities (that is, phonon emission is isotropic), we estimate that more than half the suppression of I_C for $V_{G1} < 0$ is due to electron-electron interaction. Future work might use more complex geometries to map out angular anisotropies in the phonon emission and absorption processes.

The broadening of the SPDs with gate voltage is consistent with the nanowire being subject to extremely energetic events, capable of suppressing superconductivity even at small source-drain currents. The characteristic energy spread of such events can be quantified by the Kurkijavi power law [203], which allows one to relate the width of the SPD to an effective energy E_{eff} (see section 4.4.4). For the red dots in Fig. 4.14a we obtain $E_{\text{eff}} \sim 8.6$ meV, consistent with the idea that the energy of a leakage electron (7eV) dissipates in successive scattering events in the substrate before reaching the nanowire. In the case of a remote current (orange dots in Fig. 4.14a) we get $E_{\text{eff}} \sim 6.3$ meV, indicating that on average the phonons thermalize more over the longer distance. The effective energies correspond to temperatures $T_{\text{eff}} \sim 100$ K and $T_{\text{eff}} \sim 73$ K for electron injection into the nanowire and switching via a remote current, respectively. As noted in section 2.2.2, such temperatures do not describe an equilibrium lattice temperature but are a measure of quasiparticle distribution in the superconductor. A possible framework for analysing SPDs in Josephson junctions with large T_{eff} due to high-energy electron injection was recently proposed in Ref. [218].

In Device B we noticed an anomalously large asymmetry in the parametric plot of I_C vs. I_{G1} (see Fig. 4.12c). We have confirmed with three reference devices (see section 4.4.3) that such an asymmetry is a robust feature which arises following the fabrication steps required to etch trenches into the substrate (see section 3.1). Similarly, the efficiency of the remote action of I_{G2} slightly decreased after additional fabrication, even when trenches were not etched. Interestingly, no other sample parameters were affected by the additional fabrication steps. These results suggest that some of the out-of-equilibrium processes taking place in our device are sensitive to the surface treatment of the samples. Measuring Device B, we have shown that out-of-equilibrium phonons are the main responsible for the remote action of I_{G2} on I_C. However, our work does not exclude the presence of additional energy relaxation mechanisms which contribute, together with phonons, to the suppression of I_C, such as photon emission. Previous works detected photons in a variety of devices as a result of tunneling events [219–223] as well as *bremsstrahlung* and carrier recombination of high-energy electrons [224, 225]. It is also well known that superconducting nanowires [226] and Josephson junctions [227] are highly sensitive to the impact of high-energy photons. Both phonon and photon transport may be affected by the additional fabrication steps for the trenching, e.g. by a change in surface roughness or dielectric properties (see discussion in section 2.5). The relative contribution of phonons and photons is estimated comparing the response of Devices A1 and B to $V_{G2} - V_{G3}$ (see Fig. 4.13). Device B required a six times higher power to reach the same I_C/I_0, indicating that the trench blocks 5/6 of the power that would have been otherwise absorbed by the nanowire. If we assume that any photonic contributions are unaffected but the phononic contributions are blocked entirely by the trench we can calculate an upper bound on the photonic contribution in that it cannot be larger than 1/5 of the phononic contribution. Note that the reduced power reaching the nanowire in Device B could still also be carried by phonons which, if traveling deep in the substrate, are also not affected by the trench.

4.3.7. Conclusions

We have reported a comprehensive study of the mechanism responsible for the suppression of critical currents in metallic nanowires in the presence of large gate voltages. We have shown that previously reported features, which were attributed to the electric field on the superconductor, can be obtained in the absence of electric fields. Our data indicates that critical currents are suppressed as a consequence of the relaxation of high-energy electrons, either in the substrate or in the electrodes. Our results also elucidate the mechanism behind the ambipolar suppression of I_C as a function of gate voltage (Fig. 4.11d), which was not fully explained in previous works [138, 198, 199]. The ambipolar suppression of I_C requires both an approximately symmetric gate current, which is experimentally observed (Fig. 4.11e), and an efficient energy equilibration mechanism between gate and nanowire. Energy equilibration is dominated in our devices by energetic phonons spreading through the substrate over distances in excess of 1 μm. While this remote action may pose a limit to device integration density, it could also open new paths for device design. For example, it could be used to develop efficient

superconducting switches [183, 186, 190, 228] that do not require injection of electrons into the switching element, but are instead mediated by high-energy phonons that are guided towards a switching element. It also opens new possibilities to investigate the interplay between out-of-equilibrium phenomena, resulting quasiparticle generation, and superconducting quantum hardware.

Acknowledgments

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4.3.8. Methods

Electrical Measurements

Measurements were performed in a dilution refrigerator with a base temperature of 20 mK. Critical currents I_C were measured by applying a sawtooth wave I_{SD} signal with amplitude 49 μA and repetition rates between 33 and 133 Hz while voltages V across the nanowires were recorded by a digital oscilloscope. The measurement setup was synchronized so that a switch from zero to finite voltage in the oscilloscope could be related to the source-drain current at which the switch occurred. This technique allowed us to reliably extract critical currents down to 700 nA. Critical currents presented in Fig. 4.11 were obtained by averaging 108 such switching events. Sporadic fluctuations of I_C visible at $T \geq 1.5$ K are associated to instabilities of the temperature controller. Switching probability distributions presented in Fig. 4.14 were obtained by recording $20,000$ switches over a time interval of 10 minutes. In order to keep the nanowire potential constant while I_{SD} varies, I_{SD} was generated by sourcing two synchronized sawtooth waves with opposite polarity into 163 kΩ resistors placed at both ends of the nanowire (which add to the existing 2.2 kΩ line resistance). Gate voltages were applied via high-precision source-measure units, which recorded the current flowing into the gate contacts. Gate current data as in Fig. 4.11e and h were obtained after subtracting linear components ranging between 1 and 5 pA V^{-1}, as discussed in section 4.2.1. Such resistive contributions are attributed to spurious leakage paths in our setup.

Electrostatic Simulations[2]

Electric field distributions presented in Fig. 4.11 were produced with finite element 3D electrostatic simulations performed with ANSYS Maxwell. A substrate permittivity of 12 was assumed in order to resemble the electromagnetic properties of silicon, and

[2]Electric field simulations presented in this work were performed by Dr. N. Crescini and Dr. A. Fuhrer

its thickness was set to 1 μm. The metallic layer comprising the nanowire and the gate electrodes was modeled as a 20 nm thick perfect conductor. The upper edges of the structures were filleted with a radius of 3 nm. The geometry of nanowire and gates was generated from the same layout file used for the electron beam lithography of the devices. The fields shown in Figs. 4.11b and f are slices of the three-dimensional simulation taken at half the height of the nanowire. Figure 4.11c is taken perpendicular to the substrate and intersecting the gate electrode. The color scale was saturated to a maximum value of 70 MVm^{-1} to evidence the field distribution, while the full scale reached up to 500 MVm^{-1}.

4.4. Publication II: Supporting Information

4.4.1. Device A2

Device A2 presented in Fig. 4.15 was lithographically equivalent to Device A1 (Fig. 4.11), except for the distance d between gates 2,3 and the nanowire ($d = 1$ μm in Device A1 and $d = 80$ nm in Device A2). A false color image of Device A2 is shown in Fig. 4.15a, together with a simplified measurement schematic. The nanowire under study is depicted blue, the three gates red. Critical current I_C and gate current I_{G1} as a function of V_{G1} are shown in Fig. 4.15b and c respectively. Their characteristics are almost identical to those of Device A1 (see Fig. 4.11d and e). The dependence of Device A2 on $V_{G2} - V_{G3}$ is depicted in Figs. 4.15d and e. Suppression of I_C was again correlated with the increase of the current I_{G2}. This time, sweeping gates 2 and 3 at the same voltage resulted in a partial suppression of I_C. The gray line in Fig. 4.15d shows I_C as a function of the parameter $V_S = 2V_{G2} = 2V_{G3}$. The suppression is correlated to the flow of electrons from gates 2 and 3 into the nanowire (gray line in Fig. 4.15e). The fact that I_C was affected at higher voltages for equal gate biases $V_{G2} = V_{G3}$ compared to the asymmetric bias configuration ($V_{G2} = -V_{G3}$) (markers) speaks against any effect linked to electric fields between gates and nanowire.

4.4.2. Devices B and C

In Figs. 4.12c and d we show a summary of the measurements obtained with Devices B and C using parametric plots of I_C as a function of I_{G1} and I_{G2}. Figure 4.16 shows the datasets from which these parametric plots are obtained. Measurements were performed at temperatures ranging from 20 mK (blue) to 3 K (red). Gate currents are reported for 20 mK.

4.4.3. Reference Devices After Additional Fabrication

We noted that devices which underwent additional fabrication steps, showed changes in some of their properties. Here we discuss this in more detail. In order to etch the trench into the Si substrate (see Fig. 4.12) the entire sample was covered by a hard mask comprising a 2 nm thick SiN_x layer, grown by plasma enhanced atomic layer deposition, and a 210 nm thick SiO_2 layer grown by plasma enhanced chemical vapor deposition. Both depositions were performed at a temperature of 300 °C. After definition of the trench by electron beam lithography, reactive ion etching and inductively coupled plasma etching, the hard mask was removed by immersion in buffered HF. While the trench was etched only in Device B, additional reference devices (RDs) on this chip underwent the same deposition and etching of the hard mask. We refer to these RDs as RD 1, RD 2 and RD 3, respectively. Reference devices had a similar geometry to Device A1, with $d = 1$ μm, 800 nm and 400 nm, respectively.
Figure 4.17a shows a parametric plot of I_C as a function of I_{G1} for all devices that underwent deposition and etching of the SiN_x/SiO_2 hard mask, plus Device A1. The trench in the Si substrate was etched only for Device B. All devices that underwent

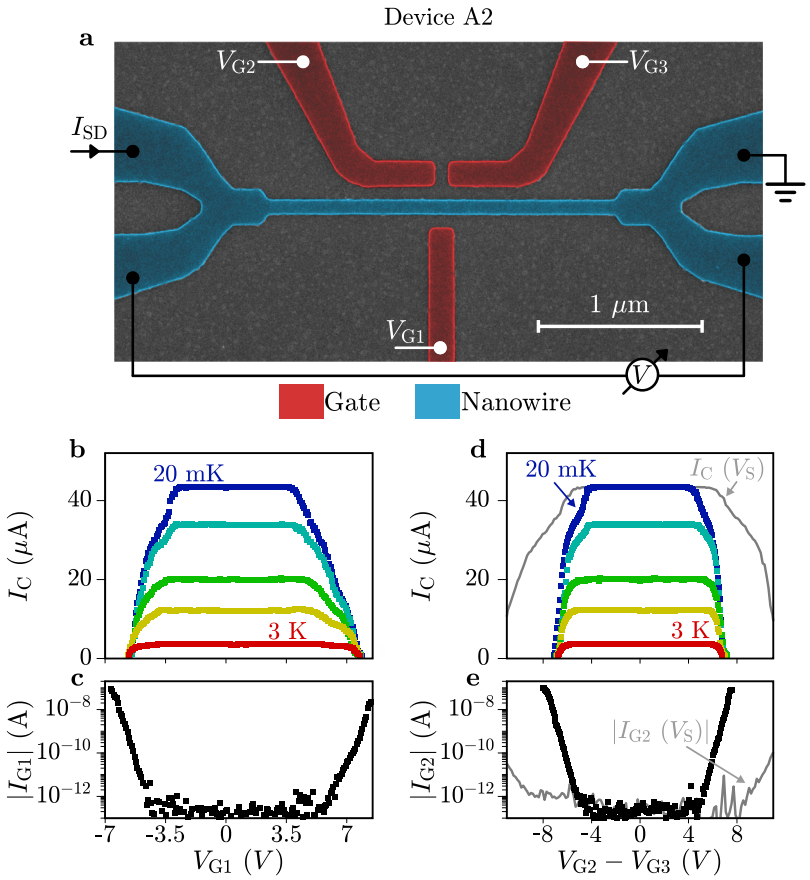

Figure 4.15. Basic characterization of Device A2. a False color scanning electron micrograph of Device A2 and simplified measurement configuration. The nanowire under investigation is depicted blue and the gates red. **b** Critical current I_C as a function of gate voltage V_{G1} at temperatures T of 20 mK (blue), 1.5 K, 2.1 K, 2.5 K and 3.0 K (red). **c** Gate current I_{G1} as a function of V_{G1} at $T = 20$ mK. **d** Critical current I_C as a function of gate voltage difference $V_{G2} - V_{G3}$ for the same temperature values as in **b** (markers) together with I_C as a function of the parameter $V_S = 2V_{G2} = 2V_{G3}$. **e** Gate current I_{G2} as a function of gate voltage difference $V_{G2} - V_{G3}$ measured at $T = 20$ mK (black markers), together with the current I_{G2} as a function of V_S. Figure adapted from Ref. [139].

further processing showed a characteristic asymmetric behavior, with I_C decreasing faster for $I_{G1} < 0$ than for $I_{G1} > 0$. We also found that RDs exhibited a reduced suppression efficiency for $I_{G1} > 0$. Figure 4.17b shows a parametric plot of I_C as a function of I_{G2}. We notice that Device A1, which did not undergo additional fabrication, showed the fastest suppression of I_C. Reference Devices 1, 2 and 3 have quantitatively similar behavior, despite the fact that d varies from 400 nm to 1 μm. This is presumably due to natural sample-to-sample variations following the additional fabrication. It makes extraction of a dependence on d difficult with just these three RDs. However, Device B

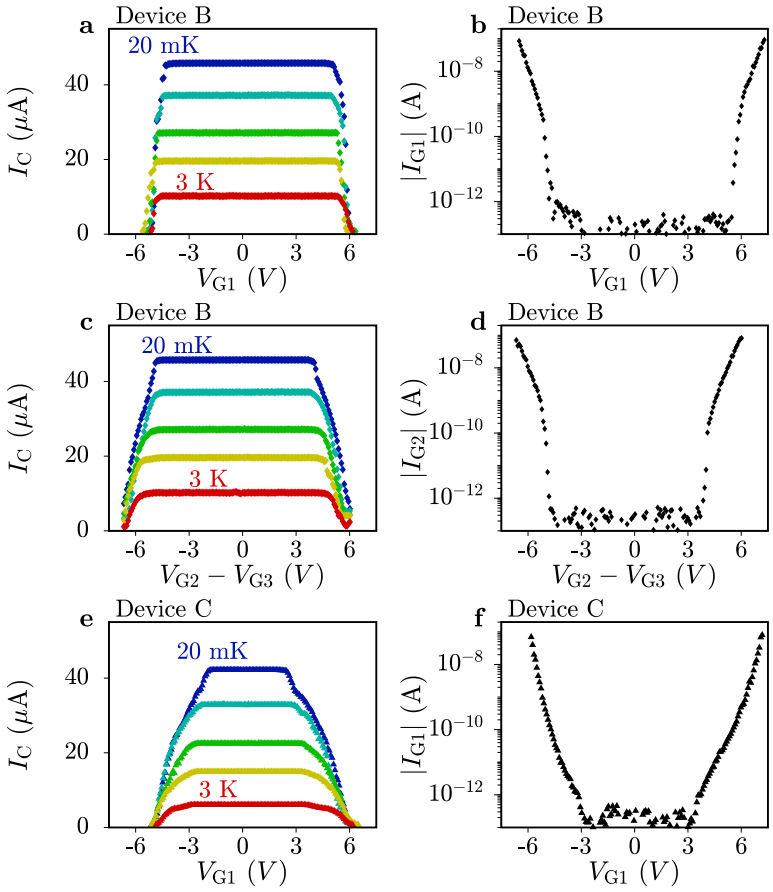

Figure 4.16. Basic characterization of Devices B and C. a Critical current I_C of Device B as a function of gate voltage V_{G1} at temperatures T of 20 mK (blue), 1.5 K, 2.1 K, 2.5 K and 3.0 K (red). **b** Gate current I_{G1} of Device B as a function of V_{G1} at $T = 20$ mK. **c** Critical current I_C as a function of gate voltage difference $V_{G2} - V_{G3}$ of Device B for the same temperature values as in **a**. **d** Gate current I_{G2} as a function of gate voltage difference $V_{G2} - V_{G3}$ measured at $T = 20$ mK. **e** Critical current I_C of Device C as a function of gate voltage V_{G1} for the same temperature values as in **a**. **f** Gate current I_{G1} of Device C as a function of V_{G1} at $T = 20$ mK. Figure adapted from Ref. [139].

clearly stands out from the rest, indicating that the presence of the etched trench in the substrate causes a significant suppression of the long distance coupling between current I_{G2} and nanowire. This clearly substantiates our explanation based on phonons.

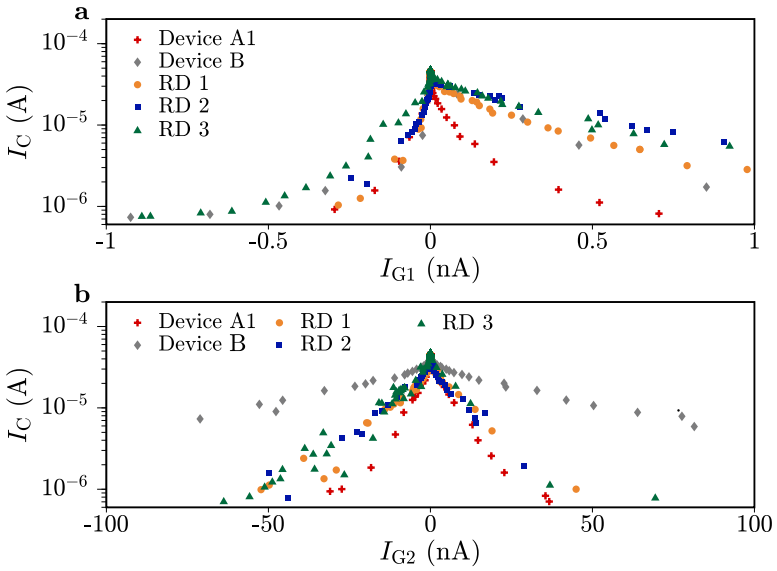

Figure 4.17. Comparison to reference devices. a Critical current I_C as a function of gate current I_{G1} for Device A1, Device B, and three reference devices (RDs). All devices except Device A1 underwent additional fabrication. **b** Critical current I_C as a function of remote gate current I_{G2} for the same devices as in **a**. Device B is the only one with a trench between gates and nanowire. Figure adapted from Ref. [139].

4.4.4. Fit of the Switching Probability Distribution[3]

Figure 4.14 shows the switching probability distribution (SPD) measured in Devices A1 and C. Such measurements were performed by ramping the source drain current I_{SD} and recording, for each sweep, the I_{SD} value where switching from superconducting to resistive state occurred. Data was acquired for 2×10^4 switching events and I_{SD} was ramped at a rate $v = 6.4$ mAs^{-1}. In Fig. 4.18a we plot again the SPDs measured in Device A1 at zero gate voltages and at a temperature of 20 mK (blue circles) and 2.2 K (green circles). In Fig. 4.18b we plot the switching rates (markers), obtained from the data in Fig. 4.18a by KFD transform [229]:

$$\Gamma(I_{SD}) = vP(I_{SD}) \left(1 - \int_0^{I_{SD}} P(I)dI\right)^{-1}, \tag{4.1}$$

where P is the measured switching probability.

We fit to the SPD for each temperature, as shown in Fig. 4.18a, a model for the switching rate of a superconducting nanowire [230] that follows the relation:

$$\Gamma(I_{SD}, T) = \Omega(I_{SD}, T) \left[e^{-U(I_{SD},T)/T} + e^{-U(I_{SD},T)/T_q}\right], \tag{4.2}$$

[3]Fitting of the switching probability distributions was performed by D. Z. Haxell and Prof. C. Bruder

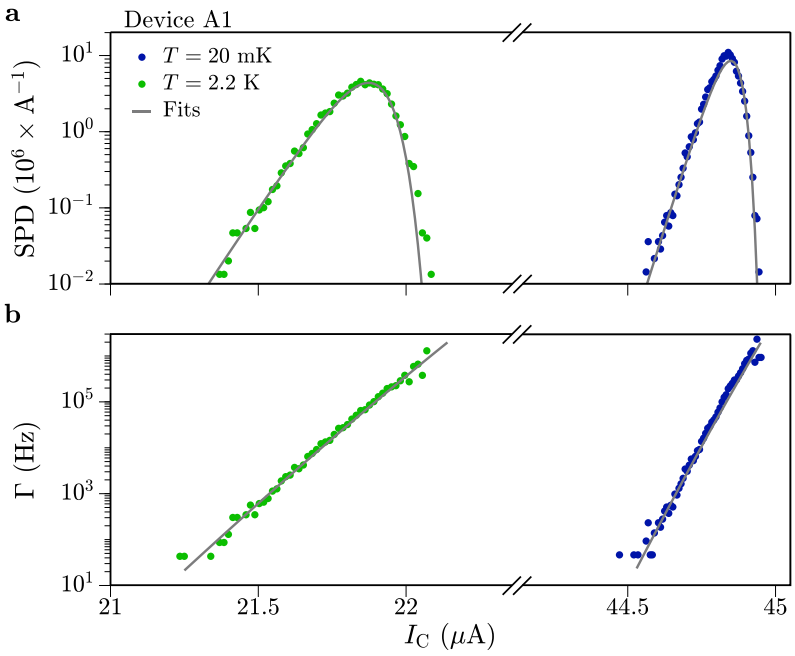

Figure 4.18. Fitting of the switching probability distributions. a Switching probability distribution in Device A1, measured at temperatures T of 20 mK (blue circles) and 2.2 K (green circles) together with fits of a theory of phase escape via macroscopic quantum tunneling and thermal activation (solid gray lines). **b** Phase particle escape rates Γ of the same data as in **a**, calculated with Eq. 4.1 (markers), together with calculations of the escape rate using Eq. 4.2, using the fit parameters obtained from **a**. Figure adapted from Ref. [139].

where the attempt frequency is $\Omega(I_{SD}, T) = \Omega_0 \left(1 - T^2/T_C^2\right)^{3/4} \left(1 - I_{SD}/I_C(T)\right)^{\nu}$ and the potential barrier height is $U(I_{SD}, T) = \frac{\kappa \hbar I_C(T)}{e} \left(1 - I_{SD}/I_C(T)\right)^{\eta}$. I_C is considered to follow Bardeen's formula: $I_C(T) = I_{C0} \left(1 - T^2/T_C^2\right)^{3/2}$. The temperature dependence of the attempt frequency follows from $\Omega(I_{SD}, T) \propto I_C^{1/2}$. For a nanowire forming a phase slip junction, we have $\kappa = \sqrt{6}/2$, $\eta = 5/4$ and $\nu = 5/8$. This model accounts for switching due to macroscopic quantum tunneling (MQT) and thermally activated phase escape mechanisms, which dominate at low and high temperatures respectively. We convert the modeled switching rate Γ to a SPD using the inverse KFP transform [229]:

$$P(I_{SD}) = \frac{\Gamma}{v} \exp\left(-1/v \int_0^{I_{SD}} \Gamma(I) dI\right). \tag{4.3}$$

We fit the logarithm of the probability distribution to optimally account for the shape of the SPD tails. We set $T_C = 3.7$ K, as measured in Ref. [138], and fit with Ω_0, I_{C0} and T_q as free parameters. From the fit, we obtain $\Omega_0 = 67.5 \times 10^{12}$ rads^{-1}, $I_{C0} = 45.7$ μA, $T_q = 0.77$ K. The finding of $T_q \gg 20$ mK confirms that MQT is the dominant phase escape mechanism at low temperatures. With these parameters, one

should be able to calculate the SPD at any given temperature. However, we find that the curve at $T = 2.2$ K is satisfactorily reproduced only by setting the parameter κ to 71% of its theoretical value, similar to previous observations [230]. The value $\kappa = \sqrt{6}/2$ was derived under the assumption of a nanowire width much larger than the superconducting coherence length [27]. This assumption might not be completely justified in the current experiment.

Alternatively to the fit, it is possible to relate the standard deviation of the switching currents σ_I to an effective energy $E_{\text{eff}} = k_B T_{\text{eff}}$ via the Kurkijavi power law [203]:

$$\sigma_I \propto I_{\text{C}}^{1/3} \left(\frac{k_B T_{\text{eff}}}{\Phi_0} \right)^{2/3} \tag{4.4}$$

where $\Phi_0 = h/2e$ is the flux quantum. In section 4.3.6 we used such a relation to extract an effective temperature from the broad SPDs resulting from current injection into the nanowires and out-of-equilibrium phonons.

4.5. Comparison to Other Experimental Studies

Having clarified that the suppression of superconductivity in our devices is not linked to the presence of an electric field, we explicitly compare our results to experimental works where phenomenologically similar suppression was observed, but effects were attributed to electrostatic gating. Tab. 4.1 compares materials, critical currents, and gate powers $P_G\,(I_C = 0)$ from literature to our work.
Experiments in literature were performed on insulating SiO_2 or Al_2O_3 substrates and superconductivity was quenched at $V_G > 10$ V, larger than in our devices on Si substrates. Gate currents were typically $I_G \sim 100$ pA, resulting in gate powers $P_G \sim 1$ nW (see Tab. 4.1). In our experiments on Ti nanowires, a much smaller P_G was sufficient to quench superconductivity. This finding is consistent with the difference in I_C between devices in Refs. [153, 154] and our Ti nanowires. In section 4.1.7 we noted that $P_G \approx 4P_R$ in our devices, irrespective of the superconductor material. Strikingly, a similar relation is true for data in Ref. [154], where $P_R \sim 2$ nW and $P_G \sim 5$ nW (see Tab. 4.1).
Altogether, these findings strongly suggest that out-of-equilibrium electrons and phonons are important not only in our devices, but also in experiments reported in Refs. [153–167].

Table 4.1. Comparison between results in literature and this work. Summary of materials, critical currents I_C, and gate powers $P_G\,(I_C = 0)$ in literature and in our experiments.

Publication	Metal	Substrate	I_C	$P_G\,(I_C = 0)$
De Simoni *et al.* (2018) [153]	Ti	SiO_2	30 μA	∼1 nW
Paolucci *et al.* (2018) [154]	Ti	SiO_2	24 μA	∼5 nW
De Simoni *et al.* (2019) [155]	Al/Cu/Al	SiO_2	6 μA	∼2 nW
De Simoni *et al.* (2020) [159]	Nb	Al_2O_3	30 μA	∼0.8 nW
Our work [138]	Ti	Si	3.2 μA	70 pW
Our work [138]	TiN	Si	45 μA	6 nW
Our work [138]	TiN	SiO_2	29 μA	50 nW
Our work [138]	Nb	Si	190 μA	90 nW

In fact, recent work supports this conclusion. In Ref. [198] the superconducting DOS of a Ti wire was measured by means of tunneling spectroscopy while a voltage was applied to a nearby gate. The authors found that the DOS was accurately described by a model of electron injection into the wire, resulting in a non-thermal quasiparticle distribution (see charge-mode disequilibrium in section 2.2.3). The difference in DOS as a consequence of reducing I_C via thermal versus non-equilibrium quasiparticles was experimentally measured in [218]. Moreover, the authors performed leakage current measurements using lock-in techniques and a separate gate line to reduce stray capacitance. This configuration allowed the detection of gate currents down to ~ 10 fA. The importance of gate currents was further highlighted in experiments on epitaxial InAs/Al nanowires [231], microwave resonators [199, 200], and spatially resolved electron injection using scanning tunneling microscopy [232].

4.6. Conclusions and Outlook

We investigated the quench of superconductivity in gate-tuned metallic nanowires. In our devices, the suppression of I_C was always linked to the flow of a gate current. The gate power required to reach full suppression P_G was closely related to the power dissipated by wires at the retrapping power P_R. The gate power scaled with the superconducting gap and we found the lowest value $P_G = 70$ pA for Ti. We demonstrated that the suppression of I_C is not linked to the presence of electric fields on the nanowire surface, instead gate currents affect superconductivity even if they are routed ~ 1 μm away from the nanowire without reaching the latter. We concluded that a switch to the normal state is triggered by direct injection of quasiparticles into the superconductor and generation of out-of-equilibrium phonons in the substrate as a result of electron relaxation. Impeding the propagation of phonons by means of a trench in the substrate highlighted the importance of such out-of-equilibrium phonons. Their non-thermal nature resulted in a more efficient suppression of superconductivity compared to an on-chip heater placed proximal to the nanowire. Moreover, switching probability distributions were broadened with respect to the case of increased lattice temperature, indicating that switches are triggered by high-energy events.

Our work serves as the starting point for future experiments investigating out-of-equilibrium phenomena in superconductors at so-far unexplored energy scales. We determined an (upper) switching time (90 ns, section 4.2.4), characteristic decay length ($\lambda \sim 1.8$ μm, section 4.1.6) and typical switching power (6 nW in TiN, section 4.3.5), but stressed the convoluted nature of these quantities. Disentangling the relative contributions of phonons in the substrate, quasiparticles and phonons in the superconductor, and potentially the excitation of photons, will be of fundamental importance to build fast, densely integrated, and power efficient devices.
A first experiment in this direction could investigate potential spatial anisotropies of phonons as a function of substrate crystal direction, gate current direction and gate shape. Phonons could be detected using arrays of superconducting tunnel junctions [42] and nanowires. These detectors may be tuned to operate at distinct energy scales by choice of material and geometry. Hence, they could spatially map the relaxation of substrate phonons and complement our results from SPD measurements. Furthermore, detailed studies on the I_C suppression characteristics as a function of V_G (see Fig. 4.1c) in different nanowire geometries could yield important insights. Specifically, clarifying the interplay between electron and phonon actuation, and understanding the role of current crowding close to device contacts [233, 234] could enable high control over the I_C versus V_G behavior in future devices. Further, investigating the long range decay of high-energy phonons is particularly relevant in the context of quantum devices, due to their sensitivity to quasiparticles [235–238].

Superconducting switches investigated in this thesis can readily be used in applications that do not require integration on the same chip as qubits, e.g. routers of microwave

signals and multiplexers [177, 180, 188]. Such devices can be implemented on separately packaged chips [239] far away from a quantum processor, thus eliminating coupling via substrate phonons and photons. Placing capacitors between switches and the quantum chip will further eliminate quasiparticle poisoning through the superconductor.

Applications involving dense integration of qubits and superconducting switches, such as frequency tunable resonators and couplers [199, 240], require more sophisticated solutions.
In a first step, the gate power triggering the switch should be minimized to limit the amount of quasiparticles generated. Our experiments indicate that most efficient switching is achieved for direct injection of electrons and superconductors with small gap (Ti). Detailed studies on various superconductors, substrates, and geometries of gate and channel could maximize the fraction of gate power dissipated in the superconductor. The relation between gate power and retrapping power in these future devices could deviate from that found in our nanowires ($P_\mathrm{G} \approx 4P_\mathrm{R}$), because the retrapping power is homogeneously dissipated by the nanowire, while the gate power is dissipated on the length scale λ ($\lambda \sim 1.8$ μm in our devices). Therefore, P_R is minimized for short nanowires or constrictions, whereas P_G is small for short λ, which is the scenario discussed in the following.

In a second step towards dense integration of superconducting switches with quantum hardware, quasiparticles in the superconducting channel and in the substrate should be confined. Spreading of electrons in the substrate could be inhibited by patterning of quasiparticle traps [236, 241] around gate electrodes, except for the injection area. Spreading of phonons might be controlled by expanding on the idea presented in section 4.3.4, where we blocked phonons using a trench. Future approaches could use sophisticated substrate patterning to steer phonons and block specific phonon frequencies by means of phononic crystals [242]. To confine quasiparticles in the switching segment of the device and thus prevent diffusion into the leads, devices could be fabricated from two superconductors with gaps $\Delta_1 < \Delta_2$. The actuated channel has gap Δ_1 and is contacted on both sides by the second superconductor with gap Δ_2. The diffusion of quasiparticles with $|E| < \Delta_2$ is confined to the channel volume (i.e. the first superconductor with gap Δ_1). Higher-energy quasiparticles that escape into the leads might be extracted via SIS tunnel junctions (see section 2.3), while low-energy quasiparticles could relax in normal metal quasiparticle traps [236, 243].

Instead of confining phonons and quasiparticles to a small volume as discussed above, the opposite situation is advantageous in devices designed for high output impedance and voltage. Here, quasiparticles must spread over a large area to maximize the affected segment of the superconducting channel [188, 228, 244]. Devices operated in non-latching mode ($I < I_\mathrm{R}$) would ideally consist of a long wire with high normal state resistance, closely meandering around the point of quasiparticle injection [190, 245]. We expect that such devices can be immediately realized with the methods and materials presented in

this work, due to the long-ranged spread of phonons, high patterning resolution, as well as high normal state resistivity and homogeneity of TiN films.
For operation in latching mode ($I > I_R$) [188], localized injection of few high-energy quasiparticles into narrow constrictions or weak spots formed by current crowding in sharp bends and kinks [233, 234] could quench superconductivity in long nanowires at extremely low gate power.

5 Semiconductor Epitaxy in Superconducting Templates

"Inspiration is a guest that does not willingly visit the lazy."

Pyotr Ilyich Tchaikovsky (1840-1893)

Today's quantum computers cannot yet solve practical problems faster than their classical counterparts. Quantum supremacy, a crucial scientific milestone on the way to reaching this overarching goal, was first claimed in 2019 [246]. In the work, experiments were performed on a quantum processor with 53 superconducting qubits and 86 tunable couplers, each hard-wired via wideband coaxial lines to bulky room temperature electronics. Future quantum processors are expected to host $\sim 10^8$ physical qubits [247] to perform relevant calculations and enable error correction. At such scale, the current 'brute-force' approach to wiring is clearly not viable. Therefore, developing a fast, low-noise, and low-power interface between quantum hardware and classical electronics is a key challenge on the path to scalable quantum computers.
A proposal to overcome the input-output bottleneck consists of sending microwave pulses from a single waveform generator at room temperature to a switching matrix via a coaxial line. The switching matrix is mounted on the mixing chamber stage and routes the analogue signals to individual qubits, while a classical processor at 4 K operates the switching matrix via a digital address line [180]. In recent studies [18, 248] this quantum-classical interface was further integrated by implementing pulse generation and control electronics onto a single CMOS chip. The CMOS chip was either operated at 3 K [18], or mounted on the mixing chamber stage [248]. In the latter case, the CMOS chip was physically separated from the quantum chip and had a dedicated cooling pillar to improve thermal anchoring to the mixing chamber, which was operated at 100 mK.
To achieve true scalability with lithographically patterned interconnects, monolithic integration of control electronics and quantum hardware [18, 247] will be necessary. However, the power consumption of a Si-CMOS control chip ($\sim$ 60 mW) [18] is large compared to the typical cooling power of a dilution refrigerator at 20 mK (14 μW in our setup[1]). Therefore, monolithic integration with existing CMOS technology is assumed to be feasible only for spin qubits that can operate above mK temperatures [11, 249].
Such limitations might be overcome by electronics based on III-V semiconductors, which

[1] BlueFors LD400 dilution refrigerator.

allow band-gap engineering, can be operated at high frequency, and are expected to dissipate less power compared with Si-CMOS due to their higher carrier mobility [250, 251]. Additionally, they could enable on-chip amplification for readout [252].

In this chapter, we explore a new method that might be key to monolithic integration of III-V-based control electronics and quantum hardware. Specifically, we present epitaxy of InAs nanostructures in lateral templates on a scalable and CMOS compatible platform. Distinct from previous studies, self-aligned (superconducting) TiN contacts are integrated into the templates. The interface to InAs is formed during epitaxy of the latter. In sections 5.1 and 5.2 we reprint our publication [142], where we introduce the method, discuss the intricate dynamics of selective InAs epitaxy, and characterize the TiN/InAs interface. In section 5.3 we go beyond the published results and expand our discussion of the hybrid interface (section 5.3.1) and the optimization steps undertaken to enable hybrid epitaxy (section 5.3.2). In section 5.3.3 we present additional hybrid template geometries and discuss current limitations of hybrid-TASE in section 5.3.4. Finally, we suggest future directions of the method in section 5.4.

The following chapters 5.1 and 5.2 are published in:

Semiconductor Epitaxy in Superconducting Templates
M. F. Ritter, H. Schmid, M. Sousa, P. Staudinger, D. Z. Haxell, M. A. Mueed, B. Madon, A. Pushp, H. Riel, and F. Nichele
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Author Contributions: A.P., H.R., and F.N conceived the experiments. M.F.R. and F.N. designed the samples. M.A.M., B.M, and A.P. deposited TiN layers. M.F.R. and D.Z.H. fabricated the templates and devices. M.F.R. performed semiconductor epitaxy with input from H.S. and P.S.. H.S. and M.S. prepared the lamellae. M.S. and P.S. performed TEM imaging. M.F.R. and F.N. performed the measurements. M.F.R, H.R., and F.N. analyzed and interpreted the data with input from all authors. M.F.R and F.N. wrote the manuscript with input from all authors.

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In chapters 5.3 and 5.4 we discuss additional results which are not published in the above reference.

5.1. Publication III: Semiconductor Epitaxy in Superconducting Templates

5.1.1. Abstract

Integration of high quality semiconductor-superconductor devices into scalable and CMOS compatible architectures remains an outstanding challenge, currently hindering their practical implementation. Here, we demonstrate growth of InAs nanowires monolithically integrated on Si inside lateral cavities containing superconducting TiN elements. This technique allows growth of hybrid devices characterized by sharp semiconductor-superconductor interfaces and with alignment along arbitrary crystallographic directions. Electrical characterization at low temperature reveals proximity induced superconductivity in InAs via a transparent interface.

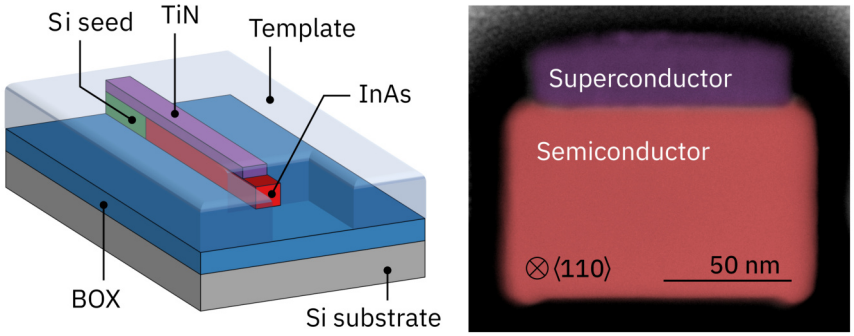

Figure 5.1. Table of contents figure. Copyright 2021 American Chemical Society [142].

5.1.2. Introduction

Hybrid semiconductor-superconductor nanostructures are promising candidates for next generation quantum devices as gate-tunable couplers [253, 254], superconducting qubits [255, 256], Andreev qubits [257–260] and qubits based on Majorana zero modes [261, 262]. Their applications rely on highly transparent semiconductor-superconductor interfaces, a milestone first achieved by the epitaxial growth of Al on InAs nanowires (NWs) [263, 264] and later on 2D electron gases [265, 266]. In recent pioneering approaches, large gap elemental superconductors such as Nb, Ta, V, Sn and Pb [267–271] were coupled to semiconductor NWs via transparent interfaces. These approaches allow exquisite control of the hybrid interface and are compatible with elaborate shadow epitaxy techniques [72] but they are challenging to scale and difficult to integrate in a CMOS architecture.
Here we demonstrate a different approach in which the order of semiconductor epitaxy and superconductor deposition is reversed. A crystalline semiconductor is grown inside an insulating SiO_2 template cavity which features integrated superconducting elements, resulting in flat semiconductor-superconductor hybrid interfaces. This technique is scalable and CMOS compatible, as it is based on the template-assisted selective epitaxy

(TASE) platform [90, 93, 94, 97] where III-V semiconductors are grown inside insulating cavities. In recent years the TASE approach enabled dense integration of III-V nanowires on Si [94], growth in branched geometries [96] and ballistic transport over hundreds of nanometers [95]. Since our approach involves formation of a superconductor-semiconductor interface, we refer to it here as hybrid-TASE.
In this work, we introduce hybrid-TASE with InAs NWs and the superconductor TiN. Nanowires are aligned laterally on the substrate and grown along arbitrary crystallographic directions. We investigate the hybrid interface by scanning transmission electron microscopy (STEM) and present a detailed study of InAs epitaxy in various templates. Finally, we present tunneling spectroscopy of a proximitized hybrid-TASE NW.

5.1.3. Concept of Hybrid-TASE Fabrication

We based the fabrication of hybrid-TASE templates on commercial Si wafers that featured a 150 nm thick buried-oxide (BOX) layer and a 40 nm or 70 nm thin crystalline silicon-on-insulator (SOI) top layer. The SOI layer had a (110) orientation, different from the (001) SOI layers used in previous work [90, 93–97]. This allowed us to laterally integrate III-V nanostructures along different directions on a single chip, such as ⟨100⟩, ⟨110⟩, ⟨111⟩, ⟨112⟩ and even lower symmetry directions.
Figures 5.2a-f show a simplified schematics of the hybrid-TASE process flow, while Figs. 5.2g-i show scanning electron microscope (SEM) images of a typical device at three fabrication steps, respectively. A detailed description of the process flow is reported in section 5.1.9. In the first step, the SOI layer was metallized by sputtering of a 25 nm thick layer of TiN (Fig. 5.2a). The TiN layer was polycrystalline with with a typical grain size of approximately 5 nm. Self-aligned TiN/SOI bilayer nanowires were dry etched in a single step (Fig. 5.2b) and TiN was locally wet etched from one end of the wire (Fig. 5.2c), leaving the underlying SOI unaffected. The patterned structures were covered in a conformal 40 nm thick SiO_2 template, which was locally etched at the template termination (Fig. 5.2d and g). Selective wet etching of the SOI resulted in hollow cavities with sidewalls of SiO_2, the BOX layer as floor and TiN as ceiling. The length of the cavity was determined by the SOI etching time (Fig. 5.2e and h). Cavities formed in this way terminated in a crystalline Si surface originating from the original SOI layer, serving as a nucleation seed for InAs heteroepitaxy. InAs nanowires were grown inside the template structures via metal-organic chemical vapor phase epitaxy (MOVPE) (Fig. 5.2f and i) using trimethylindium (TMIn) and tertbutylarsine (TBAs) as precursor species. Height and width of the resulting InAs nanowires were determined by the SOI layer thickness and template width, respectively. The NW length was determined by the cavity length and growth time. We reached a yield of about 50%, meaning that half of the InAs nanowires generally nucleate at the Si seed and radially expand to the template sidewalls.
Our choice of TiN as the superconductor was motivated by its compatibility with the hybrid-TASE process flow. In particular, TiN can be etched selectively to Si and SiO_2 while it is not attacked by typical Si and SiO_2 etchants. This property is crucial for the patterning of hybrid-TASE templates. TiN is chemically stable and has a melting

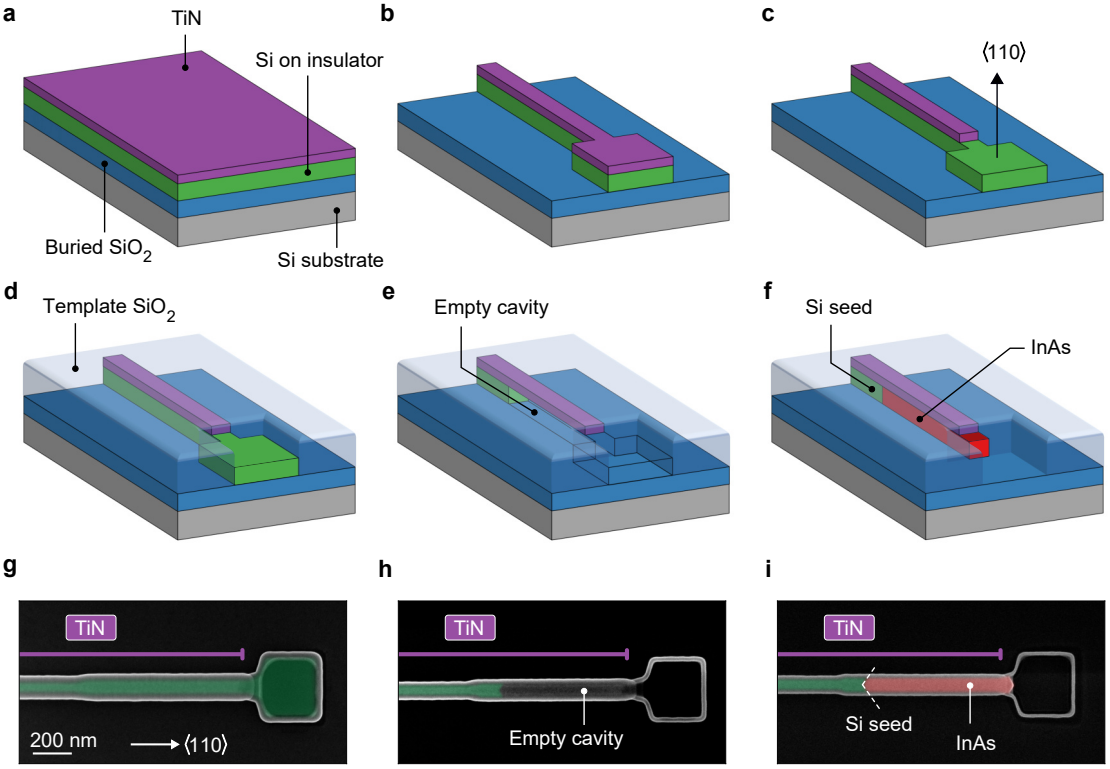

Figure 5.2. Deterministic hybrid-TASE nanowire growth inside a lateral template. **a** A silicon-on-insulator wafer consisting of a thin Si layer (green) separated from the Si substrate (gray) by a buried SiO_2 layer (blue) is metallized with a 25 nm thick film of TiN. **b** Self-aligned TiN/SOI bilayer structures are patterned. The structure terminates in a square. **c** TiN is etched from this square. **d** Devices are covered in a conformal 40 nm template SiO_2 layer (light blue). SiO_2 is locally etched to expose the Si square at the wire end. The TiN stripe remains protected. **e** Selective etching of the SOI creates a cavity formed by template SiO_2 and the TiN stripe. A segment of Si remains at the end of the cavity. **f** The surface of the Si segment acts as a seed for epitaxial growth of InAs nanowires (red). InAs nanowires are guided by the template cavity and an interface to TiN is formed during InAs epitaxy **g,h,i** Top-view SEM micrographs of the fabrication steps in subfigures **d** ,**e** and **f**, respectively. Regions of Si (green) and InAs (red) are false colored, they are located below the TiN stripe and SiO_2 template layer. The extent of the TiN stripes integrated into the template is indicated by purple lines. Dashed lines in **i** indicate Si {111} seed facets. Copyright 2021 American Chemical Society [142].

point much higher than the temperatures reached during template fabrication and semiconductor epitaxy. Furthermore, the TiN surface exposed inside our templates allowed selective InAs growth with respect to the Si seed, as we will outline below. These requirements exclude materials commonly used such as Al, however, we envision that the hybrid-TASE technique can be generalized to other nitride superconductors with similar

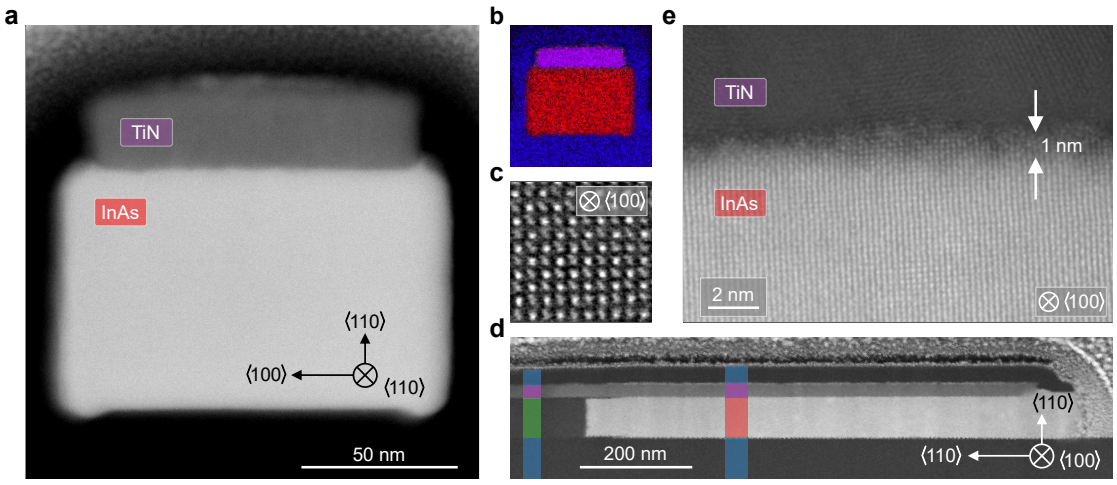

Figure 5.3. Structural study of hybrid-TASE nanowires and the InAs/TiN hybrid interface using STEM. a Transversal cross section of a hybrid-TASE nanowire similar to that of Fig. 5.2i. The ⟨110⟩ aligned InAs nanowire features a rectangular cross section and is grown inside a hybrid template formed of TiN and SiO_2. **b** EDX elemental mapping of the cross section shown in **a** with In (red), Ti (purple) and Si (blue). The frame size is 160 nm × 160 nm. **c** High-resolution STEM image of InAs along the ⟨100⟩ zone axis. The frame size is 2.3 nm × 2.3 nm. **d** Overview of the InAs crystal of **c** imaged along the ⟨100⟩ zone axis. The cut is performed along the axis of the device in Fig. 5.4e. The Si seed and the InAs nanowire form an interface at the InAs nucleation site, a stripe of TiN covers both materials. Colored boxes indicate SiO_2 (blue), Si (green), InAs (red) and TiN (purple), respectively **e** Typical zoom-in on the hybrid interface formed by TiN and InAs shown in **d**. The interface roughness between polycrystalline TiN and the InAs single-crystal is approximately 1 nm. Copyright 2021 American Chemical Society [142].

refractory properties such as NbN, VN and TaN.

5.1.4. Structural Analysis and Hybrid Interface

We investigated the structural quality of our nanowires by high-resolution scanning transmission electron microscopy (STEM) and energy-dispersive X-ray spectroscopy (EDX) at 200 kV on lamellae prepared across and along the nanowire axis via focused ion beam techniques. Figure 5.3a presents an annular dark field (ADF)-STEM cross sectional view of a hybrid-TASE nanowire similar to the device shown in Fig 5.2i. The InAs crystal (bright) exhibits a rectangular cross section with a flat interface to TiN.[2] EDX elemental mapping shown in Fig. 5.3b highlights the elemental distribution of the templated nanowire with In (red), Ti (purple) and Si (blue). A representative high

[2]We attribute the slightly rounded corners and the expansion of the InAs crystal beyond the width of the TiN segment to an enlargement of the SiO_2 template during a final HF etch prior to InAs epitaxy (see section 5.1.9).

magnification ADF-STEM image of the InAs crystal along the ⟨100⟩ zone axis is presented in Fig. 5.3c. Figure 5.3d shows the view along the ⟨100⟩ zone axis, obtained by cutting the device illustrated by the SEM image in Fig. 5.4e. Colored boxes in Fig. 5.3d highlight the material stack with SiO_2 (blue), Si (green), InAs (red) and TiN (purple), respectively. The Si seed, discussed in more detail below, is visible on the left-hand-side of Fig. 5.3d as a vertical interface. We investigated the interface between TiN and InAs by recording high-resolution ADF-STEM images of this region along the growth axis. A typical example is shown in Fig. 5.3e. The interface between InAs and poly-crystalline TiN shows an interface roughness on the order of 1 nm, furthermore EDX elemental line profiles (see section 5.2.3) indicate a small amount of contaminations. A lower bound for the roughness of the hybrid interface was set by the initial SOI layer roughness of 0.3 nm rms, which is likely to increase during processing prior to TiN deposition (see section 5.1.9). We also point out that the lamella thickness of $\sim$ 80 nm might cause the observed interface roughness to appear larger. In previous studies, the roughness of metal top surfaces was found to promote detrimental parasitic nucleation during semiconductor epitaxy [272]. In contrast, our approach utilizes the pristine and freshly exposed TiN back surface, which allows selective growth in geometries with high aspect ratio.

5.1.5. Nucleation and Growth Uniformity

The morphology of the Si seed from which III-V epitaxy started is detailed in Fig. 5.4. Figure 5.4a shows a high-resolution ADF-STEM image of the interface between Si and InAs from the device presented in Fig. 5.3d. As visible in Fig. 5.2i, the Si seed terminates into {111} facets, inclined with respect to the nanowire axis. The projection of such V-shaped facets onto the ⟨100⟩ viewing plane of the TEM micrograph results in decreased contrast close to the Si/InAs interface. Similarly, the native SiO_2 layer on Si appears to extend over InAs. In section 5.2.4 we provide schematics of the seed and an ADF-STEM overview image of the seed region.

The epitaxial relation between the Si seed and the grown InAs NW is evidenced by fast Fourier transforms (FFTs) of the Si seed (Fig. 5.4b), the Si/InAs heterointerface (Fig. 5.4c) and the InAs nanowire (Fig. 5.4d) along the ⟨100⟩ zone axis.[3] The analysis shows a clear transition from the diamond cubic crystal structure of Si to the zinc blende crystal structure of InAs. The mismatch in lattice constant between Si and InAs is resolved in Fig. 5.4c as double peaks in the FFT. The alignment between the two peaks demonstrates the epitaxial relation between the two materials, confirming InAs nucleated from Si and not from TiN. Detailed comparison of the alignment of the SOI and InAs crystal revealed a rotation of $\sim 1^\circ$ along the ⟨100⟩ zone axis. This is expected in TASE epitaxy where rotations of up to 3° are observed [90]. EDX data of the seed interface, as well as further FFTs of the InAs crystal which confirm that its epitaxial relation is maintained along the full NW, are presented in sections 5.2.3 and 5.2.5, re-

[3]The FFTs are computed from an overview image of the seed area larger than the frame shown in Fig. 5.4a. More FFTs computed along the nanowire length are reported in section 5.2.5.

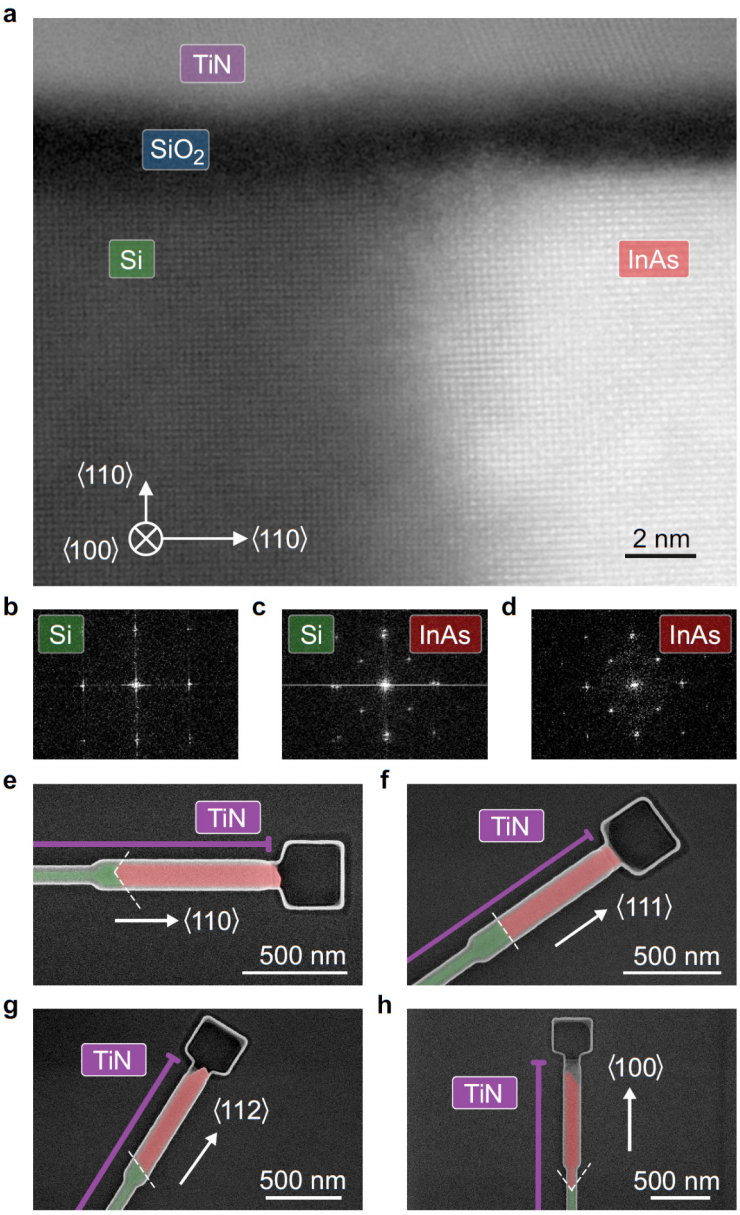

Figure 5.4. Nucleation and growth uniformity of InAs hybrid-TASE. a Detailed view of the seed area of Fig. 5.3a imaged along the ⟨100⟩ zone axis. {111} facets of the seed are inclined with respect to the zone axis (see text). **b, c, d** Fast Fourier transforms of the Si seed layer, the heteroepitaxial interface of Si and InAs and the InAs NW, respectively. **b** and **d** highlight the single crystaline structure of Si seed and hybrid-TASE grown InAs, double spots in **c** are testament to different lattice constants of the materials. **e** Top-view false color SEM micrograph of a hybrid-TASE NW oriented along ⟨110⟩ direction. The entire length of the InAs wire is covered by a TiN stripe (purple line). **f, g, h** As in **e** but with templates oriented along ⟨111⟩, ⟨112⟩ and ⟨100⟩ direction, respectively. Si {111} seed facets are indicated by dashed lines. Copyright 2021 American Chemical Society [142].

spectively.
The key concept of hybrid-TASE epitaxy, that is the formation of a hybrid interface during semiconductor growth, required the InAs crystal to radially expand to the template walls. We achieved this using a high V/III precursor ratio of 150 and a nominal temperature of 550 °C to promote growth of {110} facets deep inside cavities, where the local V/III ratio was reduced due to differing diffusion mechanisms of the precursor species [93]. Furthermore, these conditions enabled an isotropic growth rate along a plethora of orientations. We present devices grown in hybrid templates along the ⟨110⟩, ⟨111⟩, ⟨112⟩ and ⟨100⟩ direction in the false colored SEM micrographs of Figs. 5.4e-h. Further examples along lower symmetry directions, which are challenging to grow using standard approaches [80], are shown in section 5.2.1. Such NWs are interesting for the investigation of spin-orbit interaction along low-symmetry crystallographic directions [273–275]. Independently of the wire direction, all devices featured {111} seed facets which were oriented perpendicular to the wafer surface, while their alignment with respect to the InAs NW axis changed depending on the template orientation. The formation of {111} facets is a consequence of the anisotropic Si wet etch, which favors the formation of {111} facets. In the particular case of ⟨111⟩ aligned templates, this resulted in a single seed and growth facet, perpendicular to both the wafer plane and the wire axis (Fig. 5.4f). Finally, we observed that the presence of a TiN layer impacted the growth dynamics of our nanowires. In particular, hybrid-TASE nanowires displayed an axial growth rate which was up to 4 times higher than that of wires grown with the standard TASE method. Further epitaxy experiments at decreased precursor flow indicated an increased V/III ratio inside hybrid-TASE templates compared to TASE, likely due to enhanced surface diffusion of the precursors on the TiN surface. An enhanced surface diffusion could originate from a higher reactivity of the TiN surface compared to SiO_2, which would result in a higher sticking coefficient and a decreased desorption of precursor species.[4] In section 5.2.2 we provide a detailed discussion of the altered growth dynamics in hybrid templates.

5.1.6. Tunneling Spectroscopy Experiments

We performed electrical characterization of the hybrid TiN/InAs interface by means of finite bias spectroscopy on the device of Fig. 5.5a. It featured a total length of 1.16 μm and a cross section of 50 nm × 80 nm. We altered step 3 of the hybrid-TASE process flow (Fig. 5.2c) such that TiN was etched on a 560 nm long segment, allowing for a normal metal probe to be integrated after InAs growth. We also patterned side gates and tunneling gates on either side of the wire. Both the normal contact and the gates (yellow in Fig. 5.5a) were fabricated by evaporation of Ti/Au and lift-off. On the seed side of the wire, the TiN layer branched off to bonding pads.[5] The Si substrate (Fig. 5.2a) was metallized on the backside by evaporation of Ti/Pt and used as a global back-gate.

[4] We are grateful to Referee 1 for pointing out that a higher sticking coefficient could be the origin of the enhanced growth rate when a TiN surface is present.
[5] This specific device was grown with a precursor ratio of V/III=70.

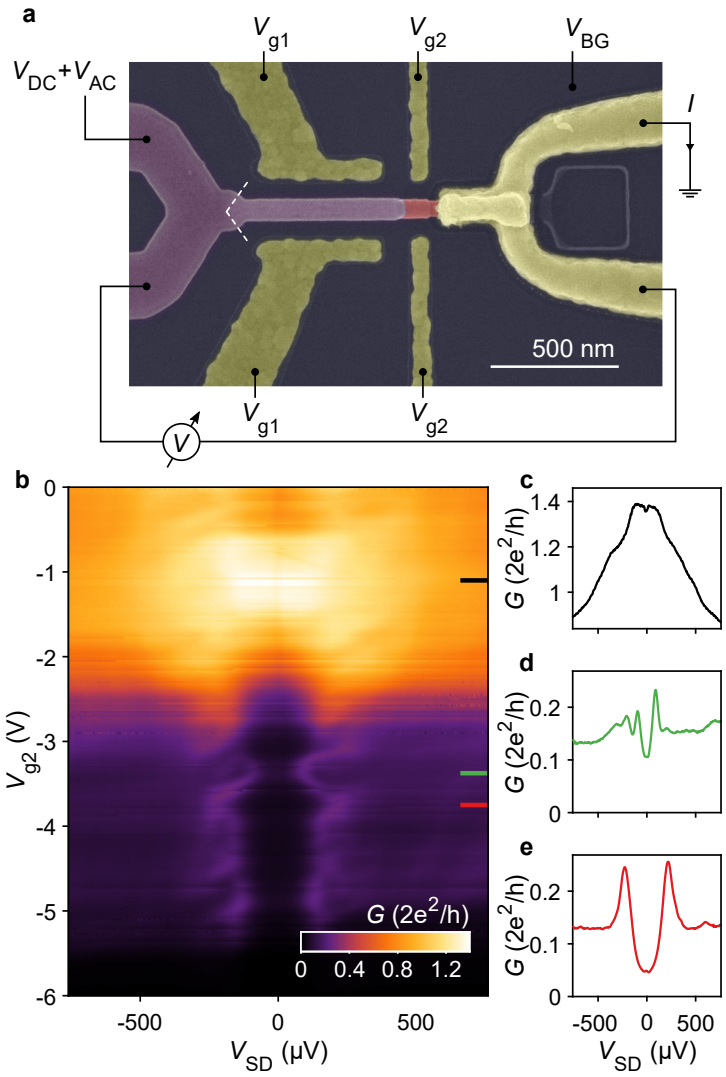

Figure 5.5. Finite bias spectroscopy of a hybrid-TASE tunnel junction. **a** False colored SEM micrograph of a hybrid-TASE device where InAs (red) is grown inside a template with integrated TiN segment and contacts on one side (purple). Normal contacts and gates (yellow) are patterned with lift-off. Dashed lines indicate the InAs nucleation site below TiN. **b** Finite bias spectroscopy of a hybrid-TASE tunnel contact formed by tuning the tunneling gate voltage V_{g2} at $V_{BG} = -15$ V and with the side gate voltage $V_{g1} = 0$ V. **c, d, e** Line cuts of the data in **b** at $V_{g2} = -1.1$ V, $V_{g2} = -3.375$ V and $V_{g2} = -3.75$ V, respectively. Copyright 2021 American Chemical Society [142].

Measurements were performed by low-frequency lock-in technique at a temperature of 20 mK. A voltage bias $V_{DC} + V_{AC}$ was applied at one end of the nanowire while the resulting voltage difference V and current to ground I were measured via a differential voltage amplifier and a low impedance IV converter, respectively. As the Si handle-wafer

became insulating below 10 K, we used the back-gate voltage V_{BG} to define the operating point of the device at 14 K (see section 5.2.6) and subsequently cooled down the device to mK temperatures. Devices prepared in this way showed remarkable electrical stability over several days of measurements.
Data presented in Fig. 5.5b was obtained by applying a voltage V_{g2} to two tunneling gates (see Fig. 5.5a), and recording the differential conductance G as a function of the source-drain voltage V_{SD}. Three distinct regimes are identified, based on the normal state transmission of the tunneling probe (see linecuts in Figs. 5.5c-e). At $V_{g2} = -1.1$ V the conductance at small V_{SD} was enhanced, a hallmark of Andreev reflection (Fig. 5.5c). The conductance spectrum at $V_{g2} = -3.375$ V highlights discrete subgap states (Fig. 5.5d). Further decreasing the transmission, at $V_{g2} = -3.75$ V, we measured an induced superconducting gap of $\Delta^* = 220$ μeV (Fig. 5.5e). These findings are consistent with a transparent semiconductor-superconductor interface, with electronic transport governed by Andreev reflection [263, 266, 276]. The induced superconducting gap Δ^* depended on the specific gate tuning and we achieved the highest value of $\Delta^* = 300$ μeV at $V_{BG} = 0$ V and $V_{g1} = -5$ V. For bulk TiN the expected superconducting gap is $\Delta = 500$ μeV [192]. A possible cause for the reduced superconducting gap in our device is degradation of TiN during fabrication. In section 5.2.7 we present measurements on reference TiN nanowires which were exposed to different steps of the hybrid-TASE fabrication. Patterned reference NWs showed a critical temperature of 3.5 K while wires encapsulated in a SiO_2 template and annealed at 600 °C for 30 s exhibited a reduced T_C of 2.8 K. In contrast, T_C of TiN wires encapsulated in a SiN_x template did not decrease after annealing at 600 °C for 30 minutes, simulating conditions during InAs epitaxy. To avoid degradation of the superconductor during high temperature processing, future devices could, therefore, use a SiN_x template dielectric, as routinely employed in selective-area-grown devices [277].

5.1.7. Discussion

Our approach to semiconductor-superconductor device fabrication is complementary to existing methods, which are based on the in-situ growth of elemental superconductors on semiconductors at low temperatures. Furthermore, hybrid-TASE enables new semiconductor-superconductor material combinations. In particular, TASE was already demonstrated for semiconductors such as GaAs, InSb and GaSb [90, 93, 94]. Future hybrid devices might employ superconductors which are chemically similar to TiN, but characterized by higher critical temperatures and magnetic fields, such as NbN and VN, making the hybrid-TASE platform particularly interesting for applications requiring high magnetic fields. The compatibility of hybrid-TASE with standard CMOS fabrication can furthermore enable 3D integrated [94] cryogenic qubit control electronics at few K temperature such as amplifiers and multiplexers with low power dissipation, beyond the offerings of Si-CMOS [250].

5.1.8. Conclusion

We presented epitaxy of InAs nanowires on Si inside superconducting TiN/SiO_2 lateral cavities, a scalable and CMOS compatible approach to semiconductor-superconductor hybrids. We demonstrated InAs growth in a large variety of crystal directions and observed enhanced growth rates in the presence of exposed TiN. Transport spectroscopy revealed proximity induced superconductivity in the semiconductor, with a transparent hybrid interface.

Acknowledgments

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5.1.9. Methods

Marker Fabrication

Before patterning the hybrid-TASE templates, we defined markers for optical and electron beam lithography. First, we deposited a 30 nm layer of SiO_2 via plasma-enhanced chemical vapor deposition, then a 100 nm layer of W via sputtering. Using electron beam lithography, we exposed markers on a AR-N 7520.17 negative tone resist and transferred the pattern into W by reactive ion etching (RIE) in N_2/SF_6 plasma, using the SiO_2 layer as etch stop. After removing the resist, we encapsulated the markers in 300 nm SiO_2 grown with plasma-enhanced chemical vapor deposition using tetraethyl orthosilicate as precursor. The wafers were annealed at 750 °C for 30 s and device areas were defined via optical lithography and buffered hydrofluoric acid (BHF) etching by exposing the SOI layer in regions where hybrid-TASE templates will be patterned.

Fabrication of Templates with Integrated TiN Segments

Wafers were cleaned in concentrated piranha solution (sulfuric acid and hydrogen peroxide 2:1) followed by a rinse in ultrapure water and cleaning in a 600 W oxygen plasma. The native SiO_2 layer formed in this way was thick enough to protect the back face of the TiN layer during wet etching of Si, greatly enhancing the fabrication yield. We will comment on the importance of this SiO_2 layer in more detail below.

We sputtered a 25 nm thick layer of TiN on the entire wafer via DC reactive magnetron sputtering (Fig. 5.2a).
We patterned Si/TiN bilayer nanostructures via inductively coupled HBr plasma etching. For this purpose we defined a 50 nm thick layer of hydrogen silsesquioxane (HSQ) negative tone resist as etch mask, using electron-beam lithography. After etching, HSQ was removed in diluted hydrofluoric acid. Typical Si/TiN wires patterned in this fashion were 2 μm long and had a width ranging from 40 nm to 100 nm. The lithographically defined width corresponds to the width of InAs nanowires grown inside hybrid-TASE templates. Si/TiN wires terminated in a square, as shown in Fig. 5.2b.
To ensure adhesion of a 80 nm AR-P 6200.04 positive tone resist layer on TiN, we encapsulated the structures in a 5 nm SiO_2 layer deposited via oxygen plasma-enhanced atomic layer deposition (ALD). Using electron-beam lithography, we defined regions for TiN etching and etched the exposed ALD grown SiO_2 layer in BHF. We selectively removed TiN in a wet-etch solution of H_2O, H_2O_2 and NH_4OH (5:2:1) at 65 °C [278] as indicated in Fig. 5.2(c).
The resist was removed with organic solvents and a 40 nm layer of SiO_2 was deposited using oxygen plasma-enhanced ALD at 300 °C. This SiO_2 layer will guide the growth of III-V structures and we refer to it as SiO_2 template. To reduce the template etch rate in diluted HF, we annealed devices at 600 °C for 30 s in Ar/H_2 atmosphere. Using electron beam lithography on a 80 nm layer of AR-P 6200.04 positive tone resist, openings in areas where TiN had been etched previously were defined. We transferred the openings into the SiO_2 template using RIE in Ar/CHF_3 plasma and BHF etching. In this way, the Si square at the end of each wire was exposed. Importantly, the exposed area did not overlap with TiN segments on top of the sacrificial Si wire, i.e. TiN features remained protected by SiO_2. This situation is sketched in Fig. 5.2d.
The exposed Si square allowed us to selectively etch the sacrificial Si structures, creating cavities formed by template SiO_2 and TiN. We etched Si in a 2 % tetramethylammonium hydroxide (TMAH) solution at 80 °C. The cavity length was determined by the etching time which was chosen such that a segment of Si remained, as shown in Fig. 5.2e. Typical Si etching times to achieve a back etch of 1.2 μm ranged from 12 min to 15 min. We found that the presence of a native SiO_2 layer below TiN as mentioned above was crucial to achieve consistent Si etching results. Without this layer, Si etch rates were reduced drastically, potentially due to interaction between TMAH and TiN. Because TMAH etches Si anisotropically, residual Si segments exhibited typical {111} facets as seen in Fig. 5.2h. The facets were oriented perpendicular to the (110) wafer surface.

InAs Epitaxy Inside Hybrid-TASE Template Cavities

Prior to MOVPE semiconductor growth, we immersed the templates in diluted hydrofluoric acid H_2O:HF 20:1. The etching served two purposes as it removed both the native SiO_2 protection layer below the TiN segments and etched native SiO_2 from the Si {111} seed facets while creating hydrogen terminated facets. At the same time, the inner template dimensions increased slightly. This effect can be seen in Fig. 5.3a, where the InAs nanowire was approximately 20 nm wider than the TiN region.

We promptly transferred chips into a MOVPE growth reactor where they were annealed at 600 °C for 5 min under TBAs flow. H_2 was used as carrier gas and InAs growth started as we introduced TMIn into the reactor. InAs growth was performed at a pressure of 60 Torr at temperatures of either 550 °C or 600 °C and V/III ratios between 70 and 150. Typical growth times ranged from 9 min to 11 min. The dynamics of InAs epitaxy in hybrid-TASE templates are described in section 5.2.2.

Device Contacting and Gates Patterning

After InAs growth, we spun a double layer of PMMA 669.04 (300 nm) and AR-P 672.03 (100 nm) resist and patterned device contacts with electron beam lithography. After resist development in methyl isobutyl ketone (MIBK) and isopropanol (IPA) with ratio 1:2, we etched the SiO_2 template with BHF in exposed regions and passivated the InAs surface by immersion in 2 % ammonium sulfide solution prior to evaporation of Ti (10 nm) and Au (150 nm). After lift-off in dimethyl sulfoxide (DMSO), we spun a single layer of AR-P 672.03 (100 nm) and patterned gate structures via electron beam lithography. The resist was developed in MIBK:IPA (1:2) and layers of Ti (5 nm) and Au (20 nm) were evaporated prior to lift-off in DMSO. After etching of native SiO_2 in BHF, we metallized the Si handle wafer by evaporation of Ti (5 nm) and Pt (40 nm). During these steps, devices on the chip were protected by a 6.2 μm thick layer of AZ 4562 optical resist.

5.2. Publication III: Supporting Information

5.2.1. Hybrid-TASE Epitaxy Along Low-Symmetry Directions

Uniform III-V semiconductor growth inside hybrid-TASE templates in multiple crystallographic directions can be of great importance for applications that require engineering of spin-orbit interaction [273–275]. In Fig. 5.4e-h we demonstrated that an isotropic growth rate in high-symmetry directions was accomplished via growth at As rich atmosphere with V/III=150. In Fig. 5.6 we demonstrate growth in the lower symmetry ⟨113⟩, ⟨114⟩, ⟨115⟩ and ⟨116⟩ directions. The same results were obtained for templates oriented in ⟨115⟩, ⟨116⟩, ⟨221⟩, ⟨331⟩ and ⟨441⟩ direction (not shown). As discussed below, these results are not only a consequence of the global growth conditions in the reactor but also due to the presence of an exposed TiN surface inside the template cavities.

5.2.2. InAs Epitaxy Dynamics in Hybrid-TASE Templates

InAs epitaxy inside hybrid-TASE templates exhibited significantly altered growth dynamics compared to TASE epitaxy inside full SiO_2 templates. Our observations include a change of facet morphology and increased axial growth rate. In the following, we investigate these effects at a range of epitaxy conditions and draw a direct comparison to TASE reference growth.

To study the impact of exposed TiN inside the templates, we patterned SiO_2 reference

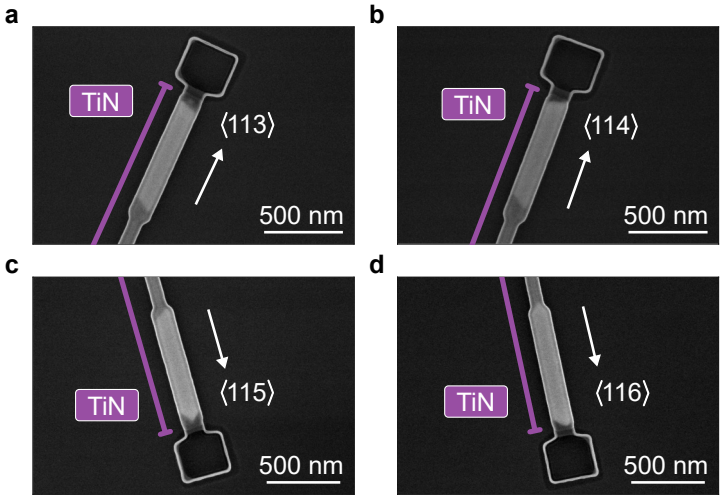

Figure 5.6. Hybrid-TASE InAs epitaxy in lower symmetry directions. Templates have similar aspect ratio and equal growth conditions as devices shown in Fig. 5.4 but different crystallographic alignment in **a** ⟨113⟩, **b** ⟨114⟩, **c** ⟨115⟩ and **d** ⟨116⟩ direction, respectively. Purple lines indicate the extent of TiN stripes inside hybrid templates. Copyright 2021 American Chemical Society [142].

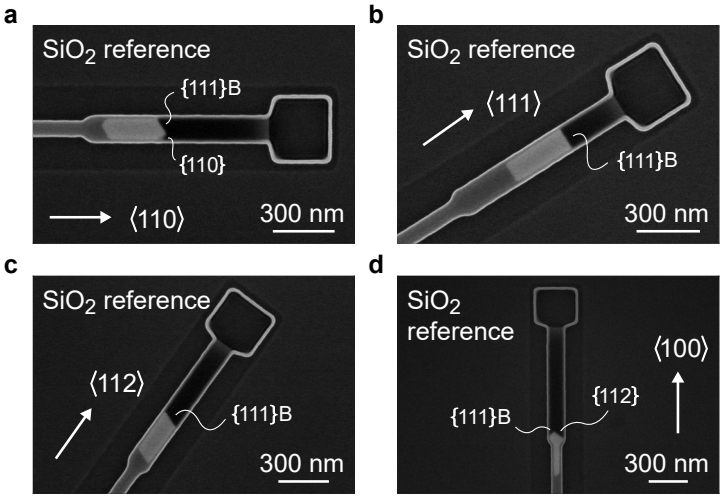

Figure 5.7. TASE reference epitaxy. InAs growth inside TASE templates without integrated TiN surface. Reference templates have a similar aspect ratio and were exposed to equal growth conditions as hybrid-TASE templates presented in Fig. 5.4. Crystallographic alignment of normal reference templates in **a** ⟨110⟩, **b** ⟨111⟩, **c** ⟨112⟩ and **d** ⟨100⟩ direction is equal to hybrid-TASE devices in Fig. 5.4. Copyright 2021 American Chemical Society [142].

templates on the same chips as hybrid-TASE templates, thereby ruling out parameter variations between epitaxy runs as the origin of our observations. To pattern TASE cavities, we extended the area of TiN etching in Fig. 5.2c to remove TiN on the entire NW length.

Growth inside normal reference templates is presented in Fig. 5.7. The reference templates have similar aspect ratio and equal crystal orientation as hybrid templates shown in Fig. 5.4. While the uniformity of growth rates along ⟨110⟩, ⟨111⟩, ⟨112⟩ and ⟨100⟩ template directions was reproduced in normal templates, the axial NW growth rate was reduced by more than a factor of two compared to hybrid epitaxy. {110}, {111}B and {112} facets at the InAs growth front can be discerned in Fig. 5.7, viewed through the thin SiO_2 template layer. These results are consistent with faceting observed in previous studies on epitaxy in normal SiO_2 templates [90, 92]. The high growth uniformity and radial filling of the templates as well as the formation of prominent {111}B facets at As rich epitaxy has been attributed to enhanced growth of {110} facets and suppressed growth in ⟨111⟩ direction due to As trimer formation on the {111}B facet [101–103]. We note that this was particularly apparent in normal templates along the ⟨111⟩ and ⟨112⟩ direction (Fig. 5.7b and c), where we observe formation of single {111}B facets, indicating that {110} facets are grown out completely, despite the growth front is still deep inside the template.

Results presented in Figs. 5.4, 5.6, and 5.7 were obtained by growth in As rich atmosphere with V/III=150. Reducing the V/III precursor ratio to 70 and decreasing the TBAs and TMIn flows to 137 μmol/min and 1.9 μmol/min, respectively, allowed us

to study the dependence of the apparent growth rate enhancement inside hybrid-TASE templates as a function of crystal direction. Under these conditions, a growth time of 42 min was required to obtain devices presented in Fig. 5.8. Importantly, the effective V/III ratio inside the templates was further decreased as a consequence of the high aspect-ratio of our template geometry [93]. Hence, the new growth conditions resulted in an As sparse atmosphere. In Fig. 5.8 we compare epitaxy along the ⟨110⟩ and ⟨111⟩ direction inside normal and hybrid templates. When grown at low As flux, InAs does not cover exposed Si areas after nucleation [279, 280]. To prevent the size of the Si seed to impact our comparison between TASE and hybrid-TASE growth in Fig. 5.8, we etched cavities deep enough as to reach a constriction with lithographically defined cross section of 40 nm × 70 nm. The constriction smoothly expanded into a cavity with cross section 100 nm × 70 nm, as the InAs growth front progressed.
In Figure 5.8a we present InAs growth inside a normal template aligned along the ⟨110⟩ direction. In this geometry we consistently obtained short wires that did not extend beyond the seed constriction but exhibited distinct {110} facets. This behavior is consistent with growth at low V/III ratio, where growth of the {111}B facet far exceeded that of the {110} facet. For growth inside normal ⟨111⟩ aligned templates (Fig. 5.8b) this behavior was further emphasized as growth of the {111}B facet was not limited by the template side walls. This resulted in a 770 nm long wire with a single {111}B growth facet. Growth of the six {110} NW side facets was suppressed completely and the NW diameter was effectively determined by the Si seed cross section and not by the template. The suppression of {110} side facet growth corroborates the lack of group-V precursor molecules [99, 100], since they access the template predominantly via Knudsen diffusion [93, 97] and are then incorporated at the {111}B facet.

The situation changed when a TiN surface was present in the cavity. In the ⟨110⟩ aligned hybrid template (Fig. 5.8c) the InAs crystal extended into the wide cavity region and radially expanded to the template walls. The increase in both radial and axial growth rate points towards a faster growth of {110} facets compared to the reference growth in SiO_2 templates. While the wire exhibited a {110} facet as in the reference example, there was a second, most likely {111}B facet, that is not grown out entirely, indicating a more balanced growth between {110} and {111}B facets. Again, our findings are confirmed by epitaxy in ⟨111⟩ direction (Fig. 5.8d) where a single {111}B facet formed, similar to the reference (Fig. 5.8b). However, the cavity was radially filled similar to growth in ⟨110⟩ direction (Fig. 5.8c), confirming faster growth of {110} facets when a TiN surface was present. The NW in Fig. 5.8d was 260 nm shorter than the reference, since the higher growth rate of {110} facets caused a competition between {110} and {111}B facets for precursor material. We emphasize that such a decrease in axial growth rate was observed only in this specific situation, that is at reduced precursor flow in ⟨111⟩ oriented templates. In all other growth regimes investigated in this work, accelerated growth in ⟨110⟩ direction resulted in longer wires.
While growth in normal templates with the conditions of Fig. 5.8 always resulted in the growth morphology presented in Fig. 5.8a and b, we observed a higher variability in faceting for the hybrid case. Two further examples are presented in Fig. 5.8e and f where

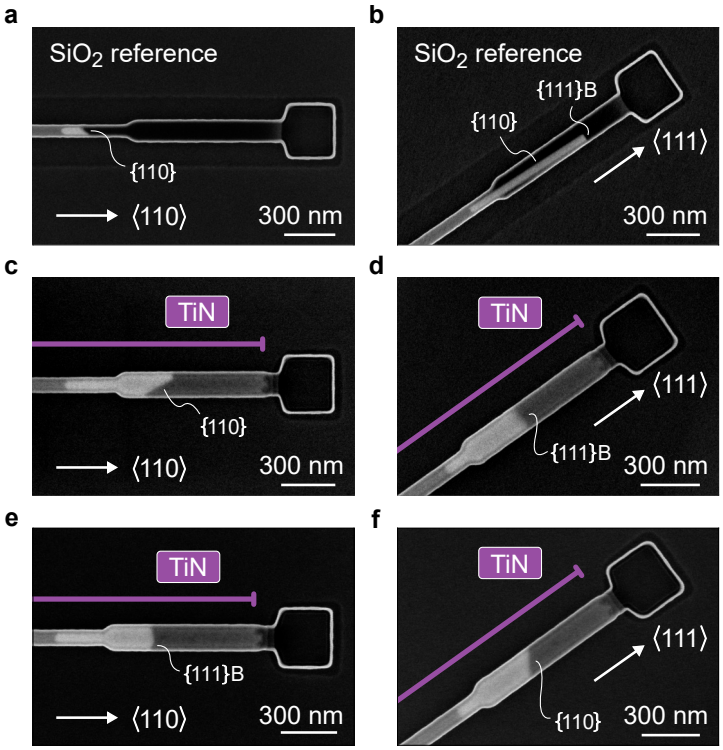

Figure 5.8. Comparison of TASE and hybrid-TASE InAs epitaxy at low As flow. InAs epitaxy with reduced precursor flow and V/III=70 inside TASE templates aligned along the **a** ⟨110⟩ and **b** ⟨111⟩ direction and inside hybrid-TASE templates along the **c, e** ⟨110⟩ and **d, f** ⟨111⟩ direction, respectively. Purple lines indicate the extent of TiN stripes integrated into hybrid templates. Copyright 2021 American Chemical Society [142].

we observe at least one {111}B facet in a ⟨110⟩ hybrid template and a single {110} facet in a ⟨111⟩ hybrid template. A wide range of possible facet morphologies has previously been observed for GaAs and InAs epitaxy in TASE templates [90, 92]. The variability in morphology between individual wires has been ascribed to microscopic details of the Si seed morphology and nucleation on it. Consequently, the multitude of facet configurations in hybrid-TASE growth of Fig. 5.8c-f points towards a more balanced growth equilibrium compared to epitaxy in reference templates of Fig. 5.8a and b. In the latter case, the InAs facet morphology was entirely dominated by the As supply limited growth conditions.

Increased semiconductor growth rates have previously been reported in literature in the context of vapor-liquid-solid (VLS) NW growth and selective area growth (SAG) using a metal mask. Catalytic decomposition of group-III precursors molecules on the Au droplet surface caused a faster growth of GaP, GaAs and InAs VLS NWs [281] while fast lateral growth in SAG was attributed to enhanced surface diffusion of group-III precursors on a W mask surface [282, 283]. Growth selectivity in the latter process was

found to significantly decrease for low growth temperature and rough metal surfaces [272, 284]. We stress that in our work the smooth back face of an integrated TiN layer was exposed, the roughness of which was set by the native SiO_2 layer below (see Fig. 5.4). We speculate that the smooth TiN surface morphology leads to a more homogeneous surface energy that was less dominated by anisotropic surface energies of grain facets [285], enabling selectivity during hybrid-TASE epitaxy.

To summarize, fast epitaxy in hybrid-TASE templates could be the result of enhanced precursor surface diffusion on the integrated TiN segment. The change in facet morphology from TASE reference epitaxy to hybrid-TASE epitaxy (Fig. 5.8) indicated an increased effective V/III material ratio at the growth front. The increase in {110} facet growth rate leads us to the conclusion that the origin of the V/III ratio increase is a locally enhanced As vapor pressure rather than a reduced In pressure inside template cavities. We are not aware of previous work where an increased efficiency of group-V precursor incorporation by means of a metal surface was reported. Future work will include a detailed study of growth dynamics in the presence of metal surfaces.

5.2.3. EDX Analysis of Hybrid-TASE Interfaces

The characteristics of the hybrid TiN/InAs interface and the Si/InAs seed interface were discussed in sections 5.1.4 and 5.1.5. Figures 5.9a and b show EDX lines profiles of the interfaces presented in Figs. 5.3e and 5.4a, respectively.

5.2.4. Seed Morphology

We obtained the lateral ADF-STEM images of a hybrid-TASE NW presented in Fig. 5.3d and Fig. 5.4a by cutting a lamella parallel to the ⟨110⟩ nanowire axis. This scenario is sketched in the schematic top view of Fig. 5.10a. To highlight the V-shaped seed morphology, the figure only shows the Si seed (green) and the InAs nanowire (red) and we omit a layer of native SiO_2 on top of the seed and a stripe of TiN covering both the seed and the InAs NW. In Fig. 5.10b we show a schematic representation of the ⟨100⟩ zone axis view of the lamella, similar to the ADF-STEM image shown in Fig. 5.3d. The {111} facet planes of the Si seed are inclined by an angle of 54.7 ° with respect to the nanowire axis. Consequently, the zone axis of the high resolution ADF-STEM image of the seed in Fig. 5.4a is not perpendicular to the Si/InAs interface. This has two important consequences: First, the imaged Si/InAs interface does not show an abrupt transition from Si to InAs. This is a consequence of the geometrical projection of the inclined interface on the viewing plane. Secondly, the layer of native SiO_2 is only present at the Si/TiN interface but appears to extend towards the InAs/TiN interface. This observation can be understood as a consequence of the complex seed morphology as well. We highlight the location of the native SiO_2 layer in the exploded-view drawing of Fig. 5.10c. In Fig. 5.10d we present an ADF-STEM image recorded in the region highlighted by the orange box in Fig. 5.10b. Both geometrical projection effects discussed above can be recognized in this image: the Si/InAs interface appears smeared out and

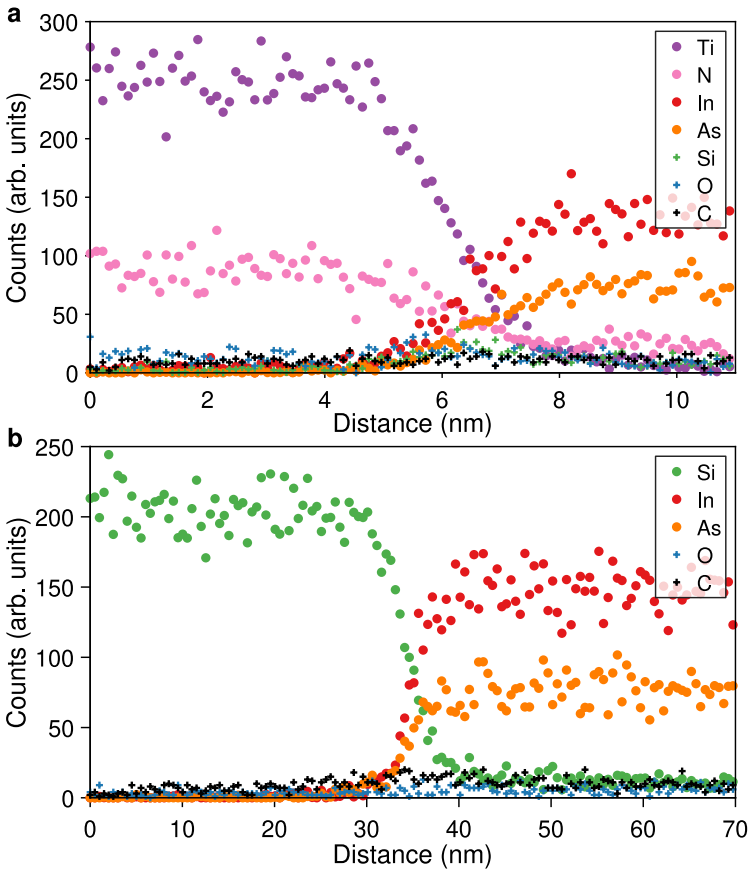

Figure 5.9. EDX elemental line profiles. **a** EDX line scan of the hybrid TiN/InAs interface of Fig. 5.3e. **b** EDX line scan of the Si/InAs seed interface of Fig. 5.4a. Copyright 2021 American Chemical Society [142].

the native SiO_2 layer appears to extend to the hybrid interface only in the region where inclined Si {111} facets are present.

5.2.5. Crystallinity of a Hybrid-TASE Nanowire

In Fig. 5.4 we present Fast Fourier Transforms (FFTs) of the Si/InAs seed interface region. We conclude that InAs grew epitaxially from the Si seed. In Fig. 5.11 we present further FFTs recorded at different positions along the InAs nanowire axis. The data show that the InAs nanowire is a single crystal since the epitaxial relation is maintained throughout the nanowire.

5.2.6. Electrical Tuning via a Back-Gate

At a temperature $T = 14$ K, TiN in the device of Fig. 5.5a was resistive and we operated the metallized silicon handle wafer as a back-gate. A representative pinch-off curve is

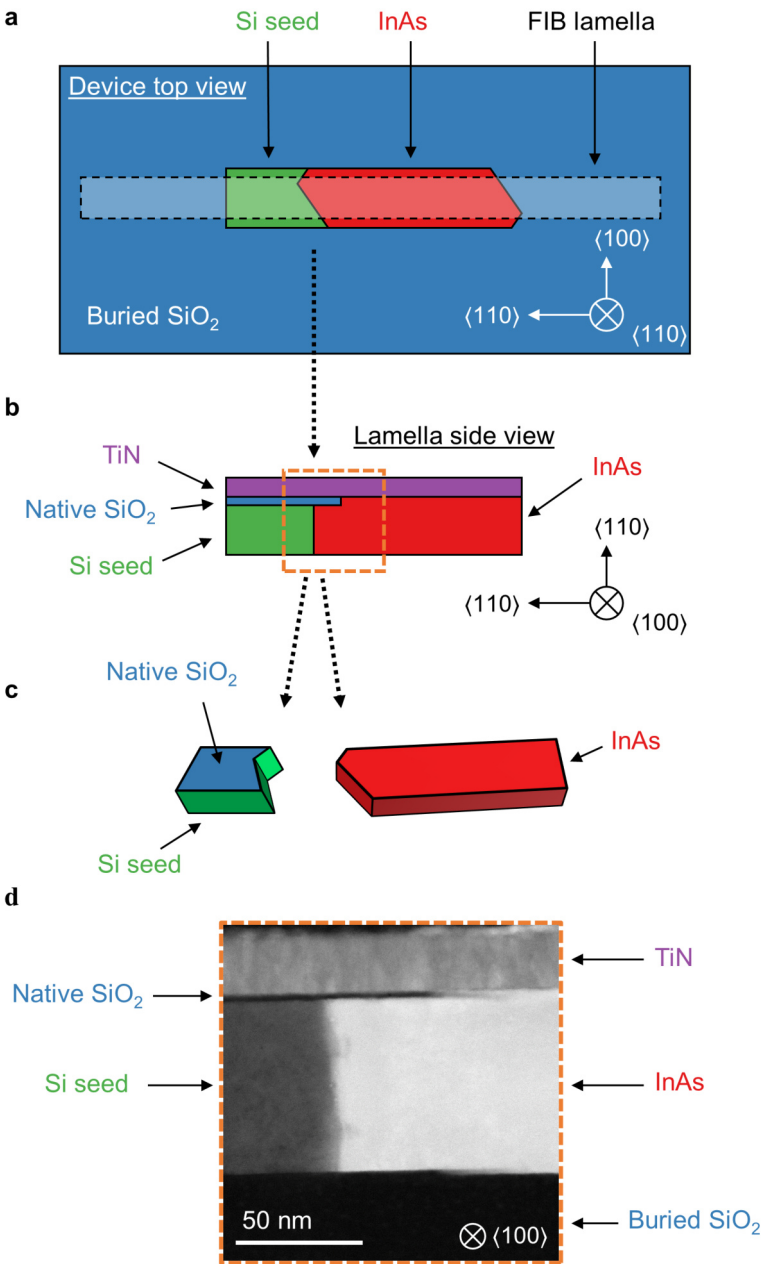

Figure 5.10. Morphology of the Si seed. **a** Schematic top view of a InAs NW (red) grown along the ⟨110⟩ direction. Native SiO_2 and TiN are omitted for clarity. The FIB lamella orientation of Fig. 5.3d is indicated. **b** Schematic representation of the ADF-STEM image presented in Fig. 5.3d. A thin layer of native SiO_2 (blue) is present between the Si seed layer (green) and the TiN layer (purple). **c** Exploded-view drawing of the Si/InAs seed interface. The thin native SiO_2 layer covers the V-shaped Si seed. **d** ADF-STEM overview image of the seed region indicated by the orange square in **b**. Copyright 2021 American Chemical Society [142].

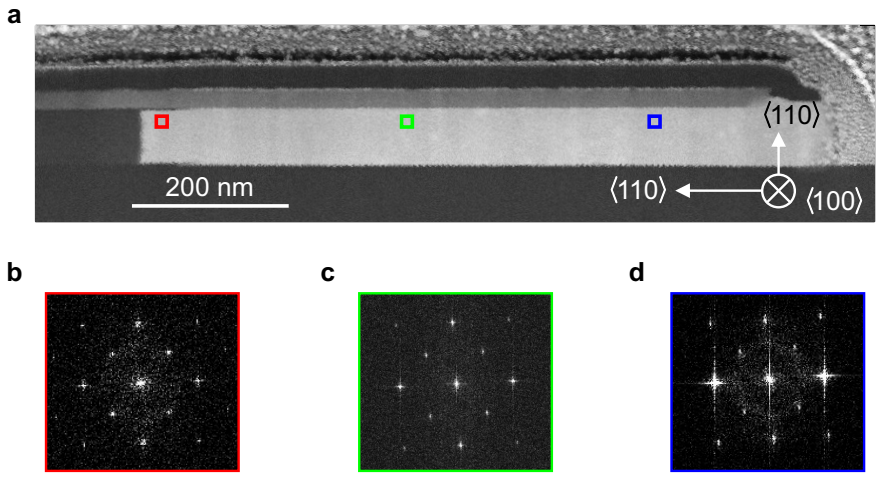

Figure 5.11. Single-crystallinity of a hybrid-TASE nanowire. **a** Overview of a hybrid-TASE InAs crystal cut along the nanowire axis and imaged along the ⟨100⟩ zone axis. Image is the same as Fig. 5.3d. Colored squares indicate regions where FFTs of **b**, **c** and **d** were extracted. **b** FFT of the InAs crystal close to the seed interface. Image is the same as Fig. 5.4d. **c** FFT of the InAs crystal in the center region of the nanowire. **d** FFT of the InAs crystal close to the template opening. Copyright 2021 American Chemical Society [142].

presented in Fig. 5.12. Oscillations in the conductance trace were reproduced throughout several sweeps of the back-gate voltage V_{BG}, consistent with conductance fluctuations in the wire. Measurements in Fig. 5.5 were performed at $V_{\mathrm{BG}} = -15$ V, indicated by the dashed line in Fig. 5.12.

5.2.7. Titanium Nitride Superconducting Gap

We investigated the impact of template fabrication on the superconducting properties of TiN. For this purpose, we characterized TiN NWs after exposure to different steps of the hybrid-TASE fabrication scheme. The NWs were dry etched from a 20 nm thick layer of TiN, they were 80 nm wide and 2 μm long. The patterning was performed in analogy to the TiN dry etching presented in the hybrid-TASE process flow (see section 5.1.9). In Fig. 5.13 we present the critical current I_{C} of a typical NW as a function of temperature T. The NW was not exposed to further fabrication and we use it as a reference in the following comparison. We fit I_{C} with Bardeen's formula [229]:

$$I_{\mathrm{C}}(T) = I_{\mathrm{C0}}\left(1 - \frac{T^2}{T_{\mathrm{C}}^2}\right)^{\frac{3}{2}} \tag{5.1}$$

where I_{C0} is the critical current at $T = 0$ and T_{C} is the critical temperature. Both quantities are fit parameters and we obtain $I_{\mathrm{C0}} = 46$ μA and $T_{\mathrm{C}} = 3.5$ K which corresponds to a superconducting gap $\Delta(T = 0) = 1.76 k_{\mathrm{B}} T_{\mathrm{C}} = 531$ μeV, consistent with Ref. [192]. In chapter 4 we presented an extensive study on etched TiN NW devices and obtained

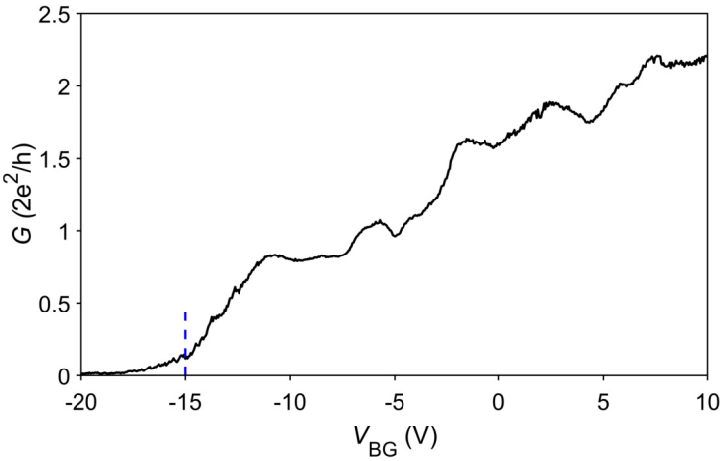

Figure 5.12. Back-gate tuning of a hybrid-TASE device. Tuning of a hybrid-TASE nanowire using the Si back-gate at $T = 14$ K. The blue dashed line ($V_{BG} = -15$ V) indicates the operating point of measurements in Fig. 5.5. Copyright 2021 American Chemical Society [142].

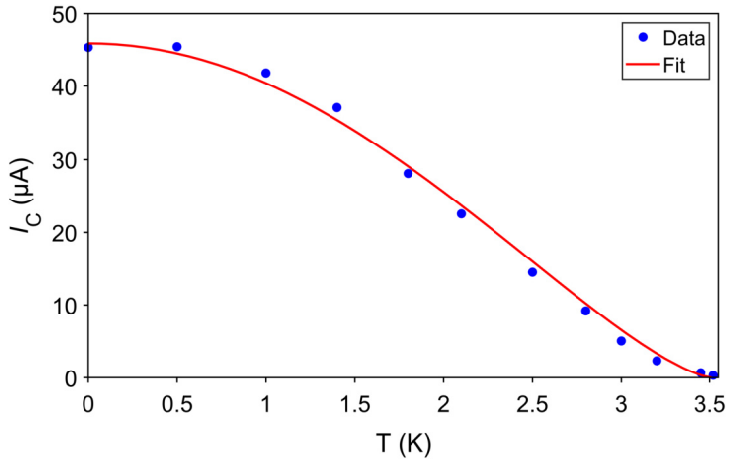

Figure 5.13. TiN nanowire critical current. Critical current of a patterned TiN NW on a Si substrate as a function of temperature. Bardeen's formula was used to fit the data. Copyright 2021 American Chemical Society [142].

similar values of T_C for more than 20 devices, irrespective of the NW width or length. This confirms that the extracted value of T_C is representative of the TiN quality prior to any further template fabrication. We list the superconducting properties as Stage 1 in Tab. 5.1.

Next, we investigated NWs that were encapsulated in a 40 nm SiO_2 template using the same plasma-enhanced ALD process as for hyrbid-TASE devices (see section 5.1.9). For these devices, we measured a critical temperature of 3.3 K (Stage 2a in Tab. 5.1).

Table 5.1. Comparison of TiN NWs at different fabrication stages. TiN NWs were exposed to different stages of the hybrid-TASE process flow and the critical temperature was measured after each step. **Stage 1** TiN NWs were patterned on a Si substrate. **Stage 2a** TiN NWs were encapsulated in a SiO_2 template. **Stage 3a** NWs encapsulated in SiO_2 were annealed at 600 °C for 30 s. **Stage 3b** NWs encapsulated in a SiN_x template were annealed at 600 °C for 30 min.

Fabrication stage	T_C (K)	Δ (μeV)
Stage 1 NW patterned	3.5	531
Stage 2a, **SiO_2** NW encapsulated	3.3	500
Stage 3a, **SiO_2** NW annealed for 30 s	2.8	425
Stage 3b, **SiN_x** NW encapsulated and annealed for 30 min	3.7	561

At Stage 3a we annealed wires encapsulated in SiO_2 for 30 s at 600 °C in Ar/H_2 atmosphere, similar to the annealing process we performed during template fabrication of hybrid-TASE devices (see section 5.1.9). After this short annealing step, wires showed a significantly reduced T_C of 2.8 K. We attribute the degradation to the partial oxidation of TiN in the presence of SiO_2 at the annealing temperature. Note that in this experiment devices were annealed only for a short time of 30 s. During InAs epitaxy, devices are exposed to similar temperatures for much longer times of approximately 30 min. Therefore, it is reasonable to assume that the superconductor will degrade even further during InAs epitaxy.

To investigate the influence of template material on TiN degradation we encapsulated TiN NWs in a SiN_x template using plasma-enhanced ALD and annealed the devices at 600 °C for 30 min (Stage 3b in Tab. 5.1). Note that this annealing time and temperature were representative of the conditions during InAs epitaxy in hybrid-TASE templates. Despite the long annealing time, T_C of these devices did not decrease compared to the reference devices. This finding corroborates our interpretation that the presence of a SiO_2 template during high-temperature processing is the main source of TiN degradation in our process flow. We envision that future devices will employ SiN_x as the template material to preserve the superconducting properties of integrated nitride superconductors.

5.3. Additional Results

This section contains additional results that are not published in [142]. In particular, we discuss the electronic properties of the hybrid interface in further detail (section 5.3.1), review challenges that needed to be overcome to enable hybrid-TASE fabrication (section 5.3.2), review epitaxy inside advanced template geometries (section 5.3.3), and discuss current limitations of the method (section 5.3.4). Finally, we suggest improvements that could expand the quality and flexibility of hybrid-TASE for future applications (section 5.4).

5.3.1. Induced Superconducting Gap

We turn our attention back to the measurement of Fig. 5.5b and expand our discussion on the hybrid InAs/TiN interface. In section 2.4 we reviewed BTK theory as a means to describe Andreev reflection at normal metal/superconductor (NS) interfaces. This approach was expanded by Beenakker [276] to the case of a quantum point contact (QPC) proximal to an NS interface. In the single channel limit and assuming perfect Andreev reflection at the interface, the conductance of the junction reads [276]

$$G_{\mathrm{S}} = \frac{4e^2}{h} \cdot \frac{\mathcal{T}^2}{(2-\mathcal{T})^2} = 2G_0 \cdot \frac{G_{\mathrm{N}}^2}{(2G_0 - G_{\mathrm{N}})^2} \tag{5.2}$$

where $\mathcal{T}$ is the channel transmission and $G_{\mathrm{N}} = \mathcal{T} G_0$ is the conductance of a normal QPC. In Fig. 5.14 we compare the theoretical predictions of G_{S} and G_{N} to the experimental data of Fig. 5.5b. Since data was measured using a quasi-four terminal configuration (see device geometry in Fig. 5.5a) which precludes line resistance but not contact resistance, we subtracted a contact resistance of 2.8 kΩ from the measured resistance, to move the first conductance plateau in Fig. 5.12 to $2e^2/h$. In analogy to previous works on Al/InAs NWs and 2DEGs [263, 266], we identify G_{S} as the zero-bias conductance $G\,(V_{\mathrm{SD}} = 0)$ and assume for the normal state conductance $G_{\mathrm{N}} = \bar{G}\,(V_{\mathrm{SD}} = \pm 760\ \mu V)$, i.e. we calculate the average of conductance at the highest and lowest bias (see Fig. 5.5c to e).[6]

In the high conductance regime ($G_{\mathrm{N}}/G_0 = \mathcal{T} \geq 0.5$ in Fig. 5.14) the experimental data follow the predicted behavior of G_{S}. The in-gap conductance G_{S} exceeds G_{N} above a transmission $\mathcal{T}' = 0.83$, similar to the theoretically predicted value of $\mathcal{T}' = 0.76$ in the case of perfect Andreev reflection at the NS interface [276] and similar to experimental findings of $\mathcal{T}'$ ranging from 0.7 to 0.8 in hybrid 2DEGs [46]. To quantify the probability of Andreev reflection at the NS interface, superconductor/normal metal/superconductor (SNS) devices need to be investigated [286, 287]. We discuss the challenges associated with SNS device fabrication in hybrid-TASE in sections 5.3.3 and 5.3.4.
Despite the conductance increase of the hybrid-TASE QPC at high channel transmission,

[6] While this approximation is consistent with a measurement at $B > B_{\mathrm{c}}$, yielding $G\,(V_{\mathrm{g2}} = -1.2\ \mathrm{V}) = 0.85\ G_0$, we stress the uncertainty related to G_{N} when using the above method. In particular, the conductance in Fig. 5.5c is not saturated at high bias and in the case of Fig. 5.5d, the values at positive and negative bias differ significantly. In a more systematic study, G_{N} could be recorded in an independent measurement, e.g. at $T > T_{\mathrm{C}}$.

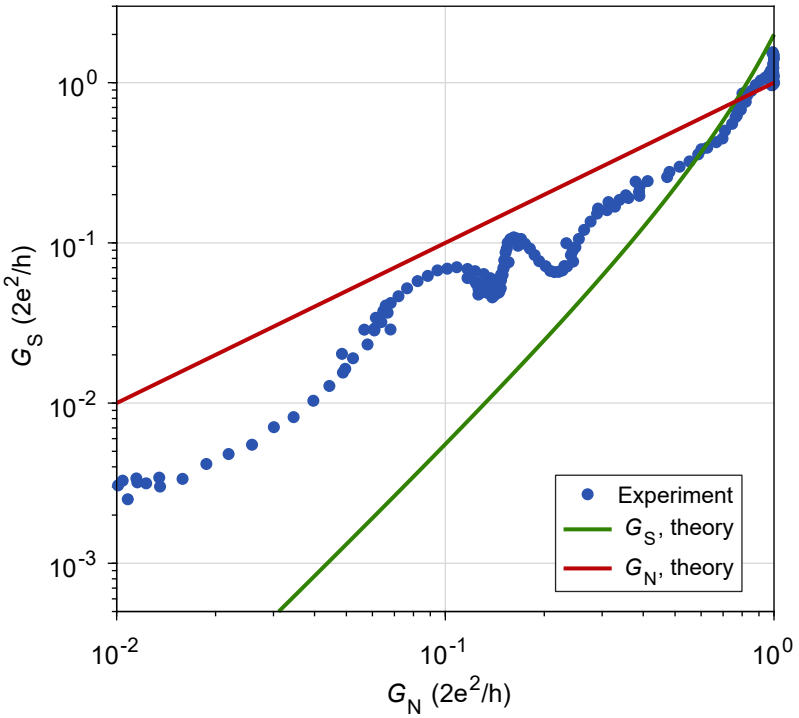

Figure 5.14. Comparison between hybrid-TASE QPC and ideal NS QPC. Experimental in gap conductance of a hybrid-TASE QPC as a function of high bias conductance (see text for details), as well as theoretical predictions of the in gap conductance G_S of an ideal NS QPC, and conductance G_N of a normal QPC.

$G\,(V_{SD} = 0)$ starts to deviate significantly from the ideal case below $G_N = 0.5G_0$ in Fig. 5.14. This finding is consistent with the finite in-gap conductance in tunneling spectroscopy data (Fig. 5.5e) and we will comment on it below.

In Fig. 5.15 we investigated the behavior of the induced superconducting gap as a function of the magnetic field B_z applied parallel to the NW axis of the device in Fig. 5.5. Data in Fig. 5.15 was recorded with the gates set to $V_{BG} = -15$ V, $V_{g1} = -2.6$ V, and $V_{g2} = -5.4$ V. At $B_z = 0$ T we extract $\Delta^* = 180$ μeV (Fig. 5.15b), similar to data in Fig. 5.5e. The gap appears to close at $B_z \approx 0.5$ T, at $B_z = 1$ T a peak in conductance is observed at zero bias (Fig. 5.15c). In similar NW systems such features have been associated with Kondo signatures [288], Andreev states [77, 259, 289, 290], or an interplay of the two [291, 292].

While a soft gap behavior as in Fig. 5.5e and Fig. 5.15 has previously been attributed to disorder at the NS interface [293], a recent experimental study [270] demonstrated a hard superconducting gap in InSb nanowires with polycrystalline Sn shell, implying that a long range, lattice matched epitaxial hybrid interface might not be required. We further point out that a deviation from the ideal model of G_S is not necessarily linked to the NS interface transparency, instead, other factors can contribute to a finite in-gap

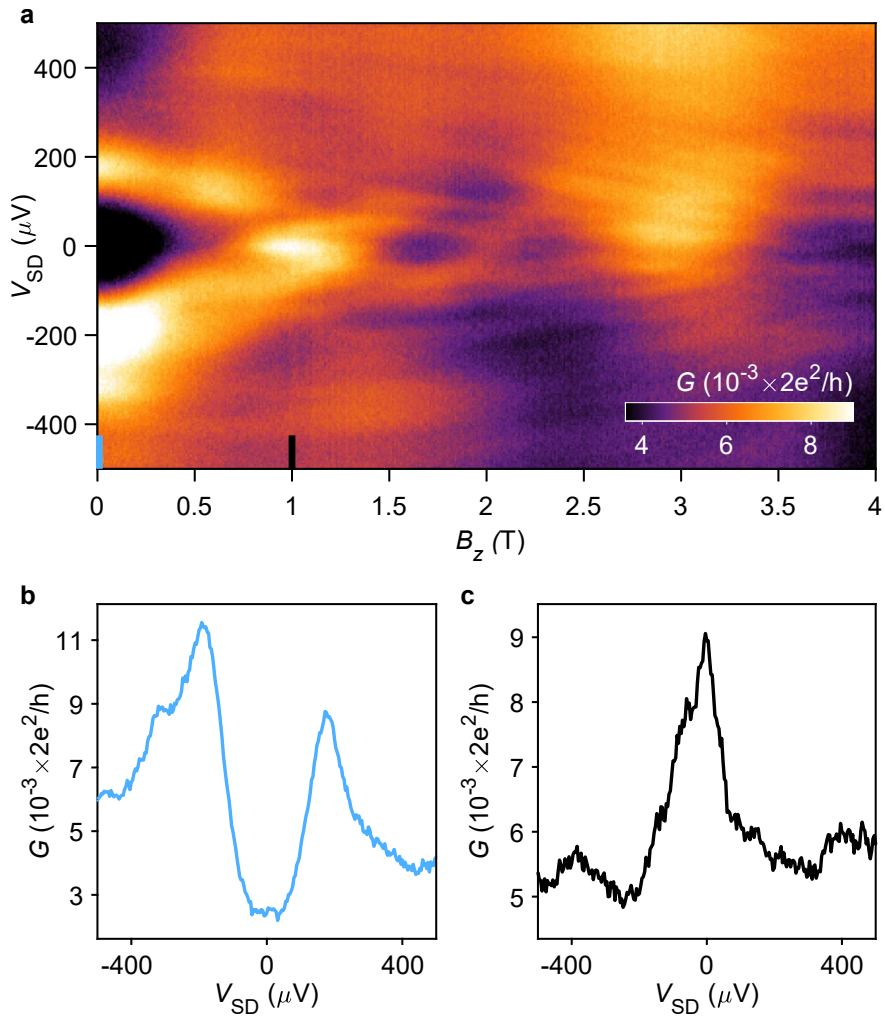

Figure 5.15. Tunneling spectroscopy of a hybrid-TASE device in magnetic field. a B_z is applied parallel to the wire axis, gates are set to $V_{BG} = -15$ V, $V_{g1} = -2.6$ V, and $V_{g2} = -5.4$ V (device in Fig. 5.5a). **b** Line cut at $B_z = 0$ T. **c** Line cut at $B_z = 1$ T.

conductance. For example, the observation of quasiparticle states in the superconducting gap of Nb was previously assigned to oxidation of the superconductor [294], resulting in quasiparticle poisoning of superconducting Nb islands. A similar effect might occur in our structures, since we find TiN to degrade significantly in hybrid-TASE fabrication (see section 5.2.7). Moreover, the interaction of TiN with the template and in particular diffusion of excess Ti atoms into SiO_2 [295, 296] and formation of Ti silicide [297] during high temperature fabrication could create parallel conduction paths which might contribute to a finite conductance when the InAs nanowire is pinched off. The conductance tail observed in the pinch-off trace of Fig. 5.12 at $V_{BG} < -15$ V indeed suggests the presence of such parallel paths. In experiments on early devices with integrated

TiN gates (see discussion of Fig. 5.16a), we found that TiN gates were shorted both to neighboring gates as well as to distant gates of other devices across the chip after high temperature processing.[7] This finding further corroborates our hypothesis of mobile Ti atoms diffusing in the template during fabrication, however, further experiments are required to quantify these effects. In particular, probing the TiN DOS via a tunnel junction and parity lifetime measurements on TiN islands [241] might provide valuable insights. The characterization of such devices could be performed after patterning of bare TiN elements and might then be repeated after encapsulation in either SiO_2 or SiN_x templates (see Tab. 5.1) to clarify the role of TiN degradation in the observed soft gap.
In summary, we point out that hybrid-TASE at its current state is not yet a suitable candidate for investigation of topological qubits, since sub-gap states would participate in braiding operations and break parity protection [298]. Further optimization of the hybrid-TASE process is required to achieve this goal. Alternative fabrication routes and experiments are outlined above and in section 5.4.

5.3.2. Hybrid-TASE Yield Optimization

A major challenge of this work consisted in achieving a sufficiently high nanowire epitaxy yield inside hybrid templates. The fabrication details of hybrid-TASE templates played a crucial role in achieving this goal. In chapter 5.1.3 we outlined the general idea of the process flow. Here, we shine light on the optimization steps that enabled successful InAs growth.
In a first generation of devices (Fig. 5.16), we used wafers with a 30 nm thick SOI layer with (001) orientation. The native SiO_2 layer on the SOI was etched in HF before a 20 nm thick layer of TiN was sputtered directly on the SOI. We were not able to achieve successful hybrid-TASE inside templates based on such wafers. After fabricating more than 100 chips and performing more than 60 epitaxy runs in a wide parameter space, we could rule out sample-to-sample variations as the origin of our observations. Instead, we identified the following key issues:

- **Unreliable Si backetch**
  In normal templates, the backetch length can easily be controlled via the etching time in TMAH solution. This was not the case in the first generation of hybrid-TASE templates. Instead, the etch rate was highly unreproducible and strongly varied between different template geometries. In particular, we observed that the etch rate drastically decreased when etching regions of Si located directly below TiN elements.

[7] TiN gates were etched from the same TiN layer and in the same processing step as TiN template elements. This approach made the gates self-aligned with respect to the template and allowed for high patterning resolution. The gates were encapsulated in SiO_2 during the template deposition and were exposed to high temperatures during template annealing and InAs growth (see section 5.1.9). Since all gates were shorted after fabrication, we resorted to a more conventional lift-off approach as seen in Fig. 5.5a.

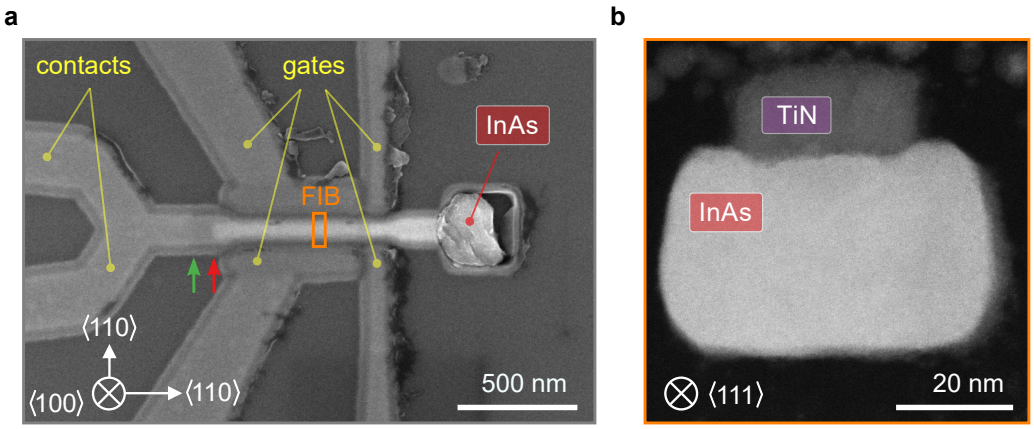

Figure 5.16. First generation hybrid-TASE nanowire. **a** Top view SEM micrograph of an early hybrid-TASE nanowire from the first generation. The device is based on a 30 nm thick (100) SOI layer. Note that nucleation of the InAs crystal (red arrow) does not occur on the Si seed surface (green arrow) but on the template surface. **b** STEM cross section of the nanowire at the location indicated in **a**. The nanowire axis points along a ⟨111⟩ direction, confirming that it is not epitaxially related to the seed. Note the smaller cross section of this device compared to the successful device based on a 70 nm thick SOI layer in Fig. 5.3a

- **Parasitic nucleation**
  The high aspect ratio of templates based on 30 nm thick SOI meant that InAs growth times typically exceeded 1 hour. The long growth time caused a high chance of parasitic nucleation on the SiO_2 chip surface. Parasitic crystals complicated subsequent fabrication steps, in particular lift-off processes for patterning contacts and gates.
  To mitigate the issue of parasitic nucleation on the SiO_2 substrate and the large overgrowth outside the templates (see next point), we manually polished the chips. This approach removed most of the parasitic crystals but was also difficult to control, as the nanowires were easily destroyed if the pressure applied during polishing was too high. Even in the case of successful polishing, large quantities of residual InAs and organic residues remained on the chip.

- **Nucleation and selectivity**
  Despite exploring a large parameter window of growth time, temperature and precursor ratio, we were not able to achieve selective epitaxy inside hybrid templates. Instead, InAs nucleated on the exposed TiN surface inside the template. Such nucleation preferentially occurred close to the cavity opening, causing the crystal to rapidly grow out of the template opening, thereby covering the entire device.

Figure 5.16a presents the most successful result we achieved with the first generation of hybrid-TASE templates.[8] The device exhibits most of the characteristic issues de-

[8] Growth conditions: $T = 550°C$, V/III=70, growth duration: 2500 s.

scribed above. Firstly, InAs did not nucleate on the Si seed (green arrow) but on the template surface close-by (red arrow). Secondly, the InAs crystal expanded outside of the template and had to be removed with mechanical polishing. This step contaminated the TiN side gates which were self-aligned and replaced by lift-off gates in later devices, as outlined above.
Figure 5.16b shows an ADF-STEM cross-sectional view of the nanowire in Fig. 5.16a at the indicated location. FFT analysis revealed that InAs is a single crystal across the entire cross section of the wire. However, the nanowire axis is aligned along $\langle 111 \rangle$, i.e. not along a $\langle 110 \rangle$ direction as would be expected from the orientation of the Si seed. This observation manifests the problem of random nucleation in hybrid-TASE templates of the first generation.

To enable InAs epitaxy inside hybrid-TASE templates we implemented the following changes, which resolved the issues outlined above.

- **Lower template aspect ratio and (110) SOI layer**
  We based the template fabrication on wafers with a thicker 70 nm SOI layer. This increased the cross-section of hybrid templates (see Fig. 5.3a) and enabled growth of ~ 1 μm long nanowires in 10 minutes. The shorter growth time meant that the size and number of parasitic crystals on the SiO_2 substrate was no longer a limiting factor for consecutive lift-off processes. Furthermore, the SOI layer in second generation devices had a (110) orientation. Thus, templates along high- and low-symmetry directions could be patterned alongside each other on a single chip, whereas low-symmetry directions were not accessible with in-plane templates based on (100) wafers. Epitaxy along high- and low-symmetry orientations was discussed in section 5.2.2 and allowed us to gain a deeper understanding of the growth dynamics inside hybrid templates.

- **Protection layer for TiN**
  The slow Si etch rate below TiN regions indicates an interaction between exposed TiN and the TMAH solution in devices of the first generation. To protect the TiN back face during Si etching, a 25 nm thick TiN layer was sputtered on the SOI layer without prior etching in HF. Consequently, an approximately 1.7 nm thin native SiO_2 layer separated the SOI crystal from the TiN film. Due to the extremely high Si/SiO_2 etch selectivity of $\sim 10^5$ [299, 300], this was sufficient to protect TiN structures during etching in TMAH. The consistent backetch achieved with this method is summarized in Fig. 5.17 where all templates show a backetch length of 730 nm, irrespective of the template width and geometry of TiN elements. The backetch consistency also meant that the InAs growth rate was similar in templates with similar diameter, crystal orientation, and TiN geometry. Consequently, the number of templates with large overgrowth was significantly lower. This, together with reduced parasitic growth on the SiO_2 mask allowed us to omit any mechanical polishing before fabrication of gates and normal contacts (see Fig. 3.3d).

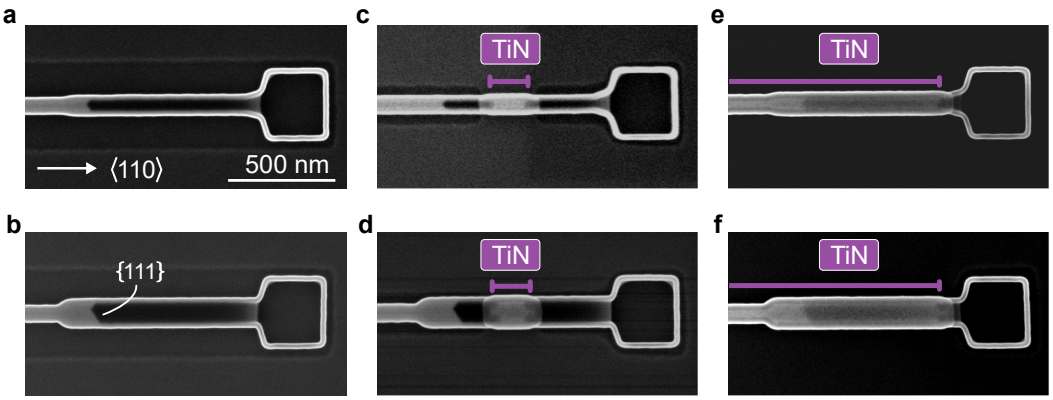

Figure 5.17. Consistent cavity etching in various geometries. Cavities etched for 15 min in 2 % TMAH at 80 °C on a chip from the second template generation which features a protective native SiO_2 layer below TiN elements. **a,b** SiO_2 reference templates with a lithographic width of 60 nm and 100 nm, respectively. **c,d** Templates with integrated islands of TiN. The lithographic widths are 40 nm and 100 nm, respectively. **e.f** Hybrid templates with a continuous stripe of TiN, similar to devices in Figs. 5.2 and 5.3. Lithographic widths are 60 nm and 100 nm, respectively. Crystallographic direction and scale bar indicated in **a** are the same for all subfigures. The extent of TiN template segments is indicated by purple lines.

- **Clean TiN surface**
  Protecting the TiN surface during Si etching had another crucial advantage: it allowed us to expose the TiN surface just before introducing the chip into the growth reactor, by etching the SiO_2 layer in diluted HF. Templates prepared in this way enabled selective epitaxy inside hybrid structures with InAs nucleation on the Si seed (Fig. 5.4a) and no parasitic nucleation on the template walls (Fig. 5.11). In the following, we comment on the epitaxy yield.

We analyzed large device arrays to approximate the yield of hybrid-TASE after implementing the above improvements. Figure 5.18a shows a representative subset of such an array with lithographic template widths ranging from 40 nm to 100 nm between device columns. Device yield is categorized into four classes. Devices in green successfully nucleated on the Si seed and radially filled the cavity. Failed devices with nucleation of InAs on the template walls are highlighted in red. Such devices exhibit a void between seed and InAs wire, which is easily discernible in SEM. Orange devices had successful nucleation, yet the InAs wire did not fully expand to the side walls.[9] Lastly, devices in blue showed successful nucleation and initial InAs growth, however, nucleation of a second InAs crystal on the template walls eventually prevented the first crystal from

[9] This issue is not related to the presence of a TiN surface in the template and can be solved by increasing the V/III precursor ratio, as discussed in sections 2.6.2 and 5.2.2.

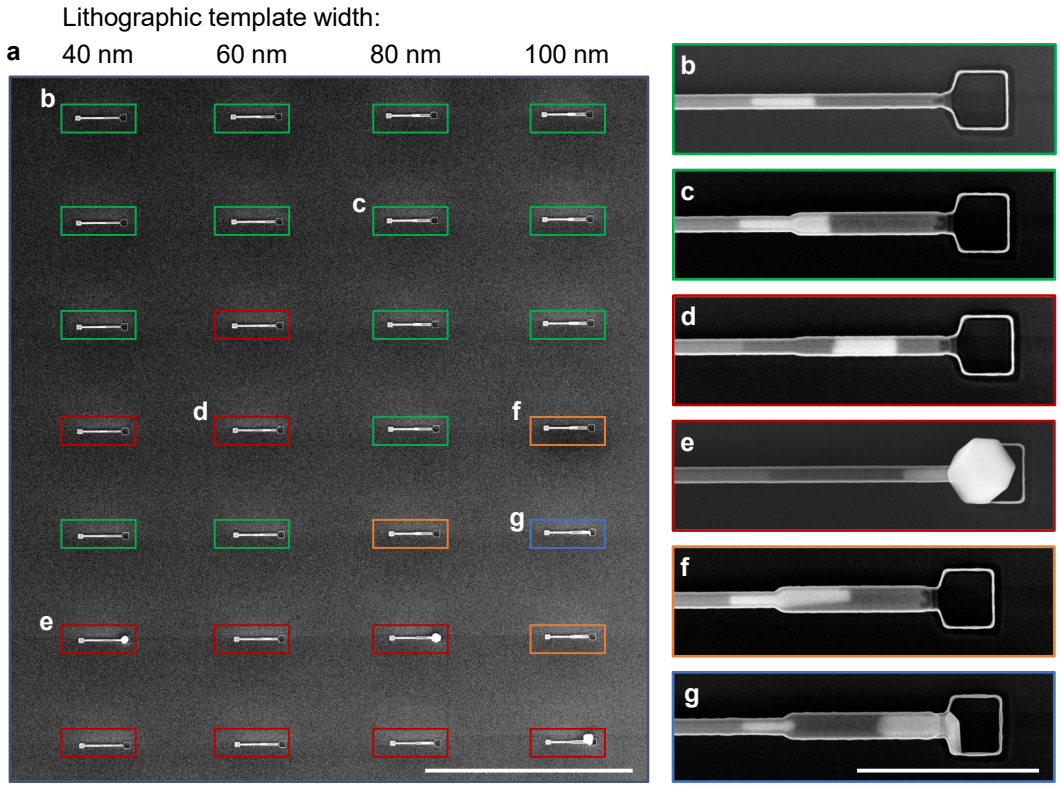

Figure 5.18. Hybrid-TASE epitaxy yield. a Array of hybrid-TASE devices after growth for 10 min at $T = 550°C$ and V/III = 70 with low precursor flow (same chip as in Fig. 5.8). The lithographic template width in each device column ranges from 40 nm to 100 nm. The scale bar is 10 μm. Devices highlighted in green show successful hybrid-TASE (detailed view in **b,c**). Red frames indicate devices with failed epitaxy due to nucleation on the TiN template surface (examples in **d,e**). Devices in orange nucleated successfully but wires did not radially expand to the template sidewalls (example in **f**). The device highlighted in blue successfully nucleated on the seed, yet a second crystal formed on the TiN template surface and prohibited successful growth (example in **g**). The scale bar in **g** is 1 μm and equal for all detailed-view panels.

growing further as it was cut off from precursor supply. Examples of these scenarios are presented in Fig. 5.18b-g. From analyzing template arrays with a total of 960 devices, we concluded that the yield of the hybrid-TASE process is approximately 50 %, where we defined the green and orange categories in Fig. 5.18a as successful growth.

It is important to acknowledge that this yield in hybrid templates is far from the near 100 % yield in normal SiO_2 TASE templates [90]. Normal reference templates which we fabricated alongside hybrid devices on every chip featured a similarly high yield as found in earlier studies [90], confirming that the lower yield in hybrid templates is indeed

correlated to the presence of TiN. Considering that systematic changes in the process flow increased the hybrid-TASE yield from 0 to 50 %, it seems reasonable to assume that future optimization can further improve the yield. A particularly important aspect of such optimization is to control the microscopic properties the TiN surface inside hybrid templates. The analysis and optimization of this surface is not an easy task, as its location on the template inside makes it inaccessible for standard characterization techniques such as top view SEM and AFM, both powerful tools for optimizing selective-area-growth masks. Furthermore, the microscopic properties of this surface do not only depend on the TiN deposition parameters, but also on the preparation of the SOI substrate. The complex surface geometry further rules out conventional surface energy measurements [301, 302], which could elucidate important precursor diffusion mechanisms on TiN surfaces (see sections 2.6.2 and 5.2.2). Considering the involved fabrication and technical challenges related to such analysis, investigating the impact of various TiN deposition and substrate preparation parameters was beyond the scope of this work. Detailed surface studies and use of other nitride superconductors in the future could aid the understanding of microscopic mechanisms in hybrid epitaxy.

5.3.3. Advanced Template Geometries

Devices discussed up to this point featured continuous stripes of TiN, either covering the entire nanowire (Fig. 5.2) or half of the nanowire without extending all the way to the template opening (Fig. 5.5). In Fig. 5.19a we present yet another geometry. It consists of a template which is not covered by a single TiN element, but rather by two separate stripes of TiN on either side, similar to the geometry of a lateral Josephson junction (JJ). We achieved this SNS geometry by modifying the TiN wet etch step (Fig. 5.2c) to remove the middle section of TiN parallel to the template axis. The template in Fig. 5.19 is aligned along a $\langle 111 \rangle$ direction and the Si seed has a single $\{111\}$ facet. The device shows an overgrown InAs crystal with well-defined facets at the entrance of the template. Lateral TiN arms can be operated as device contacts. Figure 5.19b shows an ADF-STEM cross section, recorded perpendicular to the device axis (see orange box in Fig. 5.19a), with clearly discernible lateral TiN contacts.

The device in Fig. 5.19a was grown with the same conditions as devices shown in Fig. 5.8, i.e. at low precursor flow and low V/III ratio of 70. In section 5.2.2 we established that such conditions heavily favor growth in $\langle 111 \rangle$ direction over growth of $\{110\}$ facets. Nevertheless, the InAs crystal in Fig. 5.19 expanded to a width of more than 300 nm, making it another striking example of the drastically changed growth dynamics inside lateral templates when TiN surfaces are present. We note that the differences in growth rate of $\{110\}$ facets between the devices in Fig. 5.19a and Fig. 5.8b are not explained by the differences in template aspect ratio or seed size. Normal reference devices with similar templates as in Fig. 5.19a showed equally suppressed growth of $\{110\}$ facets as in Fig 5.8b.

On the left-hand side of Fig. 5.19b we observe a distinct $\{110\}$ facet that did not fully expand to the template side wall. As discussed in chapter 5.2.2, the growth rate of this facet is further increased at higher V/III precursor ratio. Figure 5.19c details the

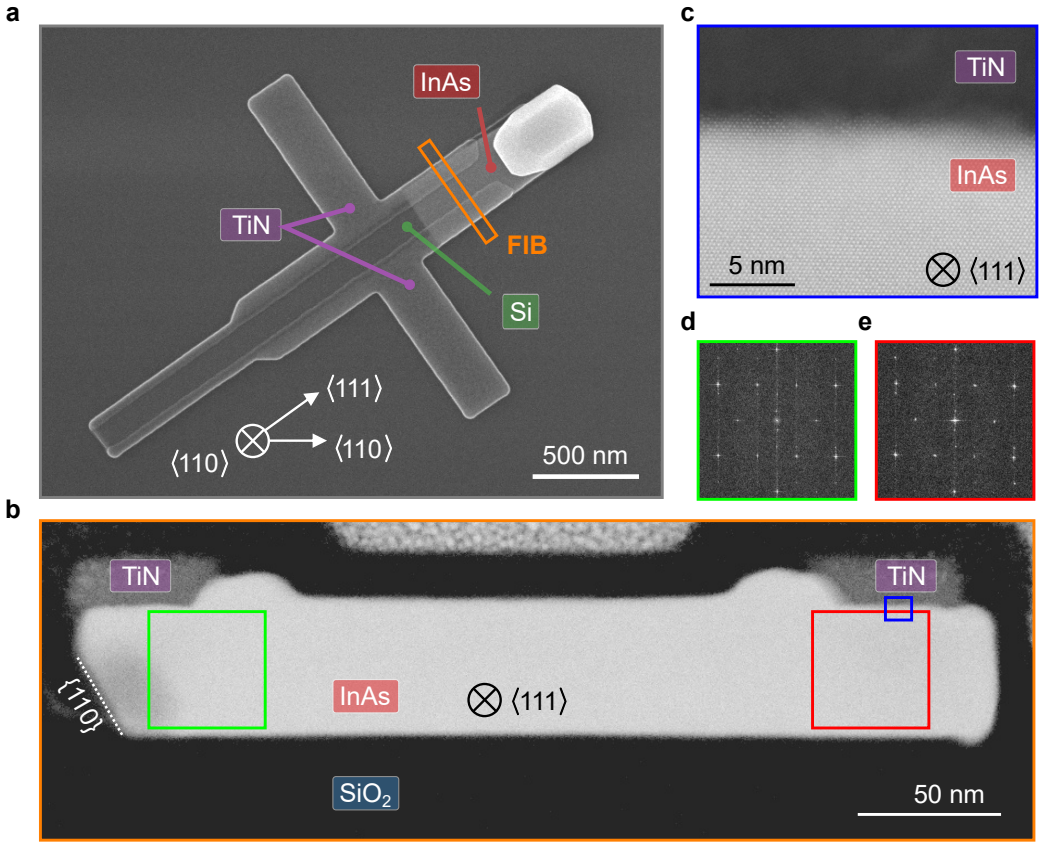

Figure 5.19. Hybrid-TASE with lateral SNS geometry. a Top view SEM micrograph of a hybrid-TASE device grown inside a ⟨111⟩ aligned template with single {111} Si seed facet. Lateral TiN arms serve as contacts to the InAs crystal. **b** Cross-sectional ADF-STEM image of the indicated region in **a** (orange box). The InAs crystal is 320 nm wide and aligned along a ⟨111⟩ direction. Further details are discussed in the text. **c** Representative ADF-STEM image of the hybrid TiN/InAs interface at the indicated location in **b** (blue box). **d,e** FFTs of the InAs crystal extracted from regions below the TiN elements (green and red box in **b**).

TiN/InAs hybrid interface. We observe a similar interface roughness as in the device of Fig. 5.3e. FFTs of Fig. 5.19d and e were extracted from the locations indicated in Fig. 5.19b. They confirm the single crystalline nature of the InAs channel and its alignment along the ⟨111⟩ zone axis, manifesting that InAs nucleated on the {111} Si seed.

We performed electrical characterization of similar lateral SNS devices. Figure 5.20a shows a typical device, together with the schematic measurement configuration. The device is aligned along the ⟨110⟩ direction and lateral TiN contacts branch out (outside of the image frame) to form four-terminal contacts. Measurements were performed using

standard low-frequency lock-in techniques, sourcing a current $I_{AC} = 10$ nA and measuring the differential voltage V. The device resistance at $T = 20$ mK as a function of perpendicular magnetic field $B_\perp$ is plotted in Fig. 5.20b. The device resistance dropped to $R \approx 70\ \Omega$ around zero field, but a zero-resistance state was not observed.
The resistance increase at $B_\perp = \pm 10$ mT in Fig. 5.20b might correspond to the critical field of the TiN leads. This would again point towards significant degradation of the superconductor, since the TiN nanowires described in chapter 4 had a critical field $B_\perp^C > 2$ T (see Fig. 4.2b). Moreover, a device similar to the one in Fig. 5.20a exhibited a 2-terminal resistance of $\sim 100\ \text{k}\Omega$, which is likely dominated by a large contact resistance between TiN contacts and evaporated Ti/Au bonding pads. In superconducting nanowire devices with similar fabrication of Ti/Au contacts (Fig. 3.1b), this resistance was negligible. Such high contact resistance corroborates the assumption that TiN degraded during high temperature processing.
The junction resistance at zero-field decreased during cooldown of the device and saturated at $R \approx 70\ \Omega$ (Fig. 5.20b), corresponding to a normal state resistivity of 350 Ω per square. Similar metallic behavior was recently identified as the intermediate regime between superconducting and insulating phase in JJ arrays based on hybrid 2DEGs [303]. There, tuning between the regimes was possible via a top gate voltage. Similar experiments could not be conducted in the present case, since devices did not feature gates in the first round of experiments and were destroyed (presumably during unbonding) by electrostatic discharge before gates could be fabricated. In the future, such experiments will be crucial to better understand the electrical properties and potential limitations of the hybrid-TASE method. We further stress that four-terminal experiments presented here could only be performed on one device, thus more statistics are required to judge if the observed behavior is representative.

5.3.4. Limitations of the Hybrid-TASE Approach

In the previous chapters we demonstrated that hybrid-TASE, i.e. selective III-V growth from a Si seed in the presence of a superconductor surface, is feasible, albeit with a lower yield than in normal TASE (see chapter 5.3.2). In our efforts to optimize template fabrication and semiconductor epitaxy, we steadily increased the yield of such devices and it is, therefore, reasonable to assume that further improvements can be made. Nevertheless, we identified specific template geometries inside which hybrid-TASE systematically failed, despite the template optimizations outlined in section 5.3.2 and irrespective of template aspect ratio or growth conditions. Figure 5.21 summarizes our findings, where devices in the same row belong to the same chip and growth run. Devices in Fig. 5.21a to d feature an SNS geometry, where a segment in the center of the TiN stripe was etched out during the wet etching step shown in Fig. 5.2c. The opposite is true for devices in Fig. 5.21e to h, which feature an island of TiN in the center of the template (NSN geometry). Green arrows in Fig. 5.21 indicate the Si seed location, red arrows highlight (parasitic) InAs nucleation sites.

While few devices (Fig. 5.21c, d and h) show InAs nucleation deep inside the template or on the seed surface, epitaxy failed in all devices because a rapidly expanding InAs

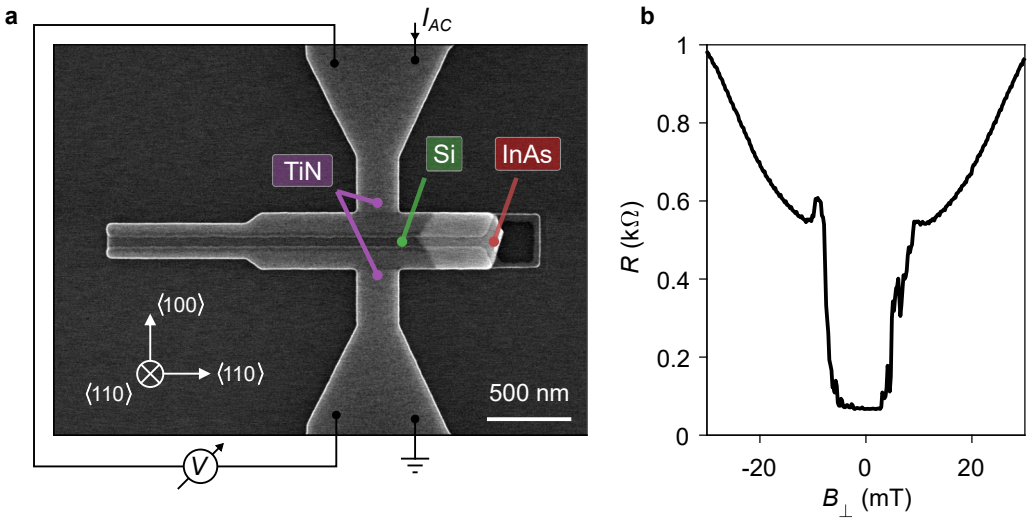

Figure 5.20. Hybrid-TASE SNS device. a SEM micrograph of a device with InAs grown along ⟨110⟩ and contacted by two TiN electrodes, which branch out into four contact pads outside the image frame. The measurement configuration is schematically indicated. **b** Resistance of the device in **a** as a function of perpendicular magnetic field $B_\perp$.

crystal formed on the TiN surface. Remarkably, the position of this nucleation site was consistent across devices of the same growth run and always occurred below the first TiN element in SNS junctions and below the TiN island in NSN junctions, regardless of growth conditions. Thus, our findings indicate that such parasitic nucleation is not random but correlated to the arrangement of TiN elements in these devices. In contrast to successful hybrid-TASE geometries, TiN segments in SNS and NSN templates of Fig. 5.21 do not extend to the seed without interruption. The fact that such an interruption of TiN hinders successful growth in our templates might further substantiate the finding that TiN plays an active role in the dynamics of hybrid-TASE. In particular, precursors might have a high sticking coefficient and diffusion length on a TiN surface (see section 2.6.2). If precursors cannot efficiently reach the Si seed by diffusion on a continuous TiN surface, they might accumulate on the template surface and nucleate there. This interpretation could be consistent with our finding in section 5.2.2 of accelerated growth rates in hybrid templates with continuous TiN segments. Nevertheless, we do not rule out that successful epitaxy inside templates with the geometries of Fig. 5.21 could be possible in the future. Detailed understanding of the processes at play, highly controlled template fabrication, and epitaxy runs in a wide parameter space will be necessary to clarify the origins of our observations.

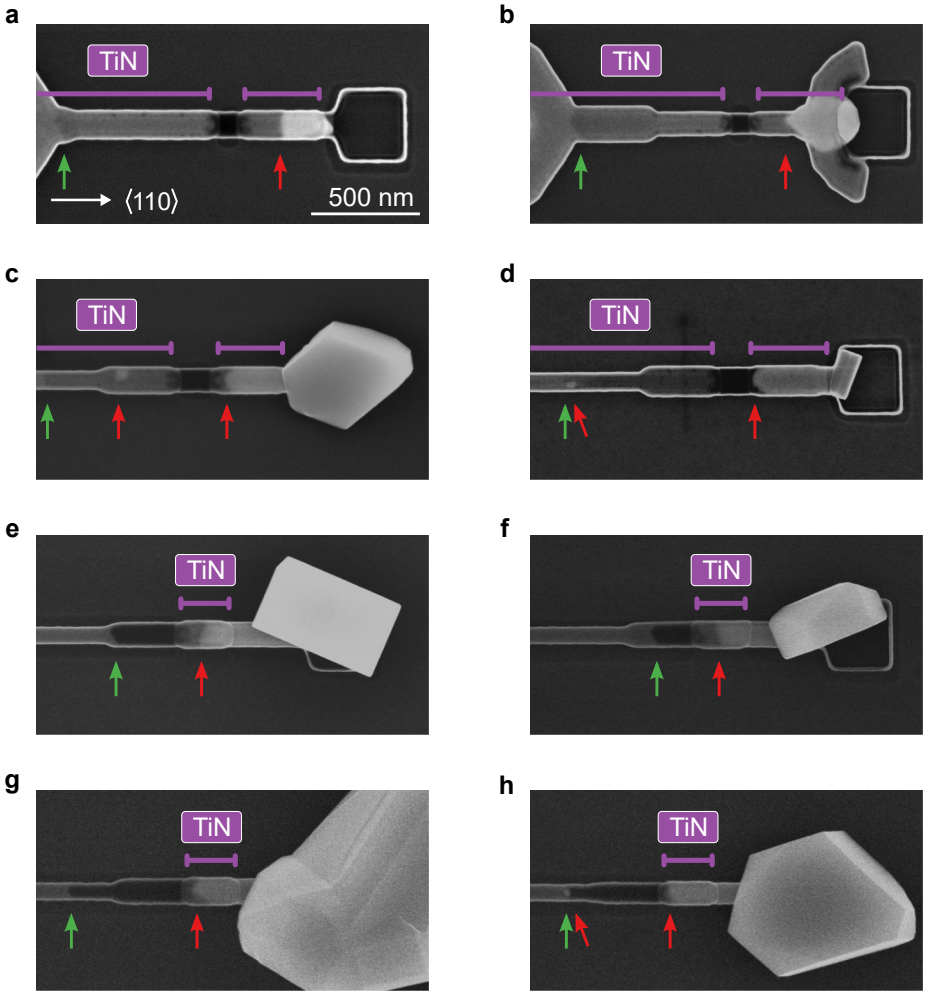

Figure 5.21. Systematic failure of hybrid-TASE in SNS and NSN geometries. Crystallographic direction and scale bar as indicated in **a** are the same for all subfigures. Position of TiN template segments is indicated by purple lines. Green arrows indicate Si seed location, red arrows highlight InAs nucleation sites. **a,b** SNS template geometry, InAs growth for 600 s at $T = 600$ °C, V/III=70, and low precursor flow. **c,d** SNS template geometry, InAs epitaxy for 600 s at $T = 550$ °C, V/III=70, and low precursor flow. **e,f** NSN template geometry, InAs growth for 500 s at $T = 550$ °C, V/III=150, same growth run as devices presented in Fig. 5.2i, Fig. 5.4e to h, Fig. 5.6, and Fig. 5.7. **g,h** NSN template geometry, InAs growth for 850 s at $T = 550$ °C, V/III=70.

5.4. Conclusions and Outlook

We demonstrated a novel method to fabricate semiconductor-superconductor hybrid structures. Our approach is based on the TASE method [90, 93, 94, 97] which we expanded by integrating self-aligned TiN elements into the template. The hybrid-TASE method stands out from established approaches to hybrid device fabrication, since it is compatible with CMOS fabrication and the III-V semiconductor can be grown as the last fabrication step. We analyzed the hybrid TiN/InAs interface using FIB+STEM and found a clean hybrid interface. Electrical characterization revealed enhanced conductance in a hybrid QPC with large transmission, while tunneling spectroscopy measurements revealed finite in-gap conductance. A hybrid-TASE device with lateral SNS geometry showed a decrease in resistance around zero magnetic field, but no supercurrent. We argued that the soft gap, as well as the absence of a supercurrent might be related to the degradation of the superconductor during high temperature fabrication. We quantified this effect by characterizing TiN reference nanowires after exposure to individual steps of the template fabrication.
Analyzing the morphology of InAs nanowires grown along various high and low-symmetry crystallograpic directions revealed significantly altered epitaxy dynamics in hybrid templates compared to standard SiO_2 templates. In particular, our findings point towards a locally increased V/III precursor ratio at the growth surface. Further, we outlined the optimization steps which enabled selective nucleation on Si and reduced parasitic nucleation on the TiN template surface. Finally, we elaborated on specific template geometries which - so far - did not allow selective epitaxy and we speculated that this finding might be related to the diffusion of precursor species on the TiN surface.

Our proof of concept is an encouraging first step towards CMOS compatible hybrid devices, yet crucial improvements are needed before the implementation of hybrid-TASE into a technology can be considered. The most urgent task is to prevent degradation of TiN during high temperature fabrication. SiN_x is a promising material for future hybrid-TASE templates, since our preliminary results showed no decrease of the TiN critical temperature after encapsulation and simulation of the epitaxy conditions (see Tab. 5.1). In selective-area-growth, SiN_x masks are routinely used, suggesting a transfer to TASE might be possible. Due to the large aspect ratio of TASE templates which sets high demands on the template surface properties for selective growth, a new template material might require recalibration of the epitaxy conditions. An alternative approach to preserve the properties of the superconductor could involve engineering of diffusion barriers around TiN elements or the use of an alternative superconductor, less susceptible to metal diffusion and oxidation.
After such fabrication improvements, important experiments presented here should be revisited. In particular, improved SNS devices with a gate will show if hybrid-TASE can serve as a platform for classical electronics applications such as (de)multiplexers or densely integrated cryogenic CMOS qubit control electronics. We note that these applications do not require a hard induced superconducting gap.

In section 5.3.2 we discussed how (seemingly minor) changes in the fabrication drastically increased the InAs epitaxy yield. Systematic optimization of TiN template surfaces could boost the yield further and will shed light on the microscopic processes at play in hybrid-TASE. Quantifying key parameters such as precursor diffusion lengths, sticking coefficients and collection areas on different template surfaces might enable growth inside more advanced template geometries. The possibility of growth inside templates with specifically tailored surface properties might further allow epitaxy of large networks and crystal phase tuning in high aspect-ratio templates, both currently inaccessible to standard TASE. The involved fabrication and susceptibility of the epitaxy yield on fabrication details suggests that such studies should ideally be performed in an industrial cleanroom.

6 Transport Experiments on Selective-Area-Grown Lead Telluride

In 2010, two theoretical proposals [261, 262] predicted the emergence of Majorana zero modes at the ends of a one-dimensional semiconductor nanowire, if an axial Zeeman field is applied, if the nanowire features strong spin-orbit coupling, and if it is proximity coupled to a superconductor. This prospect has sparked immense theoretical and experimental efforts in the field of semiconductor-superconductor hybrids [304], since Majorana zero modes could serve as the building blocks for topologically protected qubits [305]. Early experimental studies on nanowires with the above properties found zero bias conductance peaks, which were interpreted as a hallmark for such Majorana zero modes [306]. However, the disambiguity of these signatures for topological states was later questioned, since similar behavior can be reproduced by topologically trivial states [307]. Improvements in material quality, in particular of the hybrid interface, enabled a hard induced superconducting gap [263], which paved the way for careful studies of the interplay between Andreev bound states and potential Majorana zero modes [77, 290]. Further material advancements were mainly focused on combining established InAs and InSb nanowires with various superconductors. In particular, elemental superconductors such as Nb, Ta, V, Pb, and Sn [267, 269–271] hold great promise due to their large energy gap compared with Al, which is widely used in hybrid devices.

On the other hand, less attention has been paid to the investigation of alternative semiconductors with potentially advantageous characteristics. In section 2.7 we reviewed the fundamental properties of the relatively unexplored semiconductor PbTe and compared them to InAs in Tab. 2.1.
In this chapter, we present a series of transport experiments investigating the electrical properties of selective-area-grown PbTe devices (see section 3.3). We extract key characteristics such as the electron mobility, density, mean free path, and phase coherence length from PbTe Hall bars, gated nanowires, and a loop structure.

Sections 6.1 to 6.3 will be published in similar form in the publication:

Selective area growth of PbTe nanowire networks
J. Jung*, A. G. Schellingerhout*, M. F. Ritter, S. C. ten Kate,
O. A. H. van der Molen, S. de Loijer, M. A. Verheijen, H. Riel, F. Nichele,
and E. P. A. M. Bakkers (**equal author contribution*)
Manuscript in preparation (2022)

Author contributions of the parts presented here: M.F.R. and S.C.K. fabricated the devices. M.F.R., S.C.K., and F.N. performed the measurements. M.F.R., S.C.K., H.R., and F.N. interpreted and analyzed the data. M.F.R. wrote the sections of the manuscript related to transport experiments with input from J.J., S.C.K., and F.N..

6.1. Hall-Mobility

In a first set of experiments, we study the Hall mobility μ_h in selective-area-grown PbTe devices. Figure 6.1a shows a false colored SEM micrograph of a 60 nm wide nanowire with lateral side arms (Hall device 1). The channel is aligned along the $[00\bar{1}]$ direction; the side arms point in $[\bar{1}10]$ direction. Contacts (yellow) and a top gate (orange) were fabricated in two consecutive lift-off steps. A 23 nm Al_2O_3 layer served as gate dielectric (see section 3.3 for fabrication details). Measurements were performed at a temperature of $T = 20$ mK, using standard low-frequency lock-in techniques with a voltage bias V_AC between 3 μV and 10 μV. The current I_AC was measured by grounding the device via a low-impedance I-V converter, unless otherwise specified. The longitudinal and transversal voltages V_xx and V_xy, respectively, were measured from lateral device contacts (see circuit schematics in Fig. 6.2a). Figure 6.1b displays the conductance $G = I_\mathrm{AC}/V_\mathrm{xx}$ as a function of top gate voltage V_TG. At zero perpendicular magnetic field $B_\perp = 0$, a conductance plateau is observed at $G_0 = 2e^2/h$. At $B_\perp = 6$ T, an additional step emerges at e^2/h (see arrows in Fig. 6.2b, trace offset by G_0), which is also recognized in the transconductance $\mathrm{d}G/\mathrm{d}V_\mathrm{TG}$ plot of Fig. 6.1c. From bias spectroscopy measurements (not shown) a gate lever arm of 0.033 was extracted, yielding a Landé g-factor of 23 for the level splitting of the first plateau (arrows in Fig. 6.1c). In Fig. 6.1d the longitudinal and transversal resistivities ρ_xx and ρ_xy were measured as a function of $B_\perp$. In this specific measurement, a current bias $I_\mathrm{AC} = 10$ nA was used. The longitudinal resistivity ρ_xx showed aperiodic mesoscopic fluctuations and ρ_xy exhibited an offset at $B_\perp = 0$. This offset is similar to ρ_xx and is attributed to the device geometry, which features opposing side arms that have a lateral offset similar to the width of the nanowire [308]. For the following analysis, a rectangular nanowire cross-section was assumed (see Fig. 3.5b) so that $\rho_\mathrm{xx} = 1/(\mu_\mathrm{h} e n_e) = R_\mathrm{xx} \cdot WH/L$ and $\rho_\mathrm{xy} = B_\perp/(e n_\mathrm{e}) = R_\mathrm{xy} \cdot H$. Here, the channel width is $W = 60$ nm (Hall device 1) or $W = 80$ nm for a second device (Hall device 2). Both devices have a height $H = 50$ nm, and length $L = 1$ μm. μ_h is the Hall mobility, e the elementary charge, and n_e the electron density. The dependence of μ_h on n_e was extracted by measuring ρ_xx and ρ_xy as a function of V_TG. The relation is shown in the parametric plot of Fig. 6.1e for Hall device 1 (blue) and Hall device 2 (red). The highest

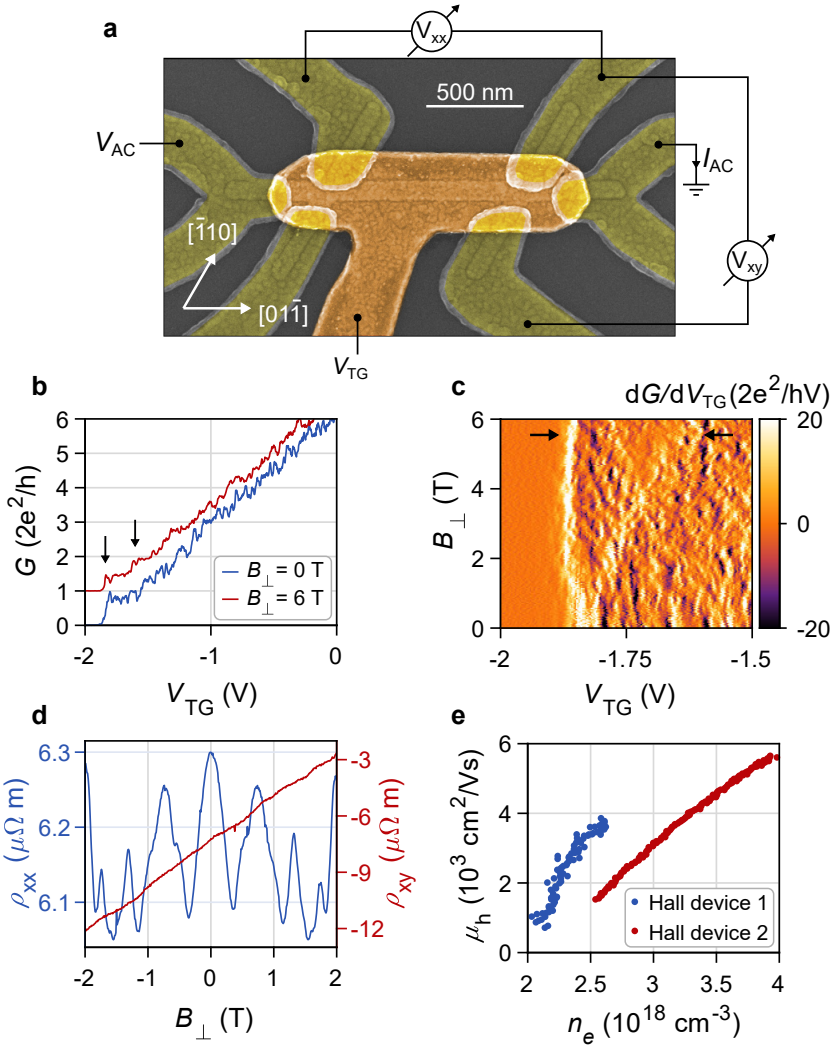

Figure 6.1. Hall mobility measurements. a Schematic measurement setup and false colored SEM micrograph of a PbTe Hall bar (Hall device 1) with a channel width of 60 nm. Contacts are highlighted in yellow, the top gate is orange. **b** Wire conductance as a function of V_{TG} at $B_\perp$=0 and 6 T (trace offset by G_0). The first conductance plateau splits at high field (arrows). **c** Transconductance as a function of $B_\perp$. The plateau splitting is indicated by arrows. **d** Longitudinal and transversal resistivity as a function of $B_\perp$ at $V_{TG} = 0$. **e** Parametric plot of the Hall mobility μ_h versus carrier density n_e of Hall device 1 and 2 with 60 nm and 80 nm width, respectively.

mobility of 3800 $cm^2/(Vs)$ (Hall device 1) and 5600 $cm^2/(Vs)$ (Hall device 2) was reached at $V_{TG} = 0$. These values correspond to a mean free path of $l_e = \mu_h m^* v_F/e \approx 100$ nm for Hall device 1 and $l_e \approx 180$ nm for Hall device 2. Here, the Fermi velocity v_F was calculated from the Fermi momentum $p_F = m^* v_F = \hbar k_F$ with $k_F = (3\pi^2 n_e)^{1/3}$. The

lowest mobility values in Fig. 6.1e are reached at $V_{\mathrm{TG}} = -1.6\ V$ (Hall device 1) and $V_{\mathrm{TG}} = -5\ V$ (Hall device 2). The range of V_{TG} was limited to $V_{\mathrm{TG}} \leq 0$, since devices showed leakage through the InP substrate at small positive V_{TG}[1]. Each point in Fig. 6.1e was averaged from ρ_{xx} and ρ_{xy} recorded at four values of V_{TG}. We note that measurements on Hall device 1 were performed at $T = 3.8$ K, though we do not expect significant change to μ_{h} at lower temperature, since all other devices showed constant μ_{h} below 3.8 K.
This, together with a higher mobility consistently found in devices with larger cross-section, suggests that the dominant mechanism limiting mobility in our devices is interface scattering. Similar conclusions were reached in an early study of μ_{h} in PbTe [129] and in a recent work, which found increased field effect mobility in PbTe devices with a CdTe capping layer [106].

6.2. Field Effect Mobility

We compare the Hall mobility values extracted in the previous section to field effect mobility μ_{f} experiments on the top-gated PbTe nanowire presented in the false colored SEM micrograph of Fig. 6.2a. The PbTe nanowire (red) is 60 nm wide, approximately 50 nm high, aligned along the $[\bar{1}2\bar{1}]$ direction, has a channel length of $L = 640$ nm, and is contacted by Ti/Au electrodes (yellow). As in the Hall bar device, a 23 nm Al_2O_3 layer served as a gate dielectric. The top gate is highlighted in orange. Figure 6.2b plots the channel conductance as a function of top gate voltage V_{TG}. A hysteretic behavior was observed between sweep directions, which was not seen in Hall bar devices discussed in section 6.1. We will comment on this behavior in more detail below.
Assuming a rectangular nanowire cross-section and a dielectric constant of $\varepsilon_{\mathrm{r}} = 9$ for Al_2O_3, finite element simulations of the gate capacitance yield $C = 130$ pA.[2] The field effect mobility μ_{f} was estimated by fitting of the model [309]:

$$G\left(V_{\mathrm{TG}}\right) = \left[R_{\mathrm{C}} + \frac{L^2}{\mu_{\mathrm{f}} C\left(V_{\mathrm{TG}} - V_{\mathrm{th}}\right)}\right]^{-1} \tag{6.1}$$

where the contact resistance $R_{\mathrm{C}} \approx 70\ \Omega$, the threshold voltage $V_{\mathrm{th}} \approx -5.94$ V, and the field effect mobility $\mu_{\mathrm{f}} \approx 6400\ \mathrm{cm}^2/(\mathrm{Vs})$ are variables of the fit.
We note that μ_{f} is similar to reports on buffered InAs nanowires [84] and similar to μ_{h} in our devices (see section 6.1). However, direct comparison between μ_{f} and μ_{h} in our work is not straightforward. First, the gate capacitance had to be estimated to extract μ_{f} (see equation 6.1). This estimation was based on the device geometry, which depends on the details of the wire height, facets, and overgrowth. These parameters were extracted from STEM analysis of the cross-section on similar devices. Second, devices in

[1] Such leakage was consistently found across more than 15 devices on several chips. It was observed irrespective of the gate dielectric material and for both top gates and side gates. We suspect that this leakage occurs at the contact pads, due to the wirebond contacting the InP substrate. A thick insulating layer below the contact pads could solve this issue in future devices.
[2] Simulations were performed by A. G. Schellingerhout.

Figs. 6.1a and 6.2a are aligned along different crystallographic directions. This results in distinct cross-sectional shapes due to the specific terminating facets. Furthermore, a highly anisotropic effective electron mass m_e^* is expected in PbTe (see Tab. 2.1), suggesting that electron mobility depends on the channel direction. Measurements on four other Hall bar devices and two other top-gated nanowires did not yield a systematic correlation between mobility and crystal direction in our devices. However, such devices had lithographic widths ranging from 60 nm to 100 nm, had different fabrication details, and were measured in various setups. All of these factors make direct comparisons difficult.

The mobility of our devices is similar to that found in InAs nanowires selective-area-grown on a buffer layer [84]. A future study could investigate, if this approach can be transferred to PbTe on InP and whether this can enhance mobility. Furthermore, a systematic study of mobility on crystal direction could elucidate the anisotropic transport characteristics of PbTe. Such experiments could be realized by patterning Hall bars along various directions on the substrate, similar to previous experiments on selective-area-grown InAs [80].
Finally, we comment on the hysteresis found in the device of Fig. 6.2a. The traces in Fig. 6.2b were highly reproducible when repeating the measurements and independent of the sweep rate. Other devices that required larger absolute V_{TG} to tune the wire conductance generally showed more pronounced hysteresis. This finding might point towards charge rearrangement in the dielectric layer, therefore further optimization of our fabrication protocol (see section 3.3) will be required to allow for high control of future devices.

6.3. Aharonov-Bohm Experiments

Aharonov-Bohm experiments were performed on the device shown in Fig. 6.3a. The PbTe ring (red) has a circumference of $L = 4$ μm and a lithographic channel width of 100 nm. Contacts are highlighted in yellow, side gates (gray) were not operated in this experiment and remained grounded. Measurements were performed using standard low-frequency lock-in techniques and sourcing a current $I_{\mathrm{AC}} = 400$ pA while measuring the voltage across the device. The loop resistance R as a function of the perpendicular magnetic field $B_\perp$ exhibits periodic oscillations with an amplitude of up to 200 Ω (Fig. 6.3b). The following analysis is performed after subtracting a low-frequency magnetoconductance background, which is indicated in Fig. 6.3b. Data after background subtraction is presented in Fig. 6.4a and its Fourier spectrum is shown in Fig. 6.3c. The latter exhibits distinct peaks which can be identified as h/e and $h/2e$ oscillations, since their periodicity of 5.6 mT and 2.8 mT, respectively, corresponds to an area of 0.74 μm^2, in good agreement with the lithographic area of 0.68 μm^2 enclosed by the PbTe loop. An additional low-frequency peak in the Fourier spectrum is attributed to a residual magnetoconductance component after background subtraction. Inverse Fourier transforms of the spectrum in Fig. 6.3c were computed after applying a Gaussian filter

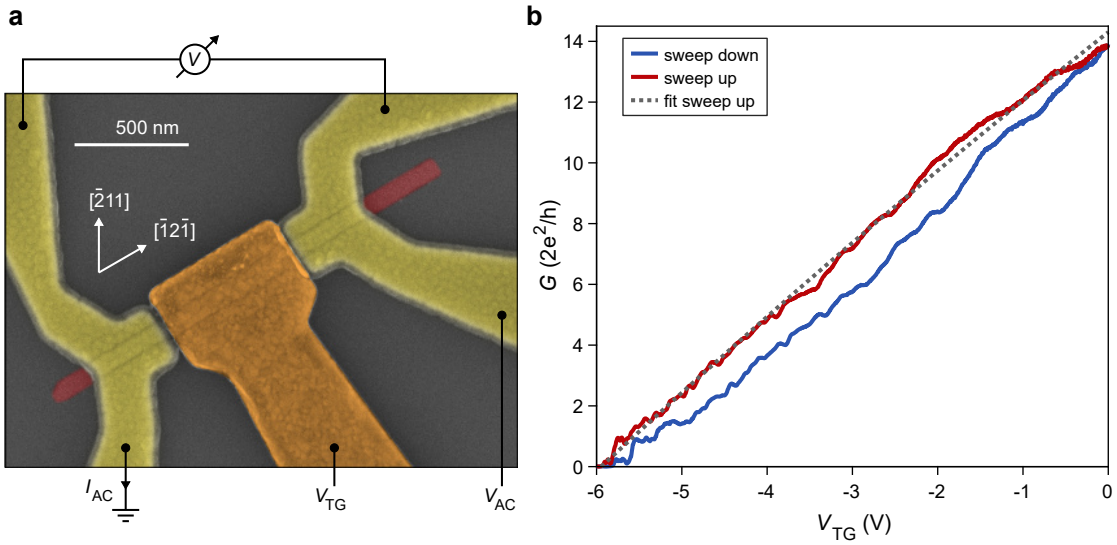

Figure 6.2. Field effect mobility. a False colored SEM micrograph of a PbTe nanowire (red) with contacts (yellow) and a top gate (orange). The measurement setup is indicated schematically. Nanowire and gate are separated by a 23 nm Al_2O_3 dielectric layer. **b** Nanowire conductance as a function of top gate voltage V_{TG} for both sweep directions. A fit to the sweep up trace yields a mobility of $\mu_f \approx 6400$ cm^2/(Vs). Details are described in the text.

centered around 180 mT^{-1} or 360 mT^{-1} with $\sigma = 60$ mT^{-1} to extract the h/e or $h/2e$ periodic signal, respectively. The corresponding inverse Fourier transformed signals are presented in Fig. 6.4b and c. Their characteristic beating reflects the multiple closely-spaced peaks in the Fourier spectrum of Fig. 6.3d. We note that similar signatures were previously attributed to an interplay between h/e oscillations and background conductance fluctuations [310], mixing between subband modes as a consequence of a finite channel width [311], multiple longitudinal modes [312], and effects from slightly varying AB oscillation frequencies of counter-propagating waves [313].

We analyzed the temperature dependence of the $h/2e$ amplitude $A_{h/2e}$ to extract the electronic phase coherence length $l_\varphi(T)$ in our device. As noted in chapter 2.8, the Altshuler-Aronov-Spivak (AAS) effect [132] occurs due to the interference of time reversed paths, making AAS oscillations more robust against disorder than Aharonov-Bohm oscillations [130, 134]. Consequently, $A_{h/2e}$ is less sensitive to the specific impurity configuration in the arms of the loop, compared with $A_{h/e}$. The amplitude $A_{h/2e}$ was extracted by applying a Gaussian filter to the Fourier spectrum centered around the $h/2e$ period and subsequently integrating the filtered signal. The parameters of the filter were the same as described above. Figure 6.3d plots the temperature dependence of $A_{h/2e}$. The insets show high-field raw data at 12 mK and 800 mK, highlighting the decrease of the oscillation amplitude as T increases. The temperature dependence of the h/e periodic signal with amplitude $A_{h/e}$ is plotted in Fig. 6.5. We fit both $A_{e/h}$ and $A_{h/2e}$ with a model of the form [314]:

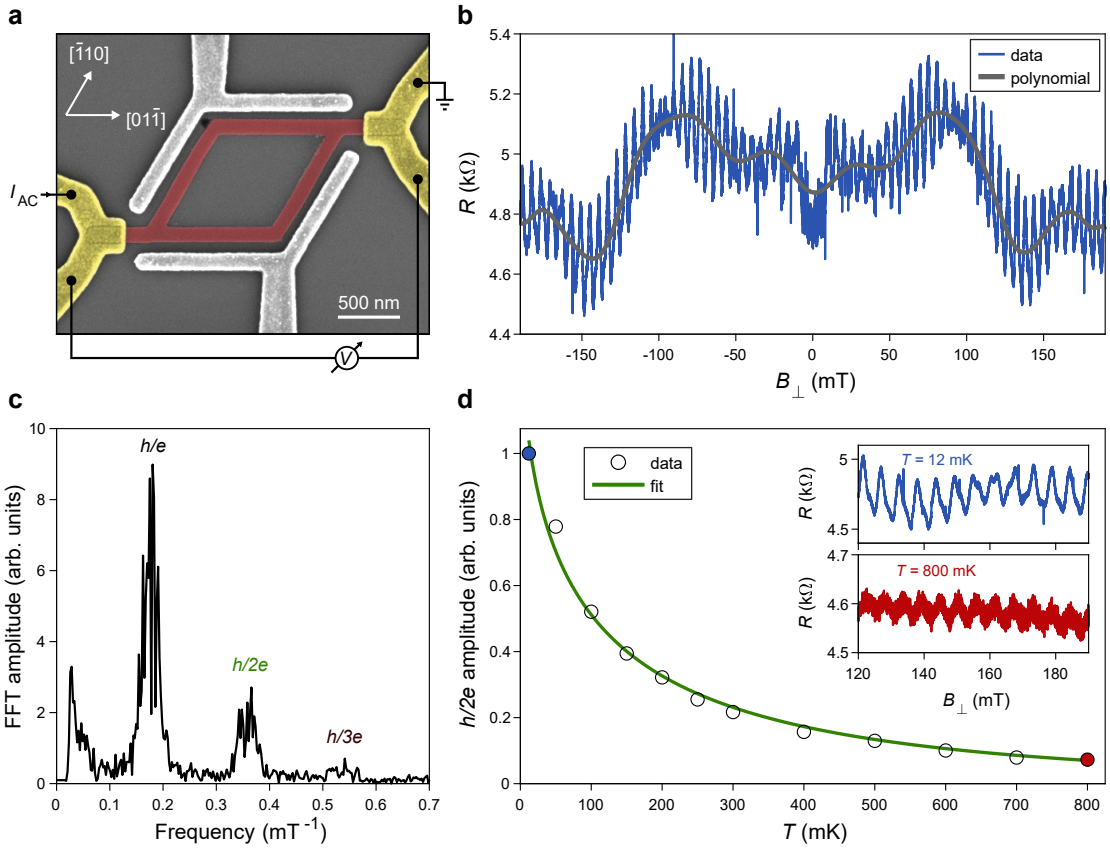

Figure 6.3. Aharonov-Bohm experiments. **a** False colored SEM micrograph of an Aharonov-Bohm device and simplified measurement setup. The PbTe ring is highlighted in red, contacts are colored in yellow. Sidegates (gray) are not operated in this experiment. **b** Device resistance R as a function of the perpendicular magnetic field $B_\perp$ and polynomial magnetoconductance background. **c** Fast-Fourier transform spectrum of data in **b** after subtraction of the low-frequency background. **d** Amplitude of the $h/2e$ oscillations as a function of temperature T. A fit to Eq. 6.2 (green line) yields a phase coherence length of $l_\varphi = 21.3\ \mu$m. The inset shows the device resistance R at high $B_\perp$ for $T = 12$ mK (blue) and $T = 800$ mK (red). Raw data at intermediate temperatures (empty markers) is shown in Fig. 6.6.

$$A_{h/ne}(T) = A_0 \cdot \exp\left(-\frac{nL}{l_\varphi(T)}\right). \tag{6.2}$$

Here, $l_\varphi(T) = C \cdot T^{-m}$ is the phase coherence length with $m = 1/2$ in the diffusive regime, n is the winding number and A_0 and C are fit parameters. For the h/e periodic signal, we have $n = 1$, for $A_{h/2e}$ the winding number is $n = 2$ (see Fig. 2.10). The fit in Fig. 6.3d is computed after extracting $A_{h/2e}$ from the full data set of Fig. 6.3b, yielding

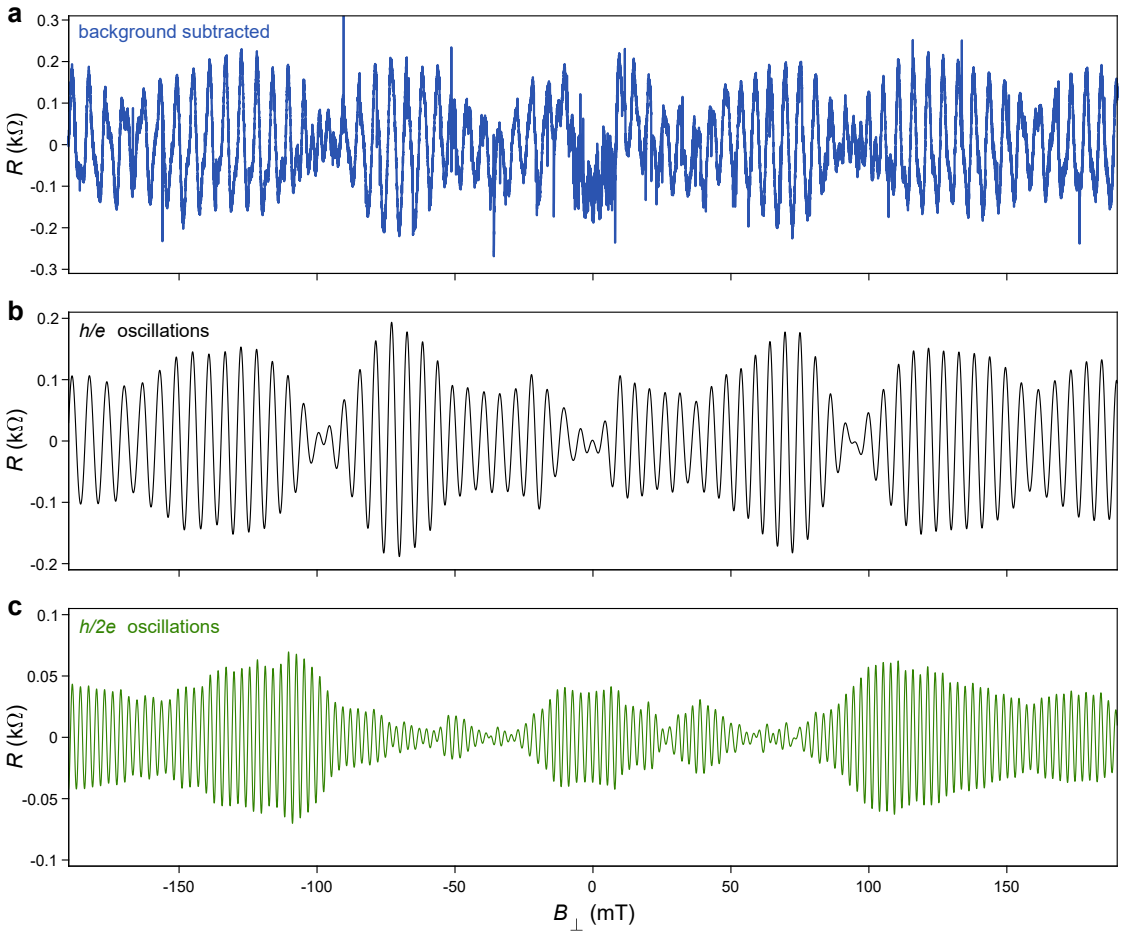

Figure 6.4. Processed data and inverse Fourier transforms. a Raw data after subtracting the background indicated in Fig. 6.3b. **b** Inverse Fourier transform of the filtered h/e signal. **c** Inverse Fourier transform of the filtered $h/2e$ signal.

$l_\varphi(12\ \mathrm{mK}) = 21.3\ \mu\mathrm{m}$. Higher l_φ are found if we limit our analysis to a smaller $B_\perp$ window (e.g. $l_\varphi > 30\ \mu\mathrm{m}$ in the case of $|B_\perp| < 80$ mT). This dependence of l_φ on the $B_\perp$ window is consistent with a fast decay of the AAS amplitude when $B_\perp$ is increased, because time reversal symmetry of AAS paths is broken [315, 316]. Fitting the full data set takes higher-order AB trajectories with $h/2e$ periodicity into account, since their interference is less sensitive to $B_\perp$ [317]. Hence, we consider the value $l_\varphi(12\ \mathrm{mK}) = 21.3\ \mu\mathrm{m}$ extracted from the full data set to be a lower bound.

We present raw data at intermediate temperatures (empty markers in Fig. 6.1d) in Fig. 6.6, highlighting the gradual decay of the oscillation amplitude as temperature is increased. Fitting the temperature dependence of $A_{h/e}$ (Fig. 6.5) yields a coherence length of $l_\varphi(12\ \mathrm{mK}) = 12.4\ \mu\mathrm{m}$, smaller than in the analysis based on $A_{h/2e}$. This finding is consistent with a higher susceptibility to energy averaging of $A_{h/e}$ compared

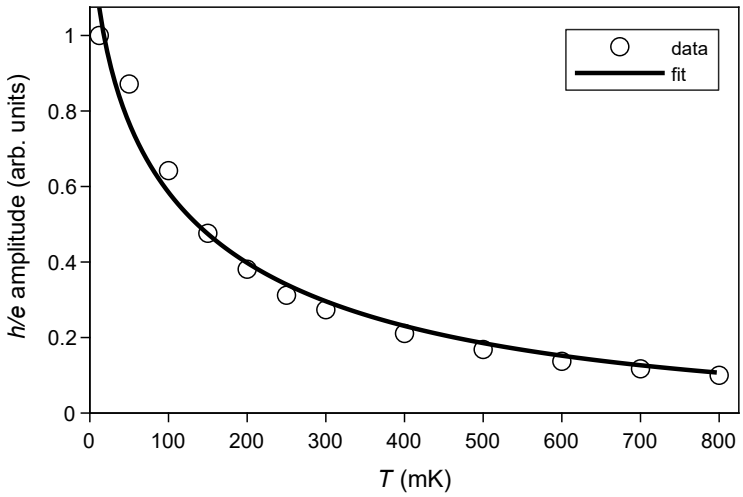

Figure 6.5. Temperature dependence of h/e oscillations. Amplitude of the h/e-periodic oscillations as a function of temperature. A fit according to equation 6.2 yields a phase coherence length of $l_\varphi = 12.4\ \mu$m.

with $A_{h/2e}$ (see section 2.8).

The phase coherence length $l_\varphi > 20\ \mu$m found in this work at the base temperature of our setup exceeds the values reported on selective-area-grown rings of InAs [80, 82, 84] and InSb [79, 83]. A recent study on PbTe structures with lattice matched CdTe substrate and capping [106] reported l_φ of approximately half the values obtained here. However, the authors of Ref. [106] used a different definition of the winding number n (see Eq. 6.2). Accounting for this discrepancy yields a phase coherence length similar to that in our work.
The high l_φ found in PbTe structures might be a consequence of the extraordinarily high dielectric constant of PbTe at low temperatures (see Tab. 2.1), leading to low electron-electron interaction. Nonetheless, we stress that a direct comparison between materials and experiments is difficult, as l_φ exponentially depends on T. Hence, small variations of the electronic temperatures in different setups and devices could affect this conclusion.

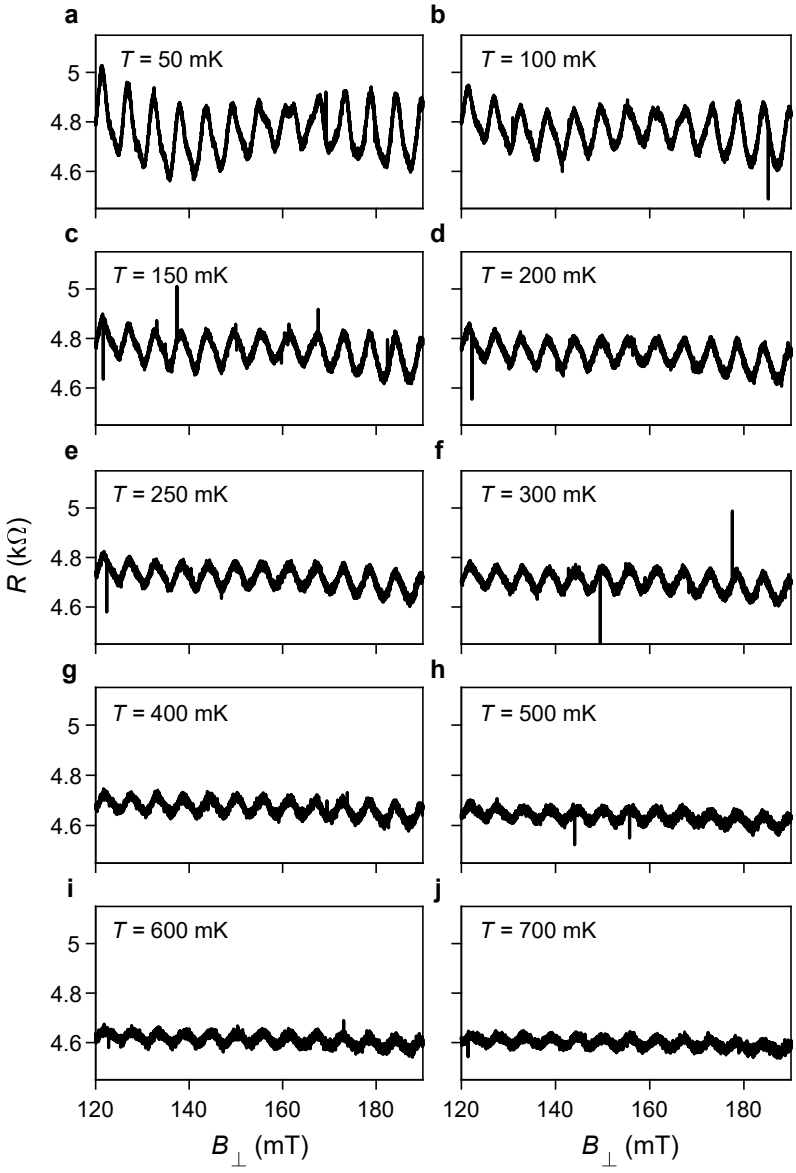

Figure 6.6. Temperature dependence of Aharonov-Bohm oscillations. Device resistance R of the Aharonov-Bohm loop presented in Fig. 6.3a as a function of perpendicular magnetic field $B_\perp$. Data at **a** $T = 50$ mK, **b** $T = 100$ mK, **c** $T = 150$ mK, **d** $T = 200$ mK, **e** $T = 250$ mK, **f** $T = 300$ mK, **g** $T = 400$ mK, **h** $T = 500$ mK, **i** $T = 600$ mK, and **j** $T = 700$ mK correspond to open markers in Fig. 6.3d.

6.4. Conclusions and Outlook

We performed a first series of experiments to determine the electrical properties of selective-area-grown PbTe structures on InP substrates. Measurements of the Hall and field effect mobility yielded peak values of $\mu_\mathrm{h} \approx 5600\ \mathrm{cm}^2/(\mathrm{Vs})$ and $\mu_\mathrm{f} \approx 6400\ \mathrm{cm}^2/(\mathrm{Vs})$, respectively. The mobility in our devices is likely limited by interface scattering, with higher mobilities found in devices with larger cross section. From a gated Hall bar, we extracted a g-factor of 23 from the Zeeman splitting of the first conductance plateau. The electron density of the Hall bar devices was on the order of $n_e \sim 10^{18}\ \mathrm{cm}^{-3}$. A loop of PbTe exhibited pronounced AB and AAS oscillations. Analyzing the temperature dependence of the $h/2e$ periodic signal yielded a phase coherence length of $l_\varphi > 20\ \mu$m at the base temperature of our setup.

Our results can serve as a starting point for future work on selective-area-grown PbTe. The high electron mobility, phase coherence length, and g-factor make it a promising building block for future hybrid devices. Therefore, the important next step will be to combine the material with a superconductor. A natural choice for the superconductor is Pb, since it can be epitaxially grown on PbTe [105] and has a large energy gap of $\Delta \sim 1.25$ meV [271]. Since both PbTe and Pb are attacked by standard chemicals (see chapter 3.3 and Ref. [271]), etching of the superconductor on PbTe wires should be avoided. Instead, Josephson junctions and advanced geometries could be fabricated via shadow epitaxy of Pb [85].
Moreover, *in-situ* grown dielectric layers (e.g. Al_2O_3) could address the chemical instability of the involved materials and protect devices during consecutive processing. Such protection layers might further serve as gate dielectrics. Some devices in our experiments (Fig. 6.2) and in other studies [105] showed reproducible hysteretic gating behavior which should be addressed in future devices to facilitate fine-tuning of the chemical potential. Moreover, next-generation devices could be grown on a buffer layer, separating PbTe wires from the InP substrate. Similar layers could also be used to cap exposed PbTe facets [105]. These adaptations might reduce interface scattering [84] and increase the charge carrier mobility further.
Finally, we note that a detailed study on the implications of the large dielectric constant in PbTe (see Tab. 2.1) could provide valuable insights. As a general question, it should be clarified whether local electrostatic gating of PbTe can be achieved despite the large dielectric constant of PbTe. Moreover, it would be interesting to investigate whether the effective impurity screening and low electron-electron interaction in PbTe could aid the realization of (Andreev) spin qubits with long coherence times.

7 Conclusions and Outlook

We explored three main topics in this thesis. Here, we briefly summarize the main findings of each project and outline future directions. A more exhaustive discussion of future experiments and applications can be found at the end of each chapter.

In chapter 4 we investigated the quench of superconductivity in **gated metallic superconducting nanowire switches**. We found that a switch to the normal state was triggered by the flow of a small gate current (section 4.1). In our devices, a switching power of 70 pW was sufficient to drive a superconducting nanowire into the normal state. The gate current was composed of high-energy electrons which created quasiparticles when impinging on the nanowire. Remarkably, similar actuation was achieved if the gate current was routed at a distance of ~ 1 μm from the nanowire and without electrons reaching the nanowire (section 4.3). In that case, superconductivity was quenched by out-of-equilibrium substrate phonons which were excited as electrons relaxed far from the nanowire. Crucially, both the direct quasiparticle injection as well as switching via a remote gate current created a non-equilibrium state distinct from thermal heating (section 4.3.5).
The devices investigated in this work can find immediate application as switching elements in superconducting signal routers and multiplexers. Given the spatial spread of quasiparticles and phonons over a length scale of ~ 1.8 μm in our devices (section 4.1.6), and the device geometry, which was not yet optimized for ultimate power efficiency, more work is required to achieve dense integration of switches with quantum hardware. In section 4.6 we suggested future experiments to quantify the long-ranged properties of phonons and we proposed device geometries to mitigate the spread of phonons and confine quasiparticles to localized injection regions.

In chapter 5 we developed a new method for semiconductor-superconductor hybrid device fabrication. At the heart of this method was the **growth of InAs inside superconducting templates**. The InAs crystal nucleated from a Si seed inside the template (section 5.1.5) and a hybrid TiN/InAs interface formed as the semiconductor expanded towards the template walls. Structural analysis with STEM revealed a clean Ti/InAs interface with roughness of ~ 1 nm (section 5.1.4). We demonstrated epitaxy in hybrid templates aligned along various crystallographic directions (section 5.2.1) and found altered epitaxy dynamics compared to reference templates without TiN elements (section 5.2.2). In particular, the growth rate inside hybrid templates was increased and the facet morphology pointed towards a locally enhanced V/III material ratio. Bias spectroscopy of a hybrid tunnel junction revealed an induced superconducting gap in

InAs with a finite in-gap density of states (section 5.1.6).
In contrast to established methods, our approach to hybrid device fabrication is both scalable and CMOS compatible. This could make it an interesting platform for the realization of classical control electronics on future quantum processors. In our work, we identified key challenges that must be addressed before this application can be considered. Firstly, degradation of the superconductor during template fabrication must be prevented (section 5.2.7). Secondly, gaining a deeper understanding of the growth dynamics in hybrid templates might enable growth inside alternative template geometries (section 5.3.4) and will be vital to increase the epitaxy yield (section 5.3.2). After implementing these improvements, the devices of section 5.3.3 with Josephson junction geometries should be revisited to clarify whether gate-tunable superconductivity can be achieved in hybrid-TASE devices.

In chapter 6 we presented **transport experiments on selective-area-grown PbTe devices**. We extracted fundamental properties like the Hall mobility $\mu_\mathrm{h} \approx 5600\ \mathrm{cm}^2/(\mathrm{Vs})$, mean free path $l_e \approx 180$ nm, and phase coherence length $l_\varphi\,(12\ \mathrm{mK}) > 20\ \mu$m.
When combined with a superconductor in future devices, these characteristics make PbTe a promising candidate for the exploration of topological states in hybrid systems. Moreover, investigating the implications of the large dielectric constant on future devices and applications could prove particularly interesting.

In the introduction to this thesis we outlined the quest for alternative quantum hardware with the aim to develop a scalable quantum computer. Each project presented in this work contributes towards this overarching goal. The gated metallic superconducting switches investigated in chapter 4 can find immediate use as superconducting signal routers and multiplexers. The CMOS compatible platform for semiconductor-superconductor device fabrication developed in chapter 5 could enable the monolithic integration of classical control electronics into scalable quantum processors. Finally, the extreme material properties and high quality of selective-area-grown PbTe structures explored in chapter 6 make them promising building blocks for future qubit architectures.

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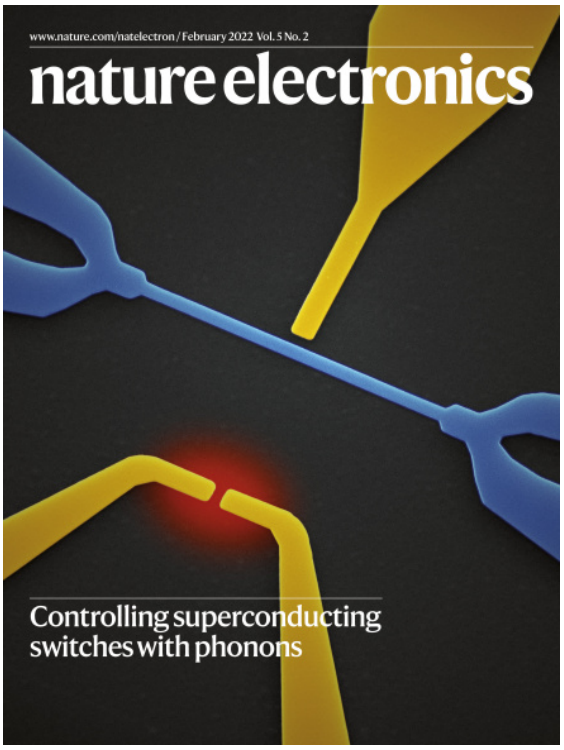

Figure A.1. Cover Nature Electronics, Volume 5 Issue 2, February 2022. False colored SEM micrograph of a TiN nanowire (blue) on a Si substrate, together with TiN gates (yellow). Image: Markus F. Ritter, cover design: Allen Beattie. Copyright 2022 Springer Nature.

Acknowledgments

"If a count were taken, the score would be
three billion [people on earth]
plus two over on the other side of the Moon,
and one plus God-knows-what on this side."

Michael Collins, Astronaut (1930-2021)
on orbiting the moon during the Apollo 11 mission

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