Adapting On Orbit: Conclusions of the STP-H6 Spacecraft Supercomputing for Image and Video Processing Experiment

Mission-Critical Computing
NSF CENTER FOR SPACE, HIGH-PERFORMANCE, AND RESILIENT COMPUTING (SHREC)
Small Satellite Conference 2022

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Outline

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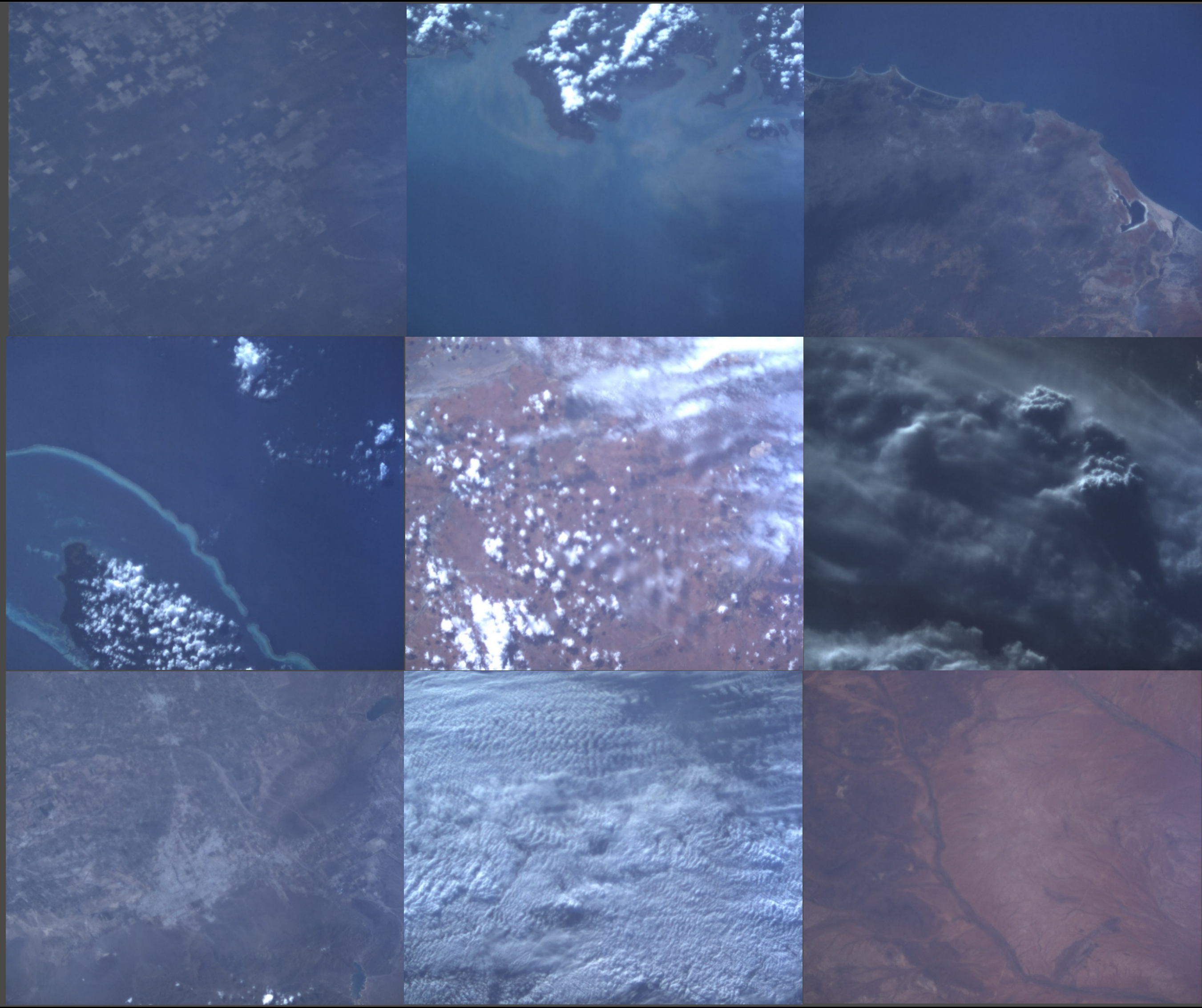
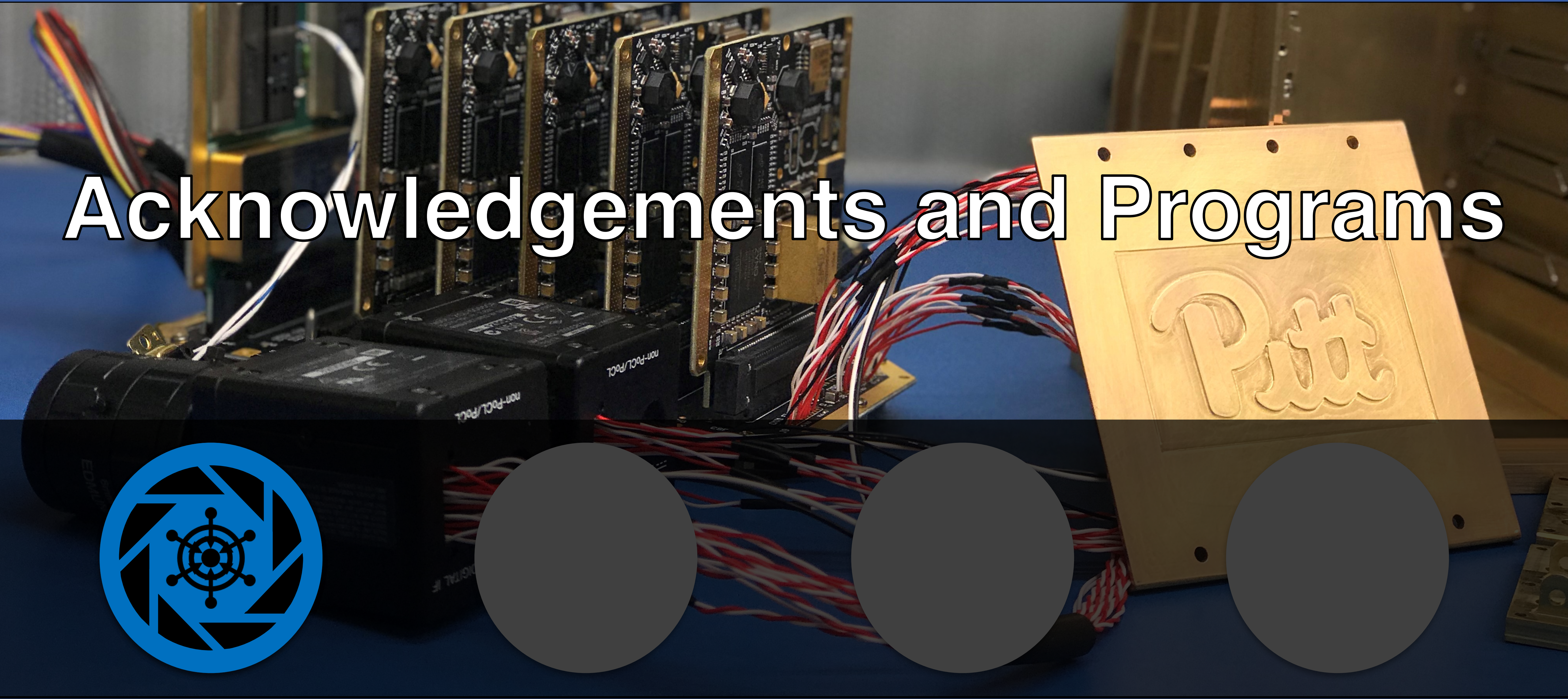


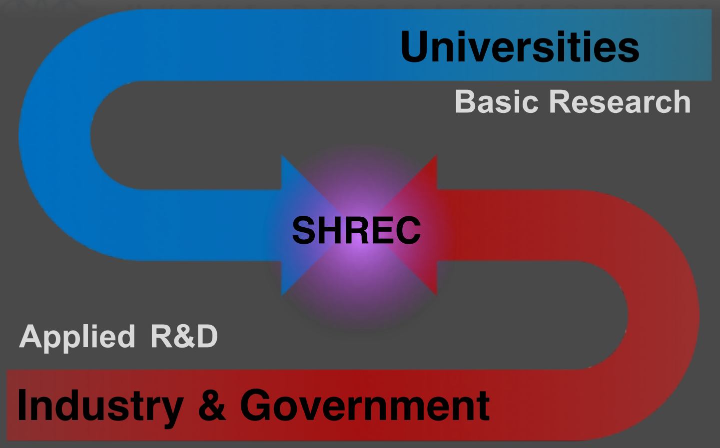
Acknowledgements and Programs



What is a SHREC?

- **NSF Center for Space, High-Performance, and Resilient Computing (SHREC)**
  - Founded in 2017
  - Formerly CHREC (2007-2017)
  - Four university sites
  - Over 30 industry and government partners
- **STP-Hx Missions are a Collaborative Effort**
  - Builds on success and experience of previous payloads and student research for experiments
  - Key development partners:
    - DoD Space Test Program
    - University of Pittsburgh
    - SHREC Members

National Science Foundation
WHERE DISCOVERIES BEGIN



See **www.nsf-shrec.org** for more info!

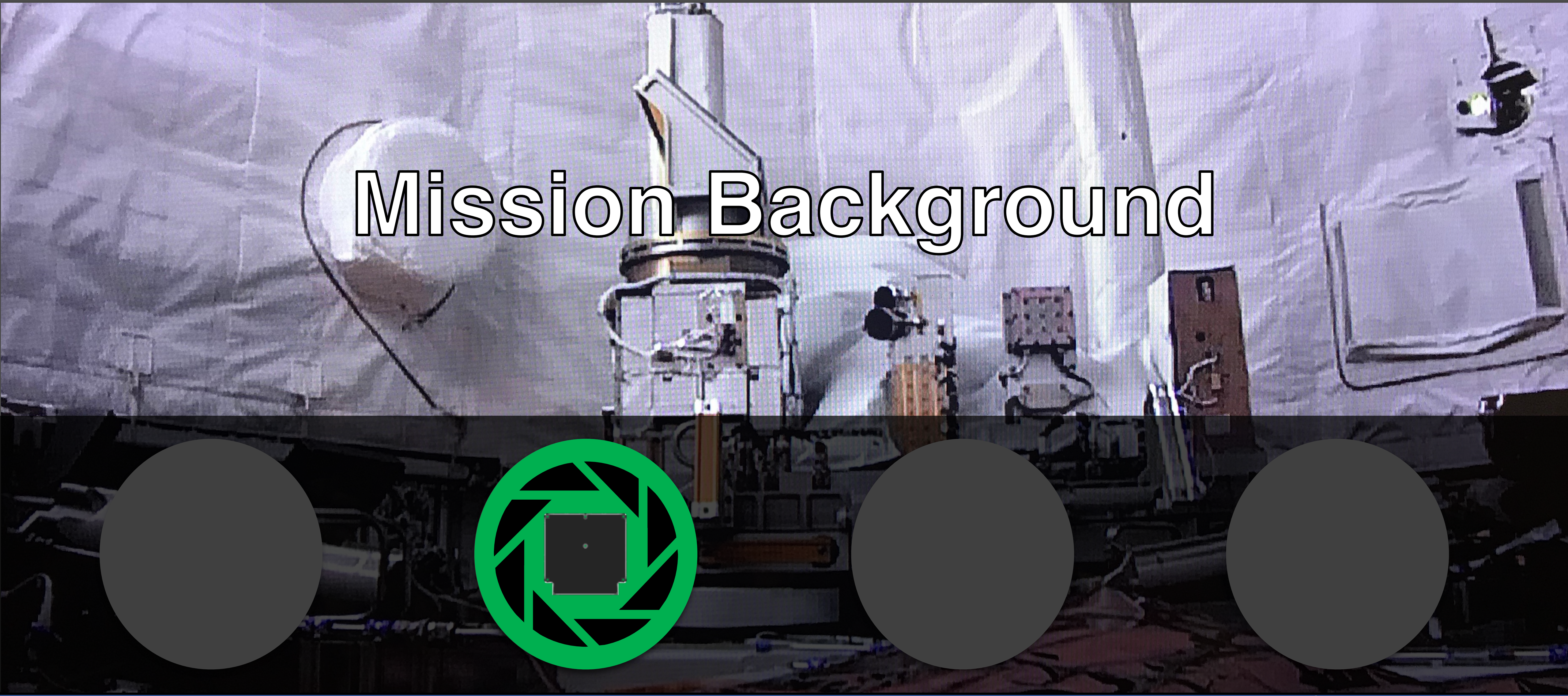
Space Test Program

- **Space Test Program – Houston**
  - Sole interface to NASA for all DoD payloads on International Space Station (ISS)
  - Timely spaceflight and payload readiness
  - Management and support for safety and integration

- **History of Mission Success**
  - Build upon successes of HREP, MISSE 6/7/8, STP-H3-5
  - Incorporate valuable lessons learned
  - Two-year build/integration schedule

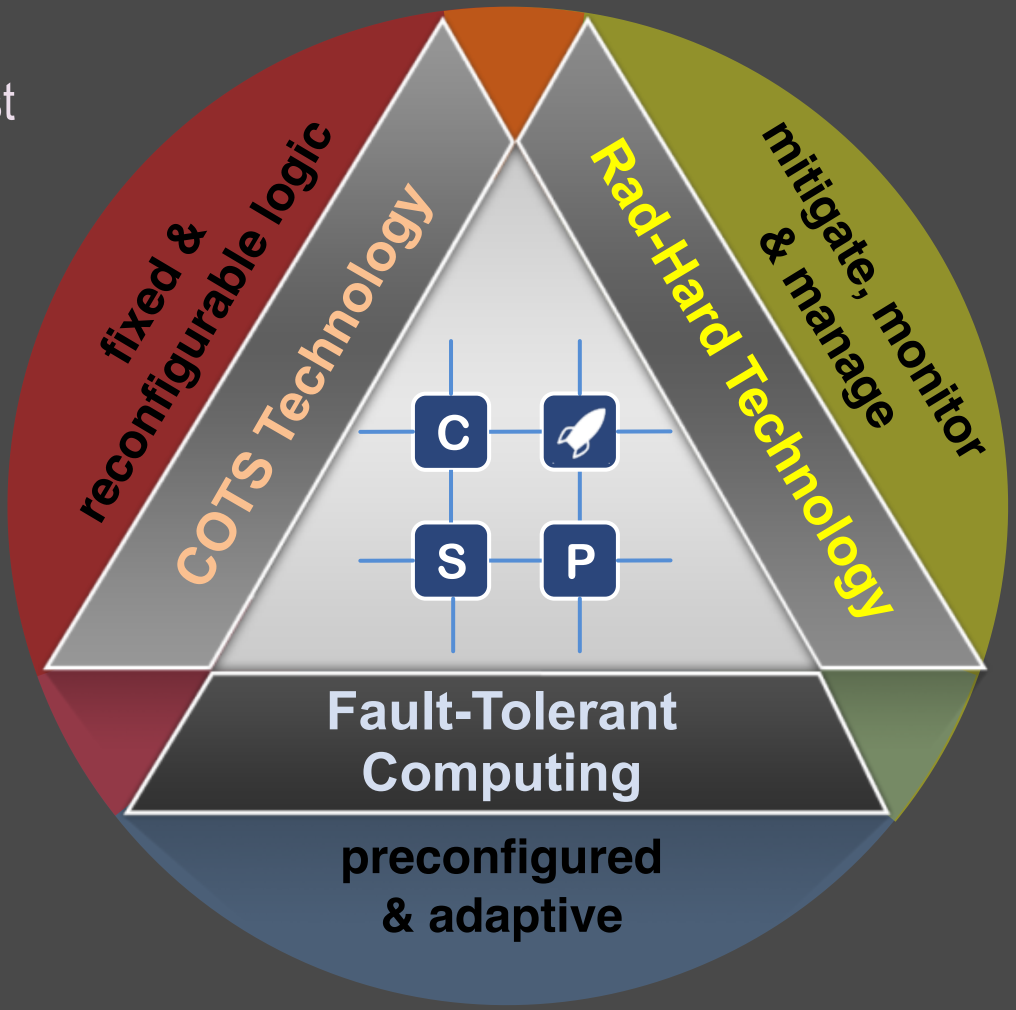
STP-H6 SSIVP was integrated and flown by the DoD Space Test Program.
Images are courtesy of the DoD Space Test Program.

Mission Background



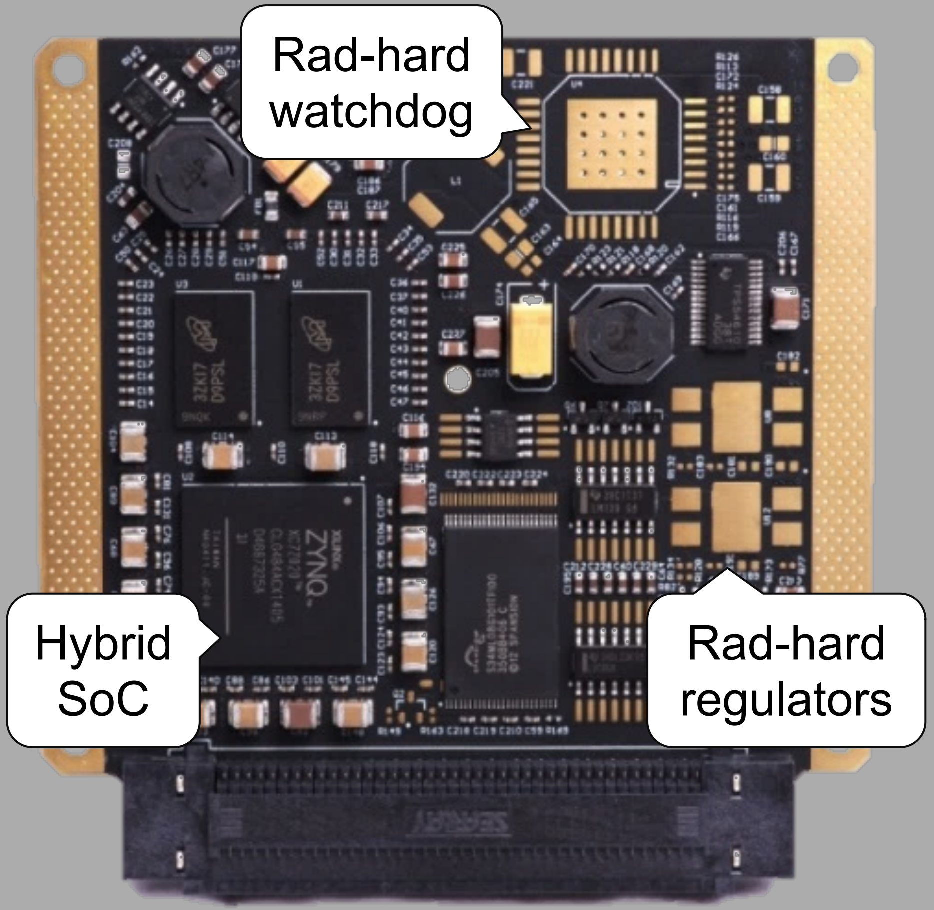
Hybrid Space Computing

- **Hybrid Design for Space Resilience**
  - Commercial devices for optimal performance, efficiency, and cost
  - Radiation-hardened components for monitoring and mitigation
  - Automotive-, industrial-, or defense-rated components
- **Hybrid System-on-Chip (SoC)**
  - General-purpose processor for core versatility
  - Field-programmable gate array (FPGA) fabric
    - Interfacing devices, sensors, networks, and I/O
    - Accelerators for mission-specific apps
- **Fault-Tolerant Computing**
  - Redundant operating-system images with checksum validation
  - Error correction codes and FPGA scrubbing



CHREC Space Processor

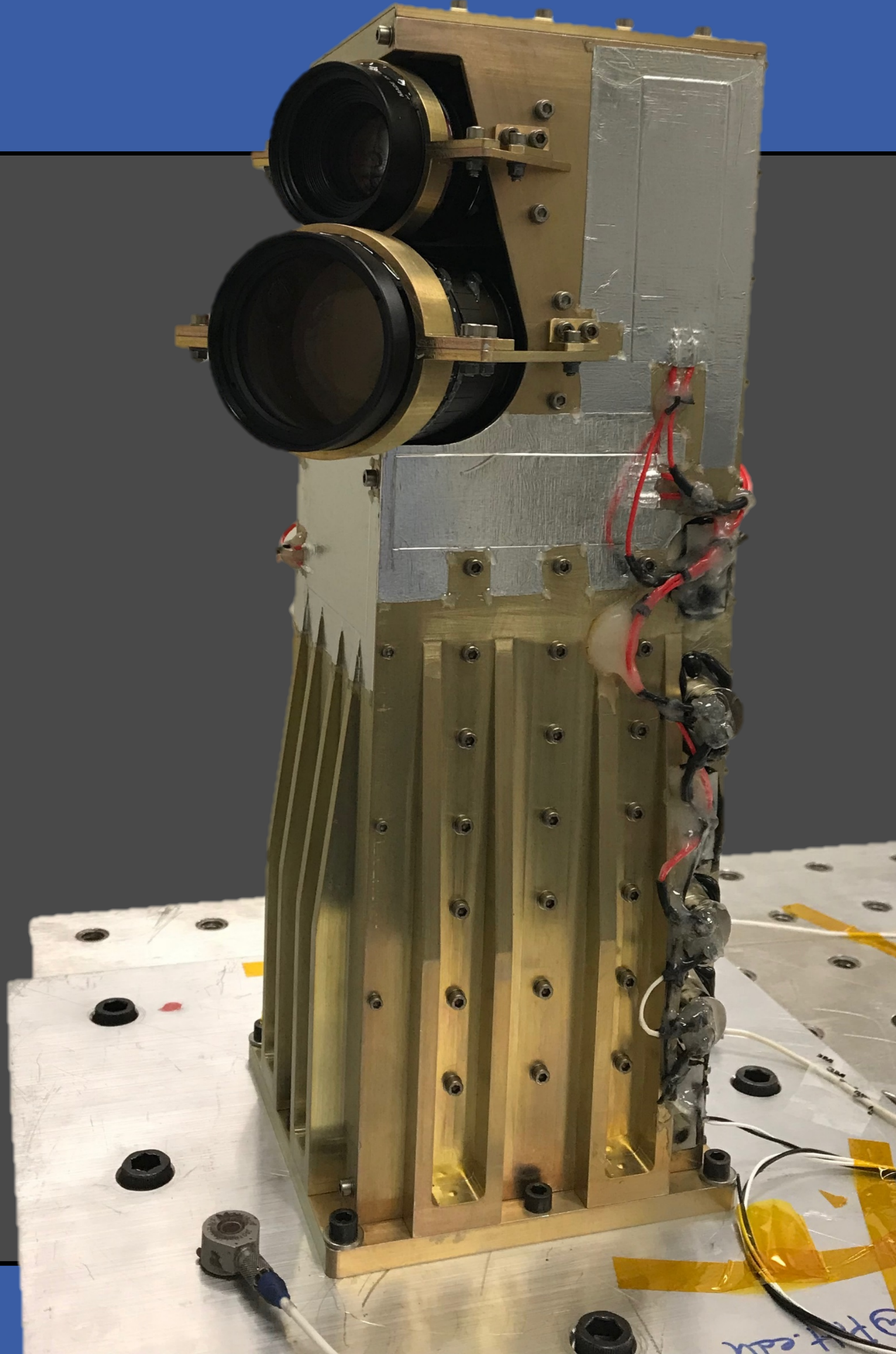
- **Selective Component Population**
  - Conventional or radiation-tolerant NAND flash
  - Radiation-hardened watchdog and reset circuit
  - Radiation-hardened power electronics
- **Xilinx Zynq 7020 SoC**
  - Dual-core ARM Cortex-A9 at 667 MHz
  - Artix-7 FPGA fabric – 90k LUTs, 220 DSPs
- **Flight Heritage and Radiation Testing**
  - STP-H5/6/7, NASA CeREs, Lockheed Martin LunIR
  - Neutron, proton, and heavy-ion characterization



LUT: Look-Up Table
DSP: Digital-Signal Processor

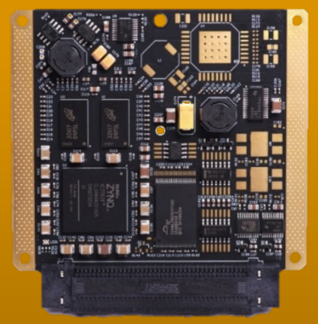
SSIVP Introduction

- **Next-Generation Spacecraft Supercomputing**
  - Develop, demonstrate, and evaluate onboard image and video processing
  - Task parallel jobs and apps like a typical supercomputing cluster
  - Compute capability enables novel algorithms such as deep learning in space
- **3U Small-Satellite Form Factor**
  - Cluster of five networked CSP flight computers
  - Two imagers with different fields of view
- **Technology Demonstration Sandbox**
  - Test student software and FPGA accelerator research in orbit
  - Deploy SHREC industry and government member apps

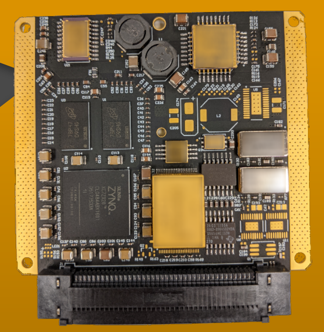


STP-H6 SSIVP was integrated and flown by the DoD Space Test Program.
Images are courtesy of the DoD Space Test Program.

SSIVP Hardware Overview



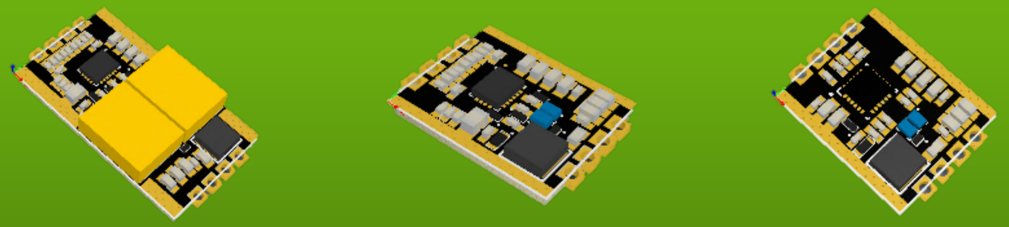
4× CSP Rev. B



CSP Rev. C

μCSP (and Smart Module, not shown)

2× 5.0 MP Sony Industrial Camera



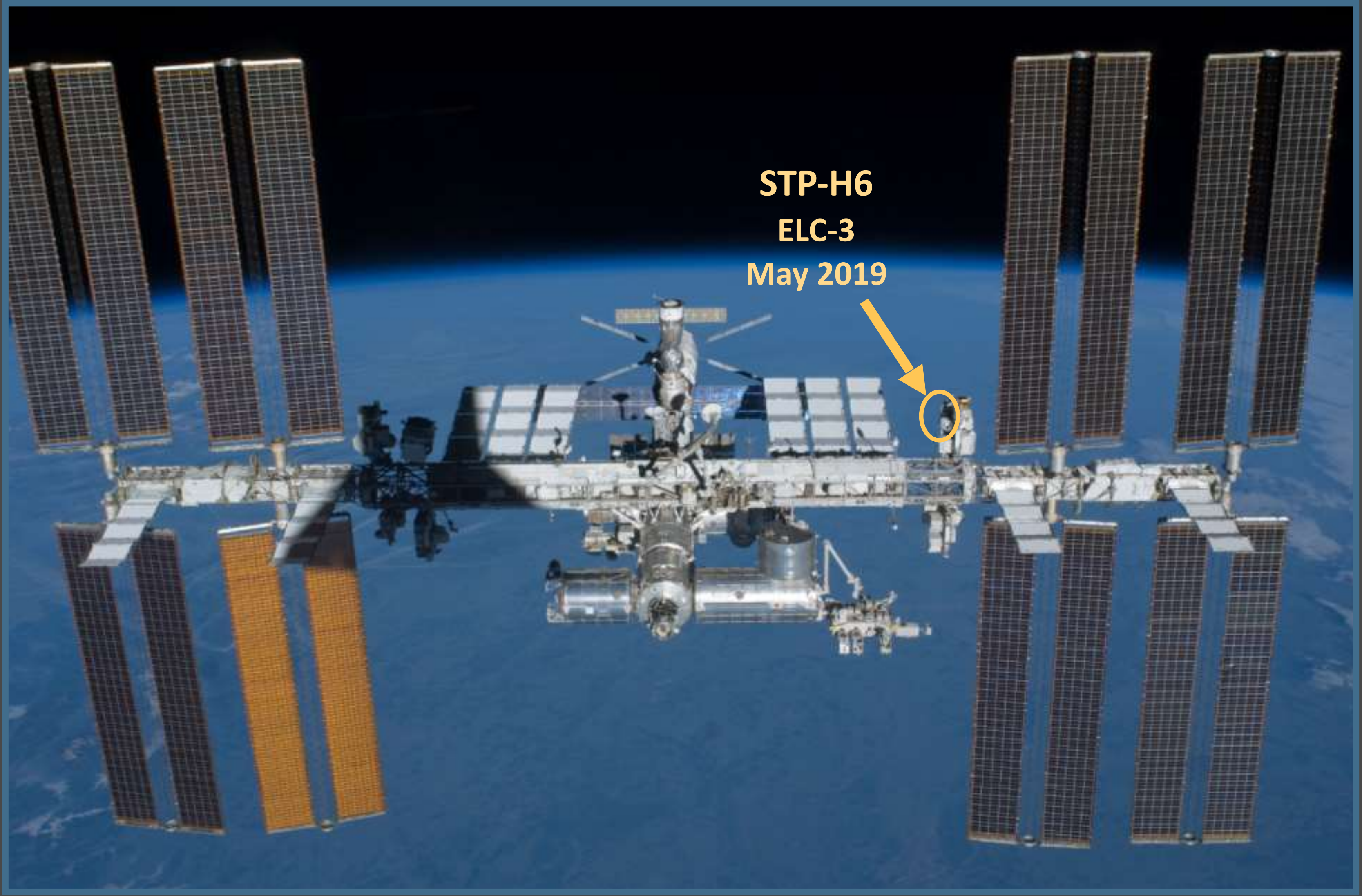
Gallium-Nitride (GaN) Point-of-Load (PoL) Converter Experiment

Approach and Experiments

Successful Launch

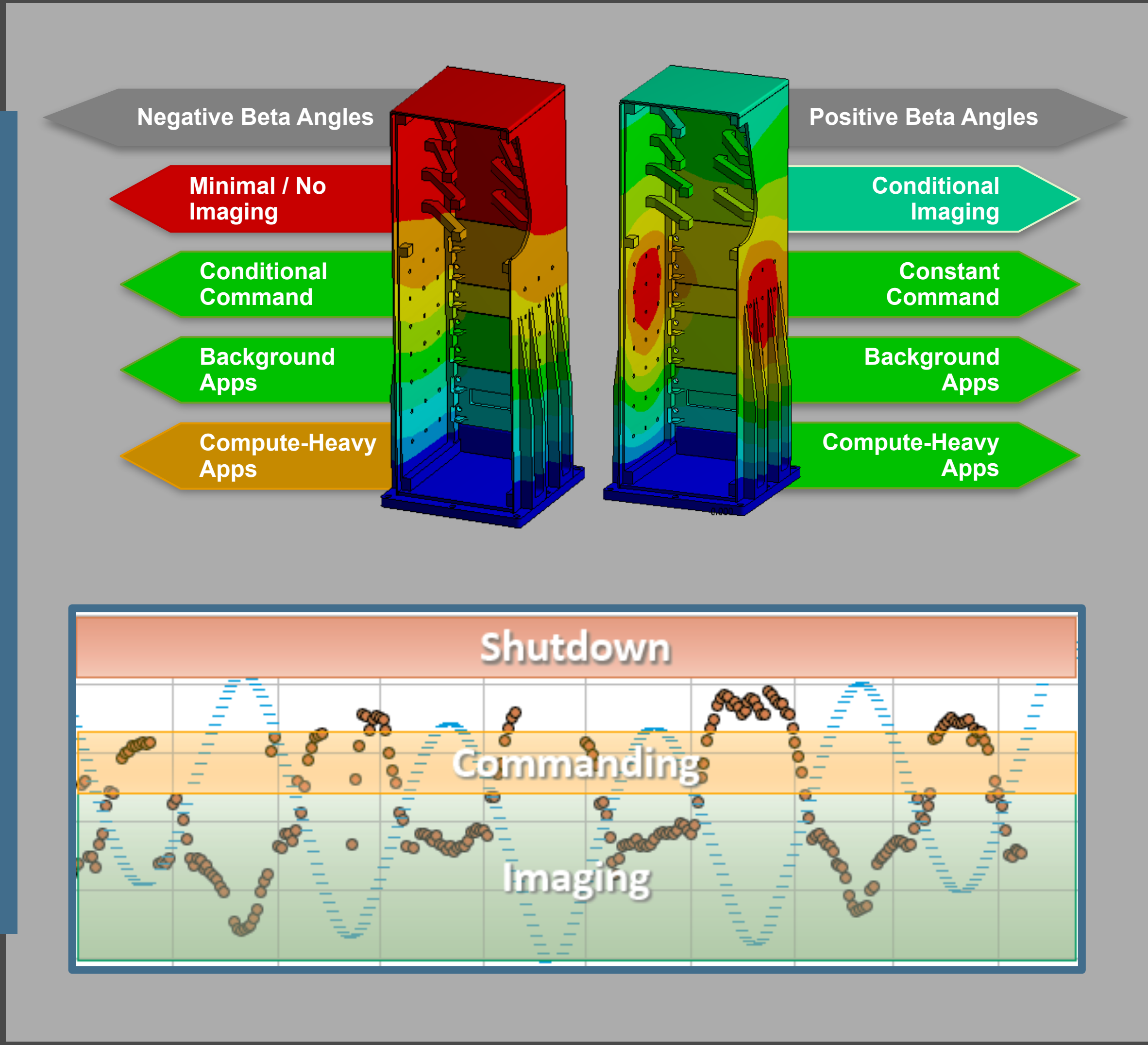
Stage Separation

Location on the ISS

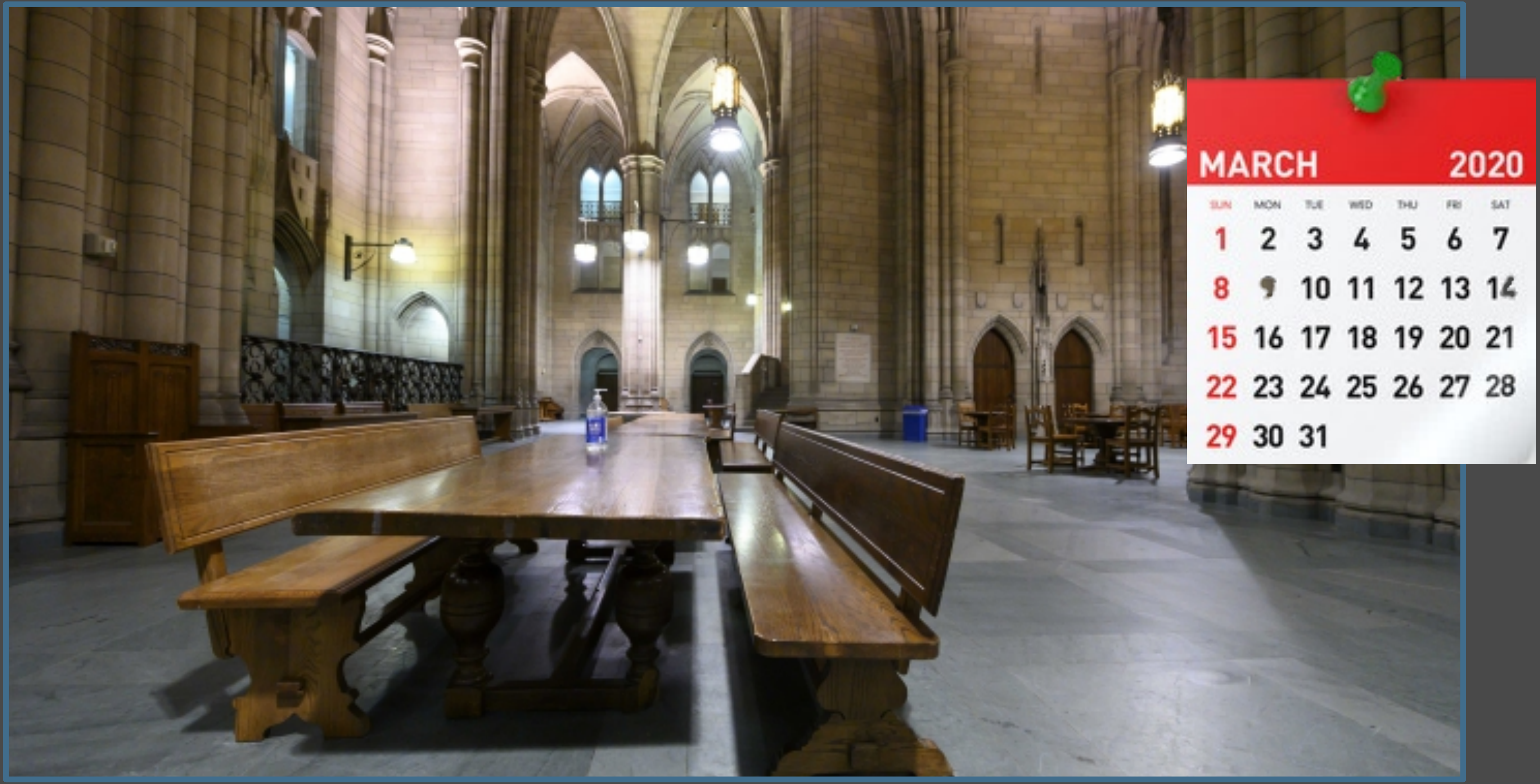


Thermal Constraints

- **Unexpected Thermal Conditions**
  - Observed high extremes at negative beta angles
  - Imagers most vulnerable: outside operating range
- **Data Collection and New Model Development**
  - Collected thermal data from devices onboard
  - Created new model of orbital conditions
- **Camera Testing**
  - Tested flight camera in new thermal window
  - Constant operation above observed temperatures
- **Software Adaptation**
  - Reduced camera duty cycle to very small periods
  - Built thermal safeguards into automation
  - Coordinated shutdowns for extreme negative betas

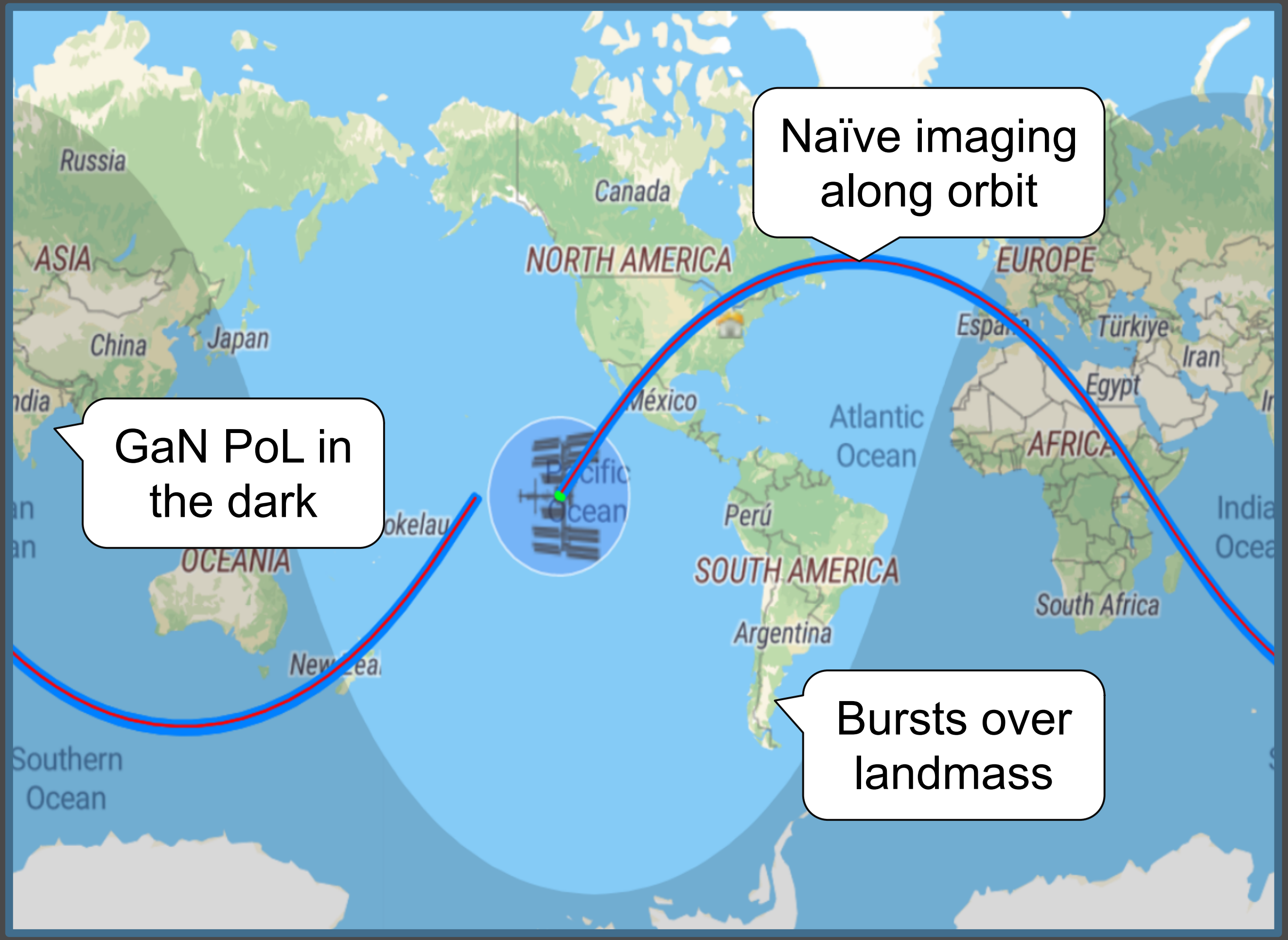


University Shutdown

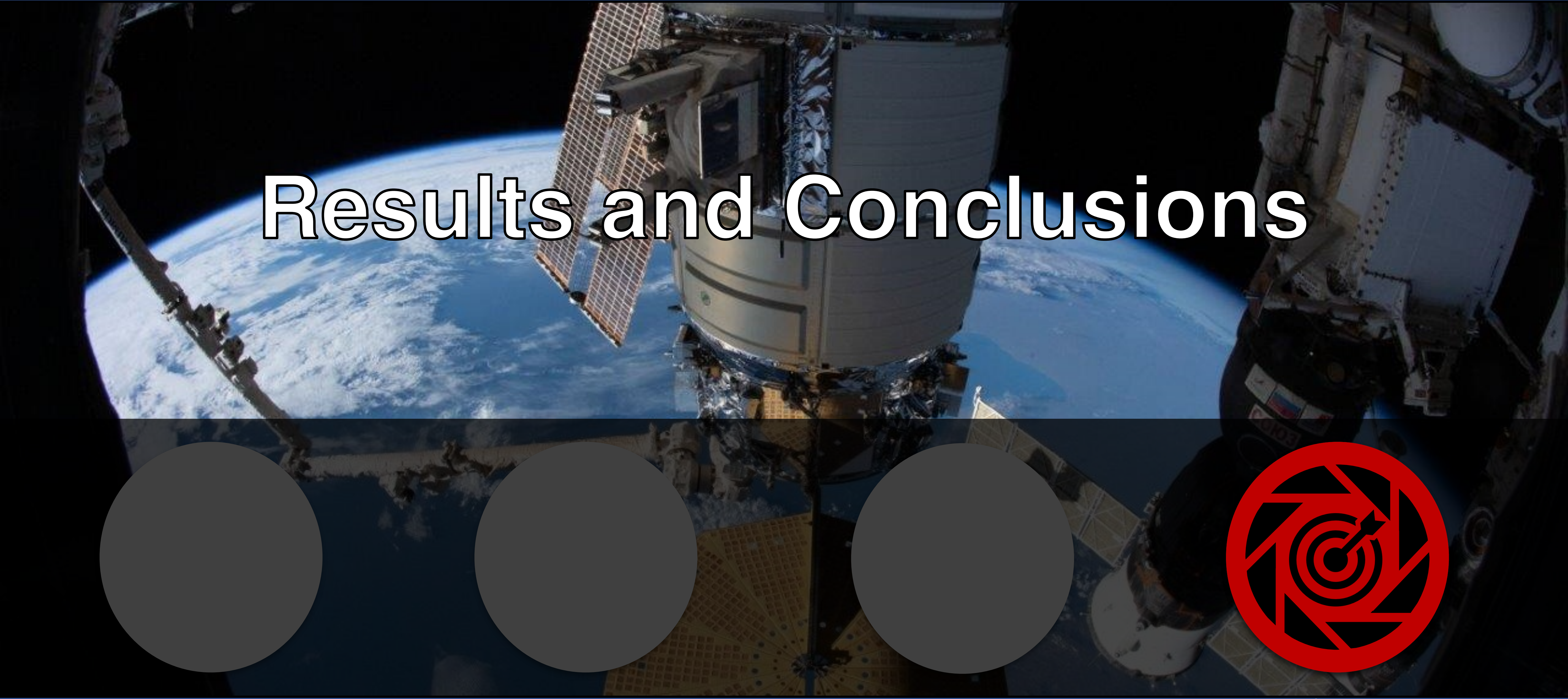


Day in the Life

- **Constant Automated Operation**
  - Naïve image capture every ten minutes
  - FPGA scrubbing and radiation upset monitoring
- **Regular Manual Commanding**
  - Manual imaging over ground targets
  - Collection of data from GaN PoL subexperiment
- **Weekly or Monthly Adaptation**
  - New function and app testing
  - Upload of new operational modes



Results and Conclusions



Review of Science Objectives

Minimum Success		Comprehensive Success	
Collect science products for at least 30 days	green	Collect science products for over one year	green
Acquire profile of daytime and nighttime full-resolution images for analysis	green	Perform autonomous algorithm correction based on observed conditions	green
Perform parallel computing experiments	green	Complete CSPv1 network reprogramming	orange
Record upset rates for CSPv1 flight boards	green	Complete functional tests of SHREC space middleware applications and suites	green
Record upset rate for μCSP	light green		
Upload and reconfigure at least one CSP device	orange	Perform integrated autonomous camera configuration based on observed conditions	orange
Upload and program at least one new parallel application	green		
Collect GaN PoL science products for at least 30 days during night cycles	green	Collect GaN PoL science products for entire mission lifetime for all experiments	green

2.5 years of operation

Due to effect on changing mission goals

Flash-based FPGA resilience

Due to effect on changing mission goals

Thermal limitations

Radiation-Effects Data

- **Ten Device Years Observed**
  - Single-event upsets (SEUs) due to radiation
  - L1/L2 caches of processors
  - Configuration and block memory of FPGAs
  - Some software bugs and logging issues
  - Results are representative, but not complete

- **Multi-Bit Upsets (MBUs)**
  - MBUs are interesting due to their ability to:
    - Overwhelm error-correction codes
    - Cause issues with triple-modular redundancy designs
  - Detect by timestamp and adjacent address, word, or bit

47 total SEUs observed

CSP#	L1	L2	CRAM	BRAM
0			12	
1	5	5	6	
2	8	8	8	
3	1	1	3	
4	1	1	2	1

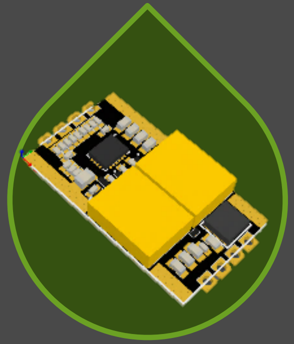
CSP	Timestamp	LFA	PFA	Word	Bit
0	1569779499	0000193E	00421318	7	3
		0000193F	00421319	7	3
0	1599816094	00000770	00001B1C	78	4
		00000771	00001B1D	78	3
0	1613692326	000012EA	0040209C	86	9
		000012EA	0040209C	86	10
1	1595498931	0000141E	00420012	87	4
		0000141F	00420013	87	3
2	1596177465	000005A6	000014A0	82	23
		000005A7	000014A1	82	24
2	1599201045	000017F6	00420E86	35	14
		000017F9	00420E89	35	12
		000017FA	00420E8A	35	13
		000017FB	00420E8B	35	12
2	1601314869	00000424	00000F1C	8	10
		00000424	00000F1C	8	11

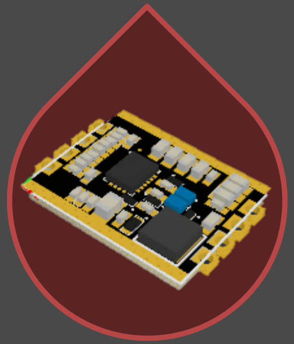
7 MBUs, including a 4-bit

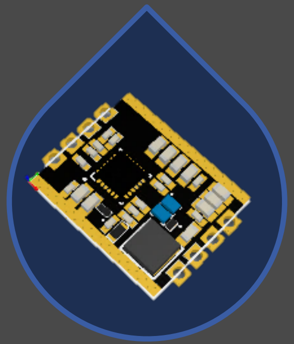
GaN PoL Converter Testing

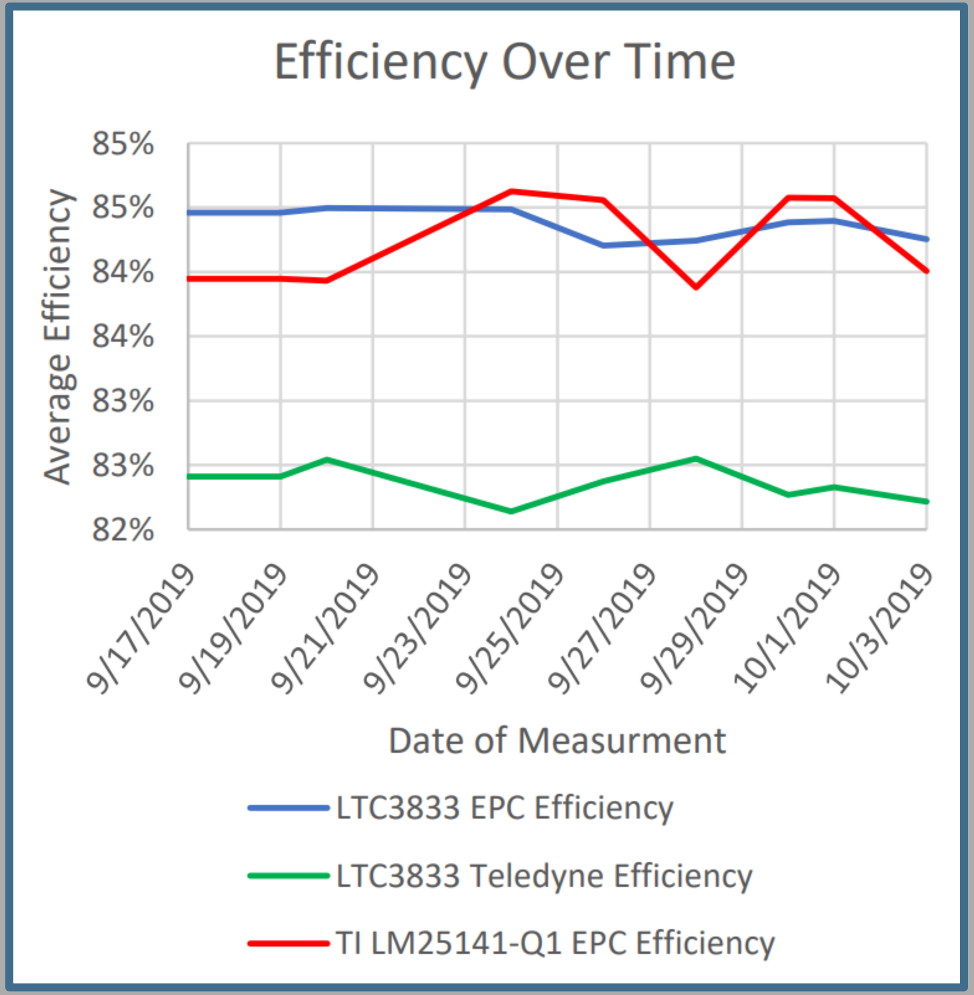
- **Benefits of GaN PoL Converters**
  - Inherent radiation tolerance
  - Low switching and conduction losses
  - Smaller supporting component packages

- **Critical Results**
  - Demonstrated long-term function in low-Earth orbit
  - Up to 85% efficiency for devices tested



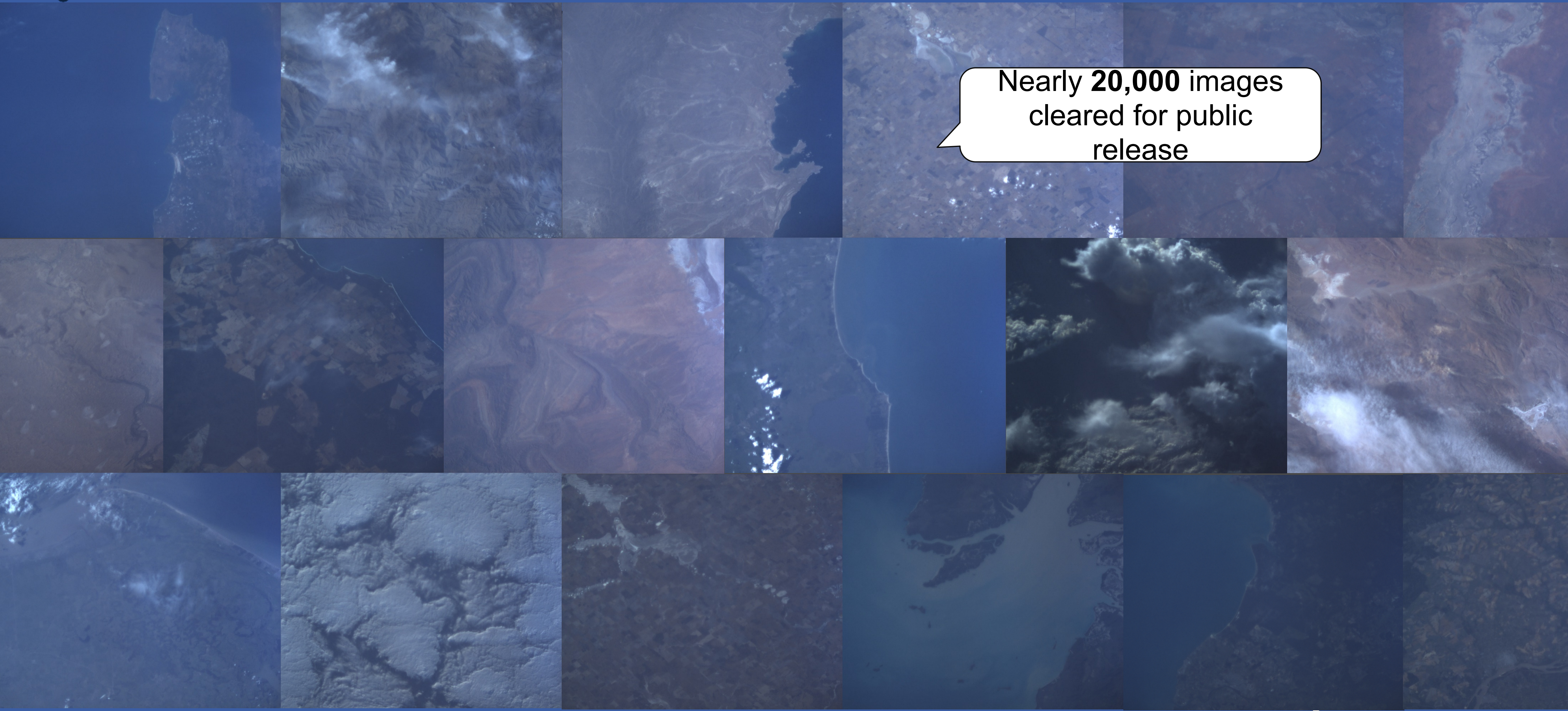






T. Cook, A. Phillips, C. Siak, A. D. George and B. M. Grainger, "Evaluation of Point of Load Converters for Space Computational Loads," 2020 IEEE Aerospace Conference, 2020, pp. 1-12, doi: 10.1109/AERO47225.2020.9172360.

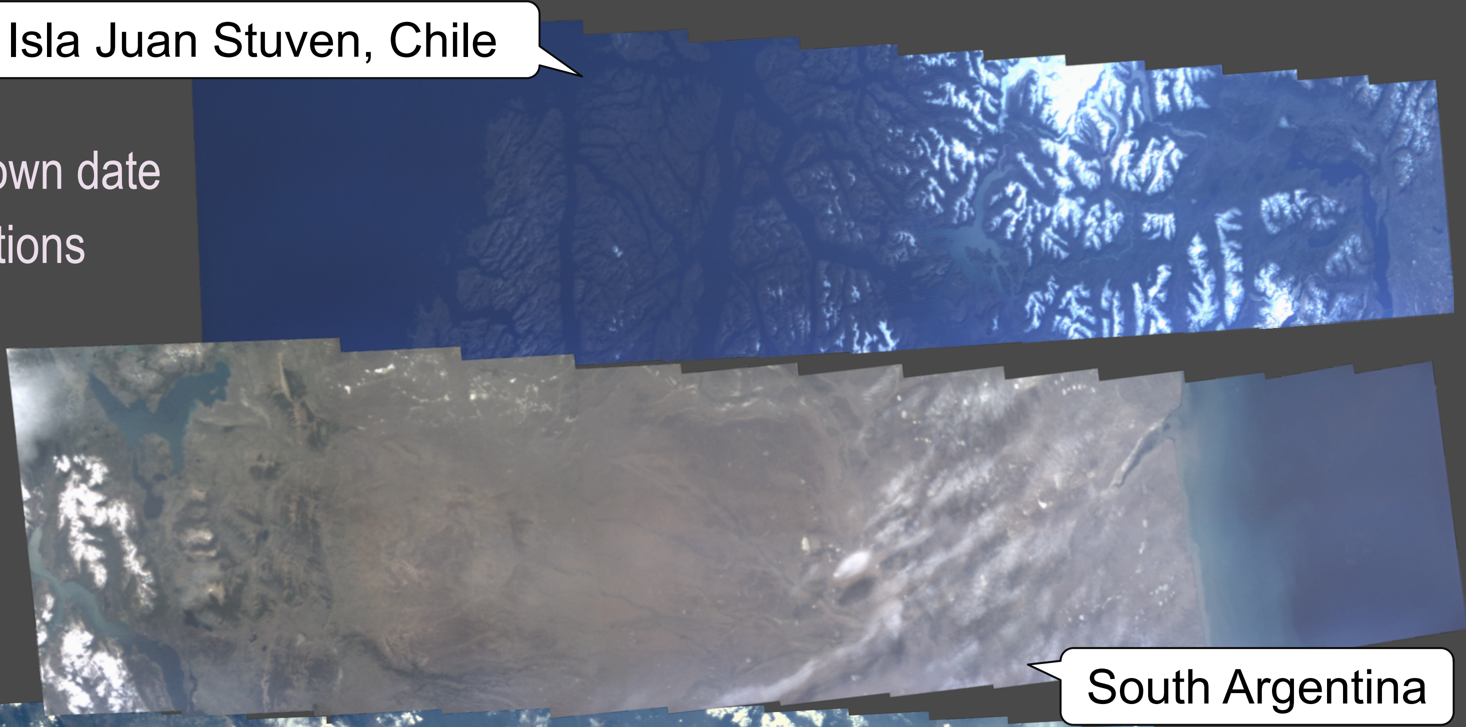
Earth-Observation Imagery

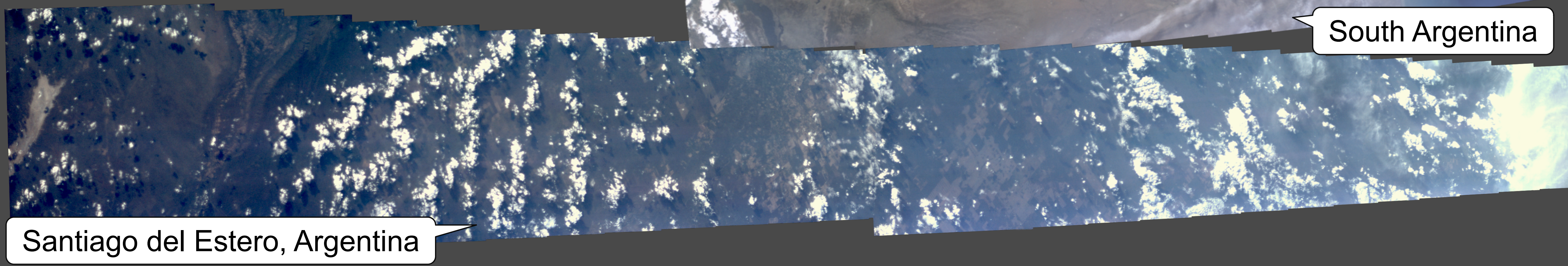


STP-H6 SSIVP was integrated and flown by the DoD Space Test Program.
Images are courtesy of the DoD Space Test Program.

Image Bursts

- **Improved Frame Grabber**
  - Integrated and tested on the ground
  - Upload could not be completed before shutdown date
  - Adapted on-orbit capabilities to suit new functions
- **Successful Image Bursts**
  - Up to 31 frames per burst
  - Combined on the ground
  - Up to 22k-pixel swath





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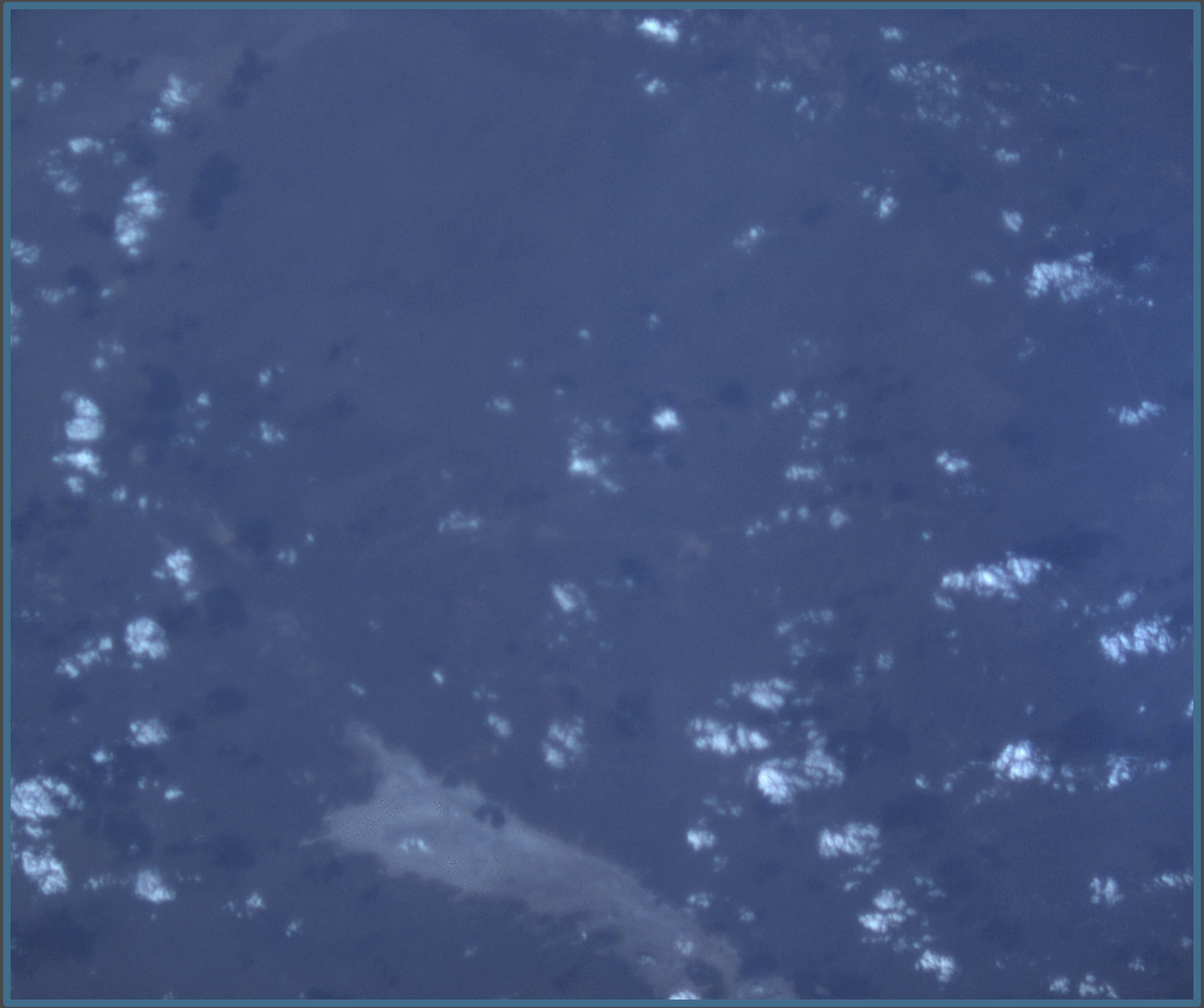
Burst as Video



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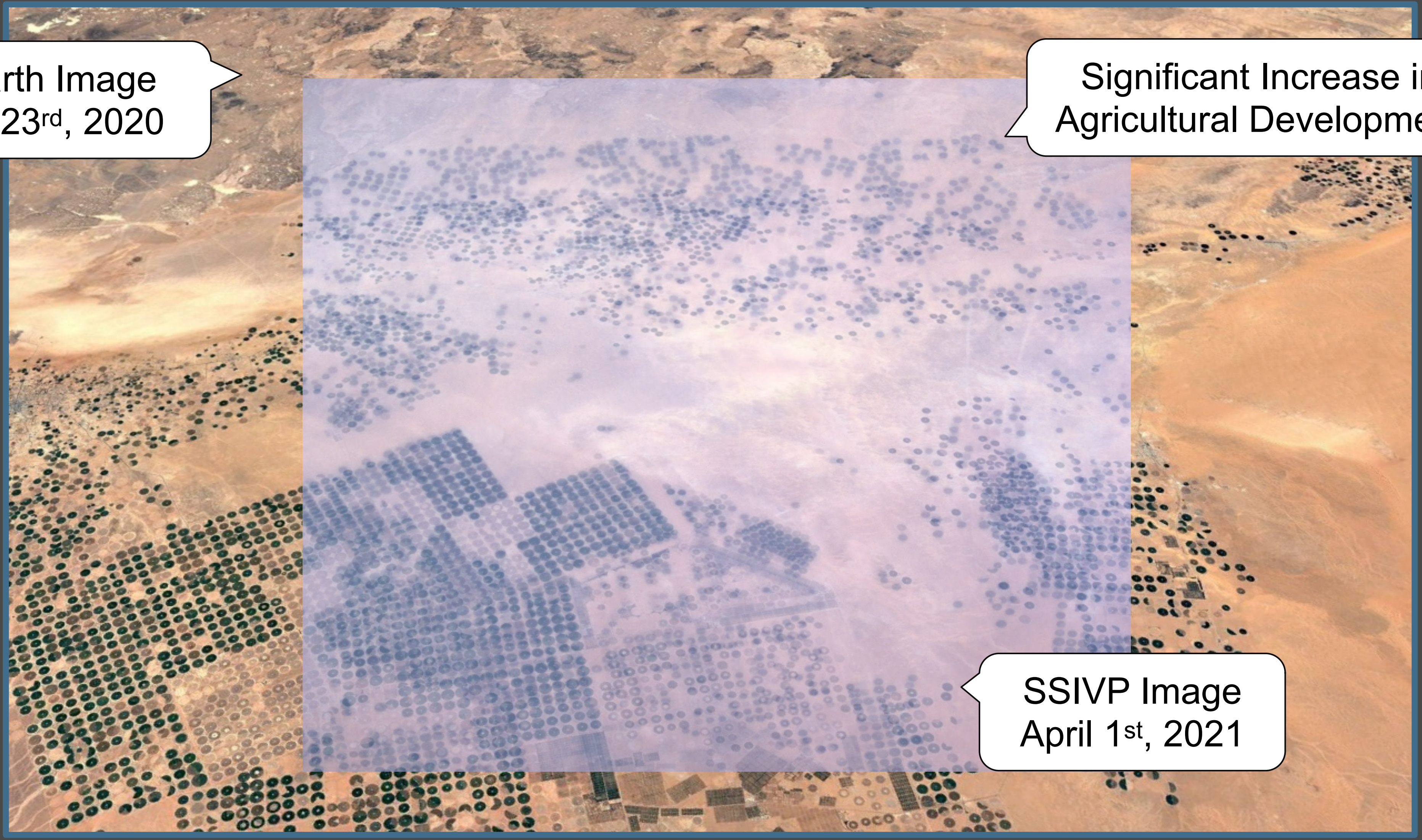
Temporal Change



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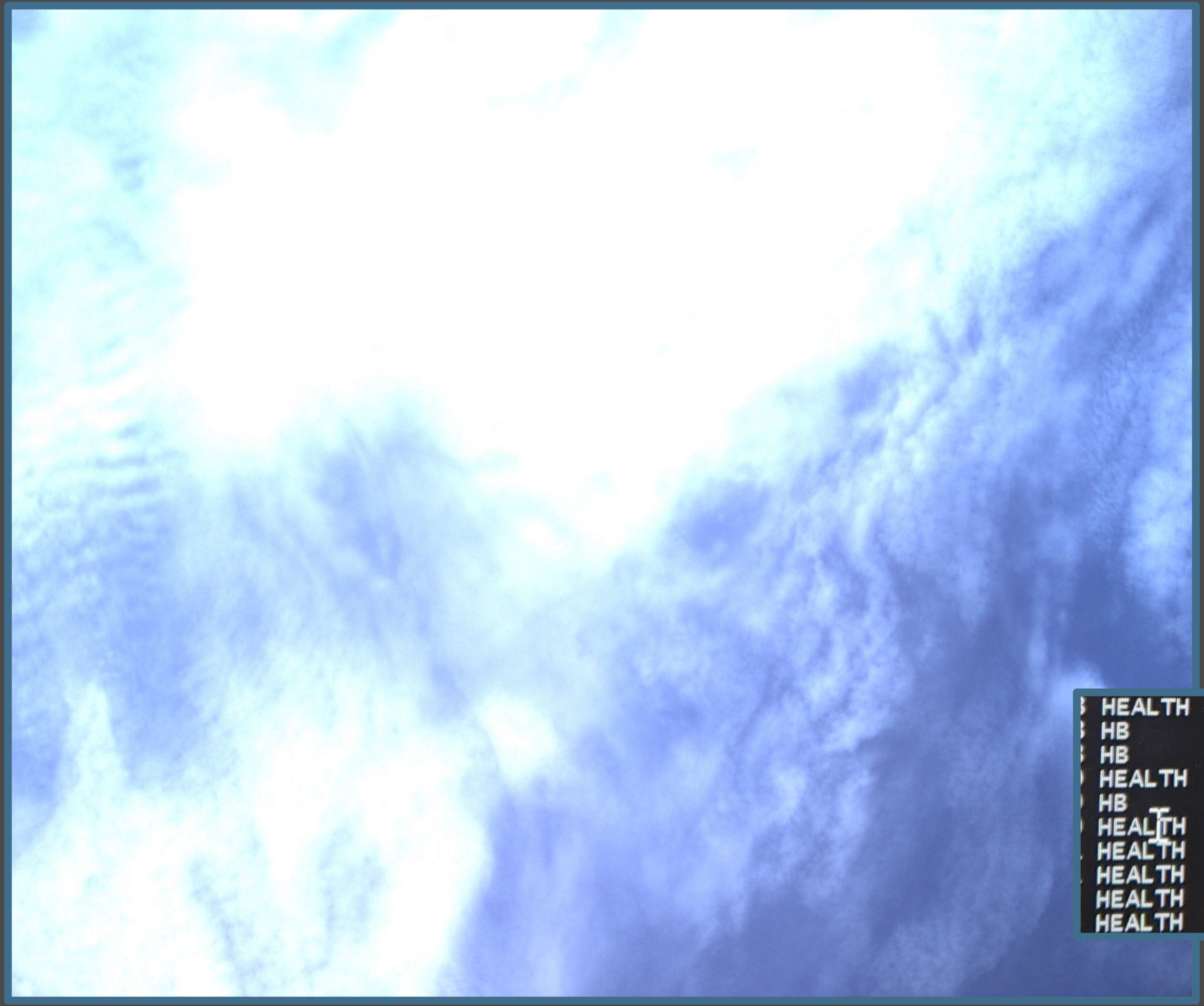
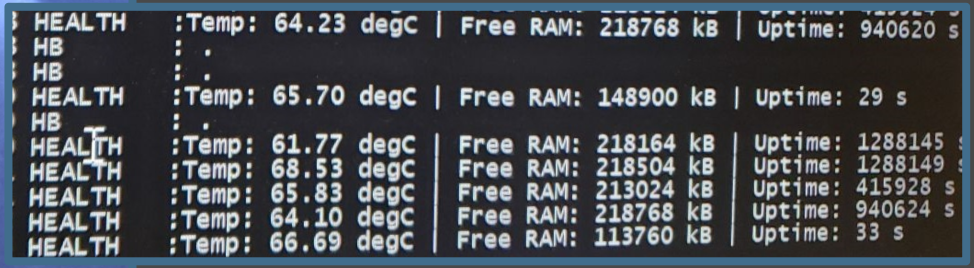
Last Transmission





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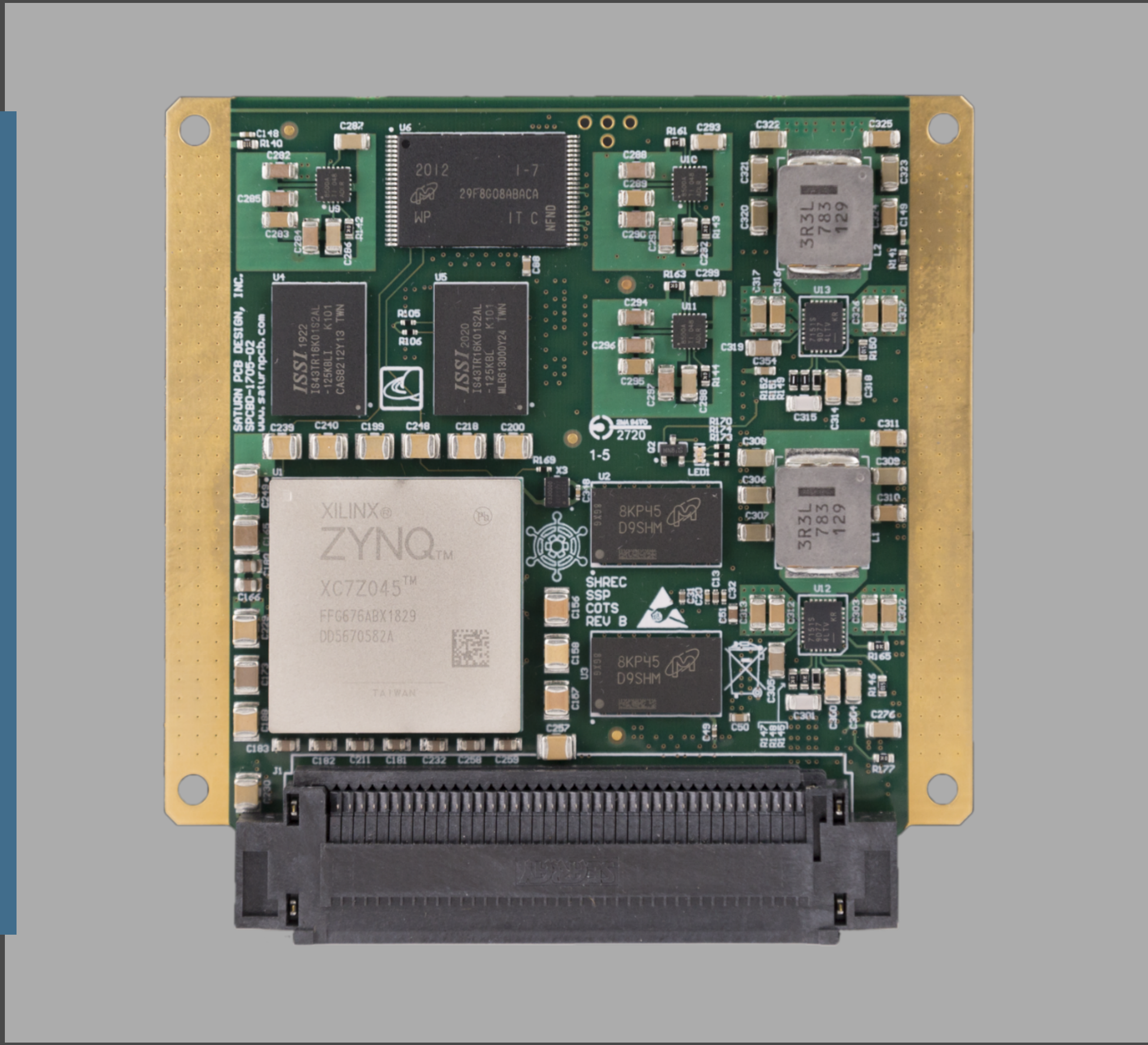
Deorbit

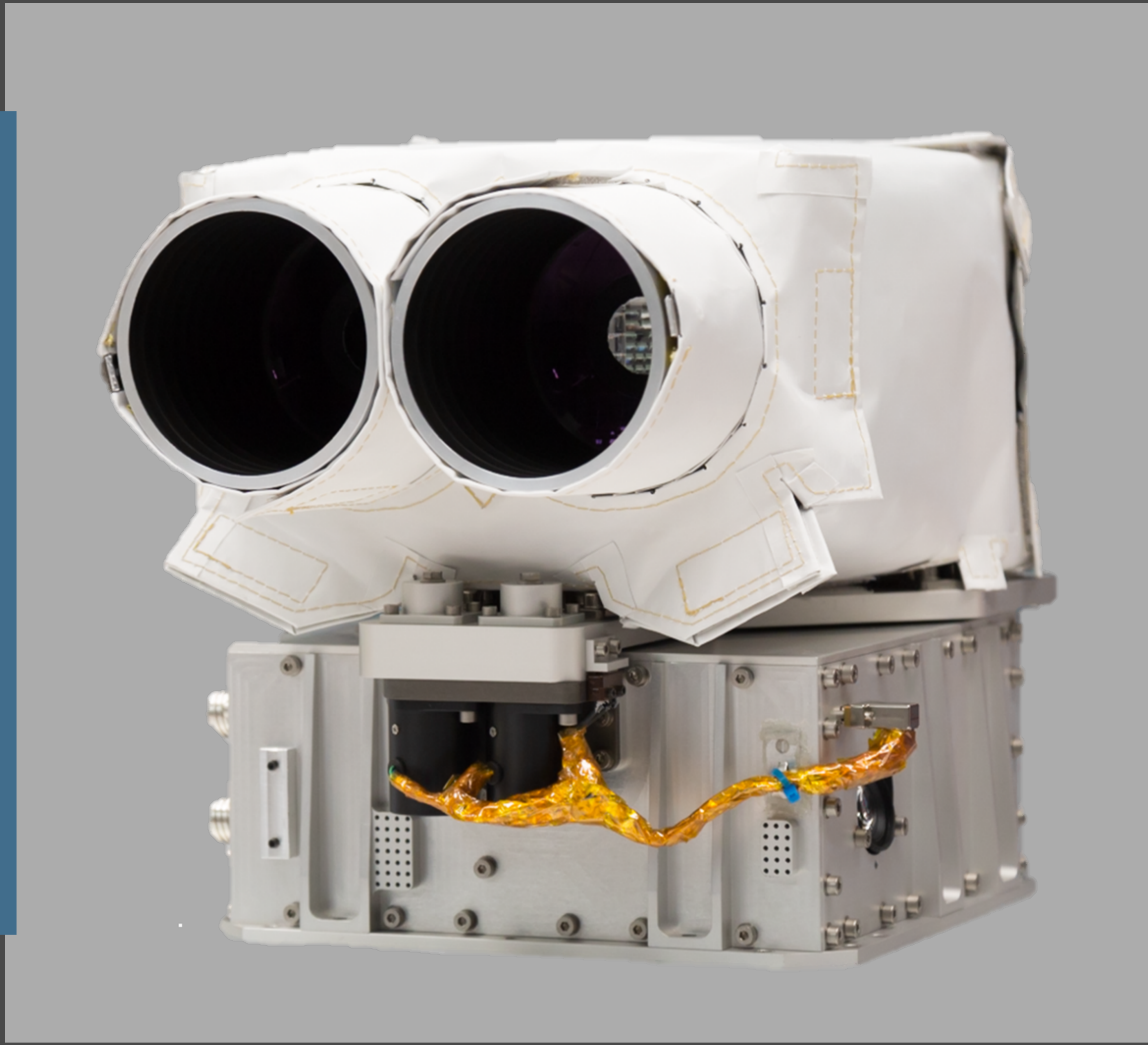
SHREC Space Processor

- **SHREC Space Processor**
  - Rev. A launched in December 2021
  - Rev. B completed in early 2022
- **SSP Expands CSP Capabilities**
  - 4-5× larger FPGA fabric
  - Dedicated memory for FPGA accelerators
  - Multi-gigabit transceivers for rapid I/O



STP-H7-CASPR

- **Configurable and Autonomous Sensor Processing Research**
  - Launched in December 2021
  - Operating nominally aboard the ISS
- **Incorporates SSIVP Lessons**
  - CSP Rev. C and µCSP
  - Dual Networked SSPs
    - Larger partial-reconfiguration region
    - More versatile accelerator integration
    - Faster parallel computing capability
  - Improved radiation-effects tracking
  - Updated frame grabber and burst capability



See **caspr.space** for more info!

Conclusions

- **Definitive Mission Success**
  - Collected data over 2.5 years of operation
  - TRL rise of CSP Rev. C and μCSP Smart Module
  - Captured over 20,000 images
  - Successfully deployed parallel apps onboard
  - Successful operation of GaN PoL converters

- **SSIVP has Contributed to:**
  - 12 research publications
  - 3 Masters theses
  - 6 PhD disseratations

More Information?

- **Dr. Alan D. George (PI), Department Chair, R&H Mickle Endowed Chair, Professor of ECE, and NSF SHREC Center Director**

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    1238D Benedum Hall, 3700 O'Hara Street Pittsburgh, PA 15261 412-624-9664
    Email: alan.george@nsf-shrec.org

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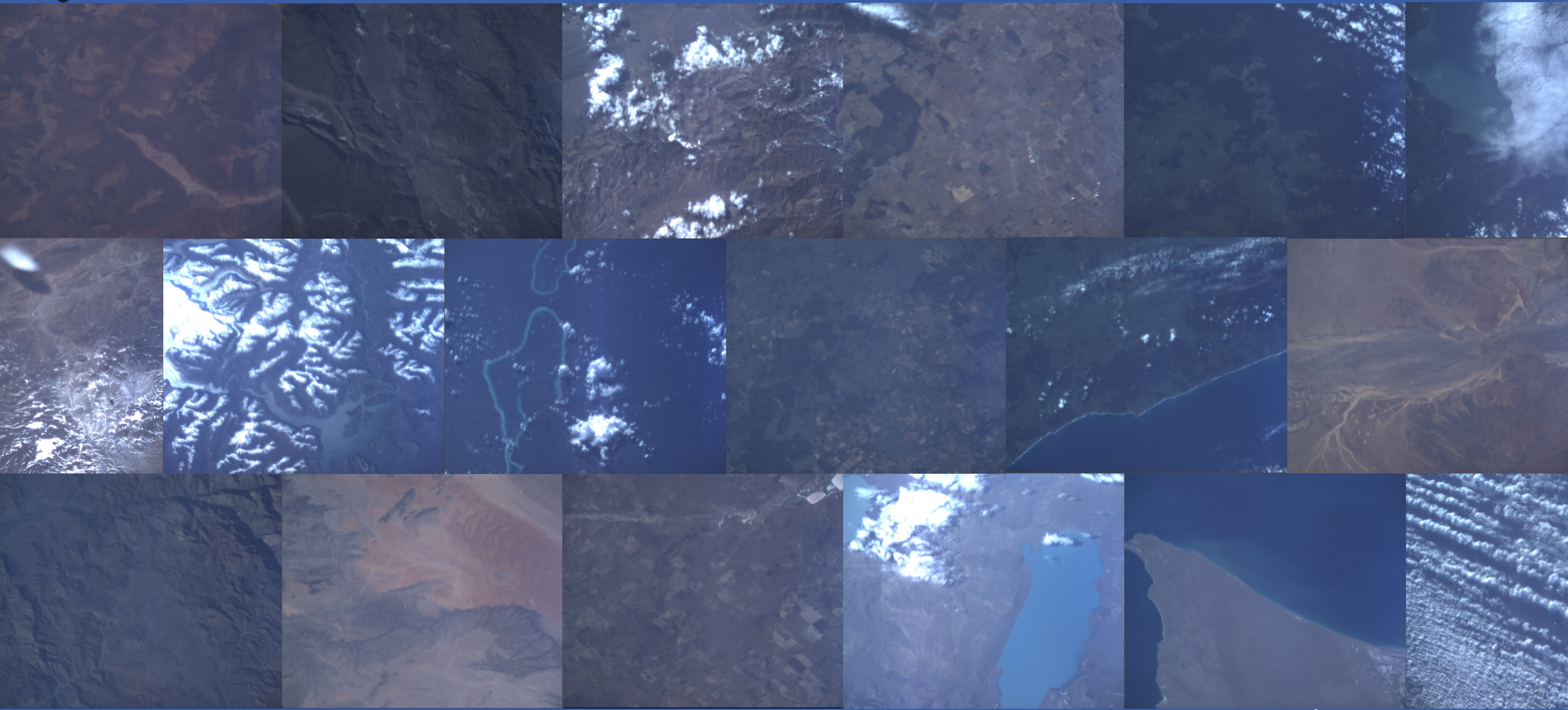
- **Seth Roffé, CASPR Experiment Manager**

  - Email: seth.roffe@nsf-shrec.org

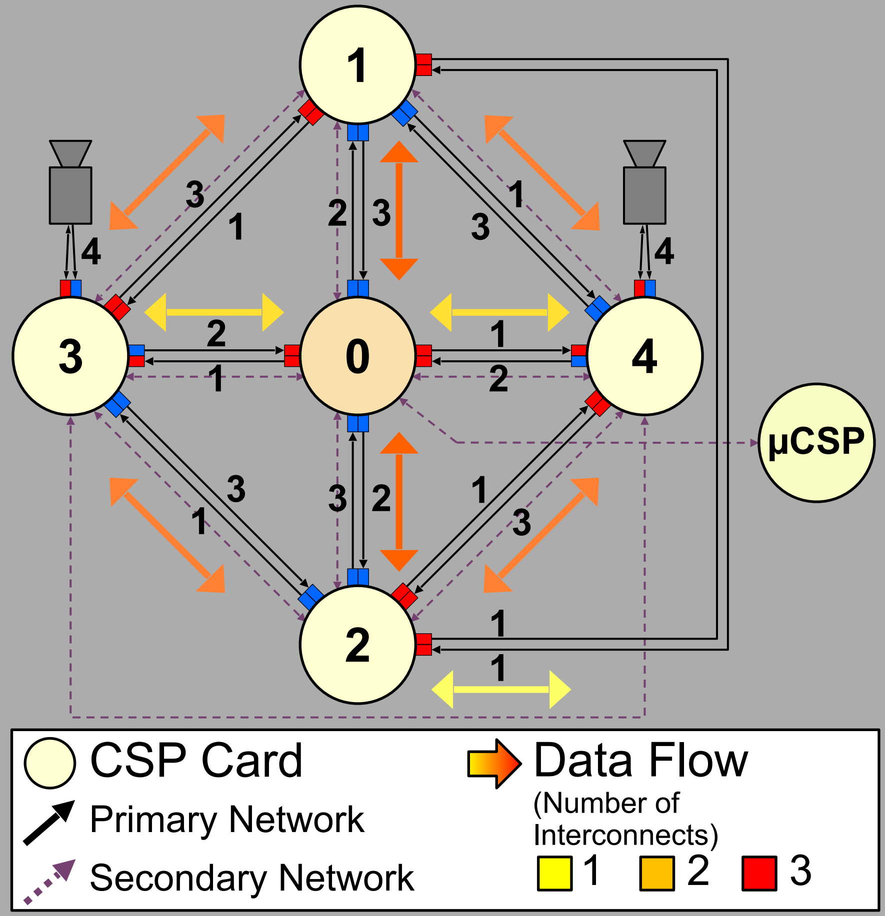
Thank You Very Much! Any Questions?



Backup Slides

SSIVP Network

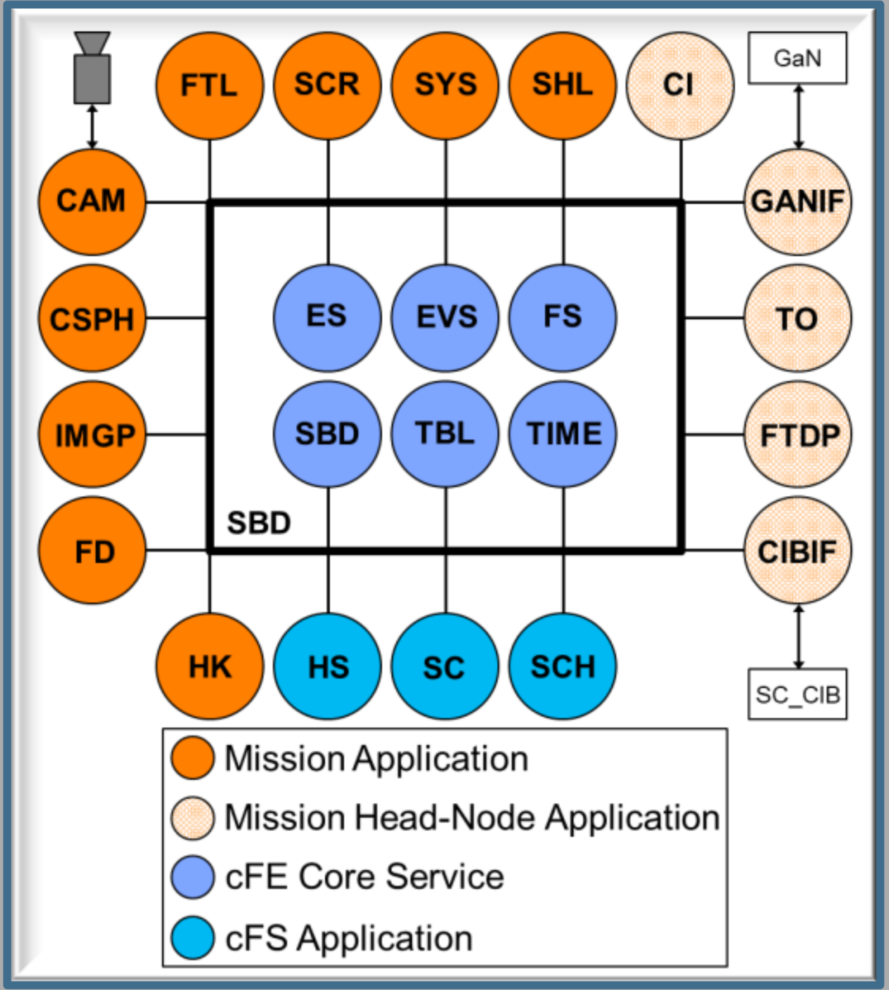
- **SaboLink High-Bandwidth Interconnects**
  - High-speed SerDes differential signaling
  - Resides in FPGA – entirely reconfigurable
- **Optimized Asymmetric Bandwidth**
  - Designed for scatter-gather operations
  - Camera nodes have more transmission lanes
  - Central node has more reception lanes
- **Secondary Network**
  - Resilient node communication if primary fails
  - Low-bandwidth communication and control



SSIVP Software

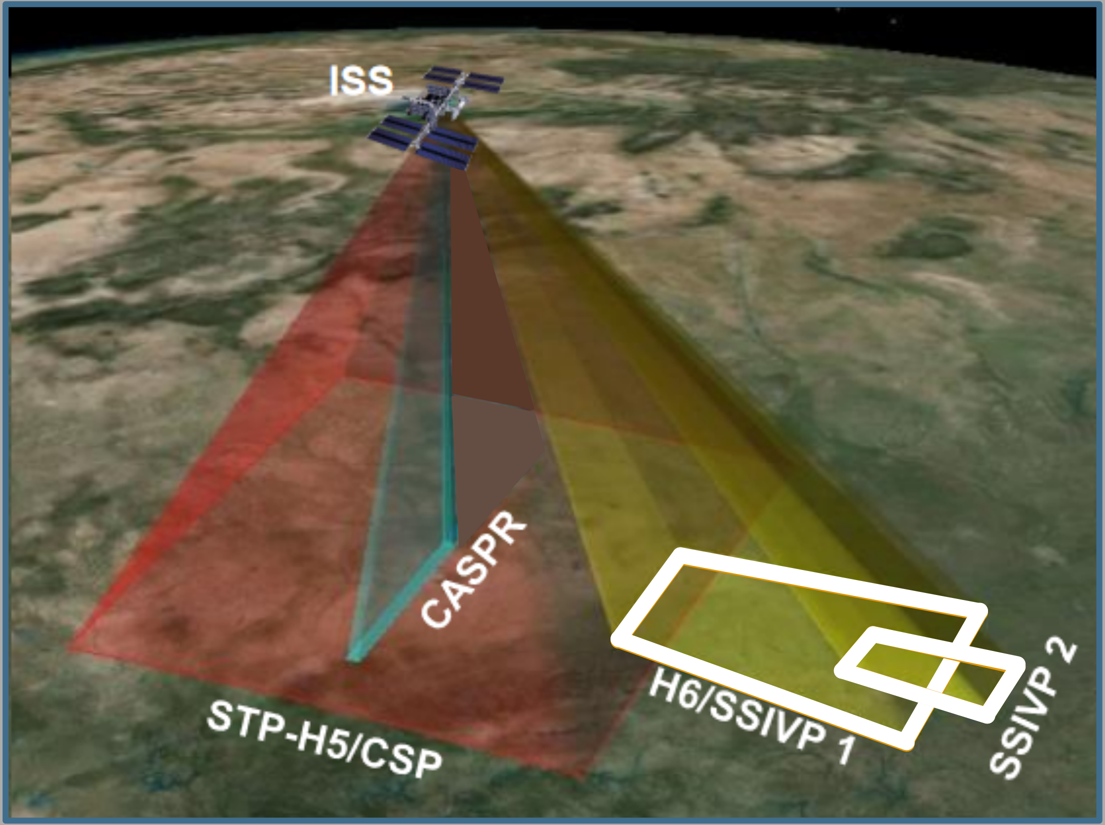
- **NASA Core Flight System (cFS)**
  - NASA Goddard's reusable flight-software framework
  - Core Flight Executive services
  - Select cFS apps for mission-critical services
    - Health and status, telemetry
    - File transfer, file downlink, automated downlink

- **"Wumbo" Linux**
  - Lightweight, custom operating system
  - Based on Xilinx Linux kernel fork and BusyBox
  - Variety of Linux shell apps and tools
  - Tremendous versatility



Imaging Capabilities

- **Wide Field of View**
  - Wide 22.5° × 19.7° viewing angle
  - Angled 35° toward ram from nadir
  - Approximately 167 m GSD and 334 m GRD
- **Narrow Field of View**
  - Narrow 7.6° × 6.6° viewing angle
  - Angled 45° toward ram from nadir
  - Approximately 30 m GSD and 60 m GRD
- **5.0 MP 2448×2050 Pixel Frames**



Imaging Totals

STP-H6-SSIVP Image Batch Details				
Batch #	Window Details			Images
	Start	End	Length (Days)	
0	3/4/2020	3/23/2020	19	1495
1	5/5/2020	5/14/2020	9	
2	5/20/2020	5/28/2020	8	
3	7/2/2020	7/25/2020	23	1266
4	9/9/2020	9/30/2020	21	1154
5	11/11/2020	11/13/2020	2	168
6	1/6/2021	1/11/2021	5	302
7	1/12/2021	1/19/2021	7	107
8	1/19/2021	1/28/2021	9	980
9	2/26/2021	2/28/2021	2	156
10	3/17/2021	4/1/2021	15	1783
11	4/28/2021	5/14/2021	16	1953
12	5/20/2021	5/24/2021	4	891
13	6/29/2021	7/11/2021	12	1302
14	7/21/2021	7/24/2021	3	179
15	7/30/2021	8/12/2021	13	720
16	8/21/2021	8/25/2021	4	105
17	10/21/2021	11/17/2021	27	7247
Bursts	11/8/2021	11/12/2021	4	260
				20068