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**Especialidad en Diseño de Sistemas en Chip**



## **Implementing a TSPC D Flip Flop as an Arbiter for a low power 10- bits 200kS/s ADC with Adaptive Conversion Cycle for High-Quality Audio Applications in 0.18um TSMC CMOS Technology**

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**TRABAJO RECEPCIONAL** que para obtener el **GRADO** de  
**ESPECIALISTA EN DISEÑO DE SISTEMAS EN CHIP**

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ITESO – The Jesuit University of Guadalajara

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SPECIALIZATION PROGRAM IN SOC DESIGN



**Implementing a TSPC D Flip Flop as an Arbiter for a low power 10-bits  
200kS/s ADC with Adaptive Conversion Cycle for High-Quality Audio  
Applications in 0.18um TSMC CMOS Technology**

Thesis/Project to achieve the university degree of  
SOC DESIGN SPECIALIST

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# Abstract

This document presents the design of an arbiter circuit for a time-based SAR-ADC. The arbiter is a TSPC D flip flop. It was designed in TSMC 0.18  $\mu\text{m}$  CMOS technology with 1.8 V supply voltage. It was tested at a clock frequency of 200 KHz, but it can operate even at 100 MHz. Simulation results using the typical process parameters shown a setup time of 5.02 ps and Hold time of 51.72 ps, the TSPC D flip flop power consumption is 62.61  $\mu\text{W}$ @200 KHz, and the layout area is 368.284  $\mu\text{m}^2$ .

The simulation is performed across all PVT corners that vary from a temperature of  $-40\text{ }^\circ\text{C}$  up to  $125\text{ }^\circ\text{C}$ , with a supply voltage variation from 1.62 V up to 1.98 V and the TSPC D flip flop functionality is correct.

# Introduction

An ADC is a circuit that converts a continuous analog input voltage to a discrete binary word. ADCs are high in demand due to the increase of numerous mixed-signals systems. There are several conversion techniques in which analog-to-digital conversion can be done such as pipeline, delta-sigma, and flash. Nevertheless, Successive-Approximation technique is one of the most popular because of its accuracy, moderate conversion speed as well as low power consumption [1]. It is generally a feedback system that applies a trial-and-error algorithm to obtain a proportional digital word to an analog input voltage.

## The SAR ADC

A SAR-ADC (Fig. 1) consists of the following design blocks:

- i. Sample and Hold circuit
- ii. Compararator
- iii. N-bit SAR logic
- iv. Digital-to-Analog Converter (DAC)

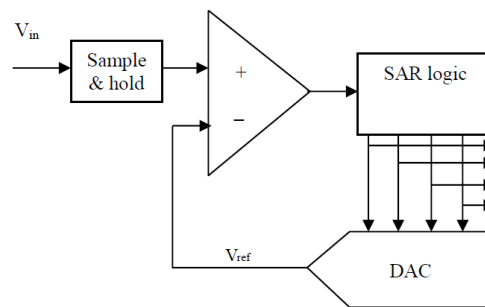


Fig. 1. Block Diagram of a Typical SAR-ADC

The conversion sequence of a SAR-ADC is listed below:

- i. The system samples the analog input  $V_{in}$  in a sample and hold circuit. Simultaneously, the SAR Logic resets the DAC.
- ii. The MSB bit is set in the DAC by the SAR logic. The DAC output is known as Voltage Reference ( $V_{ref}$ ).
- iii. The  $V_{in}$  sampled and  $V_{ref}$  are compared by the comparator circuit. If  $V_{in}$  is greater than  $V_{ref}$  the Comparator output is '1' logic, else the output is '0' logic.
- iv. The SAR logic saves the comparator output in the MSB position of the SAR output register and sets the bit MSB-1 and presents this partial conversion to the DAC input.
- v. The conversion continues for MSB-1, MSB-2, and finishes on the LSB bit.



# The Adaptive Conversion SAR-ADC Proposal

Our proposal is a modification of the conventional SAR-ADC algorithm (

Fig. 2) to perform a conversion in fewer clock cycles. This is possible by a prediction of the consecutive 1's or 0's in the conversion result. Such prediction is based on the difference between  $V_{in}$  and  $V_{ref}$  signals. Our proposal is capable of predict 1 bit or 3 to 9 consecutive equal bits on a single clock cycle.

The conversion sequence of the proposed system is listed below:

- i. The system samples the analog input  $V_{in}$  in a sample and hold circuit
- ii.  $V_{in}$  and  $V_{ref}$  are converted to a time-domain signal via the VTC
- iii. The time-amplifier (TA) extends the time difference between these two signals and distributes them to the arbiter and the counter.
- iv. The arbiter decides which signal came in the first place.
- v. The SAR Logic uses the information from the arbiter and the counter to predict equal-consecutive bits and to adapt the conversion cycles

This will improve overall conversion time and power dissipation per conversion.

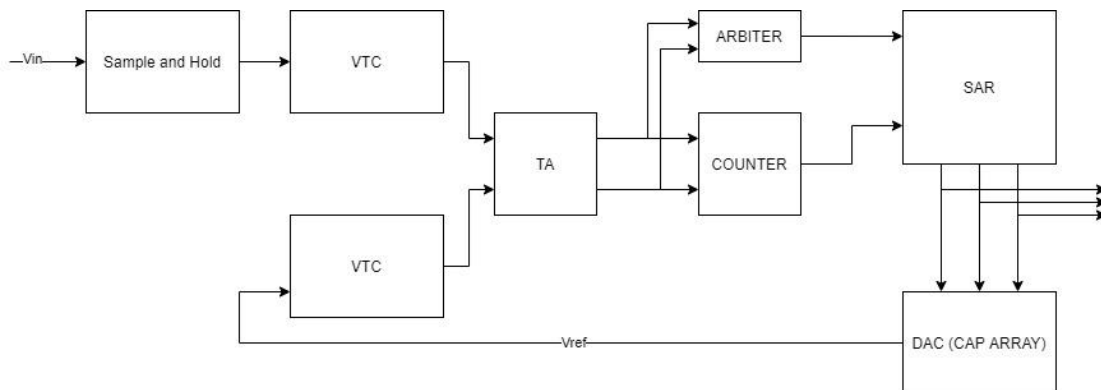


Fig. 2. SAR-ADC Proposal

# 1. The Arbiter circuit

In this document, an arbiter is a circuit that detects which signal in time domain came first. In this project, we have chosen a D flip flop (D-FF) with a TSPC topology.

There are asynchronous circuits and synchronous circuits, the main difference is that in asynchronous circuits there are no clock signals, and the circuit output changes as soon as the input changes. In a synchronous circuit, only the output can change when there is a change in the clock.

A D flip flop follows the input D doing a transfer to the output Q, this is performed in the positive edge of the signal clock. It can be considered a basic cell of a bit memory.

The symbol of a basic D flip flop (D-FF) is shown in Fig. 3

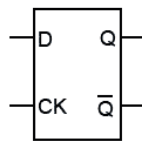


Fig. 3. Symbol of a D flip flop

The timing diagram in Fig. 4 illustrates that input data D is transferred to Q output only when the clock is at the positive edge, and during the rest of the clock cycle, Q remembers the previous state of the Q. Table. 2 summarizes the operating principle of the D-FF circuit. Notice when the clock is low, any change to the D input makes no difference to the output, in the Table. 2 it is marked as don't care 'X' state.

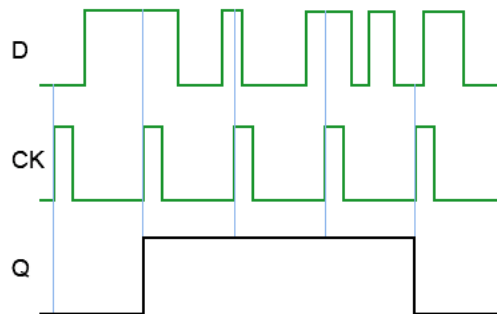


Fig. 4. A timing diagram for a D flip flop

Inputs		Outputs	
Clock	D	Q	/Q
X	X	No change	
↑	0	0	1
↑	1	1	0

Table. 1. Trued table

As shown in

Fig. 2 the two outputs of the TA (Time Amplifier) go to ARBITER circuit, consequently, a decision is taken to determine what signal pass first. The criterion considered for the SAR-ADC project is if  $D > CLK$ , Q should be a logic 1, and if  $CLK > D$ , Q should be a logic 0. As seen in

Fig. 2 the Q, from the TSPC D-FF (Arbiter) module output enters the SAR Logic module input.

In the present project, we need a flip flop having very short setup time, this is the reason why we have chosen a True Single Phase Clock D flip flop (TSPC D-FF) topology. It is known that one of the issues in a traditional flip flop is the complex clock distribution circuits. The larger the circuit, the larger the interconnects and long interconnects cause slow transitions but also skew, jitter, or another problem, making it difficult to distribute multiple, clock phases. The TSPC D-FF architecture promises surmount these issues.

## 1.1. TSPC D-FF architecture

The TSPC D-FF is a flip flop whose concept was developed in the 1980s [3]. It uses a dynamic logic and its features are mainly high speeds, low power, and area saving. It depends on a clock to work correctly. It can be a positive or negative clock edge, this means that the input (D) is transferred to the output (Q) only during the positive or negative clock edge. For this project, we use a positive clock edge flip flop.

Fig. 5 shows the schematic diagram of the TSPC D-FF proposed in [2]. We have started the study on this initial implementation.

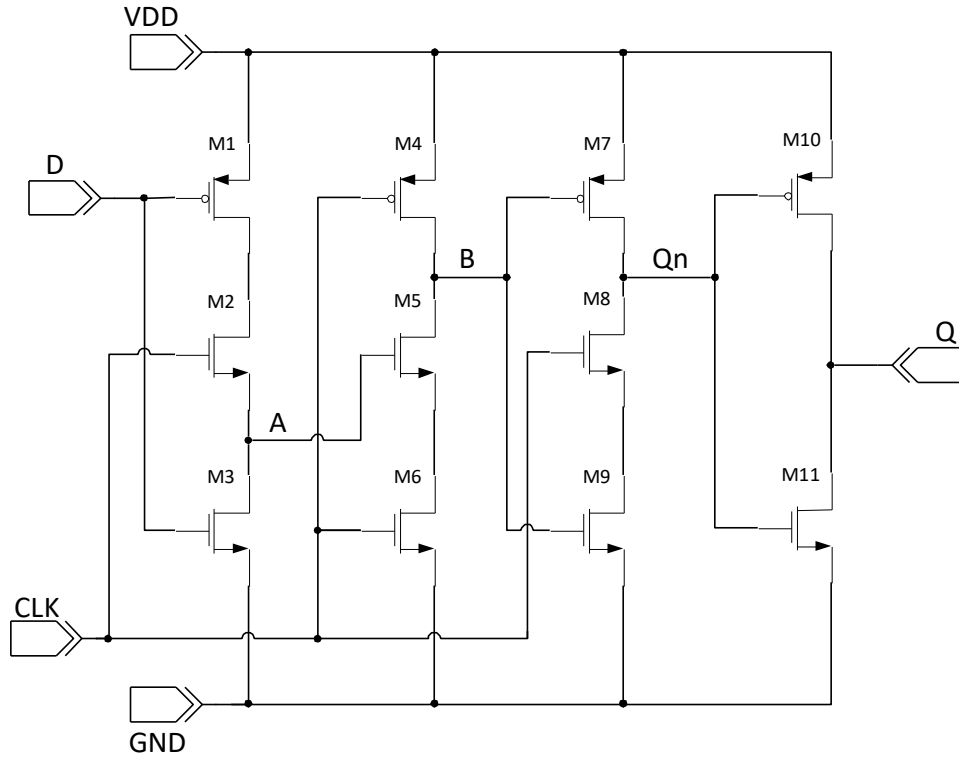


Fig. 5. Schematic of the TSPC D-FF proposed in [2].

Table. 2. shows the truth table for a TSPC D-FF.

D	CLK	Q
0	↑	0
1	↑	1
X	X	Q <sub>0</sub>

Table. 2. TSPC D-FF truth table

The characterization results of the TSPC D-FF architecture of Fig. 5, have shown an unexpected behavior, notice for instance in Fig. 6 that the output Q follows the input D during the positive edge of the clock and goes to logic low when the D input goes low. The expected response of the TSPC D-FF is that Q output must follow the D input only during the positive edge of the clock and must wait to the next positive edge of the clock to capture a new value of D input and must apply that logic level to the Q output.

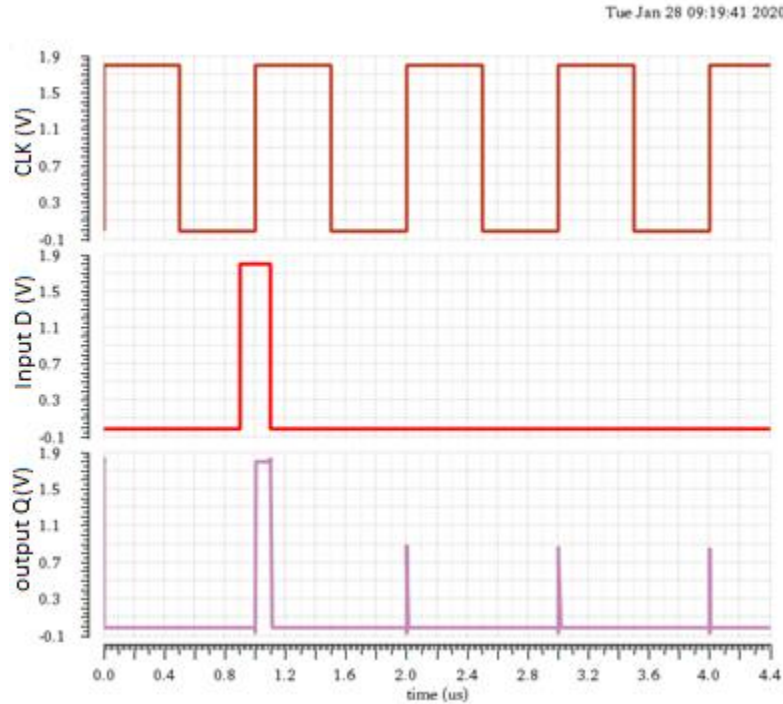


Fig. 6. Original schematic with unwanted behavior for the TSPC D-FF

To correct the unwanted behavior of the initial proposed TSPC D-FF, we changed the type of transistor M2, it was substituted by a PMOS type transistor. The modified architecture of the TSPC D-FF is shown in Fig. 7.

We performed a transient simulation in order to validate the expected behavior of the modified topology. The results are presented in Fig. 8.

In the same Fig. 8 we can notice in the Q output some unwanted glitches near the 2.0 us, 3.0 us, and 4.0 us. This issue and its correction are later addressed in section 3.5.

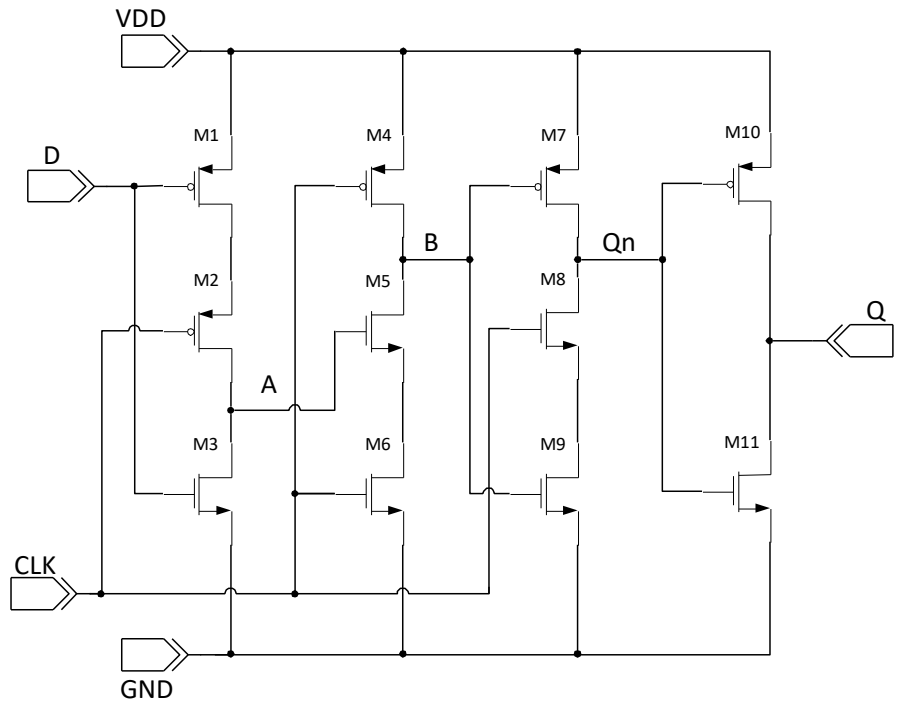


Fig. 7. TSPC D-FF implemented with M2 modification

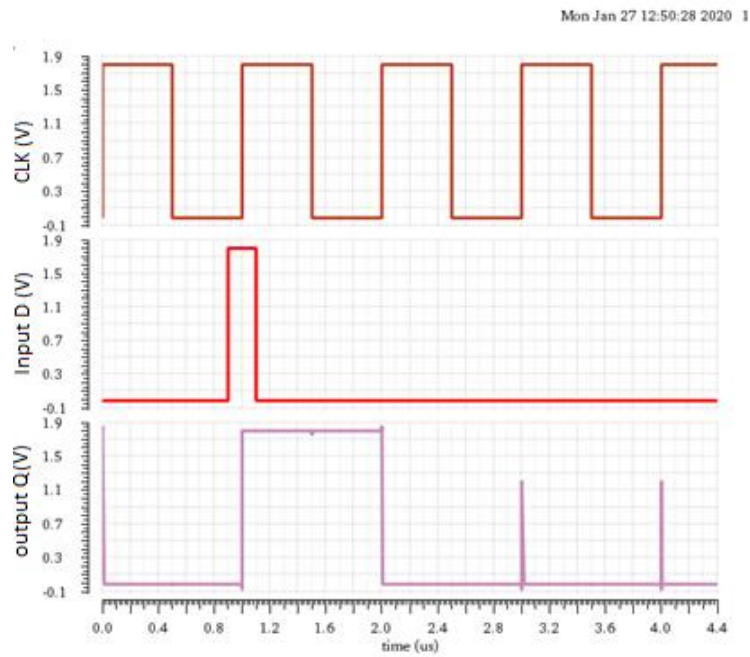


Fig. 8. The correct response of a TSPC D-FF

## 2.Design of the TSPC D-FF

Once a circuit has been defined, the next step is to calculate the W/L ratios of the TSPC D-FF circuit. These ratios are calculated to provide the gate with a current driving capability equal to the basic inverter.

It is very important to correctly size the transistors (W/L) in a circuit since this will allow a higher speed of operation and then having a shorter setup time

## 2.1. Pull-Up Network (PUN) and Pull-Down Network (PDN)

To correctly calculate the value of each MOSFET we first review the concept of Pull-Up Network (PUN) and Pull-Down Network (PDN) of logic circuits.

As seen in Fig. 9, the two networks PUN and PDN are complementary and they operate by the input variables (A, B, C), depending on the value of these inputs either PDN or PUN will conduct having in the output voltage (OUT) either VDD (logic 1) or GND (Logic 0).

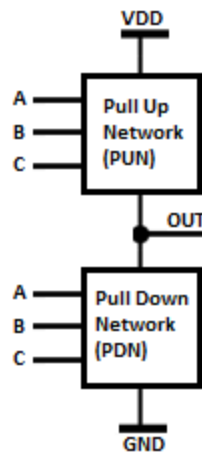


Fig. 9. Diagram of Pull-Up Network (PUN) and Pull-Down Network (PDN) [4]

## 2.2. Basic Inverter

In Fig. 10, we show a basic inverter schematic at the transistor level. As seen in this figure, this is a pair of complementary MOSFETs that act as switch activated by its input: if the input voltage is a logic 0, the output would be a logic 1, this is because the PMOS (M1) is turned on and VDD voltage is transferred at the output node. By contrast, if the input voltage is a logic 1, the output node would be a logic 0 since this time the NMOS (M2) is turned on and GND (0 V) is present at the output node [4].

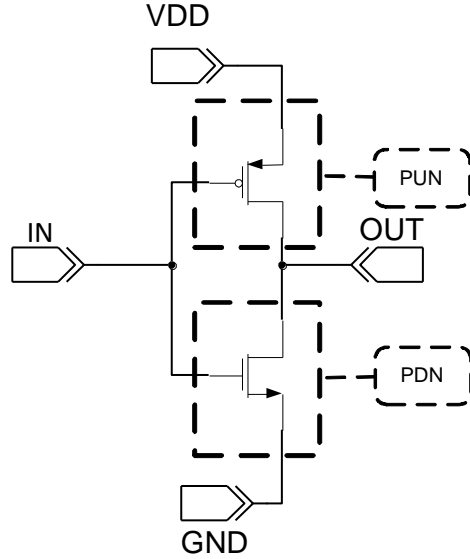


Fig. 10. Basic inverter showing the PUN and the PDN parts

### 2.3. Transistor sizing

To define the  $W$  and  $L$  transistor ratios in any logic gate we should consider that they are chosen to provide the current-driving capability equal to that of the basic inverter; in this sense, if we have an array of two transistors connected in series of either PUN or PDN sections, each  $W = 2W_{min}$ , if we have three transistors connected in series each  $W = 3W_{min}$ , and so on. By contrast, if we have an array of any transistors connected in parallel each  $W = W_{min}$  [4].

First, for the calculus of the  $W/L$  ratio of the inverter cell we use the relationship  $(W/L)_n/(W/L)_p = k_{pn}/k_{pp}$  where  $k_{pn,p}$  is the transistor transconductance which is a parameter of each CMOS technology. In the case of TSMC18 process  $k_{pn} = 260 \mu A/V^2$  and  $k_{pp} = 78 \mu A/V^2$  which results in  $(W/L)_n/(W/L)_p \approx 3$ . The length for all transistors in the TSPC circuit is  $L_{min} = 0.18$  then, the width  $W_n$  is given by (1):

$$W_{n\ min} = L_{min} * 3 = 0.18 * 3 = 0.54 \quad (1)$$

Then we apply the 3:1 ratio between the PUN and the PDN sections, to calculate  $W_p$ , that is,

$$W_p = 3W_n = 1.62 \quad (2)$$

Fig. 11, shows the inverter cell schematic with transistor sizes.



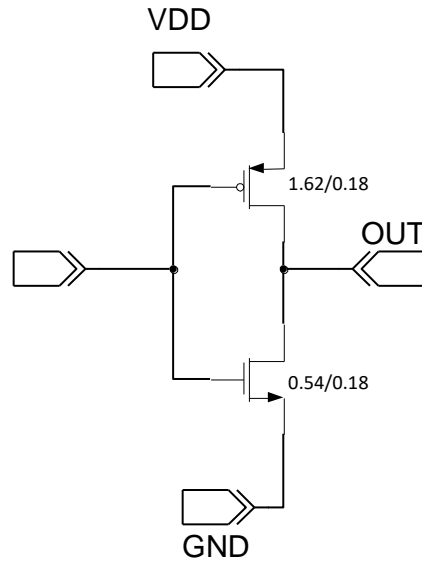


Fig. 11. Basic Inverter with W/L values for PDN and PUN.

We extend this sizing procedure for calculating the rest of the W/L ratios of the TSPC D-FF circuit (Fig. 12). As an illustrative example, notice, for instance, transistor M1 and M2 which are connected in series, their W/L are assigned twice the W/L of a PMOS transistor in the inverter cell, while M4, M7, and M10 which are connected in parallel, keep the same W/L as the PMOS in the inverter cell in Fig. 11.

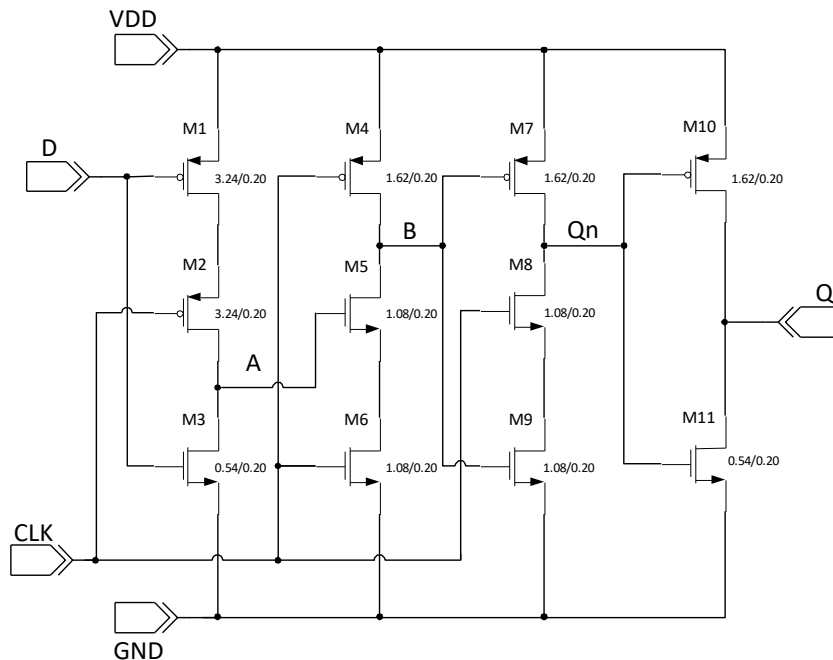


Fig. 12. TSPC D-FF with transistor sizes

## 2.4. Pre-layout Simulation Results

In Fig. 13, we present the transient response of the TSPC D-FF circuit. As it is expected, Q output is at logic 1 state when D and CLK inputs are in 1 logic state and it is at logic 0 state after next positive edge of CLK and D being 0 logic. We also can notice some glitches when Q is at 0 logic state. These glitches appear at the positive edge of the CLK signal. It is known that glitches are unwanted signals that can affect the behavior of other modules that interact with D-FF.

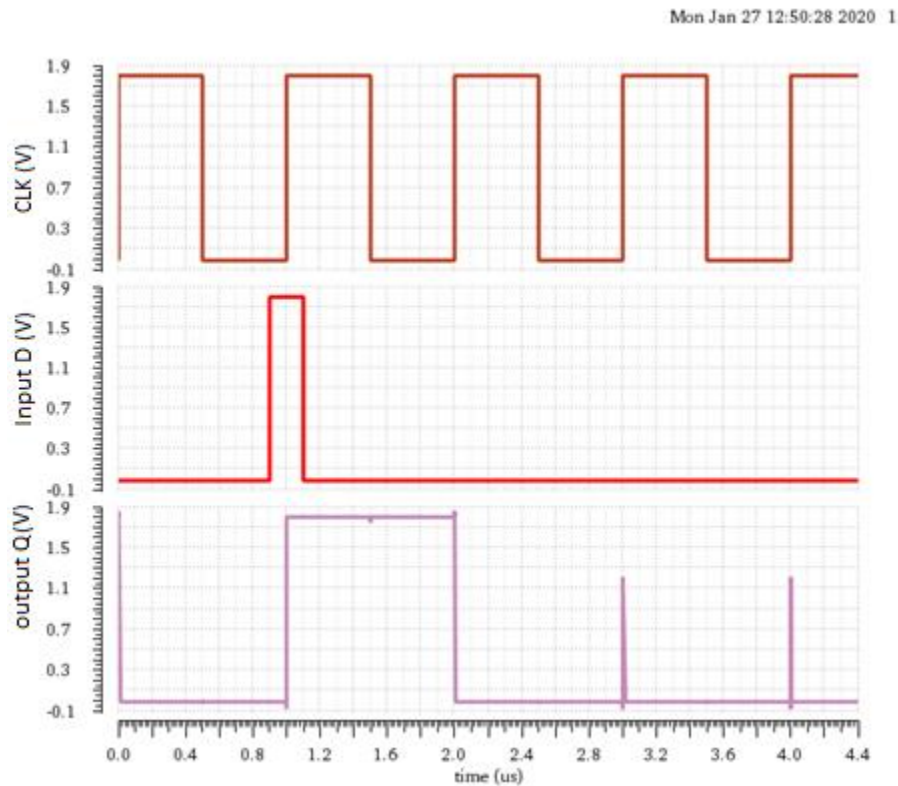


Fig. 13. Transient response of schematic of Fig. 12 showing glitches in the Q output signal

## 2.5. Glitches Elimination

To avoid the glitches in the output of D- FF, we have added an extra PMOS between M4 and M5 in Fig. 12. The selected size now must change in M4, since now there are two transistors in series it must be double the size. This PMOS is needed since when input D is low with respect to CLK node B experiences a continuous toggling. This behavior not only consumes more power but it is also a source of noise on the output Q. The modified circuit is shown in Fig. 14.

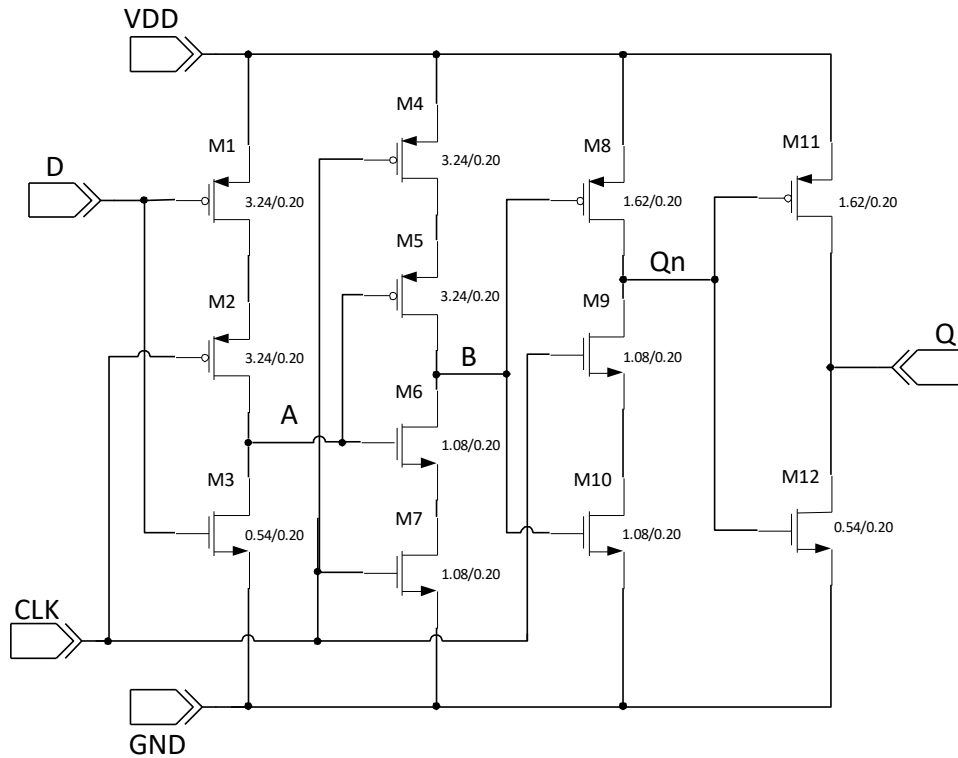


Fig. 14. TSPC D-FF with M5 to cancel glitches

In Fig. 15, the transient response of TSPC D-FF of Fig. 14 is shown. By comparing this response with the one presented in Fig. 13, we can note that the glitches are gone. This is the desired response of the TSPC D-FF circuit.

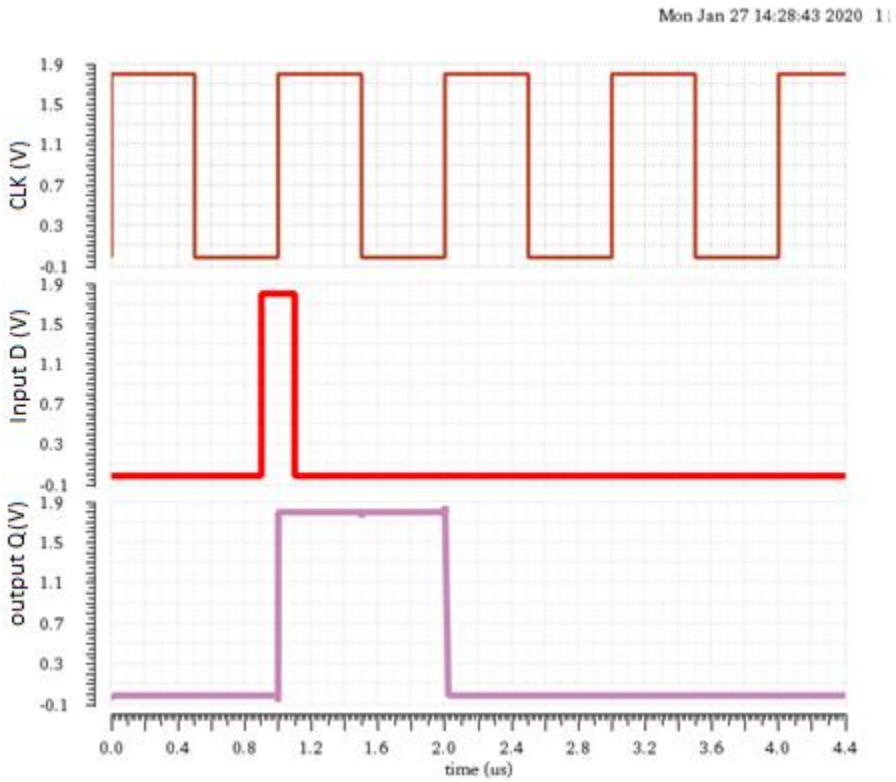


Fig. 15. Transient response of the TSPC D-FF with suppressed glitches

## 2.6. Reset Input

We initially did not plan to add a reset functionality to the TSPC D-FF, but we noticed some unwanted behavior on the first instants of transient response (see the blue box in Fig. 16) the Q output before having a valid CLK positive edge is high.

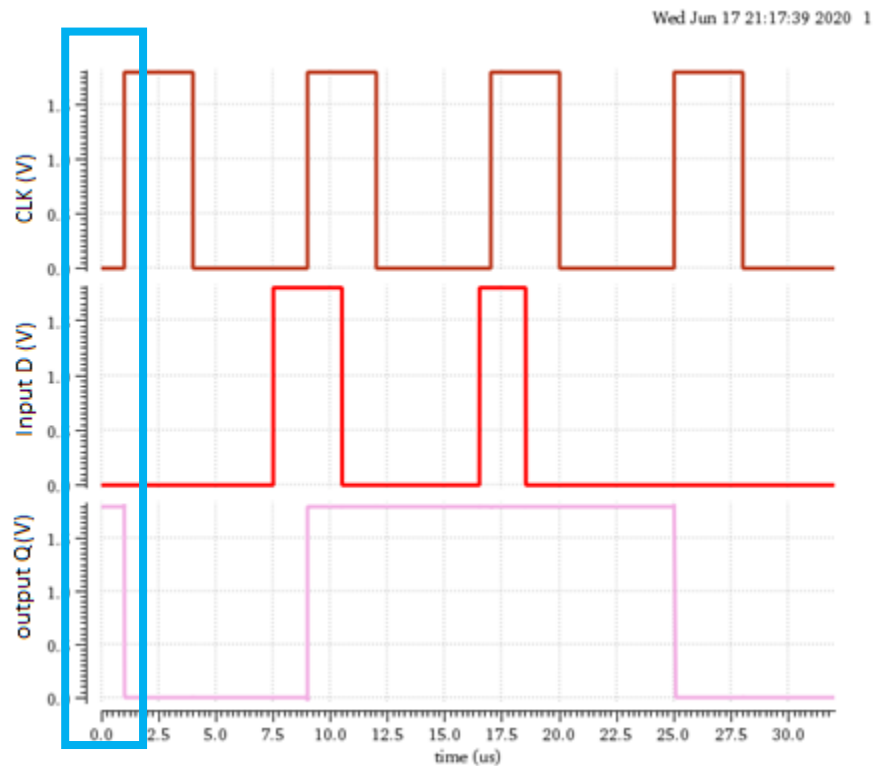


Fig. 16. Transient response of TSPC DFF showing the Q output in a high state in the first instants

To suppress the initial state  $Q = 1$ , we need to add a reset pin connected to the gates of M5 and M8 of the TSPC D-FF circuit (Fig. 17). Since the reset signal is active low then M5 will open the VDD path with this avoiding a short-circuit in node B when CLK is logic low.

Transistor M13 was added to pull node B to a logic 0 during a reset condition. If node B is at 0, M8 will be turned on, then Qn node must be at 1 or VDD. If Qn node is at VDD, M12 will turn on, and then Q output will be at 0 or GND.

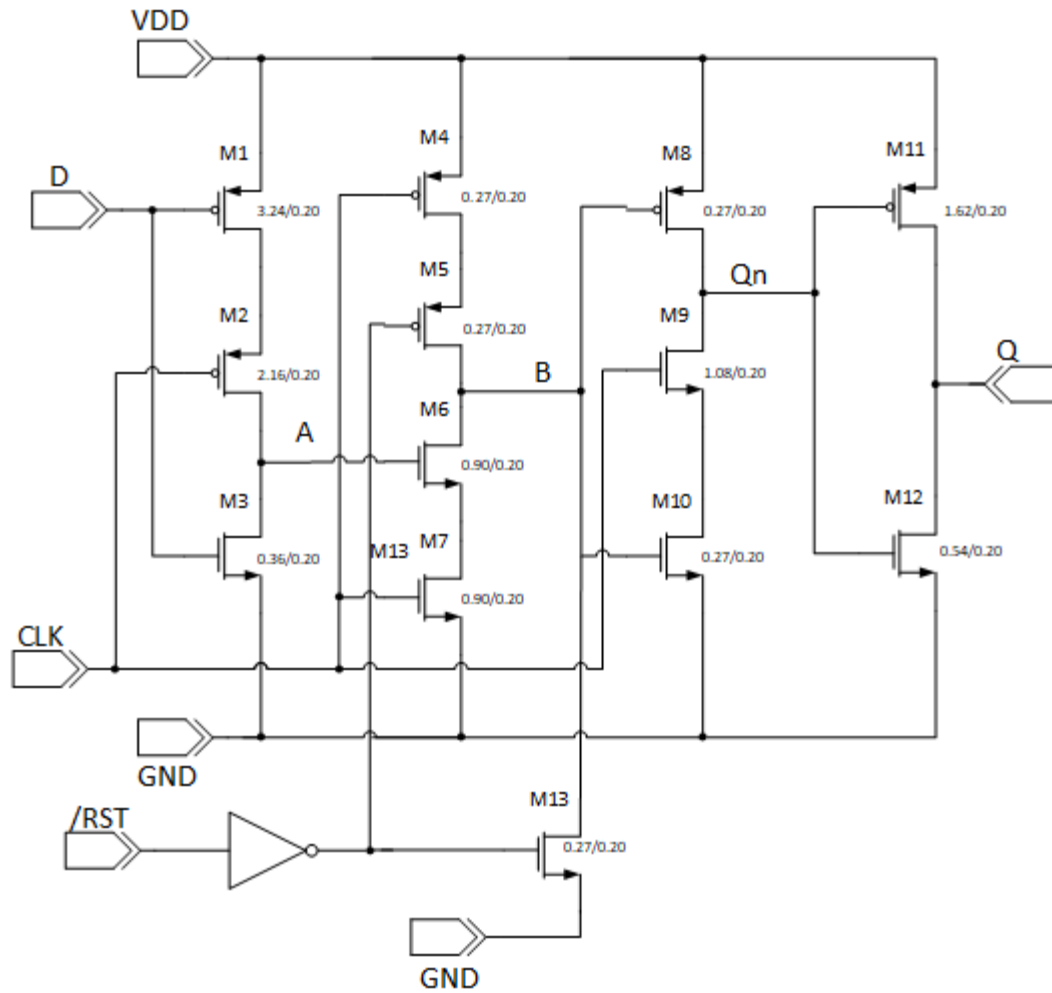


Fig. 17. Schematic of TSPC D-FF with Reset input

## 2.7. Setup and Hold times measurement

As mentioned above, in the SAR-ADC project, we need a D-FF having a short setup time, this is an important feature because this allows detecting small changes in voltage that later are changed to a time-domain in the voltage to time converter block. We are going to define the timing parameters.

Setup time is the minimum time length in which the input data must remain stable before the active edge of the clock. The time is needed to ensure that a valid value is captured [5] [6].

To find the minimum setup time at with a valid value in the Q output, we must provide different values of D from longer times to shorter times, ideally close to the rising edge of the clock.

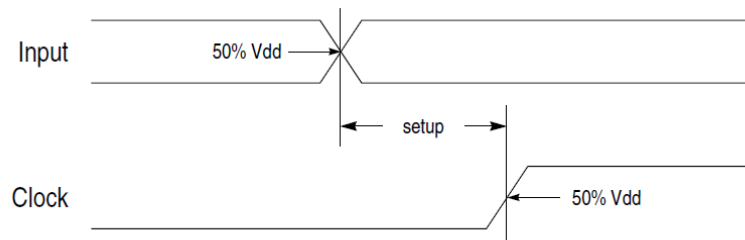


Fig. 18. Setup time for a positive edge flip-flop

Hold time is defined as the minimum time-length that the input data must remain stable after the active edge of the clock, this time is needed for a valid value is captured [5] [6].

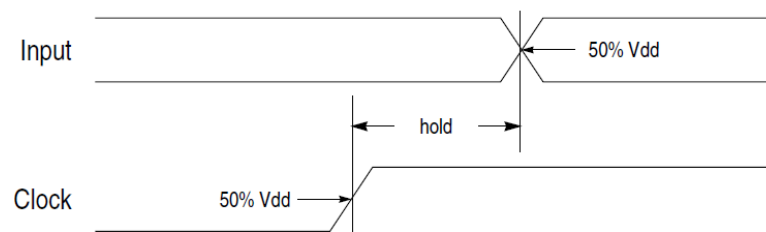


Fig. 19. Hold time for a positive edge flip-flop

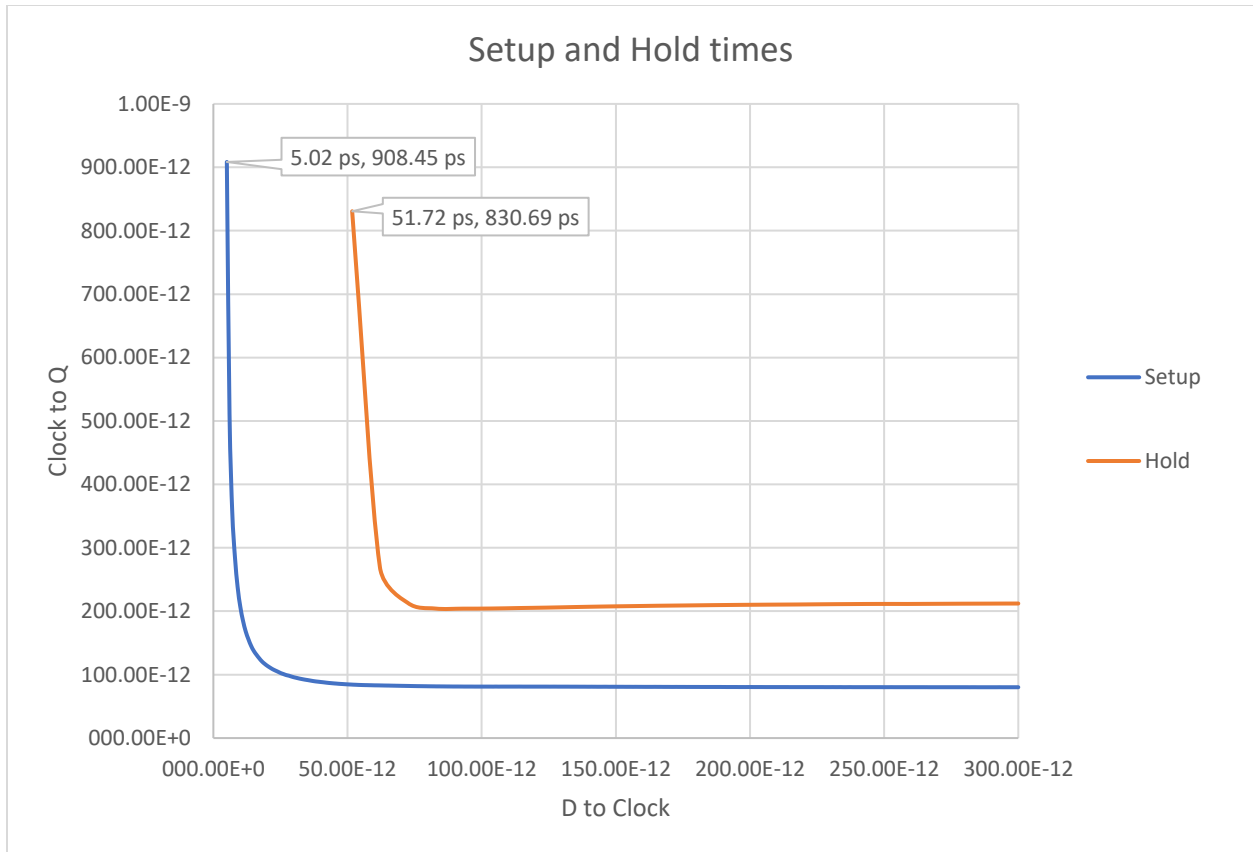


Fig. 20. Setup and Hold Times response of the TSPC D-FF

The plot in Fig. 20 shows that a minimum time of 5.02 ps is required from D to clock, and the corresponding delay from clock to Q is 908.45 ps. This is the setup time of the TSPC D-FF circuit. Referring to the setup in Fig. 20 plot we understand that with higher values of D to clock we will have a lower delay measured clock to Q.

The hold time is measured similarly from Fig. 20, we note it takes a minimum time of 51.72 ps of D to clock delay and its corresponding delay of the clock to Q is 830.69 ps. This is the hold time of the TSPC D-FF circuit.



## 2.8. Propagation Delay

In a logic circuit, the propagation delay is measured from the input pin to the output pin, Fig. 21b illustrates this concept.



Fig. 21. Propagation Delay in a Cell

The change of state of the input A would change the output (Z) immediately. However, this change does not occur immediately as expected but after some delay time, this delay time is called propagation delay.

The propagation delay is mainly due to capacitive loads. To have an idea of the effect of capacitance from the TSPC D-FF circuit, we measure the capacitances at D input and CLK input.

## 2.9. Input capacitance

In the MOSFET, the input capacitance ( $C_{iss}$ ) is the combined capacitance of the Gate node ( $C_{gs}$ ) and Drain node ( $C_{gd}$ ) (Fig. 22).

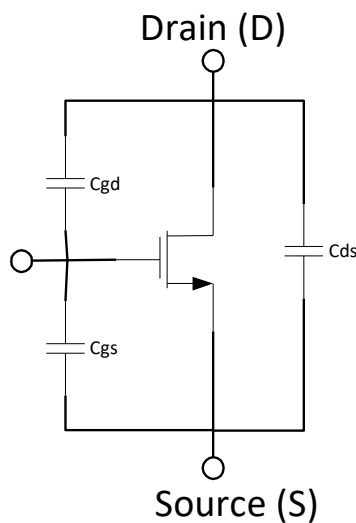


Fig. 22. Input Capacitance Dependency on VDS

One can measure the unknown capacitance of a circuit if we apply a step voltage and we measure in the charge/discharge curve the time constant  $t = RC$  involved in the time-varying voltage in the RC circuit given by (3)

$$V_C(t) = V_O \left( 1 - e^{-\frac{t}{RC}} \right) \quad (3)$$

Where  $V_O$  is the output voltage at the capacitor when a given time large enough and a stable state has been reached.

When the voltage is removed from the circuit, the capacitor starts to discharge through the resistor, and in this case, the time variation of the discharge voltage in the capacitor concerning is defined by (4).

$$V_C(t) = V_O e^{-\frac{t}{RC}} \quad (4)$$

The  $RC$  product in equations (1) and (2) will determine the speed of charge or discharge and it is called the time constant, generally defined by the greek letter  $\tau$ . There are many ways to measure the time constant, one of them is measured through the time need for a voltage  $V_C$  to fall to  $V_O/2$ . This time is known as the half-life  $T/2$  and it is given by (5).

$$\frac{T_1}{2} = (\ln 2) * \tau \rightarrow \tau = \frac{T_1/2}{\ln 2} = \frac{T_1/2}{0.693} \quad (5)$$

The time in which voltage has reached its final value is generally defined as  $5\tau$ .

To find  $\tau$  value, we connect a step waveform voltage source in series with a known value of resistor at the inputs of the TSPC DFF circuit. In the case of input D capacitance measurement, we used an  $R = 100 \text{ M}\Omega$  and the CLK input is tied to GND.

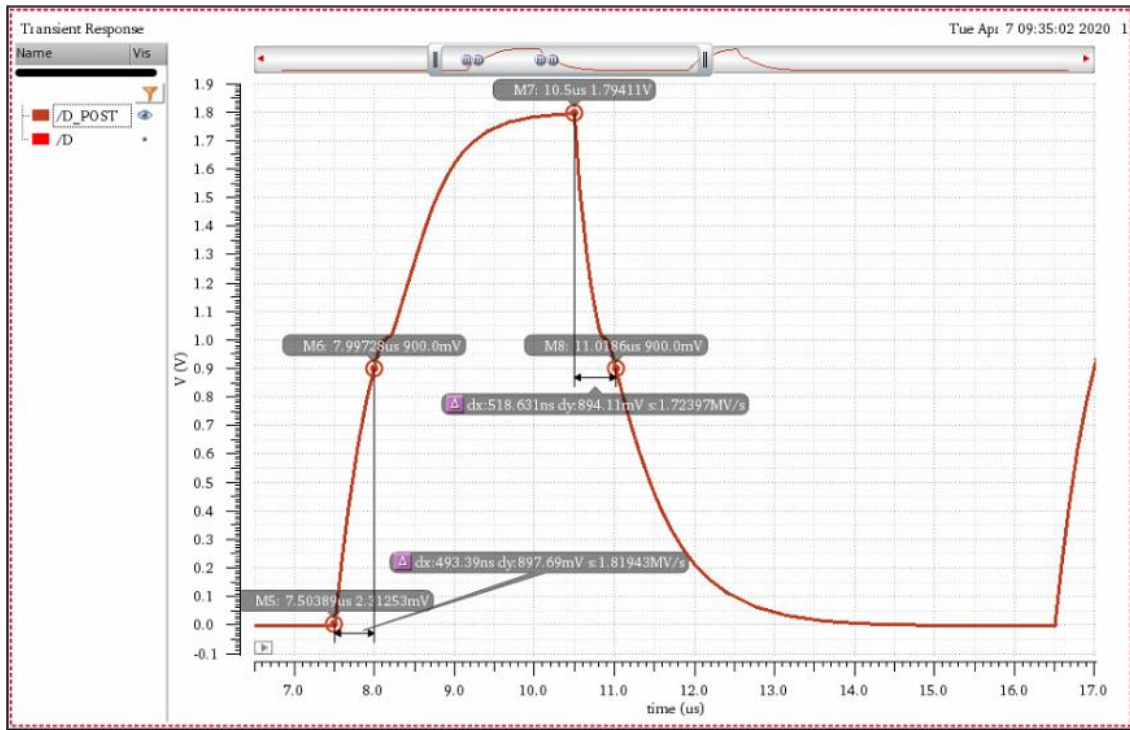


Fig. 23. Step response of TSPC DFF measured at the D input

Fig. 23, Step response of the TSPC DFF circuit to measure the equivalent capacitance at D input.

Equivalent capacitance is calculated through  $\tau$  from discharge part of the step response curve

$$\tau = \frac{dt}{0.639} = \frac{493.39 \text{ ns}}{0.639} = 772.128 \text{ ns}$$

$$C_{in} = \frac{772.128 \text{ ns}}{100 \text{ M}\Omega} = 7.284 \text{ fF}$$

The equivalent capacitance was also calculated from the charge portion of the step response curve, and the resulting value is.

$$\tau = \frac{dt}{0.639} = \frac{518.631 \text{ ns}}{0.639} = 811.629 \text{ ns}$$

$$C_{in} = \frac{811.629 \text{ ns}}{100 \text{ M}\Omega} = 7.656 \text{ fF}$$

We repeat the procedure to measure the equivalent capacitance at the CLK input; in this case, we place a 70 M $\Omega$  resistor in series with the step waveform voltage and also we tied D input to GND.

In the capacitance measurement, we used different values of resistors, 100 MΩ, and 70 MΩ because we have noticed when uses a 70 MΩ resistor at D input a better charge/discharge curve is obtained.

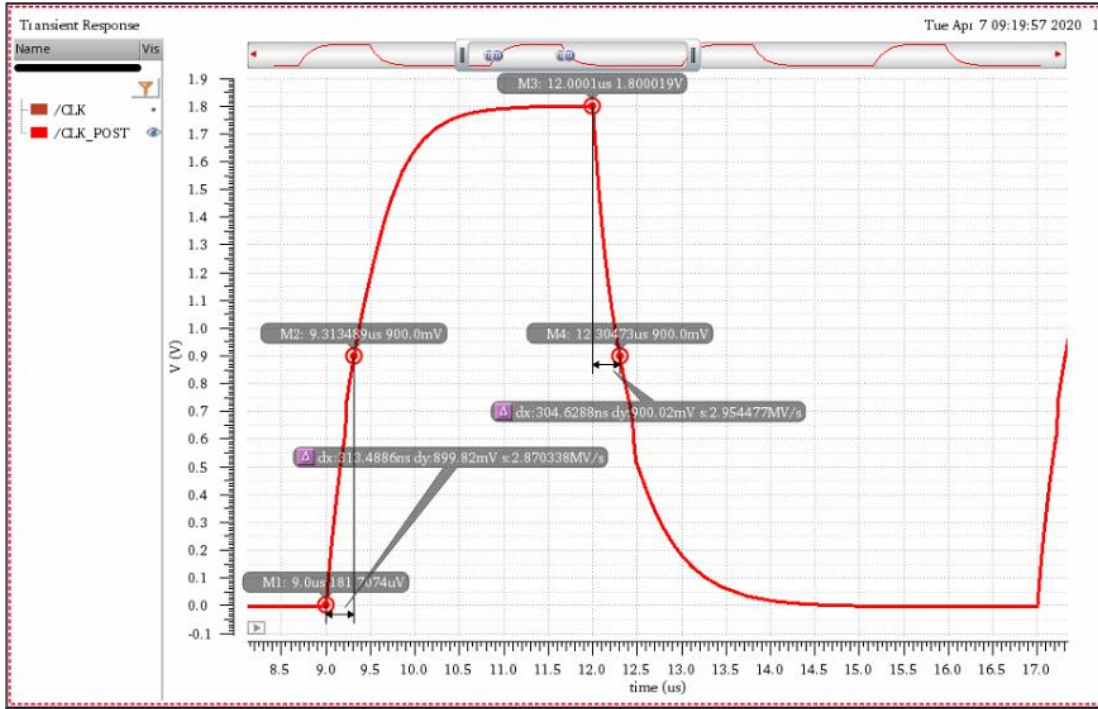


Fig. 24. Step response of TSPC DFF measured at CLK Input

Fig. 24, Shows the capacitance in the CLK input for from Low to High and from High to Low.

The equivalent capacitance at CLK input calculated in the discharge part of the step response is

$$\tau = \frac{dt}{0.639} = \frac{313.489 \text{ ns}}{0.639} = 490.593 \text{ ns}$$

$$C_{in} = \frac{490.593 \text{ ns}}{70 \text{ M}\Omega} = 6.455 \text{ fF}$$

And the capacitance calculated in the charge part of the step response curve is

$$\tau = \frac{dt}{0.639} = \frac{304.629 \text{ ns}}{0.639} = 476.727 \text{ ns}$$

$$C_{in} = \frac{476.727 \text{ ns}}{70 \text{ M}\Omega} = 6.272 \text{ fF}$$

The capacitance values are summaries in Table 2

Parameter	Simulated Value	Comment
Input Capacitance	D: C <sub>in</sub> (L-to-H)=7.284 fF C <sub>in</sub> (H-to-L)=7.656 fF  CLK: C <sub>in</sub> (L-to-H)= 6.455 fF C <sub>in</sub> (H-to-L)=6.272 fF	
Transistor Number	15	
Average Power@200 KHz	84.4 nW	
Load Capacitance	3 fF	Tested 10 pF
Propagation Delay	683.5 ps@7.47 ps	Clock to Q delay
Propagation Delay	690.9 ps@7.47 ps	D to Q
Setup time	5.02 ps	
Hold time	51.72 ps	

Table. 3. Final Parameters of TSPC D-FF with reset functionality

## 2.10. PVT analysis

PVT stands for Process, Voltage, and Temperature. There is a deviation of the transistor attributes during fabrication. There is a statistical variability of the physical characteristics from chip to chip. This includes mask alignment, etching times, doping levels. During manufacturing, a die will have a different process variation if it was taken from the center of the wafer than of the edge of the same wafer. This happens because of the layers used to fabricate a die are not uniform all over the wafer. As we go away from the center of the die, layers can differ in size.

Some of the effects of the process variation are:

- i. Oxide thickness
- ii. Dopant and mobility fluctuations
- iii. Transistor width and length
- iv. RC Variation

An for the design to work properly in all junction and ambient temperature ranges from -40 to 125 °C, and with a variation supply from 1.62 V to the typical 1.8 V and up to 1.98 V. We need to simulate at different corners of the process which might be what the design faces after fabrication.

The design needs to meet all specifications measured with a typical process. Not all corners are critical and then we perform simulations only for the corners indicated in Table 4.

Corner Name	Model	Temperature	Voltage
tsmc018_tt_1p8V_25C	tt	25	1.8 V
tsmc018_ff_1p98V_125C	ff	125	1.98 V
tsmc018_ff_1p98_m40C	ff	-40	1.98 V
tsmc018_ss_1p62V_125C	ss	125	1.62 V
tsmc018_ss_1p62V_m40C	ss	-40	1.62 V

Table. 4. PVT Corners

The result of PVT is reported in Appendix A.

# 3. Physical design

Physical design refers to the process used to transform a design from schematic into a pattern array of layers which is called layout. The layout describes the position of the transistors, interconnects, pins, and layers used for interconnection between them.

## 3.1. Stick Diagram

Stick diagrams are used to plan the layout. Stick diagram was first introduced by Mead and Conway in the '80s, as a way to translate circuits into silicon. A stick diagram uses layers and connections in several layers using simple stick arrays. It acts as an interface between the schematic and the layout of the circuit bringing closer to the layout.

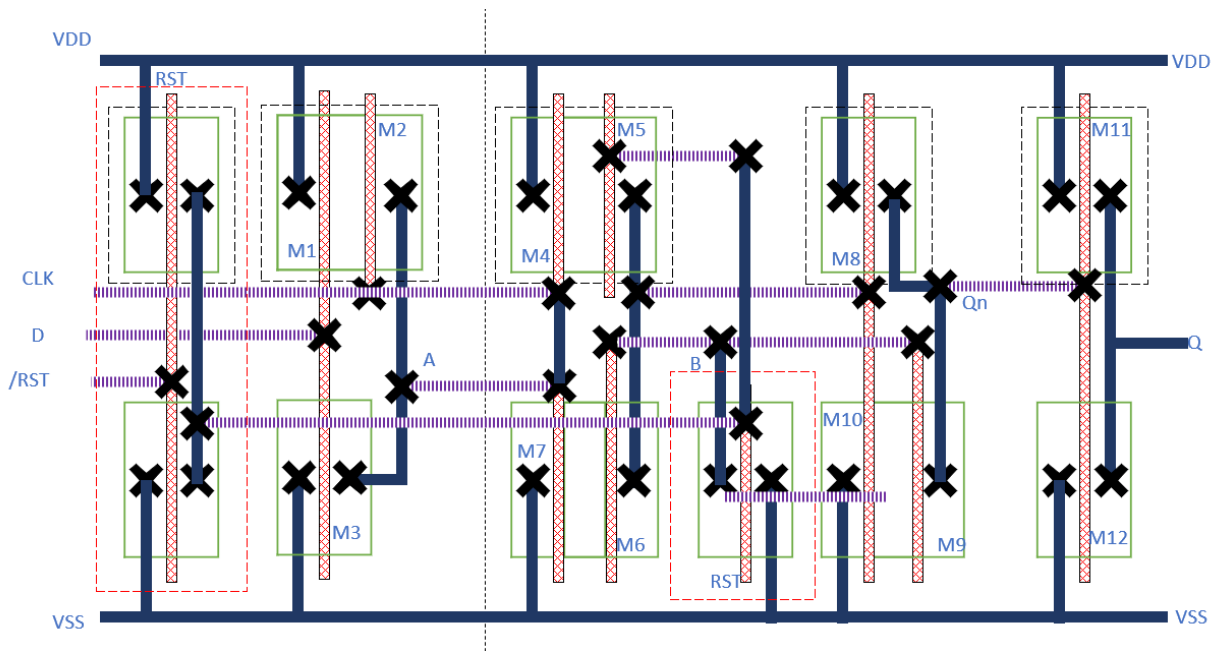


Fig. 25. Stick Diagram for the TSPC D-FF

## 3.2. Layout

Specifications of the full custom layout for TSPC D-FF are the following.

The final dimensions of the height are  $19.6\mu\text{m}$  and that height is a multiplier of a standard cell of  $3.92\mu\text{m}$ .

This dimension is needed since in Encounter tool, which is the software used to place custom cells and Verilog cells, tries to place those cells and is not able to connect the full custom cells either power or in and out connections.

All the inputs, outputs, and power connections were placed in metal 3 since Encounter will try to automatically route the connections and if the connections or power were placed in Metal 1 and Metal 2 Encounter will not be able to route the cells successfully.

The routing was done using Metal 1 with  $230\text{ nm}$  and Metal 2 with  $0.28\text{ nm}$  since Polysilicon which is why we used  $0.2\text{ nm}$  since it is a highly resistive material, and this will give you problems in Post Layout Simulation. In some cases where you cannot avoid it. Routing in this Polysilicon must be kept to a minimum.

To have a list of capacitance and resistance of your layout, we must perform a parasitic extraction, and with those values, you must decrease the resistance and capacitances high values since those will impact your Post Layout Simulation. To reduce the parasitic, you must reduce the lengths and the interconnection wires

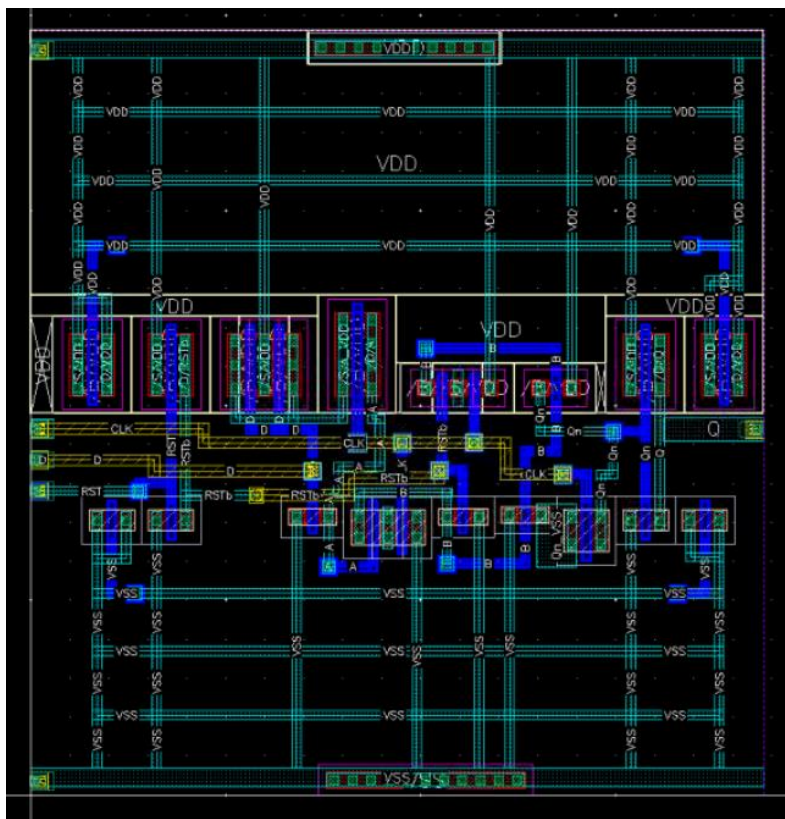


Fig. 26. Layout for MTSPC D-FF



### **3.3. Layout Verification.**

This is a process in which a layout corresponding to design is verified to ensure proper electrical and logical functionality. Verifications involve design rule check (DRC), layout versus schematic (LVS), and parasitic extraction.

#### **Design Rule Checking (DRC)**

At any time during the design, we can verify if any dimensions are being violated. Dimensions like metal to metal minimum spacing in the same layer or via to via minimum spacing. The report can be found in Appendix A, Fig. 28

#### **Layout Versus Schematic (LVS)**

This is used to find mismatches between the layout and schematic. It helps identify if there is any difference between the schematic and the layout. The report can be found in Appendix A, Fig. 29

#### **Parasitic extraction**

It is the calculation of the parasitic capacitance, parasitic resistance, and even parasitic inductance and the final purpose is to create an accurate model of the design. This will help to create detailed simulations that can emulate real-world conditions of the design. The report can be found in Appendix A, Fig. 30

### 3.4. Post-Layout Verification.

We must verify the correct functionality according to how your layout is done since this might be critical in the actual performance of the design. To have an idea of how the final design will work, we should perform a post-layout simulation using the extracted view that includes the parasitic capacitances and resistances. The procedure is identical to that of a simulation using ADE L

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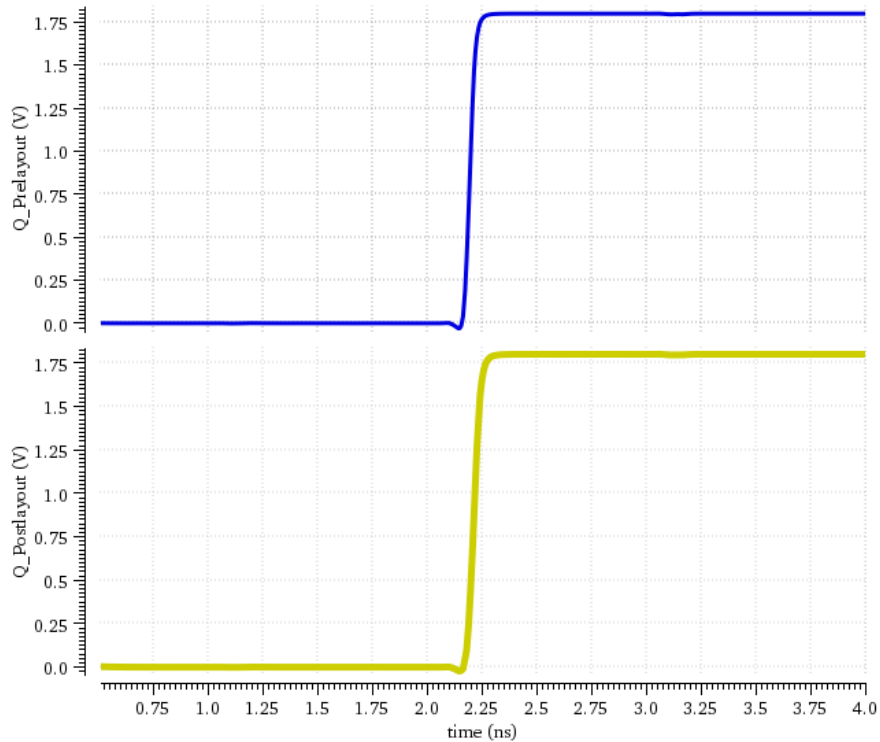


Fig. 27. Post and Pre Layout simulation

In Fig. 27 we can notice that both graphs look very similar, we can infer from this plot that the layout was done correctly.

	Pre-Layout	Post-Layout	Variation
Setup time	5.02 ps@908.45 ps	2.01 ps@695.18 ps	-59.96% @-23.48%
Hold time	51.72 ps@830.69 ps	72.41 ps@453.59 ps	40% @-44.93%
Maximum frequency	1 MHz	1 MHz	
Power Consumption	62.61 $\mu$ W	67.13 $\mu$ W	7%

Table. 5. The variation between Post and Pre Layout

The maximum frequency depends that it does not violate the setup time.

The main difference between pre and post-layout have to do with parasitics that are added to the post layout extraction since those are analyzed and extracted from the layout one way to compensate for those errors are reduce the capacitance by increasing the thickness of the traces another possibility is to reduce the traces and the resistance is by shorting the traces like polysilicon that we know is highly resistive.

## Conclusions

Among the different blocks of the based-time SAR-ADC, designed as the team project. I chose the design of the TSPC D-FF arbiter. Part of my technical assignment was to examine several D-FF topologies of different amounts of transistors; my goal was to find a working topology of an arbiter circuit with the fewest transistors possible. It was not able to find a working configuration with fewer transistors than the TSPC D-FF reported in [2]. However, we proposed a design that responds to what is expected for the based-time SAR-ADC.

With the analysis done in the initial approach of the arbiter circuit, I found that one of the transistors was misplaced and additionally this transistor must be a PMOS instead of an NMOS.

We add a reset functionality to avoid the TSPC D-FF is in an unknown state before a valid clock rising edge.

The transistor sizing of the TSPC D-FF was done to achieve the required setup time and hold time for the SAR-ADC without increasing power consumption or layout area. The achieved setup time is 2.01 ps, the hold time is 72.41 ps, and the power consumption is 67.13  $\mu\text{W}$ @200 KHz. All these measurements were done with typical process parameters, nominal supply voltage, and room temperature.

We used the stick diagram approach to make easy the layout and satisfy floorplan requirements of the SAR-ADC layout. The layout area of the TSPC D-FF circuit is 368.284  $\mu\text{m}^2$ .

I also contributed to the DAC block design. The DAC topology that I analyzed was the R2R. This topology was not selected because of its higher power consumption compared with the split segmented switched-capacitor topology. This design experience was a very valuable opportunity for me to acquire knowledge about the full design flow of an ASIC and in specific subjects. For example, properly sizing of the transmission-gates switches, and go deeper in learning the real response of full-custom DAC blocks.

## Reference

- [1] T. Matsuura, “Integrated CMOS ADC — Tutorial review on recent hybrid SAR-ADCs,” in 2017 MIXDES - 24th International Conference "Mixed Design of Integrated Circuits and Systems, Jun. 2017, pp. 29–34, doi: 10.23919/MIXDES.2017.8004589.
- [2] Zarate Jorge, Liu Xiaosen, and Hazariwala Harshad, “Low Power Modified SAR Converter.” internal report.
- [3] B. Razavi, “TSPC Logic [A Circuit for All Seasons],” IEEE Solid-State Circuits Mag., vol. 8, no. 4, pp. 10–13, 2016, doi: 10.1109/MSSC.2016.2603228.
- [4] A. S. Sedra and K. C. Smith, Microelectronic circuits, 5. ed., student ed. New York, NY: Oxford Univ. Press, 2004.
- [5] S. Levitan and B. Zhao, “Tutorial4B.” [http://www.pitt.edu/~kmram/1192-2192/tutorials/Tutorial4B/Tutorial\\_Parametric.html](http://www.pitt.edu/~kmram/1192-2192/tutorials/Tutorial4B/Tutorial_Parametric.html).
- [6] K. Kamalpreet, M. Nishant, and I. Syed Shakir, “Delay Characterization for Sequential Cell,” Design And Reuse. <https://www.design-reuse.com/articles/37652/delay-characterization-for-sequential-cell.html> (accessed Feb. 09, 2020).
- [7] Martinez, Esteban and Cotero, Bernardo, “Practica 02\_Medición de la constante de tiempo en un circuito RC.” ITESO, internal report.

# Appendix A. Layout Verification

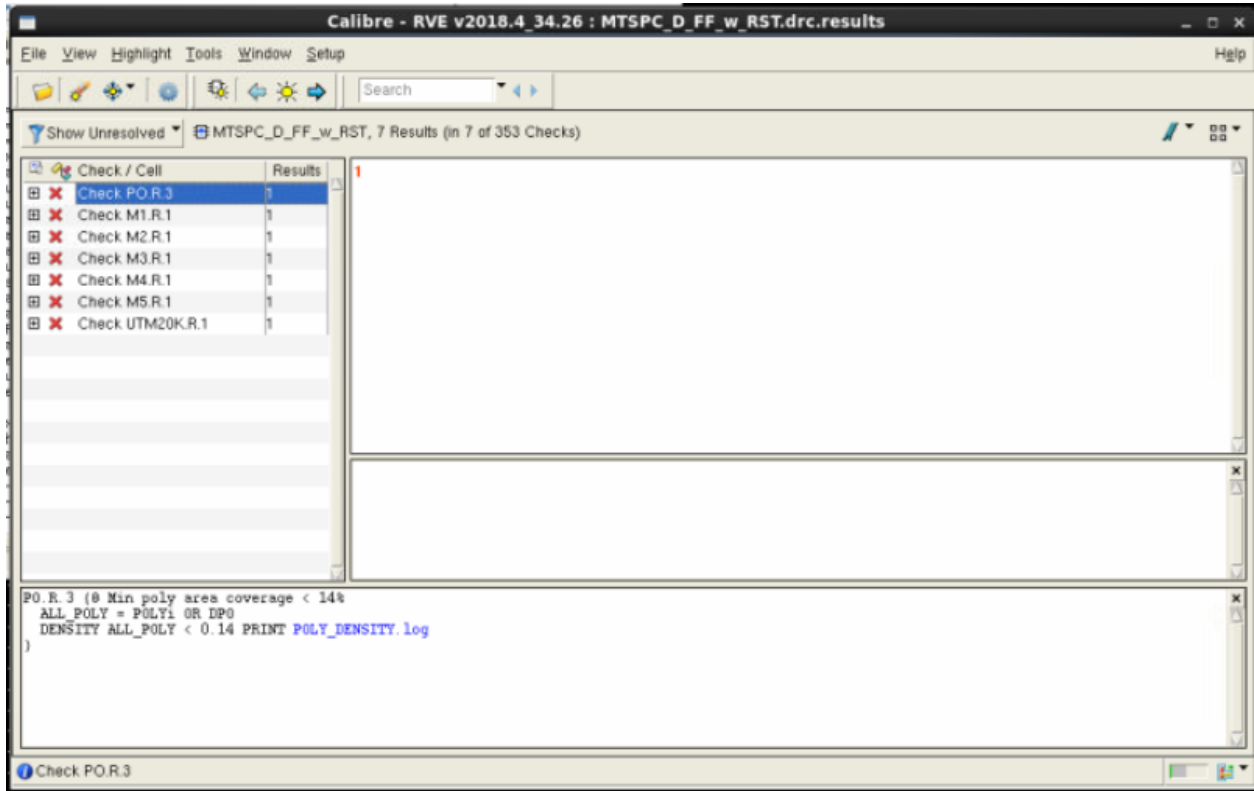


Fig. 28. DRC report of the TSPC D-FF

```

1
2
3
4 | #####
5 | ##                                ##
6 |           CALIBRE SYSTEM           ##
7 |           ##                        ##
8 |           LVS REPORT                ##
9 |           ##                        ##
10 | #####
11
12
13
14 REPORT FILE NAME:      MTSPC_D_FF_w_RST.lvs.report
15 LAYOUT NAME:          /home/imartinez/Querio/MTSPC_D_FF_w_RST.sp ('MTSPC_D_FF_w_RST')
16 SOURCE NAME:          /home/imartinez/Querio/MTSPC_D_FF_w_RST.src.net ('MTSPC_D_FF_w_RST')
17 RULE FILE:            /home/imartinez/Querio/calibre.lvs_
18 CREATION TIME:        Wed Jun 3 18:35:15 2020
19 CURRENT DIRECTORY:    /home/imartinez/Querio
20 USER NAME:            imartinez
21 CALIBRE VERSION:      v2018.4_34.26   Mon Dec 3 14:38:12 PST 2018
22
23
24
25             OVERALL COMPARISON RESULTS
26
27
28
29             #   #####
30             #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #
31             #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #
32             #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #
33             #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #   #
34
35
36
37
38 .....
39             CELL SUMMARY
40 .....
41
42 Result      Layout      Source
43 -----
44 CORRECT     MTSPC_D_FF_w_RST     MTSPC_D_FF_w_RST
45
46
47 .....
48
49             LVS PARAMETERS
50 .....
51

```

Fig. 29. LVS Report of the TSPC D-FF

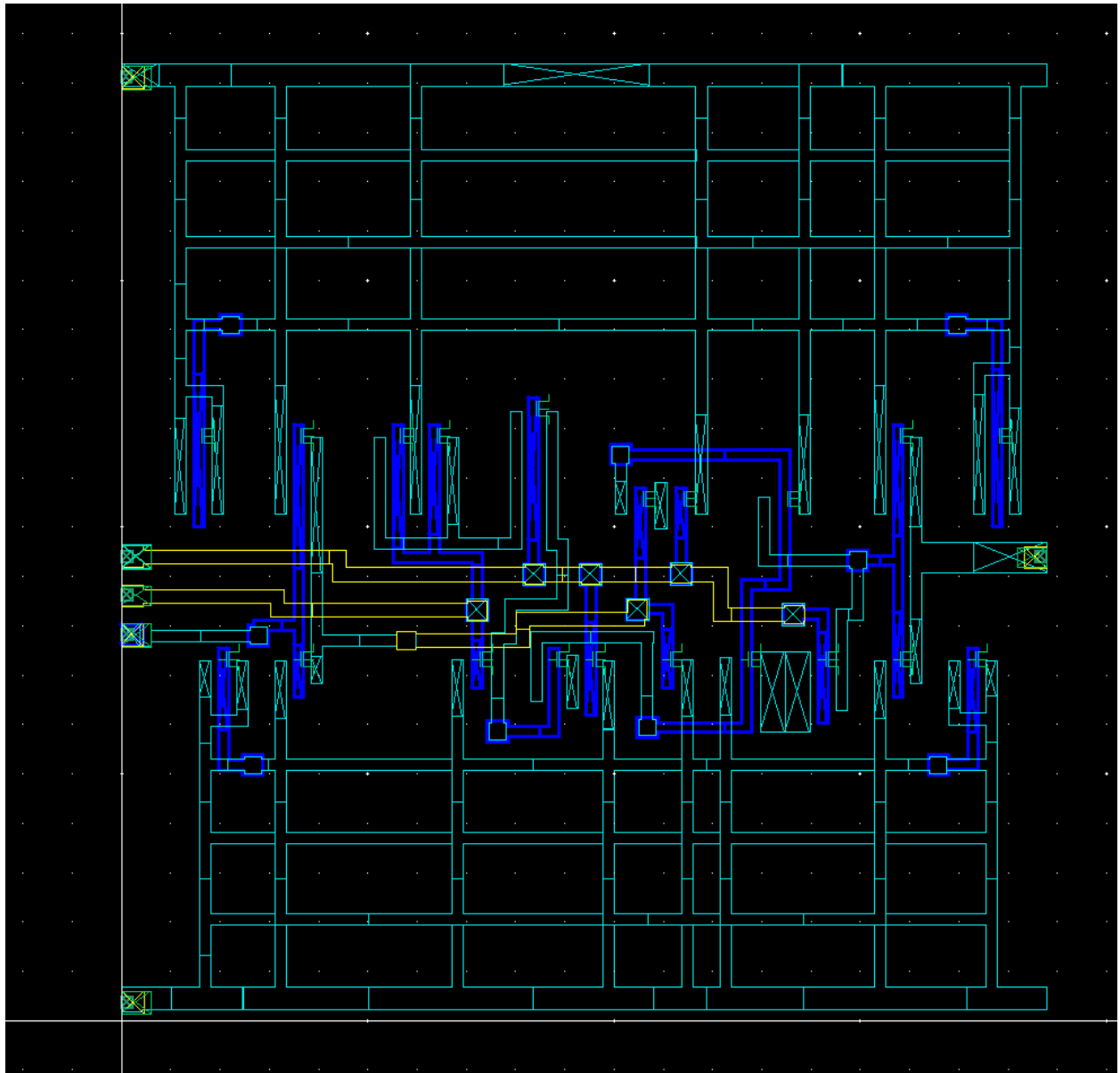


Fig. 30. Extracted view of the TSPC D-FF

## Appendix B. Post and Pre layout PVT Simulation

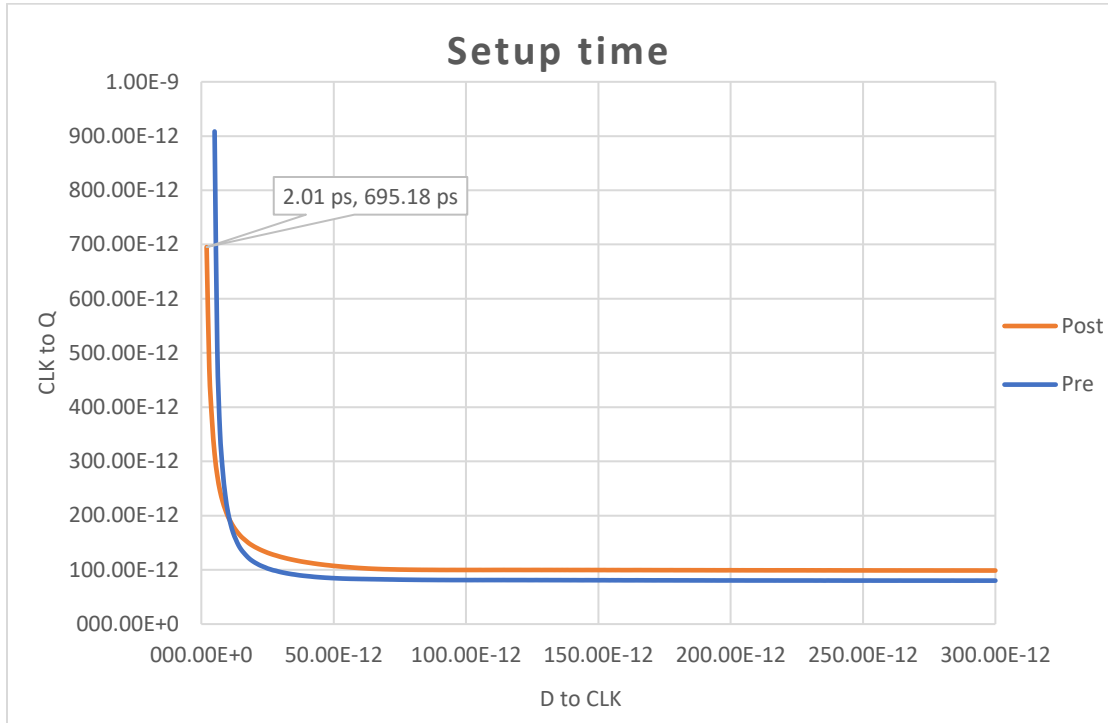


Fig. 31. Corner tsmc018\_tt\_1p8v\_25c for Setup

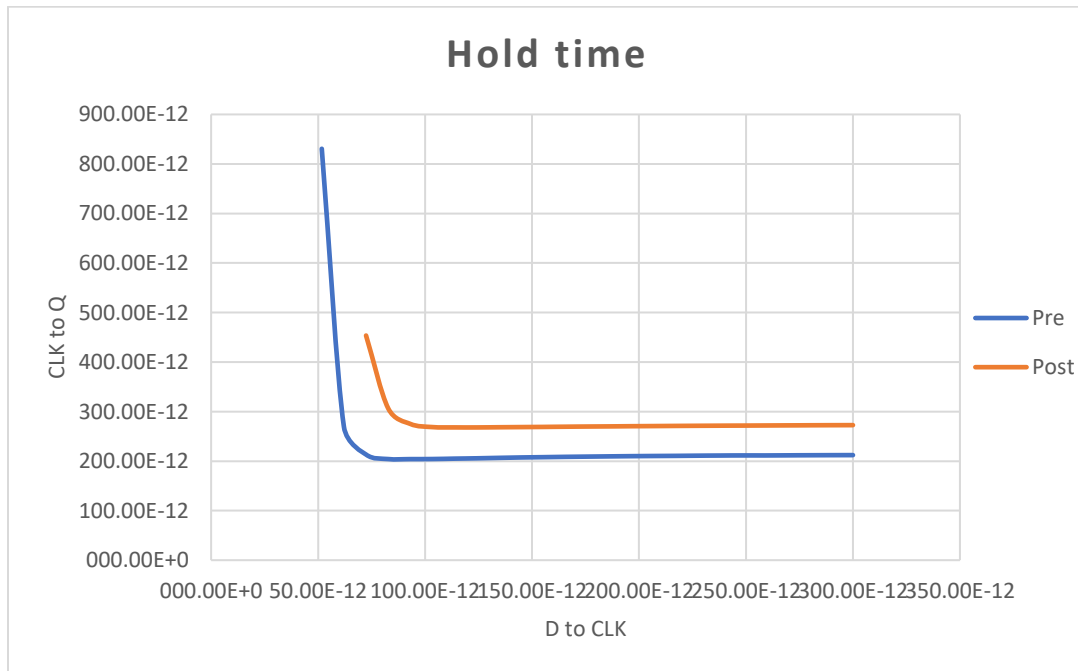


Fig. 32. Corner tsmc018\_tt\_1p8v\_25c for Hold



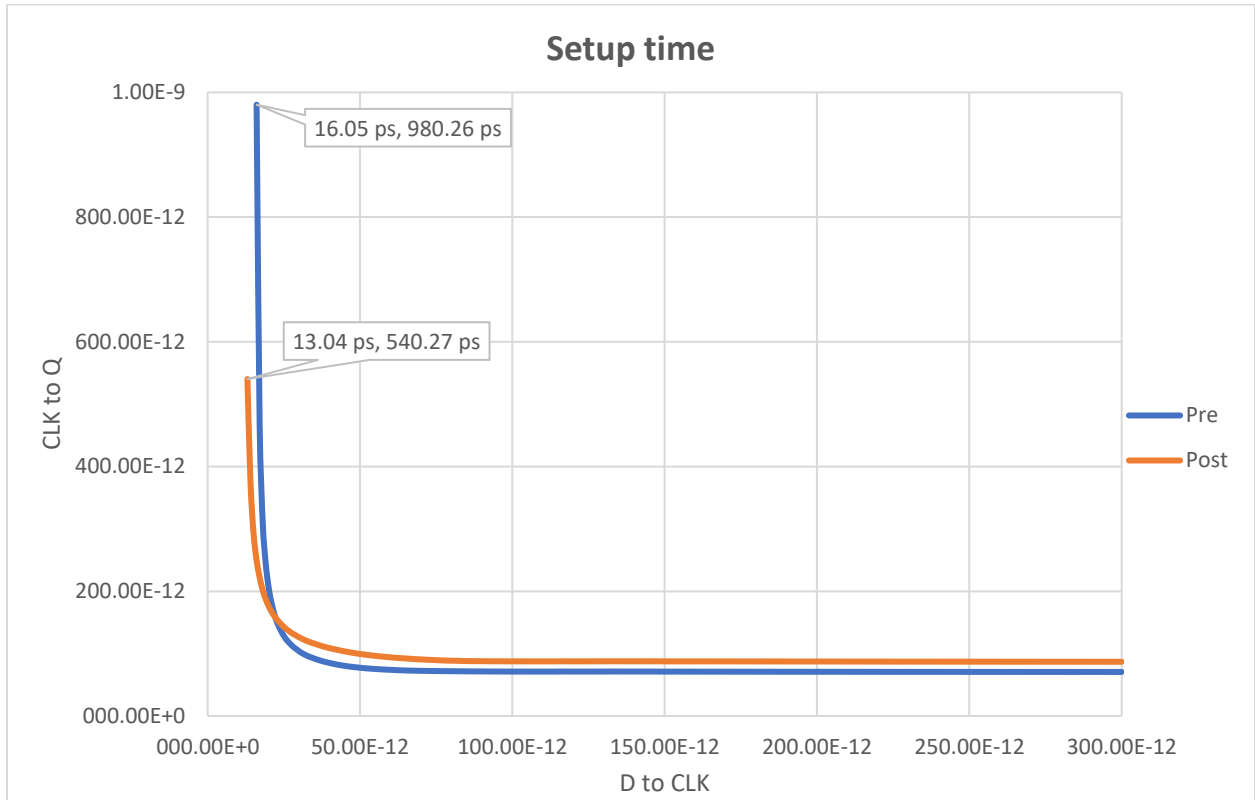


Fig. 33. Corner tsmc018\_ff\_1p98v\_125c for Setup

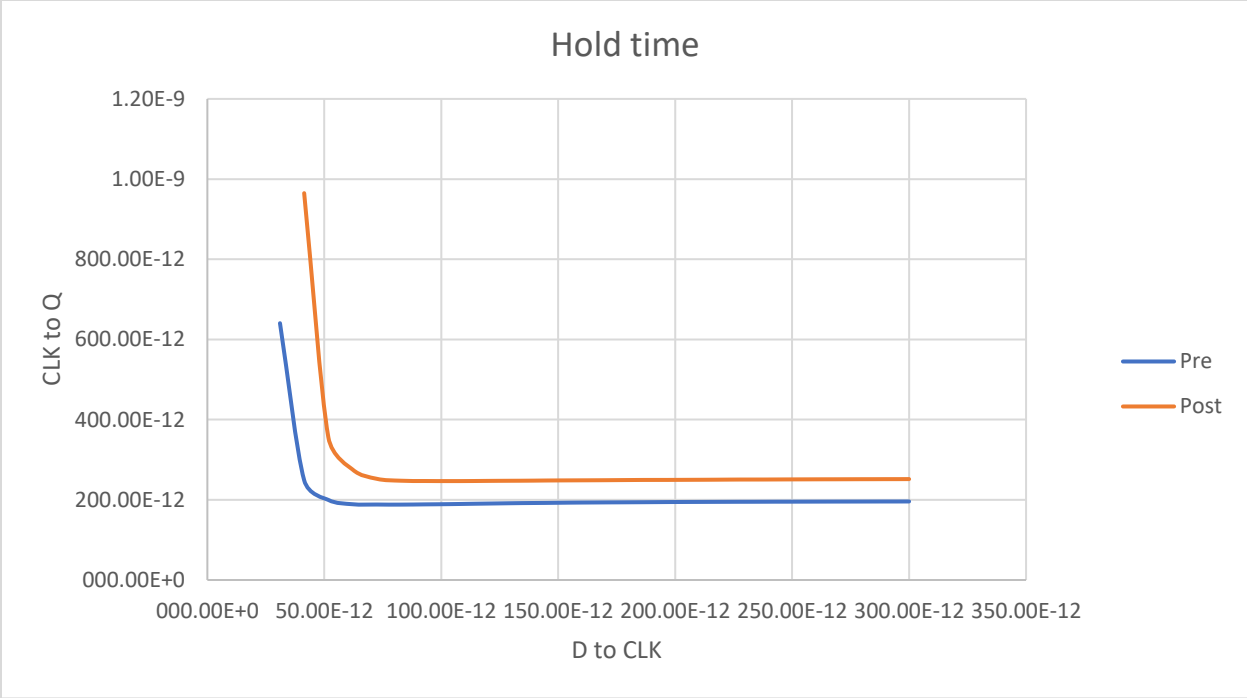


Fig. 34. Corner tsmc018\_ff\_1p98v\_125c for Hold

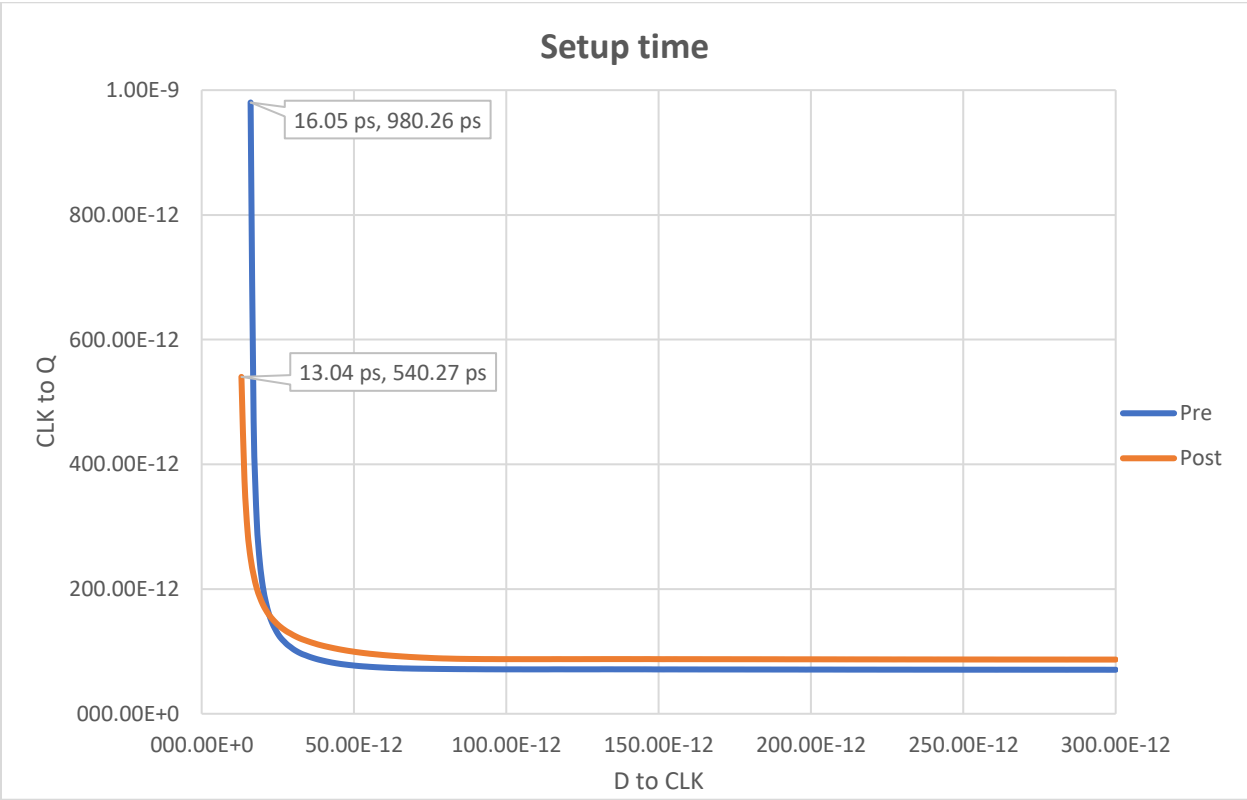


Fig. 35. Corner tsmc018\_ff\_1p98v\_m40c for Setup

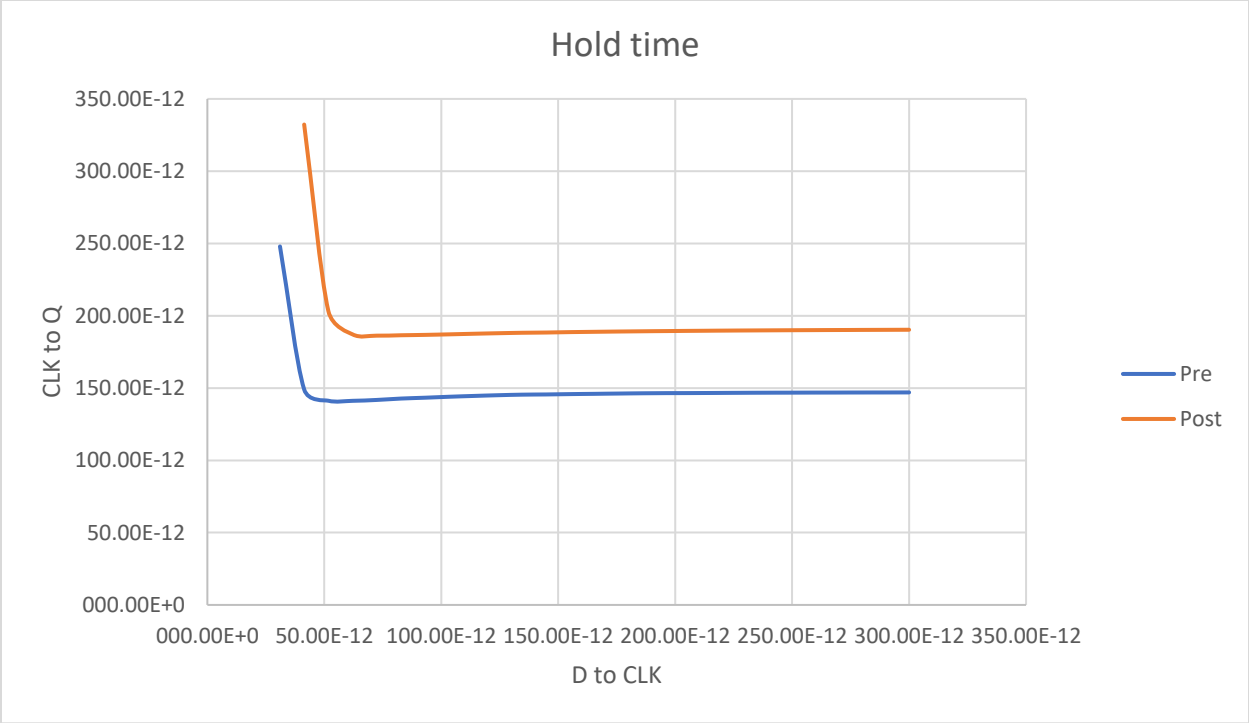


Fig. 36. Corner tsmc018\_ff\_1p98v\_m40c for Hold

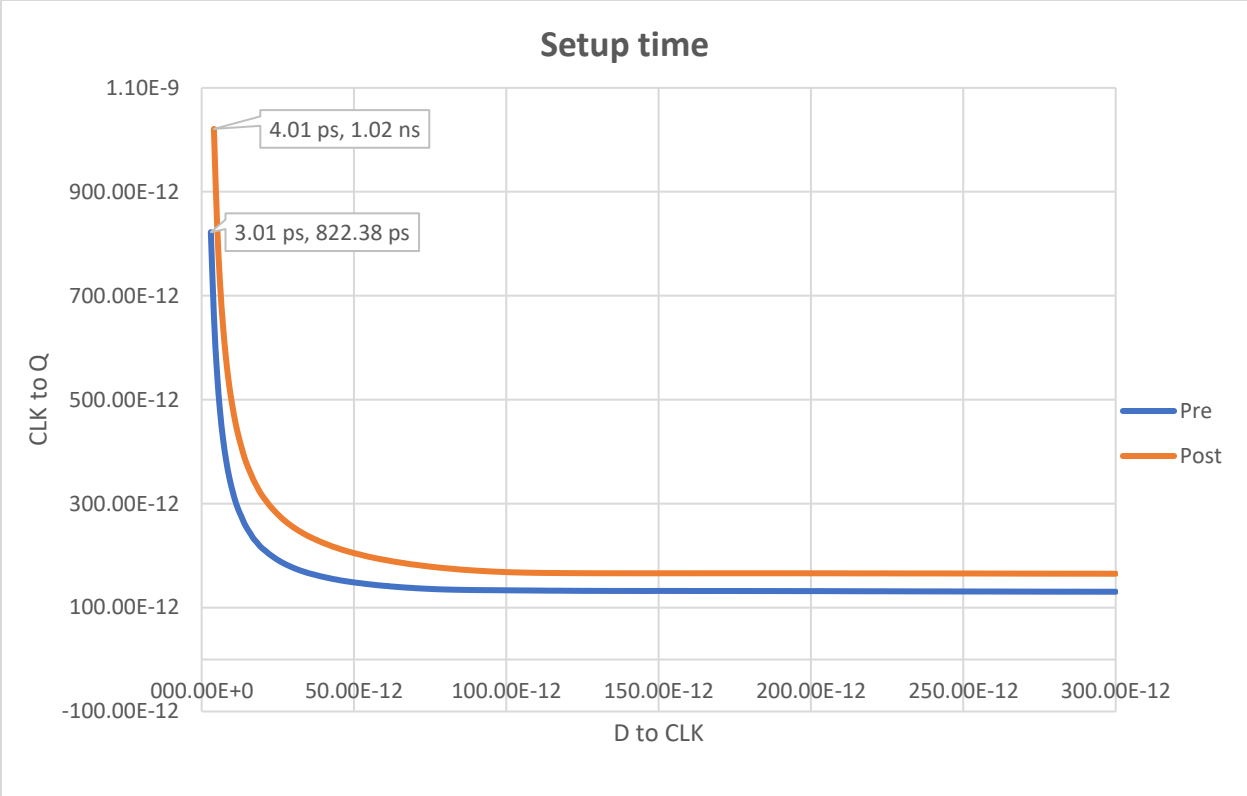


Fig. 37. Corner tsmc018\_ss\_1p62v\_125c for Setup

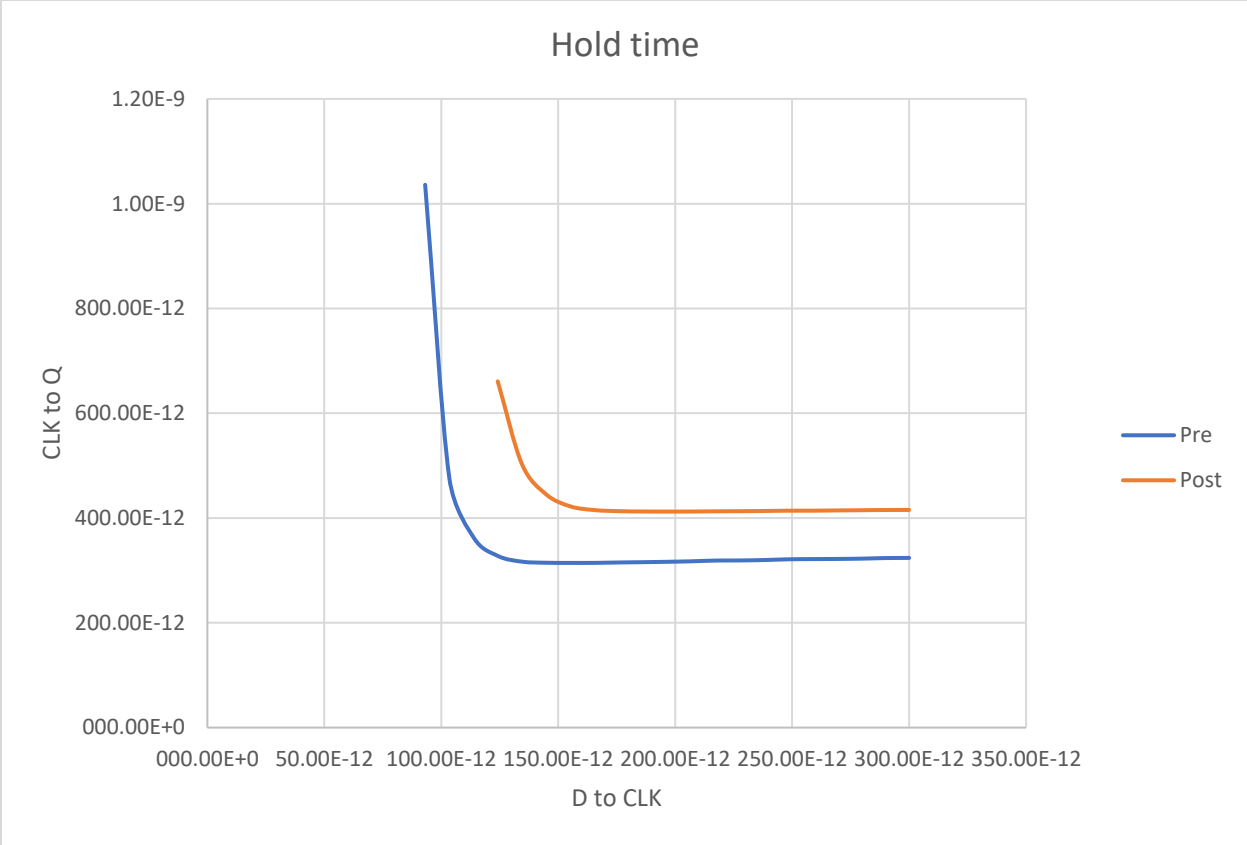


Fig. 38. Corner tsmc018\_ss\_1p62v\_125c for Hold

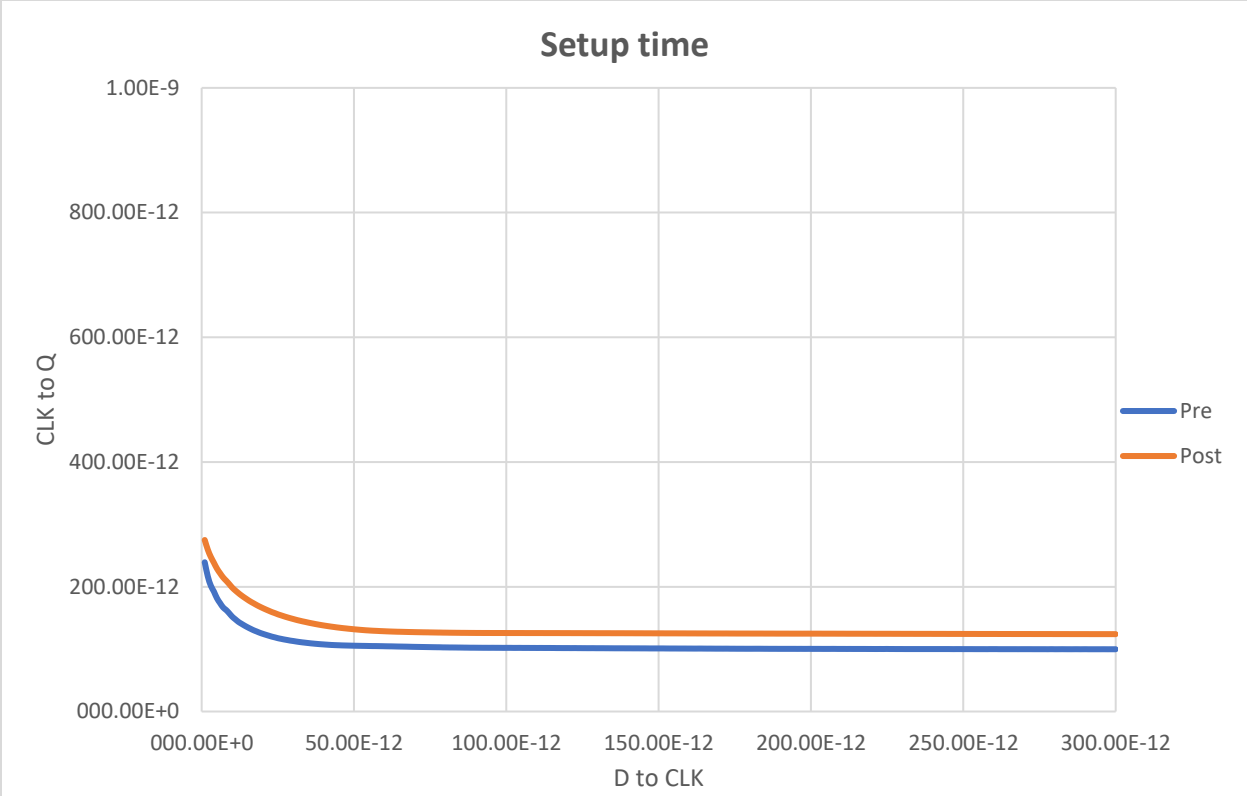


Fig. 39. Corner tsmc018\_ss\_1p62\_m40c for Setup

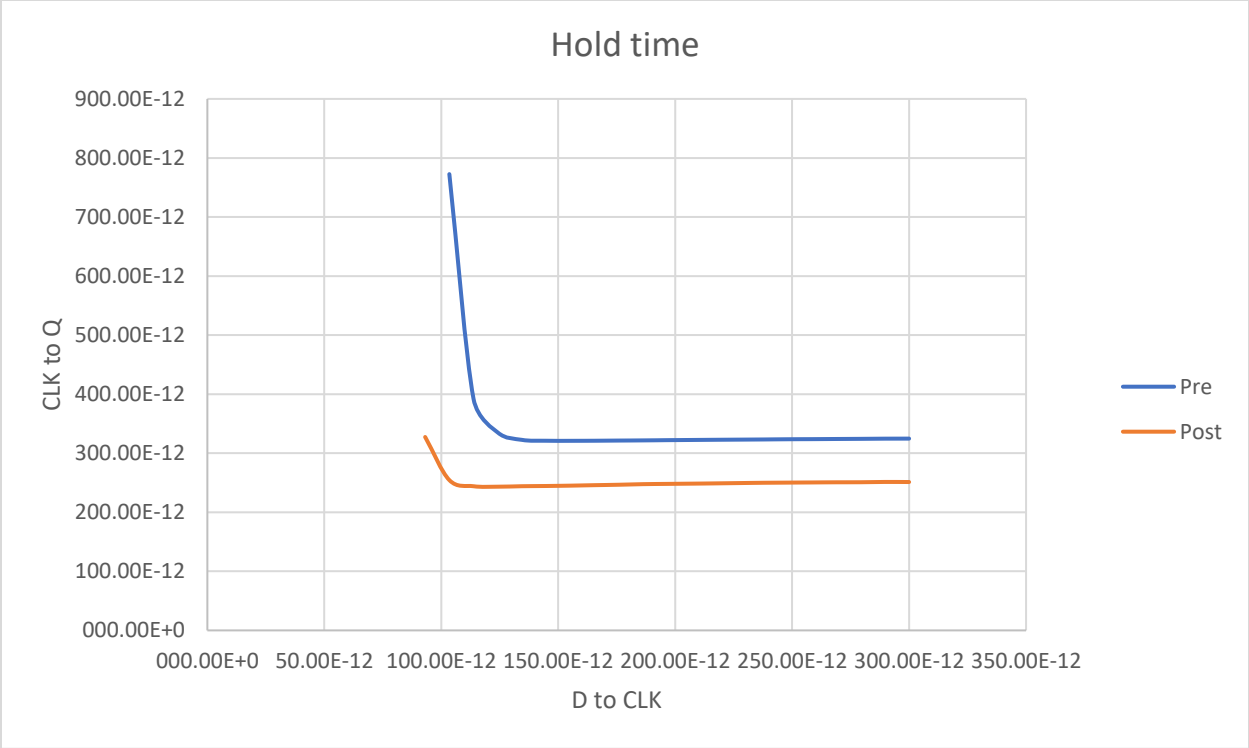


Fig. 40. Corner tsmc018\_ss\_1p62\_m40c for Hold

## Appendix C. Virtuoso Schematic with W and L values

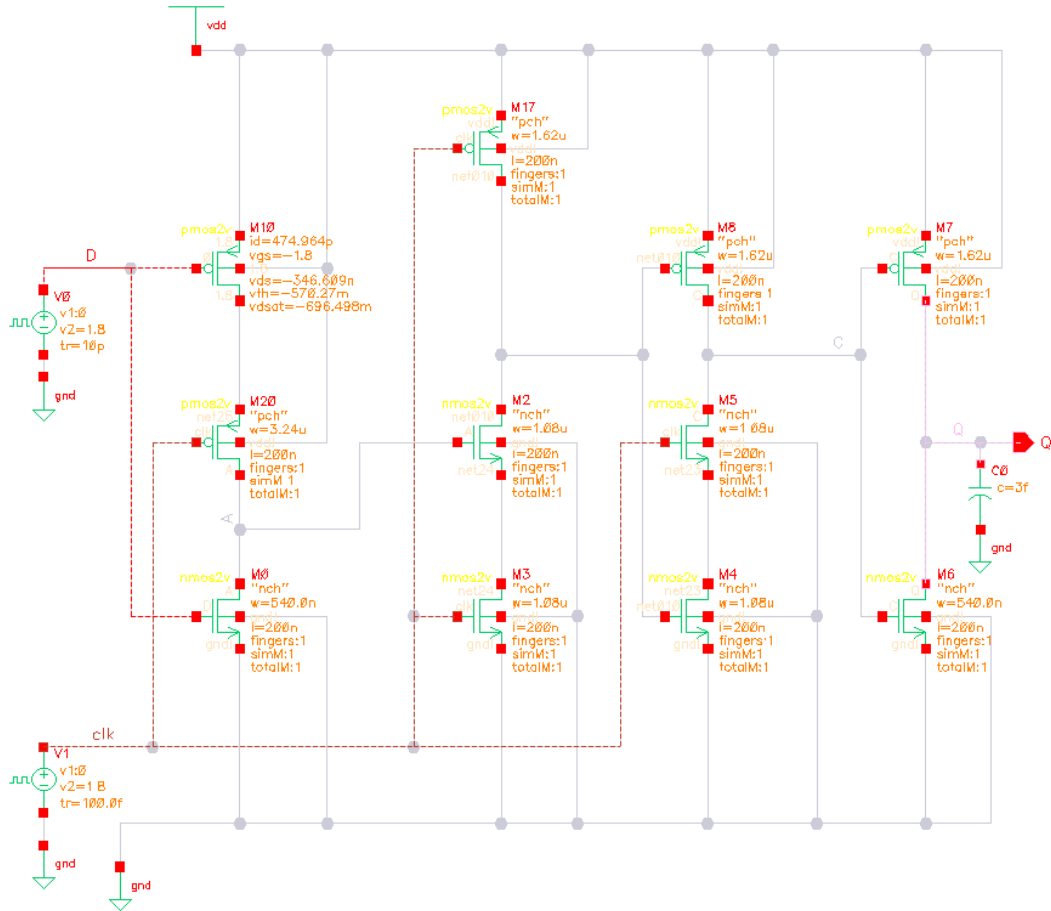


Fig. 41. Virtuoso Schematic Design with its W and L values



## Appendix C. Virtuoso Schematic to remove glitches with W/L

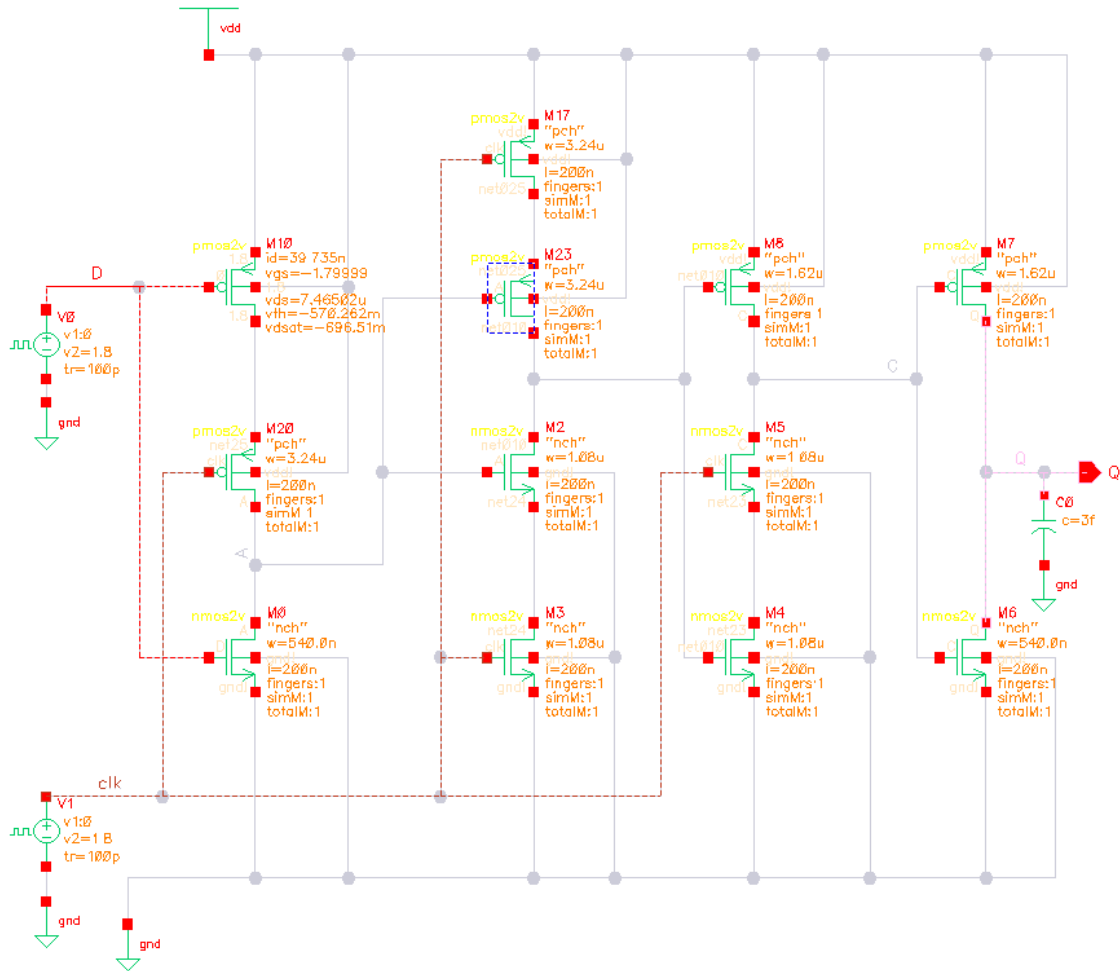


Fig. 42. Virtuoso Schematic Design without glitches of the TSCP D-FF along with its W and L values