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A Holistic Formulation for System Margining and Jitter Tolerance Optimization in Industrial Post-Silicon Validation

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Abstract— There is an increasingly higher number of mixed-signal circuits within microprocessors and systems on chip (SoC). A significant portion of them corresponds to high-speed input/output (HSIO) links. Post-silicon validation of HSIO links can be critical for making a product release qualification decision under aggressive launch schedules. The optimization of receiver analog circuitry in modern HSIO links is a very time consuming post-silicon validation process. Current industrial practices are based on exhaustive enumeration methods to improve either the system margins or the jitter tolerance compliance test. In this paper, these two requirements are addressed in a holistic optimization-based approach. We propose a novel objective function based on these two metrics. Our method employs Kriging to build a surrogate model based on system margining and jitter tolerance measurements. The proposed method, tested with three different realistic server HSIO links, is able to deliver optimal system margins and guarantee jitter tolerance compliance while substantially decreasing the typical post-silicon validation time.

Index Terms—bit-error-rate, DOE, equalization, eye-diagram, high-speed serial I/O, interconnects, jitter, Kriging, optimization, post-Si validation, receiver, SerDes, transmitter.

1 INTRODUCTION

Complexity of new embedded systems has grown to an amazing level. Today's most advanced processors and systems on chip (SoC) incorporate millions of transistors, and must be compatible with dozens of operating systems, hundreds of platform components and thousands of hardware devices and software applications. To ensure leading performance, reliability and compatibility in this complex environment, companies invest over hundreds of millions annually in component and platform validation [1].

The combined effects of increased product complexity, performance requirements, and time-to-market (TTM) commitments have added tremendous pressure on post-silicon validation [2], which is usually the last step prior to volume manufacturing.

Within the server segment, there are conditions that further increase system complexities. These include increased I/O density and serviceability, decreased cost and power consumption, as well as non-flexible form factors [3]. The latter implies that channel lengths remain unchanged, thus turning the problem towards analog circuitry optimization.

One of the major challenges in HSIO electrical validation (EV) is the so called physical layer (PHY) tuning process, where equalization (EQ) techniques are used to cancel any undesired effect, such as transmitter (Tx) jitter, attenuation or inter-symbol interference (ISI), among others [4]-[6]. PHY tuning is one of the most time-consuming processes in post-silicon validation [7], [8]. In addition, when process, voltage, and temperature (PVT) conditions, as well as the multiple channels and devices or add-in cards are considered, the tuning complexity increases dramatically.

The current industrial practice to perform PHY tuning is based on an exhaustive or complete enumeration method; it is an empirical procedure based on the expert knowledge of the validation engineers on how the eye diagram is shaped. The method consists of maximizing either the functional eye diagram on the receiver (Rx) based on the system margining response [9] or the jitter tolerance (JTOL) measurements [10] and then doing a trade-off to arrive at a single set of EQ coefficient values that satisfy both test scenarios. Due to the large number of electrical parameters, the number of PHY tuning settings, the number of system margin measurements required, and the long JTOL test time, finding the best set of EQ coefficients for margining and meeting the JTOL mask is challenging and very time consuming [11].This process is usually performed on a small sample of silicon units due to the very long time typically required; however, once the best settings are obtained, the parameters are checked on a larger sample size to verify their validity. In order to overcome the limitations aforementioned, new techniques

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to optimize the EQ coefficients are required.

In this paper, we describe a holistic optimization approach that merges system margining and jitter tolerance measurements to optimize the Rx analog circuitry during industrial post-silicon validation. Our methodology concurrently optimizes Rx system margins and JTOL, by defining an objective function that combines both type of measurements, and by using a Kriging surrogate-based modeling approach to efficiently perform optimization. The proposed method is able to deliver optimal system margins and guarantee jitter tolerance compliance while substantially decreasing the typical post-silicon validation time.

This work corresponds to an extended version of [12]. Here we present a detailed description of system margining and jitter tolerance measurements and how they are used for PHY tuning. We also provide a detailed mathematical development of the objective function and the Kriging surrogate-based modeling. In contrast to [12], here we illustrate our methodology by optimizing the Rx tuning on three different HSIO links, including USB3, SATA3 and PCIe3, on a real industrial validation platform. In all the examples, we demonstrate the efficiency of our method to deliver optimal margins while ensuring jitter tolerance compliance. Our results show a substantial improvement for both system margins and jitter tolerance as compared with the current industrial practice, as well as a dramatic reduction of the typical time required for PHY tuning.

The paper is organized as follows. Section 2 offers a summary of silicon validation. Section 3 describes the PHY tuning process. Section 4 provides a description of system margining. Section 5 defines the JTOL tests. The objective function formulation is presented in Section 6 and the surrogate model and optimization technique are described in Section 7. Section 8 shows the case studies where our holistic approach was tested, and finally Section 10 presents our conclusions.

2 Silicon Validation

Functional verification of modern embedded systems has become a huge task because of the increasing system complexity [13]. It requires tens or hundreds of person-years and needs the computing power of thousands of workstations. Despite this tremendous effort, it is virtually impossible to detect and fix all bugs in the design before it tapes-out. Given the highly time-sensitive nature of the semiconductor industry, waiting for exhaustive tests is clearly a failing economic approach, even before considering the expense associated with testing silicon [14].

Silicon validation involves pre-silicon and post-silicon validation techniques. The later considers operating hundreds of manufactured silicon samples in actual application environments to validate a correct behavior across specified operating conditions and industrial standards; it implies electrical validation (EV) to check for robustness of the design under test by performing measurements on both Rx and Tx circuitry of the HSIO links. These measurements have to comply with electrical standards and ensure that the design can operate under worst stressing conditions. The ultimate goal of HSIO post-silicon electrical validation is to statistically predict the I/O behavior in a real system environment over lots of dies and operating conditions. Such a prediction leads to a reasonable production release qualification (PRQ) decision.

3 PHY Tuning

Modern nanometric transistor technologies exhibit larger die-to-die process variations. In addition, board impedances, channel losses, add-in cards, end-point devices, etc., also present important variations, which are compounded by the changing operating conditions, mainly voltage supply and temperature. All these factors cause large variations in the performance of I/O links.

During validation, we may observe a failure that requires debugging. Ideally, we root-cause the bug and fix it by re-designing. However, this approach is inefficient and costly. In practice, instead of re-designing the circuit, many link failures can be fixed by modifying the PHY tuning settings, which are usually embedded in the I/O links and can be digitally adjusted. They provide a way to reconfigure I/O links in post-silicon to cancel out the effects of system channels' variability. PHY tuning settings include, among others: parameters of an equalizer at the Tx, Rx, or both; the clock and data recovery (CDR) circuit settings; the variable gain amplifier (VGA); and the bias voltages or currents values. A typical system may have hundreds of combinations of just equalization parameter values. Finding the optimal PHY tuning settings that guarantee the bit error ratio (BER) required by an industrial specification is called PHY tuning. In the worst case, this means sweeping all possible combinations of all PHY settings, which is prohibitive in the post-silicon validation time frame [15].

More specifically, PHY tuning aims at finding the combination of EQ settings that maximizes the functional eye diagram and simultaneously passes the JTOL mask under the system variability caused by multiple factors, e.g., signal integrity phenomena, process variation, channel losses, power supply noise, thermal effects, etc. As mentioned before, the current industrial approach is based on exhaustive enumeration methods to first improve the system margins and then a trade-off to pass the jitter tolerance compliance test. This empirical approach heavily depends on the expert knowledge of the validation engineers.

4 System Margining

System margin validation (SMV) is a methodology for verifying the signal integrity of a circuit board and assessing how much margin is in the design relative to silicon characteristics and processes that vary over time, including voltage, temperature, frequency, humidity, and component aging, among other factors. The intent of SMV is to ensure the silicon parts meet the industry specifications, and their operation is robust across frequency, voltage, temperature, and manufacturing process variations.

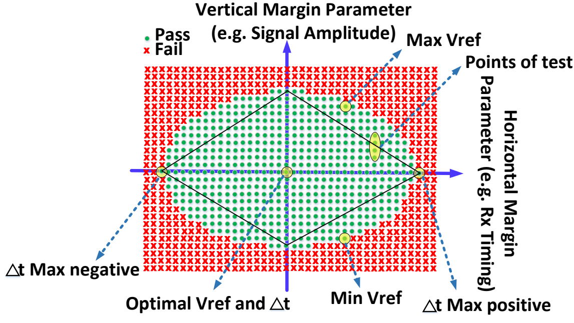

Fig. 1. Functional eye diagram based on SMV.

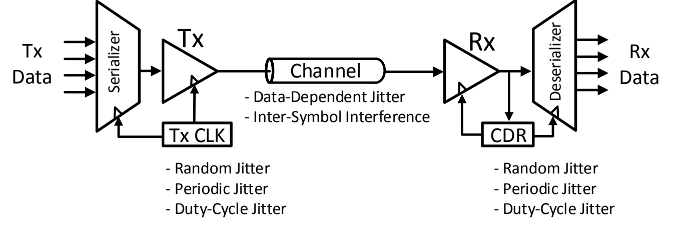

Fig. 2. Jitter sources in a HSIO link.

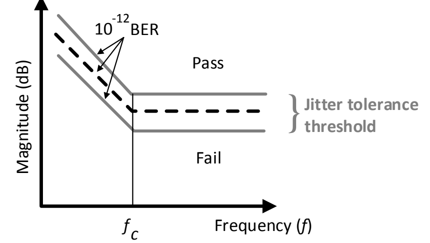

Fig. 3. Rx jitter tolerance threshold for testing.

The fundamental process behind the SMV consists of systematically adjusting the corner conditions under which the validation platform operates, then measure the Rx functional eye opening by using on-die design for test (DFT) features. The DFT circuitry is able to send data traffic through the device under test (DUT) link, while monitoring reception errors. The next step is to sweep margin parameters to verify the system stability. Some examples of sweep margin parameters include: signal amplitude, timing parameters of the Rx circuit, I/O buffer impedance, and I/O buffer voltage references.

During SMV, the DFT circuitry varies the voltage threshold and the sampling point relative to time (phase interpolation) while errors are checked at each margin parameter setting. The resulting pass/fail matrix yields the solution space in which the system can operate without failure, as shown in Fig. 1. The resulting graph, known as functional eye diagram, resembles the eye diagram seen on a traditional oscilloscope. In Fig. 1 the horizontal axis provides timing margin (eye-width), while the vertical axis indicates voltage margin (eye height). We aim at maximizing the area of this functional eye diagram by using equalization to achieve optimum electrical margining of the HSIO interconnects.

5 Jitter Tolerance Testing

Typical jitter sources in HSIO links that contribute to the overall accumulated jitter at the Rx are illustrated in Fig. 2. A non-ideal clock synthesizer within the Tx block induces jitter. ISI, reflections and crosstalk also degrade the signal integrity depending on the quality of the channel. At the Rx side, non-ideal equalizers and PLL-inherent phase noise on the CDR will additionally induce jitter [16]-[19]. Despite these conditions, the Rx must be capable of decoding the incoming signals for correct link communication.

One of the most common ways to measure the performance of a HSIO link is by measuring the BER through the HSIO link [20]. The fewer the errors measured, the better the performance of the link. BER measurement is typically used to characterize the Rx JTOL performance in order to determine compliance with the industry standard specifications such as XAUI [21], PCIe [22], USB [23], and SATA [24]. Most HSIO protocols require a BER in the range from 10^{-12} to 10^{-15}.

The goal for Rx JTOL is to verify that it can operate at a target BER when operating under worst case signaling conditions. JTOL testing consists on verifying that the measured Rx clock-recovery tolerance across frequencies is above the target threshold. If the measured JTOL curve is above the threshold curve, it indicates a passing result, thus the Rx can tolerate some more jitter. On the other hand, if the measured curve is below the threshold curve, it indicates a failing result. Both scenarios are shown in Fig. 3 [25], where f_c is the corner frequency in the jitter mask that defines two different areas: the in-band and the out-band jitter. The single inflection point at f_c in the curve comes from the dominant pole in the Rx's CDR PLL loop filter implementation [25].

JTOL for HSIO requires validating the BER against standards specifications, but measuring at a 10^{-12} target is very time consuming, since it takes several minutes to perform a BER test [26], [27]. Measurement time depends on the link data rate and the required BER. In addition, JTOL is usually measured across a range of frequencies to determine the frequency response of the device. The quantity of data bits N needed to guarantee a target BER at a certain statistical confidence level [28], [29], is

$$N = \frac{1}{B}\left[-\ln(1-a)+\ln\left(\sum_{k=0}^{E}\frac{(N\times B)^k}{k!}\right)\right] \quad (1)$$

where B is the desired BER level, a specifies the confidence level of having a BER less than or equal to B, and E is the number of detected errors during measurements. Assuming a confidence level of 95% (a = 0.95), then it is necessary to transmit N = 3×10^{12} bits without errors in order to meet a BER = 10^{-12}. In a SATA3 link this translates to a time per testing point of

$$\text{time} = \frac{N}{\text{speed}} = \frac{3\times10^{12}}{6\times10^{9}} = 500\,\text{sec} = 8.3\,\text{min} \quad (2)$$

Therefore, the measurement time for a complete set of JTOL values can take a long time depending on the conditions. Such a large test time to perform a single BER test is not feasible for PHY tuning or for high volume production testing. The test time problem becomes much worse when taking into considerations that many design parameters and DUT settings can affect the JTOL performance.

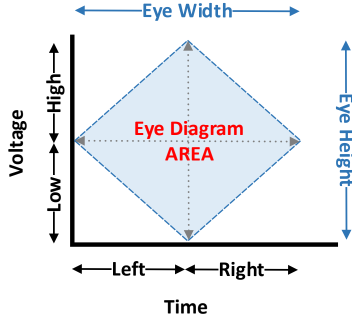

Fig. 4. Graphical representation of the objective function based on the functional eye diagram area.

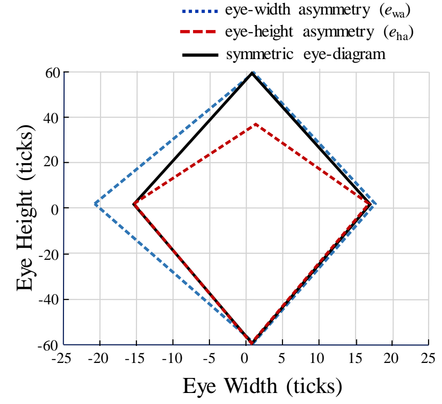

Fig. 5. Asymmetries of the functional eye diagram.

6 Objective Function Formulation

Here we describe the development of our PHY tuning objective function for optimizing system margins ensuring jitter tolerance compliance.

Let $\boldsymbol{R}_m \in \Re^2$ denote the electrical margining system response, which consists of the eye width e_w and eye height e_h of the functional eye diagram,

$$\boldsymbol{R}_m = \boldsymbol{R}_m(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = \begin{bmatrix} e_w(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \\ e_h(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \end{bmatrix} \tag{3}$$

This electrical margining system response depends on the PHY tuning settings $\boldsymbol{x}$ (EQ coefficients), the operating conditions $\boldsymbol{\psi}$ (voltage and temperature), and the devices $\boldsymbol{\delta}$ (silicon skew and external devices). $e_w \in \Re$ and $e_h \in \Re$ are obtained from measured parameters,

$$e_w(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = e_{wr}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) + e_{wl}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \tag{4}$$

$$e_h(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = e_{hh}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) + e_{hl}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \tag{5}$$

where $e_{wr} \in \Re$ and $e_{wl} \in \Re$ are the eye width-right and eye width-left measured parameters, respectively, and $e_{hh} \in \Re$ and $e_{hl} \in \Re$ are the eye height-high and eye height-low parameters, respectively, as illustrated in Fig. 4.

We want to find out the optimal set of PHY tuning settings $\boldsymbol{x}$ to maximize the functional eye diagram area which is a function of e_w and e_h. Therefore, our initial objective function is given by

$$u(\boldsymbol{x}) = [e_w(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})][e_h(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})] \tag{6}$$

Based on the operating conditions and devices, the eye diagram can be decentered with respect to the eye-width, eye-height or both. A well centered Rx eye diagram is required to have a proper sampling on the CDR. The better Rx data is aligned, the easier the phase interpolator circuitry will track for edges on the recovered data. Therefore, the objective function must consider the asymmetries of the eye diagram, as illustrated in Fig. 5.

Let e_{wa} and e_{ha} be the eye-width asymmetry and eye-height asymmetry, respectively. They are defined as

$$e_{wa}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = |e_{wr}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) - e_{wl}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})| \tag{7}$$

$$e_{ha}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = |e_{hh}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) - e_{hl}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})| \tag{8}$$

The area of the eye diagram and the asymmetries must be scaled by weighting factors w_1, w_2, $w_3 \in \Re$ such they become comparable. The values of these weighting factors depend on the operating conditions and devices, and they can be selected by using initial e_w and e_h measurements.

Therefore, the objective function is now defined as

$$u(\boldsymbol{x}) = w_1[e_w(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})][e_h(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})] - w_2[e_{wa}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})] - w_3[e_{ha}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})] \tag{9}$$

with w_1, w_2, and w_3 calculated from

$$w_1 = \frac{3}{\frac{1}{n}\sum_{i=1}^{n}[e_w(\boldsymbol{x}^{(i)})][e_h(\boldsymbol{x}^{(i)})]} \tag{10}$$

$$w_2 = \frac{1}{\frac{1}{n}\sum_{i=1}^{n} e_{wa}(\boldsymbol{x}^{(i)})} \tag{11}$$

$$w_3 = \frac{1}{\frac{1}{n}\sum_{i=1}^{n} e_{ha}(\boldsymbol{x}^{(i)})} \tag{12}$$

where $\boldsymbol{x}^{(i)}$ are n randomly distributed base points for initial measurements of eye width and eye height.

The optimization problem for system margining is

$$\boldsymbol{x}^* = \arg\max_{\boldsymbol{x}} u(\boldsymbol{x}) \tag{13}$$

with $u(\mathbf{x})$ defined by (9).

We will now modify the optimization problem such that the optimal set of EQ coefficients maximizes the eye diagram and exceed the JTOL mask.

The JTOL system response is denoted by vector function $\boldsymbol{R}_J$ and consists of measurements of the sinusoidal jitter amplitude $\boldsymbol{S}_{JA}$ over a frequency range of interest (see Fig. 3),

$$\boldsymbol{R}_J = \boldsymbol{R}_J(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = \boldsymbol{S}_{JA}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \tag{14}$$

The new optimization problem can be defined through a constrained formulation,

$$\boldsymbol{x}^* = \arg\max_{\boldsymbol{x}} u(\boldsymbol{x}) \quad \text{subject to } \boldsymbol{g}(\boldsymbol{x}) \le \boldsymbol{0}, \tag{15}$$

with

$$\boldsymbol{g}(\boldsymbol{x}) = \boldsymbol{S}_{JAspec} - \boldsymbol{S}_{JA} \tag{16}$$

where $\boldsymbol{S}_{JAspec}$ is the the JTOL specification mask.

A more convenient unconstrained formulation can be defined by adding a penalty term, as

$$U(\boldsymbol{x}) = u(\boldsymbol{x}) - r_0^g \|\boldsymbol{G}(\boldsymbol{x})\|_2^2 \tag{17}$$

where $\boldsymbol{G}(\mathbf{x})$ is the JTOL penalty function defined as,

$$\boldsymbol{G} = \max\{\boldsymbol{0}, \boldsymbol{g}(\boldsymbol{x})\} \tag{18}$$

The optimal solution depends on the value of $r_0^g \in \Re$, which is a penalty coefficient defined as,

$$r_0^g = \frac{|u(\boldsymbol{x}_0)|}{\|\boldsymbol{g}(\boldsymbol{x}_0)\|_2^2} \tag{19}$$

In summary, our holistic objective function to optimize system margining and meeting the JTOL mask is

$$\boldsymbol{x}^* = \arg\max_{\boldsymbol{x}} U(\boldsymbol{x}) \tag{20}$$

with

$$U(\boldsymbol{x}) = w_1[e_{\mathrm{w}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})][e_{\mathrm{h}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})] - w_2[e_{\mathrm{wa}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})] - w_3[e_{\mathrm{ha}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})] - r_0^g\|\boldsymbol{G}(\boldsymbol{x})\|_2^2 \tag{21}$$

7 Surrogate Model and Optimization

To solve (20), we follow a surrogate-based optimization strategy. As the underlying modeling technique, we select Kriging [30] given its adequacy for dealing with multiple optima and non-continuous responses. Our implementation exploits the Matlab Kriging toolbox DACE [31]. To enhance the efficiency of our approach, we apply design of experiments (DOE) for selecting fitting points.

7.1 Design of Experiments

DOE is a set of statistical methods for allocating points in the design space with the objective to maximize the amount of useful information. In our case, we take measurements from the system at these points to create the training data set that is subsequently used to construct the surrogate model. When sampling the points, there is a clear trade-off between the number of points used and the amount of information that can be extracted from these points. The samples are typically spread apart as much as possible in order to capture global trends in the design space [32].

In our case, we selected a low discrepancy sequence algorithm for DOE to cover the non-uniformity of data points sequence by using the Sobol sequence [33], [34]; thus we guarantee to cover the space as uniformly as possible for the number of points we choose.

7.2 Kriging Surrogate Model

Kriging is a surrogate modeling technique to approximate deterministic data. It has proven to be very useful for tasks such as optimization [35], design space exploration, visualization, prototyping, and sensitivity analysis [36]. A detailed mathematically description of Kriging is given in [37] and [38]. The popularity of Kriging has generated research in many areas, including several extensions to Kriging to handle different problem settings, e.g. by adding gradient information in the prediction [39], or by approximating stochastic simulations [40].

It is named after the pioneering work of D.G. Krige (a South African mining engineer), and was formally developed in [41]. Then [42], [30], and [35] made it popular in the context of the modeling, and optimization of deterministic functions, respectively. The Kriging method in its basic formulation estimates the value of a function at some unsampled location as the sum of two components, the linear model (e.g., polynomial trend) and a systematic departure representing low (large scale) and high frequency (small scale) variation components, respectively.

Kriging considers both the distance and the degree of variation between known data points when estimating values in unknown areas. A kriged estimate is a weighted linear combination of the known sample values around the point to be estimated. Applied properly, Kriging allows to derive weights that result in optimal and unbiased estimates. It attempts to minimize the error variance and set the mean of the prediction errors to zero so that there are no over- or under-estimates.

A unique feature of Kriging is that it provides an estimation of the error at each interpolated point, providing a measure of confidence in the modeled surface.

In this work, we use ordinary Kriging [43] that estimates a deterministic function f as

$$f_p(\boldsymbol{x}) = \mu + \varepsilon(\boldsymbol{x}) \tag{22a-c}$$

$$E(\varepsilon) = 0$$

$$\mathrm{cov}(\varepsilon(\boldsymbol{x}^i), \varepsilon(\boldsymbol{x}^j)) \neq 0 \forall i, j$$

where μ is the mean of the response at base points ($\boldsymbol{x}$), and ε is the error with zero expected value, and with a correlation structure being a function of a generalized distance between the base points.

A possible correlation structure [42] is given by

$$\mathrm{cov}(\varepsilon(\boldsymbol{x}^i), \varepsilon(\boldsymbol{x}^j) = \sigma^2 \boldsymbol{R} \tag{23}$$

where σ^2 is the variance, and $\boldsymbol{R}$ is the correlation n x n matrix between the base points

$$\boldsymbol{R} = \begin{bmatrix} R(\boldsymbol{x}^1,\boldsymbol{x}^1) & R(\boldsymbol{x}^1,\boldsymbol{x}^2) & R(\boldsymbol{x}^1,\boldsymbol{x}^N) \\ R(\boldsymbol{x}^2,\boldsymbol{x}^1) & R(\boldsymbol{x}^2,\boldsymbol{x}^2) & R(\boldsymbol{x}^1,\boldsymbol{x}^N) \\ \vdots & \vdots & \vdots \\ R(\boldsymbol{x}^N,\boldsymbol{x}^1) & R(\boldsymbol{x}^N,\boldsymbol{x}^1) & R(\boldsymbol{x}^N,\boldsymbol{x}^N) \end{bmatrix} \tag{24}$$

We use a Gaussian correlation function of the form

$$R(\boldsymbol{x}^i,\boldsymbol{x}^j) = \exp[-\sum_{k=1}^{N}\theta_k|\boldsymbol{x}_k^i - \boldsymbol{x}_k^j|^2] \tag{25}$$

where θ_k are unknown correlation parameters used to fit the model, while $\boldsymbol{x}_k^i$ and $\boldsymbol{x}_k^j$ are the kth components of the base points $\boldsymbol{x}^i$ and $\boldsymbol{x}^j$, and N denotes the number of dimensions in the set of design variables $\boldsymbol{x}$, σ identifies the standard deviation of the response at sampled design points.

The Kriging-based surrogate model $\boldsymbol{R}_s$ is defined as

$$\boldsymbol{R}_s(\boldsymbol{x}) = [R_{s.1}(\boldsymbol{x}) \ldots R_{s.m}(\boldsymbol{x})]^T \tag{26}$$

The model estimates the responses at unsampled points by the Kriging predictor [42] by

$$R_{s.j}(\boldsymbol{x}) = \overline{\mu}_j + \boldsymbol{r}^T(\boldsymbol{x})\boldsymbol{R}^{-1}(\boldsymbol{f}_j - \boldsymbol{1}\overline{\mu}_j) \tag{27}$$

where $\boldsymbol{1}$ denotes an N-vector of ones, and

$$\boldsymbol{f}_j = [R_{sm.j}(\boldsymbol{x}^1) \ldots R_{sm.j}(\boldsymbol{x}^N)]^T \tag{28}$$

The bar above the variables denotes estimates, $\boldsymbol{r}$ identifies the correlation vector between the set of prediction points $\boldsymbol{x}$ and the base points,

$$\boldsymbol{r}^T(\boldsymbol{x}) = [R(\boldsymbol{x},\boldsymbol{x}^1) \ldots R(\boldsymbol{x},\boldsymbol{x}^N)]^T \tag{29}$$

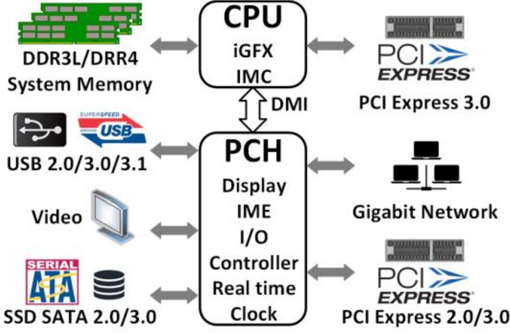

Fig. 6. Block diagram of the platform controller hub (PCH).

The mean $\bar{\mu}_j$ is the estimated value of μ_j and can be calculated using

$$\bar{\mu}_j = \frac{\mathbf{1}^T \mathbf{R}^{-1} \mathbf{f}_j}{\mathbf{1}^T \mathbf{R}^{-1} \mathbf{1}} \tag{30}$$

The unknown parameter θ_k, for the Kriging model can be estimated by maximizing the following likelihood function $g(\mathbf{R})$ given by [43]

$$g(\mathbf{R}) = -\frac{N}{2}\ln(\bar{\sigma}^2) - \frac{1}{2}\ln|\mathbf{R}| \tag{31}$$

in which the variance

$$\bar{\sigma}_j^2 = \frac{1}{N}(\mathbf{f}_j - \mathbf{1}\bar{\mu}_j)^T \mathbf{R}^{-1}(\mathbf{f}_j - \mathbf{1}\bar{\mu}_j) \tag{32}$$

and $|\mathbf{R}|$ are both functions of θ_k.

7.3 Optimization using the Surrogate Model

Once the Kriging model is built using a set of training data, the parameters of the model have to be estimated to give the best fit to the training data. After finding an optimum design by the Kriging model, this design evaluation (infill point) has to be added to the training data set. Then the Kriging parameters have to be re-estimated and again re-search the model. This process is iterated until we reach the convergence criteria: 1) maximum number of iterations reached, 2) maximum number of functions evaluations reached, or 3) difference between model responses and measurements is small enough. Our surrogate-based optimization procedure solves (20) using objective function (21). For optimization, we use the DACE toolbox that employs the *fmincon* optimization routine from Matlab optimization toolbox.

8 Test Cases

The proposed surrogate-based optimization method was applied on a single random unit for each interface, at nominal voltage and temperature conditions. However, the general validity of the optimal parameters obtained was later verified following the traditional coverage in analog post-silicon validation, that includes a large volume of silicon units considering process variations as well as full-range voltage and temperature conditions. We are using an Intel server platform, comprised mainly of a CPU and a platform controller hub (PCH). The PCH is a family of Intel microchips which integrates a range of common I/O blocks required in many market segments, and these include USB [23], PCI Express [22] controller, SATA [24], SD/SDIO/MMC, and Gigabit Ethernet MAC, as well as general embedded interfaces such as SPI, I²C, UART, and GPIO. The PCH also provides control data paths with the Intel CPU through direct media interface (DMI), as shown in Fig. 6. Within the PCH, our methodology was tested on three different HSIO links: USB3 Super-speed Gen 1, PCIe gen3, and SATA3.

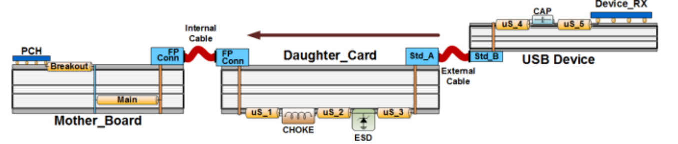

Fig. 7. USB3 Rx channel topology.

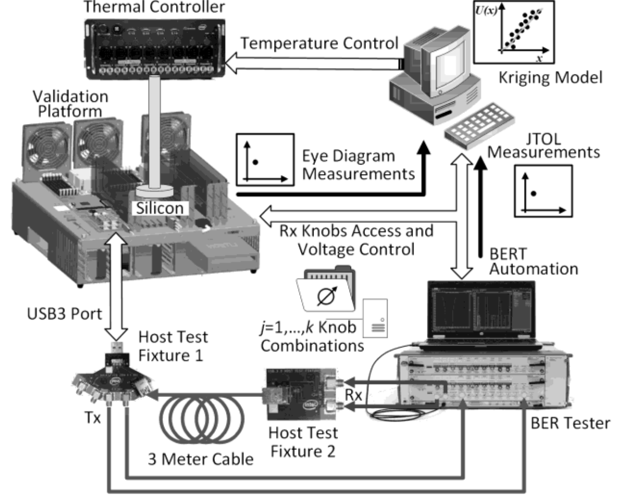

Fig. 8. The holistic methodology test setup for USB3 system margining and JTOL optimization. Figure taken from [12]

As mentioned before, the complexity of HSIO buses used on Intel server platforms are exacerbated by the interaction of channel components characteristics, such as packages, PCB, input/output density, connectors, cables and devices, as well as its intrinsic elements such as insertion loss (IL), signal to noise ratio (SNR), high volume manufacturing (HVM) variations, temperature and humidity impact on IL, etc. Several channel optimizations, including flexible routing [44] hybrid PCB stack-up [45], crosstalk cancellation [46], and impedance mismatch [47], are utilized to mitigate the aforementioned complexity. Despite the use of these techniques during platform design, the Rx of each interface still needs to be tuned for optimal performance during post-silicon validation time frame.

8.1 Test Case 1: USB3

In the case of USB3, the channel topology is comprised of the Tx driver, the Tx based board transmission lines (TL), several via transitions, an I/O card connector, an internal cable that attaches a daughter card, followed by an external cable at which is attached at the other end another connector for the Rx I/O card, followed by another set of TL, and DC blocking capacitors at the Rx side of the device. Its simplified topology is illustrated in Fig. 7. The bandwidth limitations and inherent non-idealities of this system essentially result from the large amount of interconnects. Hence, we are looking to optimize the Rx

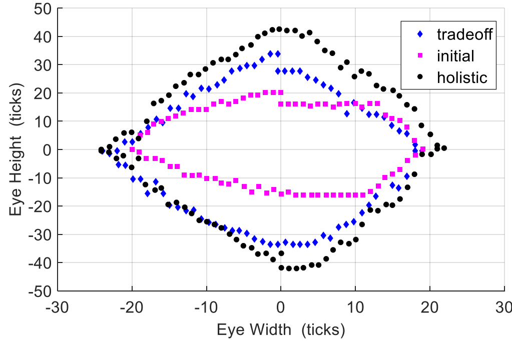

Fig. 9. USB3 eye width versus eye height results: comparing the proposed methodology against the initial design and the trade-off approach. Figure taken from [12].

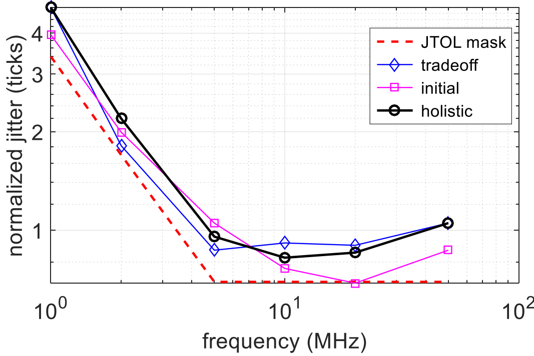

Fig. 10. USB3 JTOL testing results: comparing the proposed methodology against the initial design and the trade-off approach. Figure taken from [12].

equalization coefficients as a way to compensate for the channel limitations.

Fig. 8 illustrates the test setup specific for USB3. We stress the Rx with a BER tester, sending a compliant pattern including all jitter impairments as per specification. The host computer is capable of modifying Rx EQ coefficients and DFT circuitry of the DUT as well as sending commands to the BER tester to sweep the injected jitter amplitude and frequencies. Then, we measure system margins and JTOL and record results for each set of Rx EQ coefficients.

Following the surrogate-based optimization methodology described in Section 7 to solve problem (20) that uses the objective function (21) as a figure of merit, an optimal set of EQ coefficient values was found. The set of values found were verified by measuring the Rx inner eye height/width as well as JTOL using a commercial device. The EQ settings obtained through our proposal showed an improvement of 125% on eye diagram area as compared to the initial EQ settings, and a 32% improvement as compared with the traditional (tradeoff) approach, as shown in Fig. 9. Similarly, the JTOL results show a substantial improvement with margins well above the specification limit template, as seen in Fig. 10. The efficiency of this approach was also demonstrated by a significant time reduction on post-Si validation: while the traditional process requires days for a complete optimization, the method proposed here can be completed in a few hours.

8.2 Test Case 2: SATA3

A similar scenario to the USB3 topology is found in the

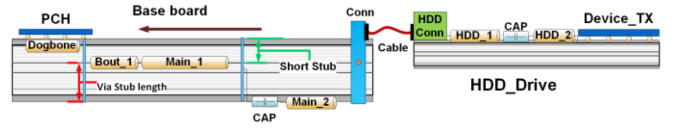

Fig. 11. SATA3 Rx channel topology.

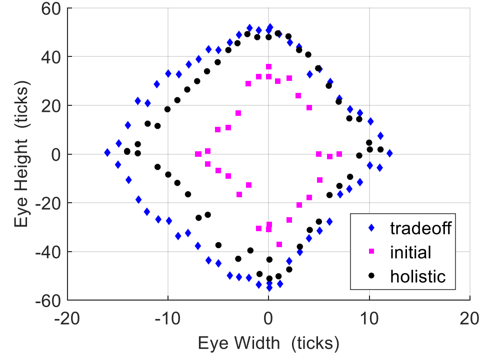

Fig. 12. SATA eye width versus eye height: comparing the proposed methodology against the initial design and the trade-off approach.

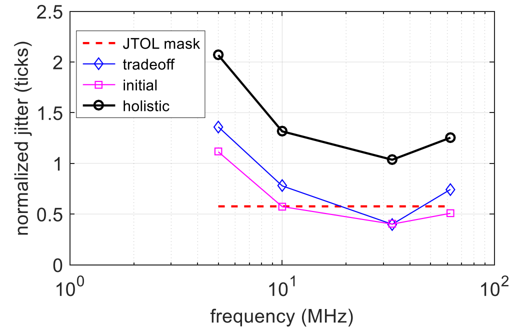

Fig. 13. SATA JTOL results: comparing the proposed methodology against the initial design and the trade-off approach.

SATA3 channel, which also includes board TLs, several via transitions and I/O card connectors, however, a 1 m SATA cable is used to connect the base board to the device I/O card, as illustrated in Fig. 11. Fig. 8 also applies in general to the test setup used for SATA3, with the exception of replacing the respective test fixtures and switching the 3 m cable for a SATA3 compliance interconnect channel.

The eye diagram area measured when using the EQ coefficients obtained through our holistic methodology show a 182% improvement against the initial values, as depicted in Fig. 12. The tradeoff approach derives a slightly larger eye area than the one obtained with our proposal. However, the JTOL results from the tradeoff approach fall below the spec mask at 33 MHz, as seen in Fig. 13, rendering a compliance failure. Thus, it is clear in the SATA3 case that with our holistic approach both the eye diagram and the JTOL margins are optimized. Furthermore, the execution following our proposal took less than 30% of the time required for the tradeoff approach to reach a passing solution for both type of measurements.

8.3 Test Case 3: PCIe

Figure 14 shows the PCIe topology implemented. As in the previous test cases, the PCIe topology includes the Tx driver, the base board TLs and via transitions. It also

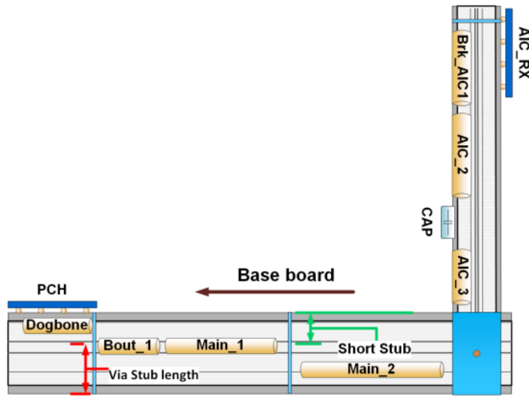

Fig. 14. PCIe Gen3 Rx channel topology.

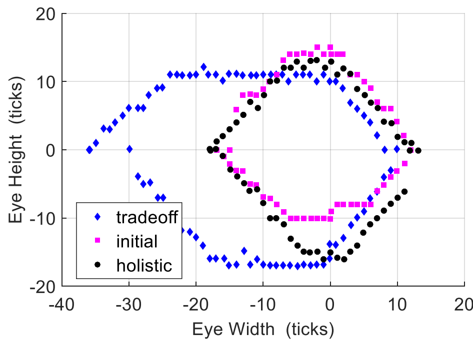

Fig. 15. PCIe eye width versus eye height: comparing the proposed methodology against the initial design and the trade-off approach.

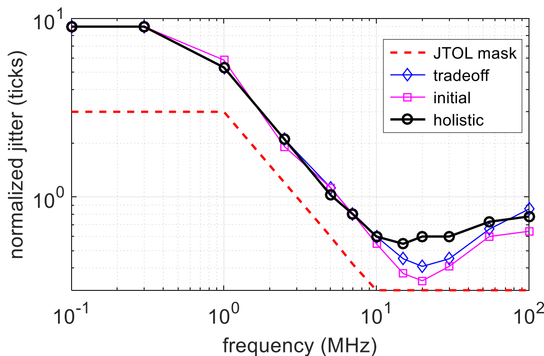

Fig. 16. PCIe JTOL results: comparing the proposed methodology against the initial design and the trade-off approach.

includes a slot connector and an add-in card in which TLs and other internal devices are found. In the PCIe test setup, a compliance load board is used to connect the measuring instruments, as seen in Fig. 14, instead of the test fixtures and cables shown in Fig. 8 for USB3 and SATA3.

Results from the PCIe test case provide a clear example of the role of asymmetries in the objective function discussed in Section 6. Fig. 15 shows the PCIe functional eye diagram results, where the smallest area is obtained with the initial Rx EQ coefficients. The area obtained with our holistic approach is 14% larger than the area measured with the initial Rx EQ settings. The center of both of these eyes is located near the 0-tick value in both axis, thus the width and height asymmetry values are low. The area obtained from the tradeoff approach is the largest from the three eyes, however, the large asymmetry seen on the horizontal axis could eventually lead to system failures (see Fig. 15). Additionally, the JTOL results obtained with our holistic approach show the largest margins with respect to the specification limits, as shown in Fig. 16. As with the other two test cases, validation time was significantly decreased using our holistic approach, in this test case by up to 70% with respect to the traditional trade-off approach.

9 Conclusion

Product complexity, performance requirements, and TTM commitments are adding tremendous pressure on post-silicon validation. In this scenario, validation teams are continuously looking for opportunities to make validation faster and cheaper. In this paper we demonstrated a holistic optimization approach that merges system margining and jitter tolerance measurements for PHY tuning during industrial post-silicon validation. Our method uses Kriging to build a surrogate model for efficient optimization, and a novel objective function based on system margining and jitter tolerance measurements. Our experimental results, tested on three different HSIO links on a real industrial validation platform, demonstrated the efficiency of our method to deliver optimal margins while ensuring jitter tolerance compliance, showing a substantial improvement for both system margins and jitter tolerance as compared with the current industrial practice, and dramatically accelerating the typical time required for PHY tuning.

Acknowledgment

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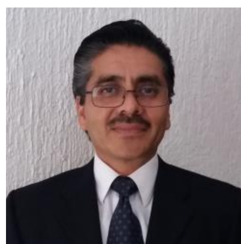

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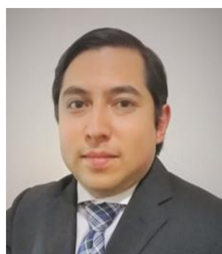

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