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Power Delivery Network Impedance Profile and Voltage Droop Optimization

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***Abstract* — The design process of power delivery networks (PDN) in modern computer platforms is becoming more relevant and complex due to its relationship with high-frequency effects on signal integrity. When circuits start operating, the changing current flowing through the PDN produces fluctuations creating voltage noise. Unsuccessful noise control compromises data integrity. A suitable PDN design approach is the use of decoupling capacitors to lower the impedance profile and mitigate current surges, ensuring a small variation in the power supply under significant transient current loads. An optimization approach to determine the number of decoupling capacitors in a PDN is presented, aiming at decreasing the amount of decoupling capacitors without violating the PDN design specifications, looking at both the impedance profile in the frequency domain and the resulting voltage droop in the transient time-domain.**

***Keywords* — power delivery network, power integrity, noise control, impedance profile, voltage droop.**

I. Introduction

A power delivery network (PDN) consists of all the devices and interconnects that distribute the electrical power supply (biasing voltages) and return the electrical current throughout a board of an electronic system. Voltage regulator modules (VRM) distribute voltage to the various active devices and need to provide a steady power supply at a desired DC voltage level with an acceptable noise level or ripple. However, when the signals at different on-board modules of a PDN start switching, they cause current surges that create voltage noise (fast voltage transitions) on the pads of the on-board modules, introducing high-frequency components. As explained in [1], unsuccessful noise control on the PDN will cause the amplitude of the eye diagram in the vertical direction to collapse due to the voltage noise. Additionally, the signal flowing to a reference plane will increase skin and proximity effects (due to the high-frequency components), increasing jitter due to dispersion and further reducing the eye opening. This leads to functional failures in the computer platform as internal core circuits suffer setup- and hold-time errors. Some of these common problems can be mitigated by using decoupling capacitors.

Parallel decoupling capacitors are used to lower the impedance magnitude of the power distribution network in order to ensure a small variation in the power supply voltage under a significant current load [2]. Additionally, parallel decoupling capacitors are also used as local sources of charge to mitigate the current surges by quickly supplying current to loads and stabilizing voltage levels [3].

A typical industrial practice in PDN design consists of placing multiple stages of different decoupling capacitors hierarchically. This avoids using a single capacitor stage that would need a high capacitance and at the same time a low parasitic inductance to be effective at maintaining a low impedance at all frequencies. The speed at which the decoupling system provides charge is inversely proportional to the capacitance of the stage and its distance to the load. An adequate distribution of suitable decoupling capacitors allows them to provide a time response significantly shorter as compared to the power supply. In the initial moment when the switching begins, charge is only supplied to the load by the decoupling system until the power supply is activated [3]. Ideally, large amounts of decoupling capacitors are needed to mitigate PDN-related signal integrity problems, at the expense of higher manufacturing costs.

Most of the research work on decoupling capacitors optimization for PDN design has been developed either in frequency-domain or time-domain. For instance, model order reduction (MOR) techniques have been employed to compute the impedance profile and search for optimal locations of the decoupling capacitors [4]. Authors in [5] obtain frequency dependent Poynting vectors and iteratively place decoupling capacitors at the port with maximum Poynting vector. The work done in [6] models the inductive effect of packages and extracts a resistance-capacitance-susceptance model to build a macromodel using MOR techniques; then a simulated annealing algorithm is used to search for the optimal types of decoupling capacitors. Authors in [7] use simulated annealing to minimize the total cost of decoupling capacitors under the constraints of a worst-case voltage noise bound instead of using impedance targets. A surrogate modeling methodology for PDN optimization in transient-domain exploiting machine learning techniques is described in [8].

In this paper, an optimization-based technique to determine the number of parallel decoupling capacitors in a PDN considering simultaneously frequency- and time-domain

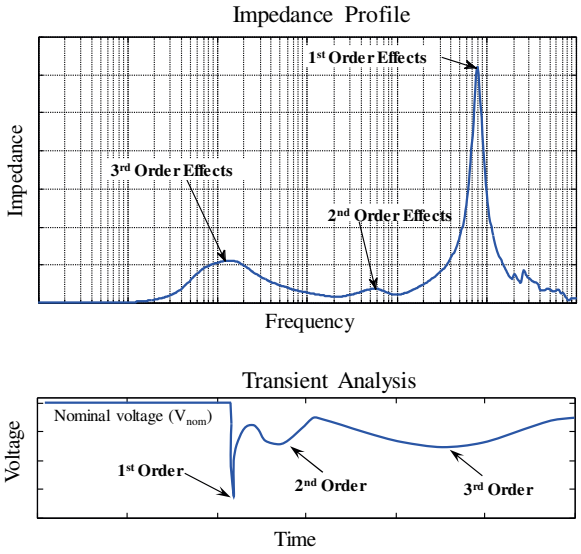


Fig. 1. Typical relationship between PDN frequency-domain impedance profile and transient-domain voltage droop [10],[8].

performances is presented. Several optimization experiments are conducted to reduce as much as possible the number of decoupling capacitors and in consequence, the overall PDN cost, without violating the PDN target impedance and transient voltage design specifications.

II. PDN Frequency- and Time-Domain Performances

The most relevant frequency-domain performance of a PDN is its impedance profile. Fig. 1 illustrates a typical PDN impedance profile, where some frequency resonances are normally present, with a large resonance at high frequency caused by the die and package parasitics. The ideal target impedance profile should be as low and flat as possible across all frequencies. However, designing a PDN that complies with such ideal target impedance can be too expensive given the high number of capacitors needed. Additionally, reducing the large resonance at high frequencies would imply a redesign at the package and die levels, which can be extremely expensive.

Furthermore, multiple capacitors of different magnitude placed in parallel can result in sharp anti-resonant impedance peaks [9]. These peaks can magnify noise problems when

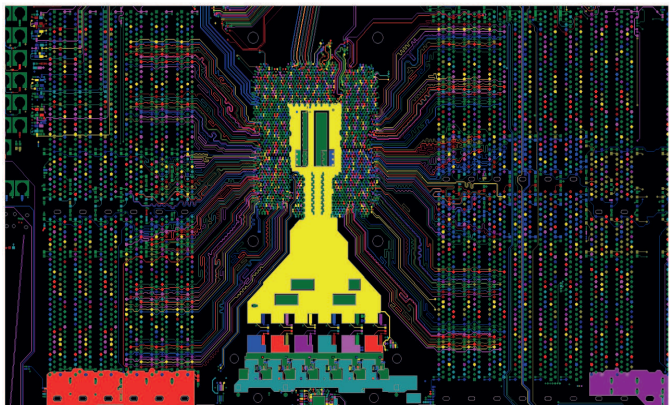


Fig. 2. Power delivery network (PDN) layout of an Intel® Xeon® platform (courtesy of Intel®).

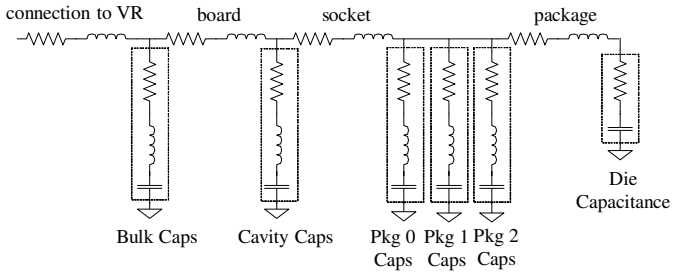


Fig. 3. Lumped equivalent circuit of the Power Delivery layout schematic of Intel® Xeon® platform.

current transients contain considerable components at frequencies close to those resonant peaks. Frequency-domain effects will then translate into time-domain as voltage droops at different stages, potentially causing operational errors or failures [10]. This relationship is also illustrated in Fig. 1. The first voltage droop is typically driven by the on-die capacitance, on-die resistive parasitics, and the package connections. The second droop is dominated by package capacitance and sometimes the connector pins. The third droop is usually caused by the voltage regulator capacitance and the bulk capacitance nearby. The tolerance to the droop events depends on their magnitude and duration; as the droop events get larger and in a longer time, signal integrity becomes compromised, and thus the need for limiting the droop events.

III. Representing the PDN Structure

For argument sake, we consider the PDN of a dual data rate (DDR) memory interface of an Intel® Xeon® server platform. Fig. 2 shows a portion of the PDN platform layout. The yellow section is the power delivery network under study, corresponding to the VCCIN net. Other colors represent other DDR networks.

Each component in the PDN has a different impedance associated with it, which causes voltage variations as the transient current passes through them. The PDN structure can be modeled in a limited frequency band by simple lumped RLC circuits [11]. Different types of capacitors and lumped models circuits are typically used in designing a PDN [12]. Bulk capacitors are the biggest in the PDN and are used to provide low impedance at the frequency at which the VRM is not able to do so. They are effective from 1 KHz to 1 MHz and typical values range from hundreds to thousands of µF. Cavity capacitors are located under the cavity of the package and range from a few to tens of µF and are effective at higher frequencies, up to several MHz. Package capacitors are slightly smaller and are effective at higher frequencies, up to several hundred MHz.

Fig. 3 shows the equivalent lumped model extracted from the PDN layout. This lumped circuit is used in the following optimization approaches.

IV. Optimization of a PDN Combining Frequency- and Time-Domain Effects: First Approach

We now optimized the number of decoupling capacitors

using as design specifications a maximum target impedance of 2.4 mΩ for frequencies lower than f_H = 28.8 MHz, a minimum target impedance of 1.02 mΩ for frequencies lower than f_{H2} = 2 MHz, and a minimum voltage specification of 0.8 V for the voltage transient pulse.

The optimization problem uses a minimax formulation as

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} \left\{ \ldots e_k(\boldsymbol{x}) \ldots \right\} \tag{1}$$

where the k-th error function is given by

$$e_k = \begin{cases} \dfrac{|Z_{11}|(\boldsymbol{x})}{2.24\ \text{m}\Omega} - 1 & \text{for } f_k \le f_H \\ 1 - \dfrac{|Z_{11}|(\boldsymbol{x})}{1.02\ \text{m}\Omega} & \text{for } f_k \le f_{H2} \\ 1 - \dfrac{V_{\text{pulse}}(\boldsymbol{x})}{0.8\ \text{V}} \\ L_B - N_{\text{BulkCap}} \\ L_B - N_{\text{CavityCap}} \\ L_B - N_{\text{Pkg0Cap}} \end{cases} \tag{2}$$

where f_k is the k-th simulated frequency point, and L_B is the limiting lower bound in the number of capacitors.

To reduce the number of design optimization variables, we only consider the Bulk, Cavity, and Pkg 0 decoupling capacitors, since previous studies on the circuit provided the insight as to the capacitors with the largest effects on the circuit responses. Pkg 1 and Pkg 2 capacitors were left at the minimum of 1 for all seeds excepting seed 3, where we explore the optimization with twenty Pkg 1 capacitors. All capacitors of the same type have the same capacitance and parasitics.

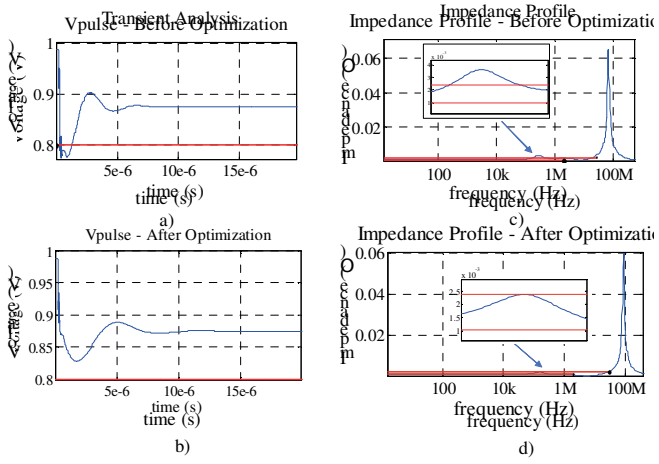
We used the Nelder-Mead optimization algorithm to solve (1). The optimization was able to meet the voltage and impedance requirements with some seeds. However, with several seeds the algorithm failed, finding in some cases an infinite amount of capacitors. In those cases, the optimization ends by exceeding the maximum number of iterations or objective function evaluations allowed.

V. Optimization of a PDN Combining Frequency- and Time-Domain Effect: Second Approach

The error function in (2) was modified to add a constraint U_B for the maximum number of capacitors allowed, in this case U_B = 140 (only considering the Bulk, Cavity, and Pkg 0 capacitors). The optimization was done with the same seed values as in Section IV.

$$e_k = \begin{cases} \dfrac{|Z_{11}|(\boldsymbol{x})}{2.24\ \text{m}\Omega} - 1 & \text{for } f_k \le f_H \\ 1 - \dfrac{|Z_{11}|(\boldsymbol{x})}{1.02\ \text{m}\Omega} & \text{for } f_k \le f_{H2} \\ 1 - \dfrac{V_{\text{pulse}}(\boldsymbol{x})}{0.8\ \text{V}} \\ L_B - N_{\text{BulkCap}} \\ L_B - N_{\text{CavityCap}} \\ L_B - N_{\text{Pkg0Cap}} \\ (N_{\text{BulkCap}} + N_{\text{CavityCap}} + N_{\text{Pkg0Cap}}) - U_B \end{cases} \tag{3}$$

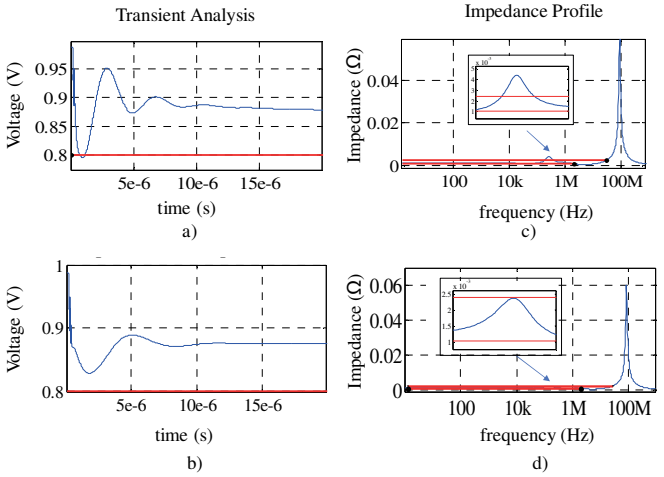
Fig. 4 shows the results with seed 1; the optimization successfully meets the voltage and impedance requirements with 142 capacitors in total. Fig. 5 shows results with seed 2; the optimization was also successful with only 141 capacitors in total. Fig. 6 shows the results for seed 3; the optimization was successful in meeting all the requirements with 152 capacitors. Finally, Fig. 7 shows the results for seed 4; the



	Bulk	Cavity	Pkg0	Pkg1	Pkg2	Total
Seed	1	20	20	1	1	43
Optimized	2	64	74	1	1	142

e)

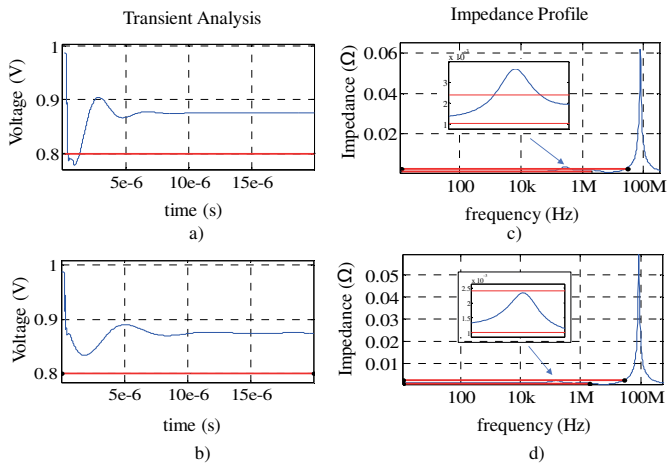
Fig. 4. Results for seed 1: a) voltage pulse before optimization; b) voltage pulse after optimization; c) impedance before optimization; d) impedance after optimization; e) seed and optimized values.



	Bulk	Cavity	Pkg0	Pkg1	Pkg2	Total
Seed	40	20	80	1	1	142
Optimized	1	63	75	1	1	141

e)

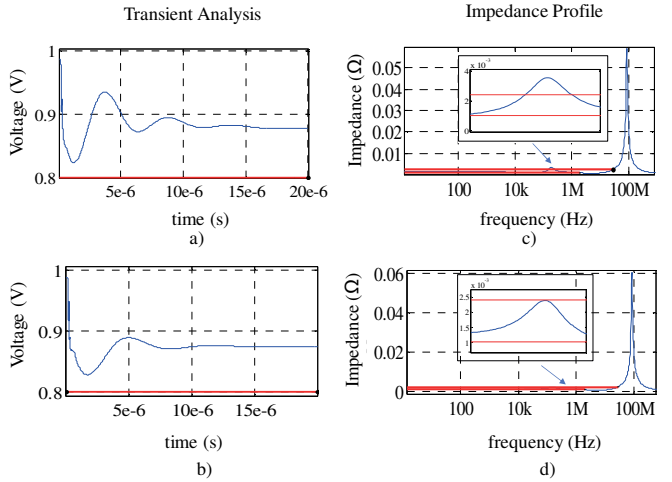
Fig. 5. Results for seed 2: a) voltage pulse before optimization; b) voltage pulse after optimization; c) impedance before optimization; d) impedance after optimization; e) seed and optimized values.



	Bulk	Cavity	Pkg0	Pkg1	Pkg2	Total
Seed	1	20	20	20	1	62
Optimized	3	70	58	20	1	152

e)

Fig. 6. Results for seed 3: a) voltage pulse before optimization; b) voltage pulse after optimization; c) impedance before optimization; d) impedance after optimization; e) seed and optimized values.



	Bulk	Cavity	Pkg0	Pkg1	Pkg2	Total
Seed	35	40	80	1	1	157
Optimized	1	62	73	1	1	138

e)

Fig. 7. Results for seed 4: a) voltage pulse before optimization; b) voltage pulse after optimization; c) impedance before optimization; d) impedance after optimization; e) seed and optimized values.

optimization was successful in meeting all requirements with only 138 capacitors, even though total number of capacitors used for the seed was larger than the 140 allowed for the Bulk, Cavity, and Pkg 0 capacitors.

Using the error function in (3), the optimization algorithm gave much better results than using (2), obtaining lower amounts of capacitors and yielding a more robust formulation.

We also found in all cases that the optimal PDN design requires a few Bulk capacitors. Additionally, when adding more Pkg 1 capacitors in the seed, more total capacitors were needed to meet the requirements. Optimizing the Cavity and Pkg 0 capacitors, while keeping Pkg 1 and Pkg 2 capacitors at the minimum amount, was enough to meet both the frequency- and time domain design specifications.

VI. Conclusion

An optimization approach to determine the number of capacitors in a power delivery network was presented. Several optimization efforts were done to optimize the PDN, aiming at decreasing the number of decoupling capacitors without violating the PDN design specifications, looking at both the impedance profile in the frequency domain and the resulting voltage droop in the transient domain. We found better results by limiting the amount of design variables. Also, by limiting the maximum total number of capacitors we were able to minimize the number of capacitors yielding a PDN that satisfies the target impedance and minimum voltage supply specifications.

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