Development and RF-Performance of AlGaN/GaN and InAlN/GaN HEMTs on Large-Diameter High-Resistivity Silicon Substrates

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***Abstract*— A CMOS-compatible industrial processing and RF analysis of 150 mm GaN-on-HR-Si substrates with AlGaN and InAlN barrier is presented. Process development along with transfer to large-wafer scale is shown and some HEMT calibration devices produced on AlGaN/GaN following the aforementioned procedure are characterized in terms of RF-performance by using a set of measured multi-bias S-parameters. An automatic small-signal equivalent circuit extraction strategy for these AlGaN/GaN DUTs is validated and some de-embedded figures of merit, namely $f_T \approx 20$ GHz and $f_{max} \approx 41$ GHz are drawn out for initial evaluation of the technology.**

***Keywords*— Aluminium Gallium Nitride (AlGaN), Indium Aluminium Nitride (InAlN), High Resistivity Silicon (HR-Si), High-Electron Mobility Transistor (HEMT) and Large-Diameter.**

I. Introduction

High Electron Mobility Transistors (HEMTs) based on III-V nitride hetero-structures, due to their advantageous Johnson and Baliga figures of merit (FoM), are widely recognized as attractive high-performance transistor families for microwave power amplifier applications [1], [2]. The highly conductive 2-dimensional electron gas (2DEG) channel can be induced in either conventional AlGaN/GaN or more recent InAlN/GaN hetero-structures, and the devices can be grown on a variety of hosting semiconductor substrates [3]. While low-resistivity Si is the typical substrate of choice for mass market-oriented consumer applications such as switched-mode power converters, and transistors are scaled for high current and high blocking voltages, high-resistivity (HR) substrates such as SiC with its high thermal conductivity or native GaN with its perfect lattice match are popular substrates for transistors optimized for maximum cut-off frequencies through short gate lengths and short extrinsic drain and source access regions. This paper focuses on the use of large-diameter (150 and 200 mm) HR-Si wafers as the underlying substrate hosting the AlGaN/GaN and InAlN/GaN HEMTs oriented towards microwave applications [4]. Such a substrate presents a good trade-off between cost efficiency through large-diameter low-cost Si wafers and advantageous low-loss properties at microwaves bands. In view of evaluating the radio-frequency (RF) performance of the GaN-on-HR-Si HEMT devices, it has been developed and presented a small-signal vectorial network analysis of a test field hosting on-wafer calibration structures and several scaled transistor devices optimized for high frequency performance in terms of the lateral device structure. This document is split into three main parts: wafers processing, HEMT small-signal modeling (for a de-embedding based on these parameters), and RF-validation.

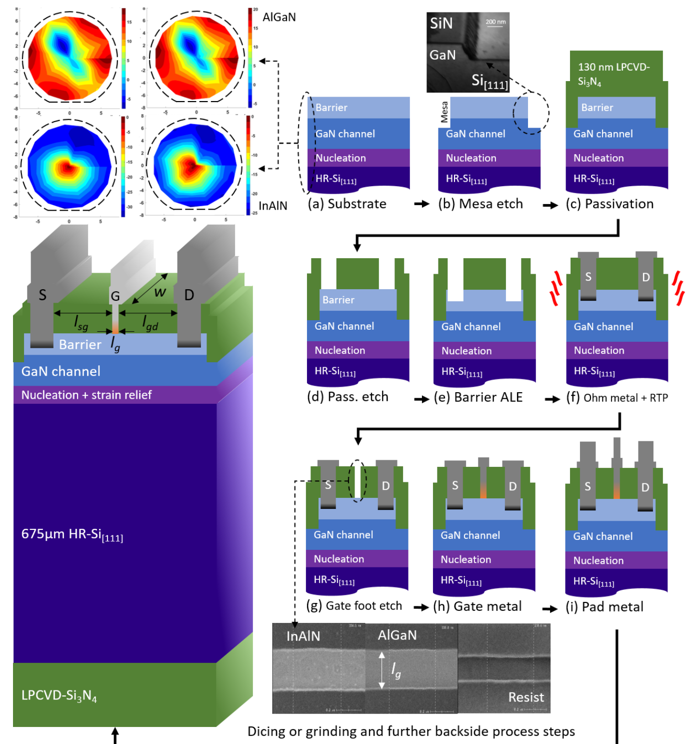

Fig. 1. Schematic of RF device manufacturing steps on AlGaN/GaN and InAlN/GaN wafers. The SEM (Scanning Electron Microscope) insets shows detailed cross-sections and top-down pictures of the individual process steps. The final devices structure (on the left) shows the relevant HEMT dimensions.

II. The GaN-Based RF Process

The devices introduced for this work are fabricated in a CMOS-compatible manner at IMS CHIPS™ cleanroom facility [3]. The RF process, generally described in Fig. 1

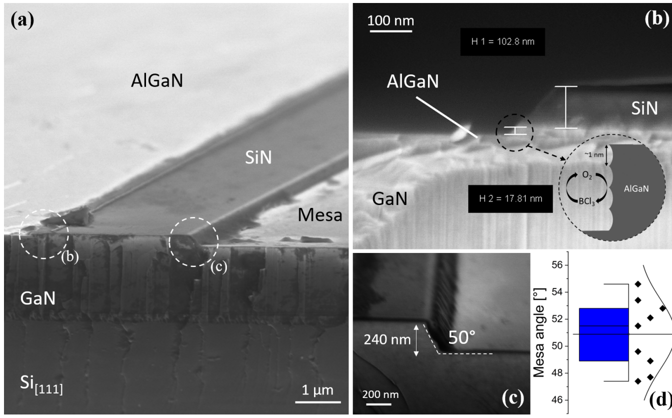

Fig. 2. (a) SEM cross-section of the device edge on a AlGaN/GaN substrate showing ohmic recess and Mesa region covered with LPCVD-Si_3N_4. Detail (b) shows the ohmic region with ALE process inset. Detail (c) shows a magnification of the Mesa edge with an angle of 50°, which is the mean of the (d) Mesa angle distribution.

diagram is executed on 150 mm Enkris™ GaN-on-HR-Si substrates featuring both, AlGaN and InAlN barriers. The substrates are specified with a thickness of 675 µm, a 2DEG sheet resistance less than 400 Ω/□ and a 2DEG density larger than $8{\cdot}10^{12}$ 1/cm² and $1{\cdot}10^{13}$ 1/cm² for AlGaN and InAlN barrier, respectively. After substrate bow investigation (Fig. 1a), device processing starts with Mesa formation using Cl-based inductively coupled plasma (ICP) reactive ion etching (RIE) in Oxford Instruments Plasma-Pro 100 Cobra™ (Fig. 1b) to achieve electric isolation (Fig. 2a, c and d). Mesa angle is 50° and allows good edge coverage of the following low-pressure chemical vapor deposition (LPCVD), which is used to passivate the surface with Si_3N_4 (Fig. 1c).

In the next step, the passivation is opened by SF_6-based ICP RIE (Fig. 1d). Following this, atomic layer etching (ALE) [5] with alternating steps of oxidation and BCl_3 oxide etch is used to recess the barrier layer damage-free and condition the surface prior to metal deposition (Figs. 1e and 2b). GaN surface conditioning and recess contact optimization will be discussed in more detail later. Ti/Al stack (10/200 nm) evaporation follows in a Leybold UNIVEX 900™[1].

The metal stack is structured by lift-off technique and the ohmic contacts are formed by low-temperature rapid thermal processing (RTP) annealing (Fig. 1f). Gate foot etching is done with the above mentioned etching process (Fig. 1g). After cleaning, Ni/Ti/Al gate stack (50/10/500 nm) is evaporated and structured using lift-off (Fig. 1h). To allow probe card measurements, a final Ti/Al pad (10/750 nm) is deposited in the same manner (Fig. 1i).

A. *Ohmic Contact Formation*

As referred above, recess ohmic contacts are used in the RF process. Barrier recessing is done by O_2/BCl_3 ALE in a digital, self-limiting approach [5]. Ohmic contacts are characterized by transmission line measurement (TLM) structures (inset of Fig.

[1]Tool used for all similar process steps.

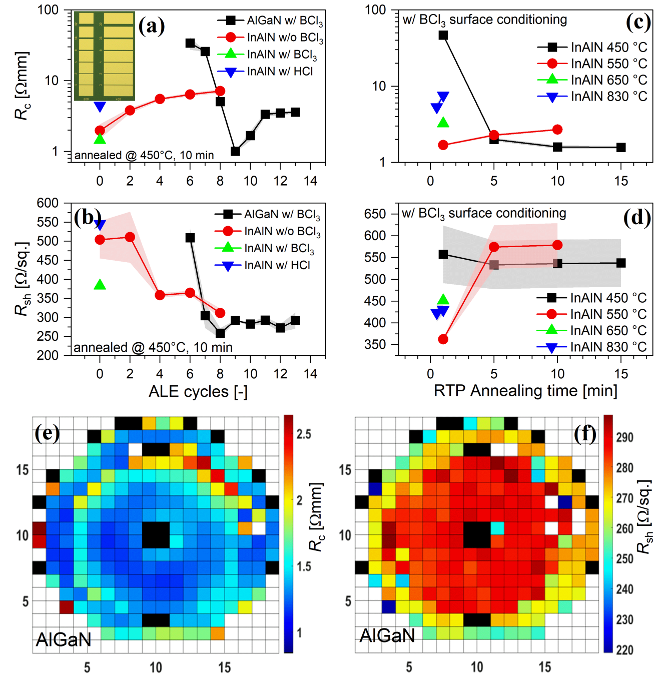

Fig. 3. Recess ohmic contact experiments using ALE on wafers with AlGaN and InAlN barrier: (a) Contact resistance (R_c) and (b) sheet resistance (R_{sh}) for contacts annealed at 450°C for 10 min at different ALE cycles and surface conditioning. To further optimize the InAlN contact, a temperature series (c, d) was done at different temperatures and times. All contacs were formed with Ti/Al (10/200 nm) metal stacks. Wafer maps of (e) R_c and (f) R_{sh} of the optimized AlGaN ALE process show transferability to full-wafer size with high uniformity.

3a) to extract the contact (R_c) and the sheet resistance (R_{sh}). The metal stack used for all contacts is Ti/Al (10/200 nm).

Ohmic contact optimization is done by piece-wise etching different number of ALE cycles followed by surface conditioning. In the case of AlGaN barrier, the optimal etching depth is 9 cycles followed by BCl_3 surface conditioning with a value of 1 Ω·mm (Fig. 3a). A cross-section of recessed AlGaN contact region is depicted in Fig. 2b. Deeper etching results in further R_c increase, while R_{sh} remains constant at 285 Ω/□ (Fig. 3b). In contrast to this, any recessing done on InAlN leads to higher R_c values. Instead of optimizing the recess depth, surface conditioning (Fig. 3a) and annealing temperature (Fig. 3c) is optimized for InAlN. BCl_3 conditioning resulted in the lowest InAlN R_c of 1.4 Ω·mm at 383 Ω/□ (Fig. 3d). HCl conditioning, in contrast, does not improve the contact, but leads to higher R_c and R_{sh} values. InAlN contact annealing optimization was done by annealing at different temperatures and times. The optimal conditions for annealing are found at 450 °C for longer than 10 min, similar to AlGaN contact.

Recess optimization of AlGaN contacts can successfully be transferred to full-wafer size with high uniformity of R_c (Fig. 3e) and R_{sh} (Fig. 3f). The measured R_{sh} is in good agreement with the supplier's specification.

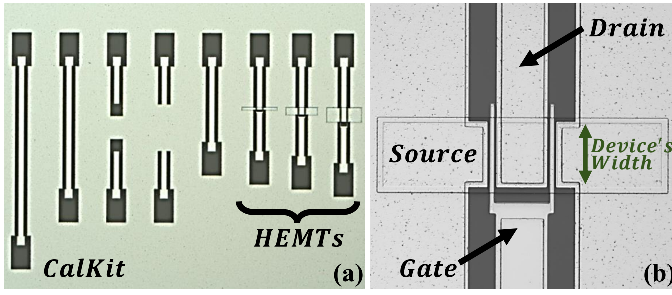

Fig. 4. (a) "CalField" layout including the TRL cal-kit (on the left) together with the AlGaN/GaN HEMTs for several w_g and l_g values (on the right). In (b), the two gate-fingers device by the microscope view.

III. CalField Design & Testing

A. Layout & Physical Specifications

In an effort to characterize the process technology at microwave and millimeter-wave frequencies, the RF-oriented AlGaN/GaN test structures were implemented into a calibration field (the so-called "CalField") on 150 mm HR-Si substrates, as shown in Fig. 4a. Six coplanar two-finger transistor devices, scaled both in terms of gate width (w_g = 10, 30, 60 µm per finger) and gate length (l_g = 1, 0.75, 0.5, 0.25 µm), are complemented by several on-wafer *Thru-Reflect-Line* (TRL) calibration structures including 760 and 560 µm *Lines*, and one 180 µm *Open*, *Short* and *Thru*.

Some intrinsic dimensions to be highlighted would be the drain-gate and source-gate distances of $l_{dg} = l_{sg} = 2$ µm, and the source-drain space of $l_{sd} = l_g + l_{dg} + l_{sg}$. These small sizes becoming a key factor in order to achieve modern high-speed and high-power transistors by downscaling the physical geometry to reduce transit times and to minimize the power dissipation [4]. The two gate-fingers structures displayed in Fig. 4b are considered for a width normalization.

The embedding into a coplanar (CPW) contact pad and access line environment with a characteristic impedance of 50 Ω allows for precise measurements at microwave frequencies using VNA equipment. The coplanar contact pads use a closed ground reference surrounding the signal pad in order to limit the coupling of the port-incident and port-leaving waves to neighboring structures during on-wafer measurements. The length of all HEMT's access lines is identical and matches the on-wafer TRL structures in order to allow shifting the reference plane of the S-parameter calibration directly to the transistor devices' in- and output, eliminating the need for further de-embedding procedure.

Alternatively, a conventional off-wafer calibration using an Impedance Standard Substrate (ISS) with de-embedding of the pads and access lines can be used[2]. The gate and drain bias points during the small-signal S-parameter measurements are provided by off-wafer bias tees from the VNA DC-input.

The dedicated set-up for the multi-bias S-parameters measurements includes the HP8510C™ network analyzer, an external power supply (up to 32 V pre-bias per channel), the

[2]Both TRL and ISS calibrations were implemented with similar results, however, the measurements were a little less rippled at high frequency with the ISS. Therefore, the presented results were achieved with the ISS calibration together with a specific open-short de-embedding strategy for the access lines.

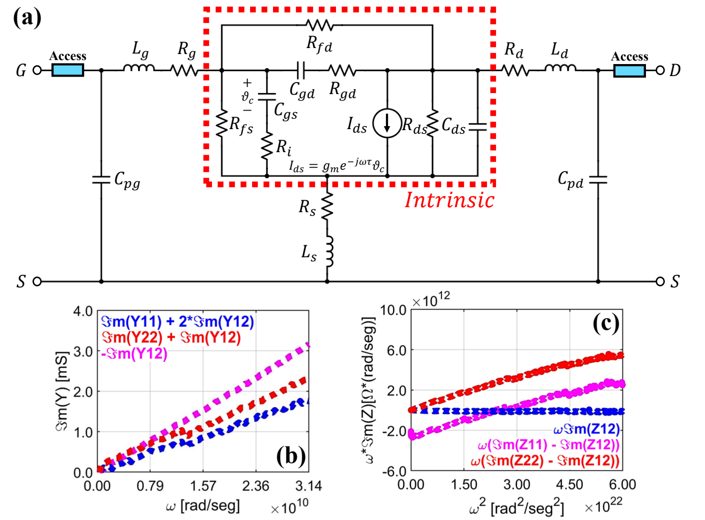

Fig. 5. (a) Small-signal 18-element AlGaN/GaN HEMT equivalent circuit, and resulting graphs for parasitic (b) capacitances and (c) inductances extraction.

Table 1. AlGaN/GaN HEMT Model Parameters from 0.05 to 38 GHz.

*Parasites. Note that (a) and (b) DC-points belong to Fig. 6†					
Bias	C_{gd} [fF]	C_{gs} [fF]	R_i [Ω]	R_{ds} [Ω]	R_{gd} [Ω]
(a)	140.00	168.00	14.24	176.56	20.63
(b)	27.40	172.00	11.32	734.48	66.67
Bias	C_{ds} [fF]	g_m [mS]	τ [psec]	R_{fs} [kΩ]	R_{fd} [kΩ]
(a)	28.60	0.44	1.23	3.44	3.71
(b)	43.40	23.00	2.18	1.62	1.84
*C_{pg} = 40.90 fF C_{pd} = 13.40 fF L_g = 99.20 pH L_s = 1.44 pH					
L_d = 101.00 pH R_g = 10.07 Ω R_d = 6.88 Ω R_s = 1.30 Ω					
†*Optimized results for a* w_g = 60 µm and l_g = 0.25 µm device					

S9i Leica™ Microscope for controlling the overtravel, and two Ground-Signal-Ground 100 µm-pitch FormFactor™ probes ("S" width = 35 µm) which fits the access-point width.

B. Modeling Strategy Road to the Intrinsic Plane

Before the S-acquisition, some worthy basic-performance HEMT info was measured (allowing comparation with other foundries, e.g. [6]): I_{DS} ($g_{m(max)}$) ≈ 0.85 A/mm, R_{on} ≈ 3.13 Ω·mm, V_{pi} (pinch-off) ≈ -1.9 V, or V_{Br} (breakdown) ≈ 81 V.

A proper device modelling relies on accessing its intrinsic plane. This way, a suitable de-embedding is required for removing the effects of the undesired parasitic elements of the structure. The small-signal topology (Fig. 5a), which was successfully tested and validated in [7] and includes 8 extrinsic (bias-independent) and 10 intrinsic (bias-dependent) components, has been considered. The extraction method, that starts with the dummy *Short* and *Open* in order to de-embed the access lines, follows three main steps (results in Table 1):

- Estimation pad capacitances at low frequencies (0.05 to 5 GHz) and *cold-pinched-off* (e.g. V_{GS} = -3 V) by the linear fitting of π-model $[Y]$ versus $\omega = 2\pi f$ (Fig. 5b).
- Retrieval of extrinsic inductances (Fig. 5c) and resistances at $V_{GS} = V_{DS} = 0$ V by linear regression of the real and imaginary $[Z]$ versus ω^2 and ω, respectively.
- Use of well-validated intrinsic HEMT proposal of [8].

The parasites resistances could also be found and match in order with the previously commented R_c and $R_{sh} \cdot (L_{access}/W)$.

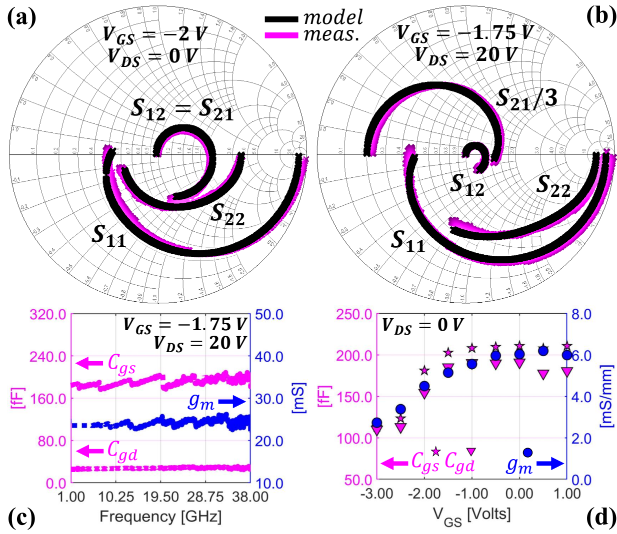

Fig. 6. In (a) and (b), S-parameters from 0.05 to 38 GHz range for a $w_g = 60$ µm and $l_g = 0.25$ µm DUT. (c) Invariant frequency behavior of some intrinsic parameters and (d) bias-dependency of those extracted ones versus V_{GS}.

As shown in Fig. 6a and b, the modeling task was successful for several bias in a range from 0.05 to 38 GHz. The HEMT equivalent circuit was built and simulated on Keysight-ADS™, and the optimization was performed for $M = 801$ frequency samples by minimizing this cost function $((|S_{xy}^{\text{model}} - S_{xy}^{\text{meas}}|)^2)/M \approx 0$ which leads to a *mean relative error* (1) of $\bar{\delta} < 5\%$ for a required slot-time $t_{\text{op}} < 8$ min [7].

$$\bar{\delta}|_{x,y=1,2}[\%] = mean\left(\left|\frac{S_{xy}^{\text{model}}|_M - S_{xy}^{\text{meas}}|_M}{S_{xy}^{\text{meas}}|_M}\right| \cdot 100\right) \quad (1)$$

C. Analysis of the HEMTs RF-Performance

Two major additional ideas are also drawn from the bottom of Fig. 6. On the one hand, Fig. 6c shows the flat-behavior over the frequency of some intrinsic modeled parameters, evidencing the good performance of the technique. On the other hand, according to Fig. 6d, the bias-dependency of some intrinsic ones can be plotted as a preliminary step for an upcoming and more challenging large-signal modeling.

However, at the RF-performance level, the most remarkable information is provided by the Fig. 7. These results are parly shown in Fig. 7a (measured) and b (intrinsic) which include gains and other RF-FoM. Indeed, it is verified that extrinsic $f_T \approx 15$ GHz and $f_{\max} \approx 27$ GHz become in $f_T \approx 20$ GHz and $f_{\max} \approx 41$ GHz at the intrinsic plane, for a $w_g = 60$ µm and $l_g = 0.25$ µm DUT at $V_{GS} = -1.75$ V and $V_{DS} = 20$ V. Moreover, it has been certified that these curves perfectly agree with the extracted HEMT model predictions (Fig. 7b).

Fig. 7c reveals the actual small-signal bias-dependency. Although the gate length behavior has yet to be studied and the wafer processing is still under research, these early RF-results for a $w_g = 60$ µm and $l_g = 0.25$ µm DUTs, including a $f_T \approx 20$ GHz, a $f_{\max} \approx 41$ GHz, a $J_{\text{FoM}} = f_T{\cdot}V_{\text{Br}} \approx 1.62$ THz·V, or an extracted g_m in the order of S/mm, allow optimism in the maduration of this low-losses modern manufacturing procedure for AlGaN/GaN devices on HR-Si substrate technology to satisfy the current state-of-the-art performance [4].

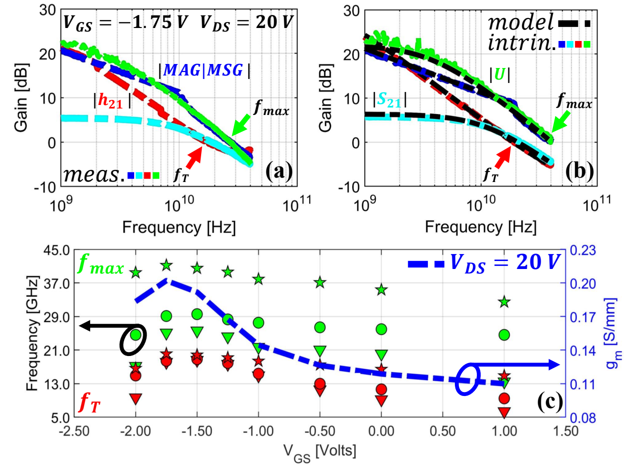

Fig. 7. (a) Measured and (b) de-embedded RF-FoM: $|S_{21}|$ (cyan), Short-Circuit Current Gain (red), Max. Avail. Gain (blue) and Mason's Gain (green) for a $w_g = 60$ µm and $l_g = 0.25$ µm DUT, versus the model (black). (c) $f_{\max}$ (green) and f_T (red) estimation for some bias ($\triangledown$, $\circ$ and $\star$ for $V_{DS} = 5$, 10 & 20 V, respectively), and extracted g_m at $V_{DS} = 20$ V (blue).

IV. Conclusion

A CMOS-compatible manufacturing process of 150 mm GaN-on-HR-Si substrates with AlGaN and InAlN barrier featuring low-temperature ohmic contacts is presented. The produced ohmics achieve $R_c = 1$ Ω·mm with high wafer uniformity. The AlGaN/GaN HEMTs are validated from multi-bias S-parameters and exhibit some intrinsic RF-FoM such as $f_T \approx 20$ GHz or $f_{\max} \approx 41$ GHz. These promising early results pave the way for the industrial development of high performance transistors. For de-embedding and simulations, a small-signal circuit is verified including useful bias-dependencies for large-signal purposes.

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