Machine Learning Techniques and Space Mapping Approaches to Enhance Signal and Power Integrity in High-Speed Links and Power Delivery Networks

José E. Rayas-Sánchez, Francisco E. Rangel-Patiño, Benjamin Mercado-Casillas, Felipe Leal-Romo, and José L. Chávez-Hurtado

***Abstract*— Enhancing signal integrity (SI) and reliability in modern computer platforms heavily depends on the post-silicon validation of high-speed input/output (HSIO) links, which implies a physical layer (PHY) tuning process where equalization techniques are employed. On the other hand, the interaction between SI and power delivery networks (PDN) is becoming crucial in the computer industry, imposing the need of computationally expensive models to also ensure power integrity (PI). In this paper, surrogate-based optimization (SBO) methods, including space mapping (SM), are applied to efficiently tune equalizers in HSIO links using lab measurements on industrial post-silicon validation platforms, speeding up the PHY tuning process while enhancing eye diagram margins. Two HSIO interfaces illustrate the proposed SBO/SM techniques: USB3 Gen 1 and SATA Gen 3. Additionally, a methodology based on parameter extraction is described to develop fast PDN lumped models for low-cost SI-PI co-simulation; a dual data rate (DDR) memory sub-system illustrates this methodology. Finally, we describe a surrogate modeling methodology for efficient PDN optimization, comparing several machine learning techniques; a PDN voltage regulator with dual power rail remote sensing illustrates this last methodology.**

***Index Terms*— Broyden, DDR, DoE, equalization, Ethernet, eye diagram, HSIO, impedance profile, Kriging, parameter extraction, PCIe, PDN, PHY, post-silicon validation, power integrity, SATA, signal integrity, SI-PI co-simulation, space mapping, surrogate, system margining, USB, voltage regulator.**

I. Introduction

High-speed input/output (HSIO) links in current microprocessors are determinant for signal integrity. Undesired high-frequency effects, such as jitter, inter-symbol interference (ISI), crosstalk, and others [1], can create multiple signal integrity (SI) problems in HSIO interfaces, such as Peripheral Component Interconnect Express (PCIe), Serial Advanced Technology Attachment (SATA), Universal Serial Bus (USB), Ethernet, etc., limiting the actual maximum data transfer rates. Given the complexity of such computer platforms, improving SI and reliability requires intensive and time-consuming post-silicon validation rutines, in which a physical layer (PHY) tuning process employing equalization techniques are typically used.

On the other hand, the relationship between SI and power delivery networks (PDN) is becoming crucial in the computer industry. In particular, SI can be severely deteriorated if the transceivers voltage supply is not sufficiently stable, which significantly depends on the PDN, while inadequate SI performance can deteriorate power integrity (PI), making the PDN a key factor in the SI-PI co-design process [2].

In this paper, surrogate-based optimization (SBO) methods, including Broyden-based input space mapping (SM), are applied to efficiently tune receiver (Rx) equalizers (EQ) in HSIO links. By using lab measurements on industrial post-silicon validation platforms, we demonstrate very significant acceleration of the PHY tuning process and substantial enhancement of the corresponding eye diagram margins. Two channel topology interfaces illustrate the proposed SBO/SM techniques: USB3 Gen 1 and SATA Gen 3. Additionally, a computationally efficient method based on parameter extraction (PE) is briefly described to develop fast PDN lumped models exploited for low-cost SI-PI co-simulation. This methodology is illustrated with a dual data rate (DDR) memory sub-system, accelerating current industrial practices. Finally, we briefly describe a surrogate modeling methodology for efficient and reliable PDN optimization, comparing several machine learning techniques: support vector machines, generalized regression neural networks, polynomial surrogate modeling, and Kriging. A PDN voltage regulator with dual power rail remote sensing illustrates this last methodology.

II. Surrogate-based Optimization (SBO) Methods for Post-Silicon Validation and PHY Tuning

A. Eye Diagram Margins and Jitter Tolerance SBO

A holistic formulation to concurrently optimize Rx system margins and jitter tolerance (JTOL) for a USB3 Gen 1 HSIO link is proposed in [3]. This formulation was applied in the post-silicon industrial test setup [4] shown in Fig. 1, whose block diagram for USB3 [5] is in Fig. 2.

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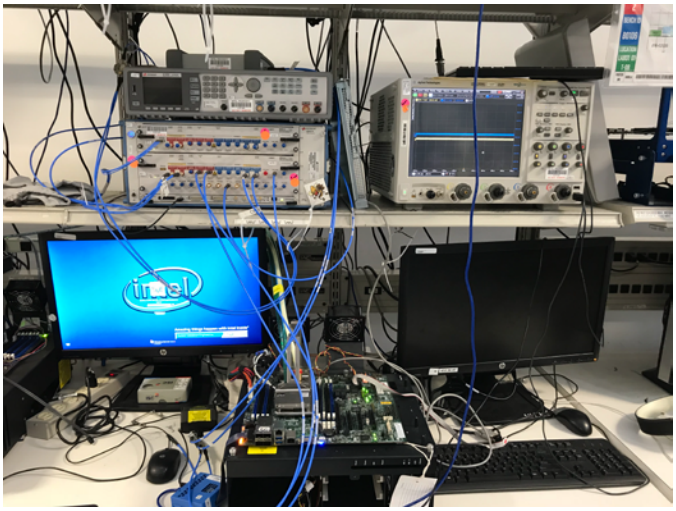

Fig. 1. Industrial test setup for simultaneous system margining and JTOL optimization. Taken from [4].

A BER tester is used to stress the Rx (see Fig. 2). The host computer controls the Rx knobs and sends commands to the BER tester to vary the jitter amplitude and frequencies. System margin validation (SMV) [6] is used to assess how much margin is in the design with respect to silicon processes, voltage, and temperature, by using an on-die test circuitry, while the jitter amplitude is swept at the specification frequencies to obtain JTOL results; a pass/fail criterion is defined from the specification limits (JTOL mask).

The Rx knobs settings are used as optimization variables $\boldsymbol{x}$ for the objective function $U(\boldsymbol{x})$ described in [3]. SBO is applied by exploiting a Kriging model [7] (see Fig. 2) using the Matlab Kriging toolbox DACE [8] and a design of experiments (DoE) approach for data sampling.

The optimal Rx knobs obtained from optimizing the Krigging model are validated by actual measurements of both the Rx eye diagram margins and jitter tolerance. We found an improvement of 175% on eye diagram area as compared to the initial knobs setting, and a 34% improvement as compared with the traditional (tradeoff) approach, as shown in Fig. 3, while the jitter tolerance also improves and is well above the JTOL mask, as seen in Fig. 4. The proposed SBO method can be completed in a few hours, in contrast to the traditional process that requires days for a complete optimization.

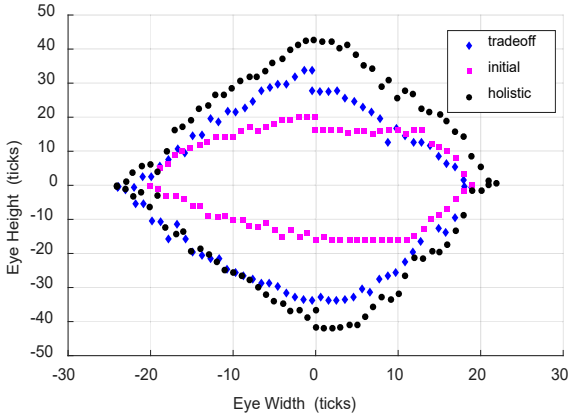

Fig. 3. Eye diagram margins: comparing proposed methodology against the initial design and the trade-off approach. Taken from [3].

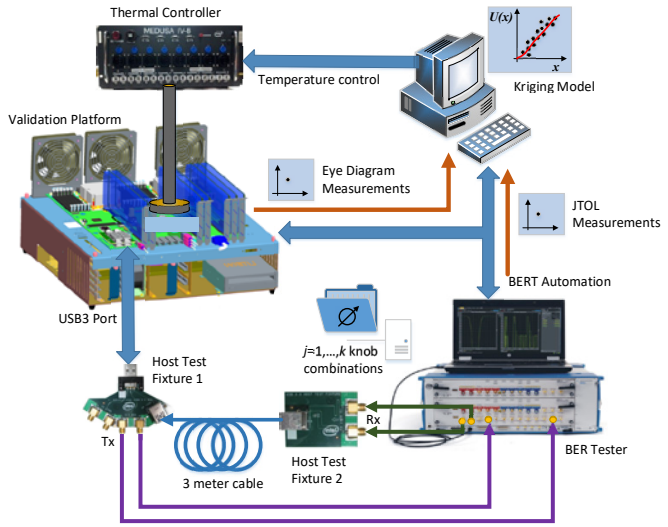

Fig. 2. The holistic methodology test setup for USB system margining and JTOL optimization. Taken from [5].

B. PHY Tuning by Space Mapping

Broyden-based input space mapping (SM), better known as aggressive SM (ASM) [9], [10], is used in [11] to optimize the receiver (Rx) equalizer settings for a SATA Gen 3 interface topology. The fine model is a measurement-based post-silicon validation industrial platform, as illustrated in Fig. 5 (within the PCH, our SM methodology is applied to a HSIO link SATA Gen3), where the fine model responses $\boldsymbol{R}_f$ are the measured eye diagram margins. The coarse surrogate model developed in [12], based on Kriging, is exploited.

SATA Rx PHY tuning EQ coefficients are used as optimization variables $\boldsymbol{x}$. Eye width e_w and eye height e_h are

$$e_w(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = e_{wr}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) + e_{wl}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \quad (1)$$

$$e_h(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = e_{hh}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) + e_{hl}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \quad (2)$$

where e_{wr} and e_{wl} are the eye width-right and eye width-left measured parameters, respectively, and e_{hh} and e_{hl} are the eye height-high and eye height-low parameters, respectively. The margining system response depends on the PHY tuning settings $\boldsymbol{x}$ (EQ coefficients), the operating conditions $\boldsymbol{\psi}$ (voltage and temperature), and the devices $\boldsymbol{\delta}$ (silicon skew and external devices).

Since we aim at finding the optimal PHY tuning settings that maximize the eye diagram margins area, the objective function

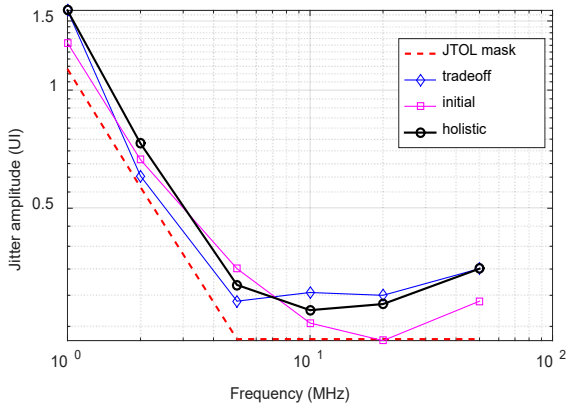

Fig. 4. JTOL testing results: comparing the proposed methodology against the initial design and the trade-off approach. Taken from [3].

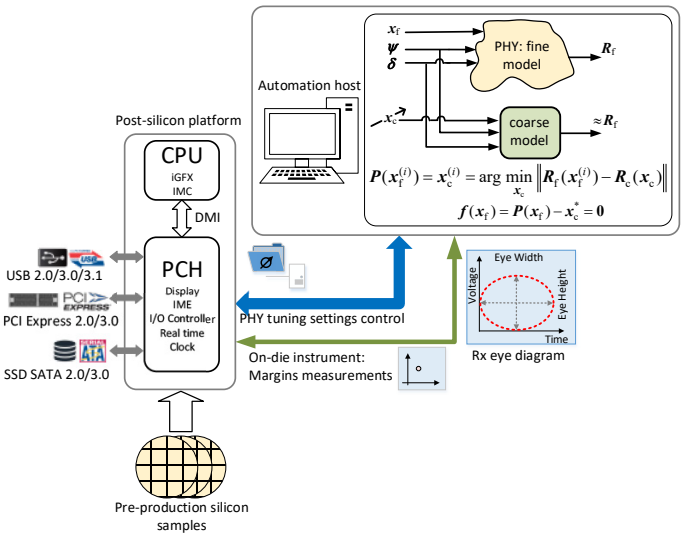

Fig. 5. An Intel server post-Si validation platform using Broyden-based input space mapping design optimization. Taken from [11].

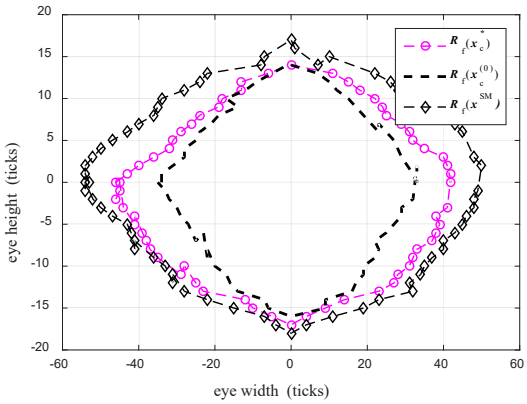

Fig. 6. Comparison between the fine model responses at the initial Rx EQ coefficients, $\boldsymbol{x}_c^{(0)}$, at the optimal coarse model solution, $\boldsymbol{x}_c^*$, and at the space-mapped solution found, $\boldsymbol{x}^{SM}$. Taken from [11].

is defined as

$$u(\boldsymbol{x}) = -\left[e_w(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right]\left[e_h(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right] \quad (3)$$

keeping $\boldsymbol{\psi}$ and $\boldsymbol{\delta}$ fixed during SM optimization.

After applying ASM [10], we obtained a space-mapped solution, $\boldsymbol{x}^{SM}$, in just 6 iterations (or fine model evaluations), making an improvement of 85% on the fine model eye diagram margins area as compared to that one with the initial settings ($\boldsymbol{x}_c^{(0)}$), and a 33% improvement as compared to that one with the optimal coarse model solution ($\boldsymbol{x}_c^*$), as shown in Fig. 6. While the traditional industrial process requires days for a complete empirical optimization, the proposed SM method can be completed in a few hours.

III. PDN Lumped Models for SI-PI Co-Simulation

A low computational cost optimization method based on parameter extraction (PE) to develop efficient PDN lumped models that sufficiently approximate more complex and detailed PDN distributed models is proposed in [13]. The resultant PDN lumped model can be used in an efficient SI-PI analysis and co-design. This approach allows identifying the PDN quality of a dual data rate (DDR) memory sub-system, assessing its impact on SI.

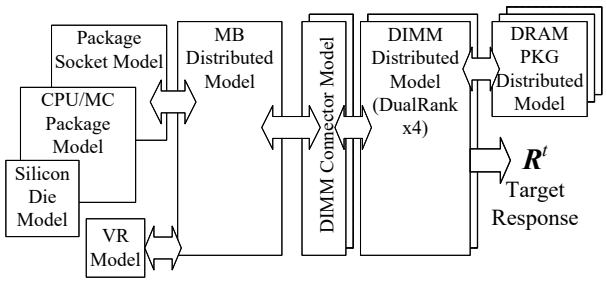

Fig. 7. Block diagram of the distributed PDN of the main power rail of a DDR3 memory sub-system. Taken from [13].

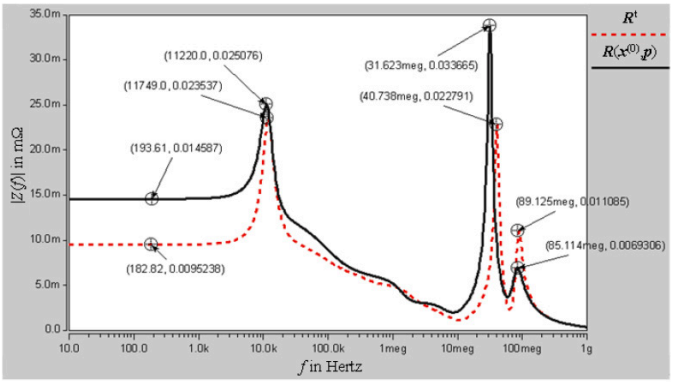

Fig. 8. Lumped model impedance profile at the starting point $\boldsymbol{R}(\boldsymbol{x}^{(0)}, \boldsymbol{p})$ *vs.* target response $\boldsymbol{R}^t$ from the distributed model Taken from [13].

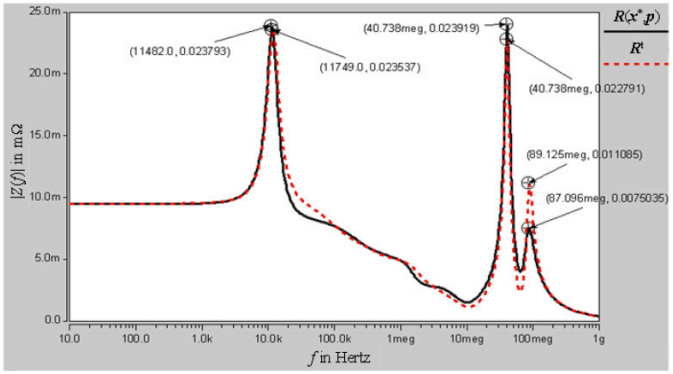

Fig. 9. Optimized lumped model impedance profile response $\boldsymbol{R}(\boldsymbol{x}^*, \boldsymbol{p})$ *vs.* target response $\boldsymbol{R}^t$ from the distributed model. Taken from [13].

A simplified block diagram of the distributed PDN model of the DDR3 memory sub-system is shown in Fig. 7. Extracting the distributed model of most of those blocks requires full-wave 3D EM solvers, yielding S-parameter files to produce SPICE compatible macro-models, creating a very large distributed PDN model, whose simulation provides the target response $\boldsymbol{R}^t$ for our PE formulation.

The PE objective function is described in [13] and uses penalty terms to constrain the optimization variables $\boldsymbol{x}$, which contains the lumped element values to be extracted, keeping fixed some of the lumped elements (as pre-assigned parameters $\boldsymbol{p}$). The response of the lumped model is denoted by $\boldsymbol{R}(\boldsymbol{x}, \boldsymbol{p})$.

The lumped model response at the starting point, $\boldsymbol{R}(\boldsymbol{x}^{(0)}, \boldsymbol{p})$ is evaluated and compared with target response $\boldsymbol{R}^t$, finding that the empirical methodology based on S-parameter matrices for estimating lumped values is not accurate enough for predicting

TABLE I
SUMMARY OF MAX. RELATIVE TESTING ERRORS (%) USING DIFFERENT SURROGATE MODELS FOR TWO POWER DOMAINS

output	e_{rGRNN}	e_{rPSM}	e_{rSVM}	$e_{rKriging}$
P_{D1}	44.32	10.46	9.45	13.44
P_{D2}	35.04	3.90	4.63	3.47
V_{min1}	38.70	32.72	25.10	23.40
V_{min2}	50.54	36.15	20.78	19.42

the PDN behavior, as seen in Fig. 8. The lumped model response after PE optimization $\boldsymbol{R}(\boldsymbol{x}^*, \boldsymbol{p})$ and the target response $\boldsymbol{R}^t$ are better matched, as shown in Fig. 9.

The transient simulation in HSPICE[1] of the lumped model takes only 0.2% of the CPU time used by the distributed model, making feasible an SI-PI evaluation, as detailed in [13].

IV. PDN SURROGATE-BASED OPTIMIZATION (SBO)

An SBO methodology for efficient PDN design optimization is proposed in [14]. It essentially consists of developing several black box metamodels using a frugal number of training and testing data within the design region of interest, selecting the PDN metamodel with the best generalization performance. Training and testing data are obtained from high-fidelity simulations (fine models). The best PDN metamodel is then used as a vehicle for direct and fast PDN optimization, to optimally satisfy design specifications expressed in terms of voltage and power consumption bounds.

The following machine learning techniques are compared in [14] for developing several PDN metamodels: generalized regression neural networks (GRNN), polynomial surrogate modeling (PSM), support vector machines (SVM), and Kriging. For instance, the main surrogate modeling results of a PDN consisting of two power domains sharing a single voltage regulator using a dual sensing scheme, intended for communications and storage applications [15], are shown in Table I. Each metamodel has four outputs: power consumptions (P_{D1}, P_{D2}) and minimum voltages (V_{min1}, V_{min2}). The corresponding PDN fine model was implemented with HSPICE. It is seen from Table I that the Kriging surrogate model shows the overall best generalization performance, selecting it to perform direct optimization to find optimal sensing resistors and loading conditions [14].

V. CONCLUSIONS

Surrogate-based optimization (SBO) methods, exploiting machine learning techniques and space mapping approaches, are briefly reviewed in this paper to enhance signal and power integrity in high-speed input-output (HSIO) links and power delivery networks (PDN). Efficient receiver equalization for HSIO interfaces is demonstrated, where lab measurements on industrial post-silicon validation platforms are used, achieving significant improvement in eye diagram margins and important speed-up of the PHY tuning process. An efficient method based on parameter extraction is used to develop fast PDN lumped models exploited for low-cost SI-PI co-simulation. Finally, we briefly described an SBO approach for efficient PDN design optimization, comparing several machine learning techniques.

[1] HSPICE®, ver. B-2008.09-SP1, Synopsys Inc., Mountain View, CA, 2008.

REFERENCES

[1] M. P. Li, *Jitter, Noise, and Signal Integrity at High-Speed*. Boston, MA: Prentice Hall, 2007.

[2] V. S. Pandit, W. H. Ryu, and M. J. Choi, *Power Integrity for I/O Interfaces: with Signal Integrity/Power Integrity Co-Design*. Upper Saddle River NJ: Prentice Hall, 2011.

[3] F. E. Rangel-Patiño, A. Viveros-Wacher, J. E. Rayas-Sánchez, I. Durón-Rosales, E. A. Vega-Ochoa, N. Hakim and E. López-Miralrio, "A holistic formulation for system margining and jitter tolerance optimization in industrial post-silicon validation," *IEEE Trans. Emerging Topics Computing*, vol. 6, 2018. (pub. online: 29 Sep. 2017).

[4] J. E. Rayas-Sánchez, F. E. Rangel-Patiño, A. Viveros-Wacher, J. L. Chávez-Hurtado, J. R. del-Rey, F. Leal-Romo, and Z. Brito-Brito, "Industry-oriented research projects on computer-aided design of high-frequency circuits and systems at ITESO Mexico," in *European Microw. Conf. (EuMC-2018)*, Madrid, Spain, Sep. 2018, pp. 588-591.

[5] F. E. Rangel-Patiño, J. E. Rayas-Sánchez, and N. Hakim, "Transmitter and receiver equalizers optimization methodologies for high-speed links in industrial computer platforms post-silicon validation," in *Int. Test Conf. (ITC-2018)*, Phoenix, AZ, Oct. 2018, pp. 1-10

[6] F. E. Rangel-Patiño, J. L. Chávez-Hurtado, A. Viveros-Wacher, J. E. Rayas-Sánchez, and N. Hakim, "System margining surrogate-based optimization in post-silicon validation," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 9, pp. 3109-3115, Sep. 2017..

[7] J. Sacks, W. J. Welch, T. J. Mitchell, and H. P. Wynn, "Design and analysis of computer experiments," *Statistical Science*, vol. 4, no. 4, pp. 409-423, Nov. 1989.

[8] S. N. Lophaven, H. B. Nielsen, J. Søndergaard, "Aspects of the Matlab toolbox DACE," Internal Report *IMM-TR-2002-13*, Technical University of Denmark, Lyngby, 2002.

[9] J. W. Bandler, R. M. Biernacki, S. H. Chen, R. H. Hemmers, and K. Madsen, "Electromagnetic optimization exploiting aggressive space mapping," *IEEE Trans. Microw. Theory Techn.*, vol. 41, no. 12, pp. 2874-2882, Dec. 1995.

[10] J. E. Rayas-Sánchez, "Power in simplicity with ASM: tracing the aggressive space mapping algorithm over two decades of development and engineering applications," *IEEE Microw. Magazine*, vol. 17, no. 4, pp. 64-76, Apr. 2016.

[11] F. E. Rangel-Patiño, J. E. Rayas-Sánchez, A. Viveros-Wacher, E. A. Vega-Ochoa, and N. Hakim, "High-speed links receiver optimization in post-silicon validation exploiting Broyden-based input space mapping," in *IEEE MTT-S Int. Conf. Num. EM Mutiphys. Model. Opt. RF, Microw., Terahertz App. (NEMO-2018)*, Reykjavik, Iceland, Aug. 2018, pp. 1-3.

[12] F. Rangel-Patino, J. L. Chávez-Hurtado, A. Viveros-Wacher, J. E. Rayas-Sánchez, and N. Hakim, "Eye diagram system margining surrogate-based optimization in a server silicon validation platform," in *Europ. Microw. Conf. (EuMC-2017)*, Nuremberg, Germany, Oct. 2017, pp. 540-543.

[13] B. Mercado-Casillas and J. E. Rayas-Sánchez, "Towards signal-power integrity analysis by efficient power delivery network lumped models obtained from parameter extraction," in *Int. Conf. Electrical Performance of Electronic Packaging and Systems (EPEPS 2019)*, Montreal, Canada, Oct. 2019, pp. 1-3.

[14] F. J. Leal-Romo, J. E. Rayas-Sánchez, and J. L. Chávez-Hurtado, "Surrogate-based analysis and design optimization of power delivery networks," *IEEE Trans. on Electromagnetic Compatibility*, (work submitted).

[15] F. J. Leal-Romo, J. L. Chávez-Hurtado, and J. E. Rayas-Sánchez, "Selecting surrogate-based modeling techniques for power integrity analysis," in *IEEE MTT-S Latin America Microwave Conf. (LAMC-2018)*, Arequipa, Peru, Dec. 2018, pp. 1-3.