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Departamento de Electrónica, Sistemas e Informática

MAESTRÍA EN DISEÑO ELECTRÓNICO

REPORTE DE FORMACIÓN COMPLEMENTARIA EN ÁREA DE CONCENTRACIÓN EN DISEÑO ELECTRÓNICO DE ALTA FRECUENCIA

Trabajo recepcional que para obtener el grado de

MAESTRO EN DISEÑO ELECTRÓNICO

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San Pedro Tlaquepaque, Jalisco. Enero de 2020.

Content

Introduction

All over the world, there has been a necessity to pass along the knowledge between human generations. One classic and functional way to do it has been through books, scientific publications and application notes, etc. The "Instituto Tecnológico y de Estudios Superiores de Occidente, ITESO Universidad Jesuita de Guadalajara" has contributed with the document called "Trabajo de Obtención de Grado (ToG)". The present ToG document is a compendium of the developed projects during the master-degree lapse in which the student reports the development, results, and conclusion per project.

The document contains 3 projects that were developed followed by the concentration area of The High-Frequency Design of Electronics Circuits. These projects were:

The 1st project is the **Band-stop filter with a microstrip line**, developed during the subject of *High-Frequency Electronics Design*.

The 2nd project is the **Modeling a strain gauge and conditioning circuit for a Natural Vacuum leak detection system**. Developed during the subject *Methods of Simulation of Electronic Circuits.*

The 3rd project is the **Output capacitor optimization for a Low voltage Drop-Out (LDO) regulator using the space mapping method**. Developed during the subject *Modeling and Design of Circuits Based on Optimization.*

In the end, all the experience and knowledge acquired when developing all these projects have been applied in the automotive industry work, which also helped to improve the engineering level of the student. Ending up with a perfect match between academy knowledge and real work design experience for Automotive development cases.

1. Summary of projects developed.

1.1. Band-stop filter with microstrip line

1.1.1 Introduction

The band-stop filter is a basic electrical circuit that can reject all the signals between a specific frequency range meanwhile it allows to pass the rest of the frequencies unaltered. This filter is also known as band-rejection filter. This project is designed under the parameters of a center frequency of 3.4GHz and 5% of bandwidth tolerance.

To develop this project, APLAC and Sonnet simulation programs will be used. This project includes a theoretical description, practical calculation, development, simulations, and conclusions. The methodology to solve this design will be the same as in class.

1.1.2 Background

There are different applications for the electrical filters, one of them is to eliminate frequency signals that are not needed. A couple of ways to build up these filters is based on passive or lumped components such as resistors, capacitors, and coils connected. Another way is by adding concentrated components in a PCB for the same purpose.

A lumped component circuit consists of several sections of PCB trace or metal lines that act in conjunction as resonators, they could be in Line shape, U shape L shape depending on the needs. This kind of circuits is usually known as a coupled microstrip line. This kind of microstrip line can be successfully implemented in small sections (less than 5cms) of a substrate with a dielectric constant such FR4 or some others.

Applications come from industrial designs such as radios, aeronautics for transmission systems, medicine in heart pulse measure equipment, automotive for engine transient pulses protection, school applications for didactics as electromagnetic labs, etc.

1.1.3 Developed solution

The bandstop filter design was developed according to the methodology seen in High-Frequency Electronics Design (during the semester). In order to do these 4 steps were followed:

1) First, the electrical requirements were defined for the filter design.
2) Next, select the number of lumped components or the quantity of sections (n) that the filter will have and then g1 to gx values can be selected.
3) After getting the desired gx design parameters, the $x1/z_0$ can be calculated. To do that, equations (1-1) and (1-2) will help to calculate each x1 value:

$$z_u=z_0 \tag{1-1}$$

$$x_1=\frac{g_0}{g_1(\mathrm{FBW})} \tag{1-2}$$

Where:

z_0 -> Source impedance

z_u->Segment impedance between resonator

g_0-> Normalized impedance

g_x-> Element value of the bandstop filter, including g1

x1-> Reactance slope parameter of shunt-series resonator

$x1/z_0$-> Relation between the normalize reactance slope parameter to the frequency bandstop resonator.

FBW-> Fractional frequency bandwidth

After the calculation of the $x1/z_0$, the normalized reactance slope parameters (S-parameter) were determined:

Summary results normalized reactance slope parameters (s) are shown in Table I.

TABLE I
S values

$x1/z_0$	s (mm)
19.387/50	0.292
17.431/50	0.221
19.387/50	0.102

4) After getting the slope parameters, which determine the separation between each L resonator section, the last parameters selected are the physical size of the L-resonators

(length and width). For length, it was ¼ of lambda and for the width, it was a value used from previous design (as a starting point). The initial values are:

length is 13.22mm and width is 1.812 mm.

After that, the circuit was simulated in Sonnet program. The result can be seen in Fig 1-1.

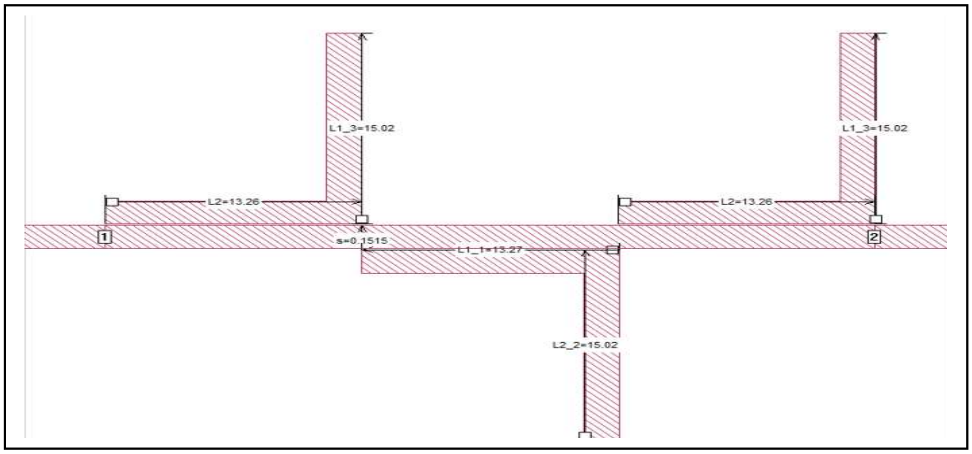


Fig. 1-1 A bandstop filter with L resonators in the Sonnet program.

1.1.4 Results analysis

Results from the APLAP simulator show that after running the simulation, the central frequency of 3.4GHz was almost obtained (3.36GHz). Also, the bandwidth expected of 170MHz was met (105MHz) as a result of the calculated segments of the filter. Results from the Sonnet simulator show the same response as in the APLAC simulator. The center frequency results were 3.49GHz, and the bandwidth was 46MHz.

Summary results from both simulators are shown in Table II.

TABLE II

Specification fulfillment vs simulation results

Paremeter	Specification values	APLAC results	Sonnet results
Center frequency (fc)	3.4GHz	3.362GHZ	3.49GHz
Fractional Bandwidth (%)	5%	3%	1.35%
Fractional Bandwidth (MHz)	170	105	46

1.1.5 Conclusions

After using the knowledge learned during the class it was possible to calculate the initial values to start the bandstop filter with 3-L resonators. Also, it has been observed that APLAC and Sonnet simulators have a different response because APLAC is a general-purpose electrical circuit simulator and Sonnet is an electromagnetic effect simulator.

As a lesson learned and conclusions for the student at the end of this project/semester, it was obtained more knowledge in the use of electrical and electromagnetic simulators, advantages disadvantages and differences. This filter will be used by 2 application in the future automotive projects, one will be as an input filter for switching power supplies together with another passive component filter, and the second will be during transient tests as impedance adaptor in an EMC lab.

1.2. Modeling a strain gauge and conditioning circuit for a natural vacuum leak detection (NVLD) system

1.2.1 Introduction

In the last 20 years, the automotive industry has been pushed to make all the vehicles (heavy and weight) less harmful for the human being and the environment. To do that new systems have been developed such as the Natural Vacuum Leak Detection (NVLD). This valve helps to control the recirculation of the gases created by the tank and after some time, send them back to the combustion chamber for better use of the burned fuel and less use of more new gasoline from the gasoline container this will end up in less contamination and air pollution. To emulate, design and improve this, a proper model of this valve sensor should be made.

1.2.2 Background

Pressure sensors have been studied in the automotive industry in the last 30 years with innovative results. As a result, new models have been developed by several researchers.

Since 1990, these models have been used for different valves designed by the automotive industry, each one of them has different characteristics and assemblies. But all of them contain mechanical or mechanical/electrical parts which with the time pass they got rusty, weak or even worst disposable. Also, the Electric control unit needed to have filters, anti-glitch circuits, and ADC converters to translate the response from the valve sensor.

Some of them are the leak detection pump (L.D.P.) which can create a positive pressure of 7.5” water and monitors a pressure decay timer to determine the sealing. Another is the Mitsubishi-system, which uses a vacuum decay method with 3 wire-sensing. However, the methodology is obsolete in more recent vehicles and it will not be used in this project.

The NVLD system developed by Chrysler in 2002 requires a 12v battery voltage level when the key is on and a 5v level when the key is off. Based on this voltage variation in the electromechanical sensor a state-of-the-art electronic sensor can be designed (as a more innovative option).

1.2.3 Developed solution

The NVLD system model was constituted by 2 main parts: strain gauge and Wheatstone bridge designs. The strain gauge represents the transducer that transforms the pressure difference (top and bottom) into a resistance change, due to silicon elongation. The Wheatstone bridge is the electric circuit that transforms the resistance change into electrical variations (DC voltage, a few millivolts). The calculation of these 2 sections is described in the next sections.

The first step was to collect certain values in order to model a close semiconductor diaphragm piezoresistive strain gauge. To accomplish this, the next values were investigated:

In the direction of a carrier flow, known as <110>, the next piezoresistive coefficients (compressive strain-hole mobility) are obtained by: πl= 71.8e-11 (1/Pa), πt= -66.3e-11 (1/Pa).

Besides, elastic constants of plain silicon Exx, Exy, Eyy, and Gxy are obtained from coordinate transformation:

Exx=1.891x10^5 MPa, Exy=0.530x10^5 MPa, Eyy=1.4571x10^5 MPa

All these parameters were introduced in MATLAB® to obtain the x directed normal stress (σx) and the directed normal stress (σy) by solving the next matrices:

$$\begin{bmatrix} \sigma x \\ \sigma y \\ Txy \end{bmatrix} = \begin{vmatrix} Exx & Exy & 0 \\ Exy & Eyy & 0 \\ 0 & 0 & Gxy \end{vmatrix} \begin{vmatrix} \epsilon x + s'13 * p \\ \varepsilon y + s'23 * p \\ \gamma xy \end{vmatrix} \qquad (1\text{-}34)$$

So σx and σy are dependent values of pressure (P), therefore a sweep from 1-1000 (P) in Pascals is done. The results of this parameters sweep can be seen in Figure 1-2:

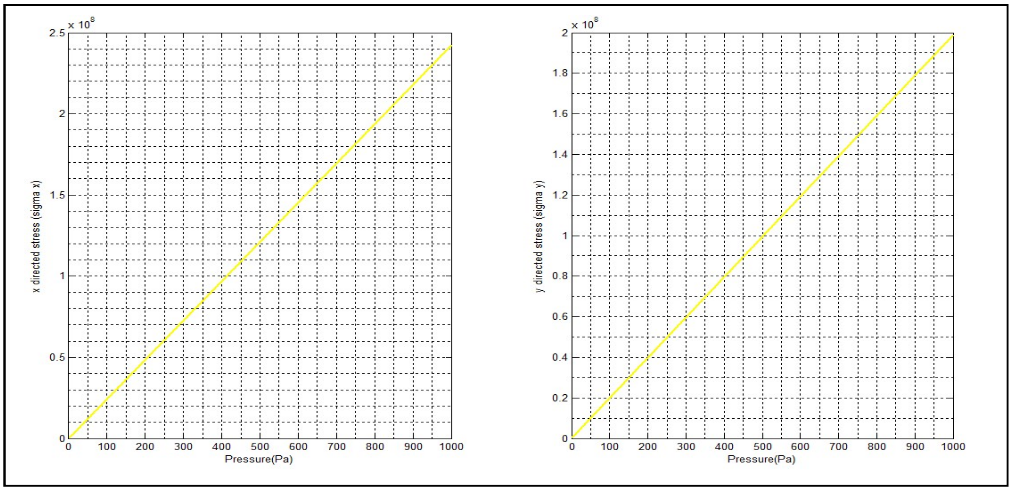


Fig. 1-2 Strain gauge stress sigma x and y parameters calculation.

By selecting a value of 120 Ω @ 25°C for the strain gauge and using previous constants/coefficients in the equation Rx=Ro (1+αT+ πl*σl+ πt*σt), the resistance variation for every change on the pressure applied on the membrane can be calculated as shown in Figure 1-3:

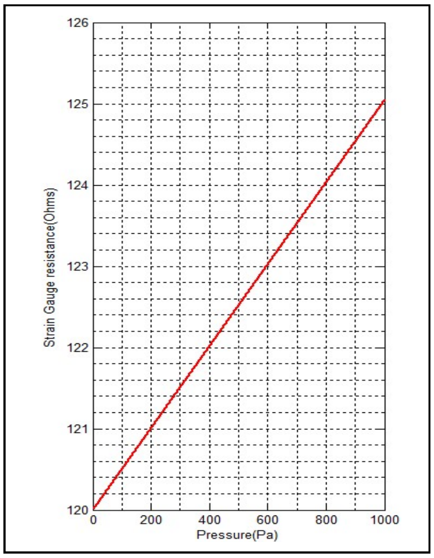


Fig. 1-3 Strain gauge resistance change calculation based on pressure variation.

1.2.4 Results analysis

The first results obtained were the x directed normal stress (σx) and the y directed normal stress (σy) were modeled and simulated, which can be seen in Figure 1-4. After applying the pressure sweep, the normal stress value increased linearly as expected.

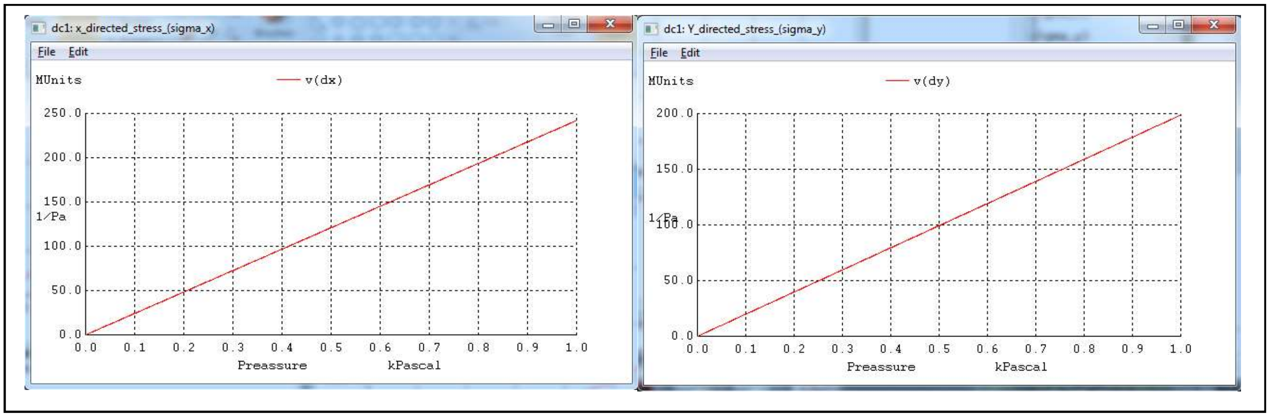


Fig. 1-4 Stress sigma x (σ1).

The next section of the model was the strain gauge resistance. The simulation, in this case, was also based on pressure variation. The resistance value increase between 120ohms, which was the initial value since all the resistors in the Wheatstone bridge must have the same value, but after changing the pressure, the strain gauge resistance changed linearly. The response is shown below in Figure 1-5:

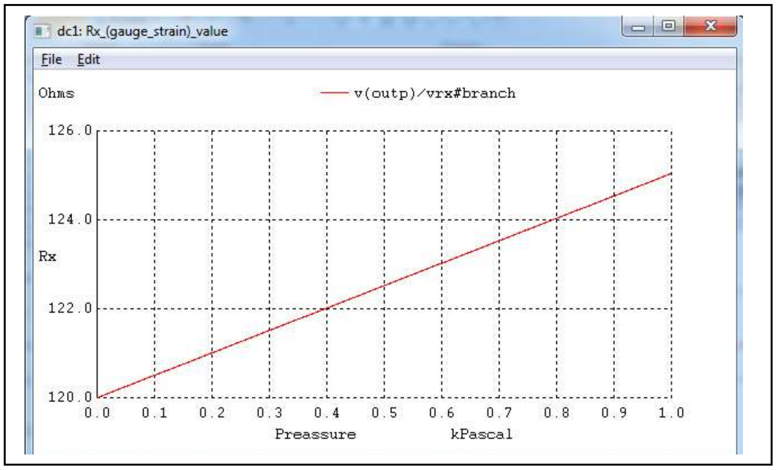


Fig. 1-5 Strain gauge resistance change.

The presented findings confirm that the complete modeled worked correctly and as expected.

1.2.5 Conclusions

The purpose of this project was to model and simulate, the complete NVLD system (strain gauge and conditioning circuit), based on the modeling sensors methodology using the MATLAB® methodology, calculations, and technical description, and WINSPICE® for the simulation and results.

The NVLD system with the strain gauge and the conditioning circuit model worked according to the design described in the methodology. The strain gauge parameters in X and Y directions implemented in the equation varied linearly under any pressure change in the silicon diaphragm. The pressure/resistance variations of the strain gauge were transformed by the conditioning circuit into voltage variation between the ranges of 0 to 5V, and it worked fine.

This proposal was submitted as an invention disclosure in the United States Patent and Trade Mark Office in July-2018.

1.3. Output capacitor optimization for an LDO regulator using Space Mapping

1.3.1 Introduction

The low-dropout linear regulators (LDOs) have gain popularity between the applications that need to operate with small power components, such as portable devices or even bigger devices as computers, televisions or sound equipment.

The increase performance of the PMOS LDOs comes with stability concerns to the load and the external capacitor. Due to this, it is necessary to see if the LDO is keeping the fast response/output stability during transient variations in the load and the input voltage.

For this, some topics were covered. The first was the LDO circuit model definition and functionality explanation. The next is the stability analysis and the calculation, which would be the basis for output capacitor optimization. The optimization was accomplished by using Space mapping implementation, which was not only described but also the use method.

1.3.2 Background

The LDO regulators have passed for several changes. The first one started in the 70s by the hand of National Semiconductor Company. The first configuration was the NPN regulator which was simple and cheap but high voltage drop (>3.5V). Then it was the PNP/LDO regulator (which is the case of study), it has very low dropout voltage (<1.5V) and low quiescent current. This one requires an output capacitor. The latest option is the MOS regulator that has a smaller low dropout (<0.5V), but the internal MOSFET a bigger output capacitor and is a more expensive transistor.

To a good linear regulator design, some parameters must be taken into consideration, a couple of them are line regulation, load regulation, and transient response. In this case for the output capacitor selection, it is necessary to use the transient response, which can be obtained by doing a stability analysis.

In this document, a stability analysis is modeled based on the main design parameters to show a real case circuit that could be used to represent the response of an LDO. Using the optimization method called Space Mapping, an optimal output capacitor value will be selected, to keep the output voltage free of any perturbation.

1.3.3 Developed solution

The solution described for this optimizing tool was to summarize the basic circuit functionality, starting with the LDO blocks or components such as:

- Reference voltage
- Error amplifier
- Feedback network
- Load resistor (RLOAD)
- Output capacitor (CLOAD)
- Output capacitor series resistor (CESR)
- Bypass capacitor (CBP)
- Error amplifier output capacitance (CPMOS)
- Error amplifier output resistance (ROA)
- The series pass element series resistance (PMOS)

Then after that, calculation of the three main poles and one zero are calculated and also the error amplifier, feedback network and pass transistor gains. At the end a total LDO open-loop gain is calculated based on the next equation (1-4):

$$\mathrm{GOL(s)} = \mathrm{GEA} * \mathrm{GFB} * \mathrm{GPMOS} * (1 + \mathrm{s}/2\pi \mathrm{fz1})/ (1 + \mathrm{s}/2\pi \mathrm{fp1}) * (1 + \mathrm{s}/2\pi \mathrm{fp2}) * (1 + \mathrm{s}/2\pi \mathrm{fp3}) \quad (1\text{-}4)$$

Space Mapping algorithm was defined in the way seen in the course of high-frequency electronic design. To do this, the next Figure 1-6 describes what would be the basic idea.

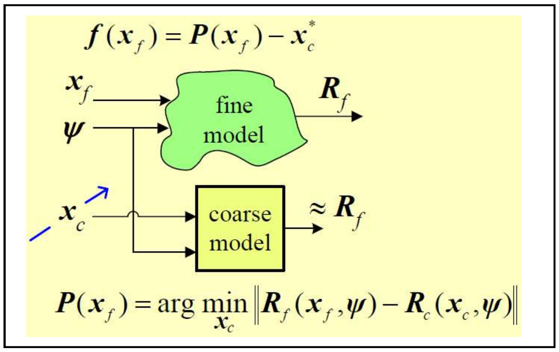


Fig. 1-6 Space Mapping approach

Basically, it is necessary to have 2 models, one is the fine model and the other is a coarse model, both with input parameters that provide a similar response but with different characteristics: The Fine model is more accurate but more expensive in terms of resources (high computer processing);the Coarse model is less accurate but cheaper and faster.

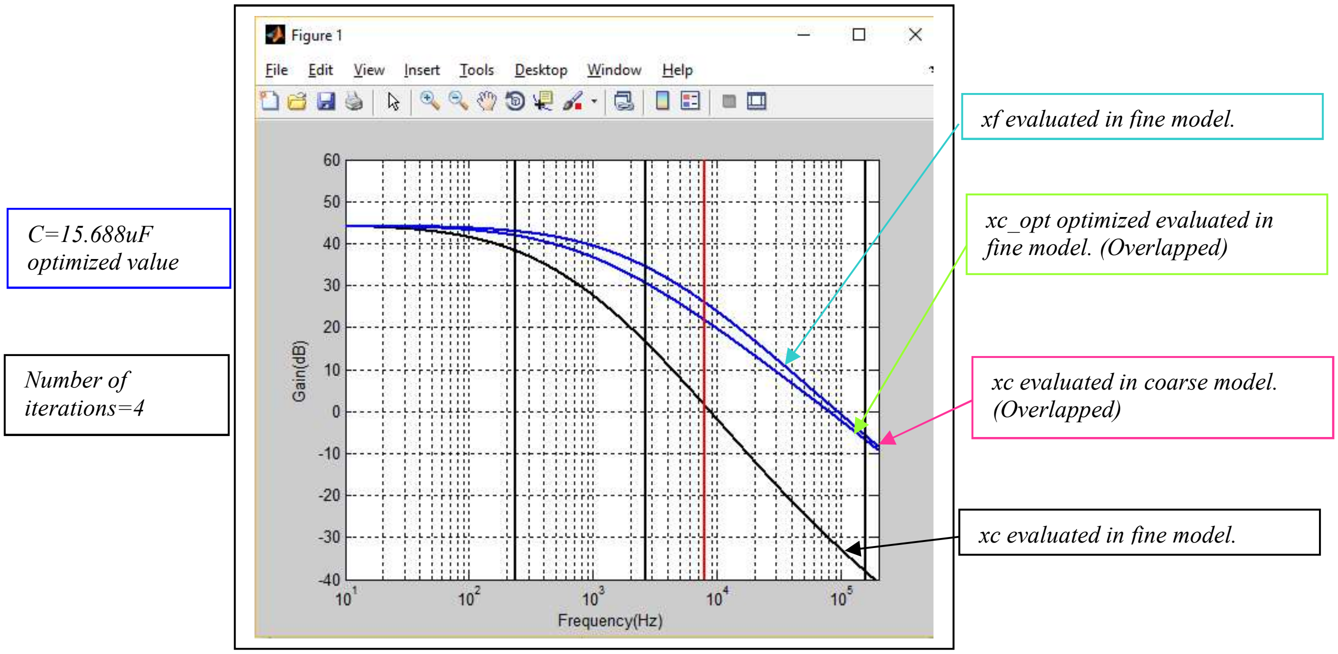
The algorithm was described in MATLAB because it has a nice graphic tool and several optimized functions that could be used at any time.

In this case the variable to be found, is the output capacitance of the LDO. At the beginning, the proposed values are C=10uF for the Fine model and 20uF for the Coarse model.

The Fine model contains all the equations as described above, but for the Coarse model ESR parameter was removed from the equations and PMOS transistor output resistance increased to make the model unstable with 10uF.

1.3.4 Results analysis

After running the scripts, the results are shown in Fig 1-7.



xf evaluated in fine model.

xc_opt optimized evaluated in fine model. (Overlapped)

C=15.688uF optimized value

Number of iterations=4

xc evaluated in coarse model. (Overlapped)

xc evaluated in fine model.

Fig. 1-7 Optimization results (top-left->xf evaluated in fine model, top-right->xc evaluated in coarse model, bottom-left->xc evaluated in fine model, right->xc optimized evaluated in fine model).

Figure 1-7(top-left) shows the result of fine parameter xf in the fine model. This becomes the expected response from the circuit, more accurate but from a computational point of view more expensive.

Figure 1-7(top-right) shows the result of coarse parameter xc in the coarse model. This becomes a “functional” response of the circuit, less accurate but from a computational point of view cheaper.

Figure 1-7(bottom-left) shows the result of fine parameter xf in the coarse model. This becomes the “optimizing” response which means this is the result will be optimized until a proper value gives a close response as figure1-7.

Figure 1-7(bottom-right) shows the result of optimized parameter xc_opt in the coarse model. This becomes the “optimized” response of the circuit, more accurate (almost as figure1) but from a computational point of view cheaper.

1.3.5 Conclusions

After using the knowledge learned during the class the optimal output capacitor value for the linear regulator. The values investigated, equations calculated, and the theory described along the project was enough to calculate the stability behavior and response of the circuit.

If the gain-phase plot was recalculated with ESR set to 10mV, the Unity gain frequency was 10 kHz, which would change to a phase margin of 16°. With a very low ESR value, one of the poles and the zero would be frequencies much higher than the Unit gain frequency, which would end up in an unstable system.

At the end of this project, I could get complete knowledge of how to create and optimizing script based on different methodologies of search, which could be used for future tools in the automotive industry. One for DCDC converters is currently running to find out a control switching frequency depending on the output current setpoint. This was possible after taking this class, learning all the concepts and putting them all together in practice.

2. Conclusions.

After taking all the assignments during the master’s degree, it helped me to improve the knowledge in the use of APLAC and Sonnet programs which were not in the pool of knowledge before. Today it is possible to do an electrical behavior simulation with APLAC to solve every day-simulations and compare them with other simulators such as SPICE and Saber. Also, an electromagnetic simulation can be run in APLAC and later this can be reproduced and run in Sonnet and compare between them with good failure-tolerance results.

High-frequency design has been untangled after doing the project presented in the document. I learnt how to design a stop band filter with lumped components and transform this to an application that could be implemented in a PCB, which is necessary for automotive industry.

From the class Optimization-based modeling and design of electronic circuits, the Automatization running scripts have been useful and these have been used in 2 automotive design applications, one of them is a 5KW DCDC converter (boost configuration) frequency setup finder for different output current. And the other 10KW DCDC converter component selection (from electrical requirements to complete design).

The fact of Modeling sensor knowledge was used for an idea developed during the class Simulation methods for electronic circuits. After the final project was delivered, the project was completed and was used to present a patent application to the U.S. patent committee.

As it has been described all projects together facilitated the student to get better development in its professional career during and after the Master study, specifically after taking these 3 assignments.

The three projects described have demonstrated the knowledge and the application of them in the real world, specifically in the automotive industry. The results and the outcomes from there have been satisfactory. With this, it has been proved that the concentration area in high-frequency electronic design was the right option for the student which has been and will constitute an important knowledge column for the personal career and the next step for the Ph.D. degree.

Appendix

A. BAND-STOP FILTER WITH MICROSTRIPLINE.

Project name:

Band-Stop filter With Microstripline.

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3. Content.

4. Introduction.

Basically, the problem described in the final project document (pdf version) proposes 2 different options:

a) Band-Pass Filter
b) Band-Stop Filter

In this case the option b was chosen to perform as design for final project due to better knowledge and understanding of the possible solution in terms of expected design response and behavior of the filter.

In principle the requirements for such Band-Stop filter are:

1. Center frequency: 3.4GHz
2. Fractional Bandwidth: 5%
3. Filter order: 3
4. Type of frequency response: 0.1dB Chebyshev
5. Reference impedance = 50Ω
6. The Circuit will be fabricated in microstrip using the following substrate:
7. Rogers RO4003 (h = 0.81 mm; cladding of 0.5oz.; er = 3.55) www.rogers-corp.com.

The methodology to resolve this filter design will be the same as in class. For this will be necessary to describe the basic theory of a band stop filter.

A bandstop filters are used when some unwanted interfering frequencies be particularly strong; or when high attenuation may be needed only at certain frequencies.

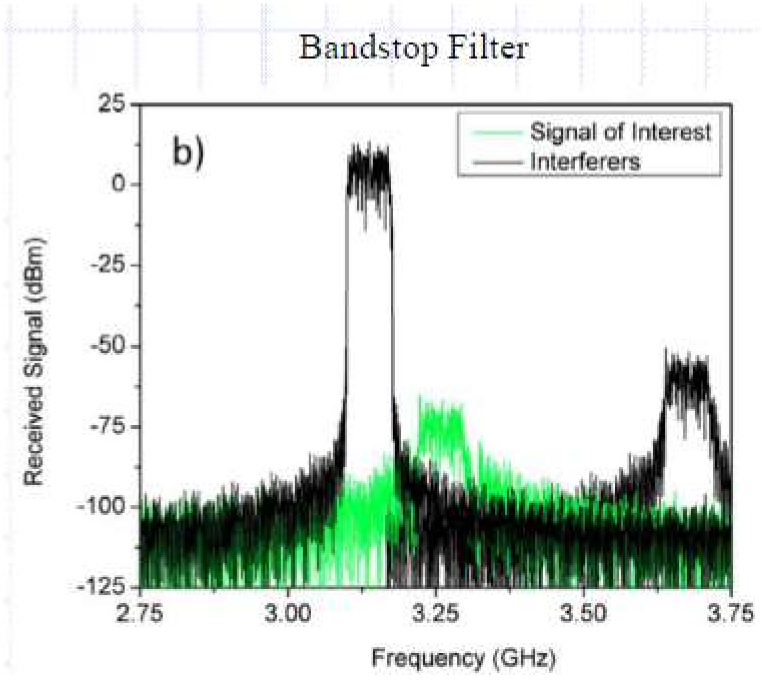
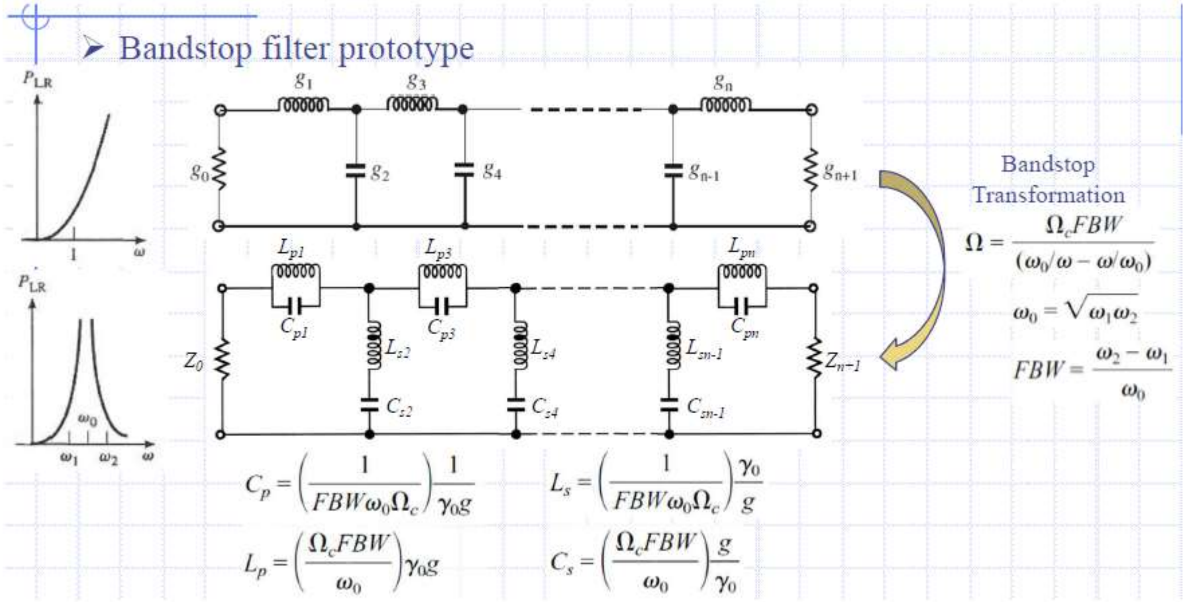


Figure 1.0 Band-stop filter response.

The next step is based on the basic ban-stop circuit use the Transformation. Each coil changes to a coil//cap and each cap changes to a coil in series with a cap.



$$\Omega = \frac{\Omega_c FBW}{(\omega_0/\omega - \omega/\omega_0)}$$

$$\omega_0 = \sqrt{\omega_1\omega_2}$$

$$FBW = \frac{\omega_2 - \omega_1}{\omega_0}$$

$$C_p = \left(\frac{1}{FBW\omega_0\Omega_c}\right)\frac{1}{\gamma_0 g} \qquad L_s = \left(\frac{1}{FBW\omega_0\Omega_c}\right)\frac{\gamma_0}{g}$$

$$L_p = \left(\frac{\Omega_c FBW}{\omega_0}\right)\gamma_0 g \qquad C_s = \left(\frac{\Omega_c FBW}{\omega_0}\right)\frac{g}{\gamma_0}$$

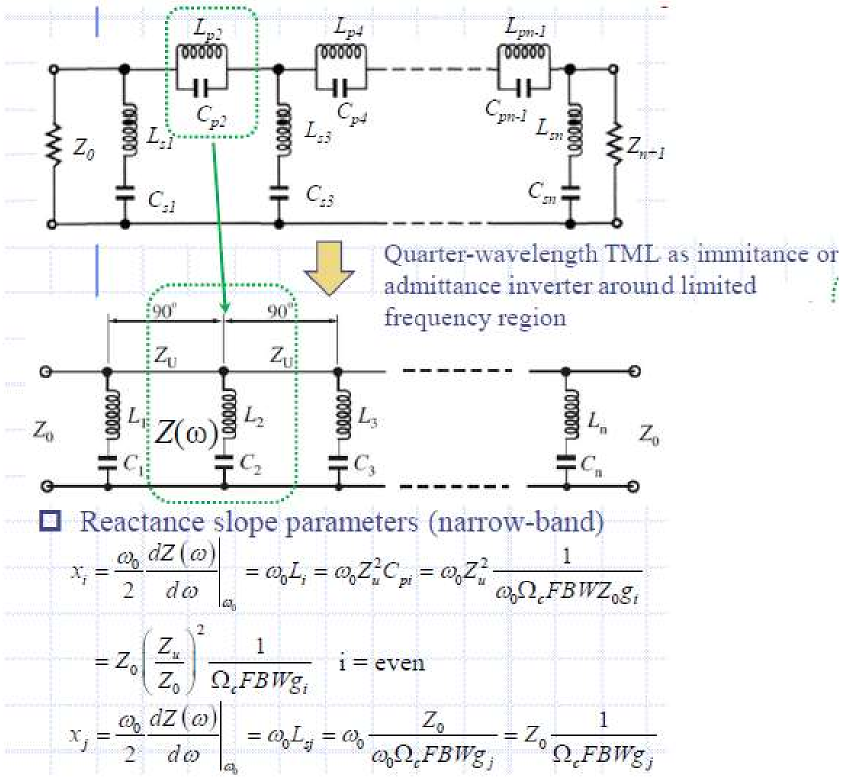
Figure 1.1 Band-stop filter transformation.

5. Once the transformation is done an appropriate microstrip realization has to be found:

- Narrowband Bandstop Filter (electric couplings and magnetic couplings)

- Bandstop Filters with Open-circuited Stubs
- Optimum Bandstop Filter
- Bandstop Filters for RF chokes

As it was done in class, the option is Narrow Bandstop Filter.



Quarter-wavelength TML as immitance or admittance inverter around limited frequency region

☐ Reactance slope parameters (narrow-band)

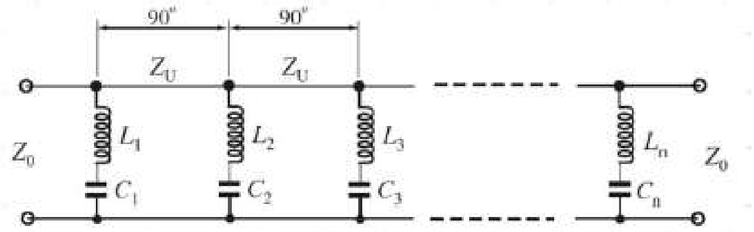
$$x_i = \frac{\omega_0}{2}\frac{dZ(\omega)}{d\omega}\bigg|_{\omega_0} = \omega_0 L_i = \omega_0 Z_u^2 C_{pi} = \omega_0 Z_u^2 \frac{1}{\omega_0 \Omega_c FBW Z_0 g_i}$$

$$= Z_0\left(\frac{Z_u}{Z_0}\right)^2 \frac{1}{\Omega_c FBW g_i} \qquad i = \text{even}$$

$$x_j = \frac{\omega_0}{2}\frac{dZ(\omega)}{d\omega}\bigg|_{\omega_0} = \omega_0 L_{sj} = \omega_0 \frac{Z_0}{\omega_0 \Omega_c FBW g_j} = Z_0 \frac{1}{\Omega_c FBW g_j}$$

Figure 1.2 Narrow band stop filter.

For more convenient realization, all shunt or series resonators are used.
Now approximate the design parameters (slope parameters)



$$\left(\frac{Z_U}{Z_0}\right)^2 = \frac{1}{g_0 g_{n+1}} \qquad \nearrow Z_0 = Z_u$$

$$x_i = \omega_0 L_i = \frac{1}{\omega_0 C_i} = Z_0\left(\frac{Z_U}{Z_0}\right)^2 \frac{g_0}{g_i \Omega_c FBW}$$

for $i = 1$ to n

Figure 1.3 Slope parameters.

Once the design parameters are gotten, the structure is chosen, as it could be with Linear, L , U shaped resonators, which the general structure is λg/2 resonators are spaced λg/4 apart

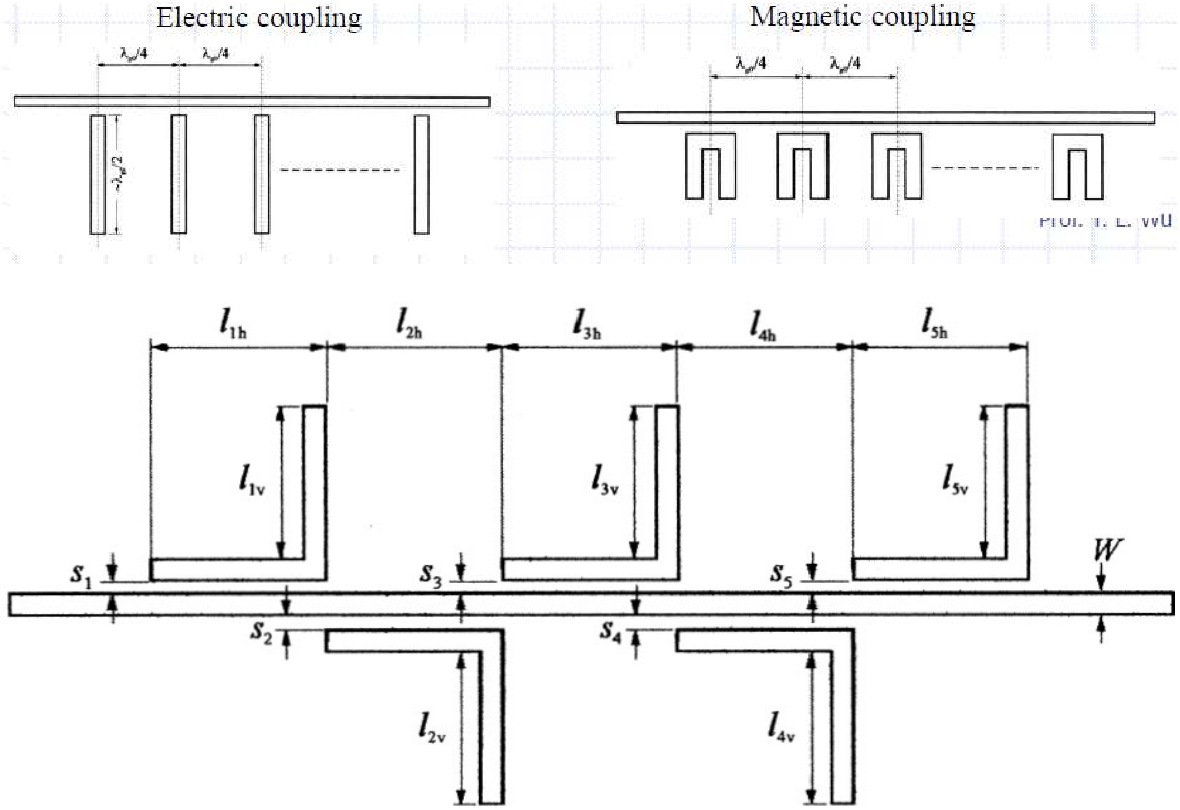
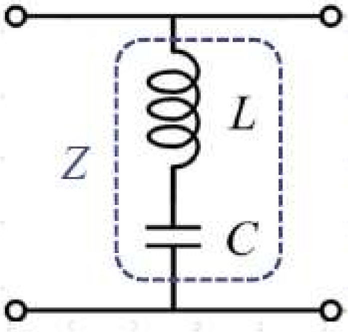


Figure 1.4 Microstrip resonators configurations.

After the resonator is build up, extraction of the slope parameters is the next step, this is by considering a 2-port network with a single shunt branch



$$Z = j\omega L + 1/j\omega C$$

$$\Rightarrow \quad x = \frac{\omega_0}{2}\frac{dZ(\omega)}{d\omega}\bigg|_{\omega_0} = \omega_0 L$$

Figure 1.5 2 port network.

Then Transmission parameter terminated with Z0

$$S_{21} = \frac{1}{1+\dfrac{Z_0}{2Z}} \quad \xrightarrow{\text{Narrowband case, } \Delta\omega \ll \omega_0} \quad |S_{21}| = \frac{1}{\sqrt{1+\left[\dfrac{1}{4(x/Z_0)}\dfrac{\omega_0}{\Delta\omega}\right]^2}}$$

$$\omega = \omega_0 + \Delta\omega, \quad Z \approx j\omega_0 L\left(\frac{2\Delta\omega}{\omega_0}\right)$$

Figure 1.6 S21 simplification.

And at the end from simulation results, the bandwidth in 3dB (S21) is selected to get X/Zo

from EM simulator

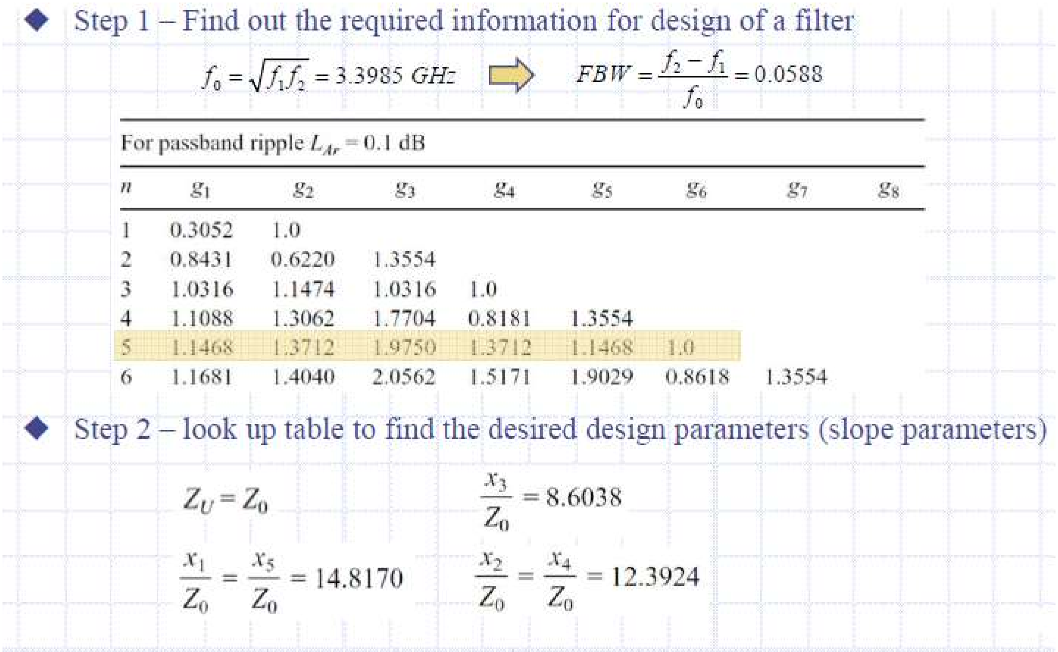
$$\frac{1}{4(x/Z_0)}\frac{\omega_0}{\Delta\omega_\pm} = \pm 1 \Rightarrow \Delta\omega_{3\text{dB}} = \Delta\omega_+ - \Delta\omega_- = \frac{\omega_0}{2(x/Z_0)} \Rightarrow \underline{\left(\frac{x}{Z_0}\right) = \frac{\omega_0}{2\Delta\omega_{3\text{dB}}} = \frac{f_0}{2\Delta f_{3\text{dB}}}} \quad (1)$$

Figure 1.7 Equation to get S21 parameters from simulation results.

So as summary a practical example can be described in 3 steps (once the requirements are clear).

__Requirements:__

Microstrip bandstop filter
n=5 (fifth order)
Chebyshev type with passband ripple of 0.1 dB
f1 = 3.3 GHz
f2 = 3.5 GHz
Z0 = 50 ohm.



◆ Step 1 – Find out the required information for design of a filter

$$f_0 = \sqrt{f_1 f_2} = 3.3985\ GHz \Rightarrow FBW = \frac{f_2 - f_1}{f_0} = 0.0588$$

For passband ripple $L_{Ar} = 0.1$ dB

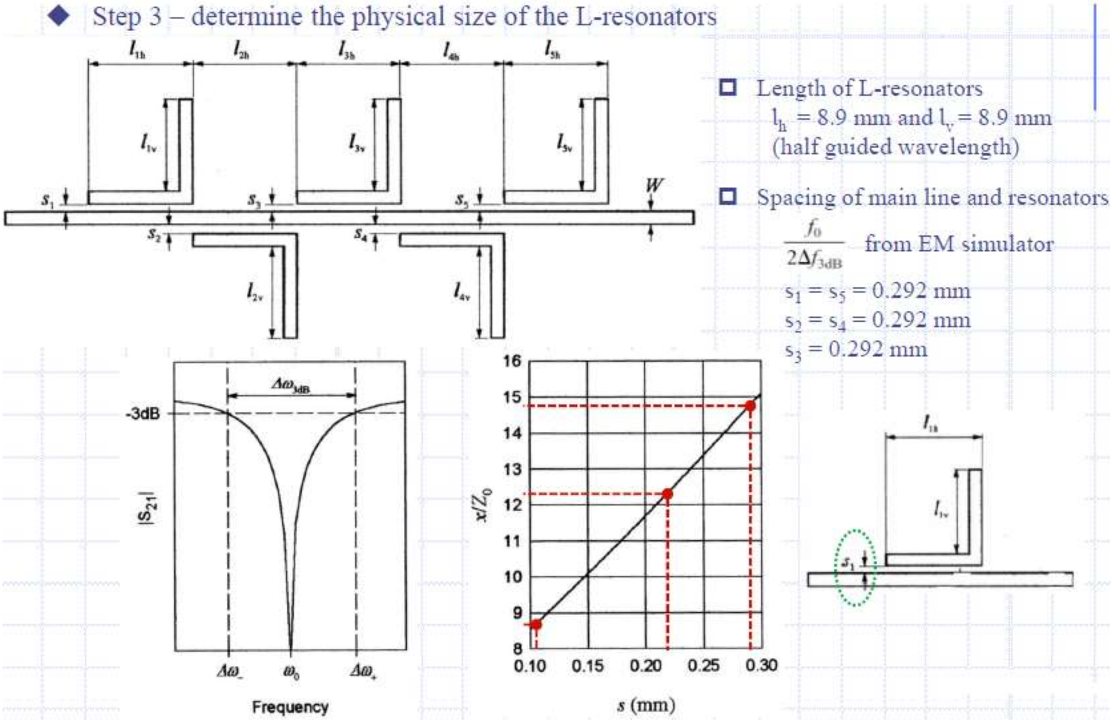
n	g_1	g_2	g_3	g_4	g_5	g_6	g_7	g_8
1	0.3052	1.0						
2	0.8431	0.6220	1.3554					
3	1.0316	1.1474	1.0316	1.0				
4	1.1088	1.3062	1.7704	0.8181	1.3554			
5	1.1468	1.3712	1.9750	1.3712	1.1468	1.0		
6	1.1681	1.4040	2.0562	1.5171	1.9029	0.8618	1.3554	

◆ Step 2 – look up table to find the desired design parameters (slope parameters)

$$Z_U = Z_0 \qquad \frac{x_3}{Z_0} = 8.6038$$

$$\frac{x_1}{Z_0} = \frac{x_5}{Z_0} = 14.8170 \qquad \frac{x_2}{Z_0} = \frac{x_4}{Z_0} = 12.3924$$

Figure 1.8 Step 1 and step 2 image description



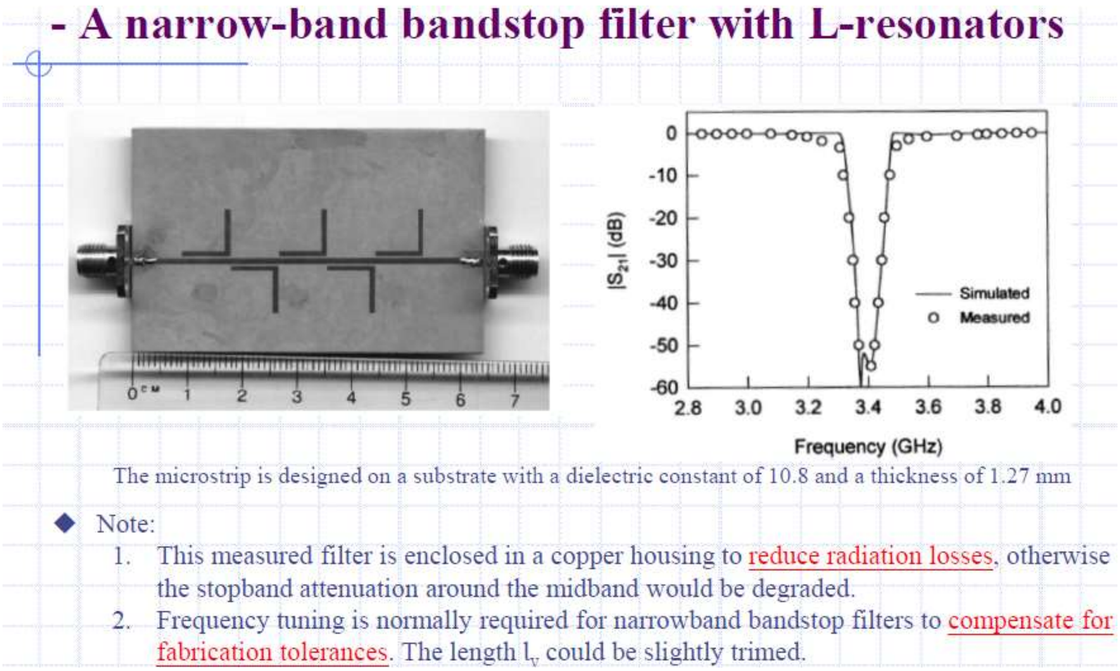
◆ Step 3 – determine the physical size of the L-resonators

☐ Length of L-resonators
l_h = 8.9 mm and l_v = 8.9 mm
(half guided wavelength)

☐ Spacing of main line and resonators
$\frac{f_0}{2\Delta f_{3dB}}$ from EM simulator
$s_1 = s_5 = 0.292$ mm
$s_2 = s_4 = 0.292$ mm
$s_3 = 0.292$ mm

Figure 1.7 Step 3 image description and how s parameters are obtained.

At the end the response and the application of this designed L resonator will response as expected (right image), and physically it will look like the one showed in the left image.



- A narrow-band bandstop filter with L-resonators

The microstrip is designed on a substrate with a dielectric constant of 10.8 and a thickness of 1.27 mm

- Note:
  1. This measured filter is enclosed in a copper housing to reduce radiation losses, otherwise the stopband attenuation around the midband would be degraded.
  2. Frequency tuning is normally required for narrowband bandstop filters to compensate for fabrication tolerances. The length l_v could be slightly trimed.

Figure 1.7 L resonator picture and expected response.

6. Theoretical Analysis.

Filter Specifications

Use bandstop filters when some unwanted interfering frequencies beparticularly strong; or when high attenuation may be needed only at certain frequencies.

Bandstop filter	Type of filter Cut off Frequency comes from F1= 3.3GHz and F2=3.5GHz.
fo := 3.4GHz	
FBW := 0.05	Bandwidth This comes from f2-f1/fo
n := 3	Filter order
ξr := 3.55	Dielectric constant of the material
Hi := 0.81mm	Height of the transmission line Rogers RO4003
Cheby := 0.1	Chebyshev=0.1dB

L shaped resonator

Wi := 2.224mm

Zo := 50Ω

g0 := 1.0

g1 := 1.0316

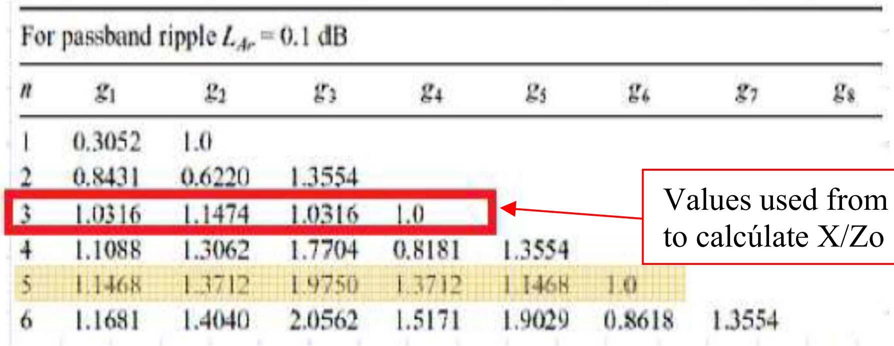
g2 := 1.1474

g3 := 1.0316

g4 := 1.0

g5 := 0

g6 := 0



For passband ripple $L_{Ar} = 0.1$ dB

n	g_1	g_2	g_3	g_4	g_5	g_6	g_7	g_8
1	0.3052	1.0						
2	0.8431	0.6220	1.3554					
3	1.0316	1.1474	1.0316	1.0				
4	1.1088	1.3062	1.7704	0.8181	1.3554			
5	1.1468	1.3712	1.9750	1.3712	1.1468	1.0		
6	1.1681	1.4040	2.0562	1.5171	1.9029	0.8618	1.3554	

Values used from table to calcúlate X/Zo

f1 := 3.23GHz

f2 := 3.57GHz

s1 := 0.292mm

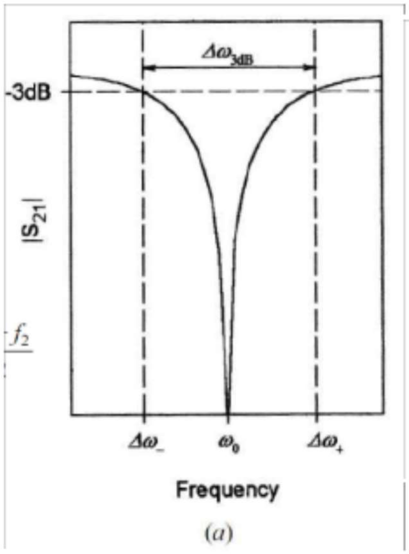
s2 := 0.221mm

s3 := 0.102mm

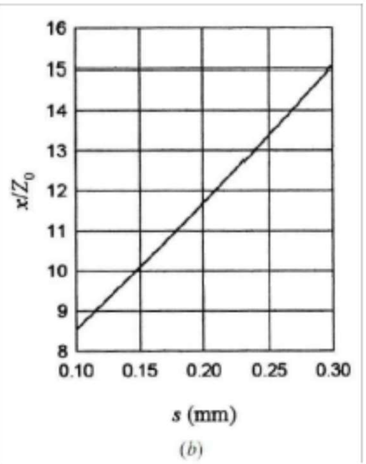
s4 := 0.221mm

s5 := 0.292mm

These values are references from previous example



(a)



(b)

FBW = 0.05

$$FBW2 := \frac{f2 - f1}{fo} = 0.1$$

$$fo\_calc := \frac{f1 + f2}{2} = 3.4 \cdot GHz$$

$fo\_calc2 := \sqrt{f1 \cdot f2} = 3.396 \cdot GHz$ This was used

$$f1\_FBW := fo \cdot FBW = 0.17 \cdot GHz$$

$$f2\_tol := fo + f1\_FBW = 3.57 \cdot GHz$$

$$f1\_tol := fo - f1\_FBW = 3.23 \cdot GHz$$

$$\Omega p := \frac{\Omega_c \cdot FBW}{\left(\frac{\omega}{\omega 0} - \frac{\omega 0}{\omega}\right)}$$

$$\omega 1_{3dB} := 3.43GHz \qquad fo\omega := 3.47GHz$$

$$\omega 2_{3dB} := 3.52GHz$$

$$X\_Zo := \frac{fo\omega}{2 \cdot \left(\omega 2_{3dB} - \omega 1_{3dB}\right)} = 19.278$$ for s=0.19mm

$$\omega 0 := \sqrt{\omega 1 \cdot \omega 2}$$

FBW =(ω2-ω1)/ω0

FBW =(f2-f1)/f0 with f0=(f1+f2)/2

$$X\_Zo1 := \frac{fo}{2 \cdot (f2 - f1)} = 5$$

x /Zo= ω0/(2Δω3dB) = f0/(2Δω3dB)

$$Rel_{Zu\_Zo\_SQR} := \frac{1}{g0(gn + 1)}$$ Relation between Zu and Zo

$$xi_{Li} := \omega 0Li$$

$$xi_{Ci} := \frac{1}{\omega 0Ci}$$

General equations, only for reference

$$xi\_Rel_{Zu\_Zo\_SQR} := Zo\left(\frac{Zu}{Zo}\right)^2 \cdot \frac{go}{gi\Omega_c \cdot FBW}$$ for i=1 to n

If Zul=Zo

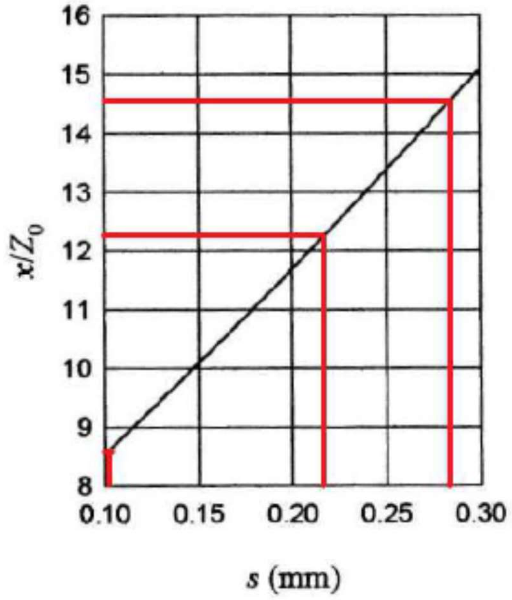
$$x1 := \frac{g0}{g1 \cdot (FBW)} \qquad x2 := \frac{g0}{g2 \cdot (FBW)} \qquad x3 := \frac{g0}{g3 \cdot (FBW)} \qquad x4 := \frac{g0}{g4 \cdot (FBW)}$$

$x1 = 19.387$ $x2 = 17.431$ $x3 = 19.387$ $x4 = 20$

The X/Zo values will be used for each L

$$x := \frac{fo}{g0(f2 - f1)} = 10$$

$s1 = 0.292 \cdot mm$
$s2 = 0.221 \cdot mm$
$s3 = 0.102 \cdot mm$
$s4 = 0.221 \cdot mm$
$s5 = 0.292 \cdot mm$



(*b*)

Example of how to graph S values from simulation results (x/Zo)

$$Ar := \frac{Zo}{60\Omega} \cdot \left[\sqrt{\frac{(\xi r + 1)}{2}} + \left(\frac{\xi r - 1}{\xi r + 1}\right) \cdot \left(0.23 + \frac{0.11}{\xi r}\right)\right]$$

Ar=A Pag 149 Pozar book

$$Ur := \frac{8e^{Ar}}{e^{2 \cdot Ar} - 2}$$

Ur= W/d<2 Pag 148 Pozar book

$$Br := \frac{377\pi \cdot \Omega}{2 \cdot Zo \cdot \sqrt{\xi r}}$$

Br = B

$$Ur2 := \frac{2}{\pi}\left[Br - 1 - \ln(2Br - 1) + \left[\left(\frac{\xi r - 1}{2\xi r}\right) \cdot \left(\ln(Br - 1) + 0.39 - \frac{0.61}{\xi r}\right)\right]\right]$$

Ur2=W/d >2

$$Areal := \begin{array}{|l} Ar \ \text{ if } (Ur \le 2) \\ Br \ \text{ otherwise} \end{array}$$

$Ar = 1.379$
$Br = 6.286$

$$Ureal := \begin{array}{|l} Ur \ \text{ if } (Ur \le 2) \\ Ur2 \ \text{ otherwise} \end{array}$$

$Ur = 2.308$
$Ur2 = 2.237$

$Areal = 6.286$

$\mathrm{Areal}_{\Omega} := \mathrm{Areal}\cdot\Omega = 6.286\,\Omega$

$\mathrm{Ureal} = 2.237$

$$\xi e_{Zo} := \frac{(\xi r + 1)}{2} + \frac{\xi r - 1}{2\sqrt{1 + \left(\frac{12}{\mathrm{Ureal}}\right)}}$$

$\xi e_{Zo} = 2.78$

$\mathrm{Wi\_real} := \mathrm{Ureal}\cdot\mathrm{Hi} = 1.812\cdot\mathrm{mm}$

$$\mathrm{Vp}_{\mu\mathrm{stripline\_Zo}} := \frac{c}{\sqrt{\xi e_{Zo}}}$$

$\mathrm{Vp}_{\mu\mathrm{stripline\_Zo}} = 1.798 \times 10^{8}\,\frac{m}{s}$

$$\lambda_{\mu\mathrm{stripline\_Zo}} := \frac{\mathrm{Vp}_{\mu\mathrm{stripline\_Zo}}}{\mathrm{fo}}$$

$\lambda_{\mu\mathrm{stripline\_Zo}} = 52.88\cdot\mathrm{mm}$

$\mathrm{Box\_size\_increase} := 5\cdot\mathrm{Hi} = 4.05\cdot\mathrm{mm}$

Regla de dedo para incrementar la caja para los lados

$\mathrm{Wi\_real} = 1.812\cdot\mathrm{mm}$

$$\mathrm{lo}_{\mu\mathrm{stripline\_Zo}} := \frac{\mathrm{Vp}_{\mu\mathrm{stripline\_Zo}}}{4\mathrm{fo}} = 13.22\cdot\mathrm{mm}$$ Length of L-resonators

$$\mathrm{lo}_{\mu\mathrm{stripline\_Zo\_2}} := \frac{\lambda_{\mu\mathrm{stripline\_Zo}}}{4} = 13.22\cdot\mathrm{mm}$$ Length of L-resonators

Values used for the design of the 3-L resonator (Stop band filter)

$$\mathrm{lo}_{\mu\mathrm{stripline\_Zo\_U\_Wi\_3}} := \frac{\lambda_{\mu\mathrm{stripline\_Zo}}}{2} = 26.44\cdot\mathrm{mm}$$

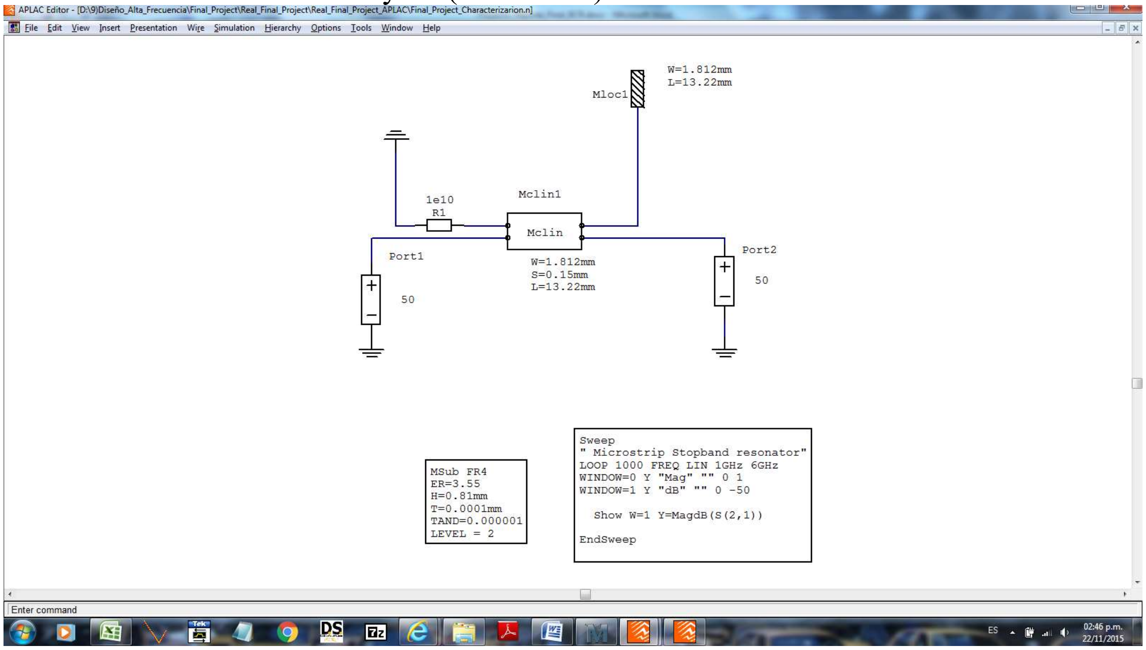
7. Practical microstrip realization.

A) Based on calculation a 1 L resonator is built up and simulated to get s values depending on cut-off Frequency. S was moved manually to get the values that provide x/Zo

X1	x2	X3
19.387	17.431	19.387

Values of x/Zo from

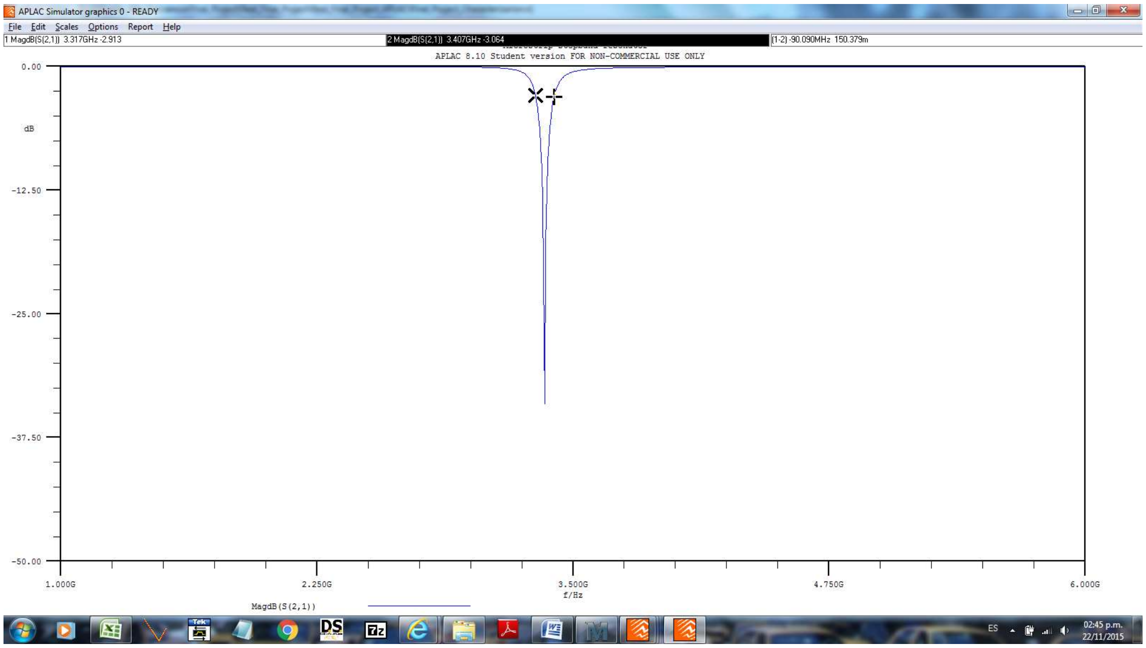
APLAC L-resonator circuit layout (s=0.15mm)



```
MSub FR4
ER=3.55
H=0.81mm
T=0.0001mm
TAND=0.000001
LEVEL = 2
```

```
Sweep
" Microstrip Stopband resonator"
LOOP 1000 FREQ LIN 1GHz 6GHz
WINDOW=0 Y "Mag" "" 0 1
WINDOW=1 Y "dB" "" 0 -50

  Show W=1 Y=MagdB(S(2,1))

EndSweep
```

L resonator circuit results (Bandwidth)


APLAC Simulator graphics 0 - READY

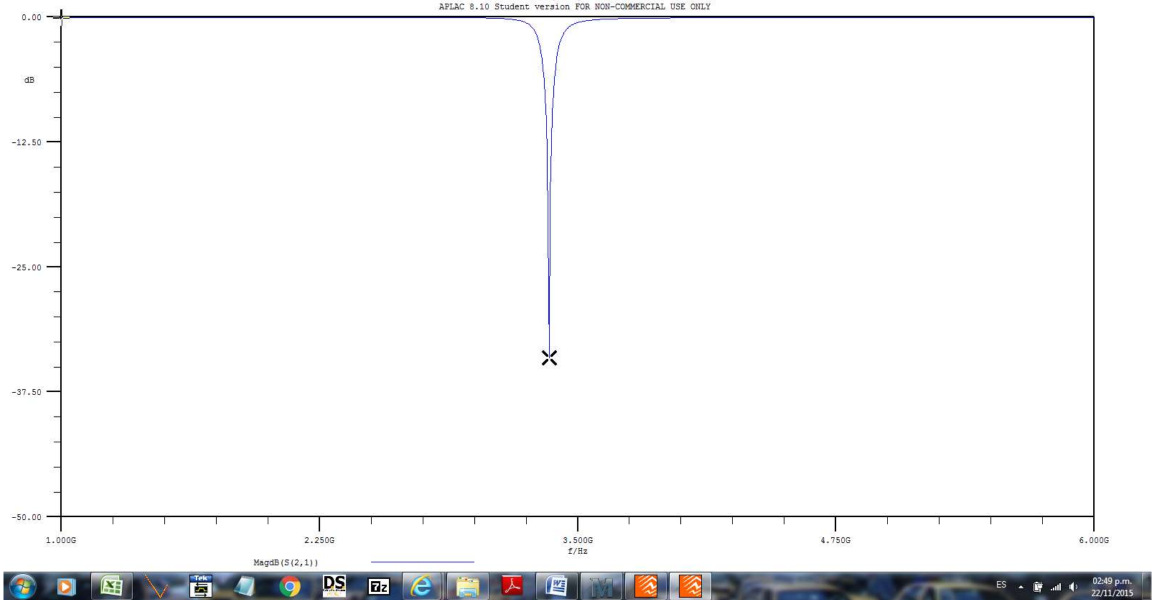
1 MagdB(S(2,1)) 3.317GHz -2.913

2 MagdB(S(2,1)) 3.407GHz -3.064

(1-2) -90.090MHz 150.379m

APLAC 8.10 Student version FOR NON-COMMERCIAL USE ONLY

L resonator circuit results (Cut off Frequency)


APLAC Simulator graphics 0 - READY

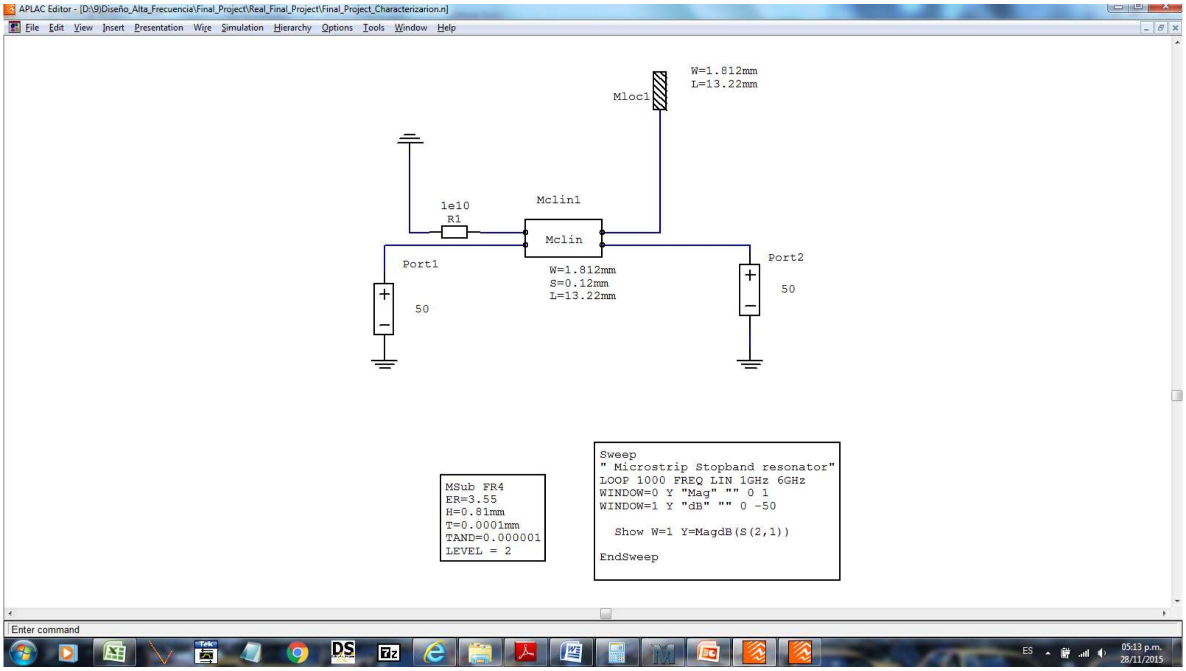
1 MagdB(S(2,1)) 3.362GHz -34.106

2 MagdB(S(2,1)) 1.000GHz -3.994m

(1-2) 2.362GHz -34.102

APLAC 8.10 Student version FOR NON-COMMERCIAL USE ONLY

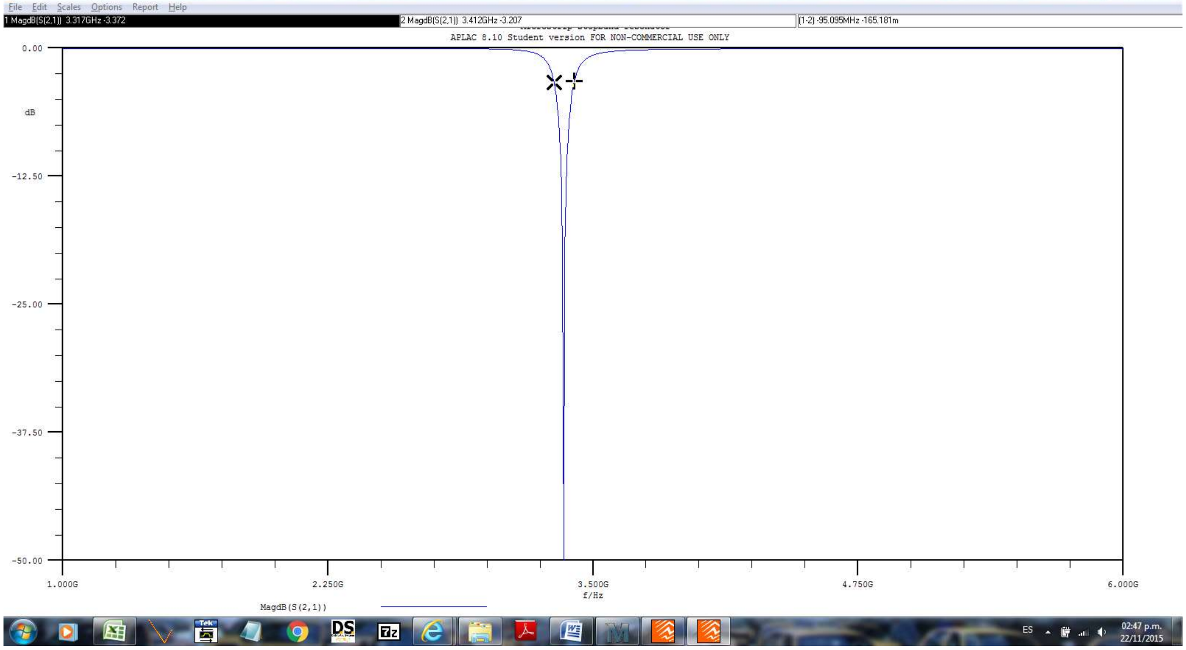
APLAC L-resonator circuit layout (s=0.12mm)


APLAC Editor - [D:\9)Diseño_Alta_Frecuencia\Final_Project\Real_Final_Project\Final_Project_Characterizarion.n]

```
MSub FR4
ER=3.55
H=0.81mm
T=0.0001mm
TAND=0.000001
LEVEL = 2
```

```
Sweep
" Microstrip Stopband resonator"
LOOP 1000 FREQ LIN 1GHz 6GHz
WINDOW=0 Y "Mag" "" 0 1
WINDOW=1 Y "dB" "" 0 -50

  Show W=1 Y=MagdB(S(2,1))

EndSweep
```

L resonator circuit results (Bandwidth)

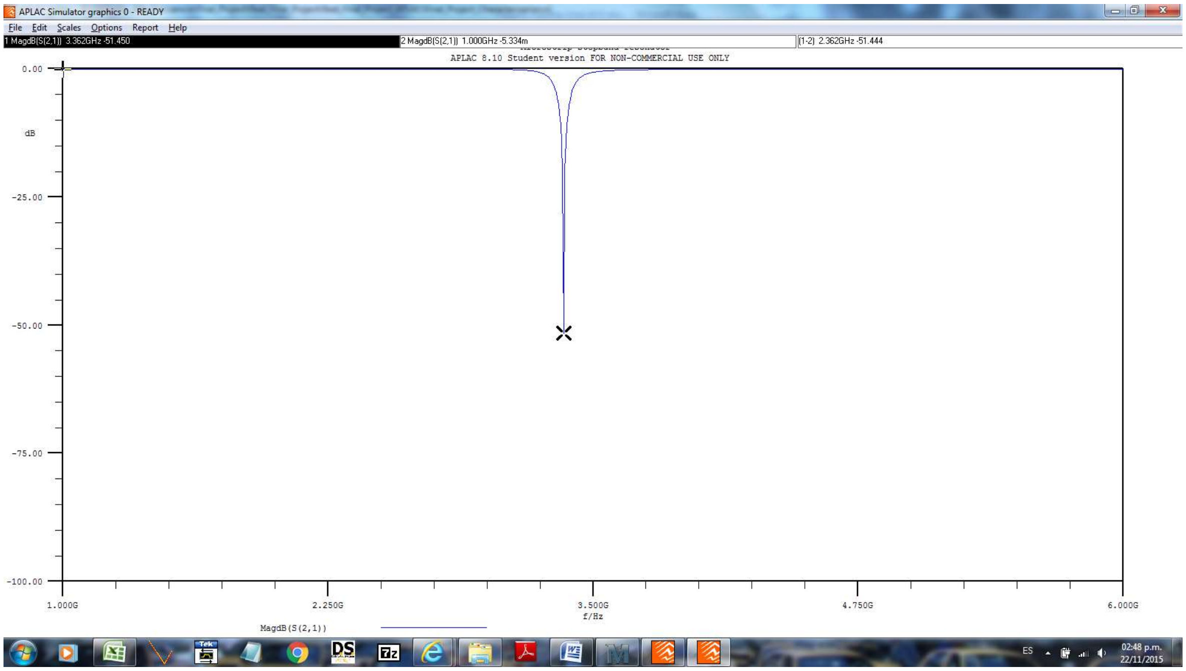

APLAC Simulator graphics 0 - READY

1 MagdB(S(2,1)) 3.317GHz -3.372

2 MagdB(S(2,1)) 3.412GHz -3.207

(1-2) -95.095MHz -165.181m

L resonator circuit results (Cut off Frequency)



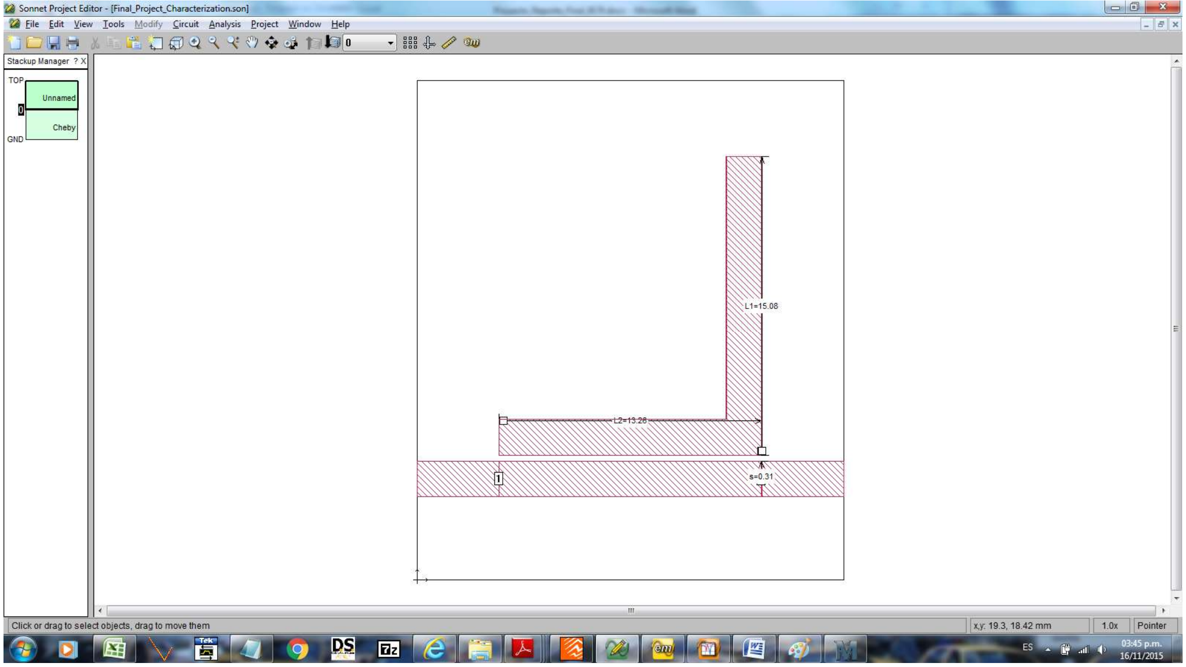
B) In the next table the S results extracted from APLAC simulation.

		APLAC			L=13.22mm in Mloc1	
	fo	f1(menor)	f2(mayor)	X/Z0	s (mm)	dB
1	3.362	3.262	3.472	8.004762	0.01	
2	3.362	3.277	3.457	9.338889	0.02	
3	3.362	3.282	3.452	9.888235	0.03	
4	3.362	3.292	3.442	11.20667	0.04	
5	3.362	3.297	3.437	12.00714	0.05	
6	3.362	3.302	3.432	12.93077	0.06	
7	3.362	3.302	3.427	13.448	0.07	
8	3.362	3.307	3.422	14.61739	0.08	
9	3.362	3.312	3.422	15.28182	0.09	
10	3.362	3.312	3.417	16.00952	0.1	
11	3.362	3.312	3.417	16.00952	0.11	
12	3.362	3.317	3.412	17.69474	0.12	
13	3.362	3.317	3.412	17.69474	0.13	
14	3.362	3.317	3.407	18.67778	0.14	
15	3.362	3.322	3.407	19.77647	0.15	
16	3.362	3.322	3.402	21.0125	0.16	
17	3.362	3.322	3.402	21.0125	0.17	
18	3.362	3.322	3.402	21.0125	0.18	

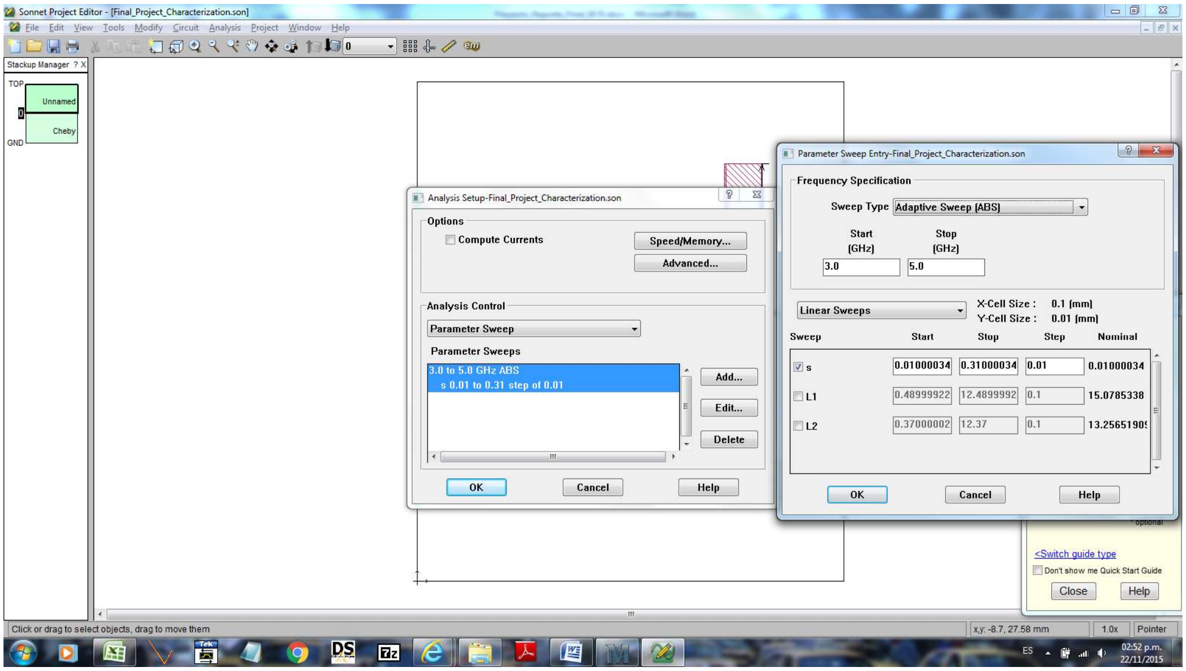
19	3.362	3.327	3.397	24.01429	0.19
20	3.362	3.327	3.397	24.01429	0.2
21	3.357	3.327	3.397	23.97857	0.21
22	3.357	3.327	3.392	25.82308	0.22
23	3.357	3.327	3.392	25.82308	0.23
24	3.357	3.327	3.392	25.82308	0.24
25	3.357	3.332	3.387	30.51818	0.25
26	3.357	3.332	3.387	30.51818	0.26
27	3.357	3.332	3.387	30.51818	0.27
28	3.357	3.332	3.387	30.51818	0.28
29	3.357	3.332	3.387	30.51818	0.29
30	3.357	3.332	3.382	33.57	0.3
31	3.362	3.332	3.382	33.62	0.31

C) And to corroborate the results a Sonet simulation was run too. To get this an s parameterization run was done automatically.

Sonet L-resonator circuit layout (Parameter sweet from 0.01mm to 0.31mm)



Simulation set up for Parameter sweep (s parameter)



Analysis Setup-Final_Project_Characterization.son

Options

☐ Compute Currents

Analysis Control: Parameter Sweep

Parameter Sweeps:

3.0 to 5.0 GHz ABS
  s 0.01 to 0.31 step of 0.01

Parameter Sweep Entry-Final_Project_Characterization.son

Frequency Specification

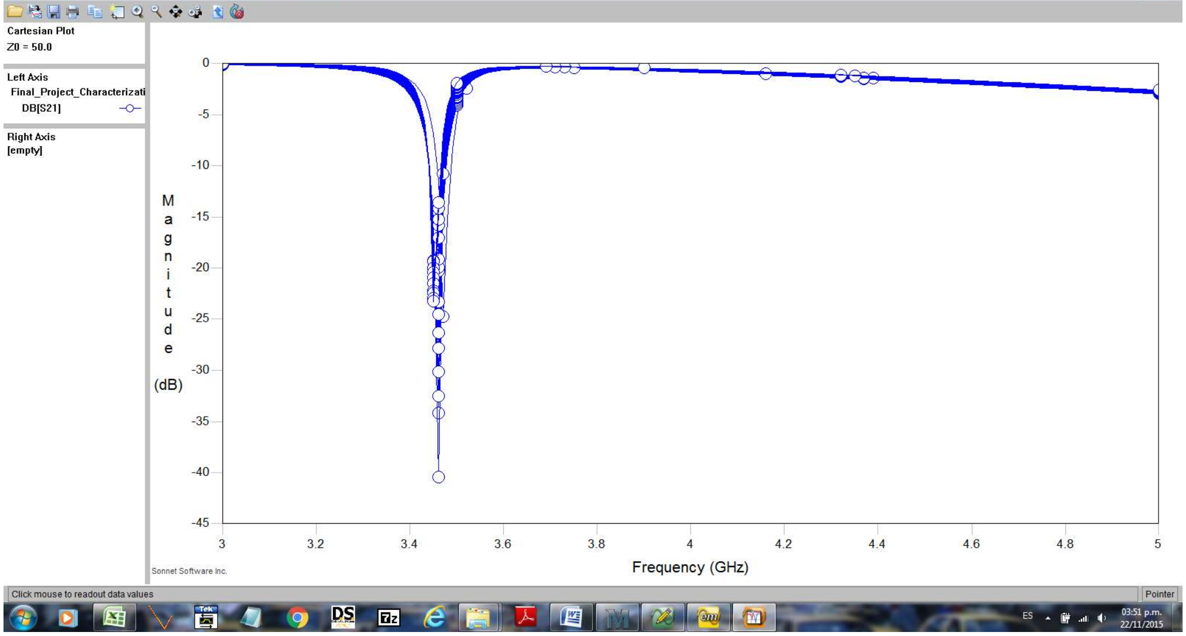
Sweep Type: Adaptive Sweep (ABS)

Start (GHz): 3.0
Stop (GHz): 5.0

Linear Sweeps
X-Cell Size : 0.1 (mm)
Y-Cell Size : 0.01 (mm)

Sweep	Start	Stop	Step	Nominal
☑ s	0.01000034	0.31000034	0.01	0.01000034
☐ L1	0.48999922	12.4899992	0.1	15.0785338
☐ L2	0.37000002	12.37	0.1	13.2565190

L resonator circuit results (Parametrization)

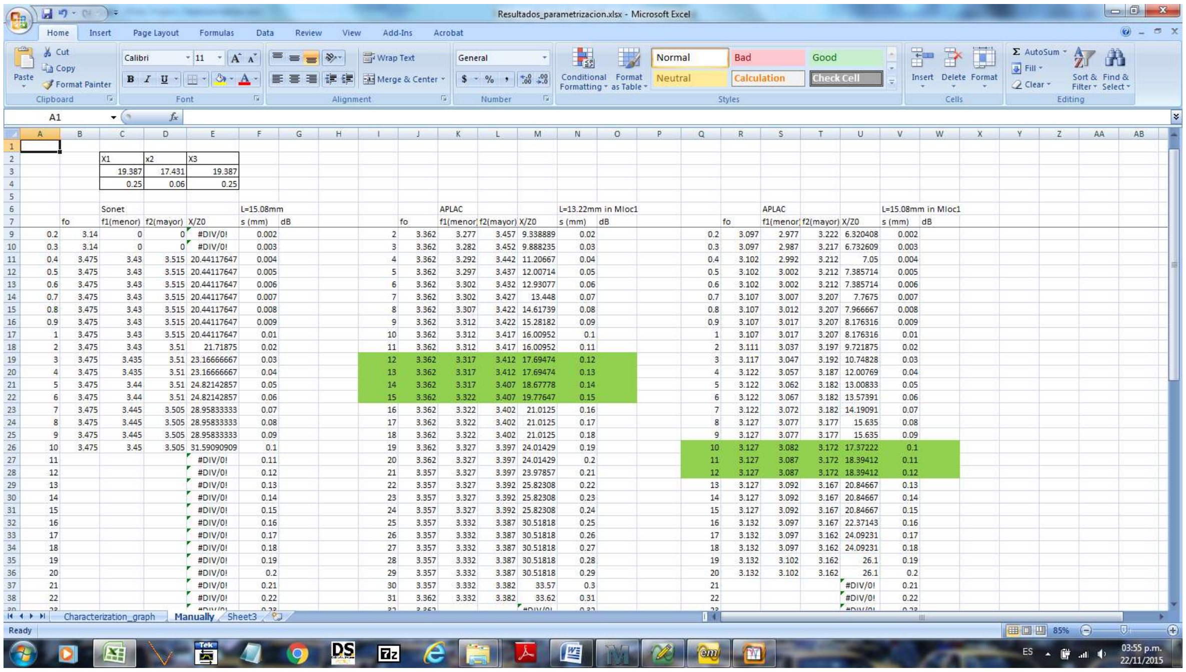


D) In the next table the S results extracted from the Sonnet simulation.

		Sonet			L=15.08mm	
	fo	f1(menor)	f2(mayor)	X/Z0	s (mm)	dB
0.1	3.14	0	0	#DIV/0!	0.001	

0.2	3.14	0	0	#DIV/0!	0.002
0.3	3.14	0	0	#DIV/0!	0.003
0.4	3.475	3.43	3.515	20.44117647	0.004
0.5	3.475	3.43	3.515	20.44117647	0.005
0.6	3.475	3.43	3.515	20.44117647	0.006
0.7	3.475	3.43	3.515	20.44117647	0.007
0.8	3.475	3.43	3.515	20.44117647	0.008
0.9	3.475	3.43	3.515	20.44117647	0.009
1	3.475	3.43	3.515	20.44117647	0.01
2	3.475	3.43	3.51	21.71875	0.02
3	3.475	3.435	3.51	23.16666667	0.03
4	3.475	3.435	3.51	23.16666667	0.04
5	3.475	3.44	3.51	24.82142857	0.05
6	3.475	3.44	3.51	24.82142857	0.06
7	3.475	3.445	3.505	28.95833333	0.07
8	3.475	3.445	3.505	28.95833333	0.08
9	3.475	3.445	3.505	28.95833333	0.09
10	3.475	3.45	3.505	31.59090909	0.1

E) In the next table the S results extracted from the both circuits simulated.



X1	x2	X3
19.387	17.431	19.387
0.25	0.06	0.25

		Sonet			L=15.08mm	
	fo	f1(menor)	f2(mayor)	X/Z0	s (mm)	dB
0.2	3.14	0	0	#DIV/0!	0.002	
0.3	3.14	0	0	#DIV/0!	0.003	
0.4	3.475	3.43	3.515	20.44117647	0.004	
0.5	3.475	3.43	3.515	20.44117647	0.005	
0.6	3.475	3.43	3.515	20.44117647	0.006	
0.7	3.475	3.43	3.515	20.44117647	0.007	
0.8	3.475	3.43	3.515	20.44117647	0.008	
0.9	3.475	3.43	3.515	20.44117647	0.009	
1	3.475	3.43	3.515	20.44117647	0.01	
2	3.475	3.43	3.51	21.71875	0.02	
3	3.475	3.435	3.51	23.16666667	0.03	
4	3.475	3.435	3.51	23.16666667	0.04	
5	3.475	3.44	3.51	24.82142857	0.05	
6	3.475	3.44	3.51	24.82142857	0.06	
7	3.475	3.445	3.505	28.95833333	0.07	
8	3.475	3.445	3.505	28.95833333	0.08	
9	3.475	3.445	3.505	28.95833333	0.09	
10	3.475	3.45	3.505	31.59090909	0.1	
11				#DIV/0!	0.11	
12				#DIV/0!	0.12	
13				#DIV/0!	0.13	
14				#DIV/0!	0.14	
15				#DIV/0!	0.15	
16				#DIV/0!	0.16	
17				#DIV/0!	0.17	
18				#DIV/0!	0.18	
19				#DIV/0!	0.19	
20				#DIV/0!	0.2	
21				#DIV/0!	0.21	
22				#DIV/0!	0.22	

		APLAC			L=13.22mm in Mloc1	
	fo	f1(menor	f2(mayor)	X/Z0	s (mm)	dB
2	3.362	3.277	3.457	9.338889	0.02	
3	3.362	3.282	3.452	9.888235	0.03	
4	3.362	3.292	3.442	11.20667	0.04	
5	3.362	3.297	3.437	12.00714	0.05	
6	3.362	3.302	3.432	12.93077	0.06	
7	3.362	3.302	3.427	13.448	0.07	
8	3.362	3.307	3.422	14.61739	0.08	
9	3.362	3.312	3.422	15.28182	0.09	
10	3.362	3.312	3.417	16.00952	0.1	
11	3.362	3.312	3.417	16.00952	0.11	
12	3.362	3.317	3.412	17.69474	0.12	
13	3.362	3.317	3.412	17.69474	0.13	
14	3.362	3.317	3.407	18.67778	0.14	
15	3.362	3.322	3.407	19.77647	0.15	
16	3.362	3.322	3.402	21.0125	0.16	
17	3.362	3.322	3.402	21.0125	0.17	
18	3.362	3.322	3.402	21.0125	0.18	
19	3.362	3.327	3.397	24.01429	0.19	
20	3.362	3.327	3.397	24.01429	0.2	
21	3.357	3.327	3.397	23.97857	0.21	
22	3.357	3.327	3.392	25.82308	0.22	
23	3.357	3.327	3.392	25.82308	0.23	
24	3.357	3.327	3.392	25.82308	0.24	
25	3.357	3.332	3.387	30.51818	0.25	
26	3.357	3.332	3.387	30.51818	0.26	
27	3.357	3.332	3.387	30.51818	0.27	
28	3.357	3.332	3.387	30.51818	0.28	
29	3.357	3.332	3.387	30.51818	0.29	
30	3.357	3.332	3.382	33.57	0.3	
31	3.362	3.332	3.382	33.62	0.31	

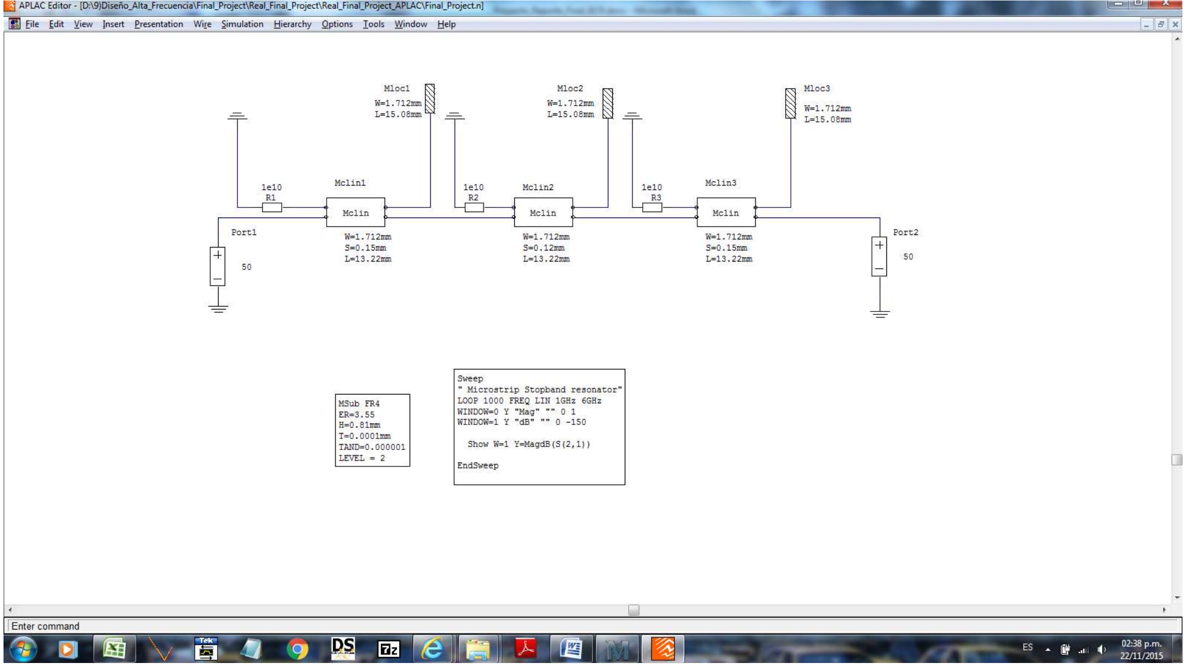
		APLAC			L=15.08mm in Mloc1	
	fo	f1(menor	f2(mayor)	X/Z0	s (mm)	dB
0.2	3.097	2.977	3.222	6.320408	0.002	
0.3	3.097	2.987	3.217	6.732609	0.003	
0.4	3.102	2.992	3.212	7.05	0.004	
0.5	3.102	3.002	3.212	7.385714	0.005	
0.6	3.102	3.002	3.212	7.385714	0.006	
0.7	3.107	3.007	3.207	7.7675	0.007	
0.8	3.107	3.012	3.207	7.966667	0.008	
0.9	3.107	3.017	3.207	8.176316	0.009	
1	3.107	3.017	3.207	8.176316	0.01	
2	3.111	3.037	3.197	9.721875	0.02	
3	3.117	3.047	3.192	10.74828	0.03	
4	3.122	3.057	3.187	12.00769	0.04	
5	3.122	3.062	3.182	13.00833	0.05	
6	3.122	3.067	3.182	13.57391	0.06	
7	3.122	3.072	3.182	14.19091	0.07	
8	3.127	3.077	3.177	15.635	0.08	
9	3.127	3.077	3.177	15.635	0.09	
10	3.127	3.082	3.172	17.37222	0.1	
11	3.127	3.087	3.172	18.39412	0.11	
12	3.127	3.087	3.172	18.39412	0.12	
13	3.127	3.092	3.167	20.84667	0.13	
14	3.127	3.092	3.167	20.84667	0.14	
15	3.127	3.092	3.167	20.84667	0.15	
16	3.132	3.097	3.167	22.37143	0.16	
17	3.132	3.097	3.162	24.09231	0.17	
18	3.132	3.097	3.162	24.09231	0.18	
19	3.132	3.102	3.162	26.1	0.19	
20	3.132	3.102	3.162	26.1	0.2	
21				#DIV/0!	0.21	
22				#DIV/0!	0.22	

F) Optimization phase.

This was not done because the ITESO lab computers have problems to run APLAC and Sonnet licenses; therefore, no optimization results are available.

G) Once all the S parameters are known, the complete 3 sections L resonator is built up and, in both simulators,

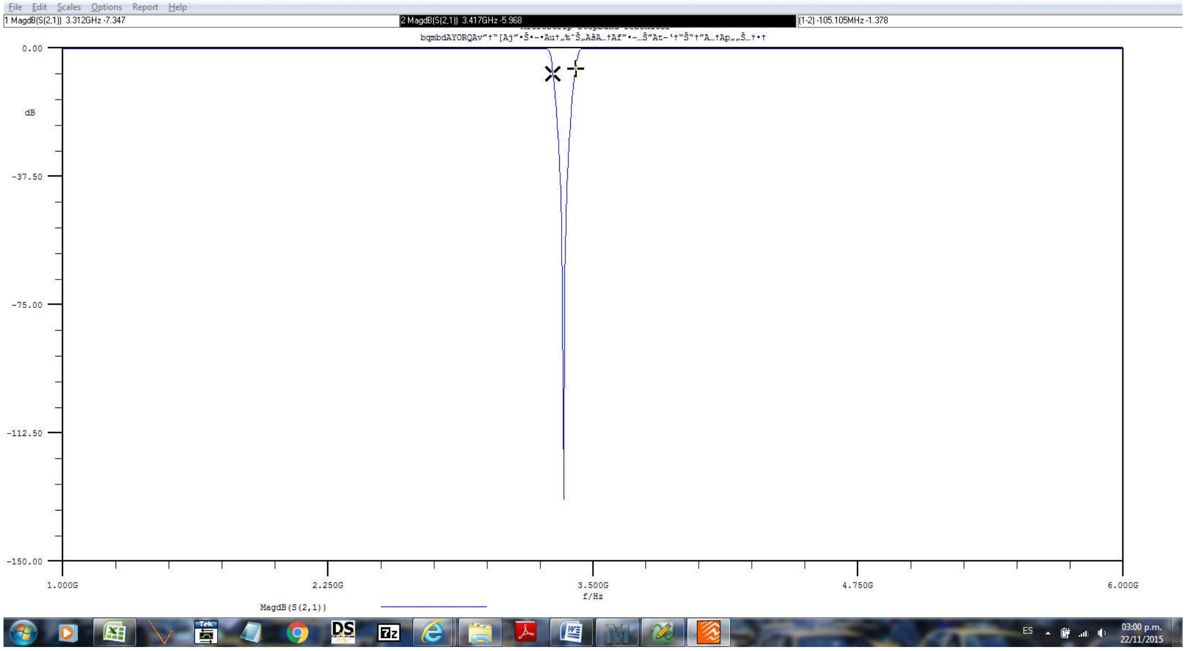
APLAC 3 sections L-resonator circuit layout



```
MSub FR4
ER=3.55
H=0.81mm
T=0.0001mm
TAND=0.000001
LEVEL = 2
```

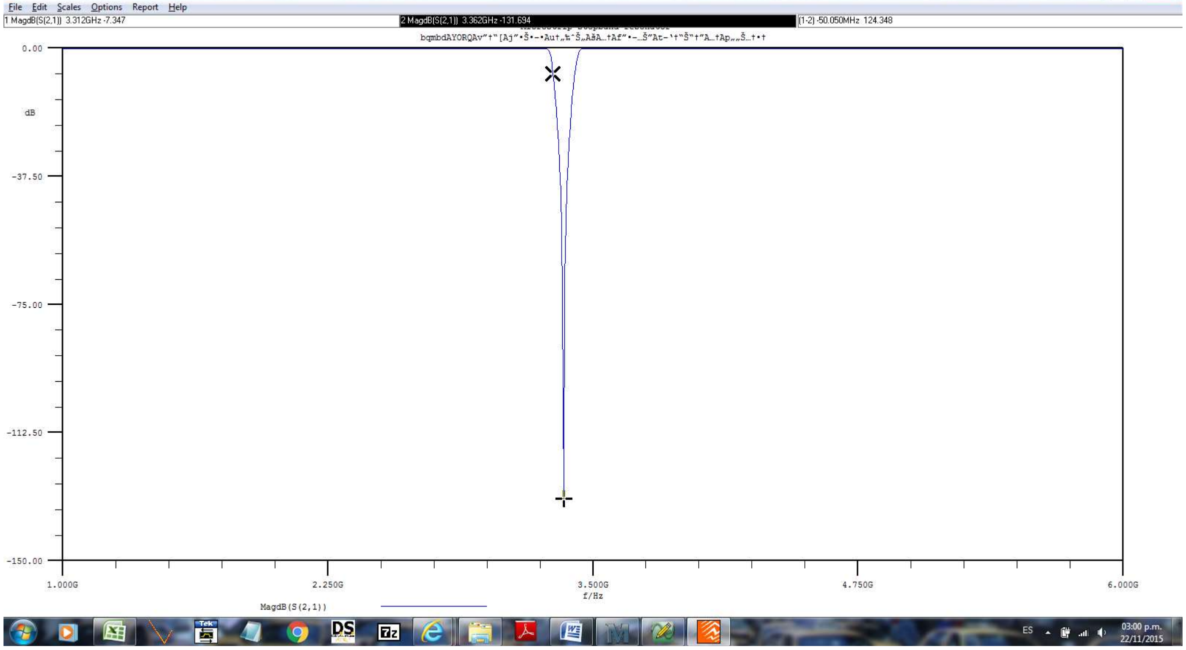
```
Sweep
" Microstrip Stopband resonator"
LOOP 1000 FREQ LIN 1GHz 6GHz
WINDOW=0 Y "Mag" "" 0 1
WINDOW=1 Y "dB" "" 0 -150

  Show W=1 Y=MagdB(S(2,1))

EndSweep
```

3-L resonator circuit results (Bandwidth)



```
1 MagdB(S(2,1)) 3.312GHz -7.347
2 MagdB(S(2,1)) 3.417GHz -5.968
(1-2) -105.105MHz -1.378
```

3-L resonator circuit results (Cut off Frequency)



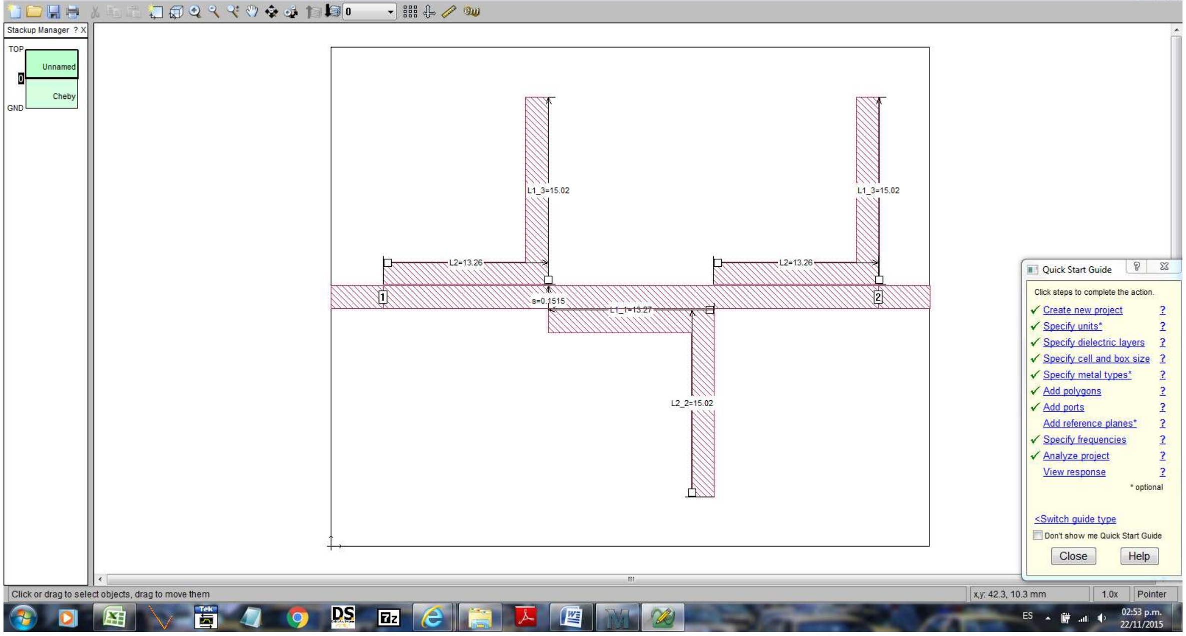
APLAC Simulator graphics 0 - READY

1 MagdB(S(2,1)) 3.312GHz -7.347

2 MagdB(S(2,1)) 3.362GHz -131.694

[1-2] -50.050MHz 124.348

Sonnet 3 sections L-resonator circuit layout



Sonnet Project Editor - [Final_Project.son]

Quick Start Guide

Click steps to complete the action.

- ✓ Create new project ?
- ✓ Specify units* ?
- ✓ Specify dielectric layers ?
- ✓ Specify cell and box size ?
- ✓ Specify metal types* ?
- ✓ Add polygons ?
- ✓ Add ports ?
- Add reference planes* ?
- ✓ Specify frequencies ?
- ✓ Analyze project ?
- View response ?

* optional

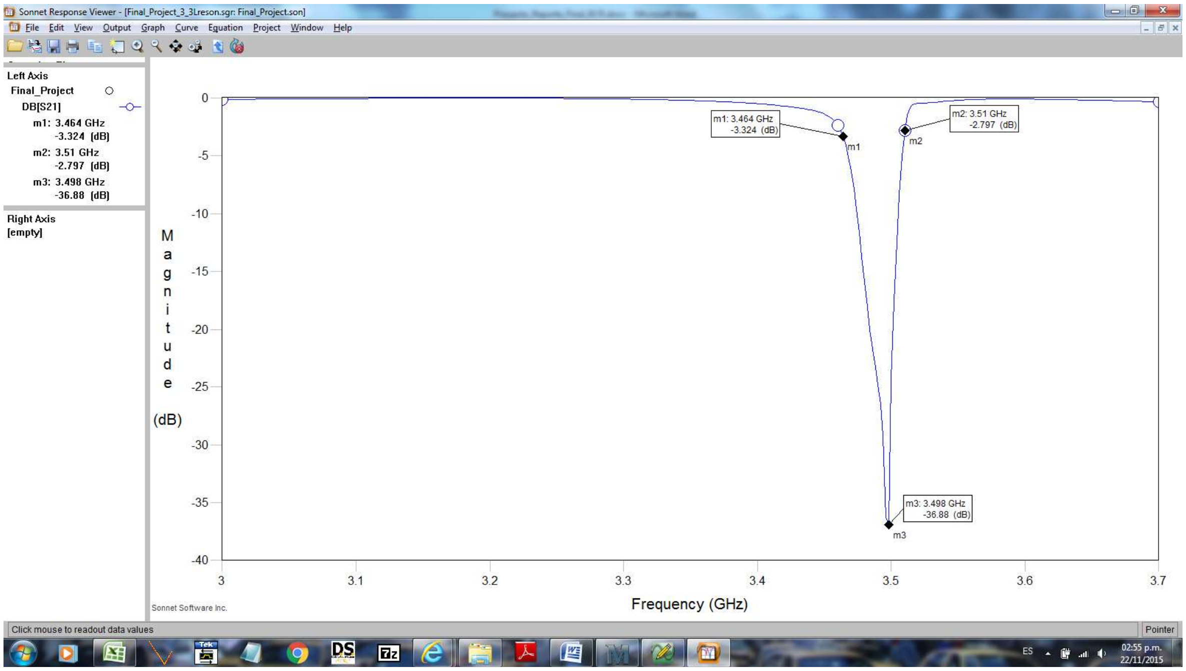
<Switch guide type

☐ Don't show me Quick Start Guide

Click or drag to select objects, drag to move them

x,y: 42.3, 10.3 mm

3-L resonator circuit results



H) Optimization phase.

This was not done because the ITESO lab computers have problems to run APLAC and Sonnet licenses; therefore, no optimization results are available.

8. Discussion of results.

Specification fulfillment vs Simulation results.

Parameter	Specification values	APLAC results	Sonnet results
Center frequency (fc)	3.4GHz	3.362GHZ	3.49GHz
Fractional Bandwidth (%)	5%	3%	1.35%
Fractional Bandwidth (MHz)	170	105	46

9. Conclusions.

->Length of the resonators changes the cut-off frequency.
->s distance can change bandwidth of the filter.
->Metallic box in the simulator can reduce/ increase transmission losses.
->Calculation helps just to get a starting point or the "seed" to start with, but once the 3 L resonators were together a new adjustment was necessary.
->APLAC vs Sonnet simulators response was different; the reason might be because APLAC is a general purpose electrical circuit simulator and Sonnet is an Electromagnetic effect simulator.
-> This was not done because the ITESO lab computers have problems to run APLAC and Sonnet licenses; therefore, no optimization results are available.

10. Bibliography.

[1] Subject notes and class presentations by Jose Ernesto Rayas Sanchez Phd.
[2] Lecture number 7 Transmission line matching using lumped L networks by Keith W. Whites
[3] Lecture Microwave filter design. by Prof. Tzong-Lin Wu
[4] Lecture Circuit design optimization by Jose Ernesto Rayas Sanchez Phd.
[5] Filter Handbook: A practical design guide by Stefan Niewiadomski

B. MODELING A STRAIN GAUGE AND CONDITIONING CIRCUIT FOR A NATURAL VACUUM LEAK DETECTION (NVLD) SYSTEM.

Final Project.

Modeling a strain gauge and conditioning circuit for a natural vacuum leak detection (NVLD) system.

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Simulation Methods for Electronics Circuits
José Ernesto Rayas Sánchez PhD.
18/May/2016

Abstract: In this document, a strain gauge is modeled based on the main design parameters to show a real case and the signal conditioning circuit that could be used to represent the variations of the pressure in a vacuum system and translate them in readable information for Power-train Control Module (PCM). This embodiment would be designed with commercial components, pressure values and voltage/current levels of automotive industry. All the calculations are performed in Matlab and the circuits simulations are developed in SPICE 3. Finally, the purpose of this embodiment is an option to substitute the current vacuum system with a more accurate and fair price design using the state of the art.

1. Introduction.

Since 1996 automobile emission control has been a worldwide concern, systems and methodologies have been developed to minimize this. One way is to recirculate gases back into the engine and burn them off before leaving to the outside world. This is done using a control method by measuring the vacuum leakage/pressure in the gas tank. In order to do that, gas law and pressure difference at certain time are measured every lap the engine is off. The "heart" of this system is the Natural Vacuum Leak detection (NVLD) system, which uses a diaphragm vacuum valve and an electromechanical switch as explained in **2.NVLD system brief description**. Due to both parts are mechanical pieces, another option is developed and described in this document using state of the art components. Using a strain gauge, described in **3. Resistance gauge principles and design,** and signal conditioning circuit, summarized in **4.Circuit conditioning design**, as proposals. Mechanical assumptions, electrical parameters and functional theory are described. For calculation of the system elements Matlab R2014a is used in order to have a reliable results and a solid foreseen of the behavior. In terms of simulation, all system are run in SPICE3 program (from Berkeley University) using a Sensor modeling method. Signal handling is done through common OpAmp (Instrumentation amplifier + comparator) configurations and active BJT-resistor switch, reference in section **5.Complete vacuum embodiment simulation in SPICE**. All these, following real design parameters used in current vehicles.

2. NVLD system brief description.

Natural Vacuum leak detection is a vacuum diaphragm valve patented by Chrysler to check on any possible leak in the emission system, in order to avoid any gas created in the vehicle gas tank due to chemical-air reaction (between gasoline and ambient conditions) to be escaped.
In figure 1 is the basic diagram of the NVLD system:

Basically, the connection To Canister is full of gas generated in the gasoline tank and is accumulated in the canister. This gas pressure goes into a "secret" internal passage up to the top of the diaphragm. The Pressure/Vacuum Relief Valve is de-energized to seal the system by means of Canister vacuum that overcomes Spring and Plunger pressure. Then atmospheric pressure comes from outside world through To Remove Filter .While the diaphragm has canister pressure (vacuum=2.2"H2O=548Pa) on top, the bottom is full of atmospheric pressure. Due to the pressure difference, this makes diaphragm goes up and activates Vacuum Switch, this switch changes from open state (>500kOhms) to close state (<100 ohms). This variation goes to the Power-train Control Module through Electrical Connector to process the response and send a signal control to activate the Solenoid and relieve the canister either pressure or vacuum to the outside world.

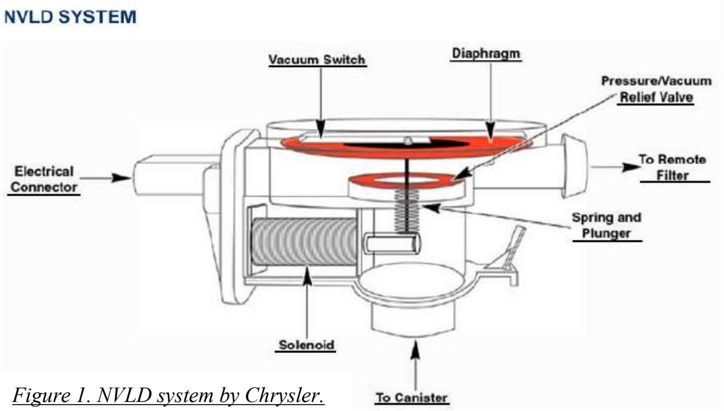


Figure 1. NVLD system by Chrysler.

3. Resistance gauge principles and design.

So the proposal or embodiment for this NVLD system is to replace the mechanical membrane or diaphragm with a piezo-resistive material diaphragm named Strain gauge.

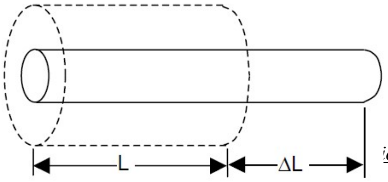
Electrical properties of resistive gauge.

The fundamental formula for the resistance of a wire with uniform cross section, A, and Resistivity ρ, can be expressed as:

$$R=\rho * L/A$$

Where L is the wire length. This relation is generally accurate for common metals and many nonmetals at room temperature when subjected to direct or low frequency currents.

The gauge to be formed from a length of uniform wire and subjected to an elongation is shown in figure 2:



ion.

The change in resistance can be expressed from previous equation as

$$\Delta R=\rho*L/A-(\rho+\Delta\rho)*(L+\Delta L/A+\Delta A)$$

Where: ΔR= Change in resistance, ρ = Resistivity of material
L = Length of the material, A= Cross section area of the material
ΔL= Change in length due to pressure, ΔA= Change in Area due to pressure
Finally adding ε and υ, the resistance change per unit resistance ($\Delta R/R$) can be written as:

$$dR/R = d\rho/\rho+(1+2\upsilon)*\varepsilon = GF*\varepsilon \text{ and if } R=Ro(1+x) \text{ then } Rx=Ro(1+GF*\varepsilon)$$

ε = Strain, υ=Poisson strain, G=Gauge factor, Ro=Resistance @25°C

Strain gauge theory.

Due to low cost, micro size, low pressure handling, best temperature compensation and reject bending strain, a strain gauge will be used. The Constantan alloy (Nickel/Copper) would be option B (figure 3), but for option A (figure 4), semiconductor (Crystal of Silicon) is the one selected for this embodiment. Figure 5 is a simulation stress picture of a Strain gauge at certain frequencies.

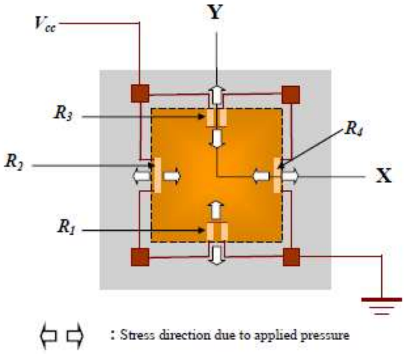


Figure 3. Strain gauge Wheatstone bridge with Constantan.

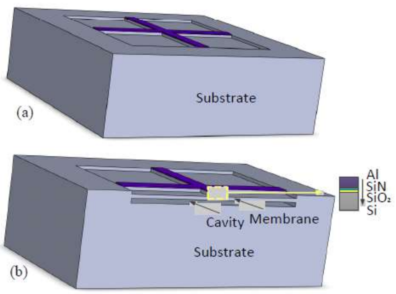


Figure 4. Strain gauge Wheatstone bridge with Si.

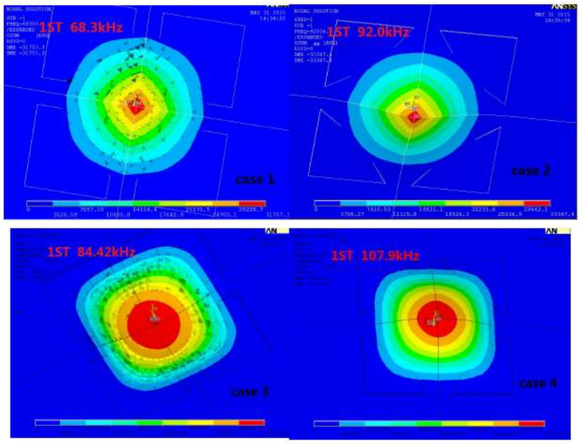


Figure 5. Strain gauge pressure simulation.

For semiconductor piezoresistor $\Delta R/R=\Delta\rho/\rho=\pi l*\sigma l+ \pi t*\sigma t$. Then substituting piezoresistive equation $Rx=Ro(1+\alpha T+G*\varepsilon)$ with $\pi l*\sigma l+ \pi t*\sigma t$,
We got $Rx=Ro(1+\alpha T+ \pi l*\sigma l+ \pi t*\sigma t)$
πl & πt = longitudinal and transverse piezoresistance coefficients
σl & σt = longitudinal and transverse stress
ΔT= Temp change, α=Material temp coefficient

Diaphragm theory.

The radial and tangential strains at the center of the diaphragm are identical, and expressed by:

$$\varepsilon RC=\varepsilon TC=3*P*Ro*(1-\upsilon^2)/8t^2*E$$

Where:
P = Pressure (Pa)
Ro = Diaphragm Radius (mm)

t = Diaphragm thickness (mm)
υ= Poisson’s ratio (dimensionless)
E = Young´s Modulus of elasticity (Pa)

Strain gauge design.

First step was to collect certain values to model a close Semiconductor diaphragm piezoresistive strain gauge, for accomplish this the next values were investigated from different documents:
From real values of a Semiconductor strain gauge (Piezoresistance in silicon.ppt Dr Lynn Fuller, 2016).
Ymax = 1 µm, b=4 µm, h=2µm, L=100 µm
Thickness = 10 µm Diameter 75 mm
In the <110> direction the next piezoresistive coefficients (Compressive strain-holes mobility) are gotten
πl= 71.8e-11 (1/Pa)
πt= -66.3e-11 (1/Pa)

And elastic constants of plain silicon Exx, Exy, Eyy and Gxy (Simulation of Circular Silicon Pressure Sensors with a Center Boss for Very Low Pressure Measurement Akio Yasukawa, 1989) obtained from coordinate transformation.
Exx=1.891x10^5 MPa
Exy=0.530x10^5 MPa
Eyy=1.4571x10^5 MPa

All these parameters were introduced in Matlab to get the x directed normal stress (σl) and the y directed normal stress (σt) solving the next matrices:

$$\begin{bmatrix} \sigma_x \\ \sigma_y \\ \tau_{xy} \end{bmatrix} = \begin{bmatrix} E_{xx} & E_{xy} & 0 \\ E_{xy} & E_{yy} & 0 \\ 0 & 0 & G_{xy} \end{bmatrix} \begin{bmatrix} \epsilon_x + s'_{13} \cdot p \\ \epsilon_y + s'_{23} \cdot p \\ \gamma_{xy} \end{bmatrix}$$

So σl and σt are dependent values of pressure (P), therefore a sweep from 1-1000 (P) in Pascals is done.

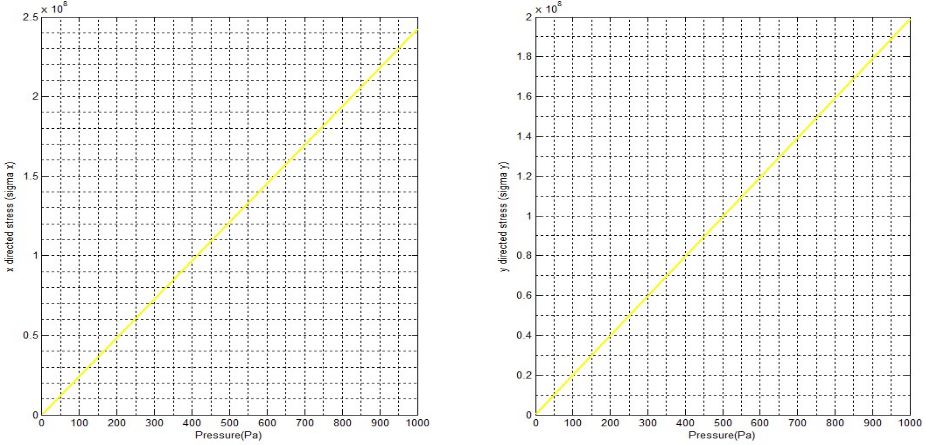


Figure 6. Strain gauge stress sigma x and y parameters calculation.

By selecting a value of 120 Ω @ 25°C for the strain gauge, and using previous constants/coefficients in the equation Rx=Ro(1+αT+ πl*σl+ πt*σt), we can get for every change on pressure applied on the membrane, the resistance variation as shown below:

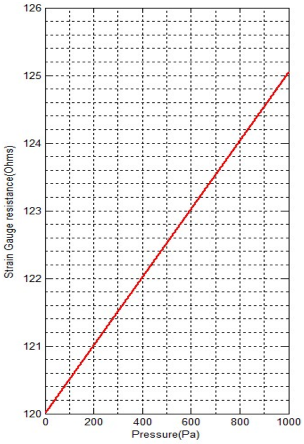
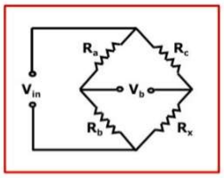


Figure 7. Strain gauge resistance change calculation based on pressure variation.

Wheatstone bridge design.

Secondly due to the small resistance variation in the strain gauge a Wheatstone bridge is chosen for good sensing. The values selected are: R1, R2, R3=120Ω to balance the whole circuit and Vf =5V as common application voltage. The equation that describes the voltage variation is:



$$R_x = \frac{R_b \times R_c}{R_a}$$

$$V_b = V_{in} \times \left(\frac{R_x}{R_x + R_c} - \frac{R_b}{R_b + R_a} \right)$$

Figure 8. Wheatstone bridge diagram and equations.

Where R1=Ra, R2=Rb, R3=Rc, Rx=strain gauge resistance, Vf = Vin, Vb=Vout. After calculation in Matlab the output voltage vs pressure results are shown in figure 9:

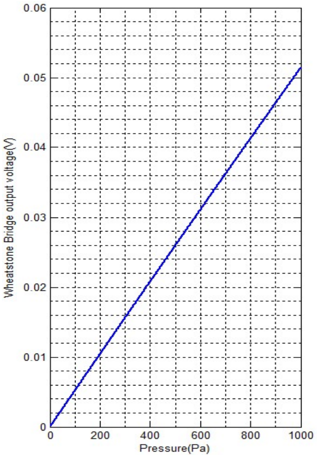


Figure 9. Wheatstone bridge output voltage vs. pressure.

4. Circuit conditioning design.

To do the handling of the Wheatstone bridge voltage variation, a conditioning circuit is design with the used of 3 topologies, instrumentation amplifier, comparator with operation amplifiers and an active BJT-resistor switch with NPN transistor as dynamic switch.

Instrumentation amplifier.

Its basic functionality response (Vout) is equal to amplify the difference input voltage (V1-V2) times a gain (1+2R/Rp):

$$\mathbf{V_o} = \left(1+\frac{2R}{R_P}\right)(V_1 - V_2) = k(V_1 - V_2)$$

So the values chosen for the circuit are: R=R2A, R2B, R3A, R3B, R4A, R4B= 5KΩ and Rp=Rg=100Ω. V1-V2 will be the Wheatstone bridge output (V1 as Voutp and V2 as Voutn), and the response is in figure 10 a.

Comparator.

This circuit responds according to a comparison between inputs (+ vs -) and outputs a digital signal indicating which is larger, as:

$$V_o = \begin{cases} 1, & \text{if } V_+ > V_- \\ 0, & \text{if } V_+ < V_- \end{cases}$$

Where 0 depends on VSS voltage level = 0V and 1 depends on VDD voltage level = 5V. Once the response is calculated, figure 10b shows results:

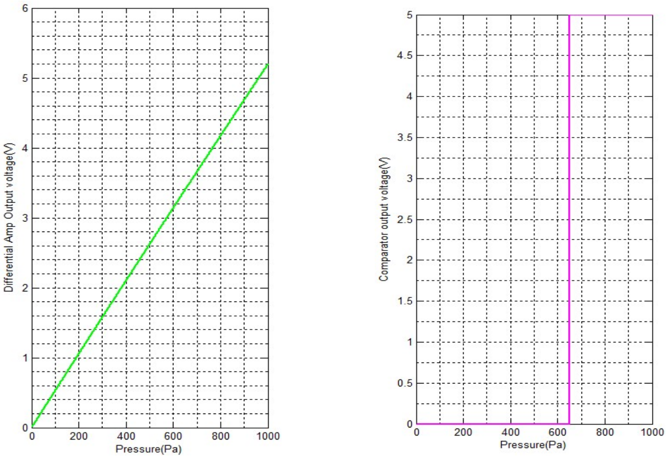


Figure 10a and 10b. Instrumentation amplifier and comparator output voltage vs. pressure.

Active BJT-resistor switch.

The current switch is a mechanical device with a 100Ω resistor which when it is closed a connection to ground is done and when it is opened an impedance>500kΩ is present.

Based on automotive requirements a 10uA fixed current through 51ohms resistor comes from the Power-train Control Module (PCM) at electrical connector pin, while switch is open (high pressure, vacuum>2.2”H2O=548Pa) and 0volts while switch is close (low pressure, vacuum< 2.2”H2O=548Pa).

The option to substitute the mechanical switch and 100Ω resistor is with a BJT transistor (2N2222) working in saturation/cut off zone plus in series with the collector a 100Ω resistor to the PCM pin and in parallel connection between collector and emitter a 500kΩ resistor.

Calculating in Matlab the base voltage (with 10kΩ in series), collector impedance (collector//emitter in parallel with 500kΩ) and collector voltage with series 100Ω resistor (applying automotive requirements) vs. pressure. Values are shown below:

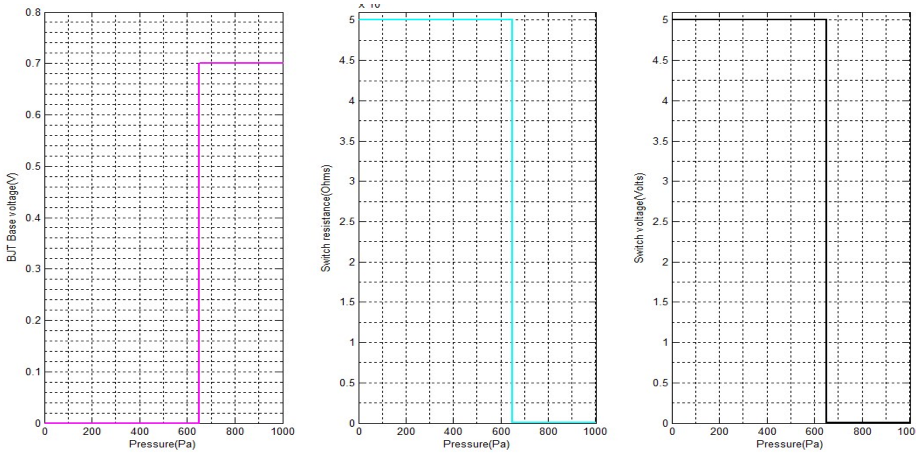


Figure 11a, 11b and 11c. Base voltage, switch resistor and switch voltage vs. pressure.

In the figure 12 the complete schematic of the NVLD system embodiment with the strain gauge can be seen for better understanding. All values are according to calculation. Once the Rx has 0Pa pressure no voltage difference will be sensed and Q1 transistor will stay open so 5V will be seen by PCM. On the contrary after pressure is applied (higher than 600Pa) voltage difference will be detected and Q1 transistor will be closed, then 1mV will be in PCM pin.

Complete circuit.

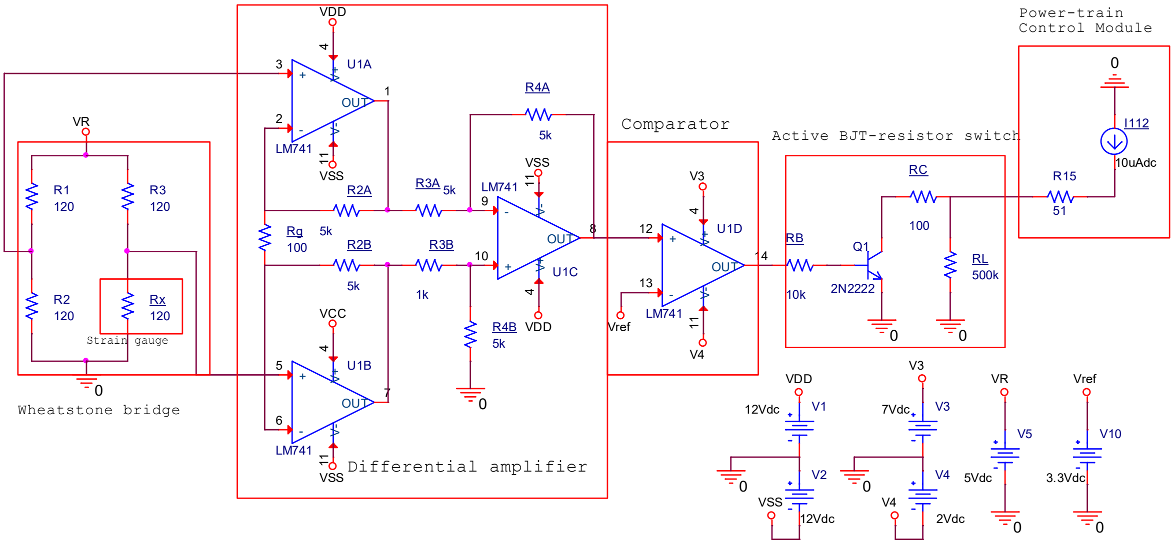


Figure 12. Strain gauge with conditioning circuit for NVLD system.

5. Complete vacuum embodiment simulation in SPICE.

To simulate the complete circuit with the calculated values, SPICE3 (from Berkeley University) is used. Here the script of the circuit:

```
*Strain Gauge
*************************************************
***Sigma X and Sigma
Y*************************************
vExx     Exx      0 DC 189e3
rExx     Exx      0 10K
vExy     Exy      0 DC 53e3
rExy     Exy      0 10K
vEyy     Eyy      0 DC 145.7e3
rEyy     Eyy      0 10K
vzero    zero     0 DC 0
rzero    zero     0 10K
vP       P        0 DC 0
rP       P        0 10K
vYxy     Yxy      0 DC 320
rYxy     Yxy      0 10K
bdx      0        dx
i=(v(Exx)*v(P)+v(Exy)*v(P)+v(zero)*v(Yxy))
rdx      dx       0 1
bdy      0        dy
i=(v(Exy)*v(P)+v(Eyy)*v(P)+v(zero)*v(Yxy))
rdy      dy       0 1
*************************************************
***Wheatstone bridge******************************
VR       vcc      0 5V
R1       vcc      outn 120
R3       vcc      outp 120
R2       outn     0 120
*************************************************
***Piezo_resistor model****************************
vPiL1    PiL1     0 DC 71.8e-11
rPiL1    PiL1     0 10K
vPiT1    PiT1     0 DC -66.3e-11
rPiT1    PiT1     0 10K
vT       T        0 DC 0
rT       T        0 10K
Valfa    alfa     0 DC 315e-5
ralfa    alfa     0 10K
vr0      r0       0 DC 120
rr0      r0       0 10K
bRx      outp1    0
i=v(outp)/(v(r0)*(1+(v(alfa)*v(T))+(v(PiL1)*v(dx))+(v(PiT1)
*v(dy))))
Vrx      outp     outp1    DC 0V
*************************************************
*Managment signal circuit
*************************************************
V1       VDD      0        DC 12V
V2       0        VSS      DC 12V
I112     0        Ix       DC 10uA
*to measure I of bRx and measure indirectly RX value in ohms
Vx       Ix       VCx      DC 0V
****Instrumentation amp****
Rg       VnA      VnB      100ohms
R1A      outn     VpA      0.001ohms
R1B      outp     VpB      0.001ohms
R2A      VnA      VoA      5kohms
R2B      VnB      VoB      5kohms
R3A      VoA      VnC      5kohms
R3B      VoB      VpC      5kohms
R4A      VnC      VoC      5kohms
R4B      VpC      0        5kohms
XUA741 VpA VnA VDD VSS VoA UA741
XUB741 VpB VnB VDD VSS VoB UA741
XUC741 VpC VnC VDD VSS VoC UA741
*****Comparator*********************************
V3       VDD2     0        DC 7V
V4       0        VSS2     DC 2V
Vref     ref      0        DC 3.3V
R1D      ref      VnD      0.001ohms
R2D      VoC      VpD      0.001ohms
XUD741 VpD VnD VDD2 VSS2 VoD UA741
****BJT 2N2222****
RB       VoD      B        10kohms
Q1       C        B        E  Q2N2222
RS       VCx      VCx1     51ohms
RC       VCx1     C        100ohms
RE       E        0        0.001ohms
RL       VCx1     0        500kohms
***********************************************
* UA741 OPERATIONAL AMPLIFIER "MACROMODEL"
SUBCIRCUIT
See file Spice_Models_for_Strain_Gauge.txt in Glosary
***********************************************
* 2N2222
.MODEL Q2N2222 NPN
See file Spice_Models_for_Strain_Gauge.txt in Glosary
***********************************************
.control
Destroy all
DC vP 0 1000 1
*x directed stress (sigma x)
plot v(dx) xlabel Pressure Ylabel 1/Pa xunits Pascal yunits Units
title x_directed_stress_(sigma_x)
*Y directed stress (sigma y)
plot v(dy) xlabel Pressure Ylabel 1/Pa xunits Pascal yunits Units
title Y_directed_stress_(sigma_y)
*Rx(gauge strain) value
plot v(outp)/i(vrx) xlabel Pressure Ylabel Rx xunits Pascal
yunits Ohms title Rx_(gauge_strain)_value
*Voutp of wheatstone bridge refered to GND
plot v(outp) xlabel Pressure Ylabel Voutp xunits Pascal yunits
Volts title Voutp_of_wheatstone_bridge_refered_to_GND
*Voutn of wheatstone bridge refered to GND
plot v(outn) xlabel Pressure Ylabel Voutn xunits Pascal yunits
Volts title Voutn_of_wheatstone_bridge_refered_to_GND
*Vout of wheatstone bridge refered to Voutp-voutn
plot v(outp,outn)  xlabel Pressure Ylabel Vp-vn xunits Pascal
yunits Volts title
Voutp_of_wheatstone_bridge_refered_to_Voutp_vs_voutn
*Vout of Instrumentation amp
plot v(VoC) xlabel Pressure Ylabel Vo xunits Pascal yunits
Volts title Vout_of_Instrumentation_amp
*Vout of comparator
plot v(VoD) xlabel Pressure Ylabel Vo xunits Pascal yunits
Volts title Vout_of_Comparator_amp
*Base voltage of 2N2222
plot v(B) xlabel Pressure Ylabel VB xunits Pascal yunits Volts
title Base_voltage_of_2N2222
*RSw resistance value
plot v(VCx1)/i(Vx) xlabel Pressure Ylabel RSw xunits Pascal
yunits Ohms title RE_resistance_value
*RSw voltage
plot v(VCx1) xlabel Pressure Ylabel VC xunits Pascal yunits
Volts title Rnsw_voltage
.endc
.end
```

Once the circuit is connected, simulations are run, pressure is selected from 0Pa to 1000Pa. A plot of each parameter has been added to compare against calculation results:

Strain gauge stress sigma x and y parameters.

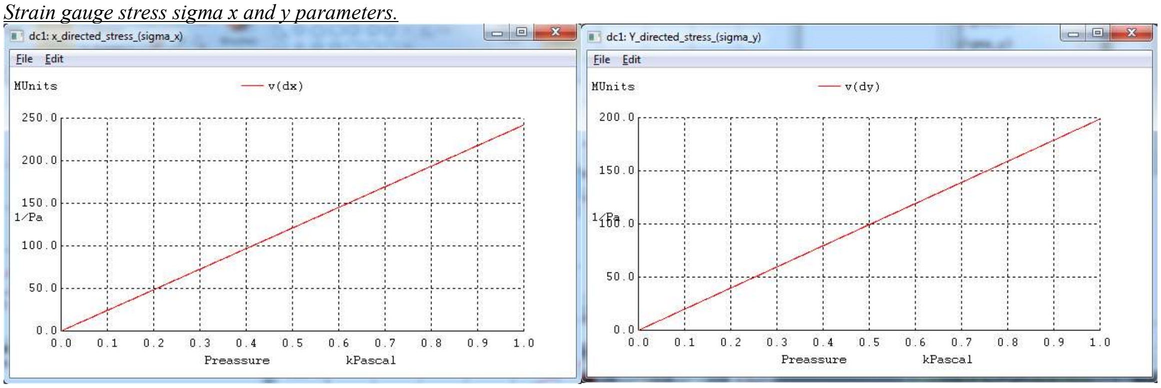


Figure 13a. Stress sigma x 13b. Stress sigma y.

Strain gauge resistance change based on pressure variation.

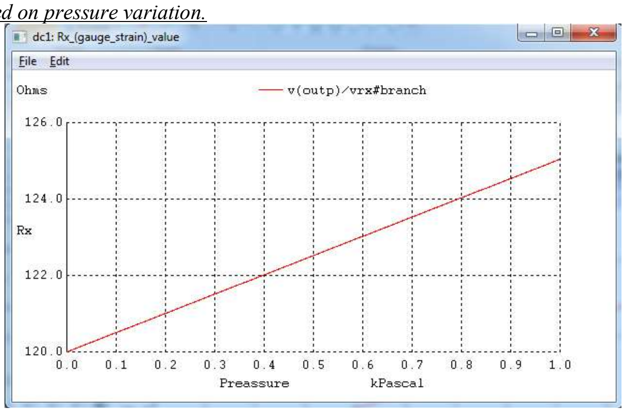


Figure 14. Strain gauge resistance change

Wheatstone bridge output voltage vs. pressure

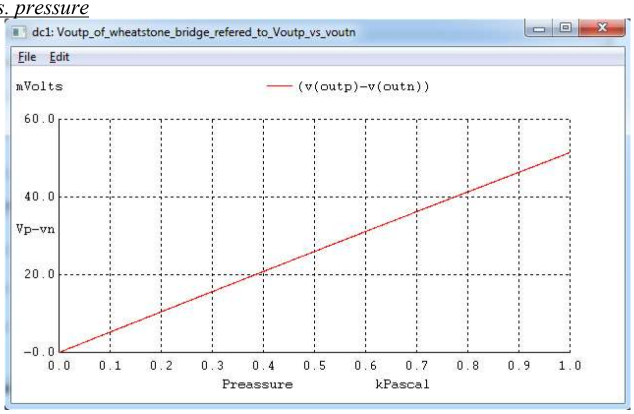


Figure 15. Wheatstone bridge output voltage

Instrumentation amplifier and comparator output voltage vs. pressure

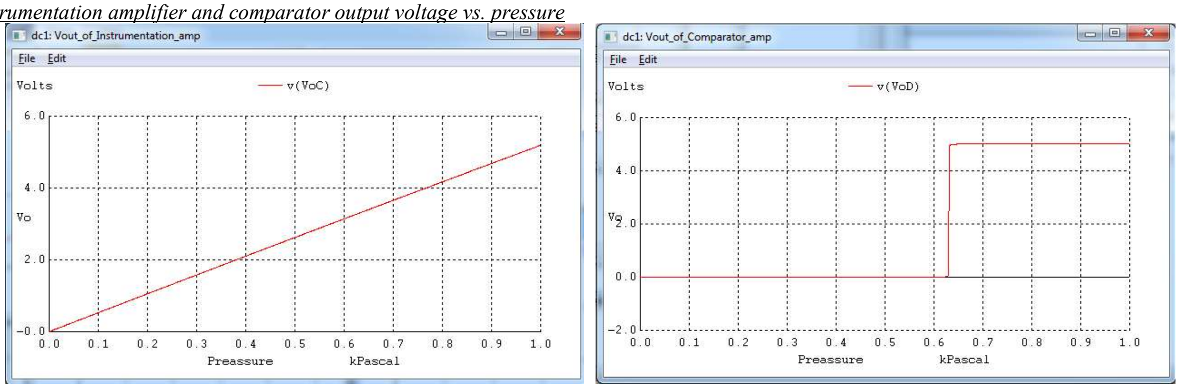


Figure 16a. Instrumentation amplifier output 16b.Comparator output voltage.

Base voltage, switch resistor and switch voltage vs. pressure.

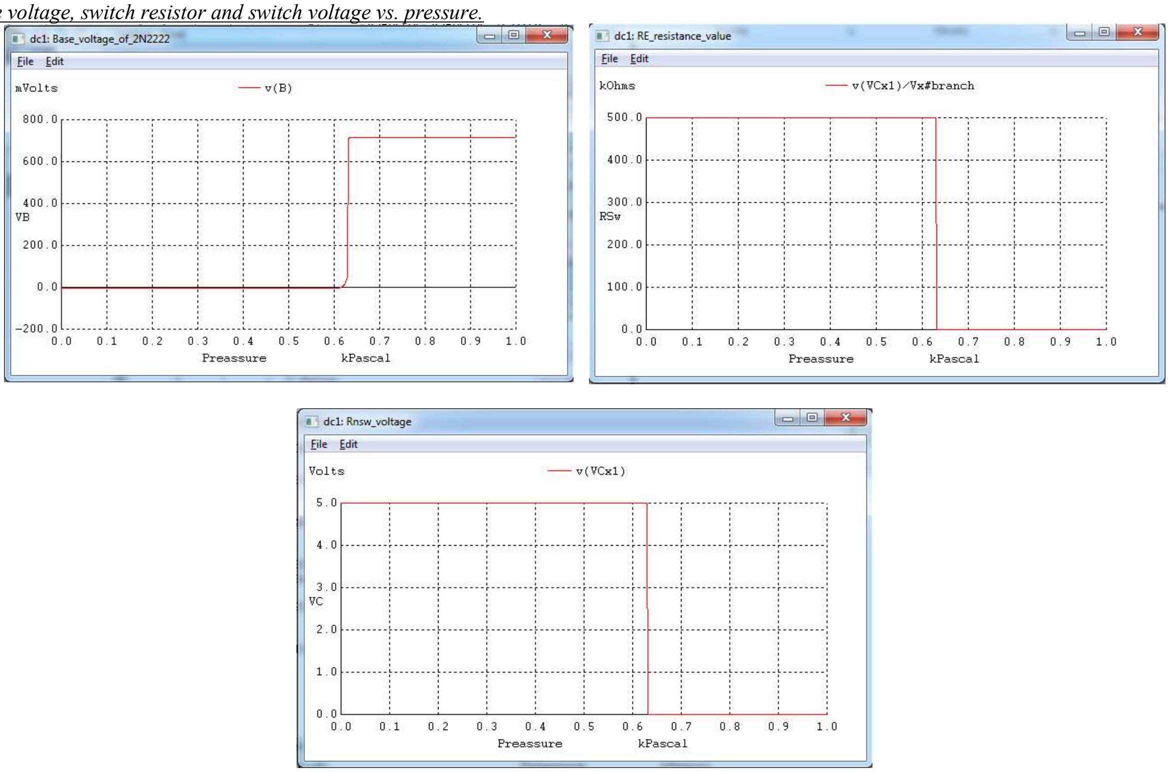


Figure 17a. Base voltage, 17b. Collector resistor and 17c. Collector voltage.

6. Conclusions.

The values investigated, equations and theory described in the scientific papers/books were enough information to calculate a fair accurate vacuum system embodiment and foreseen what would be the possible behavior/response of the circuit.

It was possible to model and simulate in SPICE the complete system (strain gauge and conditioning circuit) proposal because of the modeling sensors methodology taught in class was a reliable method.

Results comparison between calculation vs. simulation is quite similar. The only thing was the variation of the operation amplifier LM741 in the comparator, which has an "offset" that was adjusted by changing VDD to 7V and VSS to -2V, it kept the 5V output level.

The first approach of the design was done with a differential amplifier instead of instrumentation amplifier, but the low impedance input was an important factor because this affected Wheatstone bridge loading. Also, for a better and faster functionality a Mosfet transistor could be used instead of BJT transistor. This will need lower gate voltage and higher transition speed.

The strain gauge values were selected for a Silicon crystal one, if diaphragm made of metallic material is requested, only values of elastic constant should be changed for a 120Ω resistor. Based on investigation a reasonable metallic material is Constantan (45%Ni, 55%Cu), it has enough stability during temperature and pressure changes. Also, Wheatstone bridge linearity with this material is fair.

This proposal will be submitted as invention disclosure in the US office of patents in the next couple of weeks (Jun-2016).

7. Glossary.

Calculations, circuits and simulations during the Final Project process were run in either Matlab or SPICE:
-Matlab script with the complete vacuum system calculation and graphical representation per circuit.

Strain_gauge.m Strain_gauge.asv

-SPICE script with the complete vacuum system model.

Strain_Gauge.cir

-SPICE models for Operational amplifier LM741 and Transistor 2N2222.

Spice_Models_for_Strain_Gauge.txt

References.

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- http://www.ajdesigner.com/phpstress/stress_strain_equation_young_modulus.php#ajscroll
- http://www.engineeringtoolbox.com/young-modulus-d_417.html
- http://www.chemistrylearner.com/constantan.html
- https://books.google.com.mx/books?id=dQp1mtXX7_cC&pg=SA9-PA119&lpg=SA9-PA119&dq=low+pressure+semiconductor+sensor+modeling&source=bl&ots=0ZNcB5-hNX&sig=UUQ-Zi3FSpl6jajysnlkqMGhjZo&hl=en&sa=X&ved=0ahUKEwini_CL4M7MAhVq1oMKHQcDAaYQ6AEIMDAC#v=onepage&q=low%20pressure%20semiconductor%20sensor%20modeling&f=false
- https://en.wikibooks.org/wiki/Microtechnology/Semiconductors
- https://www.memsnet.org/material/silicondioxidesio2film/
- https://en.wikipedia.org/wiki/Piezoresistive_effect
- https://books.google.com.mx/books?id=8JwMjLsxZYQC&pg=PR7&lpg=PR7&dq=strain+gauge+of+polycrystalline+silicon&source=bl&ots=FHV46-SoJx&sig=UoqHANqJT_n7v66HtCrVKrcD_4c&hl=en&sa=X&ved=0ahUKEwip252e6M7MAhUD5oMKHQmUBZ04ChDoAQgjMAI#v=onepage&q=strain%20gauge%20of%20polycrystalline%20silicon&f=false
- http://www.microsystems.metu.edu.tr/piezops/piezops.html

C. OUTPUT CAPACITOR OPTIMIZATION FOR A LDO REGULATOR USING SPACE MAPPING.

Final Project.

Output capacitor optimization for a LDO regulator using Space Mapping.

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Western Institute of Technology and Higher Education
Optimization-Based Modeling and Design of Electronic Circuits
José Ernesto Rayas Sánchez PhD.
17/May/2017

Abstract: In this document, a stability analysis is modeled based on the main design parameters to show a real case circuit that could be used to represent the response of a Low drop out linear regulator (LDO). Using the optimization method called Space Mapping, an optimal output capacitor value will be selected, this in order to keep the voltage output free of any perturbation.
All the calculations and the circuit simulations are performed in Matlab this because the tool provides many functions that are used frequently for optimization purposes.
Finally the purpose of this project is to show the power of the simulation method in terms of speed and best solution for engineering applications.

8. Introduction.

Low-dropout linear regulators (LDOs) have gained popularity with the growth of battery-powered equipment. Portable electronic equipment including cellular telephones, laptop computers and a variety of handheld electronic devices has increased the need for efficient voltage regulation to prolong battery life. This can be achieved with LDOs regulators.
The increased performance of PMOS LDOs comes with stability concerns with respect to load current and external capacitance.
For this a statbility analysis is needed in order to see if the LDO is keeping the response according to the specification. In the first section **2.LDO circuit model**. It is presented the basic model of the PMOS LDO model in order to provide an image of how the linear regulator looks like internally. After that in section **3.Stability analysis.** The description of the analysis and also the input parameters are discussed this will be done based on the circuit model. After this using optimization tools, such as Space Mapping (1). The stability analysis will be transported to get an optimal solution of the output capacitor.

In section **4.Space Mapping implementation.** The description of the Space Mapping implementation is described, this includes basic block diagram, descriptions block by block, and use of the method to solve the stability analysis. Then there will be the results of the optimization in section **5.Results** and **6.Conclusions**.

9. LDO circuit Model.

To begin the stability analysis of an LDO linear regulator employing a PMOS pass transistor requires a model that contains all the necessary components to provide sufficient accuracy for the analysis. The circuit shown in Figure 1 contains these components.

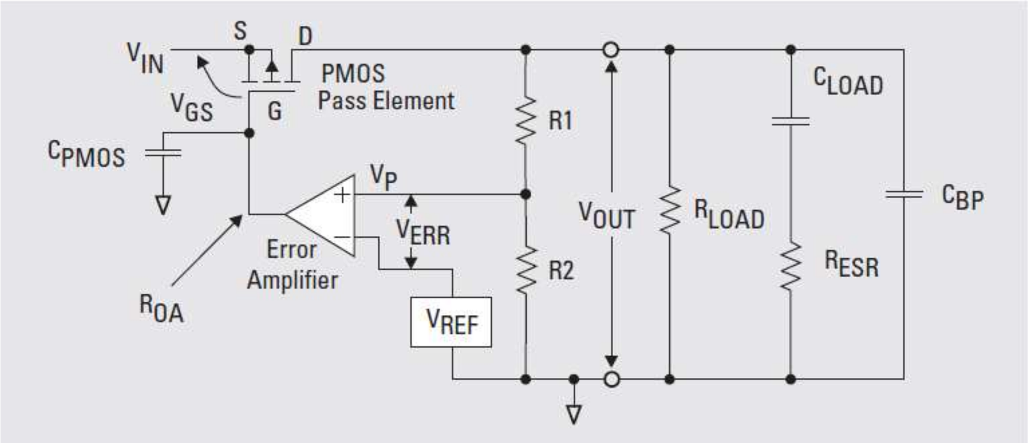


Figure 1. LDO circuit model.

In order to make a clearer idea of the stability analysis components a brief definition will be stablished by component.

Reference voltage. This voltage is the basis for the output voltage. The output voltage cannot be more accurate or stable over temperature than the reference voltage. For many of LDOs, this voltage is 1.192 V.

Error amplifier. The function of the error amplifier is to compare a scaled representation of VOUT to the reference voltage and amplify the difference. The error amplifier output then drives the PMOS pass transistor to adjust VOUT. A typical error amplifier DC gain is 25 dB to 45 dB, depending on the particular LDO.

(1) Space Mapping method was invented in 1994 by Doctor John W. Bandler at Mc Master University. This method was invented as an efficient design optimization procedure, especially suitable for optimizing computacionally expensive functions.

Feedback network. The feedback network is a resistive voltage divider. This network scales VOUT such that the scaled VOUT is equal to the reference voltage when VOUT is at its nominal value. For fixed output LDOs these resistors are internal to the LDO and have a relatively high value in order to minimize current drain.

RLOAD. Load resistance. RLOAD = VOUT /IOUT.

CLOAD. The capacitance placed on the output of the LDO for loop stability that is typically specified to be a minimum of 4.7 µF to 20 µF. Depending on the type of capacitor, it may have an internal ESR ranging from 10 W to 10 mW.

RESR. The equivalent series resistance of the output capacitor. Depending on the particular output capacitor, this resistance may include an external resistance placed in series with the output capacitor. This resistance is sometimes called the compensation series resistance.

CBP An estimate of the bypass capacitors placed across the power supply leads of the ICs powered by the LDO. These capacitors are usually 0.1-µF ceramics and have very low ESR.

CPMOS. The capacitance connected to the output of the error amplifier. This capacitance is due mainly to the capacitance of the PMOS pass element and is usually in the range of 100 pF to 300 pF.

ROA. The equivalent output resistance of the error amplifier. This parameter is one of the few parameters the LDO designer can choose to insure stability. A typical design value is approximately 300 kW.

PMOS pass. The series pass element in the LDO. This transistor operates as a variable resistance connected between the input and the output. The resistance is controlled by the gate-to-source voltage. The output resistance, RO PMOS (different from ROA), is used in the stability analysis.

10. Stability analysis

Almost all voltage regulators use a feedback loop to maintain a constant output voltage. As with any feedback loop there is phase shift around the loop and the amount of phase shift determines loop stability.
To have a stable loop the phase shift around the (open) loop must always be less than 180° (lagging) at the point where the loop has unity gain, or 0 dB. Low-dropout regulators require an output capacitor connected from *V*OUT to GND to stabilize the internal control loop.

Typically, a minimum value of output capacitance is specified. In addition, a range of ESR (equivalent series resistance) is specified.

An expression for the open-loop gain of a typical LDO linear regulator is derived that can be plotted using an analysis tool to determine the open-loop UGF (unity gain frequency) and phase margin (f*m*). In Figure 1, three poles and one zero can be identified. To simplify the expressions, it is assumed that *CBP* << *C*LOAD.

The first pole (*p1*) is due to the PMOS pass transistor output resistance plus the output capacitance ESR (*RO* PMOS + *R*ESR) and the output capacitance (*C*LOAD).

$P1= 1/2\pi *(R_{o\ PMOS} + R_{ESR}) * C_{Load}$

The second pole (*p2*) is due to the output capacitance ESR (*R*ESR) and the estimated bypass capacitance, *CBP*.

$P2= 1/2\pi * R_{ESR} * C_{BP}$

The third pole (*p3*) is due to the error amplifier output resistance (*ROA*) and the equivalent PMOS capacitance (*C*PMOS).

$P3= 1/2\pi * R_{oA} * C_{PMOS}$

The single zero (*z1*) is derived from the output capacitance ESR (*R*ESR) and the output capacitance (*C*LOAD).

$Z1= 1/2\pi * R_{ESR} * C_{Load}$

The remaining information required is the error amplifier gain, feedback network gain and PMOS pass transistor gain. Values given for the following gains are for illustrative purposes and are reasonable values for 100-mA output LDO linear regulators.

The error amplifier gain (*GEA*) is assumed to be 35 dB.

$G_{EA} = 35dB = 56.2$

The feedback network gain (*GFB*) is simply the gain of the resistive divider, R1 and R2. For an output voltage of 3.3 V (for example) and a reference voltage of 1.192 V, the feedback network gain is

GFB = VREF/VOUT = 1.192/3.3 = 0.36 = -8.8dB

The PMOS pass transistor gain (*G*PMOS) is assumed to be 8 V/V.

GPMOS = 8 = 18.1dB

The resulting expression for open-loop gain is

GOL(s) = GEA* GFB* GPMOS* (1+s/2πfz1)/ (1+s/2πfp1)* (1+s/2πfp2)* (1+s/2πfp3)

If the open loop gain is plot, the result is showed in figure 2:

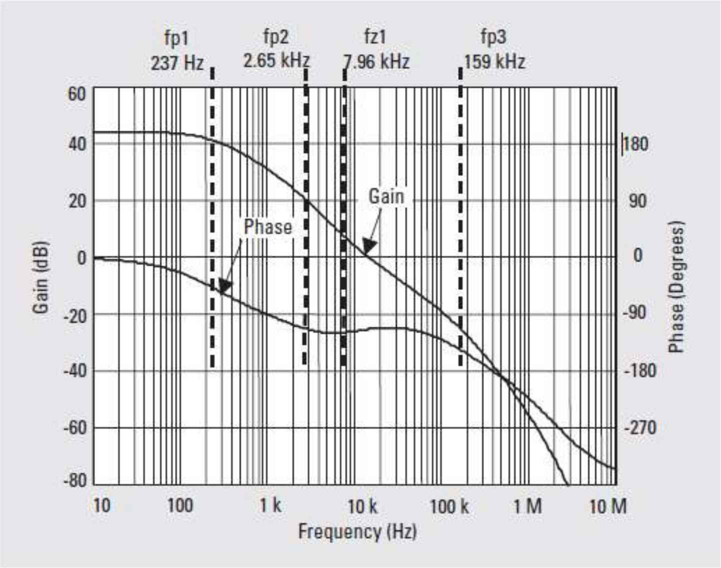


Figure2. Open Loop gain response (stable).

Figure 2 shows a gain-phase plot of the above equation using the values given. Also shown in the plot are the pole and zero frequencies. The UGF is approximately 14 kHz with a phase margin of 66°. Notice that the single zero occurs at a lower frequency than the UGF. This configuration of two poles and one zero below the UGF produces a stable system

2 Theorical cases to explain unstable response are described next:

->Reducing ESR resistance.
If the gain-phase plot is recalculated with *R*ESR set to 10 mW. The UGF is now 10 kHz with an unacceptable phase margin of 16°. With a very low ESR value such as this, pole *p2* and zero *z1* are both at frequencies much higher than the UGF. This leaves two poles below the UGF, producing an unstable system.

->CLoad reduce to 1uF.
If *C*LOAD = 1.0 µF. The UGF is now 32.4 kHz with an unacceptable phase margin of 18°. With a low *C*LOAD value such as this, pole *p2* and zero *z1* are both at frequencies higher than the UGF. This leaves two poles below the UGF, producing an unstable system.

11. Space Mapping implementation

Once stability analysis and theorical concepts are described, Optimization algorithm has to be implemented. To do this the next figure 3 describes what would be the basic idea.

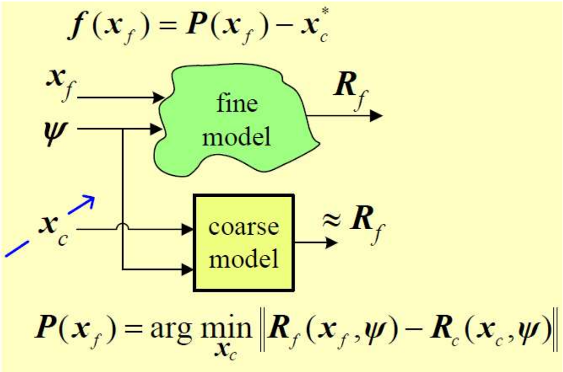


Figure3. Space Mapping approach.

Basically it is needed 2 models, one is the fine model and the other is a coarse model, both with input parameters that provide a similar response but with different characteristics:
Fine model is more accurate but more expensive in terms of resources (high computer processing).
Coarse model is less accurate but cheaper and faster.

To do the implementation, Matlab program was used because it has a nice graphic tool and also several optimized functions that could be used any time.

Figure 4 shows the algorithm of Space Mapping, which uses a few methods such: the Broyden method and parameter extraction to solve the optimal value.

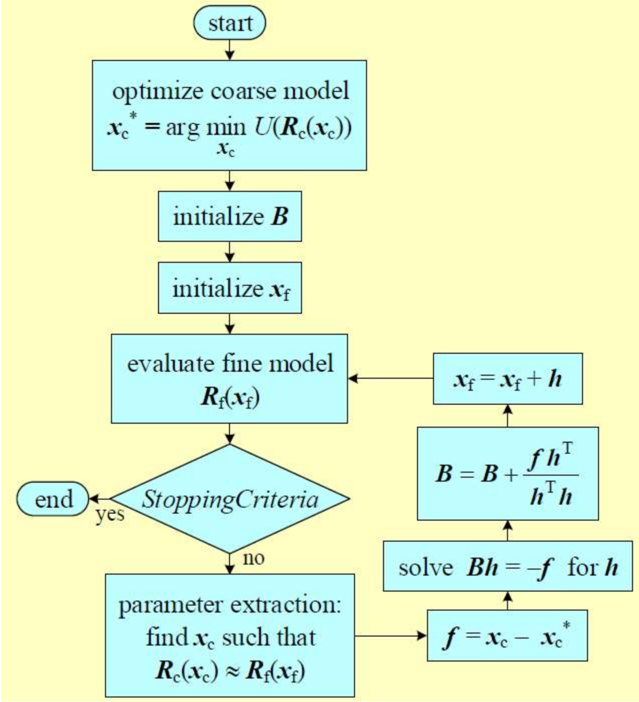


Figure4. Space Mapping approach.

In this case the variable to be found is the output capacitor of the LDO. At the very beginning the value proposal is C=10uF for the Fine model and and 20uF for the Coarse model.

The Fine model contains all the equations above described in section 3, but for Coarse model ESR parameter was removed from the equations and PMOS transistor output resistance increased in order to make the model unstable with 10uF and worked with 20uF

The next part are the scripts of the implementation in matlab of each block of Space Mapping algorithm based on the figures described above (3 and 4).

***Main Matlab script for input parameters and output responses. To see the complete script, go to Glossary section and open SM_LinearRegulator.m*

```
clc%---------------******* Plot target response with fine model*************
%Fine or Ideal value
Xf = 10e-6; % Xf Ideal value (taken from fine model)
% Plot Fine Model Response before SM
plot_LinearRegulator_f(Xf);% Plot optimized value in fine model
%**********************Plot coarse and fine models with Xc****************
XcOpt = 20e-6;%Initial value for Xc (taken from coarse coarse)
Xf = XcOpt;%Xf=Xc
plot_LinearRegulator_f(Xf);%Plot Xc with fine model (only to see effect).
plot_LinearRegulator_c(XcOpt);%Plot Xc with coarse model (only to prove it).
fun = 'PE_LinearRegulator_f';%Parameter extraction with coarse model Function
%***********************Control parameters for Broyden********************
% SM Configuration Parameters
eps_f = 1e-7;  % Maximum relative error in extracted Xc wrt XcOpt.
epsXf = 1e-7;  % Minimum relative change in Xf.
eps3 = -5e-6; % Minimum difference between fine response and optimal coarse response.
eps4 = 6e-6; % Maximum difference between fine response and optimal coarse response.
SMmax = 10;    % Maximum number of SM iterations.
%***************************Broyden Space Mapping************************
[XFSM,f,i,B,c,FunEval,EF] = BroydenSM(fun,XcOpt,SMmax,eps_f,epsXf,eps3,eps4);
disp('value of xc optimized: ');%Show the dialog marked in purple
disp(XFSM); % Show result
disp('iterations: ');%Show the dialog marked in purple
disp(i); % Show result
disp('Error flag: ');%Show the dialog marked in purple
disp(EF); % Show result
%***********************Print solution**********************************
% Plot Fine Model Response at SM Solution
plot_LinearRegulator_f(XFSM)%Plot Xf optimzed with fine model
```

***Broyden model. To see the complete script, go to Glossary section and open BroydenSM.m*

```
%*****************************************************************************************
%Find Minimum of unconstrained multivariable function by Broyden method
%*****************************************************************************************
% Usage: [x,f,i,FunEval,EF] = Broyden(fun,x0,MaxIter,epsf,epsx)
% fun: name of the multidimensional vector function (string). This
% function takes a vector argument of length n and returns a vector length n.
% x0: Starting point(row vector of length n).
% MaxIter: Maximum number of iterations to find a solution.
% epsf: Maximum aceptable error in the root of the function
% epsx: Minimum relative change in the optimization variables x.
%*******Parameters values and declaration*********
 function [xFSM,f_xi_1,i,B_i,c,FunEval,EF] = BroydenSM(fun,x0,MaxIter,epsf,epsx,eps3,eps4)
%------------------Xc optimization with Fminsearch-------------------------
options = optimset('MaxFunEvals',1000,'MaxIter',1000,'TolFun',1e-5,'TolX',1e-6);
xc=x0;
xf=xc;
%------------------- Parameter Initialization------------------------------
i=0; %iteration counter initialization
EF=-1; %Maximum number of iteractions exceeded
FunEval = 0;%Initialization of function evaluation
B_i=0.4%OK instead of eye (n)
Sigma=0.9;%intitialization 0.9->3
fi=1;
dif=1;
f_xi_1=1;
%------------------------P(xf)with Fminsearch-------------------------------
[psi,xf]=feval('LinearRegulator_f',xf);
RespAC(:,1)=psi;
RespAC(:,2)=xf;
% Read WinSpice Output Files
csvwrite('LinearRegulator_f_out.csv',RespAC,1,0); % Read AC responses.
[xi,FunVal,EF1,output]=fminsearch(fun,xc,options);
%-------------------------------------------------------------------
f_xi_1=xi-xc;
hi=1;
 while i < MaxIter %Maximum number of iteractions is reached
     c=i%To show iteration counter
         if norm(fi,inf) < epsf %Successful optimization (A root was found within epsf)
        EF=1; %Successful optimization (A root was found within epsf)
        break %Stop the iteration and show EF value
         else
            if norm(dif,2)<epsx*(norm(xi,2)+epsx)%Relative change in the optimization variables is small enough
            EF=2;%Algorith Converged (relative change in x is small enough)
             break %Stop the iteration and show EF value
            else
                  if (f_xi_1> eps3)&&(f_xi_1<eps4)%Successful optimization (Fine model response is close enough to the optimal coarse model response)
                    EF=3; %Successful optimization (Fine model response is close enough to the optimal coarse model response)
                    break %Stop the iteration and show EF value
                    else
     fi = -1*f_xi_1;%Negative Gradient only first time, B=0
     hi=B_i\fi;%To solve Bi*di=-dF
         FunEval = FunEval + 1; %Update function evaluation
        xi_i=xi; %Save xi to check on optimization variables change %82.0493
        xi= xi + hi; % Next Step %22.4642
        xi_1=xi;%Save xi+1 to check on optimization variables change %104.5135
        dif=xi_1-xi_i;
                 [psi,xf]=feval('LinearRegulator_f',xi);
                RespAC(:,1)=psi;
                RespAC(:,2)=xf;
                % Read WinSpice Output Files
                csvwrite('LinearRegulator_f_out.csv',RespAC,1,0); % Read AC responses.
                [xi,FunVale,EF1,output]=fminsearch(fun,xc,options);
                f_xi_1=xi-xc;
                 B_i=UpdateB(hi,f_xi_1,B_i);%Function to update B
               i = i + 1;% increase iteration counter
                end
            end
         end
         xFSM=xi;
 end
```

***Parameter extraction To see the complete script, go to Glossary section and open PE_LinearRegulator_f.m*

```
%*****************************************************************************************
%Plotting Norma Euclidian of the state variable filter circuit
%*************************************************************************************
%PE Parameter extraction Function
function u=PE_LinearRegulator_f(xc)
```

```
% Read WinSpice Output Files
RespAC = csvread('LinearRegulator_f_out.csv',1,0); % Read AC responses of fine model.
% type ZTranTL1sec2to1_f2_out.csv;
psi = RespAC(:,1);%fine model response
Rt = RespAC(:,2);%fine model response
%Calculate Responses coarse model with xc
[psic,Rc] = LinearRegulator_c(xc);%coarse model response
 AV = Rc;%coarse model response
 fc =psic;%coarse model response
 e=Rt-AV;%Parameter extraction
%Calculate Norm of the error vector
u=norm(e,2);%Euclidean norm
end
```

**Coarse model. To see the complete script, go to Glossary section and open LinearRegulator_c_Matlab.m

```
% LDO stability analysis simulated in Matlab (Coarse model)
%
% This function calculates the magnitude and phase of a stability analysis
%of a Linear regulator LDO
%
% Usage:[psi,R] = LinearRegulator_f_Matlab(P)
% RO_PMOS = P(1);     %(ohms)PMOS pass transistor output resistance
% R_ESR = P(2);     %(ohms)Output capacitance ESR
% C_BP = P(3);     %(uF)The estimated bypass capacitance
% R_OA = P(4);   %(Kohms)The error amplifier output resistance
% C_PMOS = P(5);     %(pF)The equivalent PMOS capacitance
% V_REF = P(6);     %(V)Reference voltage
% V_OUT = P(7);     %(V)LDO output voltage
% C_LOAD = P(8);     %(uF)Output capacitance
% IF = P(9);     % Initial frequency (GHz).
% FF = P(10);    % Final frequency (GHz).
% FP = P(11);    % Number of frequency samples.
% w2JFN = P(12); % Flag to write in journal and display simulation data.

function [psi,R] = LinearRegulator_c_Matlab(P)

RO_PMOS = P(1);     %(ohms)PMOS pass transistor output resistance
R_ESR = P(2);     %(ohms)Output capacitance ESR ###NOT USED###
C_BP = P(3);     %(uF)The estimated bypass capacitance ###NOT USED###
R_OA = P(4);   %(Kohms)The error amplifier output resistance ###NOT USED###
C_PMOS = P(5);     %(pF)The equivalent PMOS capacitance ###NOT USED###
V_REF = P(6);     %(V)Reference voltage
V_OUT = P(7);     %(V)LDO output voltage
C_LOAD = P(8);     %(uF)Output capacitance
IF = P(9);     % Initial frequency (GHz).
FF = P(10);    % Final frequency (GHz).
FP = P(11);    % Number of frequency samples.
w2JFN = P(12); % Flag to write in journal and display simulation data. ###NOT USED###

% Assumptions
GEA_dB = 35;      % (dB) The error amplifier gain.
G_PMOS = 8;    % (V/V) The PMOS pass transistor gain.

% % Preliminary Calculations
GEA = 10^((GEA_dB)/20);
G_PMOS_dB = 20*log10(G_PMOS);

% Calculating Responses
s = linspace(IF,FF,FP);
Pole1 = 1/(2*pi*(RO_PMOS)*C_LOAD);%First Pole calculation.
Pole2 = 1/(2*pi*C_BP);%Second Pole calculation.
Pole3 = 1/(2*pi*R_OA*C_PMOS);%Thid Pole calculation.
Zero1 = 1/(2*pi*C_LOAD);%First Zero calculation.
G_FB = V_REF/V_OUT ;
G_FB_dB = 20*log10(G_FB);
G_OL_Total = GEA*G_FB*G_PMOS;
G_OL_dB = 20*log10(G_OL_Total);
[~,N]=size(s);
u=zeros(1,N);%Initialize minimax objective function
             %values.
v=zeros(1,N);%Initialize minimax objective function
            %values.
w=zeros(1,N);%Initialize minimax objective function
            %values.
for j=1:N
G_OL_s = GEA*G_FB*G_PMOS*((1+(j/(2*pi*Zero1)))/((1+(j/(2*pi*Pole1)))*(+1+(j/(2*pi*Pole2)))*(1+(j/(2*pi*Pole3)))));
u(j:j) = G_OL_s;
G_OL_s_dB = 20*log10(G_OL_s);
v(j:j) = G_OL_s_dB;
Phase_G_OL_s = 180*(-atan(G_OL_s))/pi;
w(j:j) = Phase_G_OL_s;
end
psi = s';
R(:,1) = v';
R(:,2) = w';
end
```

**Fine model . To see the complete script, go to Glossary section and open LinearRegulator_f_Matlab.m

```
% LDO stability analysis simulated in Matlab (Fine model)
%
% This function calculates the magnitude and phase of a stability analysis
%of a Linear regulator LDO
%
% Usage:[psi,R] = LinearRegulator_f_Matlab(P)
% RO_PMOS = P(1);     %(ohms)PMOS pass transistor output resistance
% R_ESR = P(2);     %(ohms)Output capacitance ESR
% C_BP = P(3);     %(uF)The estimated bypass capacitance
% R_OA = P(4);   %(Kohms)The error amplifier output resistance
% C_PMOS = P(5);     %(pF)The equivalent PMOS capacitance
% V_REF = P(6);     %(V)Reference voltage
% V_OUT = P(7);     %(V)LDO output voltage
% C_LOAD = P(8);     %(uF)Output capacitance
% IF = P(9);     % Initial frequency (GHz).
% FF = P(10);    % Final frequency (GHz).
% FP = P(11);    % Number of frequency samples.
% w2JFN = P(12); % Flag to write in journal and display simulation data.

function [psi,R] = LinearRegulator_f_Matlab(P)
% Reading Parameters
RO_PMOS = P(1);     %(ohms)PMOS pass transistor output resistance
R_ESR = P(2);     %(ohms)Output capacitance ESR
C_BP = P(3);     %(uF)The estimated bypass capacitance
R_OA = P(4);   %(Kohms)The error amplifier output resistance
C_PMOS = P(5);     %(pF)The equivalent PMOS capacitance
V_REF = P(6);     %(V)Reference voltage
V_OUT = P(7);     %(V)LDO output voltage
C_LOAD = P(8);     %(uF)Output capacitance
IF = P(9);     % Initial frequency (GHz).
FF = P(10);    % Final frequency (GHz).
FP = P(11);    % Number of frequency samples.
w2JFN = P(12); % Flag to write in journal and display simulation data. ###NOT USED###
% Assumptions
GEA_dB = 35;      % (dB) The error amplifier gain.
G_PMOS = 8;    % (V/V) The PMOS pass transistor gain.
% % Preliminary Calculations
GEA = 10^((GEA_dB)/20);
G_PMOS_dB = 20*log10(G_PMOS);
% Calculating Responses
s = linspace(IF,FF,FP);
% s=1200
Pole1 = 1/(2*pi*(RO_PMOS+R_ESR)*C_LOAD);%First Pole calculation.
```

```
Pole2 = 1/(2*pi*R_ESR*C_BP);%Second Pole calculation.
Pole3 = 1/(2*pi*R_OA*C_PMOS);%Thid Pole calculation.
Zero1 = 1/(2*pi*R_ESR*C_LOAD);%First Zero calculation.
G_FB = V_REF/V_OUT ;
G_FB_dB = 20*log10(G_FB);
G_OL_Total = GEA*G_FB*G_PMOS;
G_OL_dB = 20*log10(G_OL_Total);
[~,N]=size(s);
u=zeros(1,N);%Initialize minimax objective function
             %values.
v=zeros(1,N);%Initialize minimax objective function
            %values.
w=zeros(1,N);%Initialize minimax objective function
            %values.
for j=1:N
G_OL_s = GEA*G_FB*G_PMOS*((1+(j/(2*pi*Zero1)))/((1+(j/(2*pi*Pole1)))*(+1+(j/(2*pi*Pole2)))*(1+(j/(2*pi*Pole3)))));
u(j:j) = G_OL_s;
G_OL_s_dB = 20*log10(G_OL_s);
v(j:j) = G_OL_s_dB;
Phase_G_OL_s = 180*(-atan(G_OL_s))/pi;
w(j:j) = Phase_G_OL_s;
end
psi = s';
R(:,1) = v';
R(:,2) = w';
end
```

12. Results

After running the scripts, here the results.

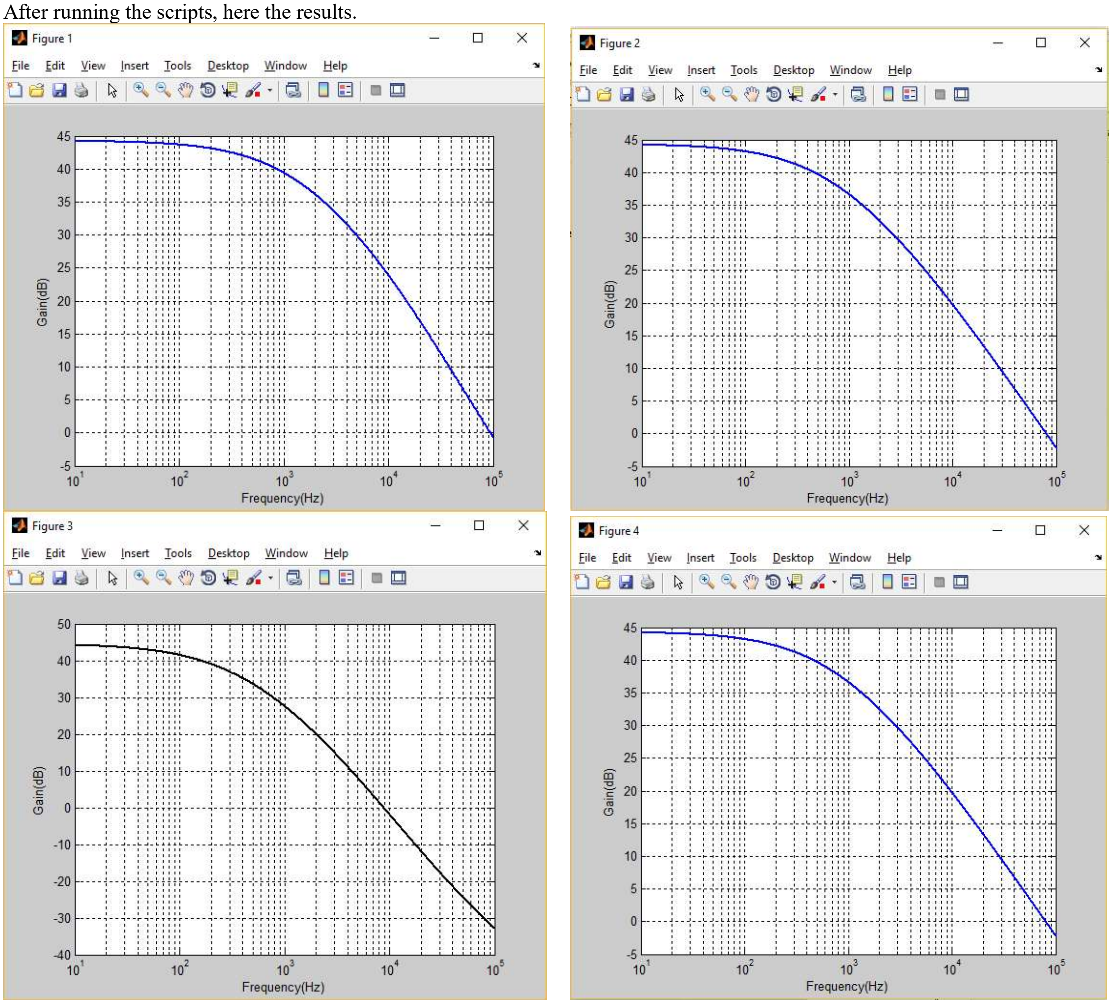


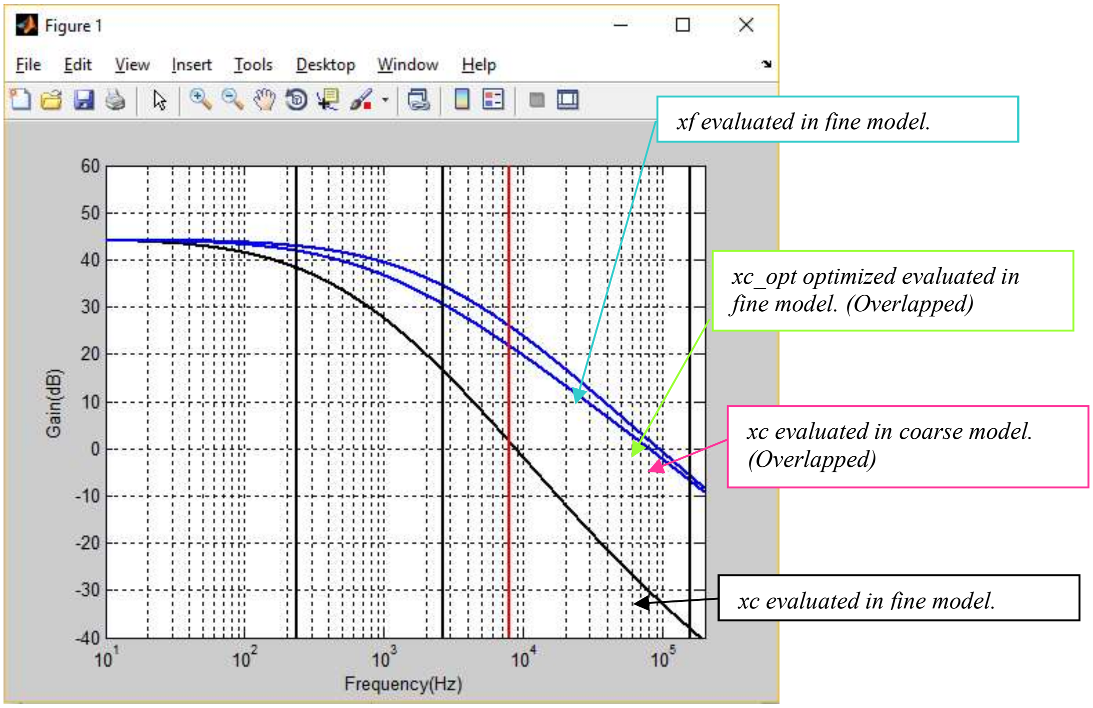
Figure5. Optimization results (top-left->xf evaluated in fine model, top-right->xc evaluated in coarse model, bottom-left->xc evaluated in fine model, right->xc optimized evaluated in fine model).

Figure 1(top-left) shows the result of fine parameter xf in fine model. This becomes the expected response from the circuit, more accurate but from computational point of view more expensive.

Figure 2(top-right) shows the result of coarse parameter xc in coarse model. This becomes a “functional” response of the circuit, less accurate but from computational point of view cheaper.

Figure 3(bottom-left) shows the result of fine parameter xf in coarse model. This becomes the “optimizing” response which means this is the result will be optimized until a proper value gives a close response as figure1.

Figure 4(bottom-right) shows the result of optimized parameter xc_opt in coarse model. This becomes the “optimized” response of the circuit, more accurate (almost as figure1) but from computational point of view cheaper.



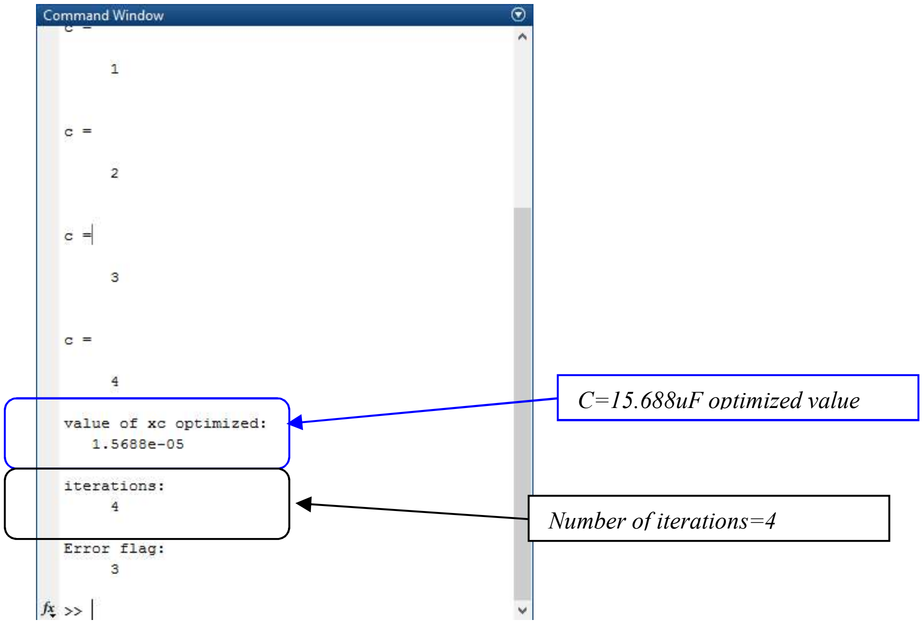
xf evaluated in fine model.

xc_opt optimized evaluated in fine model. (Overlapped)

xc evaluated in coarse model. (Overlapped)

xc evaluated in fine model.

Figure6. Optimization results (All together).



```
     1


c =

     2


c =

     3


c =

     4

value of xc optimized:
   1.5688e-05

iterations:
     4

Error flag:
     3

fx >>
```

C=15.688uF optimized value

Number of iterations=4

Figure7. Optimization iterations and result optimized.

13. Conclusions.

-The values investigated, equations and theory described in the application notes / books / and school presentations were enough information to calculate a fair accurate stability analysis and foreseen what would be the possible behavior/response of the circuit.

-One of the problems seen during the optimization was the quantity of points used to solve the calculation because all the plots shows higher frequency than the real calculated.

-Another conclusion is that the circuit chosen was not the best for this project because to show the complete plot from 10Hz to 10 GHz made the simulator spent a lot of time to get the solution, even sometimes the program did not response any longer. This was because 10 thousand millions of points during parameter extraction process made the program too slow. Therefore another electrical circuit with a less point to be used for calculation would be better.

Space Mapping is a lot faster than other methods for optimization but because it contains most of the other methods inside, even though the accuracy of the optimized value is quite good.

Another conclusion is in order to make the method worked it was necessary to do 2 things: either change the initialization value of Beta from 1 to 0.847 or to activate the while conditioning in the Broyden algorithm other wise Matlab run forever or did not get the right solution.

Also it is concluded that depending on the proper selection of the output capacitor at the LDO linear regulator output will produce the best stability response of the circuit which will give the right approach that is desired in the engineering world.

14. Glossary.

Calculations, circuits and simulations during the Final Project process were run in Matlab:

-Matlab script with the complete vacuum system calculation and graphical representation per circuit.

SM_LinearRegulator.m
BroydenSM.m
PE_LinearRegulator_f.m
UpdateB.m
LinearRegulator_c.m
LinearRegulator_c_Matlab.m
LinearRegulator_f_Matlab.m
LinearRegulator_f.m
plot_LinearRegulator_f.m
plot_LinearRegulator_c.m

References.

- An introduction to Space Mapping presentation. By Jose Ernesto Rayas Sanchez Ph.d.
- Space Mapping optimization for engineering design: A tutorial presentation By Jose Ernesto Rayas Sanchez Ph.d.
- Space Mapping : The State of the Art. By John W. Bandler and Quingsha S. Cheng.
- Space Mapping examples seen in class By Jose Ernesto Rayas Sanchez Ph.d.
- Stability analysis of low-dropout linear regulators with a PMOS pass element. By Everett Regers. Application note 76433 Texas Instruments.
- LDO Regulator stability using ceramic output capacitors. By Chester Simpson application note 1482 National Instruments