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Bachelor in Micro and Nanotechnology Engineering

Photopatternable gate insulator for oxide TFTs

MASTER OF SCIENCE IN MICRO AND NANOTECHNOLOGY ENGINEERING

NOVA University of Lisbon

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Pour ma gran-mére.

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As I was trying to write this, I realized that I had never really stopped to think about everything and everyone that has brought me to this day. I guess it all started when I decided that I wanted to be an engineer, without any real notion of what that meant. Then my brother suggested to me this degree, and as the younger sister that I am, always looking up to my older siblings, I followed his advice, mainly because I had no other direction. This was one of the luckiest events of my life, leading me to a degree that I loved and introducing me to amazing friends and professors. This section is dedicated to them.

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"Religion is a culture of faith. Science is a culture of doubt."
- Richard Feynman

ABSTRACT

A photopatternable and solution-processable dielectric polymer, as the one provided by Solvay for this work, has physical properties that make it a unique candidate for gate dielectric in thin-film transistors (TFT), allowing to save time and reduce the complexity of the processes involved. To demonstrate that this material can be patterned using Ultra-Violet (UV) light and the exposed pattern can be developed in acetone, an optimization of the processing conditions was made in terms of the deposition conditions, curing and development steps. The polymer films were deposited by spin coating, followed by a baking at 90°C for 10 minutes and cured using a lightbulb with 365nm wavelength. The films were then characterized by profilometry, transmittance, atomic force microscopy (AFM), and scanning electron microscopy/energy dispersive spectroscopy (SEM/EDS).

The polymer films were used in metal-insulator-metal (MIM) capacitors as well as gate dielectric in In-Ga-Zn-O (IGZO) TFTs. The MIM capacitors showed a dielectric constant of 8.35 at 1kHz, a leakage current density below 1.07×10^{-7} $A.cm^{-2}$ at $1MV.cm^{-1}$, and a breakdown field higher than $1.5MV.cm^{-1}$. The TFT had turn-on voltage (V_{on}) of -1V, saturation mobility of (μ_{Sat}) of 7.07 $cm_2 \cdot V^{-1} \cdot s^{-1}$ and on/off current ratio of 10^5, positioning them close to the IGZO TFTs using traditional dielectrics that require complex etching processes.

Palavas chave: Photopatternable, Dielectric, IGZO TFT

RESUMO

Um polímero foto padronizável, como o fornecido pela *Solvay*, é um polímero dielétrico com propriedades físicas que fazem dele um excelente candidato para ser utilizado no fabrico de um transístor de filme fino (TFT), permitindo poupar tempo e reduzir a complexidade dos processos. Com o objetivo de demonstrar que este material consegue ser padronizado utilizando luz UV e revelando o padrão em acetona, foi feita uma otimização das condições não só da deposição deste filme, bem como do processo de cura e revelação do mesmo, de forma a tentar manter as suas propriedades dielétricas. Os filmes foram depositados por *spincoating*, seguido de um *baking* a 90° C por 10 minutos e curados utilizando uma lâmpada com comprimento de onda de 365nm. Os filmes foram caracterizados através de medidas de perfilometria, transmitância, microscopia de força atómica e microscópio de varrimento eletrónico e espetroscopia de energia dispersiva de raio-x (SEM/EDS).

Os filmes foram também depositados em estruturas metal isolante metal (MIM) e como dielétrico de porta em transístores de filme fino de In-Ga-Zn-O (IGZO) produzidos em duas arquiteturas diferentes. Os condensadores MIM exibiram uma constante dielétrica de 8.35 a 1kHz, uma densidade de corrente de fuga de cerca de $2.21x10^{-12}$ $A.cm^{-2}$ a $1MV.cm^{-1}$ e um campo elétrico de rutura superior a 3 $MV.cm^{-1}$. Os TFTs produzidos, exibiram uma tensão on (V_{on}) de -1V, uma mobilidade de efeito de campo (μ_{FE}) de 7.07 $cm_2 \cdot V^{-1} \cdot s^{-1}$ e uma razão de corrente on/off de 10^5, colocando estes dispositivos perto de valores apresentados em TFTs de IGZO que usam dielétricos tradicionais e são produzidos por técnicas complexas de *etching*.

Palavras-chave: foto padronizável, Dieletrico, TFT de IGZO.

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LIST OF SYMBOLS

A	Area
Al_2O_3	Aluminium Oxide
d	Thickness
ε_0	Permittivity of the Free Space
HfO_2	Hafnium Dioxide
H_3PO_4	Phosphoric Acid
H_2O	Water
I_{DS}	Drain-Source Current
κ	Dielectric Constant
L	Transistor's Length
μ_{FE}	Field-Effect Mobility
μ_{SAT}	Saturation Mobility
SS	Subthreshold Swing
SF_6	Sulfur Hexafluoride
SiO_2	Silicon Dioxide
Si_3N_4	Silicon Nitride
V_D	Drain Voltage
V_{GS}	Gate-Source Voltage
VDF-TrFE-CTFE	Vinylidene fluoride-co-trifluoroethylene
Ta_2O_5	Tantalum oxide
W	Transistor's Width
W/L	With-to-length Ratio
ZrO_2	Zirconium oxide

LIST OF ABBREVIATIONS

AFM Atomic Force Microscopy
CENIMAT Centro de Investigação de Materiais
CF Capacitance-Frequency
CV Capacitance-Voltage
DUV Deep Ultra Violet
EDS Energy Dispersive Spectroscopy
i3N Institute for Nanostructures, Nanomodelling and Nanofabrication
IGZO Indium Gallium Zinc Oxide
IPA Isopropyl Alcohol
IV Current-Voltage
MIM Metal-Insulator-Metal
PES Polyethersulfone
PVP Polyvinylpyrrolidone
RIE Reactive Ion Etching
RMS root-mean-square
SCS Solution Combustion Synthesis
SEM Scanning Electron Microscope
TFT Thin-Film Transistor
UV Ultraviolet

Motivation and objectives

In the past decade there have been numerous efforts to find devices that are compatible with the Internet-of-Things, a concept that demands low voltage and low-cost devices that should be transparent and compatible with flexible substrates.[1] The oxide thin-film transistor (TFT) is considered to be a great prospective unit device, for this kind of electronics[2], however, regardless of the techniques used to fabricate these materials in the TFT stack (physical or chemical vapor deposition routes), several photolithographic steps are required to define the patterns of all layers. The combination of vacuum-based deposition routes and photolithography is time consuming and involves significant material waste, particularly photoresist, which translates into high processing costs.[3] Hence, industry always seeks to reduce the mask count of the TFT stack and to search for more cost-effective processes for each layer.[4] Solution processing offers the possibility of discarding vacuum-based tools, bringing low-cost and simple deposition techniques such as spin-coating, spray-coating or inkjet printing. The later brings another advantage: being an additive process, it does not require any photolithograhic steps for layer definition[5], [6]. Research shows that within the overall oxide TFT published papers in the last decade, a continuously growing percentage corresponds to solution-processed oxide TFT publications, reaching almost 30% in 2018,[2] showing that these above listed alternatives are being pursued. While significant advances have been made over the last years on ink-jet printed semiconductor and dielectric layer, printing resolution is still not compatible with the requirements of TFTs, which nowadays demand for sub-10 μm resolution patterning. New materials and processing technologies for this purpose need to be cost effective and offer excellent mechanical and electrical properties and meeting these requirements can be a challenge.

The dielectric in a TFT is rather important for the device's performance[7], so keeping in mind what was previously mentioned, there have been attempts to find materials that meet all the physical requirements and at the same time do not add on to the complexity or cost of the manufacturing. A photopatternable material appears to be a good compromise between complexity/cost reduction (as it does not require photoresist for pattern definition) and high-resolution patterning (as it still relies on a mask aligner/stepper for pattern definition). This work intends precisely to implement a photopatternable dielectric polymer provided by Solvay in the fabrication process of oxide TFTs at CENIMAT|I3N. Specific objectives are:

- Establish processes to fabricate thin films of this dielectric by spin-coating, assuring adequate curing;
- Study the electrical properties of the spin-coated films;
- Investigate pattern feasibility within the spin-coated films by UV patterning;
- Integrate the photopatternable gate dielectric into oxide TFTs.

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1. INTRODUCTION

1.1. Thin-Film Transistors

Thin film transistors (TFTs) are a type of field-effect transistor mainly used in display technology.[8] They are built by layering thin films of an active semiconductor, a dielectric layer, and metallic contacts (source, drain and gate) on a substrate. The working principle is based on modulating a current that flows between the source and the drain (I_D), which is achieved by applying a voltage to the gate (V_G).[9]]. In displays, a TFT is used to regulate the RGB color intensity on each individual subpixel, acting as individual switches that allow the pixels to change state rapidly between dark and bright states.[10] The different configurations used for TFTs can be seen on figure 1.1.

The materials that can be used to fabricate TFTs vary a great deal: for the active layer, hydrogenated amorphous silicon (a-Si:H), poly-silicon, organic semiconductors, amorphous-InGaZnO (a-IGZO), among others, are the main choices. The latter is the most used semiconductor for the active layer, due to its transparency and excellent electrical properties and is becoming widely adopted by display industry owing to its superior electrical performance (mostly higher mobility and lower off-curent) compared to a-Si:H, while still assuring excellent uniformity in large areas and low-temperature (sub-350 °C) fabrication.[10], [11]. For the gate dielectric material, silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) have been primary choices transversal to all TFT semiconductor technologies. During the last decade, high-κ dielectrics such as Al_2O_3 and HfO_2 have been replacing Si-based dielectrics, mostly to enable lower operating voltages.[6] There are various techniques used to fabricate a TFT, ranging from complex physical or chemical vapor deposition, to solution based ones. Usually many photolitografic processes have to take place to define the patterns of each layer, which consumes a lot of time and resources, raising fabrication costs.[12]

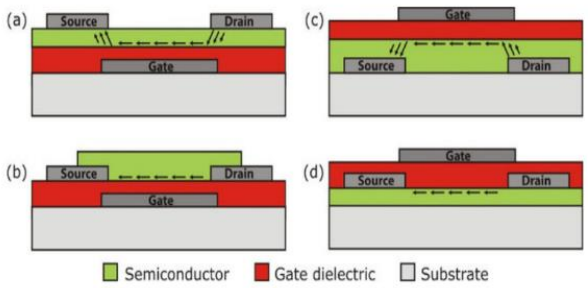

Figure 1. 1 - General thin-film transistor configurations: (a) staggered bottom-gate; (b) coplanar bottom-gate; (c) staggered top-gate and (d) coplanar top-gate.[9]

Regardless of their application, generic desired properties of a TFT are high mobility (μ_{FE} or μ_{sat}, depending if it is extracted in linear or saturation modes), high on/off ratio, a small subthreshold swing (SS) and a low operation voltage.[13], [14] These parameters can be extracted from output and transfer characteristics of the devices. The transfer curve is the plot of the drain current (I_D) over the gate voltage (V_G), for a certain drain voltage (V_D). The turn-on voltage, V_{on} can be extracted from this plot, being the V_G, at which I_D starts to increase drastically. This voltage should be close to 0, and ideally positive.[15]

μ_{FE} is calculated by equation 1.1, where W/L is the transistor's aspect ratio, C_i is the capacitance density of the dielectric and V_D is the drain voltage. V_D must be a very low voltage, to ensure the transistor stays in linear regime.[15] This parameter relates to the carrier transport efficiency, which influences the operating frequency of the device as well as the maximum drain current.

$$\mu_{FE} = \frac{\left(\frac{dI_D}{dV_G}\right)}{C_i \times \frac{W}{L} \times V_D} \tag{1.1}$$

μ_{sat} is calculated by equation 1.2 and is obtained at a high V_D.

$$\mu_{SAT} = \frac{\left(\frac{d\sqrt{I_D}}{dV_G}\right)^2}{C_i \times \frac{W}{L} \times \frac{1}{2}} \tag{1.2}$$

The subthreshold swing (SS) is calculated by equation 1.3 and pinpoints the V_G necessary to increase the drain current by one decade, which should preferably be a small value, to ensure a higher speed and lower power consumption for the devices.[15]

$$SS = \left(\frac{d(log_{10} I_D)}{V_{GS}}\right)^{-1} \tag{1.3}$$

1.2. Dielectric material

A dielectric is an electrical insulator polarized by an electric field. Positive charges are displaced in the field direction and negative charges otherwise, which generates an internal electric field on the dielectric. For a metal-insulator-metal (MIM) capacitor, in the absence of an external bias, the charge distribution in the dielectric is at equilibrium, but by applying a voltage to electrodes at both ends, a surface charge density is created at both sides of the insulator, as depicted in figure 1.2. The capacitance *per unit area* is the capacitor's ability to store charge at a certain voltage and can be described by equation 4, where k is the dielectric constant, ε_0 is the electric permittivity in vacuum ($8.854 \times 10^{-12} Fm^{-1}$) and d is the thickness of the dielectric film.[16] By observing this equation, it can be concluded that C_i is higher for high-κ dielectrics, and thinner films.

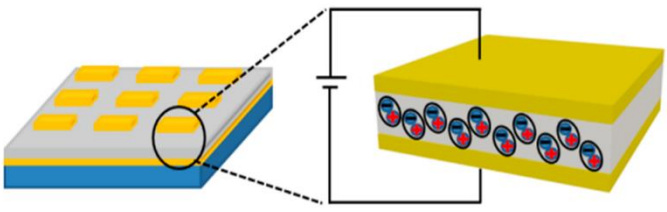

Figure 1. 2- Schematic diagram of a MIM capacitor. Adapted from[13]

$$C_i = k\frac{\varepsilon_0}{d} \quad (1.4)$$

While the semiconductor defines the range of properties achieved by a given TFT technology, the development of a suitable dielectric for transistors is of utmost relevance.[17] Indeed, the dielectric layer plays a very important role on the device's stability and overall performance. When using a high-κ dielectric, it is possible to increase the capacitance between the gate dielectric and the channel layer. Therefore, the operating voltage is reduced which leads to low power consumption on electronic devices. A poorly chosen dielectric material can lead to a narrow band offset and relevant properties variations, like the off current, pinhole density, low interface trap density and surface roughness, which leads to reliability or reproducibility issues.[18] It is known that high-κ insulators comprised by oxides show a high performance and suitability for application in TFTs.[6] The most suitable candidates for insulators are oxides like aluminium oxide (Al_2O_3), hafnium oxide (HfO_2), zirconium oxide (ZrO_2) and tantalum oxide (Ta_2O_5), which owing to its high-κ grant an easier trap filling in the semiconductor/dielectric with the increase of V_G and allow a low operation voltage. These high-κ oxide dielectrics have been obtained via solution process, yet, temperatures above 300°C are still needed, which limits applications in flexible electronics.[12], [17], [18] When pursuing the fabrication of electronics at low-temperature, the conventional dielectric materials and techniques are not the best options, so as a result, new ones have been developed, such as solution combustion synthesis (SCS) and deep ultraviolet (DUV) treatment for these oxide dielectrics. Carlos *et al*[7] have been able to boost the performance of a high-κ multilayer dielectric based on HfO_x and AlO_x by combining these two techniques. These aim to achieve excellent films at low temperatures, compatible with low-cost flexible and transparent substrates.

1.2.1. Photo-patternable dielectrics

Photo-patternable dielectric materials, i.e., materials that can be patterned without requiring a photoresist, have been suggested as an alternative more than a decade ago, as a viable solution to the reduction of manufacturing complexity and costs. Photo-patternable dielectrics have two fundamental requirements: match the performance of advanced resists that currently exist and have a good dielectric performance. Having said that, to ensure the dual functionalities of the material, it puts a lot of pressure onto the material design and development. For visualization purposes, an example on figure 1.3 shows a comparison between a conventional photolithography process and one using a photo-patternable dielectric. The difference between complexity of processes can be perceived, with the second one being much simpler.[19]

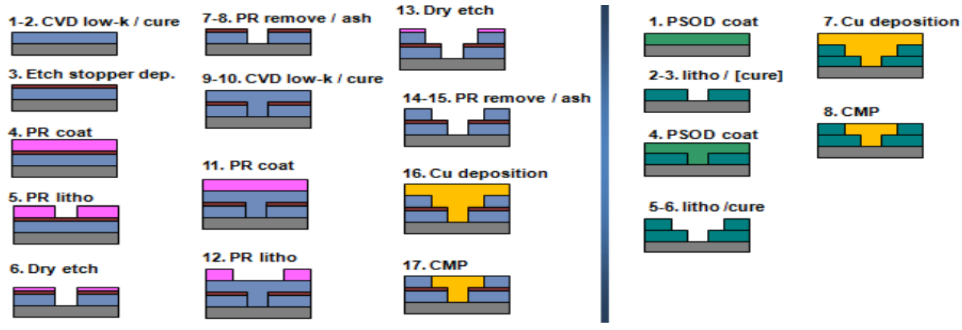

Figure 1. 3 - Comparison between a conventional process (simplified illustration with omission of some assisting layers / process steps) and process using a photopatternable dielectric (PSOD).[16]

These dielectric materials integrate photosensitive polymers in the film composition. The pattern is then created using UV light exposure through a photomask, which crosslinks the exposed areas of the film, turning them ideally insoluble when dipped in a developer, contrarily to the unexposed film. There are several

dielectric photo-patternable material systems available. An example of processing of a photo-patternable dielectric and forming vias can be seen on figure 1.4.[19]

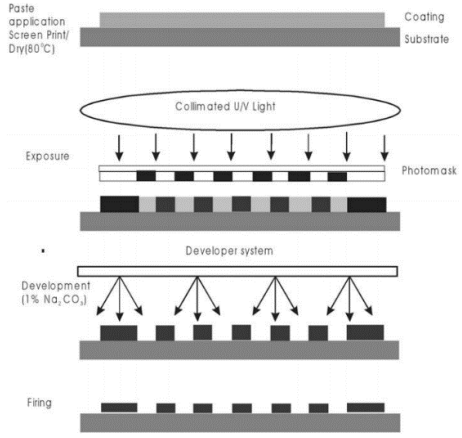

Figure 1. 4 - Process for photopatterning vias in an insulator.[17]

1.2.2. Photopatternable gate dielectrics in TFTs

As mentioned, photopatternable materials have already been proposed to be used in many electrical applications, including gate dielectric for TFTs. This application has special relevance for this work, as its objective is to test a novel photopatternable material to be used as gate dielectric. The following are some of the previous works that have tried to use a photopatternable dielectric material as a gate dielectric: Jung et al[20] reports a flexible solution-processed ZnO TFT using a direct photopatternable organosiloxane-based organic–inorganic hybrid gate dielectric, on a Polyethersulfone (PES) substrate and high-performance TFTs were obtained. Wang et al[21] explores a carbohydrate as a photopatternable gate dielectric for organic transistors. Hee Lee *et* al[22] investigate poly(4-vinylphenol) (PVP), a photopatternable polymer for the gate dielectric obtained at 180º C and Petritz et al[23] , have successfully reported in 2013 a p-type organic TFT, using a photopatternable thin polymer, and Rim *et al*[24] present a photopatterned solution-processed oxide-based gate dielectrics, such as Al_2O_3, patterned by DUV. More recently, in 2019, Lee *et* al[25] were able to achieve ultra-low driving circuits based on coplanar a-IGZO TFTs, using a photopatternable ionic polymer directly patterned by UV light, with other layers in the TFT patterned by conventional lithography. The TFTs produced had a μ_{FE} of 11.6 $cm^2.V^{-1}. s^{-1}$, on-off ratio of 10^7 and threshold voltage of 0.3V. These articles investigate photopatternable materials as great candidates for gate dielectrics, showing that is possible to simplify the fabrication process without compromising the quality of the device, taking in consideration its low power application. In section 3.3.3, table 3.11 presents a comparison of the results obtained in these papers, along with the results obtained in this work.

1.2.3. Photopatternable dielectric polymer provided by Solvay

This material, developed by *Solvay* (specific reference and some details of this development product are omitted due to confidentiality aspects), has unique characteristics. Due to its intrinsic properties, electroactive polymers (EAP) do not require specific or expensive post treatment process, being able to be used in flexible electronics, processed by techniques like screen-printing, spin-coating and on different substrates. This polymer is a terpolymer, meaning it is easily solubilized in many different solvents and shows unique properties, such as: a high dielectric constant above 10 at room temperature (making them suitable candidates to be used as gate dielectric in transistors), and good actuation power. [26]

Another very important characteristic of this polymer is that it is cross-linkable by UV and photopatternable. As a result of the selective cross-linking of its molecules, the polymer's solubility in organic

solvents changes, behaving like a negative photoresist [23]. This last characteristic means that for its integration in clean room processes does not require a resist layer for patterning, which simplifies the fabrication of the TFT. Transmittance is also a very important parameter to have in mind when one is considering a material for transparent electronics, and in these, this dielectric polymer excels.[26]

The material used to form the films is Vinylidene fluoride-co-trifluoroethylene (VDF-TrFE-CTFE) [27], with the structure seen in figure 1.5.

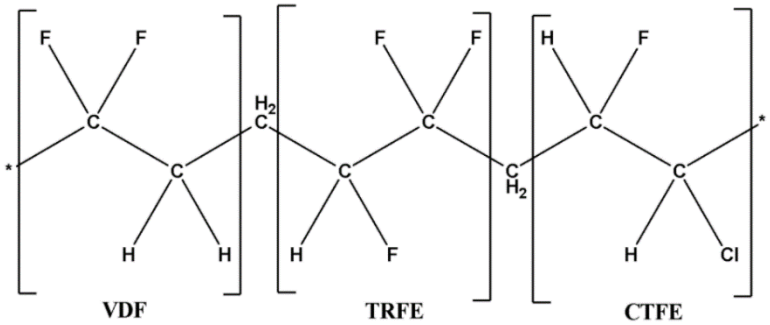

Figure 1. 5 - Molecular structure of the polymer used in this work.

2. MATERIALS AND METHODS

This chapter provides details on the fabrication and characterization processes used throughout this work. Routes to deposit the photopatternable polymeric dielectric by spin-coating were established, followed by its implementation in oxide TFTs. Characterization of dielectric films and TFTs was performed, with relevance for electrical measurements.

2.1. Photopatternable polymeric dielectric film deposition and curing

All films were deposited on Corning glass with 2.5x2.5 cm^2. The substrates were properly cleaned by submerging them in acetone followed by IPA (isopropyl alcohol) in a *Sonorex Super* ultrasound bath, for 10 minutes each. All films were deposited the same way, so for the other sections in materials and methods, when referring to the film deposition, it is referring to the deposition described in this section (2.1). Using *Suss Labpsin6 Spin Coater*, with a spinning speed of 2000 rpm for 30 seconds, the films were deposited. After this, they were placed on *Torrey Pines HS40A-2 Heating Plate*, heated at 90 °C, for 10 minutes. For the curing step, the films were placed in *Suss MA6 UV Mask Aligner* exposing it to UV light provided by an HBO-350 W/S mercury lamp (main component is 365 nm wavelength). Exposure doses were controlled by varying exposure time and light intensity through lamp power. Light intensity was measured through a *Suss Microtech UV Optometer*. For area-specific curing (e.g., in TFT fabrication), UV exposure was performed through a photomask.

2.2. MIM capacitors fabrication

On the bottom of the substrate, 100 nm thick Al films were deposited by e-beam evaporation in a home-made tool, using a shadow mask (seen in figure A.1 in Appendix A) to form the electrodes pattern. Following this, the dielectric films were deposited as described in section 2.1. To reveal the electrodes in the bottom (that had been covered by the film), dry etching with O_2 gas was performed in a small part of the substrate, using the *Trion Phantom 3 Reactive Ion Etcher (RIE-ICP) System*, for 5 minutes. Finally, 100 nm of Al were deposited for the top electrodes, using the same process as the bottom ones.

2.3. TFT fabrication

For the TFTs two different architectures were fabricated, staggered bottom and top gate as seen in figure 2.1. Table B.1 in appendix B summarizes the differences between samples, however in this section a detailed description is presented.

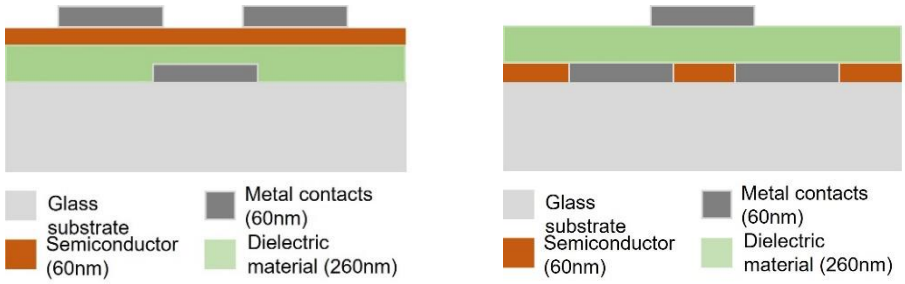

Figure 2 1 – Bottom gate architecture TFTs (left) Top gate architecture TFTs (right)

For the staggered bottom gate architecture, initially, 60 nm of Mo were deposited using the *AJA ATC-1800 F Orion Sputtering System.* For samples I-VI (figure B.1 appendix B), the Mo gates were defined using a photolithographic process: AZ ECI 3007 photoresist was deposited on the substrates by spin-coating, using *Suss Labpsin6 Spin Coater*. Following this, the substrates were placed on a hot-plate, at 90 ºC for 1 minute, for the soft-bake step. After this, they were placed in the mask aligner, where a mask to form the gate pattern was set, exposing the photoresist film to UV light. The sample was then placed again on the hot plate, at 110°C for 1 minute (post-exposure bake). To develop the pattern, an AZ 726 MIF Developer was used. To pattern the Mo, dry etching was carried out, using the previously mentioned RIE system, using SF_6 gas and lastly the substrate was submerged in acetone for approximately 10 minutes, to remove the photoresist. For sample VII (figure B.2, Appendix B) a shadow mask was used during the Mo deposition to define the pattern of the gate electrode. The dielectric layer was deposited and patterned, as described in section 2.1. To develop the pattern, samples were submerged in acetone for 30 minutes, then rinsed in water and dried out using a nitrogen gun. After this, 60 nm of IGZO were deposited using the *AJA ATC-1300 F Orion Sputtering System.* Again, for sample VII, no patterning was needed due to the use of shadow mask. For sample's I-VI the photolithography processes that followed were the same as for the gate, with 3 differences: Photoresist AZ nLof 2020 was used, with pre and post baking at 110ºC, for 2 minutes. The mask used was the semiconductor one and the type of etching, with wet etching being carried out. The substrates were immersed in HCl, diluted with a 20:1 ratio in H_2O, for 1 minute. To anneal the IGZO, the samples were placed on the heating plate at 180 ºC, for 60 minutes. Finally, for the drain and source electrodes, the deposition was the same as for the gate, apart from the deposition power, that was lowered. For patterning, sample VII used a shadow mask during deposition, while for samples I-VI, the process was like the previous gate patterning, but with AZ nLof 2020 photoresist being used, with its respective pre and post baking for 2 minutes at 110 °C, and with the drain and source mask being used.

For the top staggered gate TFTs (samples VIII and IX, figure B.3, Appendix B), first the Mo layer was deposited and patterned using the source and drain mask, with the same process as for the gate in samples I-VI. For the IGZO layer, the patterning was performed using the lift-off technique: AZ ECI 3007 photoresist was spin coated onto the substrate, followed by a 90°C, 1 minute baking and an exposure through the semiconductor photomask, to UV light. After this, another 1-minute baking, at 110 °C was carried out, followed by development. With the pattern formed in the photoresist, the IGZO was then deposited, in the same conditions as before. This was followed by the lift-off of the photoresist and IGZO, by putting it in acetone, then again, in another container with acetone and then in IPA, all for 10 minutes. Afterwards, the dielectric was deposited and patterned, as explained before and next, the Mo gate electrodes were deposited, again lowering the power deposition, and patterned using the gate mask, with the same process as source and drain electrodes in samples I-VI, but with wet etching carried out instead.

2.4. Characterization of dielectric films, MIM capacitors and TFTs

The films thickness was determined by profilometry, using *Dektak* Profilometer.Transmittance measurements were performed using a *Lambda 950 - Perkin-Elmer* with integrated sphere. Atomic force microscope topographic images were acquired with an Asylum Research MFP-3D Standalone system (Oxford Instruments, UK) operated in room conditions, in alternate contact mode, using silicon probes (*Olympus AC160TS*, f_0 = 300 kHz, k = 26 N/m). Topographic images were low-level plane fitted and exported to images using the *Gwyddion* software. Lastly, SEM/EDS characterization was performed, using a working station *Zeiss Auriga SEM-FIB*, with an *Oxford XMAX 150* detector, controlled by the *AZtec* software, from *Oxford Instruments*, using as beam conditions an acceleration voltage of 10 kV, a 60 µm aperture and a 5 mm working distance.

Both the MIM and TFTs were electrically characterized with a *Cascade Microtech EPS 150* manual probe station. CV, CF and IV measures were taken, controlled by a *Keysight B1500A semiconductor parameter analyser*. All measurements were obtained in the dark, at room temperature. For the MIM capacitors, the capacitances were measured from 1 kHz to 5 MHz and for the IV and CV measurements, a sweeping from -5 to 5 V was used. To characterize the TFTs, the parameters of the transfer curve were a V_{GS} sweeping from -3 to 8 V with V_{DS}=0.1 V for the linear region and V_{DS}=10 V for the saturation region and for the output curve, a V_{DS} sweeping from 0 to 10 V, with V_{GS} between 0 and 6 V, with step=1 V.

3. RESULTS AND DISCUSSION

In this chapter the results for the characterization of the film and the devices fabricated are shown.

3.1. Dielectric film characterization

3.1.1. Thickness

Firstly, the thickness of the films was measured by profilometry. A table with the various average thicknesses and standard deviation obtained for different measurement steps and a curve showing the average thickness dependence on the spinning speed and over those different steps are shown, on table 3.1 and figure 3.1. Step 1 is pre-UV, step 2 is pre-acetone, step 3 is post-acetone for 10 seconds and step 4 is post-acetone for 30 minutes. The reason for a measurement both after 10 seconds, and after 30 minutes is to ensure the film maintains its thickness after the 30 minutes in acetone, as required for patterning (as other tests showed, explained in section 3.3.1). As stated by *Solvay*, the crosslinking percentage is determined by equation 3.1 where T3 is the thickness after immersion in acetone for 10 seconds and T2 is thickness pre-acetone. If the polymer is fully crosslinked, this value should be close to 100 %. All the samples show values between 99.4 and 99.7%, evidencing that the dielectric polymer is almost completely crosslinked after a correct UV exposure (4440 mJ.cm^{-2}). The optimization of the correct dose to crosslink the polymer is of extreme importance and is further clarified in sections 3.2.1 and 3.2.2.

The values obtained for thickness are somewhat different from the expected values from the data provided by *Solvay*, however this difference is acceptable, as these values are merely indicative for this polymer in all its formulations and not specific for the formulation used in this work.. In table 3.1 it is seen that a higher spinning speed produces a thinner film, as expected from this technique [28], and in figure 3.1 a more coherent thickness is obtained throughout all measurement steps, for 2000 rpm. This would be expected, given the lower thickness of these films (i.e., higher thickness would require higher UV dose). Moreover, for the intended application as gate dielectric, a reduced thickness would be desirable to warrant a large gate capacitance, thus lower operating voltages. Due to these arguments, to fabricate the devices that followed and to do the remaining characterization, the speed chosen to produce the films was 2000 rpm, which is also the one that guarantees a higher XL (%).

$$XL\ (\%) = \frac{T3}{T2} \times 100 \tag{3.1}$$

It is important to note, that a measurement of thickness after 30 minutes in acetone had not been performed by *Solvay*, so there was no expected value in the data for these conditions.

Table 3. 1 – Average thicknesses and standard deviation obtained for the films for 1000, 1500 and 2000rpm, before UV (4440mJ.cm^{-2}), pre-acetone, post-acetone, for 10 seconds and 30 minutes.

Spinning speed		Thicknesses (nm)				XL(%)
	Pre-UV (T1)	Pre-acetone (T2)	Post-acetone (10s) (T3)	Expected value for T3 (*Solvay* data)	Post-acetone (30 mins) (T4)	$\frac{T3}{T2}$
2000 rpm	271.6 ± 20.8	266.9 ± 20.9	266.1 ± 21.6	200	260.3 ± 17.6	99.7
1500 rpm	322.3 ± 12.0	323.8 ± 17.4	321.8 ± 20.7	300	315.3 ± 19.8	99.4
1000 rpm	452.2 ± 22.2	435.8 ± 15.5	433.9 ± 18.3	400	423.2 ± 18.0	99.6

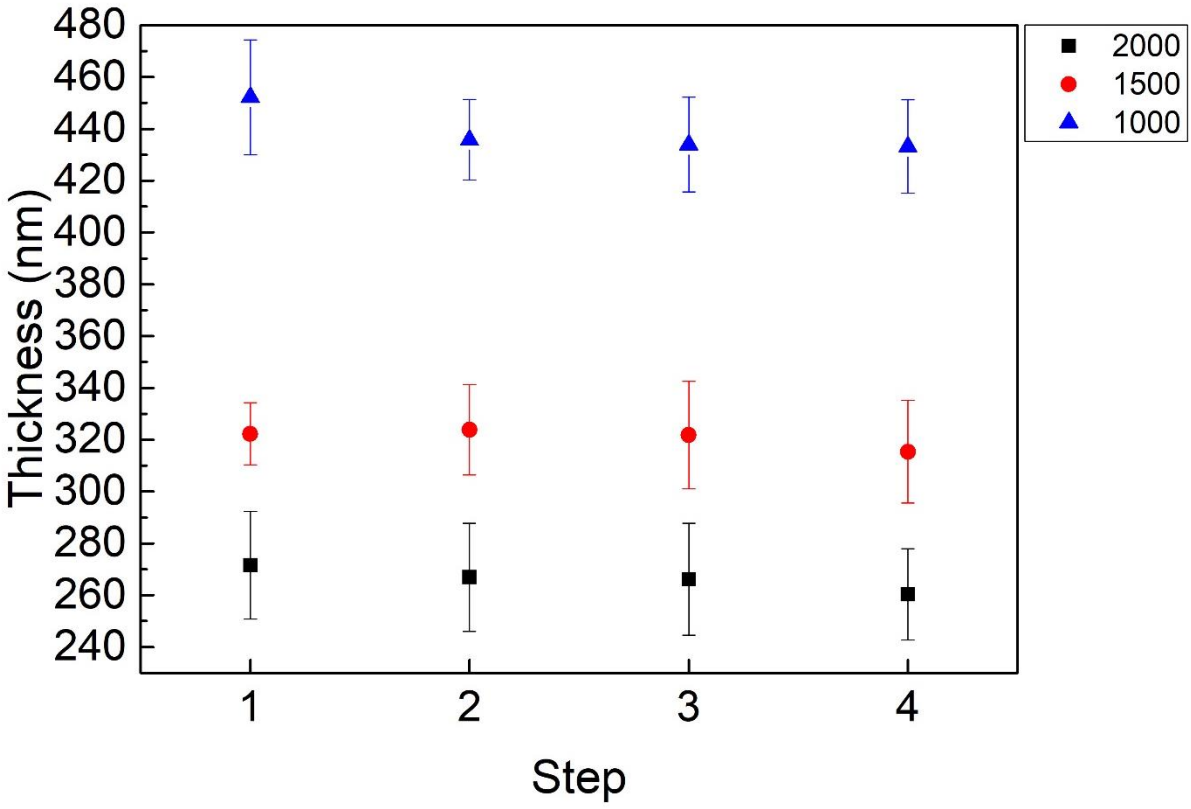

Figure 3. 1 – Average thicknesses and standard deviations obtained for the films for 1000, 1500 and 2000rpm, before UV (4440mJ.cm^{-2}), pre-acetone, post-acetone, for 10 seconds and 30 minutes.

3.1.2. Surface roughness

The films produced had a lusterless appearance after 30 mins immersed in acetone. To assess the effect of the acetone on the film surface, the root-mean-square (RMS) roughness was taken from AFM images before and after acetone. As an extra test, the effect of an annealing temperature of 180 °C, for 1 hour (temperature and time needed for the annealing of the IGZO layer for the TFT fabrication), was also investigated. The values are reported in table 3.2.

Table 3. 2 - RMS roughness for samples pre and post acetone, and post annealing.

	Pre-acetone	Post-acetone (30 mins)	Post-annealing (180°C)
RMS roughness (nm)	0.4109	10.92	7.677

The RMS roughness goes from 0.4109 nm before the acetone immersion, to 10.92 nm, which clearly demonstrates the effect that acetone has on the surface of the film, creating a rougher surface. This difference is also visible in figure 3.2. After the annealing step, the difference in surface roughness is not relevant.

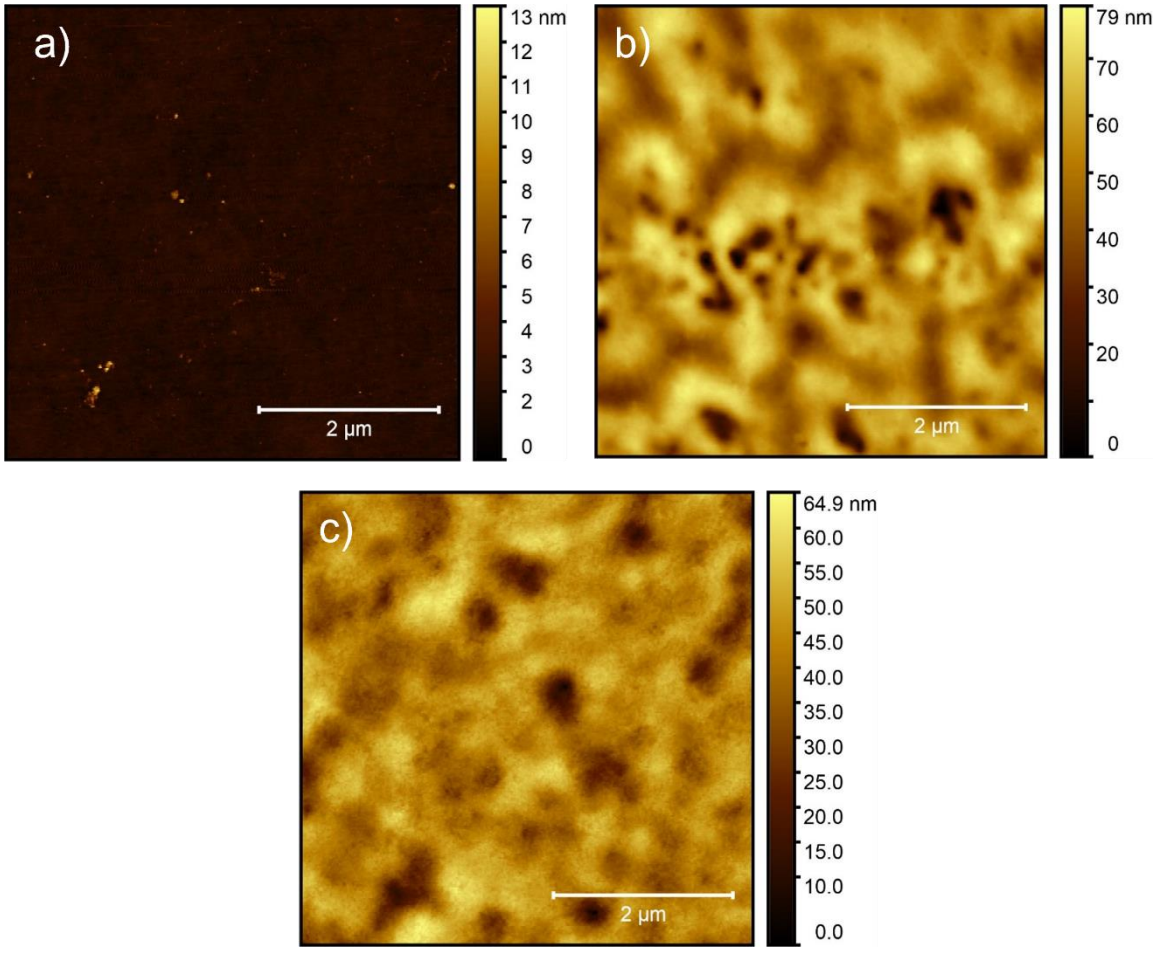

Figure 3. 2 - AFM images for cured samples: a) before acetone b) after 30 minutes in acetone c) after annealing temperature.

3.1.3. Transmittance

As said before, this material is a perfect candidate to be used in transparent electronics, so transmittance measurements were performed in the films. The samples were measured again after the same treatments as for the AFM measurements, the results are shown in figure 3.3 and table 3.3.

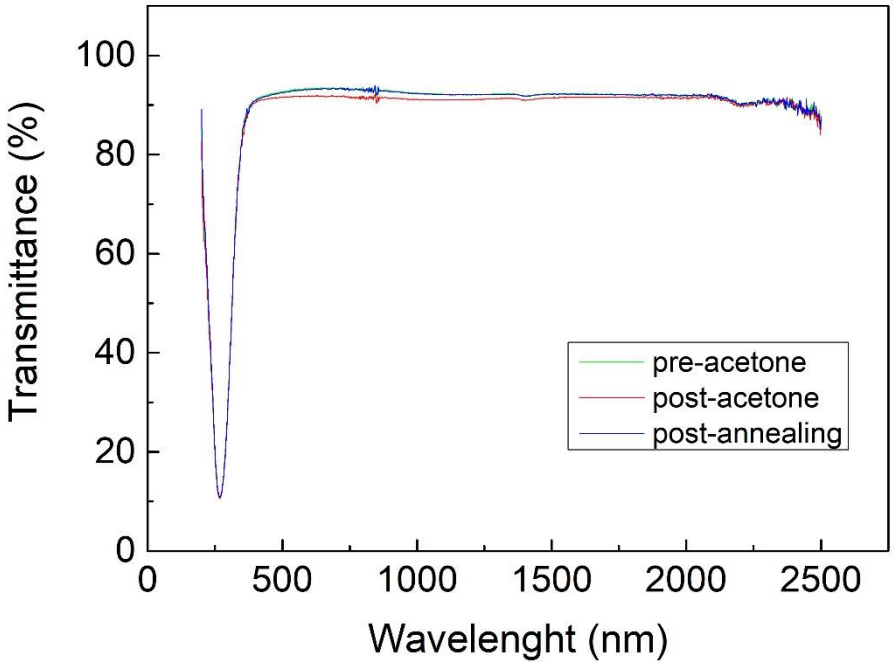

Figure 3. 3 - Optical transmittance of the photopatternable polymer dielectrics on glass substrate for pre-acetone (green), post-acetone (red) and post-annealing (blue) conditions.

Table 3. 3 – Optical transmittance values for 550nm (visible light).

	Pre-acetone	Post-acetone (30 mins)	Post-annealing (180°C)
550 nm	93.1%	91.7%	92.9%

Transmittance values are all higher than 90%, evidencing the ultrahigh transparency of the film. The acetone immersion doesn't seem to affect the film's transparency and despite its value being slightly lower, the annealing temperature effect also does not seem to be noticeable.

3.2. **MIM devices**

MIM devices were produced to study dielectric performance. Each sample has 6 capacitors named A to F, where A is the largest and F the smallest, as seen on figure 3.4. Each intersection of electrodes corresponds to a different capacitor. The areas of these capacitors can be consulted on table 3.4.

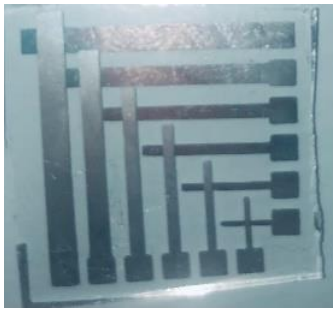

Figure 3. 4 - MIM capacitors on a sample.

Table 3. 4 - MIM capacitor area in mm^2.

	A	B	C	D	E	F
Area (mm^2)	4.00	2.43	1.24	0.77	0.39	0.17

During the electrical characterization of many samples, capacitor A, which is the one closest to the edge of the sample, was not working properly, being in short circuit, or simply with a very high leakage current. This can be justified by the fact that, when using a technique like spin coating, the film edges are always thinner and less homogeneous than the rest of the sample [28]. Furthermore, these are the largest area capacitors, thus with increased probability of having pinholes that would inhibit proper electrical insulation.

3.2.1. Gen 1 MIM capacitors

The first capacitors fabricated were cured using the doses presented on table 3.5. Although this dose revealed not to be nearly sufficient to cure the films (as other tests showed), the samples still proved to insulate properly.

Table 3. 5 - Doses used for curing each sample.

	Sample 1	Sample 2	Sample 3	Sample 5	Sample 4	Sample 5
Dose ($mJ.cm^{-2}$)	0	10	30	50	70	90

Capacitance-Voltage (CV), Capacitance-frequency (Cf) and Current-Voltage (IV) measurements were performed. The capacitance density is the capacitance *per unit area* and Figure 3.5, shows the plot for the capacitance density for a voltage between -0.5 V and 0.5 V for samples 1, 3, 5 and 6. For the sake of clarity, samples 2 and 4 were left out of the figure, because the remaining were already representative of the data.

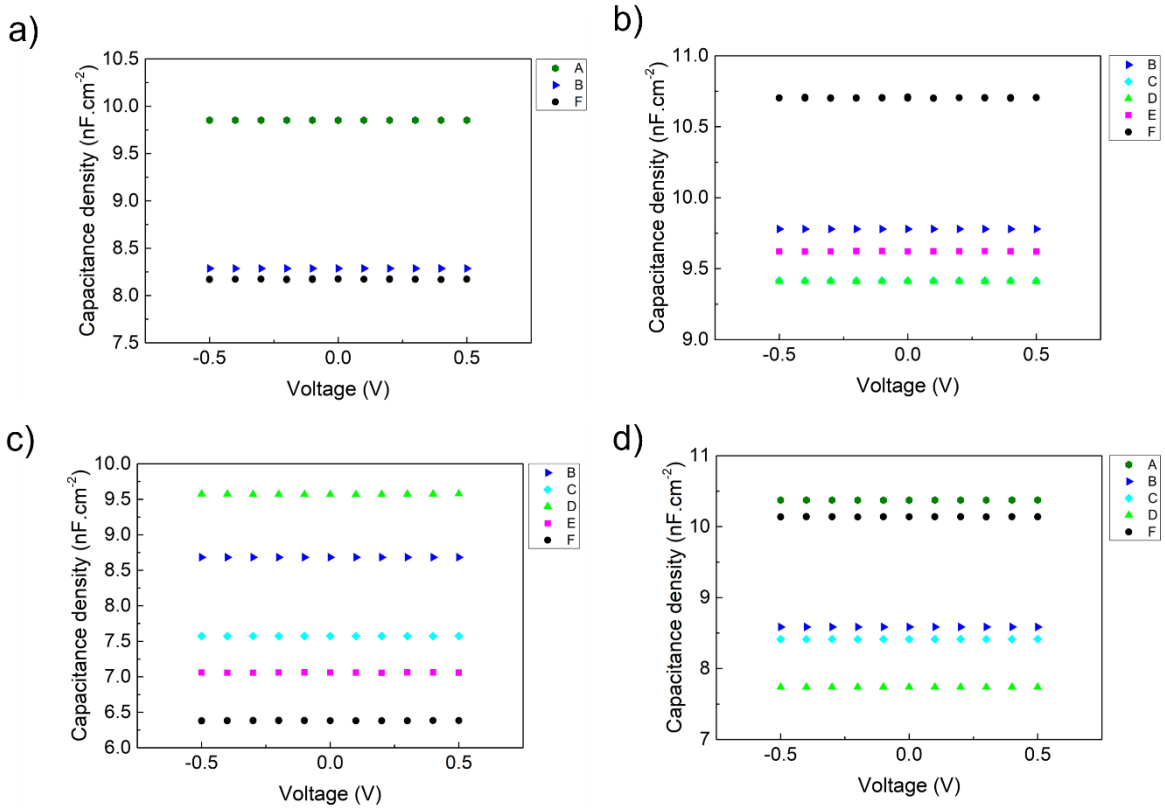

Figure 3. 5 - Capacitance density over voltage measures: a) sample1, not cured b) sample 3, cured ($30mJ.cm^{-2}$) c) sample 5, cured ($70mJ.cm^{-2}$) and d) sample 6, cured ($90mJ.cm^{-2}$).

A small variation between capacitors can be observed within the same sample. This variation can be because not all capacitors produced in all samples had their areas measured and were all assumed to have the same area. However, this is not the case, and it is known that different depositions and different placing of the masks will produce capacitors with different areas. Despite this fictional variation, results show the homogeneity of the sample to extract a very important parameter, the dielectric constant, κ, calculated with equation 3.2:

$$\kappa = \frac{C \times d}{\varepsilon_0 \times A} \tag{3.2}$$

Figure 3.6 shows the average κ for each sample, over the UV dose.

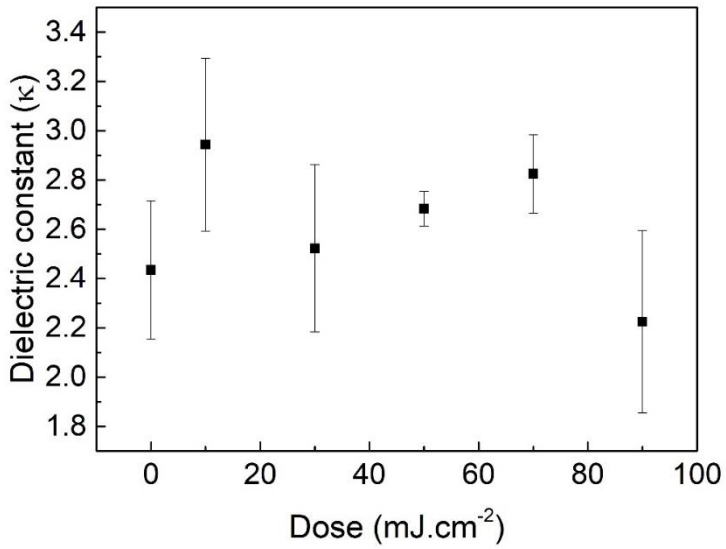

Figure 3. 6 - Average dielectric constant according to the dose used for each sample.

There doesn't seem to be a tendency in this plot meaning a higher dose does not necessarily correspond to a higher κ. Despite the small κ, almost all capacitors showed an insulating behavior for a low voltage (<5 V). To demonstrate this, the IV curve for capacitor B on all samples is presented in figure 3.7. For higher voltages the current seems to increase rapidly, which is explained by fact that the polymer is not fully cross-linked at these doses, as stated by *Solvay*.

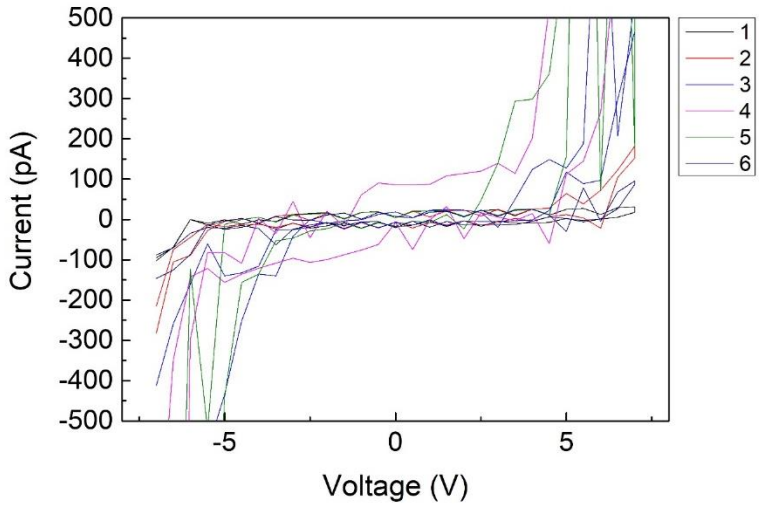

Figure 3. 7 - IV curve for capacitor B in all samples.

Finally, figure 3.8 is the plot of the capacitance density over frequency for samples 1, 3, 5 and 6. A frequency between 1 and 1000 kHz was used. The capacitors seem to roughly maintain their capacitance density until 500 kHz.

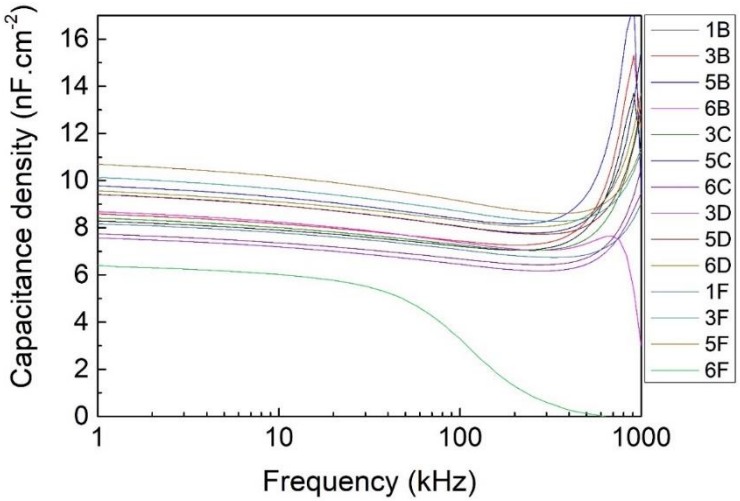

Figure 3. 8 - Capacitance density over frequency for capacitors in samples 1, 3, 5 and 6.

The average and standard deviation for important parameters one each sample are summarized in table 3.6 (average of the 6 capacitors in each sample). As can be observed, the average dielectric constant is 2.60, which is considered a low κ and is not between the expected values for this material, which should be over 10, according to *Solvay*. This low value is also due to the fact that the polymer is not fully cross-linked. [27].

Table 3. 6 – Average (of the 6 capacitors per sample) dielectric constant and capacitance density and respective standard deviation for all samples.

	1	2	3	4	5	6
Dielectric Constant κ (1kHz)	2.43 ± 0.28	2.94 ± 0.35	2.52 ± 0.34	2.68 ± 0.07	2.82 ± 0.16	2.22 ± 0.37
Capacitance Density ($nF.cm^{-2}$) (1kHz)	8.27 ± 0.94	9.38 ± 1.20	8.59 ± 1.14	9.14 ± 0.25	9.61 ± 0.54	7.57 ± 1.27

3.2.2. Gen 2 MIM capacitors

As mentioned before, the UV exposure used previously was not enough to cure the films, so after that a tuning process began, to find the optimal conditions to make sure the film was properly cured.

Lastly, the correct dose and baking temperature was achieved. New MIM capacitors were then fabricated using the doses on table 3.7.

Table 3. 9 - Doses used for curing each sample.

	I	II	III	IV
Dose ($mJ.cm^{-2}$)	5838	4438	3038	1638

Again CV, Cf and IV measurements were performed and capacitance density as well as dielectric constant κ, were calculated. Figure 3.9 shows the plot for the capacitance density over a voltage between -5 and 5V, for all the samples. As can be noted, the capacitance density is higher, being roughly 3 times as much as the Gen 1 samples, further proving this is the correct dose to expose this polymer. All samples show a similar value, with the small difference justified as before, with the areas of capacitors in each sample being assumed the same as the only sample measured.

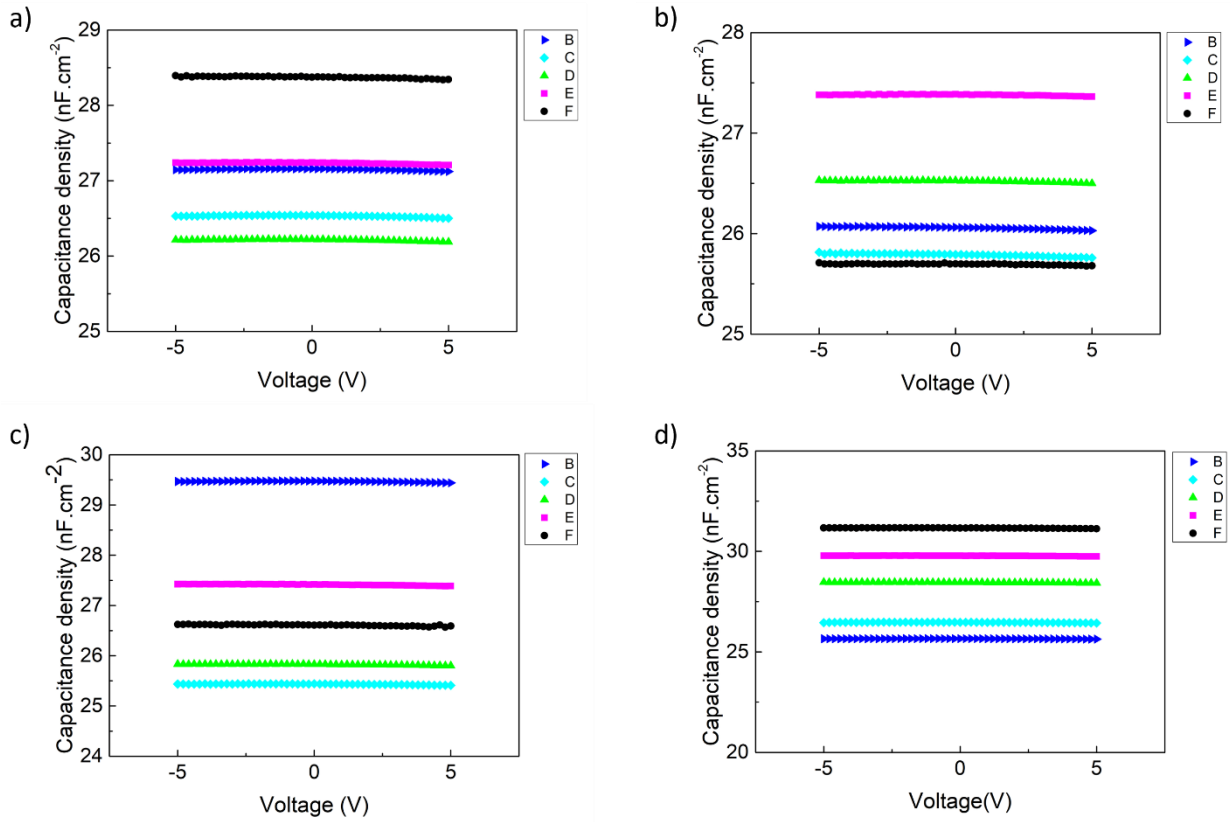

Figure 3. 9 - Capacitance density over voltage measures: a) sample I (5838mJ.cm^{-2}) b) sample II (4438mJ.cm^{-2}) c) sample III (3038mJ.cm^{-2}) and d) sample IV (1638mJ.cm^{-2}).

The average κ for each sample was calculated and a plot with the dose used in each sample is shown in figure 3.10.

The sample with highest κ, at 8.35 was II. This dose was chosen to fabricate the TFTs as explained in the end of this section, and as such, the following characterization plots are only shown for this sample.

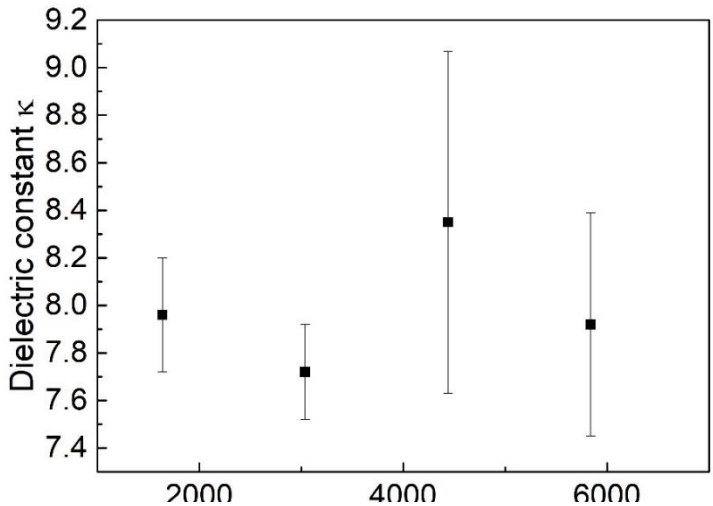

Figure 3. 10 - Average dielectric constant and respective standard deviation according to the dose used for each sample.

Figure 3.11 portrays the capacitance density stability of sample II over frequencies between 1 and 1000 kHz. All capacitors show a decrease of capacitance density lower than 10nF.cm^{-2}, a consequence of a difficulty that arises for the charges to follow the ac signal for higher frequencies, a tendency supported by literature[29], [30]. It is also seen that the capacitance density increases as the device gets smaller, which might be justified with the fact that the sample is not as smooth as it should be, leading to thickness being thinner on the outer portion of the sample, thus leading to a higher capacitance density for the smaller capacitors (the ones closer to the edge of the sample).

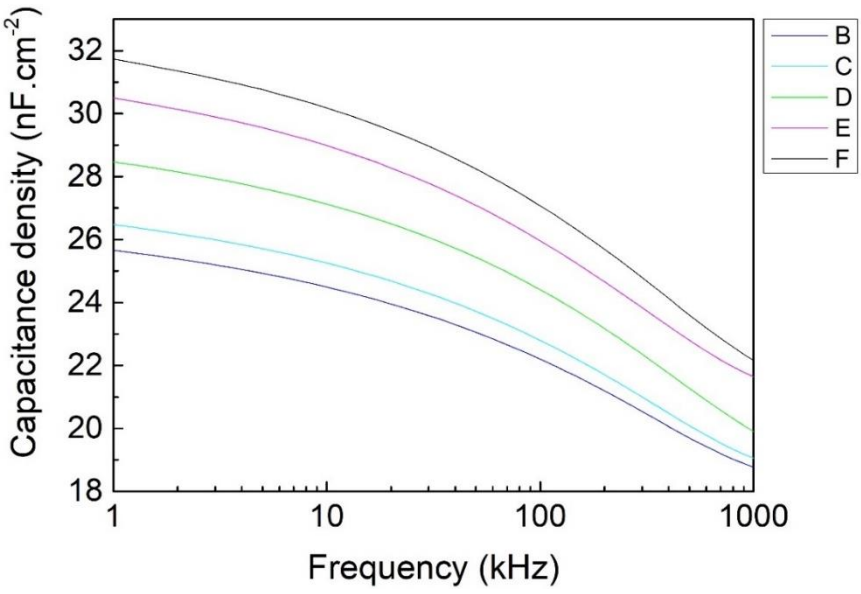

Figure 3. 11 - Capacitance density over frequency for sample II.

Figure 3.12 shows the leakage current density for capacitor B on sample II, over the electric field from 1 to 3.75MV.cm^{-1}. At 1MV.cm^{-1}, the leakage current density is 1.28×10^{-7}A.cm^{-2}. For all capacitors, after this electric field, the tips of the measuring equipment seemed to lose contact with the metal on the electrodes, as observed in figure 3.12, resulting in only noise being measured from that point onward. This was a consequence solely from the top electrodes, that visibly show superficial damage, as depicted figure A.2, Appendix

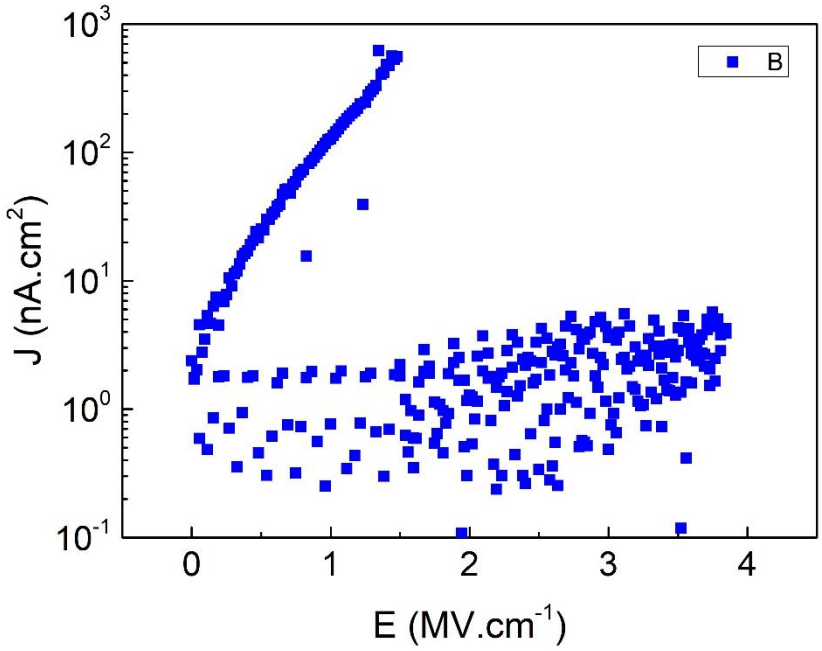

Figure 3. 12 - leakage current density for capacitor B in sample II.

A. If the tip was moved onto an undamaged site, and a new measure was performed, the behavior was the expected, with leakage current linearly increasing until loss of contact with the metal again.

To better illustrate this effect, figure 3.13 shows the I-V curve, for a voltage up to 100V. Table 3.8 shows all referred parameters summarized, for all samples. As this tip effect took place, it was not possible to achieve the breakdown field for these samples. Nonetheless, it can be guaranteed that up until the loss of contact, no breakdown was reached and those are the values reported here. The differences in the values obtained are not representative of the insulating properties of each sample, but rather a product of the difficulties in the measurements (due to the effect explained before).

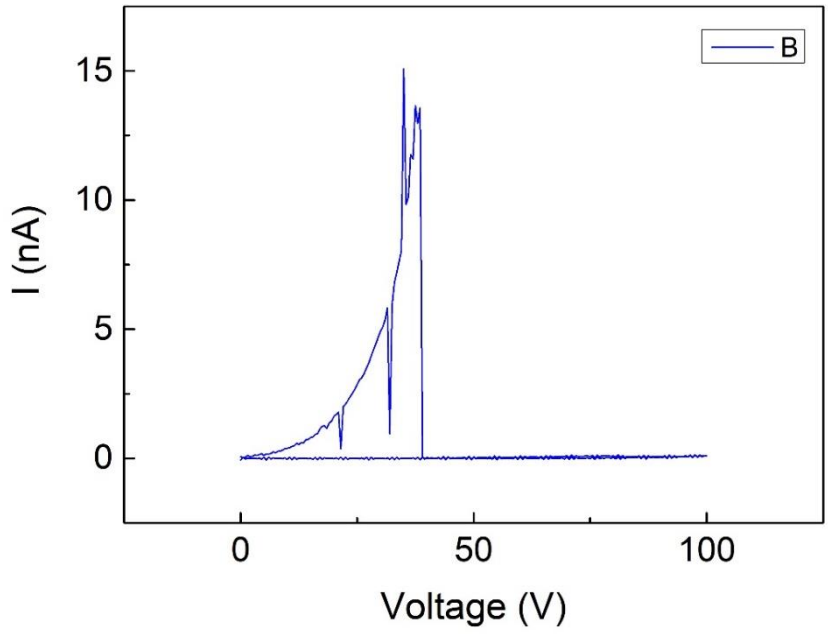

Figure 3. 13 - IV curve with a voltage sweeping of 100V.

Table 3. 7 - Device parameters for capacitors in samples I-IV.

	I	II	III	IV
Dielectric Constant κ (1 kHz)	7.92 ± 0.47	8.35 ± 0.72	7.72 ± 0.20	7.96 ± 0.24
Capacitance Density ($nF.cm^{-2}$) (1kHz)	26.61 ± 1.58	28.42 ± 2.47	26.06 ± 0.69	27.16 ± 0.83
Leakage current density ($A.cm^{-2}$) ($1MV.cm^{-1}$)	4.06×10^{-7} ± 8.55×10^{-8}	1.07×10^{-7} ± $6{,}43\times10^{-8}$	3.76×10^{-7} ± 5.87×10^{-8}	4.19×10^{-7} ± 1.84×10^{-8}
Breakdown field ($MV.cm^{-1}$)	>2	>1.5	>2.25	>1.75

The dose on sample II, with the highest κ, and the lowest leakage current density, presented itself as being the dose suited to be used in the following TFT fabrication. To obtain such dose, the time needed is around 5 minutes. This time seemed sufficient to guarantee the best crosslinking of the polymer while not exposing it to UV light for too long, which can lead to optical scattering phenomena in the glass masks used for patterning the TFTs.

3.3. TFTs

In this section, three different types of TFTs are reported. The objective was to test not only different architectures (top and bottom gate), but also different fabrication techniques, using both lithography and mechanical masks to pattern the device. The dielectric layer was produced using the same conditions for the gate dielectric film as the dielectric layer for the MIM devices in section 3.2.2. An average thickness of 260 nm is used for the parameter calculations.

3.3.1. Lithography tests

Before starting to fabricate TFTs, the patterning resolution was tested. The polymer was deposited over an aluminum film and then exposed to UV light through a photomask with 200×200 µm dark squares. As this material behaves like a negative photoresist, after development, the film should have open squares, revealing the aluminum underneath it. No information from Solvay was given regarding the time needed in acetone to reveal the pattern, so different times were tested. Optical microscopic images of the patterns formed were taken and figure 3.14 shows these images after 5, 15, 30 and 60 minutes of development. The pattern is the sharpest after 30 minutes and before this, even though the squares are already visible, they have no contrast. After 1 hour the pattern almost disappears, suggesting that even the cured polymer starts to be removed.

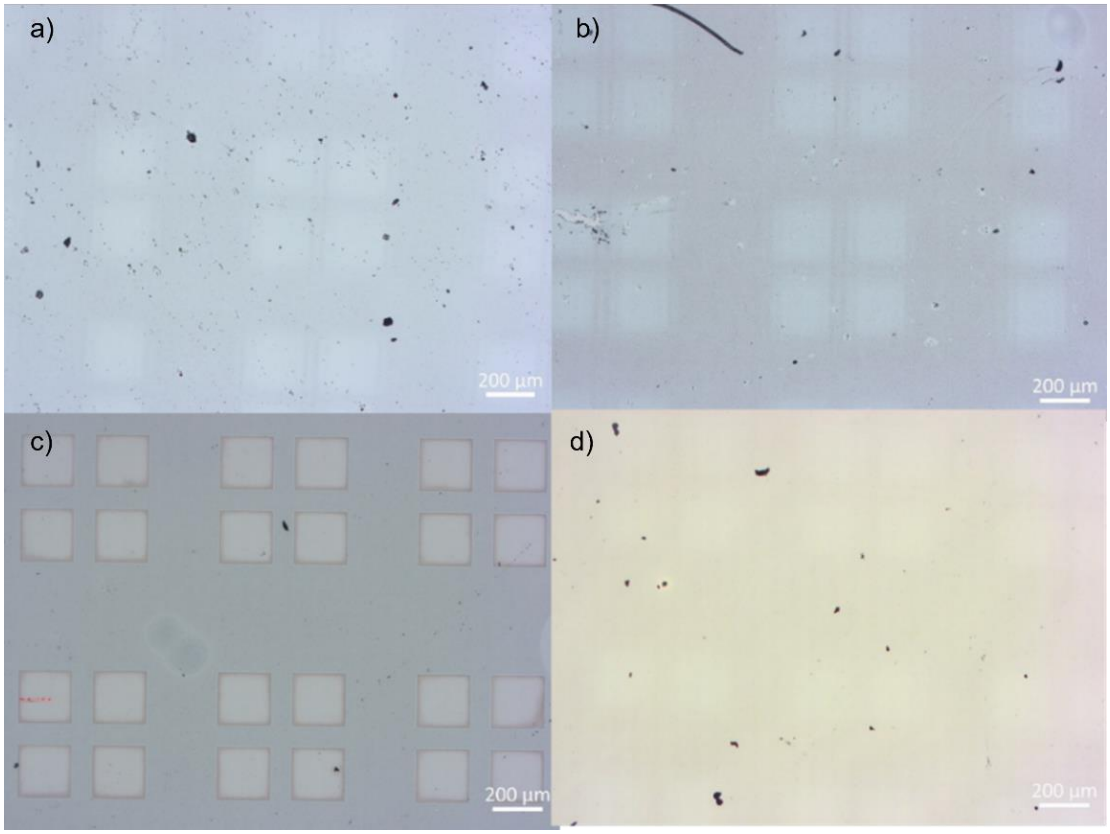

Figure 3. 14 - Optical microscopic images of the pattern formed in the film after a)5 minutes b)15 minutes c)30 minutes d)60 minutes.

To further corroborate the observations of these images, energy dispersive X-ray spectroscopy (EDS) measurements were performed on the 30 min sample. Figure 3.15 shows a SEM image of the sample and figure 3.16 shows the spectra of elements found on the squares (spectrum 2) and outside (spectrum 3). Inside the square, the elements found are O, Al, C, Si, Ca, and F. The carbon is a normal contamination of the sample and Si, O are surely components of the Corning glass substrate, while Ca is probably also in its composition

(as it is not expected to be in the polymer composition), but no literature was found on this matter. The only elements remaining are Al, from the aluminum film deposited below the polymer and F, which is in the polymer composition. This could mean that remaining traces of the film might still be in the opened squares, but to be certain of this statement, the glass substrate composition should be known. As for outside the squares, in spectrum 3, the characteristic elements of the polymer, like C and F are found in much higher quantities and Cl, which is only present in the polymer, is also found, whereas before there were no traces of it. By looking at these data, seems that the pattern is formed but there are little traces of the polymer where it should not be, meaning it is almost completely removed by acetone after 30 minutes, however further optimization is still required. Table 3.9 shows the atomic percentages of the elements found in each site on the sample.

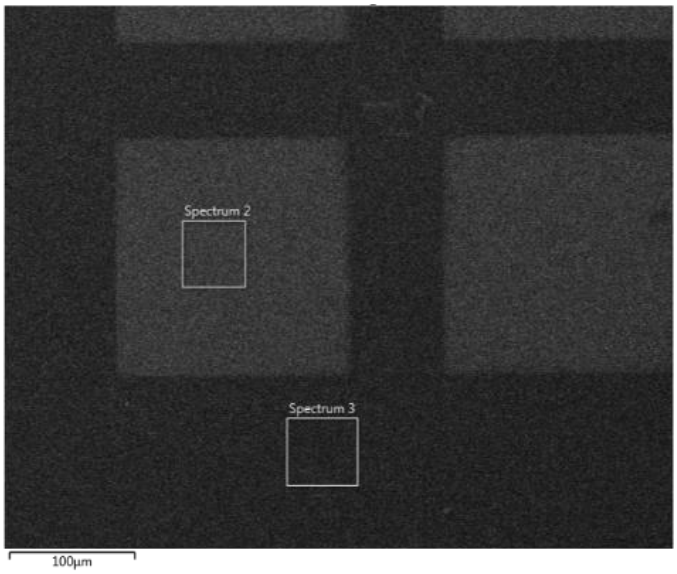

Figure 3. 15 - SEM image of the photopatterned polymeric dielectric on glass, showing etched (light gray) and non-etched (dark gray) regions used for EDS analysis.

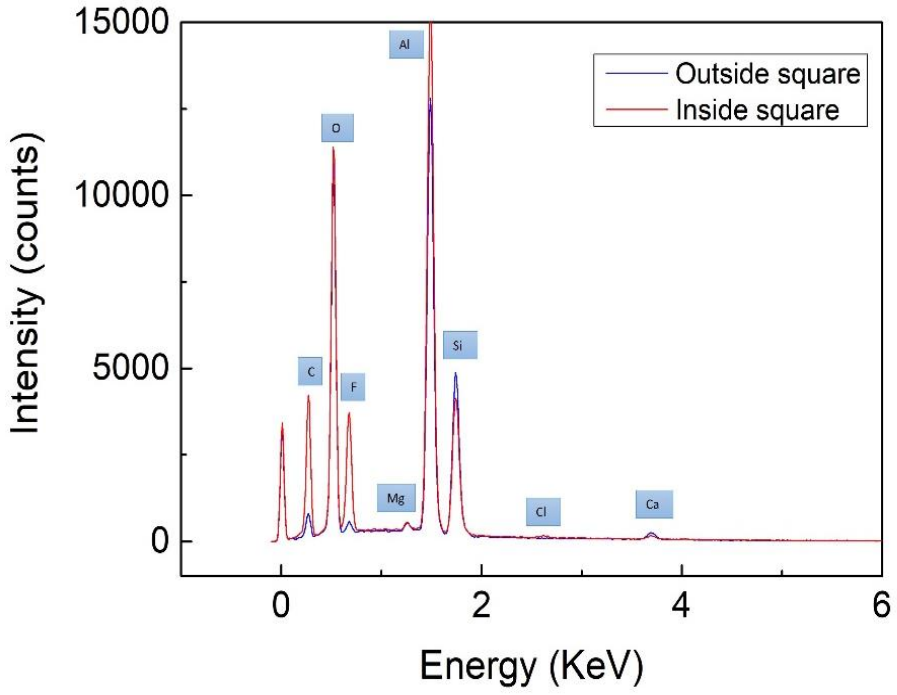

Figure 3. 16 - Spectra of elements inside the square (spectrum 2) and outside the square (spectrum 3)

Table 3. 8 – Atomic % found in each site of the sample (developed and undeveloped pattern).

	Atomic %							
Element	C	O	F	Mg	Al	Si	Cl	Ca
Developed pattern (inside squares)	10.66	48.03	1.73	0.47	25.82	12.19	-	1.10
Undeveloped pattern (out-side squares)	32.27	31.93	10.16	0.26	18.93	6.02	0.12	0.32

3.3.2. Bottom Gate TFTs

The devices fabricated with the architecture shown in figure 3.17 were patterned both by lithography and using mechanical masks. Despite efforts to adapt the fabrication techniques to this polymer, all TFTs in these samples had a very high gate current, reaching the compliance of the measuring equipment. This means the dielectric material was not insulating, suggesting that it could be affected by the IGZO deposition afterwards. Figure 3.18 shows an example of the typical transfer characteristic for all these TFTs.

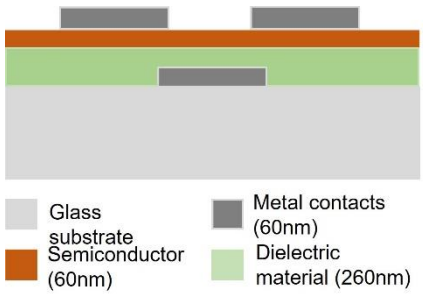

Figure 3. 17 – Staggered bottom gate architecture of TFTs produced.

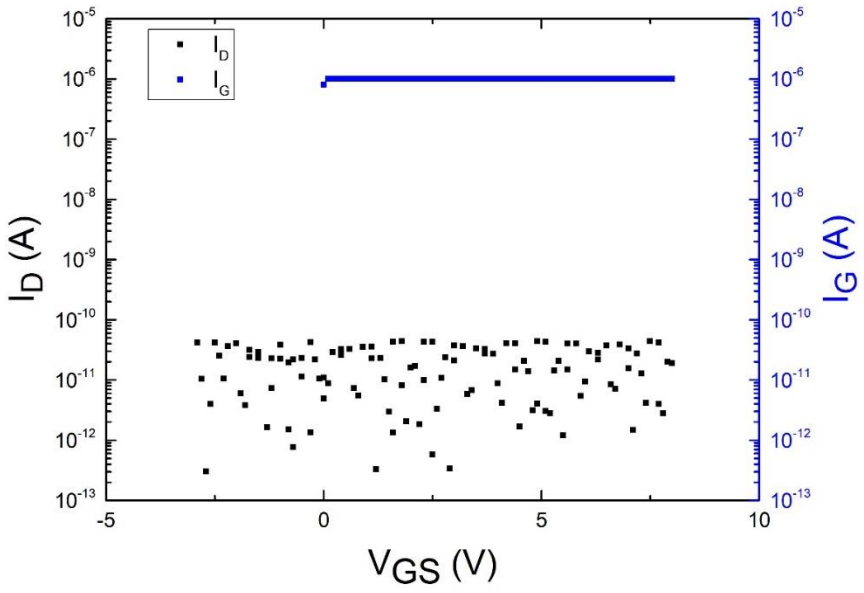

Figure 3. 18 - Representative transfer characteristic for all BG TFTs. VDS=10V.

It is highly possible that the IGZO sputtering deposition has a damaging effect on the dielectric polymer. The reason for this hypothesis is that the bottom gate TFTs are fabricated with mechanical masks (sample VII). In this sample, the TFTs show the same problems as the ones patterned by lithography which discards lithography as the reason for problems with the high leakage current. Besides, the film in the mechanical mask BG TFTs was insulating properly prior to the IGZO deposition (a simple test was performed by measuring the resistance, where values of around 11MΩ were obtained), further corroborating that the IGZO sputtering deposition must be the cause for this. This is an indication that a better suited architecture for the TFTs produced with this material is top gate.

3.3.3. Top Gate TFTs

Sample VIII and IX were fabricated in this architecture, as seen on figure 3.19. Due to deposition and/or lithography difficulties, most transistors couldn't be accessed, showed no modulation of current or had a very low field effect mobility. These problems arose after the dielectric material deposition, during the patterning of top electrodes with HCl. This acid had a damaging effect on the semiconductor and on the dielectric. Also, as to respect the time the dielectric can withstand acetone, the photoresist could not be left in acetone sufficient time to remove completely the remaining photoresist. Figure 3.20 are microscopic images of some TFTs in

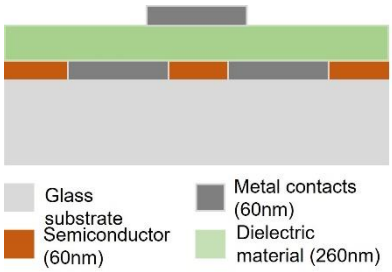

Figure 3. 19 – Staggered top gate architecture of TFTs produced.

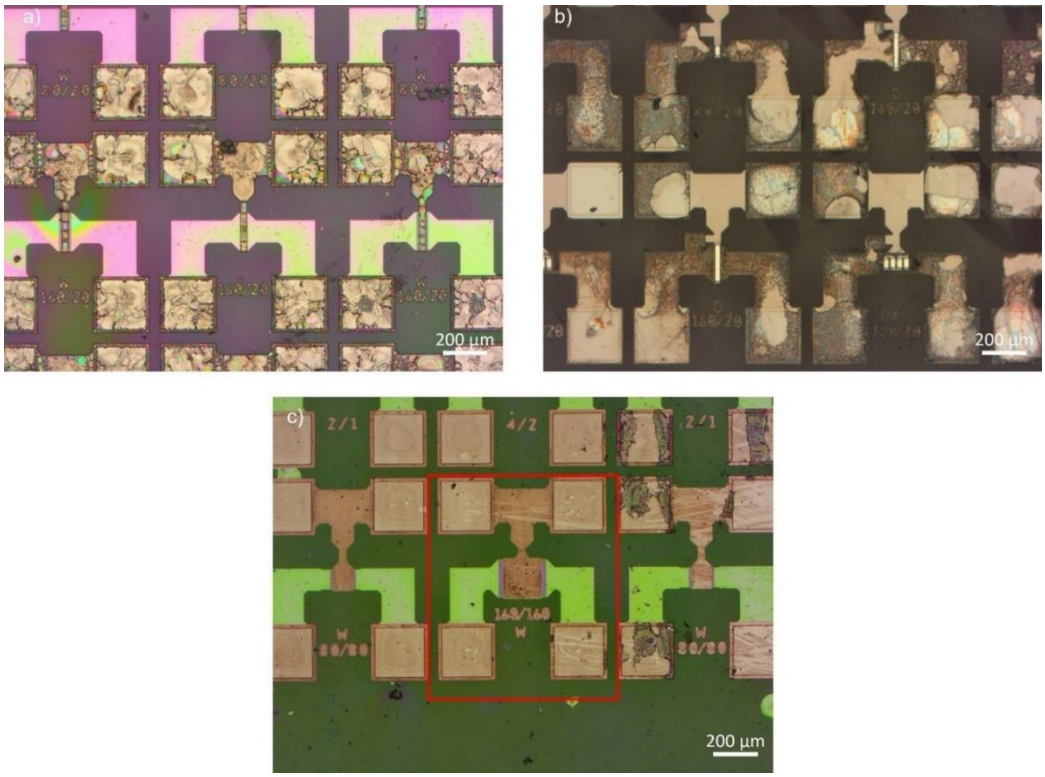

Figure 3. 20 – Optical microscope images of TFTs in samples VIII (a) IX (b) and the characterized 160×160 µm TFT (c), as seen inside the red square.

the top-gate samples, to show remains of photoresist in the sample, that impeded the access to the top contacts. Still, in sample IX some transistors could be successfully measured, as the one with aspect ratio (W/L) of (160×160) µm, shown in figure 3.20 (c).

Transfer and output curves for this TFT can be seen on figures 3.21 and 3.22. In the transfer curve, hysteresis is observed, which is attributed to the charges trapped in the interface between the semiconductor and the dielectric.[31] It can also be seen that the gate current (I_G) is at a range below nA, showing that the polymer is insulating properly. The on/off ratio is 10^5, for voltage sweepings as low as 8V. In the output curve it is seen that the maximum current obtained, at V_{GS}=6V is 0.39µA. The current crowding effect in the beginning of this plot is a characteristic effect of contact resistance already mentioned, which can be attributed to the lack of an annealing after the metal contacts deposition. The output characteristics also evidence ideal hard

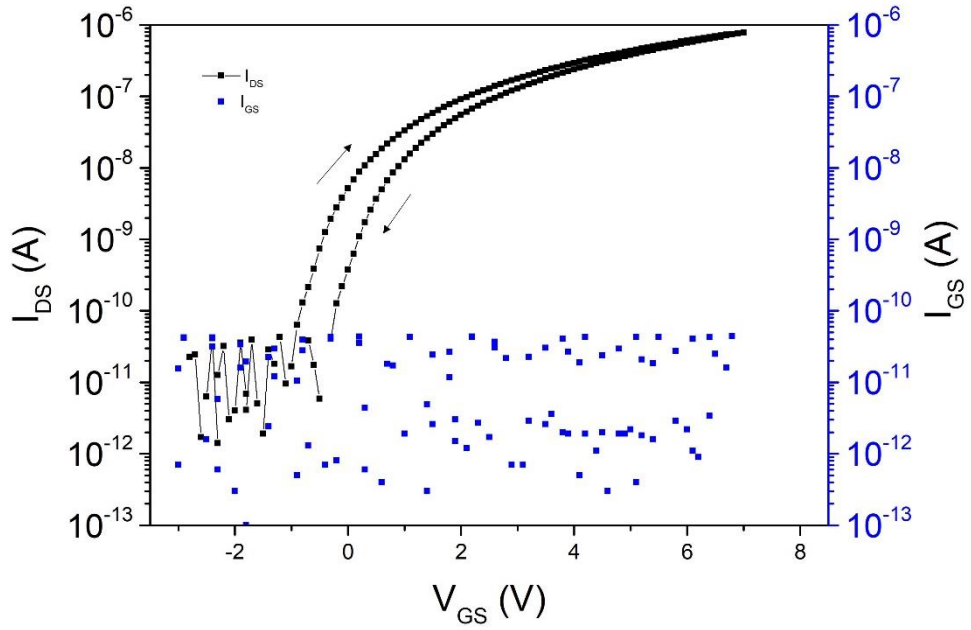

Figure 3. 21- Transfer characteristic for (160×160)µm IGZO TFT, with V_{DS}=10V.

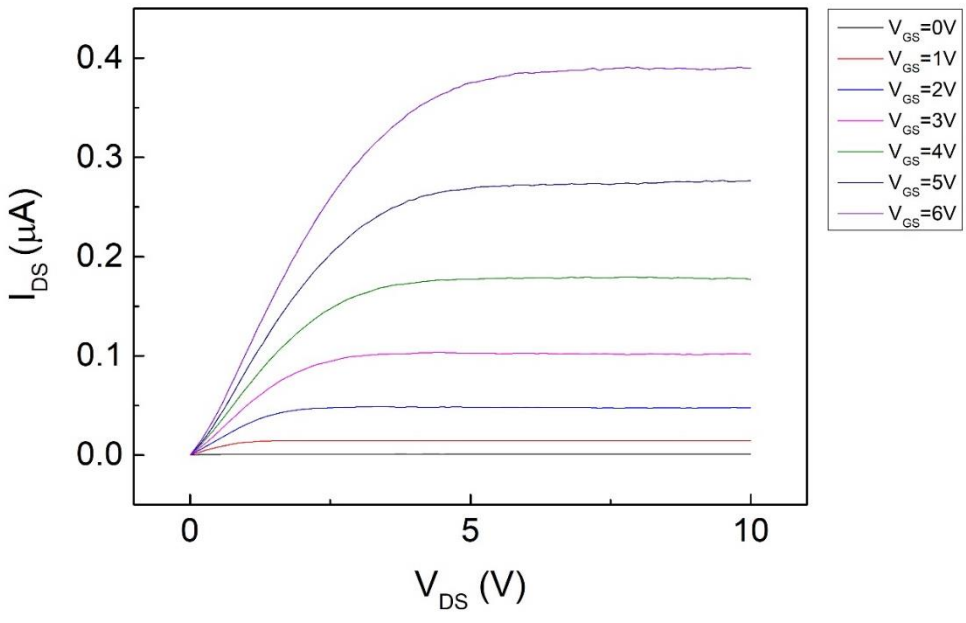

Figure 3. 22- Output characteristics for (160×160)µm IGZO TFT, with V_{GS}=[0,6], step=1V.

saturation, meaning that the channel can be fully depleted of free carriers close to the drain after pinch-off is achieved.

A CV measure was performed on this device to determine the capacitance density and dielectric constant. To ensure this value is correct (owing to the small device dimensions), a measure was also made on a MIM capacitor test structure of 300×300µm, present in the same sample and the results are shown in table 3.10. Although the dielectric material was deposited and cured using the same conditions as the dielectric in the MIM capacitors, with κ=8.35 and a capacitance density averaging 28.42 $nF.cm^{-2}$, the capacitance density obtained in the fabricated TFTs is much lower, at 5.177 $nF.cm^{-2}$ and a dielectric constant of 1.52.

Table 3. 9 - Capacitance density and dielectric constant for (160×160)µm IGZO TFT and the MIM capacitor on sample VIII.

	C_{on} (pF)	C_{off} (pF)	ΔC (pF)	Capacitance density (C/A) ($nF.cm^{-2}$)	Dielectric constant (κ)
TFT	1.787	0.459	1.33	5.177	1.52
MIM	4.84	0	4.84	5.378	1.58

This difference in the dielectric constant can be justified by two factors, all related to the fabrication of the TFTs. To pattern the other layers of the TFT, the dielectric had to be immersed in acetone for longer than 30 minutes (to remove photoresist) and despite efforts to minimize this time, it may have affected the dielectric properties of the material. In addition to this, the thickness on the TFTs is assumed to be 260 nm, which was the thickness measured for the curing and spinning conditions. However there is no certainty that this value is correct, meaning the dielectric constant portrayed here might not be accurate.

Figure 3.23 shows the saturation mobility for this device. This device showed a $\mu_{FE} < 3$ a μ_{SAT} of 7,07 $cm^2.V^{-1}.s^{-1}$ and a subthreshold swing was of 0.18 V/dec. The reason for a higher μ_{SAT} is a parameter that is less sensitive to contact resistance between electrodes and semiconductor, which was a pronounced effect in these TFTs, as seen before in the output characteristics. The evolution of μ_{SAT} with V_{GS} follows the expected trend, i.e., a significant increase after V_{on} and a stabilization/slight decrease for high V_{GS} due to increased interface scattering as the induced conductive channel is taken closer to that interface by the increased V_{GS}.

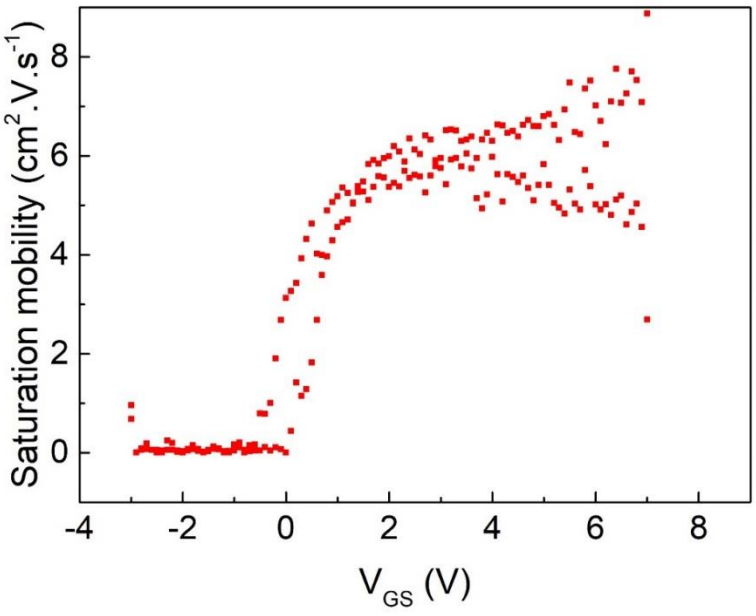

Figure 3. 23 - Saturation mobility for (160×160)µm IGZO TFT, with V_{DS}=10V.

Table 3.11 summarizes all the important parameters for the device fabricated in this work, comparing with devices produced in literature. By comparing the values obtained for the TFT produced in this work, it seems reasonable to say this transistor has a good performance. It is important to note that in literature, almost all papers report organic TFTs when trying to use a photopatternable material. This is probably due to the high compatibility of these films with low temperature techniques, characteristic of the OTFTs. As such, all those articles exhibit considerably lower mobility compared to the devices in this work. The only articles that use IGZO for the active layer are the ones by Lee *et al* and Rim *et al*, and as such are the works with more similar performance levels to the one obtained at CENIMAT. However, in the Lee case, the active layer was deposited not by sputtering, but by a solution process and the contacts were all deposited in a co-planar structure, with their deposition being prior to polymer, and hence not affecting it. As for Rim *et* al the whole TFT is obtained via solution processing as well, however an oxide already known for its good electric performance as a dielectric is used, so it is not comparable to the polymer used in this work, justifying their better results as well. Nevertheless, the present results already show the feasibility to incorporate the photopatternable polymeric dielectric provided by Solvay in CENIMAT's oxide TFT process flow.

Table 3. 10 - Device parameters for the IGZO TFTs produced in this work and other devices reported in literature making use of photopatternable gate dielectrics. The Semiconductor, dielectric and maximum process temperature are also shown. All mobility values are for the field effect mobility with the exception of the one produced in this work, being the saturation mobility.

	SC	Dielectric	Process temperature (°C)	Turn-on Voltage (V_{on}) (V)	Sub-threshold Swing (S) ($V.dec^{-1}$)	On/Off Ratio	Mobility (μ_{FE}) ($cm^2.V^{-1}.s^{-1}$)
IGZO TFT (produced in this work)	IGZO	Dielectric polymer provided by *Solvay*	180	-1	0.18	10^5	7.07
Hee Lee *et al*[22]	Pentacene	Poly(4-vinylphenol)	180	-5	---	10^7	1.23
Jang *et al*[32]	Pentacene	Poly(vinyl cinnamate)	110	-2	0.32	10^5	0.25
Petritz *et al*[23]	Pentacene	PNDPE[1]	65	-0.5	0.10	10^4	0.80
Wang *et al*[21]	Pentacene (p type) PDIF-CN_2(n type)[2]	Cinnamate natural carbohydrates	120	-10	---	10^5	0.32
Rim *et al*[24]	IGZO	Al_2O_3	350	0	1.5	10^8	15
Lee *et al*[25]	IGZO	i-PUA[3]	200	-1	0.47	10^7	11.6

1 – poly((±)endo,exo-bicyclo[2.2.1]hept-5-ene-2,3-dicarboxylicacid,diphenylester).

2 - N,N′-1H,1H-perfluorobutyl dicyanoperylenecarbox-ydiimide.

3 - ionic-polyurethane acrylate

4. CONCLUSION

The main objective of this work was to prove that the material provided by *Solvay* has the characteristics to be implemented in an oxide TFTs fabrication process, and that was achieved. However, further optimization of its deposition conditions and integration with other fabrication techniques is still needed.

The films produced during this work were fully cross-linked, with thickness around 260nm for 2000 rpm. As for the films' surface, it was clear that it is affected by acetone exposure, with the RMS value increasing from 0.4109nm to 10.92nm, before and after exposure. The transmittance in the visible range seems to maintain roughly the same value, at around 92%, showing that this material is great for transparent electronics.

The MIM capacitors produced showed a dielectric constant of 8.35, which is closer to the values reported by *Solvay*. They also proved to be stable at high frequencies, with low leakage current. Additional optimizations for the curing process are needed, including placing the samples under nitrogen protection, as suggested by *Solvay*.

The time needed in acetone to develop a pattern with good contrast and remove the polymer from where is supposed to be removed was determined, being 30 minutes for the 260 nm thickness used. EDS measurements also showed this, with Cl, which is in the composition of the film, only being found where the film was meant to be in the pattern. Due to the little traces of F still inside the square, further optimization may be required, to ensure the removal of the film is perfect.

While the number of working top gate TFTs was small due to lithography issues, devices with a W/L=160/160 (μm/μm) showed good results, with a V_{on}= -1V, an on/off ratio of 10^5, μ_{SAT} of 7.07 $cm^2.V^{-1}.s^{-1}$ and a subthreshold swing (SS) of 0.18 V/dec. Hence, the devices obtained do not differ significantly from other typical IGZO TFTs that use oxides patterned by conventional lithography. This showing that a simplification of the device's fabrication does not imply sacrificing its performance. The low current in the remaining transistors of the top gate samples, is due to a high contact resistance between the source and drain contacts and the IGZO semiconductor.

The TFTs produced in bottom gate architecture, all had a very high leakage current, so there was no modulation of current with V_{GS}. A plausible explanation for all the TFTs with this architecture having these problems, is the IGZO sputtering deposition that follows the dielectric, which may be too harmful due to the sputtering energy. The fabrication of all devices underwent lithography and vacuum processes that were adjusted to do the less damage to the dielectric material, however this compromise was a difficult task and sometimes may have resulted in problems for the other TFT layers.

For future optimization, certain problems need to be addressed, such as the development of the pattern. In this work acetone was used, however other developers might be better suited and not damage the films, or at least minimize the damage. As for the patterning of other layers, less damaging techniques should be implemented, for instance always perform dry etching instead of wet etching, as HCl seems to damage the dielectric. The tunning of the sputtering deposition of the top electrodes may also help to minimize the damage to the

dielectric material, and as such several tests should be performed to attempt to find the optimal deposition power for the top metal contacts.

Nevertheless, this material has showed its potential during this work, with solid dielectric properties being achieved in the films produced, and perhaps a different approach on the fabrication techniques used for the TFT can result in devices with even better performances. Solution processes to fabricate the entire TFT might be better suited for this material. To take further advantage of the properties of this material for oxide TFTs, future works should not only optimize the dielectric layer deposition conditions, but also other fabrication conditions used for the metal contacts and IGZO, such as the deposition power. Nevertheless, with the study of the material presented in this work, the way is paved for its implementation on oxide TFTs technology and perhaps other types too.

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Appendix A - MIM capacitors

Figure A. 1- Shadow mask used to fabricate the MIM capacitors. (Area=2.5cm^2)

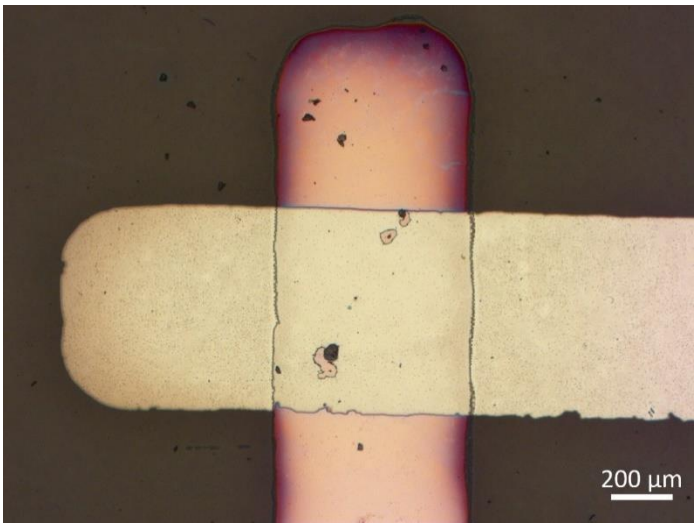

Figure A. 2- Microscope image of a capacitor F in sample II. The top electrode shows the degradation that occurred.

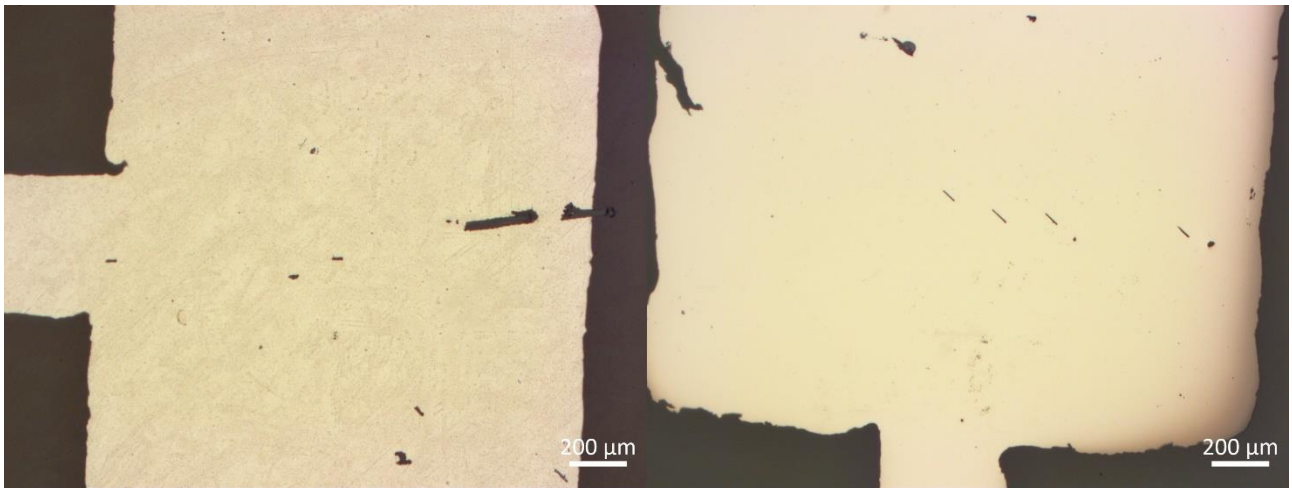

Figure A. 3 - Microscope image of electrodes for capacitor F in sample II. Top electrode (left), bottom electrode (right). The lefts electrode shows the degradation, while the right one is normal.

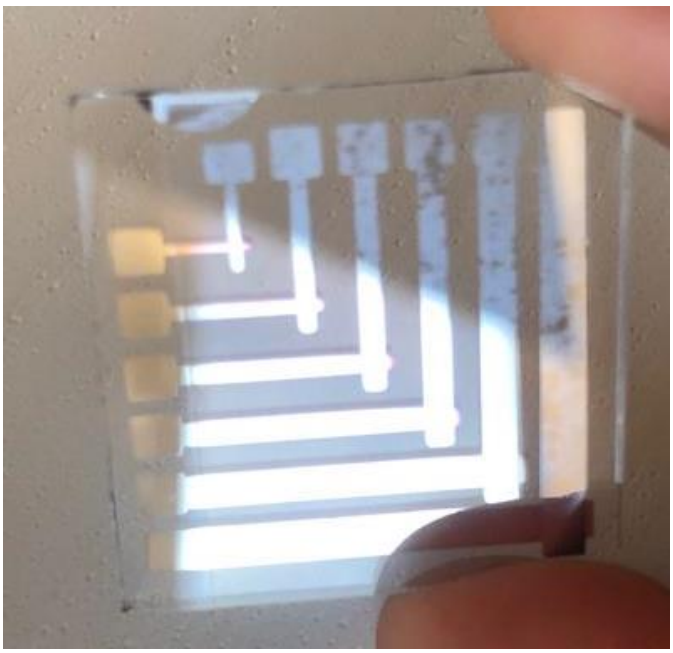

Figure A. 4 - Image of sample II. The top electrodes show the degradation that occurred.

Appendix B - TFTs

Table B. 1 - Architectures and deposition/patterning technique used in the TFTs produced for all samples (dielectric always deposited and patterned in the same manner).

	I-VI	**VII**	**VIII-IX**
Architecture	Bottom gate	Bottom gate (all patterning with shadow masks)	Top gate
Bottom electrode(s)	60 nm of Mo deposited by sputtering and patterned defined by photolithographic process with photoresist (dry etching – SF_6)	Sputtering deposition	60 nm of Mo deposited by sputtering and patterned defined by photolithographic process with photoresist (dry etching – SF_6)
Semiconductor	60 nm of IGZO deposited by sputtering and pattern defined by photolithographic process with photoresist (wet etching -HCl:H_2O 20:1)	Sputtering deposition	Lift-off technique used: Photoresist deposition and patterning followed by IGZO deposition and removal of the unwanted IGZO and photoresist by acetone and IPA immersion
Top electrode(s)	60 nm of Mo deposited by sputtering and patterned defined by photolithographic process with photoresist (dry etching – SF_6)	Sputtering deposition	60 nm of Mo deposited by sputtering and patterned defined by photolithographic process with photoresist (wet etching -HCl:H_2O 20:1)

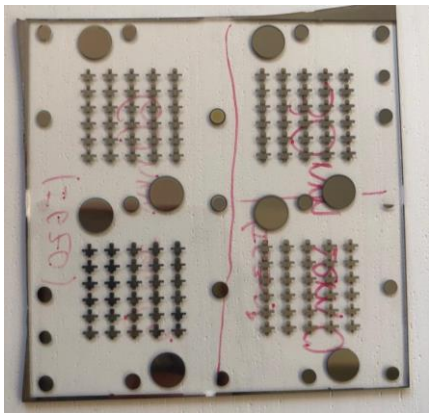

Figure B. 1 - Sample VII (Bottom gate TFTs patterned by shadow masks).

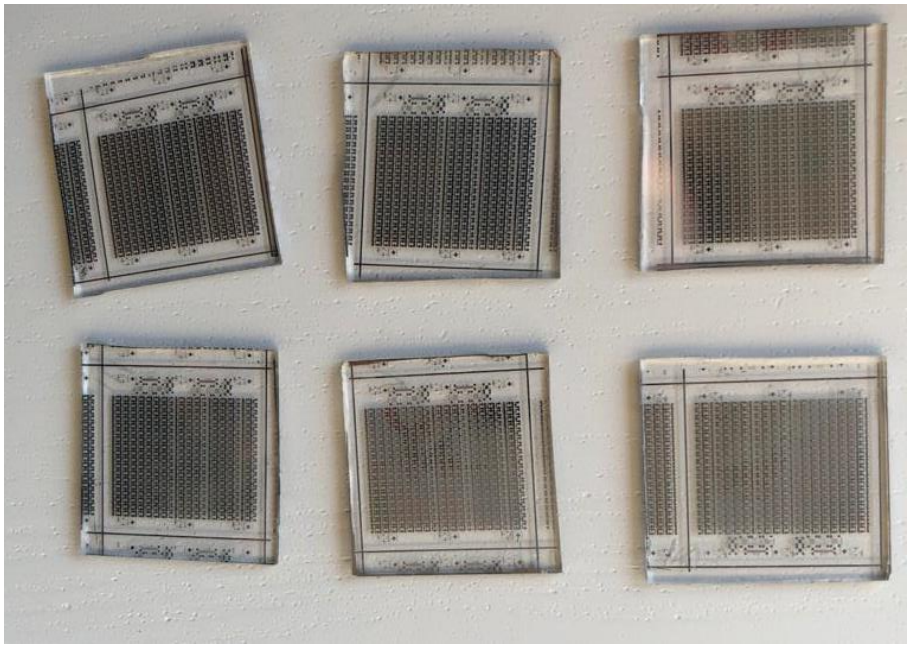

Figure B. 2 - Samples I-VI (Bottom gate TFTs patterned by conventional lithography).

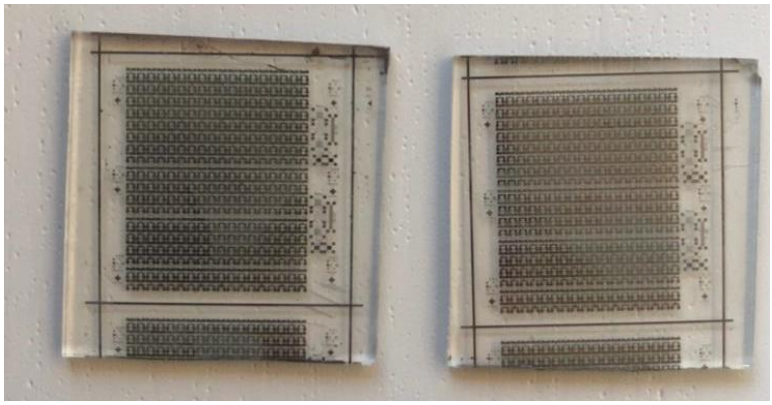

Figure B. 3 - Samples VIII and IX (Top gate TFTs patterned by conventional lithography).

ANTÓNIO PASSOS DIAS AGUIAR MOTA

UM TÍTULO DE TESE LONGO E IMPRESSIONANTE
COM UMA MUDANÇA DE LINHA FORÇADA

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