View metadata, citation and similar papers at core.ac.uk

brought to you by CORE

provided by Archivio istituzionale della ricerca - Università degli Studi di Udine

Electronics **2015**, *4*, 969-978; doi:10.3390/electronics4040969

OPEN ACCESS

electronics

ISSN 2079-9292

www.mdpi.com/journal/electronics

Article

Electrical Compact Modeling of Graphene Base Transistors

Sébastien Frégonèse [1,*], Stefano Venica [2], Francesco Driussi [2] and Thomas Zimmer [1]

[1] CNRS and University of Bordeaux, IMS UMR 5218, Talence 33400, France;
E-Mail: thomas.zimmer@ims-bordeaux.fr

[2] DIEGM—University of Udine via delle Scienze, 208 22100 Udine, Italy;
E-Mails: stevenica@alice.it (S.V.); francesco.driussi@uniud.it (F.D.)

* Author to whom correspondence should be addressed;
E-Mail: sebastien.fregonese@ims-bordeaux.fr; Tel.: +33-05-4000-2800; Fax: +33-05-5637-1545

Academic Editor: Frank Schwierz

Received: 30 July 2015 / Accepted: 2 November 2015 / Published: 18 November 2015

Abstract: Following the recent development of the Graphene Base Transistor (GBT), a new electrical compact model for GBT devices is proposed. The transistor model includes the quantum capacitance model to obtain a self-consistent base potential. It also uses a versatile transfer current equation to be compatible with the different possible GBT configurations and it account for high injection conditions thanks to a transit time based charge model. Finally, the developed large signal model has been implemented in Verilog-A code and can be used for simulation in a standard circuit design environment such as Cadence or ADS. This model has been verified using advanced numerical simulation.

Keywords: graphene; transistor; GBT; circuit; compact; SPICE; electrical; model; large signal

1. Introduction

The physical properties of graphene are of highest interest for electronic applications and its properties have been used by several research groups to develop radio frequency (RF) and microwave Graphene Field Effect Transistors (GFET) [1–3]. Unfortunately, the lack of energy bandgap in graphene induces poor DC electrical characteristics and GFETs are still under evaluation [4] and optimization. Also, new transistor concepts are explored such as the Graphene Barristor [5] or the hot electron graphene base transistor (GBT) [6,7]. As explained by the inventors [7], compared to the GFET where

the carrier transport is within the plane of the graphene sheet, "*the GBT is based on a vertical arrangement of emitter (E), base (B), and collector (C), just like a hot electron transistor or a vacuum triode*". This vertical stack considers an emitter-base and a base-collector energy barrier that are controlled by the graphene base and the collector potentials. In the off-state, the carriers face a large barrier potential, while, in the on-state, this barrier vanishes when a sufficient positive bias is applied to the base and collector. The transistor concept has been demonstrated in [7] and it is under optimization to improve the GBT electrical performance [8].

Venica *et al.* and Driussi *et al.* [9,10] have developed physics based device simulators with different level of accuracy in order to improve the understanding of the GBT operation, and to optimize the transistor as a single element [11]. A small signal model has been proposed in [6]. In order to evaluate this transistor in circuit configuration, a large signal compact model is necessary.

In this paper, we propose a large signal compact model, whose verification is done by means of comparison with numerical simulation [9,11]. The paper is organized in two parts: the developed transistor compact model is described in the first part; then the second part compares compact model results to numerical simulation data.

2. Compact Model

The GBT transistor structure is presented in Figure 1. The vertical stack comprises the emitter, the emitter-base region EBi, the graphene base, the base-collector region BCi and the collector. The barrier potential height of the EBi and BCi regions controls the carrier transport mode such as tunneling or thermionic transport. Hence, the choice of the material used for the EBi and BCi region is of major importance. EBi and BCi can be either an insulator material such as SiO_2 or high-k dielectrics to exploit a tunneling transport [6] or a semiconductor such as Ge or Si to foster a thermionic current [12].

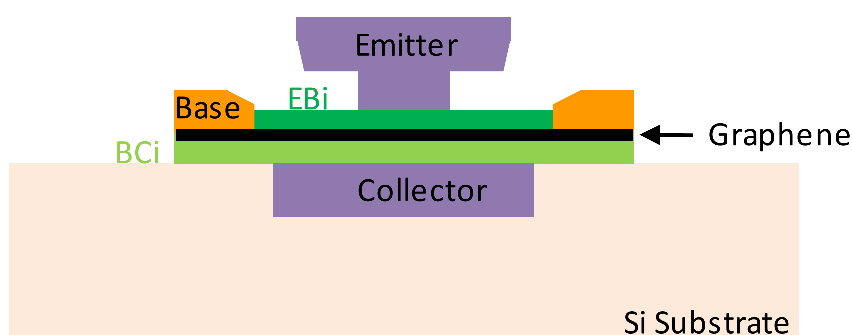

Figure 1. Schematic representation of the transistor structure.

According to the transistor structure (see Figure 1), the following equivalent circuit is proposed (see Figure 2). The extrinsic circuit is composed of three access resistances R_B, R_C, R_E. Concerning the intrinsic part, the core of the model is based on the self-consistent calculation of the internal base potential V_{Bi}, which is a function of the charge in the emitter, the collector and within the graphene layer. These charges are modeled through different capacitances. First, C_Q capacitance models the quantum capacitance of the graphene layer, while C_{BE0} and C_{BC0} describe the EBi and BCi capacitances, respectively. Finally, C_{DC} and C_{DE} are diffusion capacitances that take into account the additional charge

due to carrier transport in the EBi and BCi regions. These capacitances are of interest for medium to high injection conditions [9]. Finally, two diodes I_{BE} and I_{BC} are modeling the base-emitter and base-collector current, respectively, and one voltage controlled current source I_{CE} is introduced for the collector-emitter transfer current. Each element is described in the next section.

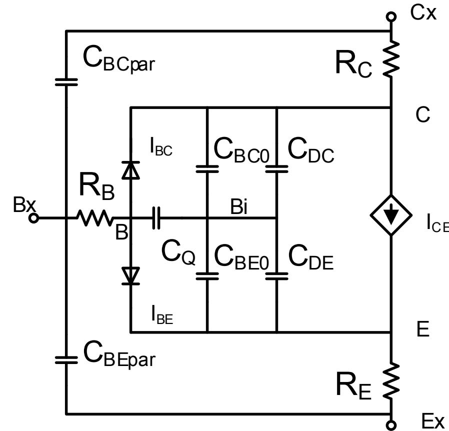

Figure 2. Equivalent circuit of the Graphene Base Transistor (GBT) electrical compact model.

2.1. Self-Consistent Calculation of the Internal Base Potential

The charge in the graphene layer can be computed by combining the specific density of states of graphene with the Fermi approach for the carrier distribution. Assuming that the potential drop into the graphene base $|V_{BBi}| \gg kT/q$ (k is the Boltzmann constant, T is the absolute temperature and q is the elementary charge), the total charge density can be approximated as follows [13]:

$$Q_G \approx q\left(-\frac{q^2}{\pi\left(\hbar v_f\right)^2}|V_{BBi}|V_{BBi}\right) = \frac{1}{2}C_Q V_{BBi} \tag{1}$$

with $\hbar$ the reduced Planck constant, v_f the Fermi velocity and $C_Q = \kappa|V_{BBi}|$, $\kappa = -2\frac{q^2}{\pi\left(\hbar v_f\right)^2}$.

Introducing the graphene charge in the equivalent circuit, the internal base potential can be calculated by solving the following equation:

$$Q_G + C_{BC}V_{BiC} + C_{BE}V_{BiE} = 0 \tag{2}$$

where $V_{BiC} = V_{Bi} - V_C$, $V_{BiE} = V_{Bi} - V_E$, $C_{BC} = C_{BC0} + C_{DC}$, $C_{BE} = C_{BE0} + C_{DE}$ (see Figure 2) and $C_{BC0} = \frac{\varepsilon_{BC} A_E}{e_{BC}}$, $C_{BE0} = \frac{\varepsilon_{BE} A_E}{e_{BE}}$ are the oxide capacitances. e_{BC} and e_{BE} are the insulator thicknesses of *EBi* and *BCi* regions, respectively, and ε_{BE} and ε_{BC} are the associated permittivity. A_E is the emitter area. The diffusion capacitances C_{DE} and C_{DC} will be described in Section II-C.

Substituting Equation (1) in Equation (2), the V_{BBi} potential is introduced in the equation:

$$\frac{1}{2}\kappa|V_{BBi}|V_{BBi} + C_{BC}\left(-V_{BBi} + V_{BC}\right) + C_{BE}\left(-V_{BBi} + V_{BE}\right) = 0 \tag{3}$$

Equation (3) is a second order polynomial that can be solved and gives the following solution [6]:

$$V_{BBi} = \frac{-(C_{BC} + C_{BE}) + \sqrt{(C_{BC} + C_{BE})^2 \mp 2\kappa(C_{BC}V_{BC} + C_{BE}V_{BE})}}{\pm\kappa} \quad (4)$$

2.1.1. Description of Diodes and Transfer Current Source

As described above, the EBi and BCi material can be either insulator or semiconductor and the charge transport can be dominated by tunneling emission or thermionic transport. In order to obtain a versatile compact model, the diode and transfer current source equations will be based on flexible and simple relationships.

For the base-emitter and base-collector tunnel or semiconductor-graphene diodes, an exponential equation is used (see [14]) and modified to gain in adaptability:

$$I_{BE} = A_E J_{SBE} \exp\left(\frac{V_{BiE} - \phi_{BE}}{B_{BE}}\right) \quad (5)$$

$$I_{BC} = A_E J_{SBC} \exp\left(\frac{V_{BiC} - \phi_{BC}}{B_{BC}}\right) \quad (6)$$

where J_{SBE} and J_{SBC} are the corresponding saturation currents, ϕ_{BE} and ϕ_{BC} are the barrier heights and B_{BE} and B_{BC} are fitting parameters of the slope of the exponential function.

For the transfer current source, a modified Landauer based equation is used [15].

$$I_{CE} = A_E J_{SF} \begin{bmatrix} \ln\left(1 + \exp\left(\frac{V_{BiE} - \phi_{BE}}{B_{BE}}\right)\right) \\ -\ln\left(1 + \exp\left(\frac{V_{BiC} - \phi_{BC}}{B_{BC}}\right)\right) \end{bmatrix} \times f_{CE}$$

$$f_{CE} = \begin{cases} 0 \; if \; V_{CE} < \phi_{CE} \\ 1 \; if \; V_{CE} > \phi_{CE} \end{cases} \quad (7)$$

J_{SF} is a saturation current and the f_{CE} parameter allows zeroing the current if the collector-emitter barrier ϕ_{CE} is too high to be crossed by the carrier at low V_{CE}. ϕ_{CE} is used as a fitting parameter for the low V_{CE} bias regime.

2.1.2. Medium to High Current Injection Effects

At medium to high current conditions, the charge injected through the transfer current in the EBi and BCi junctions needs to be taken into account. This charge will modify the charge equilibrium in the intrinsic transistor and will induce a shift of the internal base potential. Hence, as suggested in Figure 2, diffusion capacitances are included in the equivalent circuit and this will affect the potential drop V_{BBi} through the Equation (4).

The diffusion charge within the two regions is computed by considering a transit time approach. At medium injection level, the charge can be approximated by

$$Q_{DC} = \tau_{CB} I_{CE} \, , \; Q_{DE} = \tau_{EB} I_{CE} \quad (8)$$

τ_{CB}, τ_{EB} are the transit times of the BCi and EBi region at medium injection, respectively. At high injection, an additional charge ΔQ_K [9,12], with respect to Q_{DE} appears when the transfer current I_{CE} overpass the critical current I_{CK}:

$$\Delta Q_K = \Delta\tau_K \left(\frac{I_{CE}}{I_{CK}}\right)^{\gamma} I_{CE} \tag{9}$$

$\Delta\tau_K$ is the additive transit time at high injection and γ is a fitting parameter.

Combining Equations (8) and (9) and deriving the equation, the related capacitance can be deduced:

$$C_{DC} = \frac{dQ_{DC}}{dV_{CE}}, \quad C_{DE} = \frac{d\left(Q_{DE} + Q_K\right)}{dV_{BiE}} \tag{10}$$

These elements can be either derived analytically or directly computed using a derivative function in Verilog language.

2.2. Comparison to Numerical Simulation

In order to validate our model and to demonstrate its physical basis, a comparison between physics-based numerical simulations and our compact model is provided. The 1-D numerical model of [9] solves the electrostatics of the GBT self-consistently with the calculated tunneling current and estimates the transit frequency f_T. Concerning the currents, since the physical origin of the base current is still unclear and debated [7,16], a perfectly transparent graphene layer is assumed and the base current is neglected. Hence, we assume a priori that the collector current is the current due to electrons injected from the emitter and, consistently, crossing the whole device.

The simulated device assumes that the EBi and BCi layers are made of two insulators [11]: the EBi region has a 2 nm high permittivity insulator (ε_r = 25) while the BCi region has a 12 nm oxide with ε_r = 2.5. Only the intrinsic device is simulated and one would need to consider parasitic elements to have a realistic circuit simulation.

First, a comparison between numerical simulations and compact model simulations of the calculated graphene base charge is provided in Figure 3. Despite a deviation at large I_{CE} mainly due to different modeling approaches for the high injection effects (model in [9] solves the potential along the device self-consistently with the traveling electrons), a fairly good agreement is found between the two models. This verifies the adequate calculation of the intrinsic base potential V_{Bi} by the compact model (see Figure 4).

The transfer characteristics of the device are simulated in Figure 5. At low injection condition, a similar behavior is observed despite a small disagreement. A good agreement is observed at medium to high electron injection levels. Figure 6, instead, shows the associated transconductance, which is of major importance for RF circuit simulation. A very good agreement is observed for low and medium bias, a reasonable agreement can be found for high bias. Finally, Figure 7 compares the output curves confirming a good matching between the two models. It should be underlined that the slope g_{CE} (see Figure 8) is properly modeled; this is mandatory to correctly model the voltage gain of an amplifier circuit.

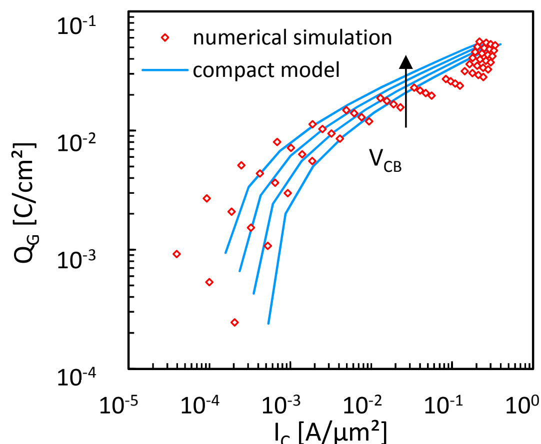

Figure 3. Charge Q_G *versus* I_{CE} curves for different V_{CB} (2, 3, 4, 5 V), numerical simulation and compact model simulation.

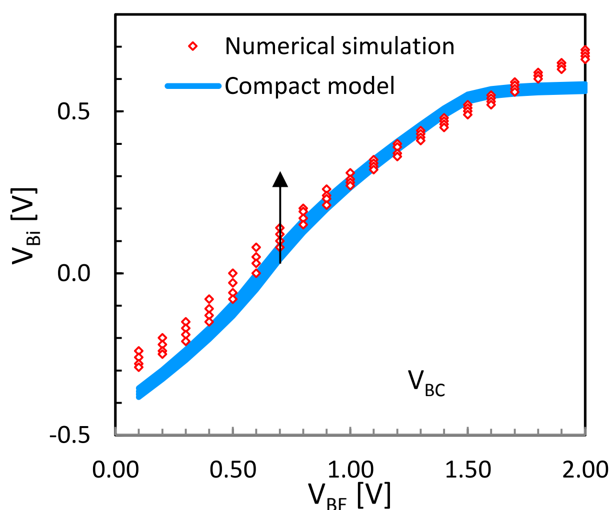

Figure 4. Graphene Fermi potential *versus* V_{BE} curves for different V_{CB} (2, 3, 4, 5 V), numerical simulation and compact model simulation.

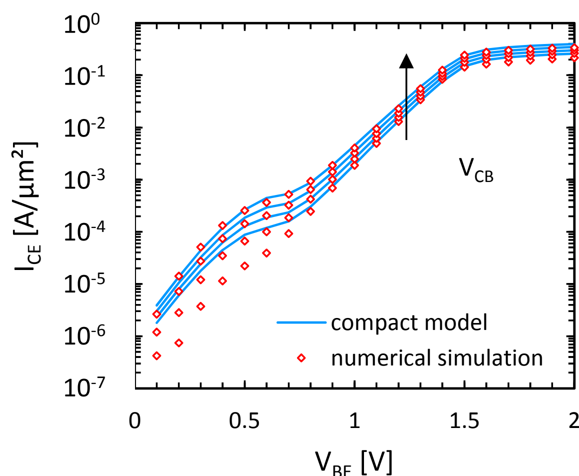

Figure 5. I_{CE} *versus* V_{BE} curves for different V_{CB} values (2, 3, 4, 5 V) simulated with the numerical model and the compact model.

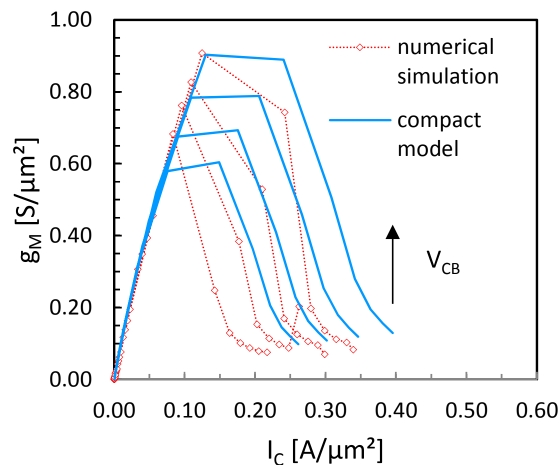

Figure 6. g_M *versus* I_C curves for different V_{CB} (2, 3, 4, 5 V) simulated with the numerical model and the compact model.

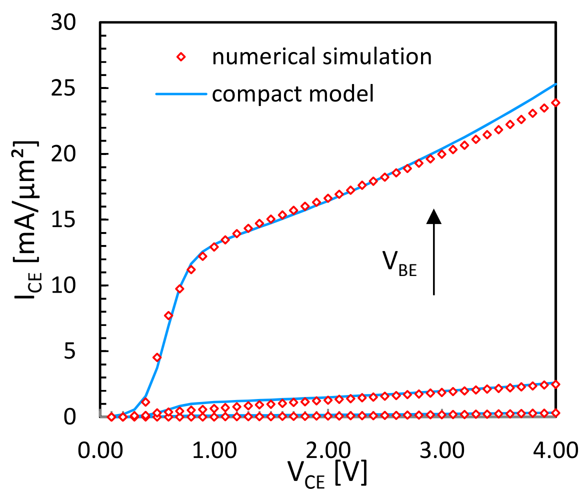

Figure 7. I_{CE} *versus* V_{CE} curves for different V_{BE} values (0.75, 1, 1.25 V), numerical simulation and compact model simulation.

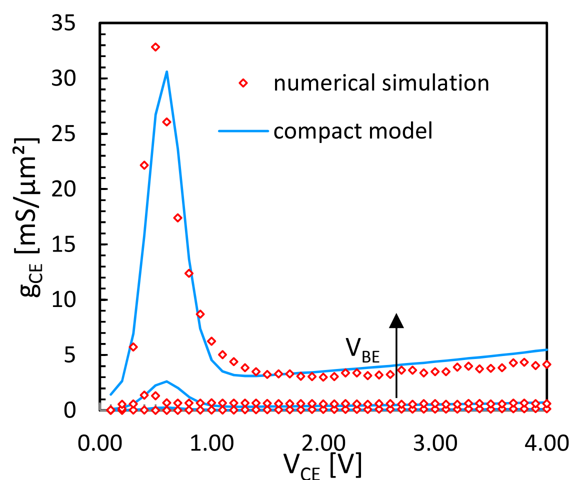

Figure 8. g_{CE} *versus* V_{CE} curves for different V_{BE} values (0.75, 1, 1.25 V), numerical simulation and compact model simulation.

In addition, *S* parameter simulations have been performed to extract the transit frequency; f_T is then compared to numerical simulation results (see Figure 9). A good agreement is observed up to peak f_T, which is the optimum bias condition for circuit applications. At higher current levels, a deviation is observed. Again this can be due to the different modeling strategies adopted to model the high current effects in the GBT.

Table 1 summarizes the used compact model parameters. e_{BC}, e_{BE}, ε_{BE} and ε_{BC} are those used in the physics based simulations, while the others have been extracted by fitting in Figures 3–8.

Table 1. Parameters used in the compact model simulation.

Parameter Name/Unit	Parameter Value
J_{SF} (mA/μm²)	437
B_{BE} (mV)	35.3
B_{BC} (mV)	94.2
Φ_{CE} (V)	0.57
e_{BE} (nm)	2
e_{BC} (nm)	12
ε_{BE}	25
ε_{BC}	2.5
τ_{BE} (fs)	0.35
τ_{BC} (fs)	6
Φ_{BE} (V)	0.893
Φ_{BC} (V)	1.2
γ	1.55
κ (μF/cm²)	25
I_{CK} (A/μm²)	0.7
$\Delta\tau_K$ (fs)	8×10^{-3}

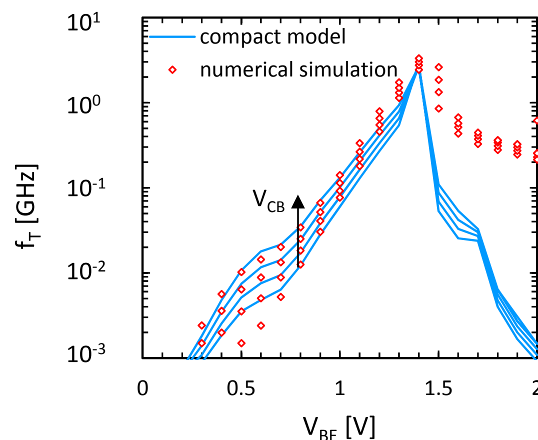

Figure 9. f_T *versus* V_{BE} curves for different V_{CB} (2, 3, 4, 5 V), numerical simulation and compact model simulation.

3. Conclusions

We have developed a compact large signal model for GBT devices. Our model represents a good trade-off in terms of physics soundness and implementation complexity. Its accuracy relies on a

self-consistent base potential calculation and a physics based charge model associated with an empirical and versatile transfer current equation. The model has been directly implemented in Verilog-A code. Hence, this model can be used to predict circuit performances based on GBT devices. Finally, the compact model accuracy has been verified by comparison with a physics-based electrical model, showing a good agreement with the numerical simulations.

Acknowledgments

This work is part of the GRADE project (317839) supported by the European Commission through the Seventh Framework Program for Research and Technological Development. The authors thank P. Palestri for fruitful discussions.

Author Contributions

S.F. and T.Z. developed the compact model equations. S.V., F.D. developed and performed the physics based simulations. All authors discussed the data and interpretation, and contributed during the writing of the manuscript. All authors have given approval to the final version of the manuscript.

Conflicts of Interest

The authors declare no conflict of interest.

References

1. Lin, Y.-M.; Farmer, D.B.; Jenkins, K.A.; Wu, Y.; Tedesco, J.; Myers-Ward, R.; Eddy, C.; Gaskill, D.; Dimitrakopoulos, C.; Avouris, P. Enhanced Performance in Epitaxial Graphene FETs with Optimized Channel Morphology. *Electron. Device Lett. IEEE* **2011**, *32*, 1343–1345.
2. Wu, Y.Q.; Farmer, D.B.; Valdes-Garcia, A.; Zhu, W.J. Record High RF Performance for Epitaxial Graphene Transistors. In Proceedings of the IEEE International on Electron Devices Meeting (IEDM), Washington, DC, USA, 5–7 December 2011.
3. Liao, L.; Lin, Y.; Bao, M.; Cheng, R.; Bai, J.; Liu, Y.; Qu, Y.; Wang, K.L.; Huang, Y.; Duan, X.; *et al*. High-speed graphene transistors with a self-aligned nanowire gate. *Nature* **2010**, *467*, 305–308.
4. Schwierz, F. Graphene Transistors: Status, Prospects, and Problems. In Proceedings of the IEEE, Ilmenau, Germany, 22 May 2013; Volume 101, pp. 1567–1584.
5. Yang, H.; Heo, J.S.; Park, S.; Song, H.J.; Seo, D.H.; Byun, K.-E.; Kim, P.; Yoo1, K.; Chung, H.-J.; Kim, K. Graphene Barristor, a Triode Device with a Gate-Controlled Schottky Barrier. *Science* **2012**, *336*, 1140–1143.
6. Mehr, W.; Abrowski, J.; Scheytt, C.; Lippert, G.; Xie, Y.-H.; Lemme, M.C.; Ostling, M.; Lupina, G. Vertical graphene base transistor. *IEEE Electron Device Lett.* **2012**, *33*, 691–693.
7. Vaziri, S.; Lupina, G.; Henke, C.; Smith, A.D.; Östling, M.; Dabrowski, J.; Lippert, G.; Mehr, W.; Lemme, M.C. A Graphene-Based Hot Electron Transistor. *Nano Lett.* **2013**, *13*, 1435–1439.
8. Vaziri, S.; Belete, M.; Litta, E.D.; Smith, A.D.; Lupina, G.; Lemme, M.; Östling, M. Bilayer Insulator Tunnel Barriers for Graphene-Based Vertical Hot-electron Transistors. *Nanoscale* **2015**, *7*, 13096–13104.

9. Venica, S.; Driussi, F.; Palestri, P.; Esseni, D.; Vaziri, S.; Selmi, L. Simulation Of DC and RF performance of the graphene base transistor. *IEEE Trans. Electron Devices* **2014**, *61*, 2570–2576.
10. Driussi, F.; Palestri, P.; Selmi, L. Modelling, simulation and design of the vertical Graphene Base Transistor. *Microelectron. Eng.* **2013**, *109*, 338–341.
11. Venica, S.; Driussi, F.; Palestri, P.; Selmi, L. Graphene Base Transistors with optimized emitter and dielectrics. In Proceedings of the Microelectronics, Electronics and Electronic Technology Conference, Opatija, Croatia, 26–30 May 2014; pp. 39–44.
12. Di Lecce, V.; Grassi, R.; Gnudi, A.; Gnani, E.; Reggiani, S.; Baccarani, G. Graphene-base heterojunction transistor: An attractive device for terahertz operation. *IEEE Trans. Electron Devices* **2013**, *60*, 4263–4268.
13. Xu, H.; Zhang, Z.; Peng, L.-M. Measurements and microscopic model of quantum capacitance in graphene. *Appl. Phys. Lett.* **2011**, *98*, 1–3.
14. Vaziri, S.; Belete, M.; Litta, E.D.; Smith, A.D.; Lupina, G.; Lemme, M.C.; Östlinga, M. Bilayer insulator tunnel barriers for graphene-based vertical hot-electron transistors. *Nanoscale* **2015**, *7*, 13096–13104.
15. Ferry, D.K.; Goodnick, S.M. *Transport in Nanostructures*; Cambridge University Press: Cambridge, UK, 1997.
16. Zeng, C.; Song, E.B.; Wang, M.; Lee, S.; Torres, C.M.; Tang, J.; Weiller, B.H.; Wang, K.L. Vertical graphene-base hot-electron transistor. *Nano Lett.* **2013**, *13*, 1435–1439.

© 2015 by the authors; licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution license (http://creativecommons.org/licenses/by/4.0/).