10-Bit 200 kHz/8-Channel Incremental ADC for Biosensor Applications

Journal of Circuits, Systems, and Computers

World Scientific
www.worldscientific.com

10-Bit 200 kHz/8-Channel Incremental ADC for Biosensor Applications*

Priya Gupta†

School of Engineering, University of Edinburgh, King's Building
Edinburgh EH9 3FF, UK,
priya.gupta@ed.ac.uk

Aruj Earnest

School of Engineering, University of Edinburgh, King's Building
Edinburgh EH9 3FF, UK,
e.aruj@sms.ed.ac.uk

Srinjoy Mitra

School of Engineering, University of Edinburgh, King's Building
Edinburgh EH9 3FF, UK,
srinjoy.mitra@ed.ac.uk

Received (Day Month Year)
Revised (Day Month Year)
Accepted (Day Month Year)

In this paper, a 2nd order Discrete-time (DT) modulator for 8-channel Incremental Sigma-Delta analog-to-digital (IADC) is presented for biomedical applications ranging from kHz. The proposed DT modulator with input bandwidth of 25 kHz on each channel is sampled at 51.2 MHz, with oversampling ratio of 128 implemented at 180nm technology. The proposed IADC has high-resolution, multichannel A/D conversion, simple architecture, low offset, low gain error and low area over the standard ADCs suitable. Measured results show that the SNR, DR, ENOB, power consumption and chip area of proposed IADC are 63.9 dB, 62.2 dB, 10.11 bits, 0.832 mW, and 0.032 mm^2 respectively at 1.8V power supply. For testing purpose, the non-coherent sampling is done to get the FFT plot of the output signal. For further validation, the proposed 2nd order IADC was also designed and compared in MATLAB/Simulink.

Keywords: Incremental-ADC, Sigma-Delta Modulator, OTA, SINC-filter

1. Introduction

In the past decade, there has been enormous progress in the development of multi-channel neural recording systems on a single chip [1]. These chips need to be small and to be fitted

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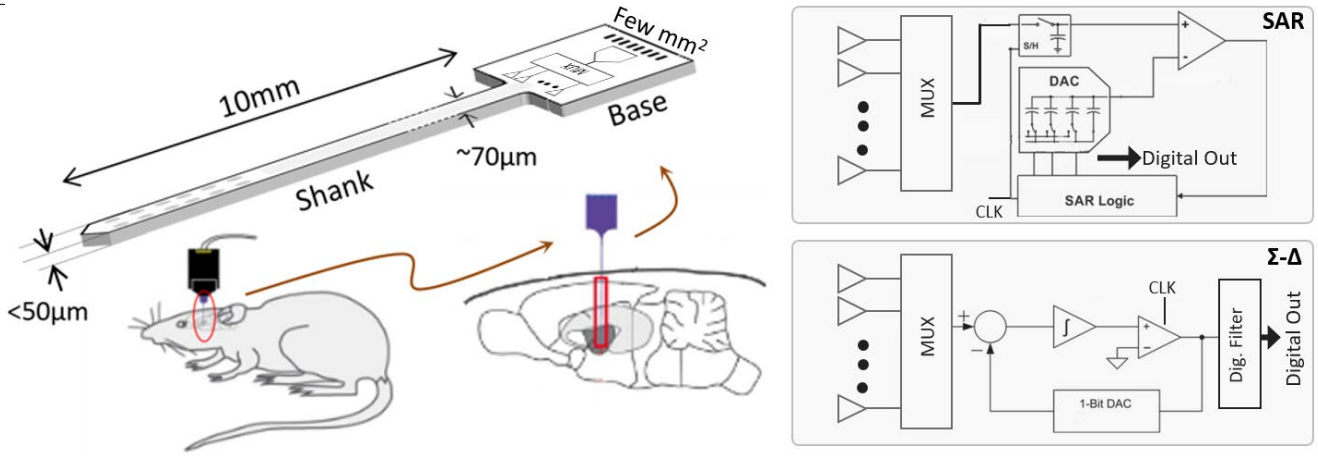


Fig. 1. Neural probes (left) implanted on an animal brain not only need to have a thin, narrow shank, but they should also have a very small base area. This is necessary for implanting multiple probes in the brain of a freely moving animal. ADCs (mostly SAR) are still one of the largest components in the base. Sigma-delta ADCs with much fewer analog blocks and matching components could be fitted in a smaller area.

on the head-stage of a freely-moving small animal (usually a mice or a rat). In such systems, analog-to-digital converter (ADC) is an important building block whose area has an impact on the entire system performance [2]. The general trend is to multiplex a large number of recording channels onto a single ADC, usually like a SAR-ADC [4][5]. Since SAR ADCs have a significant number of analog blocks and matched capacitors, their area cannot be easily reduced even while using advanced technology nodes (Fig. 1, inset).

With the number of recording channels moving towards tens of thousands, there is an essential requirement to have more compact and scalable ADCs to build a usable neural probe. Oversampled ADCs have a significant reduction of analog front-end circuit complexity and are ideal module to integrate into probes for advanced technology [6]. Unfortunately, traditional ΣΔ ADCs are not well suited for multiplexed systems where one-to-one mapping between input and output samples are required. To process the multiplexed signals, Incremental ΣΔ ADCs (IADC) are the best choice as it resets the modulator and digital filters after each conversion [7]. After each reset, IADC gives the conversion result and switches to next channel. In this way, single IADC can be used for multiple channels with benefits like high accuracy, low offset, low gain error and low area over the standard ADCs [8]. This paper shows a design methodology of a complete IADC for eight multiplexing channel. IADCs consist of an analog modulator followed by a digital low pass filter like conventional ΣΔ ADCs expect, it resets after each M number of cycles at the higher oversampling-ratio (OSR) of M [9]. In this proposed IADC circuity, the analogue modulator consists of an integrator, comparator and one-bit digital-to-analog convertor (DAC). The analogue modulator in IADC can be realized both using continuous-time (CT) and discrete-time (DT) loop filters. CT loop filters (modulators) are modelled in s domain as 1/sTs (where Ts is the time period of the sampling clock) and it employs continuous time circuits, often implemented by active RC, gm-C, or MOSFET-C based loop filters. CT modulators have better noise immunity due to their inherent anti-aliasing properties, relaxed amplifier unity-gain bandwidth requirements which are commonly used for high-speed applications[10][11].

Despite the above-mentioned advantages, the CT modulator is rarely used in biomedical applications as it processes each input in a continuous fashion, which causes non-idealities such as excess loop delay, clock jitter etc., which affects the overall performance of IADC.

Whereas, DT modulators have received much attention for neural recording system-based applications which is the main objective of this paper. The DT modulators are implemented using Switched Capacitor (SC) techniques based on charge transfer from sampling to integrating capacitors, modelled by z domain transfer function as $z^{-1}/(1-z^{-1})$.
In the proposed IADC, DT modulator has been implemented using SC technique in which resistance values are defined by capacitor and sampling clock period. They have got relatively high linearity and good clock jitter tolerance [12][13]. However, DT modulators are susceptible to settling problems in SC integrators caused by the non-idealities of the Operational Transconductance Amplifier (OTA) [4] and many topologies have already been proposed to improve the performance parameters of the OTA.
The first-order modulator achieves high resolution, but at the cost of very long conversion time, thus resulting in poor power-efficiency [15]. Several papers based on multi-bit IADCs, hybrid IADCs (which combines conventional ΣΔ ADCs with a Nyquist ADC) such as extended counting (EC) IADCs, Dual slope IADC, two-step IADC, and zoom IADC etc. have been presented [16][17]. On the other hand, increasing the modulator order more than two can bring other problems like modulator loop instability as each integrator adds further loop delay and degrades the phase margins of amplifiers (basic third order modulator (MOD3) is unstable and hence complete IADC is unstable)[16][17[18][19]. Single-loop modulator designs offer good tolerance to errors such as finite dc integrator gain and small gain matching errors in the signal path. However, they can be difficult to stabilise due to having long chains of integrators in the noise transfer function (NTF) path, and may not give an aggressive noise shaping in the signal passband.

To overcome the stability issue, multi-bit quantisation is been used which brings many advantages such as reduced in-band noise owing to a smaller quantisation step. Thus improving quantizer gain and hence NTF stability, allowing more aggressive NTF designs for lower passband noise and wider stable input range. However, a major problem with adding multi-bit feedback paths is that even slight nonlinearity in the DAC feedback path (e.g. due to random component variations) to the first integrator can have disastrous consequences for the modulator performance [21][22].
In this paper, 2nd order DT modulator for IADC has been designed and implemented at 180nm technology for bio-medical applications. The 8-channel IADC has been designed and tested by using proposed modulator, which operates at 25 kHz input bandwidth per channel and was sampled at 51.2 MHz with oversampling ratio of 128. The proposed architecture of the modulator has high-resolution and, multichannel A/D capability.

2. System Design

2.1. Incremental Converter design Architecture's and their performance parameter

As illustrated in Fig. 2, the IADC consists of a proposed ΣΔ modulator and a digital decimation filter. The ΣΔ modulator quantizes the analogue input signal and the digital decimation filter simultaneously provides the converted output digital bit streams. After each reset, the IADC gives the conversion result and switches to next channel. The final

output data bits rate is down-sampled to the Nyquist rate due to the down-sampler used in digital decimation filter. The relation between OSR and the duty cycle of the reset (DCR) pulse can be expressed by Eq. 1 as follows [2]:

$$OSR = \frac{F_S}{2.F_B} x\ DCR \qquad (1)$$

Where F_s and F_b are the oversampling and input base frequencies, respectively. This equation shows that the OSR can be adjusted by DCR. The resolution of an IADC (for an N-level quantizer and Lth-order modulator) is given by Eq. 2 as follows [23]:

$$n_{bit} = 6.02log_2\left(\alpha(N-1)\frac{(OSR+L-1)!}{L!(OSR-1)!} + 1\right) + 1.76\ \text{dB} \qquad (2)$$

where α is the quantizer overload level factor, and is usually less than one. It is clear that the resolution is determined by OSR, and for a specific OSR, the value of DCR can be set based on relation (1).

The SQNR of the IADC for Lth-order modulator is given by following Eq. 3:

$$SQNR = 10log_{10}(\frac{15L^2OSR^5}{2\pi^4}) \qquad (3)$$

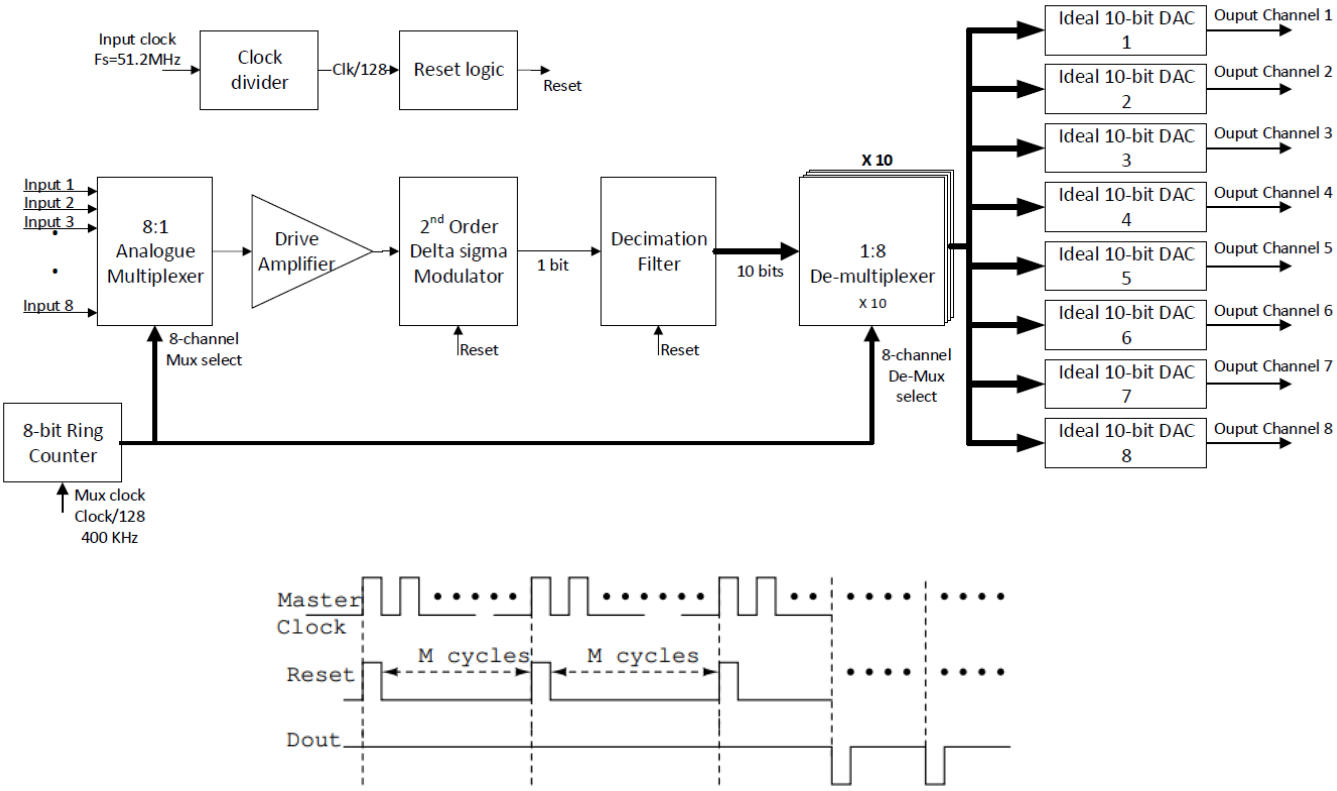


Fig. 2. IADC architectural block diagram

The number of cascaded integrators determines the order of the IADC modulator. For example, the L^{th} order IADC modulator will have L number of cascaded integrators and its output is given by Eq. 4.

$$X(z) = Y(z)z^{-1} + (1 - z^{-1})^{L}Q(z) \quad (4)$$

Where X(z), Y(z) and Q(z) are the z-transforms of the modulator input, output and the quantization error respectively. The output is just a delayed version of the signal plus quantization noise that has been shaped by an L^{th} order Z-domain differentiator or high-pass filter. The multiplication factor of Y(z) is called the signal transfer function (STF)and of Q(z) called the noise transfer function (NTF). From the above equation, higher order modulators push more noise power outside the signal band [24].

The proposed 2^{nd} order modulator architecture is based on Cascade of integrator with Feed-Forward (CIFF) topology, Hence it has L =2, resonator coefficients have zero value (g= 0). Table 1 shows the parametric data used to implements proposed 2^{nd} order DT modulator for IADC.

Table: 1 System Specifications for IADC

Name	**Value**
Modulator Order (L)	2
Effective number of bits (N)	>10 bits
Power	<1mW
Input signal bandwidth (F_b)	100 Hz-200 kHz
Supply Voltage	1.8V
Area	>mm^2
Number of Channels	>10
Applications	Biomedical

2.2. Design steps for proposed 2^{nd} Order DT Modulator for IADC

Signal to noise ratio (SNR) is one of the most crucial parameters for IADC design, therefore to meet target SNR, the first step to design proposed modulator circuit is to ensure the required capacitors sizing and basic amplifier parameters. In this paper, 2^{nd} order DT modulator architecture is selected, the design can proceed in following points

- Sizing capacitors to ensure that system kT/C noise is low enough to meet the modulator overall noise requirements/SNR specifications.
- Sizing switches to ensure that capacitors charge fully during each clock cycle.
- Setting basic amplifier parameters to meet the noise and charging accuracy (settling error) targets.

Fig. 3 shows design flow chart to find out the capacitors sizing for proposed 2^{nd} order DT modulator for IADC in MATLAB.

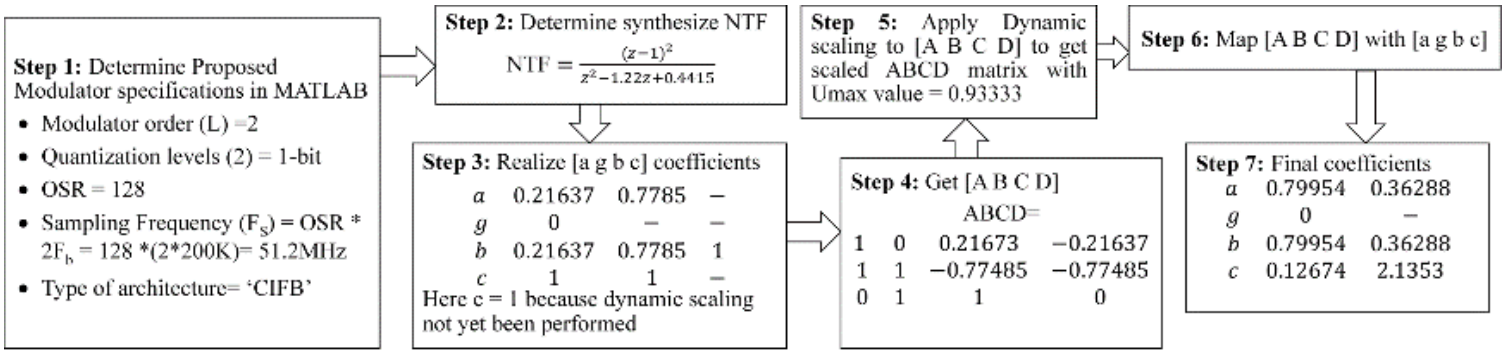


Fig. 3. Flow chart for IADC in MATLAB

Where, a= feedback coefficient from quantizer to integrators, b= feedforward coefficient from input to the integrators, c = forward path coefficients between integrator, g = resonator coefficients for finite NTF zeros.

These [a b g c] coefficients are used to suppress the noise at the specified frequency band for the proposed 2nd order DT modulator architecture. To achieve target SNR ≥ 100 dB at V_{dd}= 1.8V from full scale of the feedback DAC, the input capacitance (C_{in}) value is determined by input signal (V_{in}^2) = 1.2V [Full Scale], signal power (V_s), In-band noise ($V_{in\text{-}band}$) and the noise power (V_n) is calculated by following Eq.'s (5)-(7):

$$V_s^2 = 0.5 \times \frac{V_{in}^2}{4} = 0.64 \quad (5)$$

$$V_{in-band}^2 = \frac{\left(\frac{V_{dd}}{2}\right)^2/2}{10^{\frac{SNR}{10}}} = 0.405/10^{10} = 4.05\text{x}10^{-11} \quad (6)$$

$$V_n^2 = V_{in-band}^2 \times OSR = 4.05\text{x}10^{-11} \text{ x } 128 = 5.184\text{x}10^{-09} \quad (7)$$

The input capacitances (C_{in} and C_{2in}), integration capacitors (C_{IF} and C_{2F}) is calculated based on KT/C noise consideration and given by Eq.'s (8)-(12):

$$C_{in} = \frac{4KT}{V_n^2} = \frac{1.656\text{x}10^{-20}}{5.184\text{x}10^{-09}} = 3.19 \text{ pF} \quad (8)$$

Where Boltzmann Constant (K) = $1.38\text{x}10^{-23}$, Temp (T) = 300 K.

$$C_{2in} = 10\text{fF} \quad (9)$$

Since noise contribution is negligible for lower power consumption, so it needs to designed to be small

$$C_{1F} = \frac{\text{Cin}}{\text{a1}} = \frac{3.19\text{x}10^{-12}}{0.79954} = 3.99 \text{ pF} \quad (10)$$

$$C_{2F} = \frac{\text{C2in}}{\text{c1}} = \frac{10\text{x}10^{-15}}{0.126} = 79.3\text{fF} \quad (11)$$

$$C_{2dac} = C_{2F} \times a_2 = 78.9\text{x}10^{-12} \times 0.36288 = 28.7\text{fF} \quad (12)$$

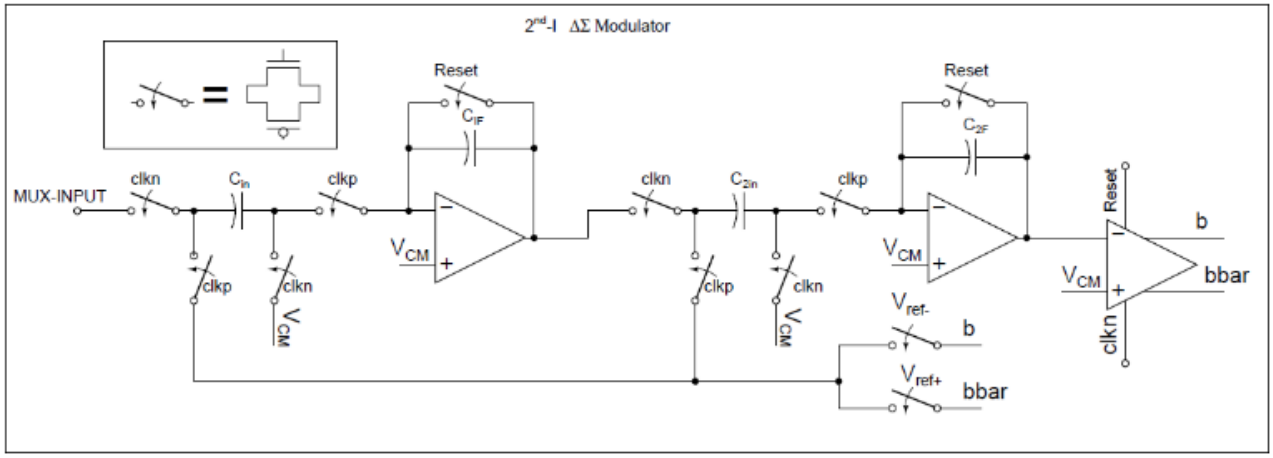


Fig. 4. Circuit diagram of 2nd order DT Modulator for IADC

Fig. 4, shows the circuit diagram of 2nd order DT Modulator for IADC. The 1st and 2nd integrator are implemented using complementary pair folded cascade operational amplifier. During the sampling phase (clkn = high, clkp = low), the input voltage is sampled onto C_{in} and C_{2in}. At the same time, the first integrator is in the unity-gain configuration. During the integration phase (clkn = low, clkp = high), elements of the 1-bit DAC are connected to either Vref+ or Vref-, depending on the quantizer bit stream values (b and bbar), thus transferring an amount of charge from input capacitors (C_{in} and C_{2in}) to the integration capacitors (C_{IF} and C_{2F}) respectively. The feedback loop, as shown in block diagram, creates error by subtracting quantizer output with input signal. By summing the error voltage, the integrator acts as low pass filter to the input signal and high pass filter to the quantization noise, thus oversampled modulator pushes the most of the quantization noise to upper high frequencies and eliminated by low-pass filtering. In reality, the oversampled method has improved the distribution of the total noise power over the wider frequency range as compared to the conventional Nyquist ADC while signal tone is same as before.

2.3. Decimation Filter

In this paper, a SINC3 low pass filter (also known as moving average filter) architecture is selected as the digital decimation filter. This decimation filter is connected after the modulator block in order to extract information from digital n-bit stream which further increase the SNR by removing quantization noise to outside the band of interest. The SINC3 filter greatly attenuates the out of band quantization noise to the extent that it becomes insignificant compared to the in-band noise and finally down samples the signal to the Nyquist rate. Hence, SINC3 filter gives the better out-of-band quantization noise suppression to get higher SNR. An efficient IADC design has required a filter of at least one order higher than the proposed modulator order L, it is define as Eq. (13):

$$M = L+1 \tag{13}$$

Where M and L is the order of the filter and modulator respectively.
For an M[th] order SINC filter with a transfer function is given by Eq. (14):

$$H(z) = \left(\frac{1}{L}\frac{1-z^{-L}}{1-z^{-1}}\right)^{M} \quad (14)$$

which requires N ≥ M.OSR. Hence, N must satisfy both conditions. After N clock cycles, the output word is stored, and the system is reset. In our proposed IADC, M = 2, OSR = 128 and N = 256 clock periods were chosen for converting an input sample.
The SINC3 filter uses a novel implementation of the familiar Hogenauer structure [9], which contains a cascade of integrating, differentiating, and scaling stages.
In this paper, 6-stage decimator have been implemented for F_b = 200 kHz and F_s = 51.2 MHz. The modulator output is decimated all way to Nyquist rate; at last, we have $\frac{F_S}{D_1 D_n} = 2F_B$ where D_1 and D_n are the First and nth stage downscaling factors respectively and F_b the filter bandwidth.

3. Circuit Level Implementation of Proposed 2nd Order Modulator for IADC

3.1. Switched-Capacitor (SC) Circuitry

Settling speed is a key performance requirement for SC circuits. If an SC integrator has a long settling time-constant then it cannot transfer all the stored charges between capacitors during each clock phase. This may seriously compromise circuit performance (gain accuracy, distortion etc.). Two factors that affect settling time are the ON-resistances of the switches and transconductance of the OTA connected to the switches. Table 2 shows the design specifications of integrators.

Table 2: Design specifications for Integrators

OTA gain (Av)	$A_v \geq \frac{2}{q}q = \frac{V_{DD}}{2^N}$	> 30.5 dB
$g_{m,\,min}$	$\sqrt{2\beta I_D}$	20.16m
F_{3dB}	$\frac{g_m}{2\pi C_L}$	54M
C_{in}	$\frac{4KT}{V_n^2}$	3.19 pF
SR_{min}	$\frac{I}{C_L}$	4.7 V / ns
$I_{load,min}$	$SR*C_L$	23.5µA
where $\beta = 237.18E-3$, I_D = 400 µA and C_L = 5fF		

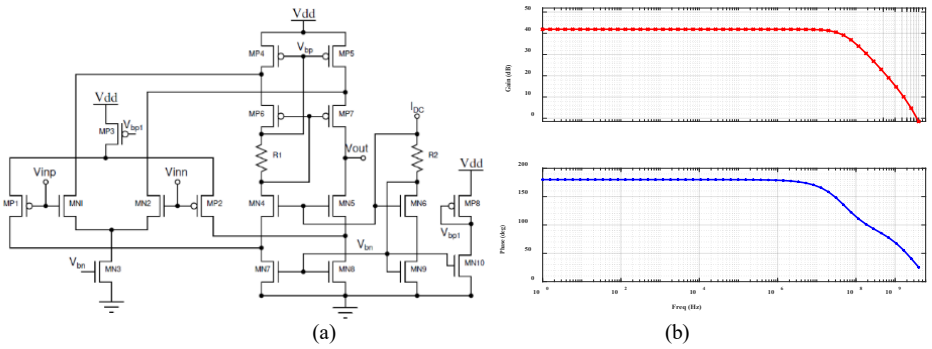
A non-overlapping clock generator with early and late sub-phases is an important block in most SC circuit designs as incorrect clocking can cause serious signal corruption or even complete circuit malfunction.

3.2. Integrator OP-AMP Design

The performance of op-amp dominates overall performance of the proposed modulator used in IADC, so extra care is taken while designing the circuit to reduce the overall power and noise of IADC. Table 3. shows the OTA specifications.

Table 3: OTA specifications	
Gain band width (GBW)	75MHz
Output Bias current	>1.5mA
Phase Margin	> 60 degree
Settling time	244.5ns
DC gain	>40dB
Load Capacitance	5.32fF

Fig. 5(a) shows the complementary input pair folded cascode operational transconductance amplifier, which is used to maximise the input common mode. To enhance the opamp's slew rate, a current mirror network is added for NMOS (MN3 to MN10) and for PMOS (MP3 to MP8), which turns on to provide additional current. Resistors (R1 and R2) are used for self-biasing purpose. The simulation result ensured that the gain of the op-amp is greater than 40dB for integrator to overcome the nonlinearity errors such as noise and charging accuracy (settling error) as shown in Fig. 5(b).



(a) (b)

Fig. 5. Details of the OTA uses (a) Schematic (b) gain and phase waveform

3.3. Dynamic Latch Comparator

The dynamic latch comparator compares the analog inputs voltages (Vinp Vinn), and provide the outputs a binary signals (OP and ON) based on the comparison. If the (+) Vinp, the input of the comparator is at a greater potential than the (-) Vinn, input, the output of the comparator is a logic 1 and vice versa. In this paper, a single-bit quantizer is used to achieve the high resolutions in proposed 2nd order modulator for IADC.

The comparator is a discrete time component with a regenerative feedback [10]. When clock is low tail transistor (MN3) is off and depending on Vinp and Vinn output reaches to VDD or gnd. When clock is high MN3 is on and both the outputs discharges to ground. The comparator needs to have nearly equal slew rate as op-amp to switch quick enough form one voltage to another. The clock provided to the comparator is 51.2 MHz to achieve the oversampling ratio of 128. The Fig. 6 shows the dynamic regenerative comparator used in this work.

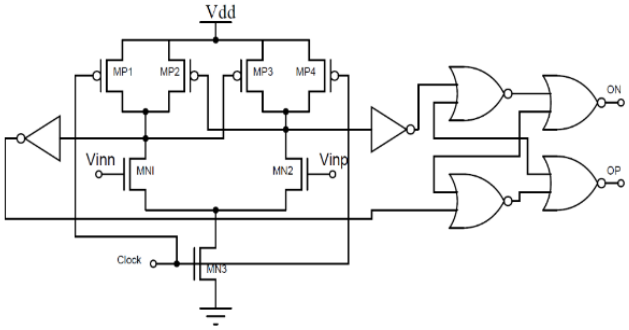


Fig. 6. Dynamic latch Comparator

In order to understand the functionality of given comparator, the circuit is designed using 0.18-µm CMOS technology and simulated at V_{DD}= 1.8V. The comparator were optimized and the transistors dimensions were scaled at the input common mode voltage of V_{CM}=0.9V. Results show the 546.75 pW power consumption and 6.21 µs delay.

4. Modelling and Results

The proposed IADC architecture has been implemented using standard 0.18µm TSMC CMOS process. To perform the experimental analysis of IADC in the incremental mode, 2-layer PCB was designed using Altium software, which consist of necessary blocks, such as a synchronization circuit, appropriate signal conditioning block, voltage/current biasing circuitries, required for the chip operation as shown in Fig. 7. For flexibility purposes, SINC3 filter were implemented in MATLAB. The proposed IADC operates at 1.8V power supply as all the columns are subject to the same 1.8 reference voltages, no column-level calibration is needed.

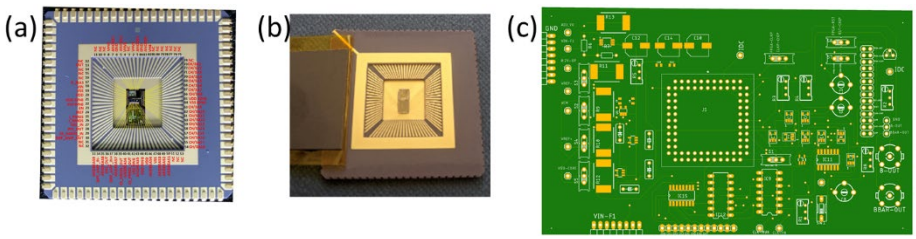


Fig. 7. Proposed Chip (a) bonding diagram of proposed chip (b) fabricated chip (c) custom PCB board layout to test the chip

4.1 Measurement Setup

The core modulator circuit has been fabricated and chracterised in a bench-top setting, using a custom PCB. To attenuate voltage ripple and noise from the external power supplies, low-dropout regulator ICs are used on the PCB to generate various voltages such as Vref+ (1.6V), Vref-(0.2V), Vcm (0.9V) and Vdd (1.8V) essential for the chip operation. The bias currents generated on PCB are derived from Vdd (1.8V) using an adjustable current source IC. A sinusoidal input test signal was fed into one channel (approximately 25 kHz) of the Mux while all the other channels were grounded. The performance is determined by the IADC's bandwidth which covers 8 channels. The external sinusoidal analog input signal was generated by signal generator and the PCB was powered up using dc power supply. To drive the synchronization circuit, the required 51.2 MHz main clock signal was generated by an arbitrary function generator. The same clock source was used tp create S/H clock signal for multiplexer, non-overlapping clock signals (clkn, clkp), and reset signals (Reset). The modulators outputs i.e. digital output data stream along with reset signals are captured by a logic analyzer (Tektronix TLA614). These data streams were then imported into MATLAB. A decimation filters described in Section 2.3 was applied and fast-fourier-transform (FFT) was performed using a MATLAB to compute the performance metrics.

4.2. Results

In order to characterize the entire ADC further, a detailed simulation setup was used. The proposed 8-channel incremental ADC with input bandwidth of 25 kHz on each channel is sampled at 51.2 MHz, with 128-clock cycles/conversion. The power consumption of each ADC is 0.832 mW, dominated by the power-hungry complementary input pair folded-cascode amplifiers.

The power spectrum density (PSD) of the IADC with multiplexed input frequencies of 11 kHz, 15 kHz, 16 kHz and 19 kHz in four different channels and rest inputs are grounded at 51.2 MS/s is shown in Fig. 8. The SNR is approximately 64.14dB (10.24 ENOB).

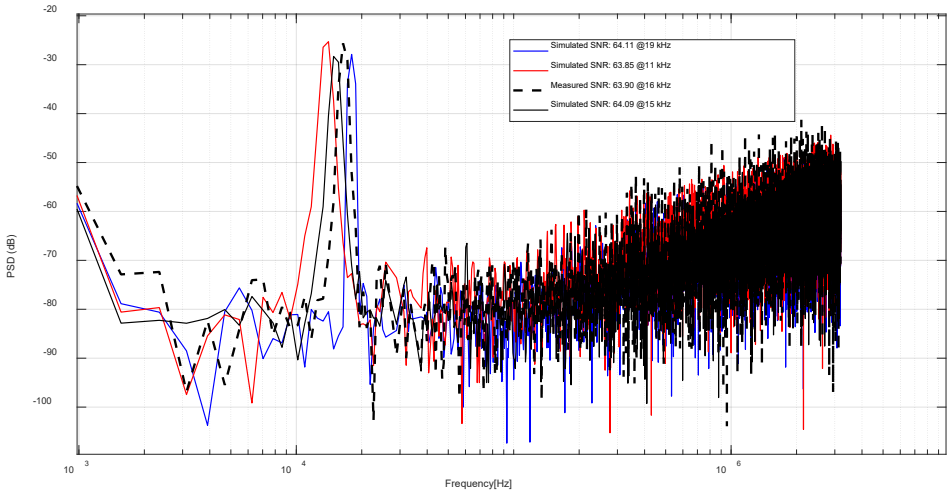


Fig.8. PSD plot of IADC

In a multiplexed ADCs, when the input channel is switched to the next channel, one of the key challenges is that ADC must be able to support a large voltage amplitude step change and fast transition, even for dc type signals, because the input step could go from negative full-scale voltage (sometimes ground) to positive full-scale voltage or vice versa. Fig. 9 shows the proposed multiplexed ADC for four different input channels with different input amplitudes while rest four channels are connected to ground. The result shows the proposed IADC has fast transition time as anticipated and it has error (298mV) which is less than the one LSB in the digitized output as expected.

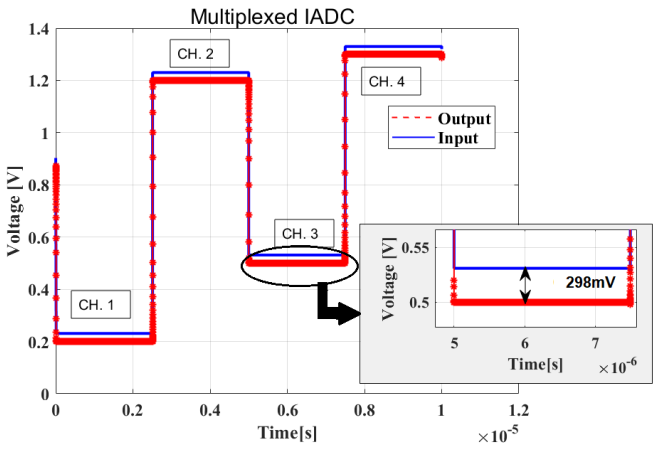
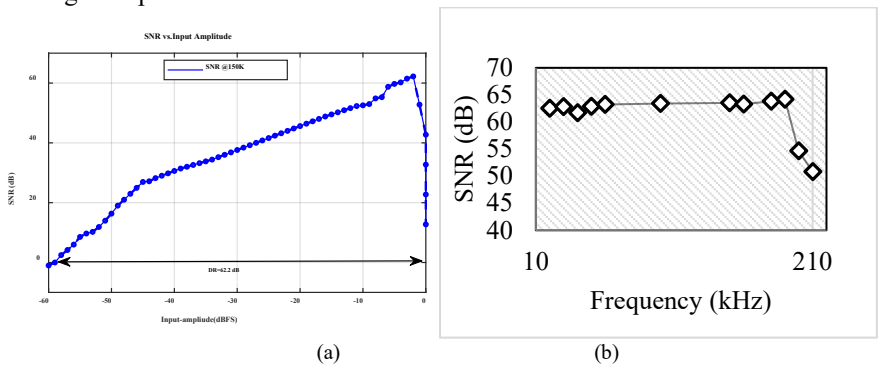


Fig. 9. Multiplexed IADC

Moreover, the proposed IADC has been tested at fixed 150 kHz bandwidth to get the SNR (dB) versus the input amplitude (dBFS) plot as shown in Fig. 10(a). The plot shows

dynamic range of the IADC is 62.2dB and it starts falling down due to large amplitude or limited headroom of IADC. Whereas Fig. 10(b) shows the SNR estimation of IADC by varying the input frequency ranging from 10k to 210k at Fs 51.2 MS/s. The graph shows that the proposed IADC gives constant SNR at maximum 200 kBW after that it starts decreasing as expected.



(a) (b)

Fig. 10. (a) SNR (dB) versus input amplitude (b) SNR versus input frequency

To demonstrate a realistic application of the IADC, pre-recorded neural data was fed into the simulation and compared after digitization at the output. Two different neural data were connected to two channels and the rest six channels were kept at a constant potential (grounded). The obtained results shown in Fig. 11 clearly indicated the satisfactory agreement with the measurement data.

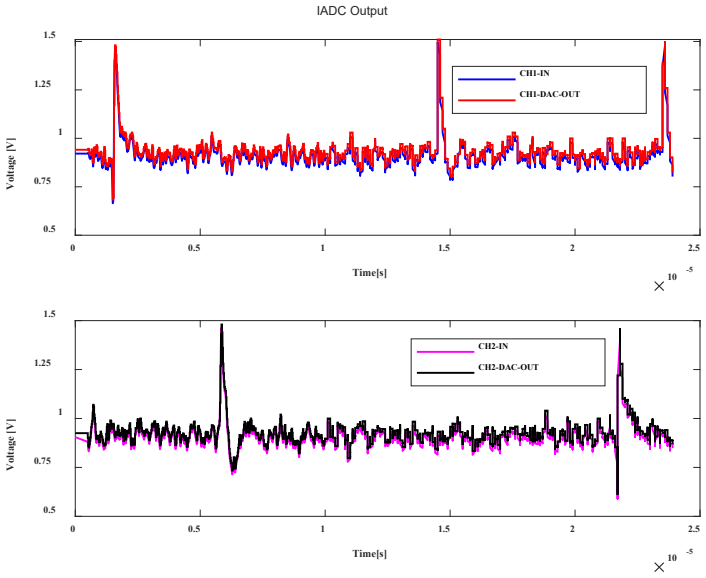


Fig. 11. 8-Channel IADC inputs and outputs

Table 4 summarized the IADC's simulated performance. The overall performance is compared with other state-of-the-art high resolution incremental ADCs [25-286] as shown in Fig. 12. For IADCs, the figure-of-merit (FoM) derived from Schreier's FoM [30] can be calculated as follows:

$$FOM = \frac{Power}{2 \times BW \times 2^{\frac{SNR-1.76}{6.02}}} \quad (15)$$

Table 4: Chip Summary and Measured Characteristics	
Technology	TSMC 0.18µm CMOS
Power supply	1.8 V
Amplifier	
Gain A_v	40dB
Bandwidth	55 MHz
I_{bias}	1.5m
ADC	
Full Scale	1.6V
SNR @200 kHz	63.90 (dB)
Sampling rate	51.2 MHz
Resolution	10.4 bits
Chip Total	
Power consumption	832.6uW
Die size	0.03262 mm^2

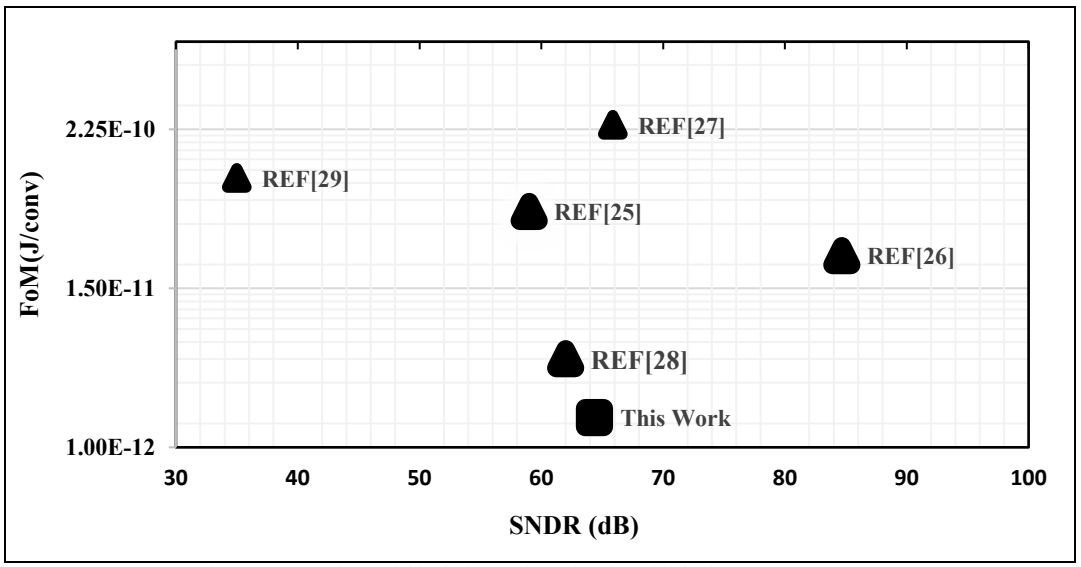


Fig. 12. Comparison of this design and previously published IADC

Table 5 shows performance comparison of various published designs, this proposed design gives significantly less FoM compared to similar spec designs.

Table 5: Performance summary and comparison with previous work

	This work	**Ref [25]**	**Ref [26]**	**Ref [27]**	**Ref [28]**	**Ref [29]**
ADC Architecture	**2nd-order DT Incremental**	**1st-order CT Incremental**	**Hybrid IADC**	**3rd-Order Modulator**	**CT-IADC**	**DT-IDC**
BW (Hz)	**200 k**	250	300	25 k	8.2 k	6 k
Sampling Frequency (MHz)	**51.2**	0.512	2.51	10.24	67.1	0.2
Resolution/ENOB (bits)	**10.4***	9.5	13.77	10.11	10	5.44
SNR (dB)	**63.9**	59	84.68	65.87	62	35
Power (μW)	**832.6**	20	218.81	18821.2	75.9	6.4
FoM_{walden} (pJ/conv)	**1.651**	55.24	26.10	242.5	4.51	98.1
Area (mm^2)	**0.032**	2.25	0.037	0.3015	9	0.036
Tech. (nm)	**180**	500	180	180	500	180
Power Supply (V)	**1.8**	1.6	1.8	1.8	3.3	1.8

5. Conclusions

The implemented modulator for IADC is well suited for high-density multiplexed neural recording. It performs well with an especially favourable power consumption and chip area. In the proposed IADC, a multiplexed modulator not only eliminates the need for a large oversampling ratio but also improves both resolution and stability. Measurements on the modulator show very good match with simulated results. The overall ENOB, power consumption and chip area (10.11 bits, 0.832 mW, and 0.032 mm^2 respectively) are comparable to the state of the art.

Acknowledgments

This project has received funding from the European Union's Horizon 2020 research and innovation programme under the Marie Skłodowska-Curie grant agreement No 798381

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