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Atomic layer deposited Al_2O_3 passivation layer for few-layer WS_2 field effect transistors

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Abstract.

We have investigated the effect of an Al_2O_3 passivation layer on the performance of few-layer WS_2 FETs. While the performance of WS_2 FETs is often limited by a substantial decrease in carrier mobility owing to charged impurities and a Schottky barrier between the WS_2 and metal electrodes, the introduction of an Al_2O_3 overlayer by atomic layer deposition (ALD) suppressed the influence of charged impurities by high-κ dielectric screening effect and reduced the effective Schottky barrier height. We argue that n-doping of WS_2, induced by positive fixed charges formed at Al_2O_3/WS_2 interface during the ALD process, is responsible for the reduction of the effective Schottky barrier height in the devices. In addition, the Al_2O_3 passivation layer protected the device from oxidation, and maintained stable electrical performance of the WS_2 FETs over 57 days. Thus, the atomic layer deposition of Al_2O_3 overlayer provides a facile method to enhance the performance of WS_2 FETs and to ensure ambient stability.

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Keywords: WS_2, Al_2O_3, field effect transistor, dielectric screening, ambient stability, Schottky barrier

[3] These authors contributed equally to this work

1. Introduction

Two-dimensional van der Waals materials such as transition metal dichalcogenides (TMDC) and graphene have attracted considerable attention owing to their wide variety of electronic properties[1]. Among various TMDC, MoS_2 attracted the most attention due to its excellent electrical properties and robustness, and showed potential as a field-effect transistor (FET)[2, 3, 4] and photo-detector with high sensitivity[5, 6]. Interest in WS_2, another representative of semiconducting TMDC, has been raised in anticipation of higher carrier mobility than MoS_2. Because of a smaller effective mass, a higher mobility and on-current density than MoS_2 were expected for WS_2[7] and there have been considerable efforts to investigate WS_2-based FETs[8, 9].

Despite excellent theoretical mobility of WS_2, $\sim$250 $cm^2V^{-1}s^{-1}$ for the monolayer at room temperature[10, 11], the performance of WS_2 FETs is limited by three factors. Firstly, charged impurities such as chemical residue and gaseous adsorbates were shown to result in a substantial decrease in carrier mobility[12, 13, 14], similar to the case for MoS_2[15]. High-κ oxide could reduce the effect of charged impurities by dielectric screening [16, 17, 18, 19, 20, 21, 22], and Cui et al.[14] reported the enhancement of the mobility in WS_2 FETs by using a thin Al_2O_3 dielectric layer between WS_2 and the SiO_2 substrate. Another limiting factor for the device performance is damage due to oxidation. Oxidation of WS_2 has been reported in many publications[23, 24, 25] and the degradation of WS_2 via oxidation under ambient conditions is a potential obstacle for application as FETs. Polymer, hBN or Ga_2O_3 encapsulation are reported to prevent the degradation in air[23, 26]. The last factor affecting the performance of FETs is the Schottky barrier and the contact resistance between WS_2 and electrodes. Achieving low contact resistance in WS_2 by simply using low work function metals is known to be difficult because the Fermi level tends to be pinned at charge neutrality level located in the middle of the bandgap[27, 28, 29, 30]. As an alternative approach, an ultrathin Al_2O_3 layer was inserted between the metal and WS_2 as a depinning layer [30] or heavy doping of WS_2 under the metal is reported to decrease the contact resistance[31, 32]. Heavy doping reduces the Schottky barrier width and enhances the electron tunneling through the barrier.

In this study, 30 nm-thick Al_2O_3 was used as the passivation layer of WS_2 FETs and the effect on the performance of devices was investigated. The introduction of an atomic layer deposited Al_2O_3 overlayer not only suppressed the influence of charged impurities by high-κ dielectric screening but also reduced the effective Schottky barrier height and provided ambient stability for a longer period.

2. Experimental Methods

WS_2 was prepared by mechanical exfoliation on a 300 nm SiO_2/Si substrate. WS_2 samples were selected with thickness ranging from 3.5 to 12 nm, determined via atomic force microscopy (AFM). Seven WS_2 FETs were fabricated using conventional e-beam

lithography, followed by e-beam evaporation of Ti(5 nm)/Au(50 nm) contacts. Al_2O_3 layers were then grown on the WS_2 FETs by using atomic layer deposition (ALD) at 200 °C. Before the ALD process, the WS_2 devices were exposed to UV-O_3 light for 3 minutes to functionalize the WS_2 surface with weak sulfur-oxygen bonds to provide nucleation sites.[33]. The UV-O_3 pre-treatment also removed any residual e-beam resist on the WS_2 surface, ensuring uniform growth of Al_2O_3[34]. For the ALD process, trimethylaluminum (TMA) and deionized water were used as precursors. 30 nm-thick Al_2O_3 was deposited by alternately injecting precursors and N_2 gas (TMA/N_2/H_2O/N_2 injections for 0.2/10/0.2/10 s) over 2 hours (300 cycles with a growth rate of 1 Å per cycle). Fig. 1(a) shows optical images of an exfoliated WS_2 on SiO_2 (upper) and the fabricated WS_2 FET covered with Al_2O_3 film (lower). And Fig. 1(b) displays an AFM image (upper) of the WS_2 FET and the AFM height profiles (lower) along the red line indicated in the AFM image. The height profiles of WS_2 over the SiO_2 substrate, recorded before and after the Al_2O_3 deposition, exhibit almost the same thickness difference of 3.5 nm, indicating the uniform growth of Al_2O_3 over the surface. Fig. 1(c) presents a typical cross-sectional transmission electron microscope (TEM) image of WS_2 capped with Al_2O_3.

3. Results and Discussion

Fig. 1(d) displays the transfer characteristics of the WS_2 device shown in Fig. 1(a), measured at room temperature in vacuum before and after the Al_2O_3 deposition. The WS_2 transistor characterized before the Al_2O_3 deposition exhibits a large clockwise hysteresis caused by charge traps such as residual e-beam resist and water molecules. By introducing the Al_2O_3 capping layer on WS_2, the hysteresis is suppressed and the carrier mobility, estimated from the slope of the transfer curves in the on-current regime, is enhanced from 0.4 to 22 $cm^2V^{-1}s^{-1}$. In addition, the on-off current ratio increased from 10^3 to 10^6 and the subthreshold swing decreased from 2.07 V/dec to 1.25 V/dec. During the ALD process, the moisture on the WS_2 surface may react with TMA to form Al_2O_3[18], and high-κ dielectric screening reduces the effect of the charged impurities, resulting in the suppression of hysteresis and the enhancement of the mobility and better performance of the WS_2 FET. On the other hand, we note the threshold voltage was negatively shifted after introducing the Al_2O_3 overlayer. It is common in Al_2O_3 that interface traps exist at the Al_2O_3/WS_2 interface and they are usually positively charged [18, 35], leading to the negative shift of threshold voltage via electrostatic doping of WS_2. Later, we show the doping effect decreases the contact resistance between the metal electrodes and WS_2, and contributes to the enhancement of the performance of transistor. Similar changes in transfer characteristics are observed for all 7 WS_2 FETs investigated. In Fig. 1(e), mobility enhancement is summarized for the 7 devices (3.5 to 12 nm in thickness) labelled from a to g. The mobility increased after the deposition of Al_2O_3, regardless of the thickness of WS_2. On average, the mobility at room temperature increased from 9.4 to 38 $cm^2V^{-1}s^{-1}$ with the Al_2O_3 capping layer. On the other hand,

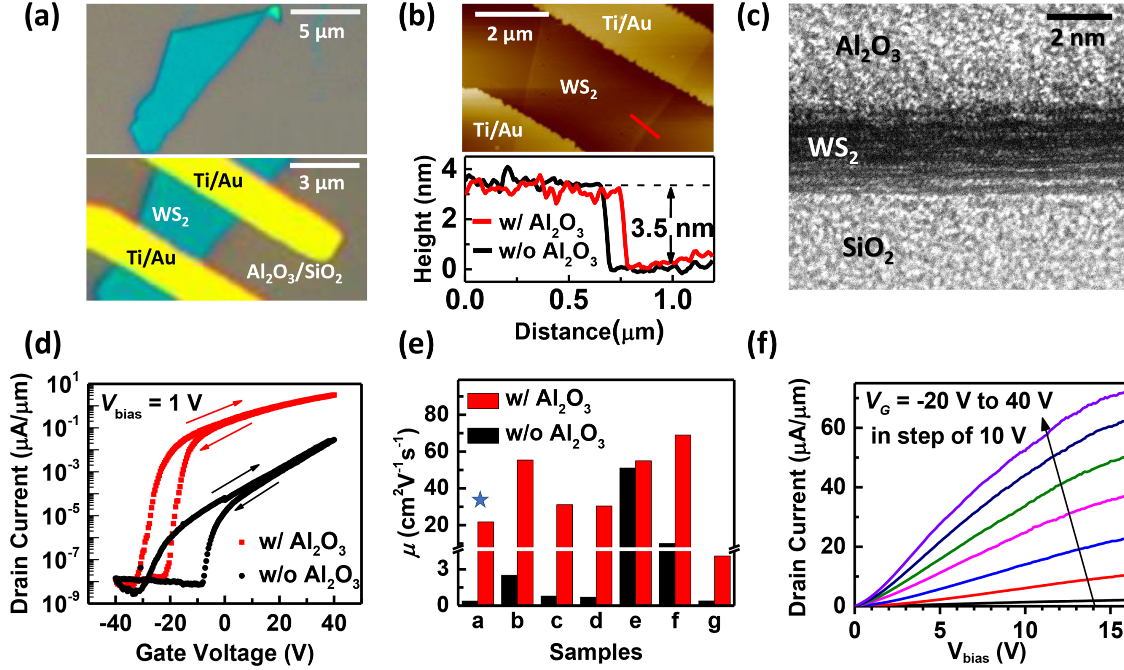

Figure 1. (Color online) (a) Optical images of (Upper) an exfoliated WS_2 on SiO_2 and (Lower) the fabricated WS_2 FET capped with Al_2O_3. (b) (Upper) AFM image of the WS_2 FET and (Lower) AFM height profiles before(black) and after(red) the Al_2O_3 deposition along the red line indicated in the AFM image. (c) A typical cross-sectional TEM image of WS_2 with Al_2O_3. (d) Drain current per unit width versus gate voltage for a WS_2 FET before and after Al_2O_3 deposition measured in a vacuum at room temperature. Source-drain bias voltage, $V_{\rm bias}$, of 1 V is applied. (e) Summary of mobility enhancement for 7 WS_2 FETs labelled from a to g. The images and the transfer characteristics shown in (a), (b) and (d) are from the sample a, marked with a star. (f) Output characteristics of a WS_2 FET (sample a) with Al_2O_3.

a clear relationship between thickness and mobility was not found. Charge transport in WS_2 FETs was dominated by extrinsic factors such as charged impurities, and the extracted mobilities (w/o Al_2O_3) varied between 0.3 and 50 $cm^2V^{-1}s^{-1}$ depending on the level of impurities. When the device was fabricated with fewer impurities, a much larger mobility resulted as seen from the sample e. With the Al_2O_3 passivation layer, the mobility was not only enhanced but also varied much less, between 5 and 70 $cm^2V^{-1}s^{-1}$. The observed mobility of 70 $cm^2V^{-1}s^{-1}$ is slightly larger than previously reported room-temperature mobility of few-layer WS_2 FETs. Chloride molecular doping [31] or LiF doping [32] enhanced the mobility of few-layer WS_2 up to 60 and 34.7 $cm^2V^{-1}s^{-1}$, respectively, by reducing the contact resistance. Inserting a thin Al_2O_3 layer between the metal and WS_2 as a depinning layer resulted in enhanced mobility of 10 $cm^2V^{-1}s^{-1}$ [30]. Fig. 1(f) shows the output characteristics of the WS_2 device with Al_2O_3.

To further understand the mechanisms that limit the mobility of WS_2 FETs capped with Al_2O_3, we have investigated the temperature(T) dependence of the transfer curves. Figs. 2(a) and 2(b) present the transfer characteristics of the WS_2 transistor on a linear

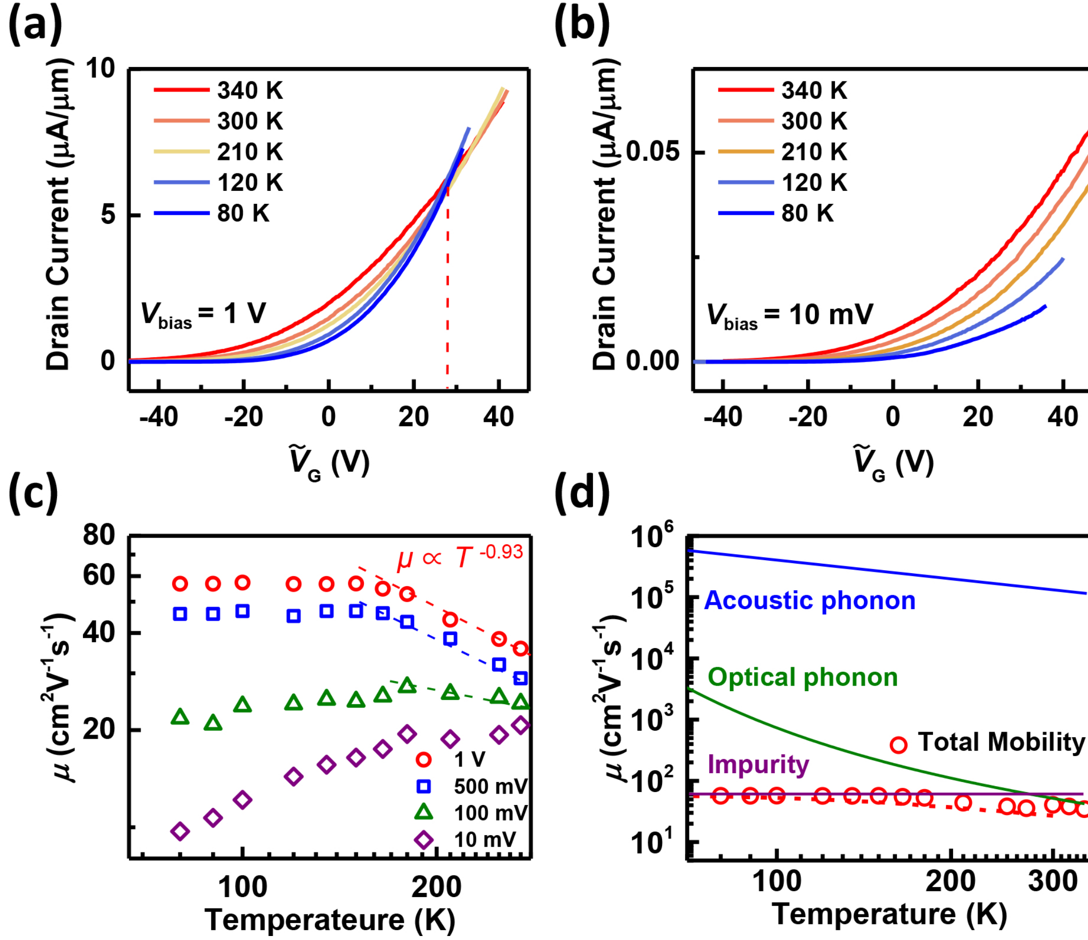

Figure 2. (Color online)(a), (b) Transfer characteristics of the WS_2 transistor measured between 80 and 340 K at $V_{\text{bias}} = 1$ V and 10 mV, respectively. The threshold voltage was adjusted to be located at $\widetilde{V_{\text{G}}} = 0$ V in order to better investigate the temperature dependence of the WS_2 FET. (c) Temperature dependence of field-effect mobility for the WS_2 FET at different source-drain bias voltages. (d) Temperature dependence of mobility at $V_{\text{bias}} = 1$ V (hollow red circles) and the fitted electron mobility (dashed line). The fitted mobility combines contributions from optical phonons (green), acoustic phonons(blue), and impurities (purple).

scale, measured between 80 and 340 K with source-drain bias voltage of $V_{\text{bias}} = 1$ V and 10 mV, respectively. We note the T-dependences of the transfer curves are distinct depending on applied V_{bias}. When $V_{\text{bias}} = 1$ V, the drain current I decreases with T, presenting metallic behavior for gate voltages $\widetilde{V_G} > 30$ V. The Ioffe-Regel criterion predicts a metal-insulator transition at $k_F \cdot l \sim 1$, with the Fermi wavevector $k_F = \sqrt{2\pi n}$ and mean free path $l = \hbar k_F \sigma / ne^2$ for 2D semiconductors. Here n is the carrier density and σ is the conductivity with $\hbar$ being Planck's constant and e being the elementary charge. For our few-layer WS_2 device, we obtain $k_F \cdot l \sim 0.5$, slightly lower than 1. The lower value of 0.5 could be due to the Schottky barrier formed between the metal electrode and WS_2 as the contact resistance results in a smaller σ, thereby a smaller l in our estimation. When a low V_{bias} of 10 mV is applied, the Schottky

barrier becomes dominant in electrical transport and exhibits insulating behavior for all gate voltages (Fig. 2(b)). Fig. 2(c) displays the temperature dependence of the field-effect mobility extracted from the transfer curves measured at various drain bias voltages. At $V_{\text{bias}} = 1$ V, the mobility follows $\mu \sim T^{-\gamma}$ with the exponent $\gamma = 0.93$ and saturates below ~150 K. Considering only the effect of phonon scattering in monolayer WS_2 devices, theory suggests a temperature dependence of mobility with $\gamma = 0.99$ - 1.28[36]. Experimentally, $\gamma = 0.73$, 1.75 were reported for mono and bi-layer WS_2 devices on SiO_2 substrates, respectively [14] and 1.15 for a few-layer WS_2 device[37]. Our results are in general consistent with previous studies, but we report a slightly lower gamma of 0.93. Suppression of the out-of-plane phonon mode by the presence of the Al_2O_3 capping layer could be responsible. On the other hand, as we decrease V_{bias} below 100 mV, the temperature dependence of the mobility presents different behavior. At $V_{\text{bias}} = 10$ mV, the role of the Schottky barrier becomes dominant and the extracted mobility decreases with decreasing temperatures. Before we discuss the Schottky barrier in the device, we focus on the charge scattering mechanism in our WS_2 FETs. Fig. 2(d) shows the temperature dependence of mobility at $V_{\text{bias}} = 1$ V and we fit the data including scattering contributions from optical phonons, acoustic phonons and charged impurities. Using Mathiessen's rule, the total mobility is given by $\mu^{-1} = {\mu_{\text{op}}}^{-1} + {\mu_{\text{ac}}}^{-1} + {\mu_{\text{imp}}}^{-1}$, combining three contributions. Here we neglect the contribution from the contact resistance R_c, as we estimate R_c to be less than 4% of the total resistance at $V_{\text{bias}} = 1$ V (see supplementary information). The temperature dependence of optical phonon scattering can be described by the equation

$$\mu_{op} = \left(\frac{4\pi\varepsilon_0\varepsilon_p\hbar^2}{e\omega m^{*2}t}\right)[\exp\left(\frac{\hbar\omega}{k_BT}\right) - 1] \tag{1}$$

, where $\hbar\omega$ is the optical phonon energy, m^* is the effective electron mass, t is the crystal thickness, and $1/\varepsilon_p = 1/\varepsilon_\infty$ - $1/\varepsilon_s$ with ε_∞ and ε_s being the high frequency and static dielectric constant, respectively[38]. The acoustic phonon scattering was calculated using following equation;

$$\mu_{ac} = \frac{e\hbar^3\rho\nu}{Dm^{*2}k_BT} \tag{2}$$

, where ρ is the crystal density, D is the deformation potential, and ν is velocity of the acoustic phonon. To fit our data, an effective mass of 0.45 m_e was used, and other parameters were obtained from the literature[39]. The temperature dependence of the mobility from the measurement agrees well with the fitted mobility. The optical phonon limits the mobility near room temperature, resulting in $\mu \sim T^{-0.93}$ as seen in the Fig. 2(c). On the other hand, for low T below 150 K, contribution from impurities dominated and the mobility saturated. Impurity limited mobility (μ_{imp}) can be extracted from the fitting result. For the device with an Al_2O_3 overlayer, $\mu_{\text{imp}} \sim 60$ cm^{2}V^{-1}s^{-1} is extracted, while for a device without the Al_2O_3 overlayer $\mu_{\text{imp}} \sim 10$ cm^{2}V^{-1}s^{-1} is estimated (data not shown). This indicates that Al_2O_3, a high-κ oxide, indeed reduces the influence of charged impurities by the dielectric screening effect.

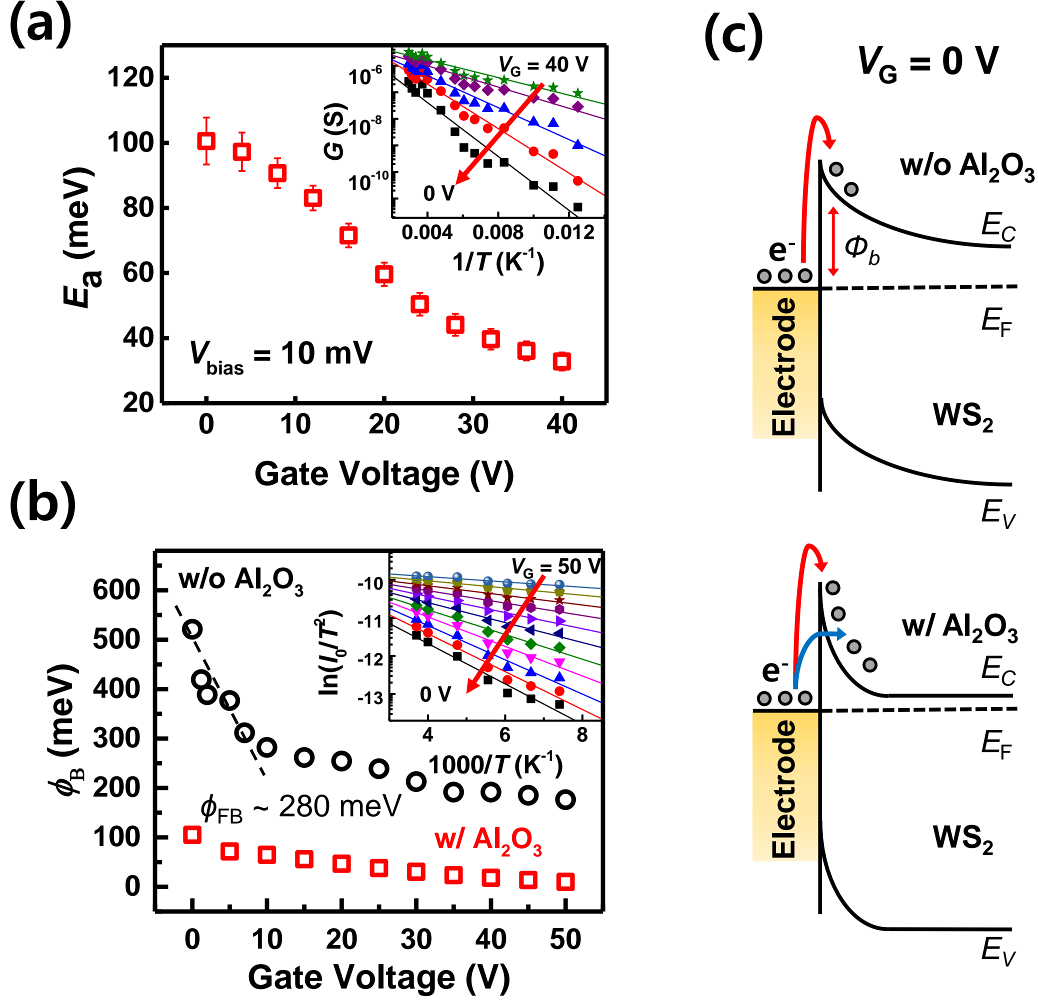

Figure 3. (Color online)(a) Thermal activation energy E_a as a function of gate voltage extracted from the Arrhenius plots of the conductance (inset). (b) Extracted effective Schottky barrier height as a function of gate voltage by using the Schottky diode equation from the inset which shows $\ln(I_0/T^2)$ versus $1000/T$ for different V_G. (c) Schematic diagram of the Schottky barrier for devices without Al_2O_3 overlayer(upper) and with Al_2O_3 overlayer(lower) at $V_G = 0$ V.

We now turn our attention to the Schottky junction formed in our device, and to the data obtained at $V_{bias} = 10$ mV, where the Schottky junction plays an important role in the electrical transport. The inset of fig. 3(a) shows the Arrhenius plot of conductance G for various gate voltages. The activation energy can be extracted by fitting the conductance with the expression $G(T) = G_0 e^{-E_a/k_B T}$, where G_0 is constant and E_a is the activation energy with k_B being the Boltzmann constant. The extracted activation energy is displayed in Fig. 3(a) and E_a decreases with increasing gate voltage. As mentioned earlier, positive fixed charges are formed at the Al_2O_3/WS_2 interface and n-doping to the WS_2 is induced. Owing to the enhanced n-doping, the Fermi-level is located near the conduction band edge and E_a ranges between 100 and 32 meV in our

gate-voltage window. E_a decreases with V_{G} as the Fermi level further approaches the conduction band. However, while the transistor already turned on at $V_{\mathrm{G}} = 30$ V, the activation energy of ~ 40 meV remained, possibly due to the presence of the Schottky barrier. Recall that the same device showed metallic behavior for $\widetilde{V_G} > 30$ V when a V_{bias} of 1 V, which is large enough to overcome the barrier, is applied (Fig. 2(a)). In order to extract the effective Schottky barrier height ϕ_B, we used the Schottky diode equation.

$$I = AA^{*}T^{2}\mathrm{exp}\left(\frac{-\phi_B}{k_BT}\right)[\mathrm{exp}\left(\frac{eV_{\mathrm{bias}}}{\eta k_BT}\right) - 1] \tag{3}$$

, where A is the area of the Schottky junction and A^* is the Richardson constant, with η being the ideality factor. Inset of Fig. 3(b) shows $\ln(I_0/T^2)$ versus $1000/T$ for different V_{G}, where $I_0 = AA^{*}T^{2}\mathrm{exp}\left(\frac{-\phi_B}{k_BT}\right)$. From the slope, ϕ_B (square) is extracted and displayed as a function of the gate voltage in Fig. 3(b). The effective Schottky barrier height decreases from 105 meV to 10 meV with increasing V_{G} from 0 to 50 V. For comparison, ϕ_B (circle) is extracted for a device without the Al_2O_3 capping layer. Flat-band Schottky barrier height (ϕ_{FB}) is estimated to be 280 meV (see dashed line in Fig. 3(b)), comparable to 240 meV from the previous study for a Ti electrode[29]. We find the effective Schottky barrier height is much lower for the device with the Al_2O_3 capping layer at the same gate voltage. Positive fixed charges formed at the Al_2O_3/WS_2 interface induce n-doping to the WS_2 and make the Schottky barrier thinner for the device with the Al_2O_3 overlayer, as illustrated in Fig. 3(c). Owing to the thinner barrier, the current can flow via thermionic-field emission in addition to the traditional thermionic emission[40], resulting in the lower effective Schottky barrier for WS_2 FETs with an atomic layer deposited Al_2O_3 passivation layer.

Lastly, we have investigated the ambient stability of WS_2 transistors capped with Al_2O_3. Figs. 4(a) and 4(b) present transfer curves and the extracted field-effect mobility of the WS_2 FET (sample a) at room temperature, recorded between 2 days and 57 days after the deposition of Al_2O_3. Over the period, transfer curves and the extracted field-effect mobility remained stable as shown in Fig. 4(b). On the contrary, clear degradation is observed for WS_2 FETs without the Al_2O_3 overlayer. Figs. 4(c) and 4(d) display transfer curves and the extracted mobility of a 7.5 nm thick WS_2 FET at room temperature, recorded for 19 days. It is known that sulfur on WS_2 detaches from the WS_2 surface in air and the surface gradually changes to WO_x over time, consequently increasing the resistance (where $x \leq 3$)[24, 25]. Over 19 days, WS_2 gradually oxidized and the mobility of the WS_2 FET decreased significantly from 6.5 to 1.0 $\mathrm{cm^2V^{-1}s^{-1}}$, as seen in Fig. 4(d).

4. Conclusion

In summary, we have investigated the effect of an Al_2O_3 passivation layer on the performance of few-layer WS_2 FETs. The performance of WS_2 FETs is limited mainly

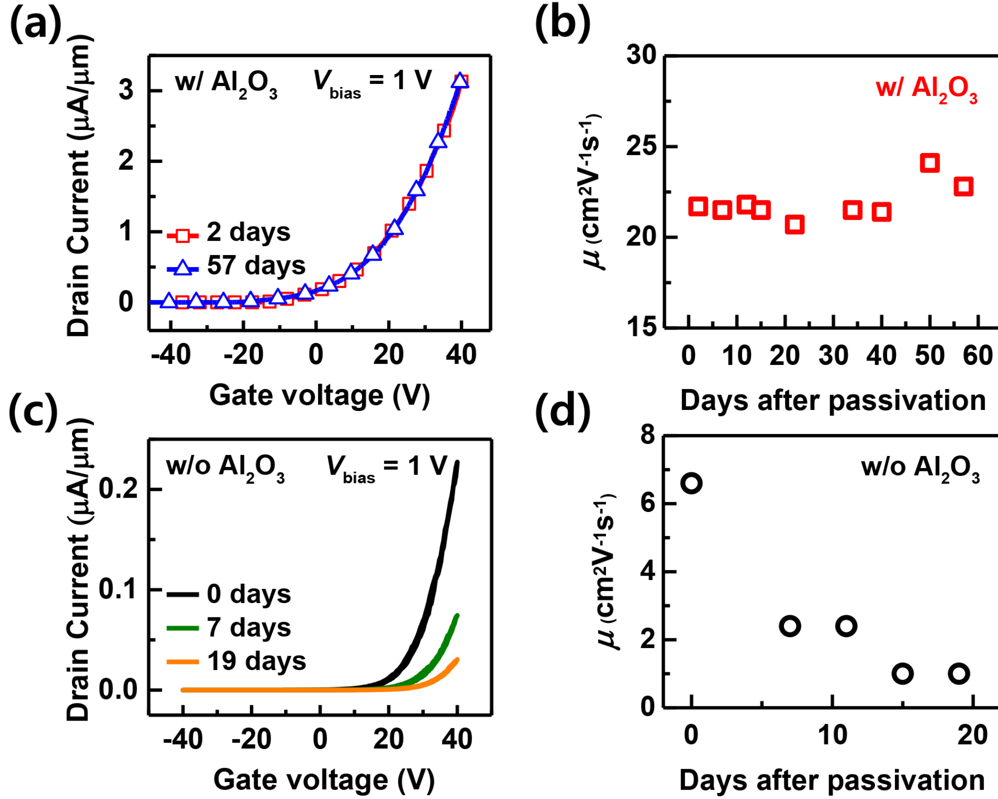

Figure 4. (Color online)(a) Transfer curves of the WS_2 transistor (sample a) recorded at 2 and 57 days after the deposition of Al_2O_3 at room temperature. (b) Extracted electron mobility of the WS_2 transistor versus the time after the Al_2O_3 passivation. (c) Transfer curves of a 7.5 nm thick WS_2 transistor without the Al_2O_3 overlayer at room temperature over time. (d) Extracted mobility of the WS_2 transistor without the passivation layer for 19 days.

by three factors; (1) substantial decrease in carrier mobility originating from charged impurities, (2) the Schottky barrier and the contact resistance between WS_2 and electrodes, (3) oxidation of WS_2 under ambient conditions. Our investigation shows that atomic layer deposition of an Al_2O_3 overlayer provides a facile method to enhance the performance of WS_2 FETs, dealing with all three issues mentioned above. Introducing the Al_2O_3 passivation layer resulted in the enhancement of field-effect mobility (20∼60 $cm^2V^{-1}s^{-1}$ at room T), subthreshold swing, and on-off current ratio by the high-κ dielectric screening effect. In addition, during the ALD process the WS_2 FET is largely n-doped by the positive fixed charges formed at the Al_2O_3/WS_2 interface, and the doping effect reduces the effective Schottky barrier via thermionic-field emission. Lastly, the Al_2O_3 passivation layer protects the device from oxidation, ensuring that the electrical properties of WS_2 FETs remain stable over the 57 days studied. This simple introduction of an Al_2O_3 overlayer can be useful for the application of WS_2 devices.

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