Voltage Control Ratiometric Readout Technique with Improved Dynamic Range and Power-efficiency for Open-loop MEMS Capacitive Accelerometer

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***Abstract*—MEMS capacitive accelerometer for the Internet of Things (IoT) applications is designed with open-loop structure rather than closed-loop structure to achieve low power consumption. In the open-loop structure, voltage control readout technique is preferred for low cost. However, the voltage control readout technique suffers from low dynamic range and low power efficiency (in terms of FoM). In this paper, the voltage control ratiometric (VCR) readout technique is proposed to improve both dynamic range and power efficiency. The VCR readout technique is demonstrated in a readout circuit fabricated in a commercial 0.18um 1.8V/5.0V CMOS process. Compared to the traditional voltage readout circuit fabricated with the same CMOS process and tested with the same sensing element, the VCR readout circuit improves full input signal range by 3.5dB (from $\pm 8\text{g}$ to $\pm 12\text{g}$) and the noise floor by 9.5dB (from $804\mu\text{g}/\sqrt{\text{Hz}}$ to $270\mu\text{g}/\sqrt{\text{Hz}}$). As a result, the dynamic range is improved by 13.0dB (from 44.0dB to 57.0dB), the FoM_1 is improved from 310pJ to 83pJ and the FoM_2 is improved from $1977\mu\text{W}\cdot\mu\text{g/Hz}$ to $796\mu\text{W}\cdot\mu\text{g/Hz}$.**

***Index Terms*—MEMS accelerometer, capacitive sensor interface, readout circuit, oversampling successive approximation technique, correlated level shifting, parasitic capacitance, low power, low noise.**

I. Introduction

MEMS (Micro-electromechanical Systems) capacitive accelerometers play a fundamental role in a wide range of monitoring systems for the Internet of Things (IoT) applications [1]-[3]. In these applications, sensors are powered by battery, therefore low power consumption is required to extend battery life [3]-[5]. To achieve low power consumption, the readout circuits of MEMS accelerometers are designed with open-loop structure (e.g., charge control readout [6]-[8] and voltage control readout [9]-[18]) rather than closed-loop one (e.g., force feedback readout [19]-[21] and oscillating/resonant readout [22][23]), This is because the force feedback readout needs additional power for electrostatic force generator and a compensation circuit to drive and stable the proof mass, and the oscillating/resonant readout needs additional power for the operational circuit modules such as trans-impedance amplifiers and multipliers. In an open-loop structure, the main issue is that sensing element's nonlinearity increases with the increase of capacitance variation of the sensing element due to its reciprocal trans-function [24]. Charge control readout structure can offer ratiometric trans-function which can linearize sensing element's reciprocal trans-function and provide other benefits such as insensitivity to process variation and resistance to vibration rectification error [25]. However, the die cost of the charge control readout structure is higher than that of voltage control readout structure. This is because the charge control readout structure requires two micromechanical sensing elements to implement fully differential structure while the voltage control readout structure requires only one [7]-[9]. Thus, the voltage control readout is preferred for lower cost in the IoT applications.

The voltage control readout circuits reported up to date cannot provide ratiometric trans-function to linearize sensing element's reciprocal trans-function [9]-[13],[26]-[29]. In order to suppress the non-linearity of the voltage control readout circuit to an acceptable level, the maximum capacitance variation of sensing element has to be limited to several femto-farad level for an acceptable die cost [5]. This leads to that the dynamic range and power efficiency of the voltage control readout structure are worse than those of the charge control readout structure. To improve the dynamic range and power efficiency of the voltage readout structure, both signal range and noise floor should be improved with minimum sacrifice of power consumption. The existing techniques such as active noise cancellation (or post-stage correlated double sampling) [30][31], bandwidth enhanced oversampling successive approximation readout technique [32], negative capacitance technique [33] and noise feedforward technique [24], etc., are very effective for noise floor improvement, but they do not deal with signal range improvement. In this paper, the voltage control ratiometric (VCR) readout technique is proposed to improve both the signal range and the noise floor, therefore increasing dynamic range and achieving high power

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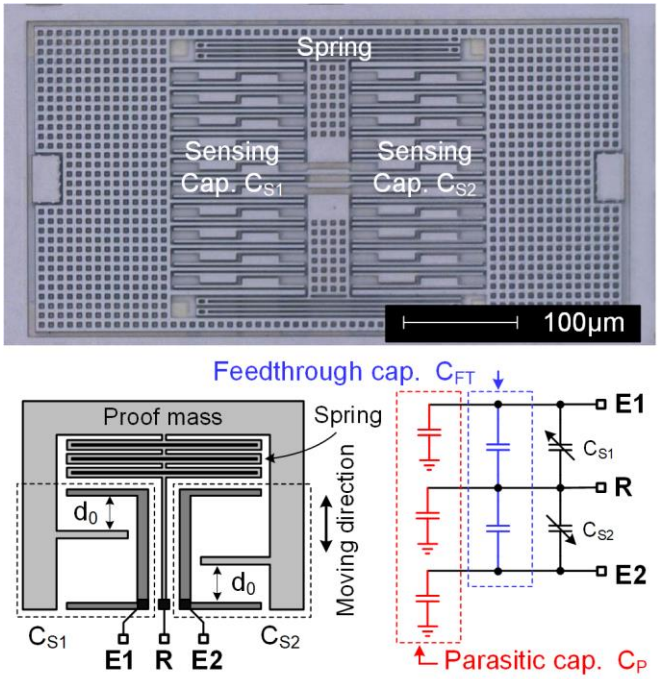


Fig. 1. Sensing element of MEMS capacitive accelerometer.

efficiency.

The rest of the paper is organized as follows. In Section II, both the traditional ratiometric readout structure and the proposed VCR readout structure are described. The circuit implementation of the proposed VCR readout structure is presented in Section III. In Section IV, the physical verification and measurement results are shown and explained. The conclusions are then drawn in Section V.

II. Voltage Control Ratiometric Readout Structures

Fig. 1 shows the photograph (top), the mechanical structure diagram (bottom-left) and the equivalent circuit (bottom-right) of a sensing element in a typical open-loop MEMS capacitive accelerometer. The capacitance C_P is the parasitic capacitance from the electrodes (E1, R, E2) to the ground. The capacitance C_{FT} is the parasitic capacitance between the electrodes E1 and E2. The sensing capacitances C_{S1} and C_{S2} are the parallel-plate capacitors formed by the stator plates (unmovable plates connected to the electrodes E1 and E2) and the rotor plates (movable plates on the proof mass connected to the electrode R via spring), which are expressed below,

$$C_{S1}(x) = C_0\left(\frac{1}{1-x}\right);\ C_{S2}(x) = C_0\left(\frac{1}{1+x}\right);\ x = \frac{\Delta d}{d_0} \quad (1)$$

where C_0 is the rest capacitance of the sensing capacitances, x is the modulation depth, d_0 is the rest distance between a pair of rotor plate and stator plate and Δd is the rotor plate displacement which is in linear proportion to applied acceleration signal [35].

In a traditional voltage control readout circuit shown in Fig. 2(a), the charge signal is generated by driving the differential sensing capacitances C_{S1} and C_{S2} with a step voltage (from zero to V_{EXE}) and driving the common-mode capacitors C_0 with an opposite step voltage (from V_{EXE} to zero). Then, the

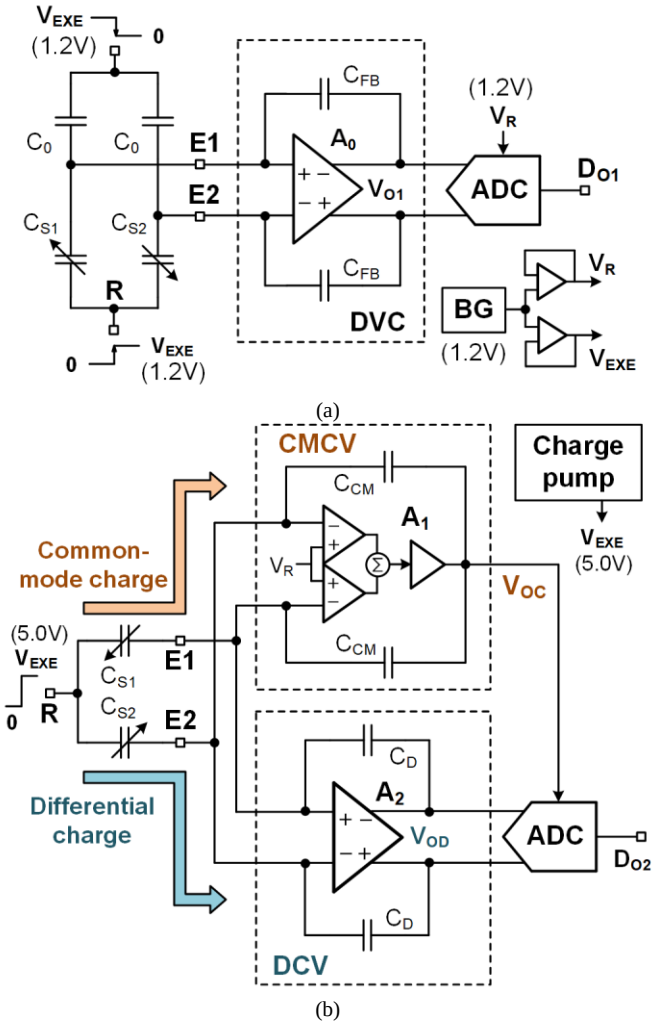


Fig. 2. The readout structures. (a) Traditional voltage control readout structure [9][14]. (b) Proposed voltage control ratiometric (VCR) readout structure.

common-mode part of the charge signal $(C_{S1} + C_{S2})V_{EXE}$ is absorbed by the capacitors C_0 and the differential part of the charge signal $(C_{S1} - C_{S2})V_{EXE}$ flows into the feedback capacitors C_{FB} and produces output voltage V_{O1},

$$V_{O1} = \frac{C_{S1} - C_{S2}}{C_{FB}} V_{EXE} \quad (2)$$

where V_{EXE} is the excitation voltage. The voltage V_{O1} is then converted by the backend analog-to-digital convertor (ADC) which uses voltage V_R as reference. The voltages V_R and V_{EXE} are usually outputted by a bandgap circuit with buffer whose typical value is $1.2V$. The final output of ADC is,

$$D_{O1} = \frac{V_{O1}}{V_R} = \frac{C_{S1} - C_{S2}}{C_{FB}} \frac{V_{EXE}}{V_R} \quad (3)$$

By combining the equations (1) and (3),

$$D_{O1} = \frac{2x}{1 - x^2} \frac{C_0}{C_{FB}} \frac{V_{EXE}}{V_R} \quad (4)$$

Equation (4) indicates that traditional voltage control readout circuit has a second-order nonlinearity term x^2 in the denominator. This is one of the main factors that limit the

dynamic range of open-loop accelerometer.

In the proposed VCR readout structure shown in Fig. 2(b), the charge signal is generated by driving the sensing capacitances C_{S1} and C_{S2} with a step voltage (from zero to V_{EXE}). Then, the common-mode part of the charge signal flows into the capacitors C_{CM} via common-mode feedback provided by the common-mode charge-to-voltage converter (CMCV), producing an output voltage signals V_{OC}. Meanwhile, the differential part of the charge signal flows into the capacitors C_D via differential feedback provided by the differential charge-to-voltage converter (DCV), producing an output voltage signals V_{OD}.

$$V_{OD} = (C_{S1} - C_{S2})V_{EXE}/C_D$$
$$V_{OC} = (C_{S1} + C_{S2})V_{EXE}/C_{CM} \quad (5)$$

The back-end ADC utilizes the output of CMCV as reference voltage to convert the output of DCV, thus resulting in trans-function as,

$$D_{O2} = \frac{V_{OD}}{V_{OC}} = \frac{(C_{S1} - C_{S2})}{(C_{S1} + C_{S2})}\frac{C_{CM}}{C_D} = x\frac{C_{CM}}{C_D} \quad (6)$$

Compared to the expression (4), the expression (6) shows that the VCR structure has two advantages over the traditional voltage control readout structure. Firstly, the sensitivity is independent to the excitation voltage. This means that a low-power open-loop charge pump can be used to provide high-voltage excitation (>VDD) for the VCR structure, in order to achieve low equivalent noise with minimum power requirement. Although the high-voltage excitation provided by the low-power open-loop charge pump can also be employed in the traditional readout circuit to reduce the noise floor, the sensitivity of the traditional readout circuit will suffer from significant variation of the output of the open-loop charge pump. Secondly, the signal range is improved. The equation (6) shows that the VCR structure canceled the second-order nonlinearity in equation (4). This means that the VCR structure can achieve higher linear signal range than that of the traditional structure.

The dominant environmental influence is the thermal drift which causes variation of the distance between the rotor plate and stator plate of the mechanical sensing capacitance, resulting in offset variation. This VCR readout structure does not specifically deal with offset variation as it focuses on enhancing the dynamic range. However, the offset variation can be effectively addressed in this structure as it is addressed in other structures by introducing a self-compensation mechanical structure [35] or a dynamic compensation circuit [39].

III. Circuit Implementation of VCR Readout Structure

The excitation circuit (open-loop charge pump), CMCV and DCV are three important circuits in the VCR readout structure, as shown in Fig. 3(b). These circuits are described in detail in this section.

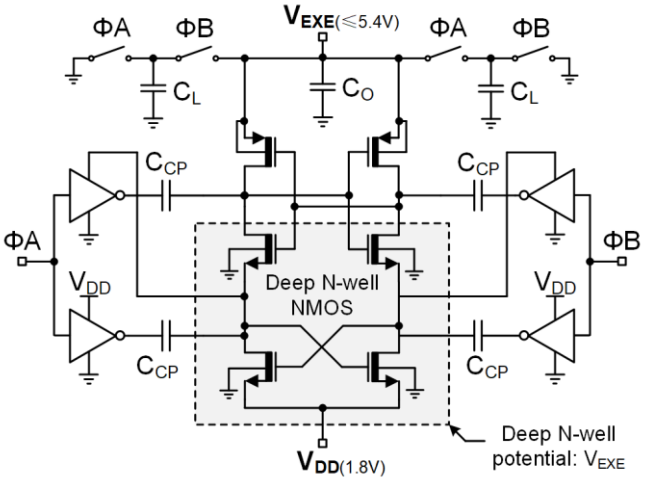


Fig. 3. Schematic of the open-loop charge pump in VCR readout structure.

A. High-voltage excitation circuit (open-loop charge pump)

High-voltage excitation is an effective way to reduce the noise of readout circuit. In the VCR readout circuit, the dominant noise comes from DCV rather than CMCV. This is because the sensitivity of the CMCV which senses the charge from pico-farad-level common-mode capacitance is far smaller than that of the DCV which senses the charge from femto-farad-level differential capacitance. The dominant noise of the DCV comes from the charge noise $\overline{Q_N^2}$ which comes from the parasitic capacitances C_P and C_{FT} [32]. Since the sensing capacitors are excited by the voltage V_{EXE} to produce signal charge, the equivalent input noise $\overline{C_N^2}$ in a sensing capacitor, which is introduced by the charge noise $\overline{Q_N^2}$, is [40],

$$\overline{C_N^2} = \frac{\overline{Q_N^2}}{V_{EXE}^2} = \frac{kT(C_P + C_{FT})}{V_{EXE}^2} \quad (7)$$

Equation (8) indicates that the high-voltage excitation V_{EXE} is helpful to reduce the noise.

Thus, the excitation circuit of the readout circuit is designed with high-voltage devices to achieve low noise while the frontend DCV and CMCV as well as the backend ADC are designed with low-voltage devices to achieve low power consumption [41]. In this work, the high voltage is 5.0V and the low voltage is 1.8V. The open-loop charge pump is designed with a cross coupled structure using 5.0V thick gate-oxide MOSFET, as shown in Fig. 3 [42]. The input voltage of the charge pump is the power supply voltage V_{DD} (1.8V) and the output voltage of the charge pump is the excitation voltage V_{EXE}. All the N-type MOSFET in the charge pump are isolated by deep N-well whose potential is supplied by the voltage V_{EXE}. When the open-loop charge pump is loaded with a synchronized switched-capacitor network, the output voltage of the charge pump is,

$$V_{EXE(FL)} = \frac{V_{EXE(ZL)}}{1 + 2C_L/C_{CP}};\ V_{EXE(ZL)} = 3V_{DD} \quad (8)$$

where C_L is the load capacitance, C_{CP} is the boost capacitor, $V_{EXE(ZL)}$ is the ideal output of charge pump when zero load capacitance is applied. Hence, the capacitance C_{CP} is designed to be far larger than C_L to guarantee that the $V_{EXE(FL)}$ is a high

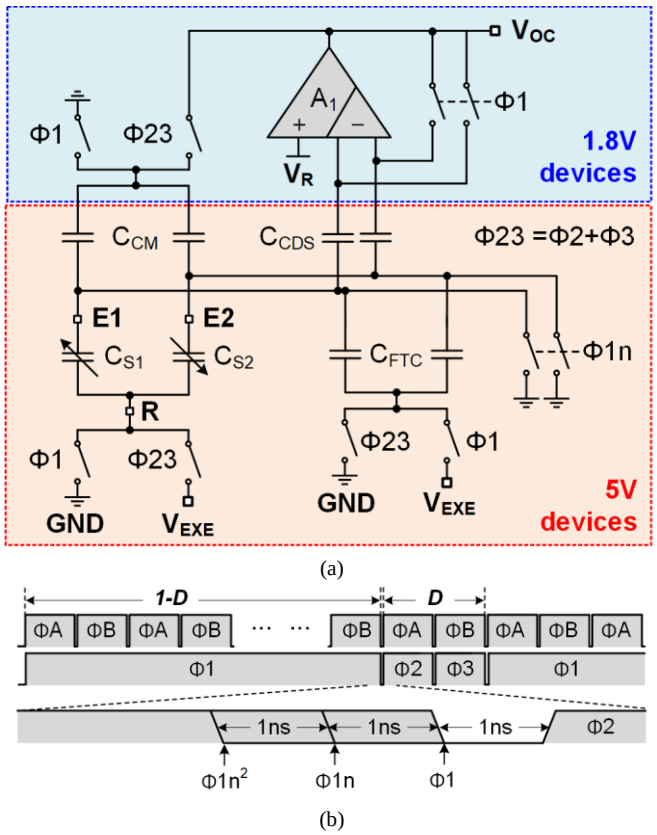


Fig. 4. Schematic of the CMCV. (a) Schematic. (b) timing diagram.

voltage. Equation (9) indicates that the excitation voltage V_{EXE} is a function of the load capacitance and the variation of $V_{EXE(FL)}$ is therefore inevitable. However, this is not a problem as both the gain and nonlinearity of the VCR readout structure are insensitive to the variation of the excitation voltage V_{EXE}, according to the equation (7).

B. CMCV

The function of CMCV is to convert the common-mode charge of the capacitances C_{S1} and C_{S2} to the voltage signal V_{OC}, as indicated in the expression (6). The schematic and typical transient waveform of the CMCV are shown in Fig. 4(a) and Fig. 4(b). The CMCV has to address the following two nonlinearity issues which limit the improvement of dynamic range: 1) The nonlinearity introduced by the feedthrough capacitance C_{FT} [36] and 2) The nonlinearity introduced by electrostatic force unbalance.

Considering the nonlinearity introduced by C_{FT}, $D_{O2}(x)$ in the ratiometric trans-function (7) becomes $D_{OFT}(x)$.

$$D_{OFT}(x) = \frac{C_{S1}(x) - C_{S2}(x)}{C_{S1}(x) + C_{S2}(x) + 2C_{FT}} \frac{C_{CM}}{C_D} \tag{9}$$

Combining the equations (1) and (10),

$$D_{OFT}(x) = \frac{(1-\alpha_1)x}{1-\alpha_1 x^2} \frac{C_{CM}}{C_D};\ \alpha_1 = \frac{C_{FT}}{C_{FT}+C_0} \tag{10}$$

The linear gain of $D_{OFT}(x)$ is $(1-\alpha_1)x$. Thus, the percentage nonlinearity of the ratiometric trans-function considering C_{FT} is,

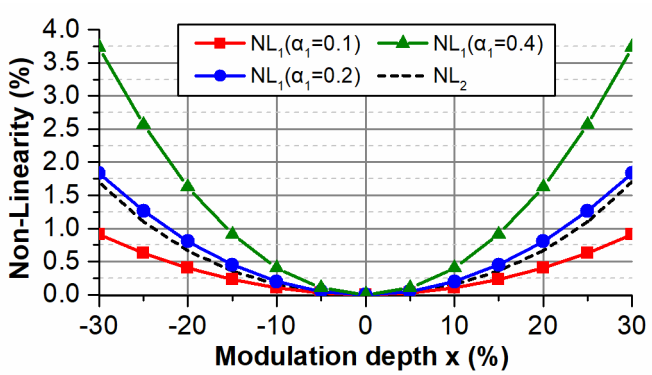


Fig. 5. Numerical analysis of the nonlinearities caused by reciprocal trans-function (NL_1) and electrostatic force unbalance (NL_2).

$$NL_1 = \frac{F_E(x) - (1-\alpha_1)x}{(1-\alpha_1)x} \frac{C_{CM}}{C_D} = \frac{\alpha_1 x^2}{1-\alpha_1 x^2} \frac{C_{CM}}{C_D}$$
$$\alpha_1 = \frac{C_{FT}}{C_{FT}+C_0} \tag{11}$$

Equation (12) shows that a small ratio of the feedthrough capacitance C_{FT} to the rest capacitance C_0 is helpful to reduce the nonlinearity. Hence, the CMCV employs the capacitors C_{FTC} as shown in Fig. 5(a) to cancel out the capacitance C_{FT}. The capacitance C_{FTC} is driven by the phase opposite to the driving phase of the sensing capacitances C_{S1} and C_{S2}, i.e., the C_{FTC} is driven to V_{EXE} by the phase Φ1 while the C_{S1} and C_{S2} are driven to V_{EXE} by the phase Φ23.

The nonlinearity introduced by electrostatic force unbalance is discussed as follows. During the period $(1-D)$, there is no voltage difference applied to the sensing capacitances C_{S1} and C_{S2}. So there is no electrostatic force unbalance introduced. During the period (D), a voltage difference V_{EXE} is applied to the sensing capacitances C_{S1} and C_{S2} and an electrostatic force unbalance $F_E(x)$ is introduced.

$$F_E(x) = \frac{1}{2} D {V_{EXE}}^2 \left(\frac{C_{S1}(x)}{d_1(x)} - \frac{C_{S2}(x)}{d_2(x)} \right)$$
$$d_1(x) = d_0(1-x);\ d_2(x) = d_0(1+x) \tag{12}$$

The linear mechanical force produced by spring in MEMS sensing element is,

$$F_K(x) = k d_0 x \tag{13}$$

where k is the spring constant. Thus, the percentage nonlinearity caused by electrostatic force unbalance is,

$$NL_2 = \frac{F_E(x) - F_K(x)}{F_K(x)} = \alpha_2 \left[\frac{2x^2 + x^4}{(1-x^2)^2} \right]$$
$$\alpha_2 = \frac{2D{V_{EXE}}^2 C_0}{k d_0^2} \tag{14}$$

According to the equation (15), an effective way to reduce the nonlinearity caused by electrostatic force unbalance is to reduce the duty cycle D of excitation voltage.

The numerical analyses of NL_1 and NL_2 are shown in Fig. 5, in which the typical conditions are $D = 1/16$, $V_{EXE} = 5.4\text{V}$,

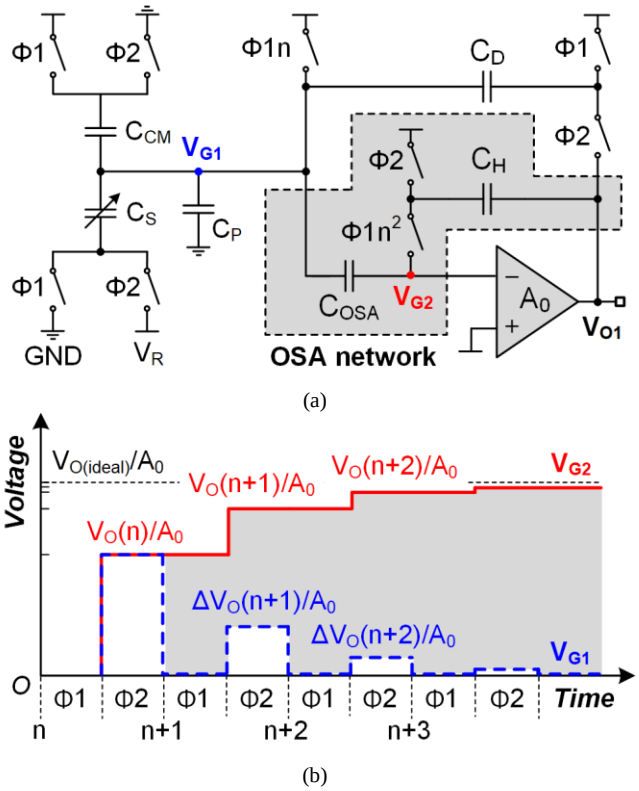


Fig. 6. The DCV employing OSA technique [13]. (a) Schematic. (b) Typical transient voltage waveform.

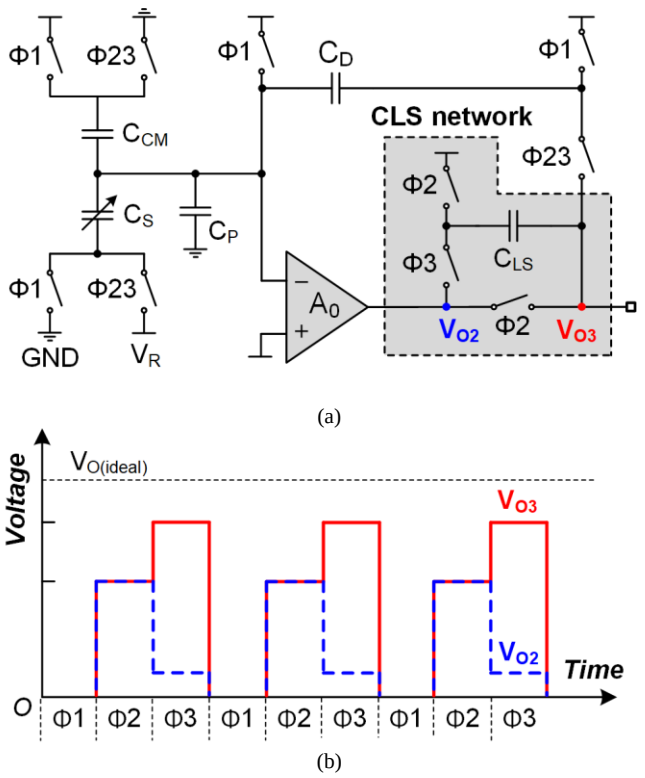


Fig. 7. The switched-capacitor amplifier employing CLS technique [43][44]. (a) Schematic. (b) Typical transient voltage waveform.

$C_0 = 300\text{fF}$, $k = 1\text{N/m}$ and $d_0 = 2\mu\text{m}$. When the capacitance C_{FT} is smaller than 75fF (or $\alpha_1 < 0.2$), the system nonlinearity becomes dominated by NL_2 as x increases. So the reduction of electrostatic force unbalance is essential. The minimum electrostatic force unbalance is determined by the minimum duty cycle D which is limited by the maximum bandwidth of the amplifiers used in the CMCV and DCV. When the capacitance C_{FT} is larger than $75fF$ (or $\alpha_1 > 0.2$), the system nonlinearity becomes dominated by NL_1 as x increases. So the cancellation of C_{FT} is essential. The minimum residual C_{FT} after cancellation depends on the manufacturing accuracy of the capacitance C_{FTC}.

C. DCV

The function of DCV is to convert the differential charge of the capacitances C_{S1} and C_{S2} to the voltage signal V_{OD}, as indicated in the expression (6). The DCV has to address the following two inaccuracy issues: 1) The gain error deterioration due to the parasitic capacitance C_P and 2) The nonlinearity due to the limited output swing of amplifier. The oversampling successive approximation (OSA) readout technique was reported to deal with the first issue [13][43]. The correlated level shifting (CLS) technique was reported to deal with the second issue [44]-[46]. In this work, the OSA-CLS technique which combines the OSA with the CLS is proposed, in order to address both issues simultaneously.

The simplified single-end circuit model of the OSA-based DCV is shown in Fig. 6(a) [13]. The network composed of the capacitors C_{OSA} and C_H provides highly accurate virtual ground, therefore minimizing the gain error deterioration. The process is illustrated by Fig. 6(b). During the step n, the virtual ground error $V_{G1}(n)$ is $V_O(n)/A_0$. This error $V_{G1}(n)$ is then sampled and cancelled out during the step $n+1$ by the capacitor C_{OSA}. Thus, the output during the step $n+1$ can achieve a more accurate level $V_O(n+1)$ and produce a new but smaller virtual ground error $V_{G1}(n+1) = \Delta V_O(n+1)/A_0$. This process iterates until the virtual ground error is sufficiently absorbed by the capacitors C_{OSA} and reduced to near zero (V_{G1}). As a result, the output can approximate to the ideal level $V_{O(ideal)}$ after multiple steps but at cost of longer settling time.

The simplified single-end circuit model of the CLS-based DCV is shown in Fig. 7 [44]. During the reset phase Φ1, capacitors are set to zero. During the "estimate phase" Φ2, the amplifier produces a coarse output which is sampled by the capacitor C_{LS}. During the "level shifting phase" Φ3, the capacitor C_{LS} is inserted between the output terminal of the amplifier and the load to enhance the output swing of the amplifier.

The schematic of the OSA-CLS-based DCV is shown in Fig. 8(a), in which the OSA operation and the CLS operation are interleaved, as shown in Fig. 8(b). The CLS operation in Fig. 8 is the same as the CLS operation in Fig. 7. Between two CLS steps, an OSA operation is inserted. The gain error is sampled during the phase Φ1 of the OSA operation and cancelled out during the phase Φ3 of the next OSA operation.

The transistor-level simulation results are shown in Fig. 9, where the traditional DCV (from [9]), the OSA-based DCV (Fig. 6), the CLS-based DCV (Fig. 7) and the OSA-CLS-based DCV (Fig. 8) are considered. The values of the key capacitors are $C_P = 4\text{pF}$, $C_{OSA} = 4\text{pF}$, $C_{LS} = 2\text{pF}$, $C_H = 0.5\text{pF}$, $C_{CM} = 1.0\text{pF}$, $C_S = 0.3\text{pF}$, $C_{FT} = 0.2\text{pF}$ and $C_D = 20\text{fF}$. The

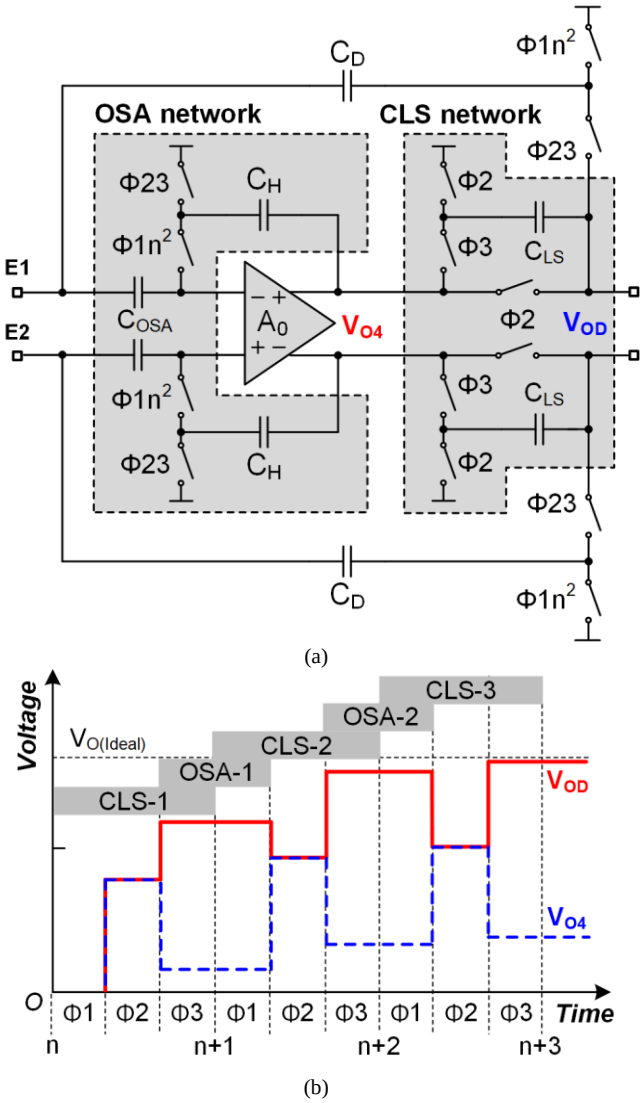


Fig. 8. The proposed DCV employing OSA-CLS technique. (a) Schematic. (b) Typical transient voltage waveform.

amplifier used is conventional folded-cascode amplifier. The nonlinearity is calculated by the difference between the maximum gain error and the minimum gain error over the full output swing (±100% in Fig. 9). For example, the maximum and minimum gain errors of the traditional DCV are 33% and 9.0%, respectively. Then the nonlinearity of the traditional DCV is 24 % (33%-9.0%). The maximum gain errors of the OSA-based DCV, the CLS-based DCV and the OSA-CLS-based DCV are 11%, 4.0% and 0.09%, respectively. The minimum gain errors of the OSA-based DCV, the CLS-based DCV and the OSA-CLS-based DCV are 0.1%, 0.9% and 0.02%, respectively. Thus, the nonlinearities of the OSA-based DCV, the CLS-based DCV and the OSA-CLS-based DCV are 10.9%, 3.1% and 0.07%, respectively. That is to say, the OSA-CLS technique achieves significantly lower gain error and nonlinearity than the other circuits do. The overall low gain error of the OSA-CLS-based DCV is due to the fact that it benefits from its 3rd-order infinitesimal of the amplifier's gain A_0, while the gain errors of the OSA-based DCV and the CLS-based DCV are the 2nd-order infinitesimal of the amplifier's gain A_0, as shown in the table I. The low

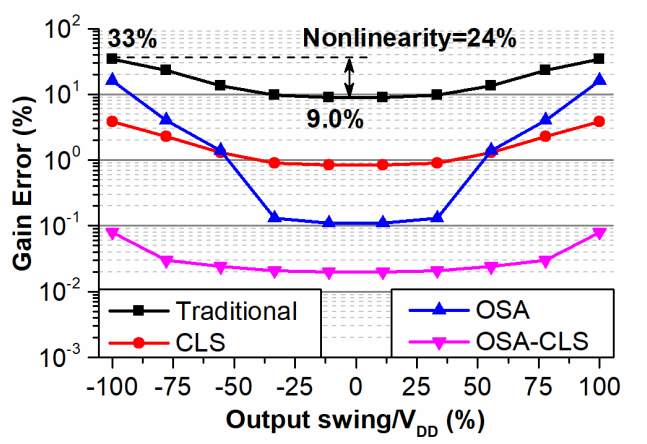


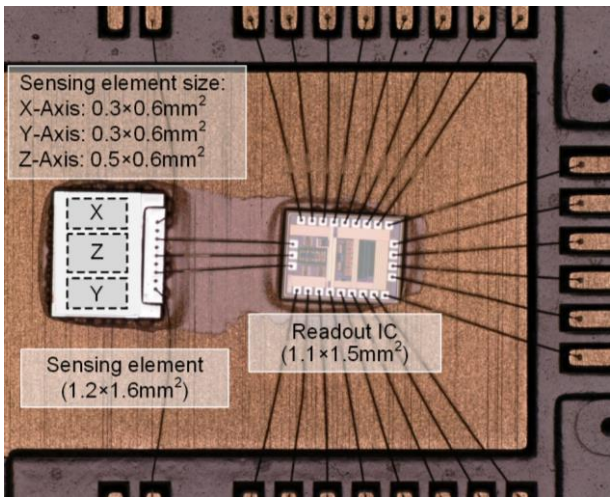
Fig. 9. Transistor-level simulation results of the gain error under full output swing, where traditional DCV, CLS-based DCV, OSA-based DCV and OSA-CLS-based DCV are considered.

TABLE I COMPARISON OF TRANS-FUNCTION OF READOUT CIRCUITS

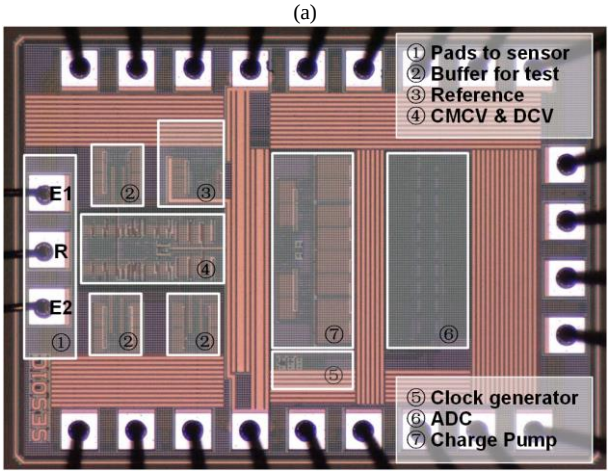
	Normalized trans-function	Order
Traditional DCV [9]	$1-\frac{1}{1+\beta A_0}$	1
OSA based DCV [13]	$1-\frac{1}{1+A_0(1+A_0)\beta}$	2
CLS based DCV [44]	$1-\frac{1}{(1+\beta A_0)^2}$	2
OSA-CLS based DCV	$1-\frac{1}{(1+A_0)(1+\beta A_0)^2}$	3

nonlinearity of the OSA-CLS-based DCV results from the CLS operation. The detailed derivations of the trans-functions in the table I can be found in Appendix.

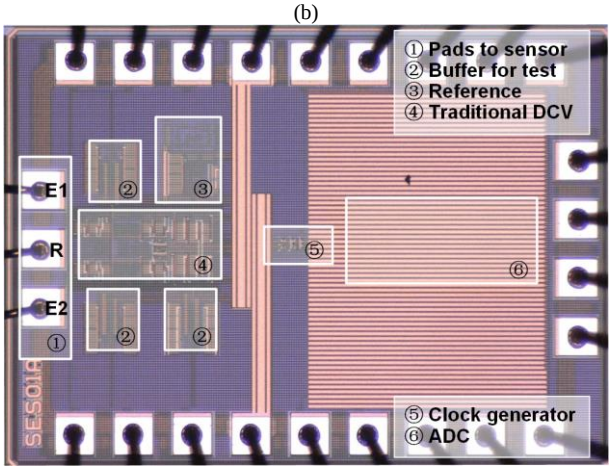
The reason why the 3rd-order DCV is employed instead of the 2nd-order DCV is explained as follows. The linearity of the whole accelerometer stems from both the sensing element and the gain variation. For the nonlinearity resulted from the sensing element, it is compensated by the ratiometric transfer function, but due to the limited manufacturing accuracy of the capacitance C_{FTC} in Fig. 4, the typical residual nonlinearity from the sensing element after compensation remains above 1%. For the nonlinearity resulted from the gain variation, it can be reduced by employing the OSA-based DCV or OSA-CLS-based DVC. However, the OSA-based DCV with 2nd-order gain variation attenuation can achieve only 3.1% nonlinearity, while the OSA-CLS-based DCV with 3rd-order gain variation attenuation can achieve 0.07% nonlinearity. Therefore, if 3rd-order technique is adopted, the overall nonlinearity of the whole accelerometer is determined predominately by the nonlinearity stemmed from the sensing element and it remains low. In contrast, if only 2nd-order technique is adopted, the overall nonlinearity of the whole accelerometer is determined by the nonlinearities stemmed from both the sensing element and the gain variation and it is significantly higher than that determined only by the nonlinearity stemmed from the sensing element.



(a)



(b)



(c)

Fig. 10. The photographs of the readout circuits. (a) photograph of test PCB. (b) micrograph of die of the proposed voltage control ratiometric readout circuit. (c) micrograph of die of the traditional voltage control readout circuit.

IV. Physical Verification

The VCR readout circuit is prototyped with a commercial 0.18um 1.8V/5.0V CMOS process and tested with a 3-axis sensing element which has a size of 1.2mm×1.6mm from a commercial MEMS accelerometer [5], as shown in Fig. 10(a). The 3-axis sensing element is comprised of X-axis sensing element (0.3mm×0.6mm), Y-axis sensing element (0.3mm×0.6mm) and Z-axis sensing element (0.5mm×0.6mm). Only the X-axis sensing element is used in this test to demonstrate VCR technique, as other axes of the sensing element will produce similar results. The VCR readout circuit includes excitation circuit (open-loop charge pump), CMCV, DCV (Fig. 9), ADC, clock generator, reference generator and output buffers, as shown in Fig. 10(b). The traditional voltage control readout circuit (from [9]) is also fabricated using the same CMOS process and tested with the same sensing element in order to provide more comparable results. For the purpose of test, the circuit includes traditional DCV, ADC, clock generator, reference generator and output buffers, as shown in Fig. 10(c). The amplifiers used in DCV and CMCV are folded-cascode amplifier and the ADC used is a conventional 10-bit set-and-down SAR ADC whose schematic can be found in the work [47].

The DC acceleration sweep measured on a vibration table for both the VCR readout circuit and the traditional readout circuit

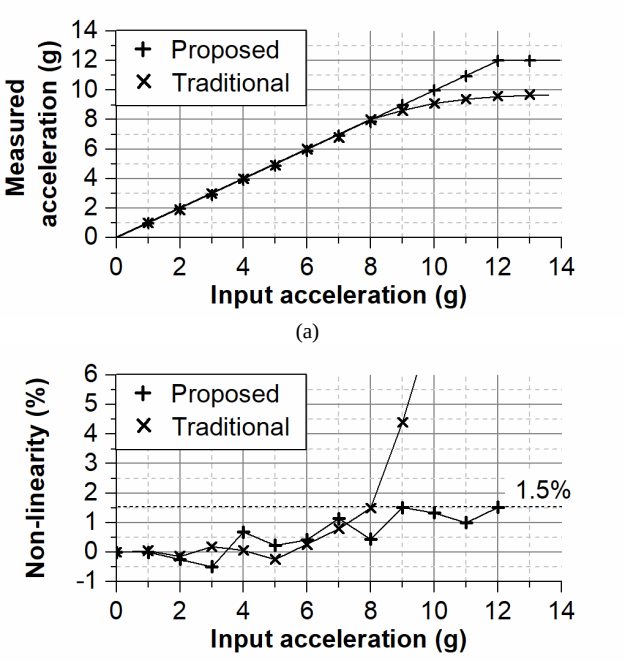


Fig. 11. DC acceleration sweep measured on a vibration table. (a) Output signal of traditional readout circuit and proposed readout circuit. (b) Residual nonlinearity of the proposed readout circuit.

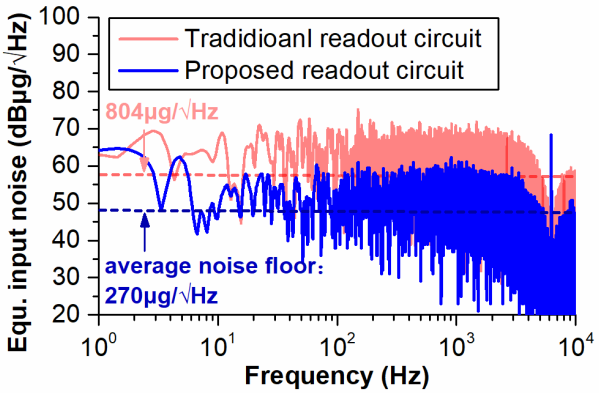


Fig. 12. The measurement transient waveform and 65,535 point FFT of the output noise of the readout circuit.

TABLE II COMPARISON OF READOUT CIRCUITS FOR MEMS CAPACITIVE SENSOR

	Amini [9]	Sun [10]	Paavola[14]	Zhong[32]	Traditional†	**This work††**
Dynamic range (dB)*	54	67	66	37	44	**57**
Full scale (g)	±1	±11.5	±4	±8	±8	**±12**
Nonlinearity (%)	-	-	0.3	1.0	1.5	**1.5**
Bandwidth (Hz)	10k	10k	25	10k	2.5k	**2.5k**
Sampling rate (Hz)	-	-	51.2k	100k	5.0k	**5.0k**
Sensor sens. S_{AC} (fF/g)	200	-		1.0	4.0	**4.0**
Noise floor $(\mu g/\sqrt{Hz})$	16	40	275	900	804	**270**
Power (μW)	6,000	1,000	97.6	248	123	**147**
Supply (V)	2.5	-	1.2	1.8	1.8	**1.8**
FoM_1 (pJ)	1,202	43.5	1,681	350	310	**83**
FoM_2 $(\mu W \cdot \mu g/Hz)$	960	400	5,365	2,230	1,977	**796**
Process	0.25μm CMOS	CMOS-MEMS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	**0.18μm CMOS**
Sensing element size (mm)	5×5×0.04	1.29×1.29×0.05	-	0.3×0.6×0.03	0.3×0.6×0.03	**0.3×0.6×0.03**

*Calculated by: $DR = Full\ scale/(noise\ floor \times \sqrt{Bandwidth \times \pi/2})$.
† Measured from the traditional readout circuit in Fig. 12(c) which was fabricated using the same CMOS process and tested with the same sensing element as for the VCR readout circuit. †† Measured from the circuit in Fig. 12(b). Data is measured at room temperature (27°C).

is shown in Fig. 11(a). The nonlinearity of both readout circuits is shown in Fig.11(b). The full input signal range of the VCR readout circuit is ± 12g with a nonlinearity of 1.5%, while the full input signal range of the traditional readout circuit is $\pm 8g$ with a nonlinearity of 1.5%. Thus, the full input signal range is improved by 3.5dB (from ± 8g to ± 12g). The equivalent input noise power spectral density (PSD) of the VCR readout circuit and the traditional readout circuit is shown in Fig. 12, in which the average equivalent input noise floors of both readout circuits are $270\mu g/\sqrt{\text{Hz}}$ and $804\mu g/\sqrt{\text{Hz}}$, respectively. Thus, the noise floor is improved by 9.5dB (from $804\mu g/\sqrt{\text{Hz}}$ to $270\mu g/\sqrt{\text{Hz}}$). As a result, compared to that of the traditional readout circuit, the dynamic range of the VCR readout circuit is improved by 13.0 dB (3.5 dB signal input range improvement and 9.5dB noise floor improvement).

In the VCR readout circuit, the power consumptions of the main blocks DVC and CMCV, ADC, reference, charge pump and clock generator are 90μW, 30μW, 22μW, 4μW and 1μW, respectively, totaling 147μW. In the traditional readout circuit, the power consumptions of the main blocks DCV, ADC, reference and clock generator are 70μW, 30μW, 22μW and 1μW, respectively, totaling 123μW. Therefore, compared to the traditional readout circuit, the VCR readout circuit has a power consumption increase of 19.5% (from 123μW to 147μW) due to the employment of the CMCV and the charge pump.

Generally, there are two main types of figure of merit (FoM) used to evaluate the power efficiency of MEMS accelerometer[14][24][32],

$$FoM_1[W \cdot F/Hz] = \frac{Power}{Dynamic\ range \times Bw} \quad (15)$$

or,

$$FoM_2[W \cdot F/Hz] = \frac{Power \times Noise\ floor}{\sqrt{Bw}} \quad (16)$$

The FoM_1 emphasizes on the voltage efficiency, i.e., to increase the signal range with as little increment of supply voltage as possible. The FoM_2 emphasizes on the current efficiency, i.e., to reduce the noise floor with as little increment of supply current as possible[32]. According to the equations (16) and (17) as well as the measurement results, the VCR readout circuit significantly improves FoM_1 from 310pJ to 83pJ and FoM_2 from $1{,}977\mu W \cdot \mu g/Hz$ to $796uW \cdot \mu g/Hz$ compared with the traditional readout circuit.

In order to present more comparable results, the table II also shows the comparison between this work and other similar voltage control readout circuits reported in [9], [10], [14] and [32]. Compared with other works apart from the work [10], this work provides the best FoM_1 and FoM_2. The work [10] employs CMOS-MEMS process to reduce the parasitic capacitance C_P, therefore achieving low noise floor (according to the equation (8)) and good FoM. However, this process is not compatible with traditional CMOS fabrication process. The dynamic range of this work is better than others except for [10] and [14]. The dynamic range of work [10] benefits from low noise floor due to use of CMOS-MEMS process. The work [14] employs oversampling technique to achieve high dynamic range, which however results in low bandwidth and very poor power efficiency (FoM_1 and FoM_2). The noise floor of the works [9] and [10] are better than this work. This is because the dimensions of the sensing element used in works [9] (5mm×5mm×40μm) and [10] (1.29mm×1.29mm×50μm) are far larger than that (0.3mm×0.6mm×30μm) used in these works. The nonlinearity of this work is slightly deteriorated, compared to the work [32] which uses the similar sensing element to that of this work. This is due to the inaccuracy of the C_{FT} cancelation, as explained in Section III-B.

V. CONCLUSIONS

For open-loop MEMS accelerometer, the voltage control readout structure can achieve low cost and low power consumption but suffers from low dynamic range and low power efficiency (FoM) compared to the charge control readout structure. These problems can be alleviated by the proposed voltage control ratiometric (VCR) readout structure. Compared to the traditional voltage control readout circuit fabricated with the same process and tested with the same

sensing element, the proposed VCR readout circuit improves the dynamic range by $13.0dB$ $(from\ 44.0dB\ to\ 57.0dB)$ and improves the FoM_1 from 310pJ to 83pJ and the FoM_2 from $1{,}977\mu W \cdot \mu g/Hz$ to $796uW \cdot \mu g/Hz$. Compared with the other voltage control readout circuits reported recently, this work still achieves favorable outcomes in terms of both FoM and dynamic range.

APPENDIX: DERIVATION OF THE EXPRESSIONS IN TABLE I

Practically, "holding error" is the most important non-ideality to be considered in the OSA-based readout circuit. As shown in Fig. 13(a), during the phase Φ2, the output V_{O1} is sampled by the capacitor C_H. Then during the phase Φ1 that follows, the capacitor C_H holds the output V_{O1}. As the left plate of C_H is switched from the reference to V_{G2} during the phase Φ1, the output level V_{O1} is changed by the amount of ΔV_{HE} which is called "holding error".

$$\Delta V_{HE} = V_{G2(\phi 1)} \tag{1}$$

ΔV_{HE} is illustrated in Fig. 13(b). Considering the holding error, the output is,

$$V_{O1(\phi 1)} = V_{O1(\phi 2)} - \Delta V_{HE} \tag{2}$$

where $V_{O1(\phi 1)}$ and $V_{O1(\phi 2)}$ are the outputs during the phase Φ1 and the phase Φ2, respectively. V_{G2} is the voltage across the input terminals of amplifier and it is in proportion to the output voltage,

$$V_{G2(\phi 1)} = V_{O1(\phi 1)}/A_0 \tag{3}$$

By combining the equations (1) to (3), the holding error is,

$$\Delta V_{HE} = V_{O1(\phi 2)}/(1 + A_0) \tag{4}$$

This holding error produces a virtual ground error V_{G1} at the input terminal,

$$V_{G1} = \frac{\Delta V_{HE}}{A_0} = \frac{V_{O1(\phi 2)}}{A_0(1 + A_0)} \tag{5}$$

According to the charge conservation law, the expression for the output voltage of the OSA-based DCV shown in Fig. 7(a) considering the virtual ground error V_{G1} is,

$$V_R(C_S - C_{CM}) - V_{G1}(C_S + C_{CM} + C_P) = V_{O1(\phi 2)}C_D \tag{6}$$

By combining the equations (5) and (6),

$$V_{O1} = V_{O(ideal)}\left[1 - \frac{1}{1 + A_0(1 + A_0)\beta}\right]$$
$$V_{O(ideal)} = \frac{V_R(C_S - C_{CM})}{C_D}; \beta = \frac{C_D}{C_P + C_S + C_{CM}} \tag{7}$$

where $V_{O(ideal)}$ is the ideal output and β is the feedback coefficient.

The CLS-based DCV shown in Fig. 8(a) outputs the estimated result in the phase Φ2 and outputs the final result in the phase Φ3. The estimated output considering the gain error in the phase Φ2 is,

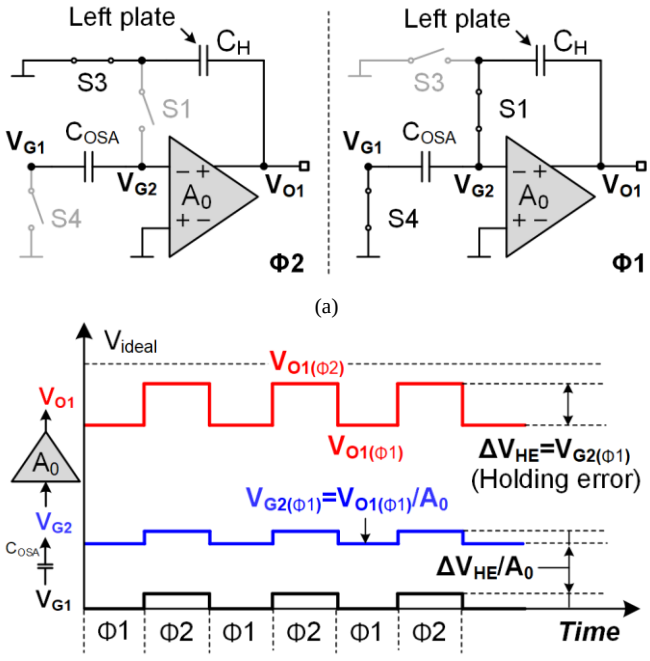


Fig. 13. Simplified model to consider "holding error" in OSA readout circuit. (a) The circuit model. (b) The analytic waveform.

$$V_{O3(\phi 2)} = V_{O(ideal)} - V_{O3(\phi 2)}/\beta A_0 \tag{8}$$

During the phase Φ3, the output swing is reduced by $V_{O3(\phi 2)}$, thus the final output considering the gain error in the phase Φ3 is,

$$V_{O3(\phi 3)} = V_{O(ideal)} - (V_{O3(\phi 3)} - V_{O3(\phi 2)})/\beta A_0 \tag{9}$$

By combining the equations (8) and (9),

$$V_{O3} = V_{O(ideal)}\left[1 - \frac{1}{(1 + \beta A_0)^2}\right]$$
$$V_{O(ideal)} = \frac{V_R(C_S - C_{CM})}{C_D}; \beta = \frac{C_D}{C_P + C_S + C_{CM}} \tag{10}$$

The OSA-CLS-based DCV shown in Fig. 9(a) executes CLS during the phases Φ2 and Φ3 and executes OSA during the phases Φ3 and Φ1. According to the equation (9) in CLS process, the amplifier's output swing $V_{O4(\phi 3)}$ during the phase Φ3 is,

$$V_{O4(\phi 3)} = V_{O(ideal)}\frac{\beta A_0}{(1 + \beta A_0)^2} \tag{11}$$

According to the equation (5) in OSA process, the virtual ground error during the phase Φ3 is determined by the amplifier's gain A_0 and the amplifier's output swing $V_{O4(\phi 3)}$,

$$V_{G1} = \frac{V_{O4(\phi 3)}}{A_0(1 + A_0)} \tag{12}$$

According to the charge conservation law, the output voltage considering the virtual ground error V_{G1} is,

$$V_R(C_{S1} - C_{S2}) - V_{G1}(C_S + 2C_{CM} + C_P) = V_{OD}C_D \tag{13}$$

By combining the equations (10) to (13), the expression for the

output voltage of the OSA-CLS-based DCV is,

$$V_{OD} = V_{O(ideal)}\left[1 - \frac{1}{(1+A_0)(1+\beta A_0)^2}\right]$$
$$V_{O(ideal)} = \frac{V_R(C_{S1} - C_{S2})}{C_D}; \beta = \frac{C_D}{C_P + C_S + C_{CM}} \quad (14)$$

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