An integrated circuit to enable electrodeposition and amperometric readout of sensing electrodes

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***Abstract*—This paper presents the design of an integrated circuit (IC) for (i) electrochemical deposition of sensor layers on the on-chip pad openings to form sensing electrodes, and (ii) amperometric readout of electrochemical sensors. The IC consists of two main circuit blocks: a Beta-multiplier based current reference for galvanostatic electrodeposition, and a switch-capacitor based amperometric readout circuit. The circuits are designed and simulated in a 180-nm CMOS process. The reference circuit generates a stable current of 99 nA with a temperature coefficient of 141 ppm/°C at best and 170 ppm/°C on average (across corners) over a supply voltage range of 1.2-2.4 V, and a line regulation of 0.7 %/V. The readout circuit measures current within ±2 μA with 99.9% linearity and a minimum integrated input-referred noise of 0.88 pA.**

***Keywords*—current reference, subthreshold region, sensor fabrication, potentiostat, switch capacitor.**

I. Introduction

Electrochemical sensors play an important role in a variety of applications such as environmental monitoring, medical diagnosis and clinical investigation which have evolved rapidly over the past decade [1]. They typically utilize a three-electrode system with amperometric measurement technique [2], in which the sensor reaction current is proportional to the analyte concentration. Compared with optical measurement techniques, electrochemical biosensors allow simple operation in complex analyte and direct electrical signal measurement without expensive external instruments. The popularity of electrochemical sensors also stems from their miniaturization potential and high sensitivity to target biomolecules [3]. The miniaturization enables the establishment of large-scale sensor arrays and parallel detection of multiple biomolecules, whilst batch manufacturing makes the system more cost-effective.

The complementary metal-oxide-semiconductor (CMOS) chip is an outstanding platform for a silicon-based lab-on-chip solution due to the fabrication compatibility between the CMOS technique and many bio/chemical biosensor interfaces [4]. Monolithic integration of sensors on CMOS provides more value such as high scalability for parallel sensing. To physically integrate electrochemical biosensors with their instrumentation, a silicon-based chip containing the instrumentation circuit can serve as the substrate for the electrochemical biosensors.

The sensing and the signal processing parts are usually developed on separate substrates and connected using wires, leading to interferences and limiting the scalability. The benefit of signal path reduction to micron size can only be achieved when sensing takes place on the surface of CMOS ICs [5]. To develop an amperometric electrochemical sensor directly on CMOS, the exposed top metal layer may be used as the base on which sensor layers may be deposited. The fabrication of on-chip sensors is achieved through methods such as electroless deposition [6], photolithography [1] and electrodeposition using external instruments [3]. Electroless deposition requires no electrical connection but lacks repeatability. Photolithography uses bulky external instrument and often requires manual handling, similar to the electrodeposition techniques. To produce scalable, low-cost and autonomous sensing devices on CMOS, we propose to implement the electrodeposition technique on chip. This allows, through programming a few parameters on the IC, the generation of the required current and voltage profiles for the deposition of various metallic and nanostructure layers when immersed in dedicated chemical solutions.

The fundamental layers of an electrochemical sensor for detection of small biomolecules may include adhesion layer, inert metallic layer, nano-structure layers, and bio-recognition layer. The majority of these layers can be electrochemically deposited onto metallic surfaces using potentiostatic [7] or galvanostatic [8]-[12] techniques. In particular, galvanostatic electrodeposition has been reported in the literature for gold [8], porous copper [9], nickel [10], silver nanostructures [11] and Prussian blue [12]. This paper introduces an integrated system on CMOS technology for the galvanostatic electro-deposition of key sensor layers, and the amperometric readout of the sensor. The following section introduces the system architecture and the design of different circuit blocks. In section III the simulation results in a 180 nm CMOS technology are presented. The conclusions are presented in Section IV.

II. System Design

A. System specification

One of the most important parameters in a galvanostatic deposition is the amount of the fixed current applied to the electrode. The reported current density for the deposition of the key metallic and nanostructure layers mentioned above is from 0.05 to 5 A/cm^2 [9] – [12]. It is shown that a 10-20% variation in the current density can be tolerated or be offset by adjusting the electrodeposition time [7]. Selecting the size of the on-chip electrodes to be between 10×10 to 50×50 μm^2, the on-chip electrodeposition circuit needs to produce various currents between 100 nA to 10 μA with an error of less than 20%.

The readout circuit is designed to allow sensor readout in some of the most common electrochemical readout techniques including chronoamperometry, cyclic voltammetry (CV), and differential pulse voltammetry. These methods typically involve applying various voltage profiles between the working and reference electrodes and reading the current of the working

electrode which may be bidirectional. The range of the sensor current depends on the recognition element and the surface morphology of the electrode, among others. The sensor current range with the above-mentioned dimension can be estimated based on the equation in [13] to be within ±2 µA. A sub-pico ampere noise level is desirable to allow high-resolution readout.

B. System architecture

The electrodeposition and the readout circuits are designed to interface an on-chip electrode array through a multiplexer. The electrode array consists of a common reference electrode (RE), a common counter electrode (CE) and a 4×4 array of working electrodes. Fig.1. shows the high-level block diagram of the proposed circuit. One working electrode (WE) is connected to the readout circuit or the electrodeposition circuit at any given time, while other WEs are kept floated. A Beta-multiplier based current reference is designed to produce a constant current of 100 nA for galvanostatic electrodeposition. Currents above 100 nA are then generated when needed using multi-stage digitally controlled current mirrors. A conventional switch-capacitor trans-impedance amplifier (SC-TIA) is designed to measure the bidirectional current of the sensor.

The CE and RE are controlled using an amplifier in negative feedback, also known as potentiostat. The potentiostat helps in maintaining a given voltage on the RE by adjusting the current flowing through the CE. The current reference (block A) and the amperometric readout circuit (block B) are connected to the WE through a 16-to-1 multiplexer.

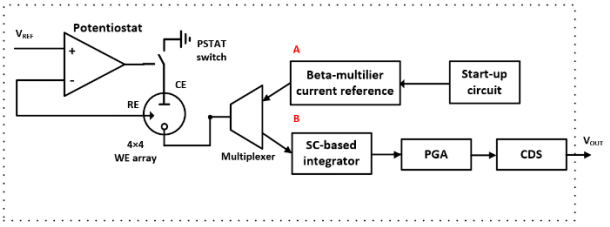

Fig.1. High-level block diagram of the integrated circuit for fabrication and readout of on-chip sensor.

C. Current reference circuit

The design is based on a Beta-multiplier current reference, to generate a fixed current of 100 nA to achieve a moderate power consumption and temperature coefficient. Beta-multiplier current references to generate nano-ampere range currents have been presented [14]-[17], however the power dissipation of these circuits is in the µW range, and they show a relatively large temperature dependence. Our design addresses these problems and generates a temperature-stable current over a wide power supply range. Fig. 2 shows the schematic view of the circuit, all transistors except M3 and M4 are biased to work in the sub-threshold region to reduce the power consumption. The conventional resistor in the Beta-multiplier is replaced by a transistor (M3) biased in the linear-region to reduce the area overhead, as in [15]. The diode-connected transistor (M4) provides the bias gate voltage for M3. M5-M7 achieve a start-up circuit to avoid the stable state in the zero current operating point. M6 behaves like a switch, turns on and starts the current feedback loop in the Beta-multiplier circuit from the steady-state. M6 will turn off once the circuit works in the desired state. A cascode configuration increases the output impedance of the current source and thus improves the isolation of power supply.

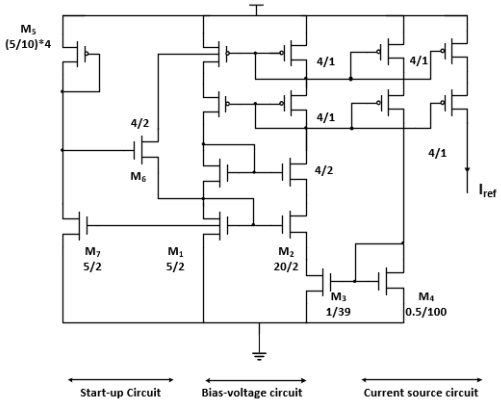

Fig. 2. Schematic of current reference circuit.

The reference current, I_{ref}, can be calculated as follows, assuming M1 and M2 are in weak inversion and their threshold voltages (as well as those of M3 and M4) are equal to each other , and the drain currents of M3 and M4 are equal and they work in the linear and saturation regions, respectively.

$$I_{ref} = \frac{2K_3^2 uc_{ox}\eta^2 V_T^2 \ln(K_2/K_1)^2}{K_4} \quad (1)$$

where K is the aspect ratio of the transistor, µ the electron mobility, C_{ox} the gate oxide capacitance, η the subthreshold slope factor of NMOS and $V_T = k_B T/q$ is the thermal voltage. The temperature dependence of the mobility is [18]:

$$\mu(T) = \mu(T_0)(T/T_0)^{-m} \quad (2)$$

where m is the temperature exponent of the electron mobility. The temperature exponent of the output current can be easily calculated from the V_T and µ formulas above to be 2-m. Although m is a process parameter, where possible, selecting a transistor with a maximum m allows minimizing the temperature dependency of I_{ref}. In this work, transistors with the largest m (1.8) in the X-FAB 180nm technology were selected leading to an overall temperature coefficient of 0.2 for the current reference.

D. Readout circuit

The most common methods to readout sensors are to use a resistive or a capacitive feedback trans-impedance amplifier (TIA) followed by an ADC [19]. For the resistive feedback TIA, to detect a pico-amp current, a large resistor is normally required which itself introduces a large amount of thermal noise into the measurement. The increased area overhead also makes the implementation of a multi-channel detector array impractical. Another common topology is a current-input ADC [20], but such a circuit can only measure unidirectional current. In this work, a switched-capacitor-based TIA is chosen as it can measure bidirectional input current and also low-pass filter part of the electrochemical noise through the integration phase.

The readout circuit has two main blocks: a capacitor feedback integrator and a SC-based programmable gain amplifier (PGA) as shown in Fig.3. The input current is integrated and converted to a voltage during the integration phase (φ_2=0, S_{int} open). During the reset phase (φ_2=1, S_{int} closed), C_{int} is discharged through S_{int}. The φ_1 and φ_2 are non-overlapping clocks at the

same frequency, f_s. The PGA amplifies the output voltage of the integrator with a gain that is proportional to the ratio of C_f and C_{in}. The correlated double sampling (CDS) scheme in the PGA provides 1/f noise and offset cancellation [21]. The output voltage of the readout circuit can be calculated as follows.

$$V_{OUT} = V_{CM} - \frac{I_{in}}{C_{\text{int}} f_S} \cdot \frac{C_{in}}{C_f} \quad (3)$$

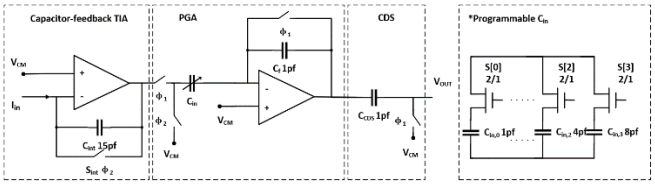

Fig. 3 Schematic of amperometric readout circuit.

where f_S is the reset frequency of S_{int} (assuming duty cycle of 50%) and I_{in} is the sensor current. The PGA gain and the clock frequency can be adjusted to support the readout of different input current range [3]. CMOS transmission gate switches are used to reduce the charge injection and on-state resistance.

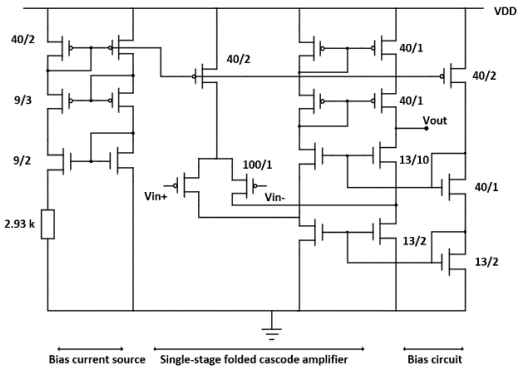

Fig. 4. Schematic of the folded-cascode amplifier used in the integrator, PGA, and potentiostat.

E. Amplifier

The folded-cascode amplifier structure is chosen for the potentiostat, PGA and the integrator circuits due to its high-gain and larger input common-mode range compared with ordinary telescopic amplifiers. A single-stage amplifier was chosen over two-stage structures here to ensure higher stability for various sensor loads (higher phase margin due to a single pole), short settling time and low power consumption [22]. PMOS transistors are used for the differential input pair and current mirror to decrease 1/f noise [23], as shown in Fig. 4.

III. Simulation Results

The schematic-level circuit is simulated in the 180nm CMOS process using Cadence V6.

A. Current reference

Corner simulations were performed to simulate the process variation of the circuit in the worst scenarios. Fig. 5. (a) shows the simulated output current I_{ref} as a function of temperature within 0-80°C at different process corners. The temperature coefficient is 169.6 ppm/°C on average. The results in Fig. 5. (a) shows the current level varies by 15% depending on the corner, while the temperature coefficient ranges from 141.3 (ws corner) to 202.3 ppm/°C (wp corner). This relatively low temperature coefficient was achieved through optimising the dimension of M3 and M4 as well as through selecting transistors with the largest mobility temperature exponent to minimise the overall tempretaure coefficient of I_{ref} as discussed in the previous section.

The temperature-dependence curves have a concave shape which is different from the theory presented in Eq.1. This may be caused by the difference in the simulated temperature dependency of mobility including high order nonlinear effect. Another reason could be the mismatch between the threshold voltage of M1 and M2 (or M3 and M4) due to the difference of their source-bulk voltages and dimensions, which were assumed equal to derive Eq.1.

Fig. 5. (b) shows the simulated current reference I_{ref} as a function of the power supply voltage at room temperature (27°C). For a supply ranging between 1.2 and 2.4 V, the current reference achieves the line regulation of 0.7 %/V. At supply voltages beyond 2.4 V, the start-up circuit will stay on and leak current into bias-voltage circuit which results in a slight increase of the output current.

Table I summarizes the simulated specifications of the current reference circuit and the comparison with other nA-size current references. Our circuit balances trade-offs among TC, power consumption and line regulation and achieves a superior overall performance.

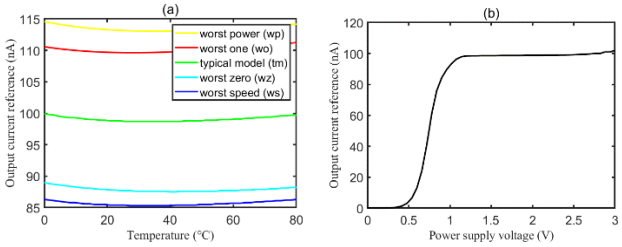

Fig. 5. (a) Simulated output current I_{OUT} as a function of temperature from four different corners. (b) Simulated output current I_{OUT} as a function of supply voltage.

TABLE I
COMPARISON WITH REPORTED NA-SIZE CURRENT REFERENCES

Specifications	This work*	[14]	[15]	[16]	[17]
Process, CMOS	180nm	350nm	2µm	180nm	350nm
V_{DD} (V)	1.2-2.4	1.8 - 3	> 1.2	1.25-1.8	1.3-3.6
Temp. (°C)	0 - 80	0 - 80	-40-80	-40 - 80	-45-125
I_{REF} (nA)	99	96	1 - 100	92.2	230
T.C. $_{mean}$ (ppm/°C)	169.9	600	1100	176.9	669
Power (nW)	558.3	1000	70	670	940
Line reg. (%/V)	0.7	0.2	10	7.5	3.8
Load reg. (%/V)	0.1	0.02	N.A.	N.A.	N.A.

*This work is based on simulation results.

B. Readout circuit

The simulated performance of the amplifier is summarized in Table II. In the current readout circuit, the clock frequency running the integration/reset phases can be adjusted to support different input current ranges. The input-output characteristic of the readout circuit is shown in Fig. 6 at two clock frequencies

20 kHz and 100 kHz, showing a 99.9 % linearity for input currents up to 400 nA and 2 µA, respectively.

TABLE II
SIMULATED SPECIFICATIONS OF THE AMPLIFIERS

Specifications	results
Gain	73.1 dB
Unity gain bandwidth	11.953 MHz
-3dB bandwidth	33.92 kHz
Phase margin (C_{load}=1pf)	44.6 degree
Power cons.	206.9 µW
Max output current	25 µA
Input offset voltage	2.3 mV
CMRR	110.4 dB
PSRR	74.2 dB
Slew rate	14.1 V/µsec
ICMR	0.2 - 1.3 V

Although the CDS technique reduces the 1/f noise, the thermal noise is still directly coupled to the integrator's output. The input-referred current noise $I_{n,in}$ is simulated with different clock frequency at zero input current. The total input referred current noise is then calculated by integrating $I_{n,in}$ over the f_{-3dB} bandwidth. The total input referred current noise at different clock frequencies (f_s) is plotted in Fig.6. (b). The total input referred current noise can be as low as 0.88 pA when the clock frequency is 100 Hz, showing the circuit can resolve sub-pA input currents.

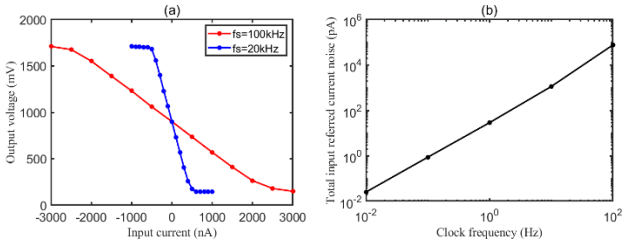

Fig. 6. (a) The input-output characteristics of readout circuit with clock frequencies. (b) The integrated input referred noise with clock frequency.

IV. CONCLUSION

An integrated circuit capable of amperometric readout within ±2 µA with 0.88 pA minimum noise has been designed and simulated. The circuit includes a current reference circuit that generates current of 99 nA for galvanostatic electrodeposition of sensor layers on chip. This is a system designed towards autonomous fabrication of on-chip electrodes. The next steps are to design the voltage generation circuit and include the ADC and digital control blocks.

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