ADVANCED POWER CONVERTERS FOR RAILWAY TRACTION SYSTEMS

by

IVAN KRASTEV

A thesis submitted to the

University of Birmingham

for the degree of

DOCTOR OF PHILOSOPHY

Department of Electronic, Electrical, and Systems Engineering

School of Engineering

University of Birmingham

March 2018

ABSTRACT

This thesis presents a new traction drive suitable for fuel-cell powered light rail vehicles based on a multilevel cascade converter with full-bridge cells. The converter provides dc-ac power conversion in a single stage, while compensating for the variation of fuel cell terminal voltage with load power. The proposed converter can replace the conventional combination of dc-dc converter, as it benefits from having a multilevel ac voltage waveform and much smaller power inductors, compared to conventional solutions.

The converter numerical and analytical models are derived showing that the converter can be modelled as a cascaded boost converter and 3-phase inverter. The design methodology for the energy storage capacitors and power inductors is presented, showing that inductance is reduced at a quadratic rate with the addition of more sub-modules, while total converter capacitance remains constant. A simulation of a full-scale traction drive in a fuel cell tram demonstrates that the proposed converter is a viable solution for light rail applications.

The concept of a boost modular cascaded converter is fully validated through a bespoke laboratory prototype driving a small induction machine. The experimental inverter achieves operation from standstill, with full motor torque, to field weakening with constant power, boosting a 50V dc supply to 200V peak line-to-line voltage.

ACKNOWLEDGMENTS

This project was a big part of my life for several years, and when I started, I really had no idea what I was getting into. In the beginning everything was nice and relaxed but, much quicker than I like to admit, the PhD poured over into my personal life. In all that time my partner Andriana stood by me, listened to me complaining about stuff blowing up and was extremely understanding when I'd spend the whole weekend fixing said stuff. She kept me clean, fed, and most of all - sane. Adi, I truly could not have done this without you.

I would also like to thank my loving parents for their support and for being so understanding – I hope I didn't worry them too much when I was locked away for days in the basement lab. They also provided priceless advice when it was time to go back to the real world and find a job and helped me prepare for interviews and negotiations.

The most fun side of the project was technical – designing and building converters, modelling and doing some embedded coding. Solving my technical problems was made easy by the wonderful people at the Birmingham Centre for Railway Research and Education (BCRRE), whom I would like to thank: Pietro Tricoli, my supervisor, was always available for a technical chat, he let me bounce so many ideas off him (most of them not very clever), and always had something helpful to say; Dr Stuart Hillmansen got me to build a hydrogen loco which is how I learned most of the engineering I know; Prof Felix Schmitt who always lent a helping hand in the right moment; Paul Weston and Louis Saade were of great help when I started writing code and were invaluable when I had to build two dozens of PCBs in the space of two months; Prof Clive Roberts for funding some power electronics shenanigans; and Adnan Zentani, for all the cutting, drilling and machining!

I would also like to thank Nadeen Taylor, for being *the best* administrator that knows everything and everyone and is always ready to help out!

Also, a big thanks to all my friends from BCRRE– Heather, Rana, Rob, Krish, Rory, Louis, Paul, and Rhys. Hanging out, playing board games and watching bad B-movies – those were lots of fun times and great memories!

Lastly, I would like to express my gratitude to the Engineering and Physical Sciences Research Council for funding this project, and ©Mitsubishi Electric Corporation for providing IGBT modules.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

A – Ampere

APOD – Alternate Phase Opposition Disposition

BMCI – Boost Multilevel Cascaded Converter

CHB – Cascaded H-bridge

CSI – Current Source Inverter

CSIsoC – Current Source Isolated Converter

DAB – Dual Active Bridge

ESR – Equivalent Series Resistance

FB – Full-Bridge

FCBC – Flying Capacitor Boost Converter

FCI – Flying Capacitor Inverter

FOC – Field-Oriented Control

HB – Half-Bridge

HVDC – High-Voltage DC

IBC – Interleaved Boost Converter

IBCCI – Interleaved Boost Converter with Coupled Inductor

IFDAB – Inductor-Fed Dual Active Bridge

IMPBCI – Interleaved Multi-Phase Boost Converter with Coupled Inductors

IsoC – Isolated Converters

IVSI – Interleaved Voltage Source Inverter

kW – kilo-Watt

kV – kilo-Volt

LLC – Stands for Inductor, Inductor, Capacitor

LSC – level-shifted carrier

MCC – Multilevel cascaded converter

MFCI – Multi-level Flying Capacitor Inverter

MMC – Modular Multilevel Inverter

MMF – Magneto-motive force

MW – Mega Watt

NO_X – Generic term for nitric oxide and nitrogen dioxide

NPC – Neutral Point Clamped

PEM – Proton Exchange Membrane

PF – Power Factor

POD – Phase Opposition Disposition

PSC – Phase-Shifted Carrier

PWM – pulse-width modulation

QZSI – Quasi Z-source Inverter

RMS – Root Mean Square

RPM – Rotations Per Minute

Si – Silicon

SIBC – Single Inductor Boost Converter

SiC – Silicon Carbide

SVM - space vector modulation

SVM – Space vector modulation

TLBC – Three-Level Boost Converter

THD – Total Harmonic Distortion

VFZSI – Voltage-fed Z-source Inverter

V – Volt

VSI – Voltage Source Inverter

W – Watt

WTHD – Weighted Total Harmonic Distortion

ZCT – Zero-current transition

ZSI – Z-source Inverter

ZVT – Zero-voltage transition

Chapter 1. INTRODUCTION

Rail transport has been a vital part of moving passengers and goods for more than a century. Electric locomotives date back to the mid-19th century, when electric motors became the standard type of traction for tram cars. In the 1890s London Underground opened the first electric deep underground railway [1], [2]. At the time all electric trains required an external power supply, that either used a third rail or an overhead catenary [3]. This was financially viable for city networks and places where steam locomotives proved too heavy, but for long distance transport of people and goods an autonomous vehicle was required.

Until sufficient advances in diesel traction technology made it viable, steam locomotives were the main type of vehicle as they were able to use multiple types of fuel and provided the necessary power. By the middle of the 20th century diesel locomotives were developed, that can use gearboxes and hydraulic torque converters to keep the diesel engine within its allowed limit of rotations per minute (RPM) [4], [5], but due to the flexibility of electric drives, diesel-electric engines became the dominant type [6], [7], [8], [9].

The role of the conversion equipment has always been to match the voltage and current waveforms of the power supply to those of the traction motors. What has changed is the efficiency of the conversion process, and the performance that can be achieved by the motors. Probably the biggest advance in railway traction has been the introduction of ac motors (both synchronous and asynchronous), that has been made possible by the availability of fast semiconductors and digital electronics. Ac motors, and the increased performance of power electronics, have allowed for a substantial reduction in system losses. The limited thermal overloading capability of semiconductor devices, however,

has made them some of the most vulnerable components in the traction drive [10]. [11], [12], with factors such as rms current and voltage stresses playing an important role in the longevity of this equipment [13], [14].

To this day, diesel-electric trains are the dominant type, as diesel locomotives and diesel multiple units do not require special infrastructure other than refuelling stations [15]. Since modern diesel railway vehicles have a fully electric drive, they can be hybridised by adding a battery or supercapacitor energy storage bank [16], [17], [18], [19]. However, diesel engines still emit high amounts of NO_x gasses, as well as fine particles, that can cause serious health conditions. This has made diesel technologies undesirable in urban areas and there is a strong incentive to develop alternatives that rely on electric power sources only.

Hydrogen fuel cells are such a source. They use hydrogen and oxygen to generate directly electrical power at a high efficiency. This efficiency is higher than that of diesel generators [20], [15]: typical diesel generators operate with peak efficiency of 40%, whereas hydrogen fuel cells can achieve as high as 55% [21], [22], [23], [24]. The only moving parts of a fuel cell are the hydrogen supply, purge valves, and any air feed pumps [25]. Compared to diesel generators, maintenance costs are lower [26], [27], and the only by-products of the hydrogen-oxygen reaction are water and heat. While the quantities of water are low, and the water can be recycled to cool and hydrate the fuel cell membrane, the heat is useful in public transport vehicles, as it can be used for vehicle interior heating when temperatures are low.

The application of fuel cells to railway vehicles requires a suitable design of the power conversion systems to ensure the required traction control of the motors and the optimal usage of the fuel cell stacks. However, traditional power converter topologies for fuel cells powered trains have significant limitations on power density and cost due to passive

components like inductors and capacitors. This thesis analyses in details the main requirements of fuel cell traction drives and proposes an innovative power converter topology suitable for the best exploitation of the capabilities of hydrogen fuel cells.

1.1. PROBLEM STATEMENT

The most widely accepted metrics of modern power converters are power density (kW/litre), specific power (kW/kg), cost (£/kW), and efficiency (%). These characteristics are measurable and are used to set goals and targets in technology roadmaps [28], [29], [30]. Depending on the specific application one or two of these parameters will drive the others. Thus, the designer's main task is optimizing the power system by choosing a power converter topology and the main building blocks – traction motor, type of power semiconductor devices, passive components, and control electronics. Assuming that state-of-the art technology can be used for any newly designed converter, the main problem becomes finding the most appropriate topology for the application.

In the automotive sector the number of vehicles is high, with 180 000 plug-in cars registered in the UK, and counting. Cost and power density stand out as the main drivers [31], and average power, across vehicles, is around 100kW [31]. Thus, automotive applications favour simple two-level power converter topologies, where power density can be improved by increasing device switching frequency. However, they are heavily reliant on advances in semiconductors [32], [33].

The railway sector, on the other hand, has a low number of powered rolling stock – less than 14 000 in total [34]. Thus, traction systems are tailored to the requirements of the train and power levels can vary between 10s of kWs and MWs [35]. From this it can be concluded that scalability of the power converter topology is an important factor. In addition, reliability, availability, maintainability, and safety (RAMS) have high importance

[36], [37], as a single train failure can have a propagating effect on a timetable and a single vehicle can transport many people.

The system design is further complicated by the requirements of alternative power sources. For example, hydrogen fuel cells, like diesel generators require a power converter to maintain a constant voltage for the dc-bus of the traction inverters, and any additional dc-dc converters that would be needed for battery or supercapacitor energy storage. Like traction inverters, these dc-dc converters are either 2-level unidirectional and bidirectional converters, or isolated converters. Unlike inverters, dc-dc converters with special topologies can improve the power density by reducing the size of the passive components. However, these approaches have limitations, which are explored in detail in Chapter 2 and the magnetic components they use have a profound effect on power density and specific power.

This thesis discusses the Modular Cascaded Converter and how it can be controlled as a buck-boost inverter, which can be called a Boost Modular Cascaded Inverter (BMCI). The topology is formed of multiple converter sub-modules linked together to function as a mixture between a boost converter and multi-level inverter. Unlike traditional power converters, power transfer from dc-side to ac-side does not occur over one switching cycle, but over one cycle of the inverter's ac-side waveform. This has implications both on the fundamental functionality of the converter and its design.

Therefore, the main challenges of the design of the proposed BMCI, discussed in this thesis, are the reduction in passive component size, the choice of number of semiconductor devices, the choice of pulse-width modulation (PWM) method that requires the smallest inductance, and the control of the proposed converter. The thesis also discusses the limitations of the BMCI and what areas require further investigation.

1.2. RESEARCH OBJECTIVES

The goal of this research project is to examine the BMCI and to define a methodology for the design of the passive components, aimed at optimising the power density of the converter. The suitability for the traction drive of a light rail vehicle is also explored. In particular, this thesis aims to investigate the following aspects:

- Compare the BMCI with the current state-of-the-art of traction drives and dc-dc converters
- Understand the operating principle of BMCIs with reference to the power transfer and voltage boost achieved
- Derive a converter mathematical model that is suitable for numerical simulation and confirmation of theoretical properties using circuit simulation tools;
- Derive the large and small signal models of the converter that can be used for the design of its control systems
- Understand the requirements of the control systems for the operation of BMCI as traction drive and demonstrate the design principle
- Examine the peculiarities of BMCI design: present and compare the possible modulation methods, and how they affect the design of the inductors; define capacitor design method based on system dc-side and ac-side voltages, as well as electric motor power factor and base frequency
- Undertake numerical simulations to verify the suitability of the BMCI as traction drive in a realistic scenario
- Validate mathematical modelling, design guidelines, and simulation with a laboratory prototype driving an induction motor and a mechanical load

- Demonstrate 4 quadrant operation with voltage buck and boost, while operating with constant torque at low speeds, and field weakening and constant power at high speeds

1.3. PUBLICATIONS

The PhD project has produced the following works, published in the proceedings of an international conference and in an IEEE magazine:

- I. Krastevm, N. Mukherjee, P. Tricoli and S. Hillmansen, "New modular hybrid energy storage system and its control strategy for a fuel cell locomotive," *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Geneva, 2015, pp. 1-10. doi: 10.1109/EPE.2015.7309371
- I. Krastev, P. Tricoli, S. Hillmansen and M. Chen, "Future of Electric Railways: Advanced Electrification Systems with Static Converters for ac Railways," in *IEEE Electrification Magazine*, vol. 4, no. 3, pp. 6-14, Sept. 2016. doi: 10.1109/MELE.2016.2584998
- M. Chen *et al*., "Modelling and performance analysis of advanced combined co-phase traction power supply system in electrified railway," in *IET Generation, Transmission & Distribution*, vol. 10, no. 4, pp. 906-916, 3 10 2016. doi: 10.1049/iet-gtd.2015.0513

The main research paper, that covers a portion of the work presented in this thesis, is still being developed, with expected submission by the end of February 2019. The thesis has also generated additional ideas for applications based on BMCI or other modular cascaded inverters. The working titles of these works are:

- “Characteristics and design of a boost modular cascaded inverter for a railway fuel cell traction drive”
- “A new Active Traction Rectifier with Bidirectional Power Flow and Fault Current Limitation”

1.4. THESIS OUTLINE

Other than this one, the thesis is organized in 6 chapters, that cover the work completed during this PhD project:

Chapter 2 - Literature review: presentation of state-of-the-art and current developments of power converters for electric vehicles. Background of the converter proposed in this thesis.

Chapter 3 - Modelling: Basic operation of BMCI, derivation of continuous-time and small-signal models.

Chapter 4 - Control: Illustration of the use of the small-signal model from chapter 3, as well as description of other control systems required.

Chapter 5 - Design of BMCI: Detailed procedures for the design of a BMCI, including choice of modulation scheme, inductor design, capacitor design. This chapter also documents the design of the experimental prototype converter.

Chapter 6 - Simulation of BMCI for a hydrogen tram: example of a converter design using data from real-life tram. Presentation of simulation results during a traction cycle, with special attention paid to converter current and voltage waveforms and harmonic distortion performance.

Chapter 7 - Experimental validation: presentation of experimental results gathered from BMCI bench prototype.

Chapter 2. REVIEW OF BOOST CONVERTERS AND INVERTER DRIVES FOR ELECTRIC TRACTION

This section starts with a discussion of the general requirements for a traction converter and draws out the specific functionality needed for hydrogen fuel cell vehicles. A set of metrics are derived to aid the evaluation of different converters and more particularly their use in railway vehicles. This subsection is followed by a review of modern power converter topologies that could be used in a fuel cell railway vehicle.

The main task is to convert a dc voltage, that can have a range of steady-state values, to a 3-phase variable amplitude, variable frequency ac-voltage. This can be achieved in different ways and this chapter discusses the following ones: direct dc to ac conversion, with voltage step-down (buck); indirect dc-dc with voltage step-up (boost) followed by dc-ac step-down (buck), illustrated in Figure 2-1; direct dc to ac with voltage buck and boost.

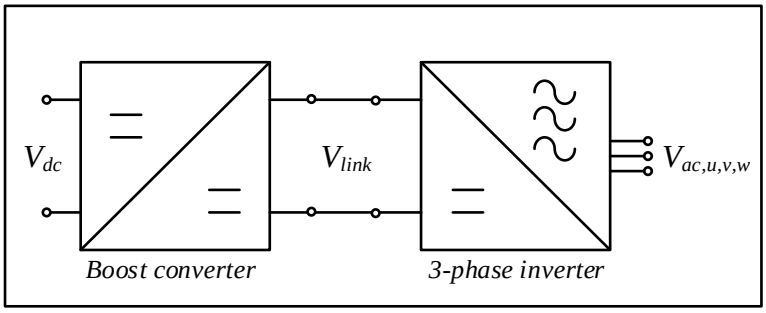

Figure 2-1 Diagram of a 2-stage conversion process - dc-dc and dc-ac, with intermediate voltage V_{link}

2.1. DISCUSSION OF REQUIREMENTS AND METRICS

To maintain the maximum acceleration of the railway vehicle, the most basic requirement for a traction converter is that it must supply the full machine current from 0 up to maximum motor speed. To achieve this, the system designer must ensure that the dc-side voltage can be inverted to produce sufficiently high ac voltage to overcome the

electric motor's back electromotive force (back EMF). In addition, a modern traction converter must be capable of 4-quadrant operation, i.e. regenerating energy from the electric machine. This energy can either be dissipated with a braking chopper [38], returned to the dc-side power source, or a third port can be added to connect an energy storage system (ESS) [39], [29], [40], [41], using batteries, supercapacitors, or a 3-phase inverter feeding a flywheel [42], [17], [43].

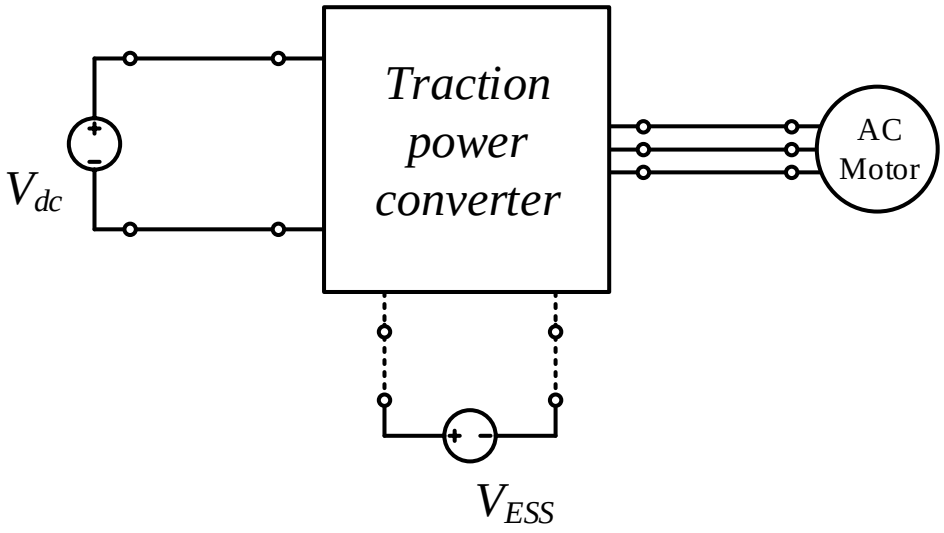

Figure 2-2 Basic diagram of a traction converter with optional energy storage

The dc-side of the converter can be connected to a power source, such as a fuel cell stack [44], battery pack [45], [39], [46], or the catenary of a railway network [47], [48], [49]. These sources are best suited to constant dc current being drawn from them, and high harmonic content is undesirable. For example, electric railway vehicles have catenary filter inductors to attenuate low and high-frequency harmonics that can interfere with communication and signalling equipment [50], [47], [51], but they add to the traction system's size and weight. Another important aspect is the level of the dc-side voltage of the traction inverter, which is affected by the impedance of the power source. This is particularly relevant for sources like hydrogen fuel cells that have a significant internal impedance. In fact, when a train accelerates from a stationary position, the fuel

cell voltage is at its peak value, but at full power it is at its lowest. During braking, if the system uses an energy storage device or a braking chopper, the fuel cell current must be reduced to 0, which means its voltage will be at its maximum again. Thus, it is beneficial for a fuel cell drive converter to maintain constant ac-side voltage with varying dc-source voltage.

The waveform at the ac-side of a traction converter not only controls the electric machine, but also affects drivetrain reliability. Fast transients at the output of the inverter can cause reflections and high voltage spikes at the motor terminals [52], [53], while leakage currents can cause damage to bearings [53], [54], [55], [56], which is a safety critical part in a railway vehicle [57]. To address these shortcomings the system designer can use a multilevel inverter, where the phase voltage has 3 or more discrete voltage levels. This type of converter reduces the peak voltage step and the unwanted effects associated with PWM inverters [58].

An additional benefit is that multilevel inverters cause lower stator current THD, which in turn reduces the flux oscillations inside the motor. These oscillations cause losses in the motor yoke and rotor laminations [59], [60], [61]. Multilevel inverters produce phase voltages that are closer to a sinusoidal waveform and have been shown to reduce iron core losses [62], [63].

Multi-level converters with series connected switches have additional benefits. A historical problem with railway drives is the limitation of the semiconductor voltage rating [49], [64]. To balance the high voltage, traction inverters had to be connected in series, with additional circuitry to equally share the voltage [65]. While current rating can be increased by connecting transistors in parallel, a series connection to increase the voltage rating requires complicated gate drive and device protection. At the same time, using a higher system voltage is the preferred method for increasing the power rating, as

higher current raises conduction losses at a quadratic rate. Thus, topologies that allow for the use of lower voltage rated transistors are preferred.

As discussed in Chapter 1, volumetric and mass power densities are important factors for traction converters. The biggest contributors to this are the energy storage elements – the reservoir capacitor and the power inductor [66], [67], [68]. In conventional 2-level converter topologies, the power density of these passive components is inversely proportional to the square of the converter switching frequency [69]. Inductors, in particular, have very poor energy density and specific energy, so alternative approaches to reducing their size and weight have been the focus of a lot of work [70], [66], [71], [72] [73], [74], [68], [75]. To judge the suitability of different topologies for traction converters, the topics discussed above are summarised as the following criteria:

- Energy storage
- Total switch apparent power
- Power source/dc-side current ripple
- Motor/ac-side maximum voltage step
- Machine/ac-side current weighted THD
- Scalability
- Availability
- Reliability

2.2. 3-PHASE INVERTERS

Inverters generate a 3-phase voltage with variable frequency and amplitude, by either chopping a dc voltage or a dc current, which in turn determines the type of converter – voltage-source or current source, respectively.

If the traction system only consists of a 3-phase inverter driving one or more ac motors, the system can manage these conditions with careful design and accepting several trade-offs. Inverter transistors are selected for the peak fuel cell voltage and peak motor current. The electric motor is designed with insulation rating that can withstand pulses equal to the open circuit fuel cell voltage, while windings are dimensioned for current at the fuel cell voltage at point of maximum power. The resultant drive will effectively be overrated and will be able to practically deliver up to 60% higher output power.

The inverters discussed are separated into two categories, depending on the number of voltage levels in each phase.

2.2.1. 2-Level inverters

2.2.1.1. 2-level voltages source inverter (VSI)

The 2-level inverter comprises a 6-transistor bridge, fed by a voltage source, decoupled by a capacitor [32], [76], [77], with a diagram shown in Figure 2-12. Each converter leg is switching at a switching frequency f_{sw} and produces 2 voltage levels. The resultant phase-to-phase voltage is a 3-level waveform, switching at twice the single transistor frequency.

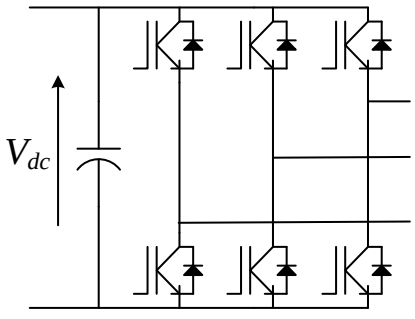

Figure 2-3 2-level voltage source inverter

Two-level voltage source inverters are the standard converter used in motor drives, with readily available transistor modules with 6 switches. Due to the inverter's simplicity and flexibility of manufacture, it has been used in a prototype fuel-cell drive [78].

As the 2-level VSI uses the minimum amount of semiconductor switches, the topology has no fault tolerance. If a single open-circuit fault occurs, the electric machine can no longer be fully controlled, as the amount of state vectors greatly reduces, and if a single short-circuit fault occurs, the inverter control must be stopped immediately to avoid short circuit of the dc-link. The properties of the 2-level VSI are summarised in Table 2-1:

Table 2-1 VSI properties

Energy storage:	Very low	Only requires 1 capacitor
Switch apparent power:	Low	Depends on machine power factor
dc-side current ripple:	High	Pulsed current, requires inductor filter
ac-side voltage step:	High	Equal to V_{dc}
Machine current THD:	High	High-voltage inverters have low switching frequency
Scalability:	Low	Wholly dependent on semiconductor technology
Availability:	Low	Single switch fault makes drive inoperable
Reliability:	High	Lowest number of switches
Function:	Buck	Max line-to-line voltage is V_{dc}

2.2.1.2. Interleaved 2-level VSI with coupled inductors (IVSI)

Two 6-transistor bridges can be interleaved using 3 inductors, [79], [80], [81]. Each inductor has a centre tap that is connected to the electric motor. For a 12-transistor inverter, the inductor does not require an air gap, but the 6-transistor version does [82]. Effectively, the inverter has a 3-level waveform, oscillating at twice the device switching frequency, as shown in Figure 2-4:

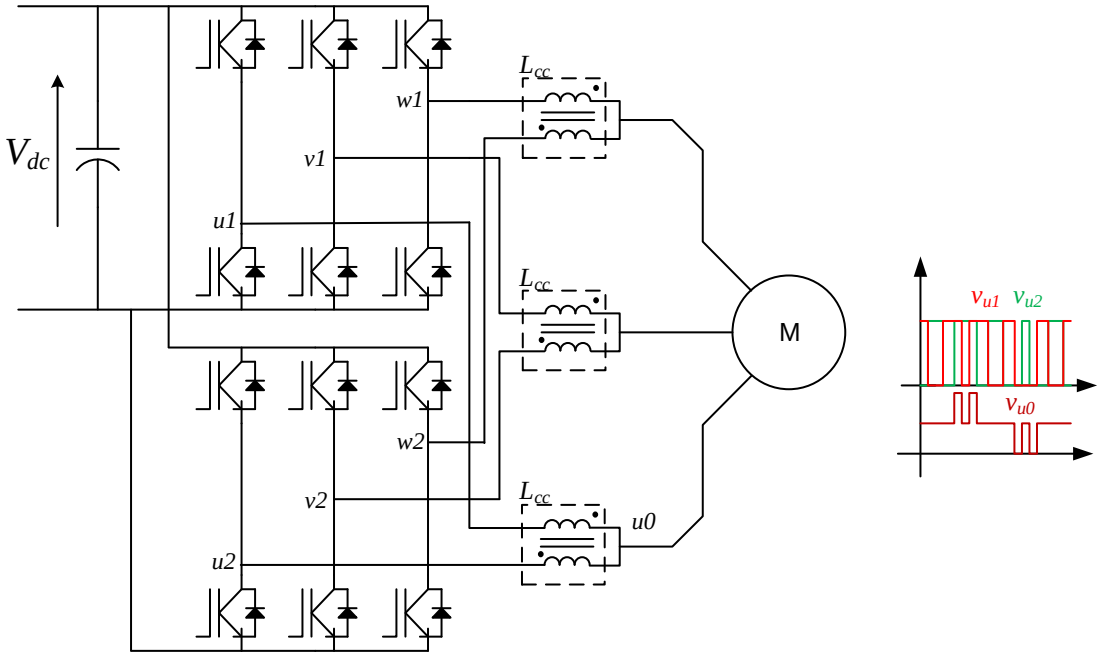

Figure 2-4 Interleaved VSI with coupled inductors

Each interleaved inverter provides half the machine current. The dc-side capacitor RMS current is also lowered, and with a higher ripple current frequency, thus reducing the capacitor size. As the system comprises of essentially two inverters operating in parallel, the system is tolerant to a single fault, both switch open circuit and short circuit.

The big drawback of the interleaved inverter is the necessity for magnetic components, that increase power dissipation and reduce power density. Also, the interleaved VSI requires 3 additional current transducers for every VSI bridge. The interleaved VSI properties are listed in Table 2-2:

Table 2-2 IVSI properties

Energy storage:	Medium	Inter-phase inductors required
Switch apparent power:	Low	Depends on machine power factor
dc-side current ripple:	High	Pulsed current, but lower RMS compared to VSI
ac-side voltage step:	Medium	Equal to $V_{dc}/2$
Machine current THD:	Medium	Phase waveform equivalent to that of a 3-level inverter
Scalability:	Medium	Interleaving more than 3 inverters is complicated
Availability:	High	One inverter can continue operating with half the power rating
Reliability:	Medium	Twice as many devices as VSI
Function:	Buck	Max line-to-line voltage is V_{dc}

2.2.1.3. 2-level current source inverter (CSI)

A 3-phase inverter can also operate as a current source, where a dc current is chopped into pulse width modulated currents. The transistor bridge consists of 6 reverse blocking switches, and the output current is filtered by 3 capacitors, connected directly across the output devices, as shown in Figure 2-5:

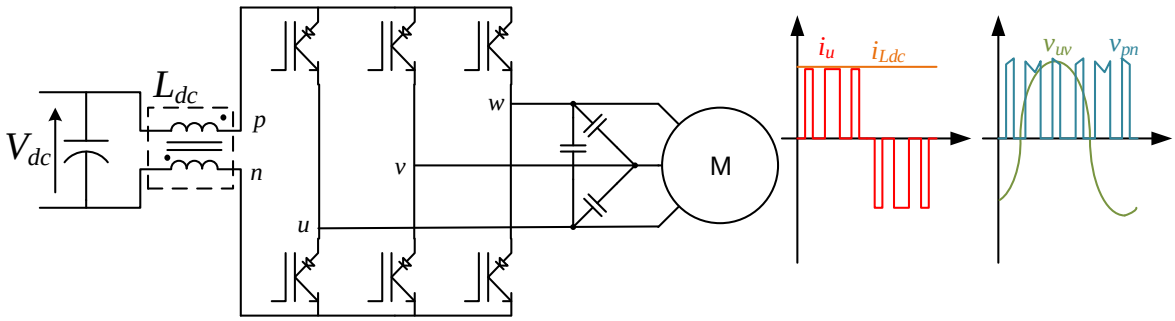

Figure 2-5 Current source inverter drive

As traction motors are inductive loads, the output capacitance of the inverter can be relatively small, with ac-side voltage harmonic distortion much lower than that of a 2-level VSI.

The CSI requires a configuration of the transistor bridge, that produces a short circuit for the dc-side current source. This condition can be utilized to boost the dc voltage, and the CSI is effectively a boost-type converter with a minimum voltage gain of 1. This is not suitable for traction loads, where motor voltage varies from 0 to V_{dc}, and an additional dc-dc converter is required for buck operations. Another drawback is that the CSI's transistor bridge can conduct current in only one direction, and to achieve power reversal, the dc-side voltage must be inverted [45]. The properties of the CSI are listed in Table 2-3.

Table 2-3 CSI properties

Energy storage:	Medium	Requires bipolar capacitors and inductor
Switch apparent power:	Medium	Reverse blocking switches
dc-side current ripple:	Low	Inductor design parameter
ac-side voltage step:	Low	ac capacitor design parameter
Machine current THD:	Very low	ac-side voltages are sinusoidal
Scalability:	Low	Wholly limited by semiconductor technology
Availability:	Low	Single fault would make inverter inoperable
Reliability:	High	Lowest number of active devices
Function:	Boost	Minimum line-to-line voltage is V_{dc}; requires buck converter

2.2.2. Multi-level inverters

Converters with more than 2 levels have lower ac voltage distortion at full modulation index, which reduces the iron losses in the electric motor. On average they also have lower switching losses, for the same effective switching frequency, and lower dc-side capacitor RMS current.

Multilevel converters can help in reducing the total *dv/dt* and *di/dt* of the converter voltages and currents. They can also utilise devices with lower voltage ratings, with most topology allowing for higher average phase voltage switching frequency. For inverters the result is improved total harmonic distortion (THD) of the motor voltage and consequently of the electric motor currents.

2.2.2.1. Neutral point clamped multi-level inverters (NPC)

This type of inverter requires 2 transistors, with anti-parallel diodes, as well as two discrete diodes for every additional output level [83], [84]. An *n*-level inverter requires

2n transistors, with antiparallel diodes, as well as *n* diodes to achieve clamping to one of the *n-1* dc-link capacitors. While the number of devices is per phase, the dc-link capacitors can be shared between phases, which increases the frequency of the capacitor power fluctuation and reduces its size. This topology has been used in railway applications [64], as it allows for a higher dc-link voltage. The 3-level NPC inverter circuit is shown in Figure 2-6 and the 4-level topology is shown in Figure 2-7.

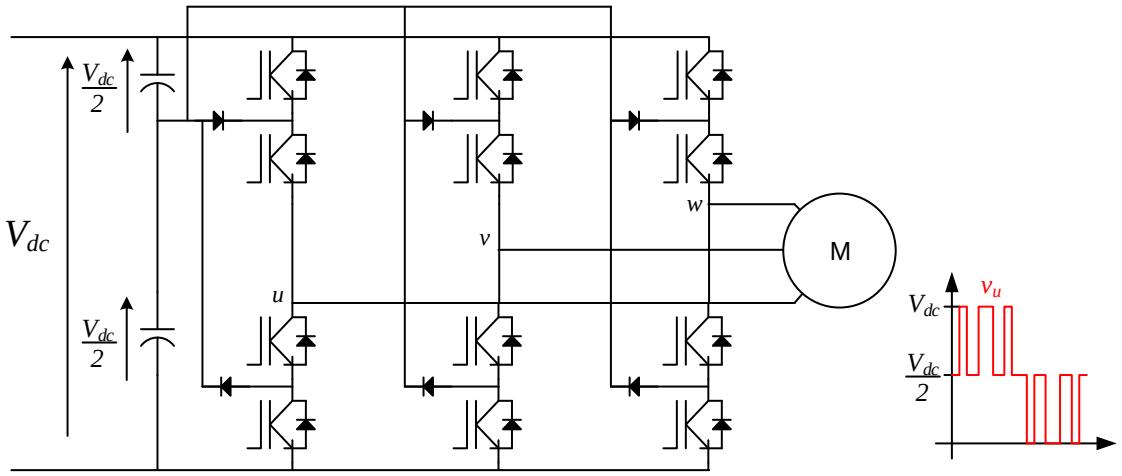

Figure 2-6 3-level NPC inverter

Additional levels require more series connected capacitors, and the dc-side voltage would be shared equally between them. For reliable operation, the NPC inverter requires measurement of all the dc-link capacitors and 3 floating current sensors. The capacitors can be balanced by using external circuits [85] or through the control of the common mode voltage. In practice, this becomes challenging for inverters with 5 or more levels.

In a phase leg, only 2 devices are switching at any given time, with the other two either constantly on or constantly off. Over one cycle of the motor waveform, the mean switching frequency will be less than the modulation carrier, but the transistors will see varying switching and conduction losses, depending on motor speed.

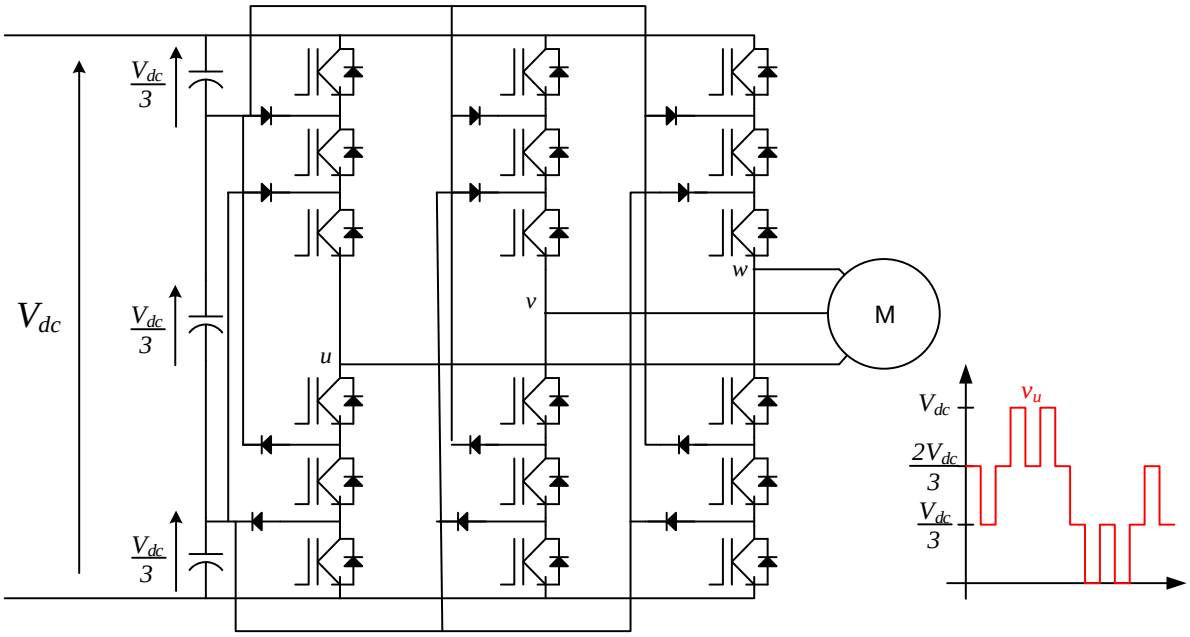

Figure 2-7 4-level NPC inverter

While each transistor switch is still rated for V_{dc}/n, each of the clamping diodes will require a rating of $nV_{dc}/(n-1)$ [86], which will require either single high voltage diodes, or multiple diodes connected in series. In addition, NPC-type topologies do not guarantee dynamic voltage sharing of the dc-side voltage, as device voltages are clamped by diodes with finite forward and reverse recovery [172].

The properties of the neutral point clamped inverters are summarised in Table 2-4:

Table 2-4 NPC inverter properties

Energy storage:	Low	Capacitors common to all 3 phases; ripple current at switching frequency
Switch apparent power:	Low	Extra pair of diodes per level necessary
dc-side current ripple:	High	Pulsed waveform
ac-side voltage step:	Low	Ac capacitor design parameter
Machine current THD:	Low to Medium	3-level inverter has a step of $V_{dc}/2$, decreased with more levels
Scalability:	Medium	Capacitor and semiconductor voltage balancing become challenging for more than 3 levels
Availability:	Medium	The converter can operate with a short-circuit fault
Reliability:	Low	High number of active switches
Function:	Buck	Maximum line-to-line voltage is equal to V_{dc}

2.2.2.2. Multi-level flying capacitor inverters (FCI)

The flying capacitor multilevel inverter is an alternative family of multilevel inverters, with the same number of transistors as an NPC converter, for the same *n*. The key difference is that the FCI does not utilise clamping diodes, and instead has phase capacitors [87], [88], as shown in Figure 2-8:

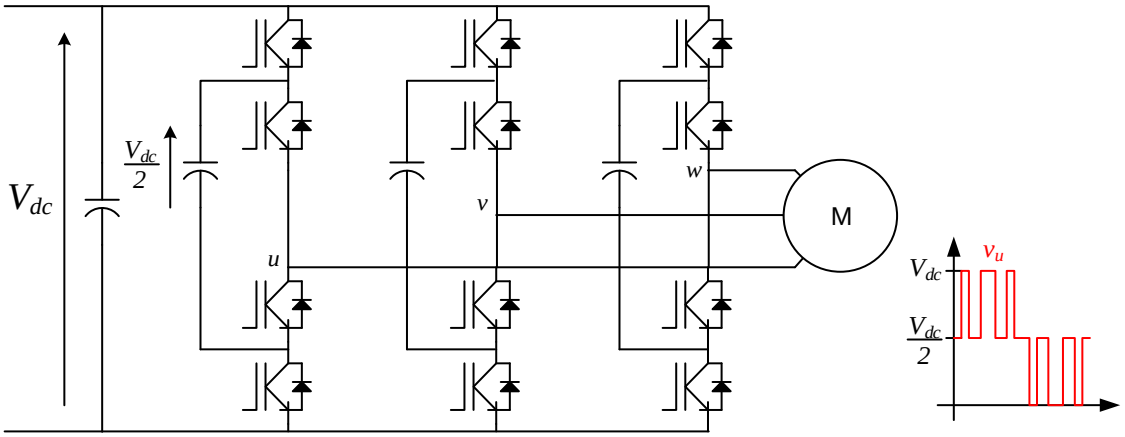

Figure 2-8 3-level FC inverter

The ideal ac-side voltage waveform is almost identical to the NPC inverter, but is produced by clamping a phase capacitor to a power rail, or to another phase capacitor. All devices operate with a constant switching frequency $f_{sw,Q}$, with the effective switching frequency of each phase equal to $f_{sw,Q}(n-1)$ [89]. Another quality of the FCI is the available redundant ac-side voltage states – for voltages not equal to the power rails, there are two switching combinations that can produce the same voltage step. This degree of freedom can be used to balance the individual phase capacitors.

The inverter requires 3 current sensors, and a voltage transducer per each flying capacitor. Figure 2-9 shows a 4-level MFCI. With $n>3$, unlike the NPC inverter, the phase capacitors have different voltages. Thus, the inverter requires multiple capacitors with different voltage ratings.

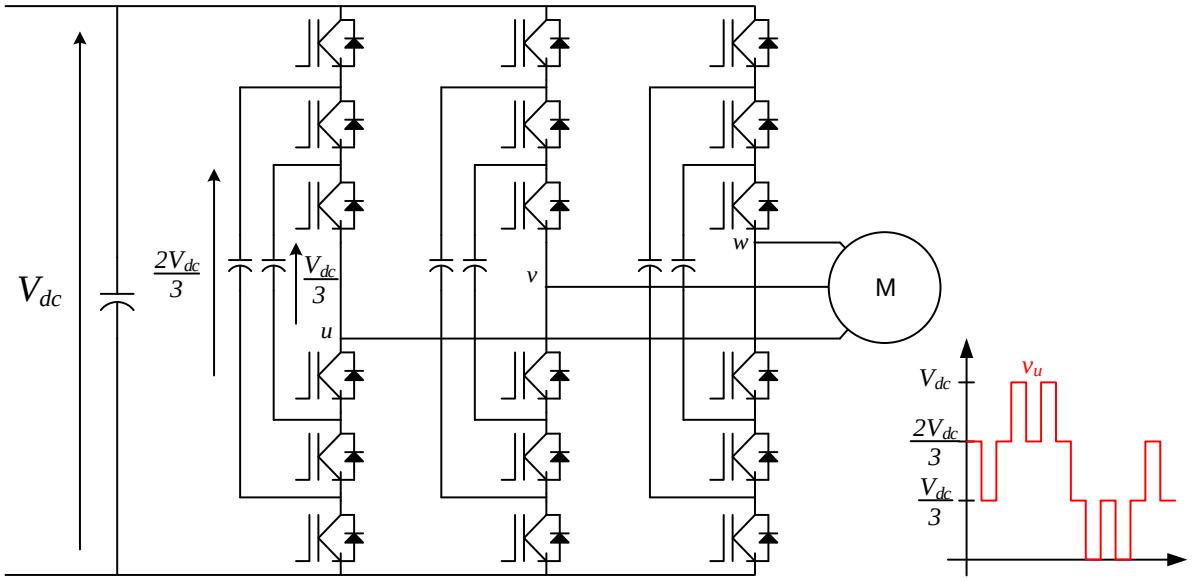

Figure 2-9 4-level FC inverter

As the only way for current to flow through the phase capacitors is through the load, the MFCI requires a separate balancing algorithm during start-up. Before capacitors are charged, their voltage is 0, and the transistors will not share V_{dc} equally. This is one of the major drawbacks of this topology. The properties of the FCI are summarised in Table 2-5:

Table 2-5 FCI properties

Energy storage:	Medium	Capacitor ripple at switching frequency
Switch apparent power:	Low	No additional diodes necessary
dc-side current ripple:	High	Pulsed waveform
ac-side voltage step:	Low	Equal to V_{dc}/n
Machine current THD:	Low to Medium	Effective switching frequency is nf_{SW}
Scalability:	Medium	Capacitor balancing becomes challenging for more than 3 levels
Availability:	Medium	The converter can retain some operation
Reliability:	Low	High number of active switches
Function:	Buck	Maximum line-to-line voltage is equal to V_{dc}

2.2.2.3. Cascaded H-bridge inverter (CHB)

The cascaded H-bridge inverter uses chains of full-bridge cells, forming 3 converter arms. They are connected in a star configuration [90], [91], [92], [93], and each end is connected directly to the traction motor. Each sub-module either has an isolated power source feeding the H-bridge, or an isolated transformer power link to the main power source. As the converter is constructed of multiple identical sub-modules, it can maintain operation if either a single open-circuit or short-circuit fault occurs. A diagram of the converter is shown in Figure 2-10:

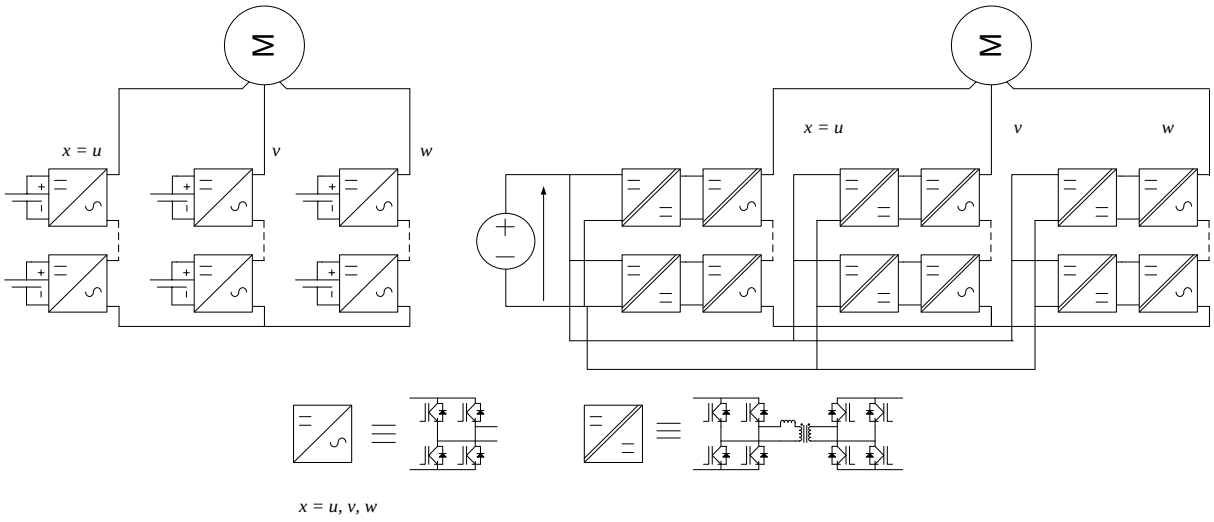

Figure 2-10 Cascaded H-bridge inverters with separate isolated power sources (left) and single dc power source (right)

For an *n*-level inverter, the number of devices required is *12n* resulting in high ac-side voltage waveform quality [94]. However, if the converter uses *n* isolated links per phase, the number of devices increases by further 4 to 8 per sub-module. This topology is particularly suited to applications where galvanic isolation between the primary power source and the electric machine neutral line is required.

As each converter arm supplies one phase of the electric machine, it is essentially a single-phase dc-ac inverter. Thus, the power in each converter arm oscillates at twice the machine electrical frequency, resulting in large energy storage requirement, compared to other converters discussed.

Another benefit of CHB converters is the fact that to achieve a higher ac-side voltage, the converter only requires additional sub-modules [95], which in turn further increases power quality.

The properties of the Cascaded H-bridge inverter are summarised in Table 2-6:

Table 2-6 CHB inverter properties

Energy storage:	High	Sub-module capacitor ripple oscillates at twice the machine frequency
Switch apparent power:	High	Isolated converter necessary for each sub-module
dc-side current ripple:	Medium	Interleaving of isolated converters reduces dc-side RMS current
ac-side voltage step:	Low	Equal to V_{dc}/n
Machine current THD:	Low	Effective switching frequency is $2nf_{SW}$
Scalability:	High	Power rating is increased by additional modules
Availability:	High	Sub-modules can be bypassed, and converter can operate with reduced rating
Reliability:	Low	High number of active switches
Function:	Buck-Boost	Boost ratio set by transformer ratio

2.2.2.4. Multilevel cascaded converter (MCC) or Modular Multilevel Converter (MMC)

The modular cascaded converter is similar to two cascaded H-bridge converters connected in series, as each phase consists of two converter arms. In contrast to the H-bridge inverter, the MCC has one inductor connected in series with each arm. The MCC has been shown to be suitable to motor drives in several publications [63] [96], [97], [98], [97], [99]. To reduce size each pair of phase inductors can be wound on the same core, reducing inverter output impedance [100], [101], [102]. Schematic of the converter is shown in Figure 2-11.

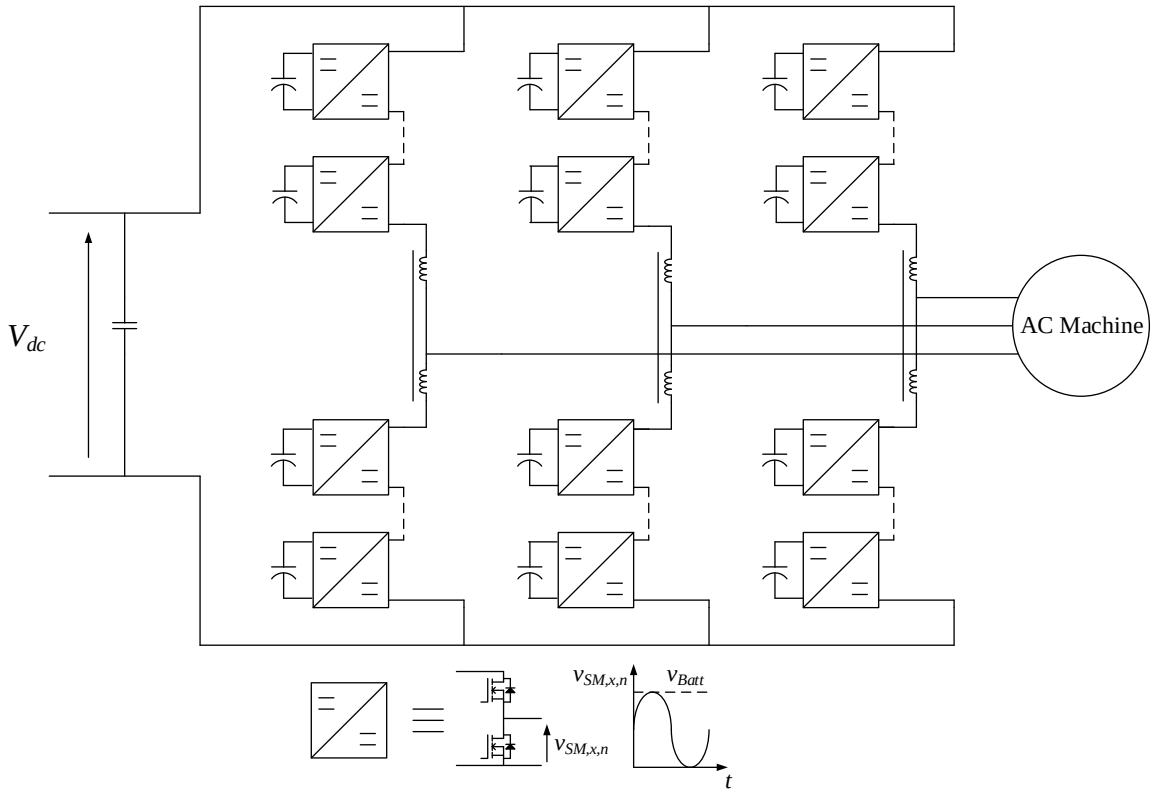

Figure 2-11 Multilevel Cascaded Converter with half-bridge cells

As with the cascaded H-bridge inverter, the MCC is essentially composed of 3 dc to single-phase dc-ac converters. The arm power oscillates at the machine electrical frequency and at twice that frequency, which is a challenge at low motor speeds.

Different types of sub-module switch configurations have been explored [103]. Most of them become impractical at low voltage levels, as they require additional diodes. The two most popular configurations are transistor half-bridges or full-bridges.

The MCC buck inverter half-bridge variant is only suitable for dc-ac operation and is susceptible to short circuit faults on the dc-side. Thus, for an *n*–level converter, the number of devices in a leg is *4n* or *2n*, depending on modulation scheme [104], [105].

The converter with full-bridge sub-modules can block dc-side short circuit faults and can actually operate as an ac-ac converter [106], [100], [107].

Alternatively, MCC sub-modules can be mixed, constructing a hybrid half-bridge and full-bridge sub-module converter [108], [109], [110]. An additional advantage of these

topologies is that they have reduced device count, while retaining dc-fault ride-through capability.

The main advantage of MCC-type converters is that increasing the number of voltage levels is relatively straightforward. Unlike NPC inverters, the MCC does not require separate balancing converter for *n>3*. Compared to the FCI, all MCC capacitors have the same voltage rating. The properties of the MCC are summarised in Table 2-7:

Table 2-7 MCC properties

Energy storage:	High	Sub-module capacitor ripple oscillates at the machine frequency; inductor necessary
Switch apparent power:	High	Switches carry both dc-side and ac-side currents
dc-side current ripple:	Low	Inductor design parameter
ac-side voltage step:	Low	Equal to V_{SM} or $V_{SM}/2$
Machine current THD:	Low	Effective switching frequency is $2nf_{SW}$
Scalability:	High	Power rating is increased by additional modules
Availability:	High	Sub-modules can be bypassed, and converter can operate with reduced rating
Reliability:	Low	High number of active switches
Function:	Buck	Maximum line-to-line voltage is V_{dc}

2.3. BOOST CONVERTER TOPOLOGIES

2.3.1. Single inductor boost converter (SIBC)

The single-inductor boost converter is the simplest possible topology, using only 2 semiconductor switches and one inductor, and one or two capacitors, as shown in Figure

2-12. The converter top switch can be a diode, for unidirectional power flow, or a transistor for bidirectional power flow [111], [112], [113].

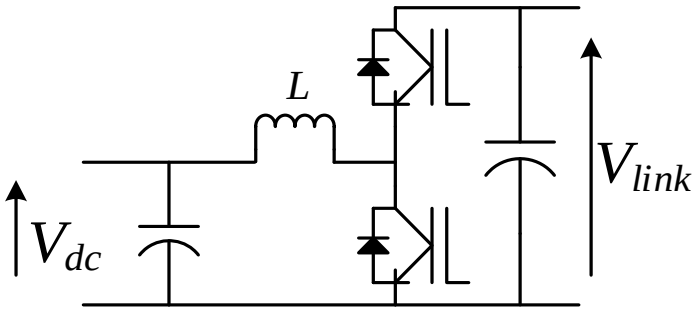

Figure 2-12 Single inductor boost converter

The semiconductors need to be rated for the full dc-side current and the peak link voltage. As the higher voltage rating means increased semiconductor thickness, the total device area needs to increase, which reduces switching speed. The maximum transistor switching frequency has a proportional effect on passive component values. Inductor volume is roughly proportional to the energy stored in it and increases with the square of the inductor dc-current. The capacitor ripple current will also oscillate at the switching frequency, with the maximum amplitude occurring at 50% duty cycle. High capacitor RMS currents have a detrimental effect on component life and result in increased size and cooling requirements.

This topology has poor fault tolerance as only a top-circuit short circuit or bottom switch open circuit faults can be tolerated. If either of these faults occur, the converter can only transfer power from V_{dc} to V_{link} and it will be without any regulation of V_{link}.

This converter is popular for traction applications in the automotive sector and is used for both fuel cell and battery/supercapacitor onboard systems [114], [113], [111], [115]. Strategies have been developed to reduce the high-side link capacitance [116], [117], but these schemes cause a higher current ripple in the power inductor. Converter properties are summarised in Table 2-8.

Table 2-8 SIBC properties

Energy storage:	High	Inductor is large and heavy for high-power converters
Switch apparent power:	Low	Lowest apparent power possible
dc-side current ripple:	Low	Inductor design parameter
Scalability:	Low	Dependent on semiconductor technology
Availability:	Medium	Limited operation possible with a fault
Reliability:	Low	Circuit can somewhat tolerate a single fault
Function:	Boost	

2.3.2. Interleaved boost converter with separate inductors (IBC)

The single inductor boost converter can be interleaved with additional phase legs, each one having an inductor, but all connected to the same output capacitor [46], [73], [111], [118], [119]. For a converter with *m* legs, each leg's carrier is phase-shifted by $2\pi f_{carrier}/m$ radians. Relative to the individual leg currents, this strategy reduces low-side current ripple and the its ripple frequency increases proportionally with *n*. A similar effect is seen by the link capacitor, reducing the RMS capacitor currents by both increasing frequency and reducing amplitude. A circuit diagram of a multi-leg converter can be seen in Figure 2-13.

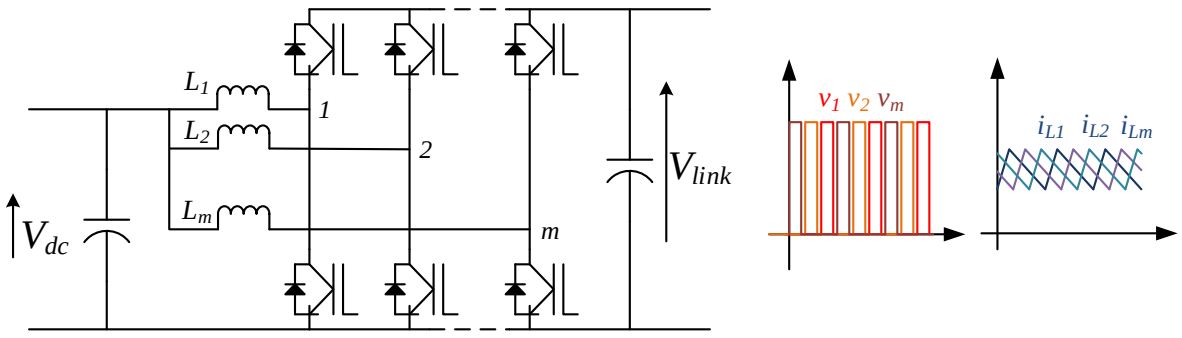

Figure 2-13 Multi-leg interleaved boost converter

At certain operating points, depending on the number of phase legs, the interleaved converter can achieve 0 ripple in the low-side and high-side currents. These duty cycle values are discrete, however, appearing *(m-1)* times over the duty range of 0 to 1. For example, a 2-leg converter will have a complete ripple cancelation only for *d=0.5*. While interleaving reduces harmonics in the passive component currents, the total volume of the separate inductors of the boost converter is higher than that of a single inductor solution [66], [68].

When the two transistor legs have opposing states, a circulating current is introduced, which is differential for each phase, and consequently does not appear at the output. This current is circulating between the two converter legs and is effectively the part of the phase current ripple that does not flow through the low-side capacitor but does flow through the high-side causing additional conduction losses.

The interleaved inductor boost converter qualities can be summarised as:

Table 2-9 IBC qualities

Energy storage:	High	Total inductor weight and size is larger than single inductor
Switch apparent power:	Low	Lowest apparent power possible
dc-side current ripple:	Very Low	Ripple reduces with number of phases
Scalability:	Medium	Depends on semiconductor technology voltage rating
Availability:	High	Faulty leg can be disabled
Reliability:	Low	High number of active switches
Function:	Boost	

2.3.3. Interleaved boost converter with coupled inductor (IBCCI)

The conventional 2-phase interleaved converter can be modified by the addition of an extra inductor L_0 and winding the individual phase inductors on the same core. When two converter legs are in opposing states, the inductor L_0 voltage is V_{dc} – ½ V_{link}, and it oscillates at twice the transistor leg switching frequency. The circulating current is limited by the high differential-mode inductance [75], [120], [68], [66]. A third alternative is to integrate L_0 and the close-coupled inductor L_{CC} into a single magnetic component. In that case, L_0 is the parallel combination of the leakage inductances of each winding [121]. A diagram of the 2-phase coupled inductor converter is shown in Figure 2-14.

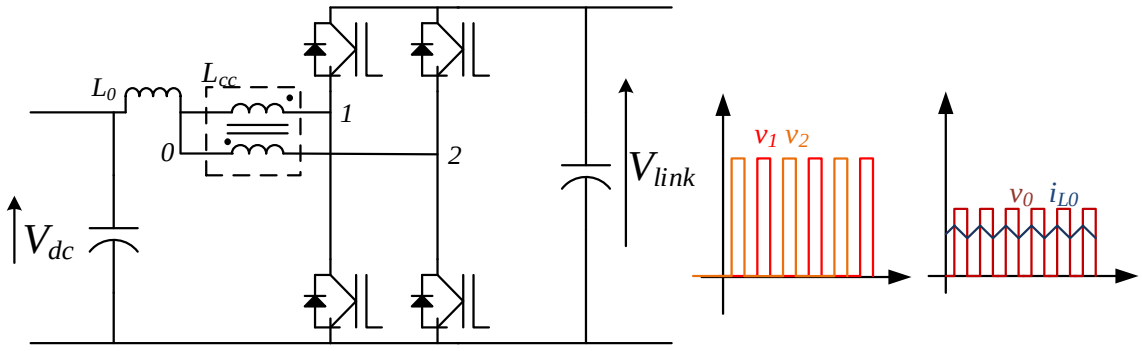

Figure 2-14 2-phase interleaved converter with close-coupled inductor

The coupled inductor can be designed with an even higher inductance by utilising the fact that each side is carrying ½ of the current of L_0, resulting in cancelation of any common mode flux. This means that no air gap is required and the close-coupled inductor can be made very small. The amplitude of the voltage across the single inductor L_0 is also reduced, as the voltage step at v_0 is ½ V_{link}, and it oscillates at twice the transistor switching frequency. To achieve the same current ripple as a single-phase boost converter, the inductor can now be almost 4 times smaller. The reduction is not quite 4-fold, as the effective duty cycle of v_0 is different from v_1 and v_2.

This converter retains the intrinsic redundancy of the interleaved converter. If one converter leg fails, the close-coupled inductor core can be saturated, and the converter

can still be operated, albeit with a much higher current ripple. Under normal operation dc current balance is mandatory between the two converter legs, as any difference between the two can result in saturation of the close-coupled inductor.

The converter can be extended to 3-phases by adding an extra winding to the close-coupled inductor [122], [123]. The interleaved boost with coupled inductor converter properties can be summarised as:

Table 2-10 Properties of the IBCCI

Energy storage:	Medium	Inductor is almost 4 times smaller than SIBC; requires interphase transformer
Switch apparent power:	Low	Lowest apparent power possible
dc-side current ripple:	Low	Inductor design parameter
Scalability:	Low	Dependent on semiconductor technology
Availability:	Medium	One phase can still operate when a fault occurs
Reliability:	High	Twice the number of switches as the SIBC
Function:	Boost	

2.3.4. Interleaved multi-phase boost converter with coupled inductors (IMPBCI)

The coupled inductor and dc inductor can be integrated into a single component, but it has been shown that using discrete parts results in a smaller size [75]. A different design of the magnetic cores, where multiple close-coupled inductors are cascaded, is shown in Figure 2-15.

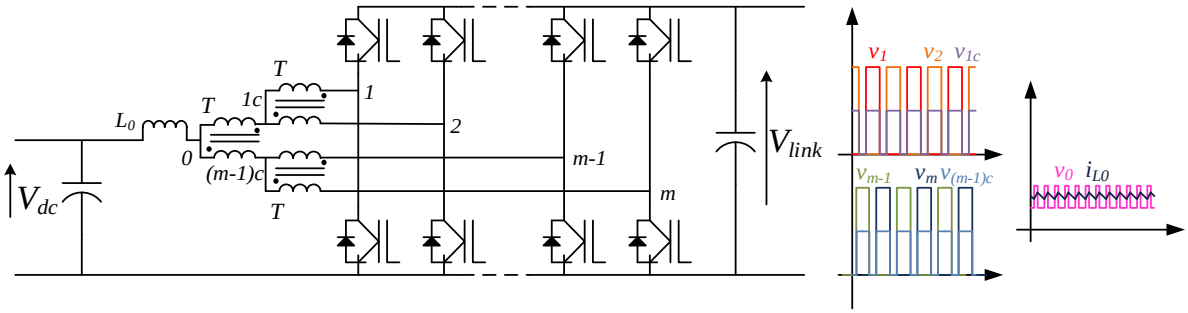

Figure 2-15 Multi-phase Interleaved converter with cascaded coupled inductors

The concept can be further extended to more phases, and the dc inductance L_0 progressively reduces in size. However, with more than two phases and a single coupled inductor, the converter loses the intrinsic redundancy typical of interleaved converters. If one phase does not carry a dc current the phase's MMF will be very small, effectively shorting the magnetic path.

At the same time the design of the coupled inductor is simplified by the lack of an air gap, and proximity effect losses depend on the circulating current and dc-current ripple, which will be designed to be small.

The multi-phase interleaved boost with coupled inductor converter properties are summarised in Table 2-11.

Table 2-11 IMPBCCI properties

Energy storage:	Low	Inductor is m^2 times smaller than SIBC, capacitor size is also reduced
Switch apparent power:	Low	Lowest apparent power possible
dc-side current ripple:	Low	Inductor design parameter
Scalability:	Medium	Transformers complicated for m>3
Availability:	Medium	Fault bypass possible
Reliability:	Low	High number of active switches
Function:	Boost	

2.3.5. Flying capacitor boost converter (FCBC)

The flying capacitor boost converter requires *2n* transistors for an *n*-level converter [72]. It uses a total of *n-1* capacitors, but they have different voltage ratings. The FCBC high-side voltage is no longer symmetrically offset from the link power rails and only connects to the middle of the series transistor chain, as shown in Figure 2-16.

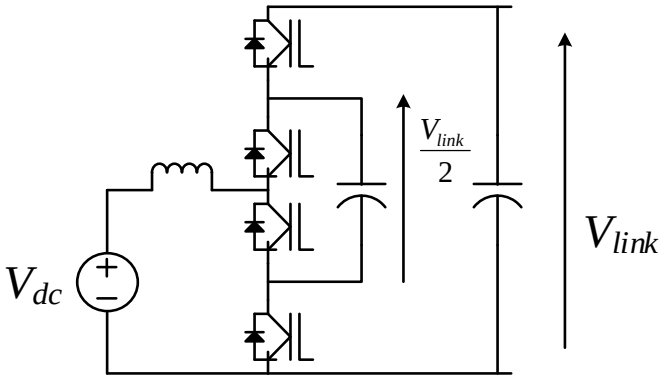

Figure 2-16 Flying capacitor boost converter

The inductor switching frequency is *n* times higher than the individual transistor switching frequency f_0, and converter voltage step is V_{link}/n. This is similar to the interleaved converter topologies, with the difference that the FCBC transistors share the same inductor current, but the required voltage rating is V_{link}/n. The converter can be

scaled up by the addition of extra pairs of transistors and flying capacitors. This converter has shown to give very high reduction of inductor size, as well as efficiency when using MOSFETs for the power switches [124]. However, it suffers from the same drawbacks as the FCI, where charging of the phase capacitors is not straightforward.

The properties of the flying capacitor boost converter are summarised in Table 2-12:

Table 2-12 FCBC properties

Energy storage:	Low	Inductor is m^2 times smaller than SIBC, capacitor size is also reduced
Switch apparent power:	Low	Lowest apparent power possible
dc-side current ripple:	Low	Inductor design parameter
Scalability:	High	Progressively higher capacitor voltage rating required for every additional level
Availability:	Medium	Fault bypass possible
Reliability:	Low	High number of active switches
Function:	Boost	

2.3.6. Three-level boost converter (TLBC)

The three-level boost converter is constructed by connecting two single-phase converters in series [125], [126]. The leg inductor can be split in two, with the return current point being the bottom converter, as shown in Figure 2-17.

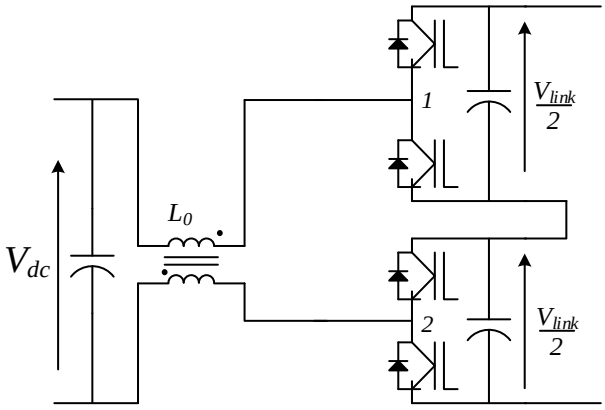

Figure 2-17 TLBC circuit diagram

The top and bottom converters can be interleaved to reduce low and high-side capacitor RMS currents. The converter is especially useful for feeding 3-level inverters, as it provides a regulated centre-split power supply. This topology is best suited to higher voltage levels, where transistors with the required voltage rating are readily available and have lower losses. It has been demonstrated that the TLBC's inductor size can be smaller than that of a SIBC or an IBC [127] and can achieve higher efficiency. However, the converter suffers from a high common-mode voltage switching component as the high-side link voltage oscillates relative to the negative point of the prime power source.

The 3-level boost converter properties can be summarised in Table 2-13:

Table 2-13 TLBC properties

Energy storage:	Medium	Inductor is smaller than SIBC
Switch apparent power:	Low	Lowest apparent power possible
dc-side current ripple:	Low	Inductor design parameter
Scalability:	Low	Only two levels possible
Availability:	Medium	Fault bypass possible
Reliability:	Medium	Twice as many switches as SIBC
Function:	Boost	

2.3.7. Isolated converters (IsoC)

Isolated converters allow for galvanic isolation and arbitrary voltage ratios between power source and link voltage. They still require large capacitors at the low and high-side terminals, as well as at least one inductor. The main challenges for isolated converters are balancing magnetic component AC losses between the ferrite cores and the windings [128]. At the same time, isolated converters can easily achieve zero-voltage switching for all semiconductor switches, drastically reducing switching losses. The main challenge for soft switching converters is maintaining zero-voltage transitions (ZVT), or zero-current transitions (ZCT), under a wide loading range. This type of system was used on a 1MW shunt locomotive [15], although exact topology details are not published.

2.3.7.1. Current-source isolated converter (CSIsoC)

Current-source isolated converters use a dc-flux inductor to approximate an ideal current source driving the transformer. The inductors used can have a small ac flux swing when low-side voltage has low steady-state variation. The converter can be either in a push-pull or full-bridge configuration [129], [130], [131]. The two-transistor bridge has simpler electronics and lower conduction losses but complicates the design of the transformer primary. It is also very sensitive to its leakage inductances.

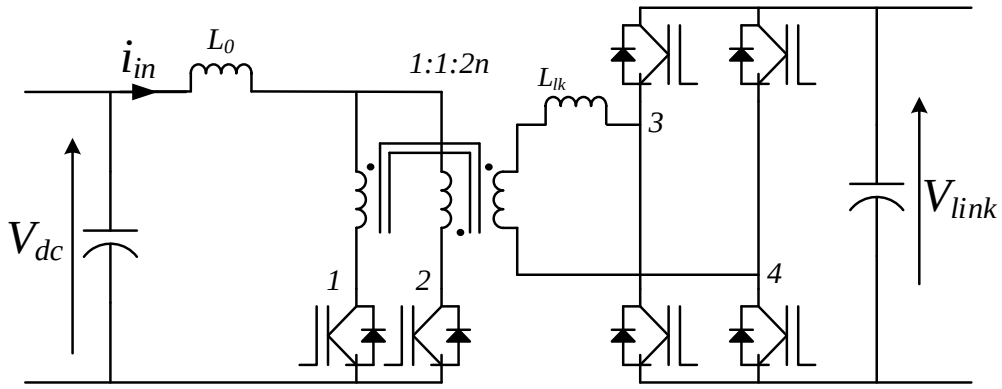

Figure 2-18 Current fed isolated converter

The push-pull current source converter is best suited to low-voltage systems, as it splits the low-side current between the two primary switches. Regardless of the configuration the converter can achieve regulation over a wide dc-side voltage range, and it also has a continuous input current. To achieve input regulation the transistor bridge switches must have a variable overlap to achieve this function, which increases the transformer RMS current and losses.

The properties of the current-source converters are summarised in Table 2-14.

Table 2-14 CSIsoC properties

Energy storage:	High	Inductor is large for wide dc-side range
Switch apparent power:	Medium	Active switches required for high efficiency
dc-side current ripple:	Low	Inductor design parameter
Scalability:	Low	Limited by semiconductor technology
Availability:	Low	Single fault makes converter inoperable
Reliability:	Low	Secondary devices do not have to be active
Function:	Buck-Boost	Arbitrary ratios can be achieved by setting the transformer winding turns ratios

2.3.7.2. Inductor fed dual active bridge (IFDAB)

This topology is a mix between the current fed converter and a dual active bridge converter. Each leg of the low-voltage side bridge doubles as a boost converter, charging a local capacitor [132], [131]. When the transformer side is included, the converter becomes a buck-boost type, and the local capacitor clamps the primary side voltage, acting as an intermediate link.

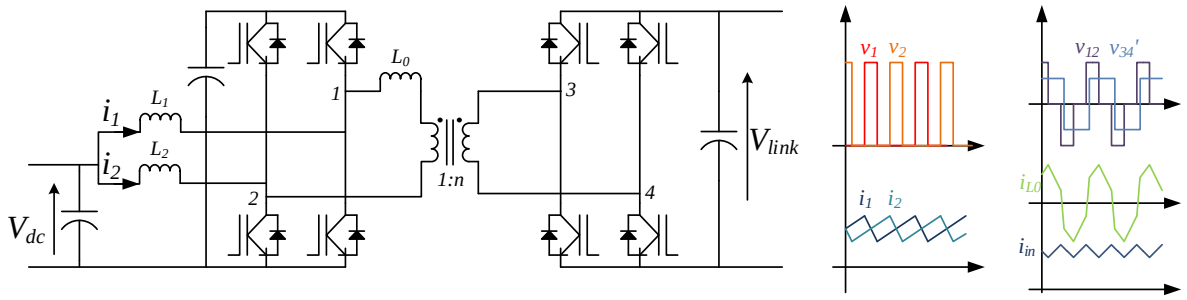

Figure 2-19 Inductor fed dual active-bridge converter

This topology has a continuous low-side current, with lower current stresses on the primary source, but still requires an ac inductor. However, to achieve wide low-side voltage regulation the transformer primary voltage is no longer a 2-level waveform, but a 3-level one, increasing primary RMS current.

The inductor-fed dual active bridge converter properties be found in Table 2-15:

Table 2-15 IFDAB properties

Energy storage:	High	Inductor is large for wide dc-side range
Switch apparent power:	Medium	Active switches required for high efficiency
dc-side current ripple:	Low	Inductor design parameter
Scalability:	Low	Limited by semiconductor technology
Availability:	Low	Single fault makes converter inoperable
Reliability:	Low	Secondary devices do not have to be active
Function:	Buck-Boost	Arbitrary ratios can be achieved by setting the transformer winding turns ratios

2.4. SINGLE STAGE BUCK-BOOST INVERTERS

Some types of inverters can achieve both buck and boost operation, necessary for driving a traction motor. These converters usually utilise one transistor bridge for both

dc-dc and dc-ac conversion. Power is provided by a voltage source or a current source, i.e. a voltage source connected via a large inductor.

2.4.1. Voltage fed Z-source inverter (VFZSI)

The bidirectional Z source inverter is comprised of a standard 6-transistor bridge, an additional semiconductor switch, as well as an impedance network comprising of two inductors and two capacitors [133], [134], [135], [136]. At the low-side the ZSI is connected to a voltage source, via a transistor. This switch is compulsory for traction drives, as at low machine speeds the ac-side current is higher than the inductor current. In this state, the ac-side current must flow through the series connection of C_1, C_2 and the dc-side source capacitance, and this must pass through Q_{aux}.

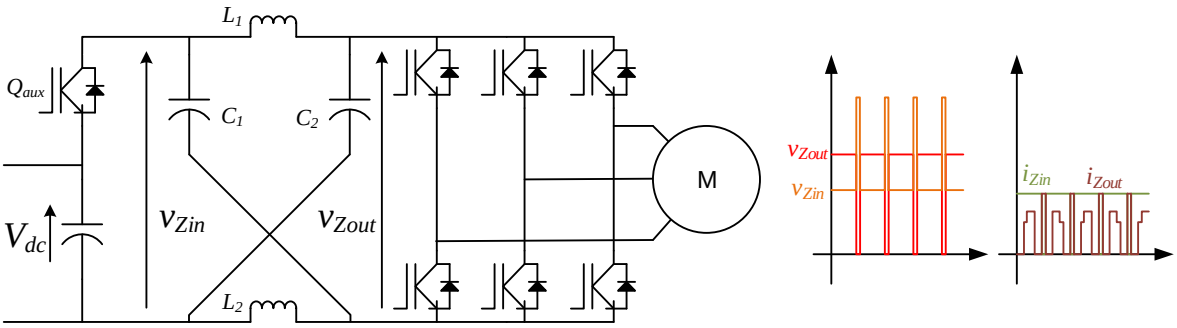

Figure 2-20 Voltage fed Z-source inverter

The ZSI achieves boost operation by inserting an overlap between the top and bottom switch of the same leg of the 3-phase bridge. The overlap creates a short circuit across the output of the impedance network, v_{Zout}, that charges the inductor from the energy storage capacitors C_1 and C_2, and during the rest of the switching cycle the low-side voltage source recharges them.

To achieve a higher boost ratio, the duration of the overlap condition needs to increase, which means the ac-side modulation index reduces. In contrast to the conventional 2-level VSI, in the ZSI the resultant peak of the fundamental phase-to-phase voltage is lower than the dc-link.

Thus, the ZSI requires a higher voltage rating of the transistors, compared to a boost converter plus VSI configuration, but it requires one transistor less. The ZSI input current has a higher RMS value, as the current drawn from the low-side source has a rectangular waveform.

Depending on the modulation scheme, the oscillating frequency of v_{Zout} is either 2, 3, or 4 times the switching frequency, resulting in a small inductor value. L_1 and L_2 can be wound on the same core, with a high coupling factor, to reduce the total inductance value. However, Q_{aux} and the 6 bridge transistors are also switching at the same frequency as v_{Zout}, increasing switching losses. Properties of this converter are summarised in Table 2-16.

Table 2-16 VFZSI properties

Energy storage:	High	Two high-voltage capacitors required; inductors still large
Switch apparent power:	Medium	Overrating required
dc-side current ripple:	High	Pulsed current, requires inductor filter
ac-side voltage step:	High	Equal to sum of capacitor voltages
Machine current THD:	High	High-voltage inverters have low switching frequency
Scalability:	Low	Wholly dependent on semiconductor technology
Availability:	Low	Single switch makes drive inoperable
Reliability:	High	Only one additional active device
Function:	Buck-Boost	

2.4.2. Voltage-fed quasi Z-source inverter (QZSI)

A bidirectional QZSI uses the same components as the ZSI, but in a different arrangement. The low-side voltage source is connected directly to the power inductor, and the auxiliary switch is moved [137], [138], [139]. Compared to the ZSI the inductor current is smaller, as it flows through the low-side source, and the two capacitors C_1 and C_2 have different steady-state voltages. In other respects, the converter operates the same way as the ZSI, having the same v_{Zout}, ac-side currents, and device stresses.

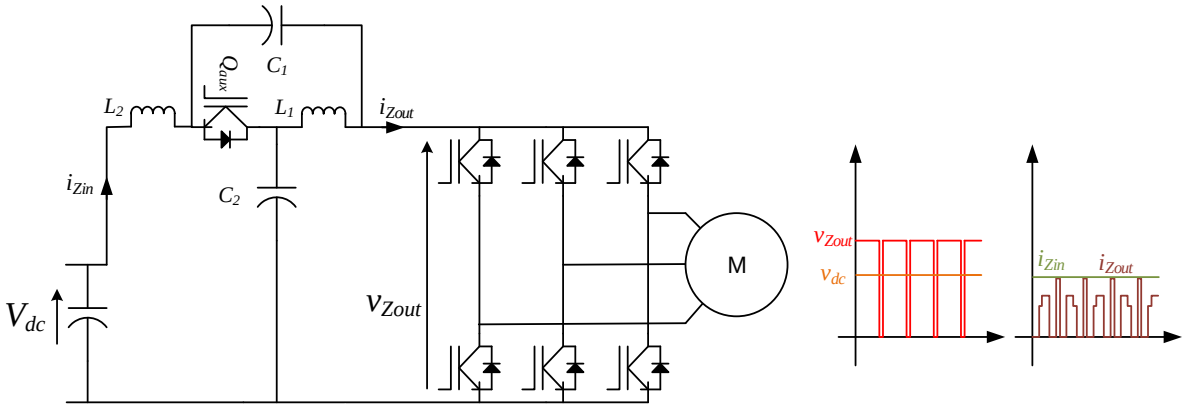

Figure 2-21 Voltage fed QZSI

The QZSI can interface additional power sources by connecting them in parallel with either C_1 or C_2. The QZSI properties are summarised in Table 2-17.

Table 2-17 QZSI properties

Energy storage:	High	Two high-voltage capacitors required; inductors still large
Switch apparent power:	Medium	Overrating required
dc-side current ripple:	Low	Inductor design parameter
ac-side voltage step:	High	Equal to sum of capacitor voltages
Machine current THD:	High	High-voltage inverters have low switching frequency
Scalability:	Low	Wholly dependent on semiconductor technology
Availability:	Low	Single switch makes drive inoperable
Reliability:	High	Only one additional active device
Function:	Buck-Boost	

2.4.3. Current-fed quasi Z-source inverter (CFQZSI)

This type of inverter has the same transistor bridge as a conventional CSI, with the input connected to an impedance source network, as well as a third inductor that provides a connection to the low-side voltage source [140], [141]. A schematic of the converter is shown in Figure 2-22:

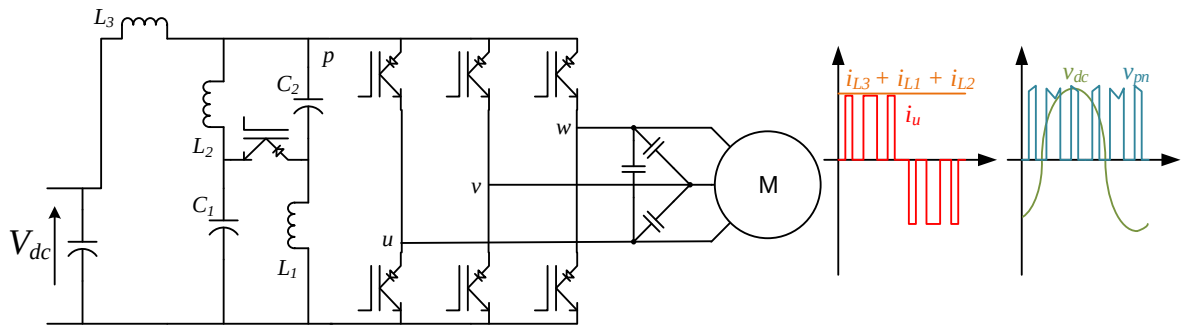

Figure 2-22 Current-fed quasi Z-source inverter

Like the CSI, the current fed QZSI benefits from the low THD of the output waveform, but still requires two large capacitors for the impedance network. Importantly, however, the current fed QZSI is a current source inverter that can buck the ac-side voltage, with only one additional semiconductor. This auxiliary switch must be either a diode or a reverse blocking transistor, with the former only usable for voltage boost ratio less than 2 [141]. If a reverse blocking transistor is used instead, higher voltage gain can be achieved, but similar to the other impedance source converters, the modulation index reduces as boost factor increases, as they are complementary.

While the current fed QZSI has been shown to operate in all 4 quadrants, the transition from positive to negative power flow is very abrupt, which makes the converter difficult to control. Additionally, the use of the auxiliary switch is not well explored, and most of the work on this inverter is done using a diode. This configuration can achieve a voltage gain less than 2, which is a limitation. Converter properties are summarised in Table 2-18:

Table 2-18 CFQZSI properties

Energy storage:	High	3 inductors required
Switch apparent power:	Medium	Overrating required
dc-side current ripple:	Low	Inductor design parameter
ac-side voltage step:	Low	Ac-side capacitor design parameter
Machine current THD:	Low	CSI-type converter
Scalability:	Low	Wholly dependent on semiconductor technology
Availability:	Low	Single switch makes drive inoperable
Reliability:	High	Only one additional active device
Function:	Buck-Boost	

2.5. PROPOSED CONVERTER: BOOST MULTILEVEL CASCADED INVERTER (BMCI)

The review of published literature has shown that the single-stage topologies in general have the advantage of simplicity but are limited by semiconductor technology, motor current harmonic distortion, ac-side voltage step, and the size of the passive components.

To address these issues, this thesis presents a new application of the modular cascaded converter with full-bridge cells – as a buck-boost single-stage inverter, to tackle the following problems: size of power inductor, high WTHD, and the need for intrinsic fault tolerance. The converter has the standard MCC structure but is used to boost the dc-side voltage. The submodules are constructed using transistor H-bridges, and each one

can produce both positive and negative voltages by inverting the voltage of the local energy storage capacitor. The schematic of the proposed BMCI is shown in Figure 2-23:

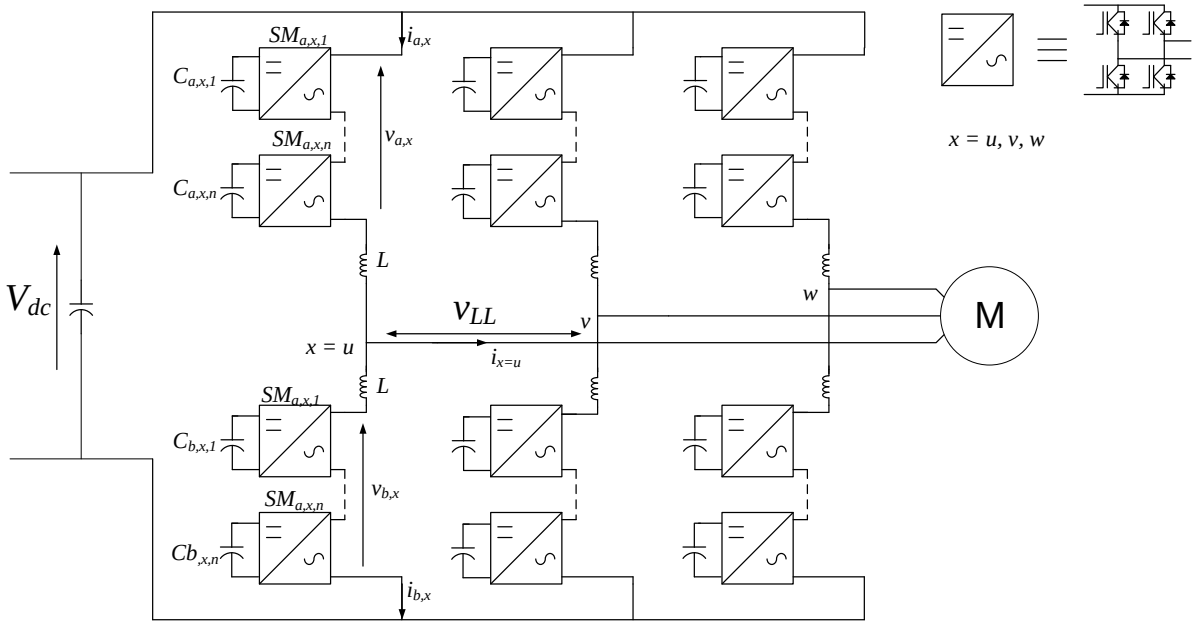

Figure 2-23 Proposed boost modular cascaded inverter

The dc-side capacitor is used to absorb the combined inductor current ripple and, like other dc-dc boost converters, can be omitted. As with the standard MCC each converter leg has a pair of inductors, and by increasing the number of sub-modules in each arm, the required inductance reduces at an almost quadratic rate. A key difference of the BMCI is that for the same sub-module voltage it can produce a higher peak line-to-line voltage.

The first key benefit of the proposed topology is the big reduction in total leg inductance, and consequently its weight and volume. This is a consequence of the multi-level nature of the converter, which also makes the ac-side voltage quasi-sinusoidal. As this project demonstrates in Chapters 6 and 7, the BMCI can produce machine currents with very low THD and the maximum ac-side voltage step equal to a-sub-module's capacitor voltage. In a practical application, these features are expected to have a positive effect on traction motor efficiency, as well as motor insulation and bearing longevity.

The second major benefit is that the BMCI can be scaled up in power by increasing the number of sub-modules in an arm – this quality is desirable for railway traction applications, where there is a significant variability of the power rating for different trains. At the same time, the leg inductance is a function of effective arm switching frequency and sub-module capacitor voltage. When the BMCI is scaled with more sub-modules, the effective arm switching frequency increases, and as long as the system terminal currents remain constant, power inductor value will actually decrease. In contrast, for any 2-level boost converter the inductor value increases, as both the peak voltage and semiconductor switching frequency losses are higher.

A combination of a multilevel inverter and multilevel dc-dc converter could have the same benefits as the proposed BMCI. However, this type of system cannot achieve the same availability, as a single switch open-circuit fault will cause a converter to become inoperable, unless redundant switches are included in the system [142], [143], [144]. The BMCI has intrinsic fault tolerance because sub-modules can be bypassed, as long as two of its active switches are operational. Multiple fault management strategies have been developed for this purpose [145], [146], [147], [148], [149].

The practical design of a BMCI is discussed in section 5.1 with an example system simulated in Chapter 6, and also compared to a conventional BVSI design. The results of the design show that the BVSI topology has 22% higher volume of capacitors and inductors and 370% heavier mass of the energy storage components. The BMCI achieves these results at the cost of lower efficiency, which would result in more power that needs to be dissipated. Albeit this is a shortcoming of this topology, it has to be noted that for traction applications the energy efficiency has secondary importance to the overall weight and volume, as any additional weight requires more energy to propel the train, nullifying

the benefits of a higher efficiency and, sometimes, even increasing the total energy consumption.

The properties of the proposed converter are summarised in Table 2-19:

Table 2-19 Summary of the proposed BMCI properties

Energy storage:	High	Large total capacitance
Switch apparent power:	High	Medium
dc-side current ripple:	Low	Inductor design parameter
Scalability:	High	Power rating can be increased by adding more sub-modules
Availability:	High	Tolerates both short circuit and open-circuit fault without additional switches
Reliability:	Low	High number of active switches
Function:	Buck-Boost	Enabled by the full-bridge converter cells

2.6. SUMMARY

This chapter has examined current state-of-the-art of 3-phase inverter drives, dc-dc boost converters and single-stage buck-boost inverters, suitable for motor drives of electric trains powered by hydrogen fuel cells. Different converter topologies have been compared, based on power density, system complexity, and converter specific functionality, summarising the advantages and disadvantages of each, when used in a railway traction application. Non-isolated converters have a lower cost and can achieve very high efficiency without using soft-switching techniques. The state-of-the-art topology is based on interleaving multiple converter legs, using non-coupled or close-coupled inductors to reduce the total energy stored in the power inductor. This technique

gives the high overall converter power density, but in practice the number of converter phases is limited to 2 or 3, as the design of the close-coupled inductor becomes more difficult with more phases and converter fault tolerance decreases drastically.

Isolated converters also offer very high efficiency, but require more transistors, a power inductor and energy storage capacitors, which limit the maximum achievable power densities. Additionally, the isolation transformer increases system cost, as it must be carefully designed to balance the multiple loss mechanisms.

To overcome the main limitations of the boost inverter topologies, presented in the literature, this thesis has proposed to use the modular cascaded converter with full bridges controlled as a boost modular cascaded inverter (BMCI). This topology achieves both ac-side voltage buck and boost, while inverting a dc voltage, in a single converter stage. The proposed BMCI benefits from multi-level ac-side voltage waveform, intrinsic fault tolerance, and mainly – a reduction in the size of the leg inductors. Unlike the interleaved converters, discussed earlier in this chapter, the inductance reduction is only limited by the number of sub-modules. Thus, the converter design can be optimised in terms of power density or system cost with a balance between the number of sub-modules, the device voltage ratings, the capacitor voltage rating, and the leg inductance. Moreover, the BMCI can tolerate short circuit faults both at its dc-side and ac-side terminals, as well as internal faults in one of its sub-modules. For these reasons, the BMCI is particularly suitable for applications where the low-side dc voltage reduces as power increases, such as hydrogen fuel for railway vehicles.

A comparison between all the converters reviewed can be found in Table 2-20.

Table 2-20 Comparison table for power converters suitable for fuel cell electric vehicles

	Low is best					*High* is best			
Converter topology	*Energy storage*	*Switch kVA*	*Current ripple*	*Voltage step*	*Current THD*	*Scalability*	*Availability*	*Reliability*	*Function*
VSI	Low	Low	High	High	High	Low	Low	High	Buck
IVSI	Medium	Low	Medium	Medium	Low	Medium	Medium	Low	Buck
CSI	High	Medium	Low	Low	Low	Low	Low	High	Boost
NPC	Low	Medium	High	Medium to Low	Low	Medium	Low	Low	Buck
FCI	Medium	Low	High	Medium to Low	Low	Medium	Low	Low	Buck
CHBI	High	High	Medium	Low	Low	High	High	Low	Buck-boost
MCC	High	High	Low	Low	Low	High	Medium	Low	Buck
SIBC	High	Low	Low	NA	NA	Low	Low	High	Boost
IBC	High	Low	Low	NA	NA	Medium	High	Low	Boost
IBCCI	Low	Low	Low	NA	NA	Low	Medium	Medium	Boost
IMBCCI	Low	Low	Low	NA	NA	Medium	Low	Low	Boost
FCBC	Low	Low	Low	NA	NA	High	Low	Low	Boost
TLBC	Medium	Low	Low	NA	NA	Low	Low	Medium	Boost
CSIsoC	High	Medium	Low	NA	NA	Low	Low	Medium	Boost
IFDAB	High	Medium	Low	NA	NA	Low	Low	Medium	Boost
VFZSI	High	Medium	High	High	High	Low	Low	High	Buck-boost
QZSI	High	Medium	Low	High	High	Low	Low	High	Buck-boost
CFQZSI	High	Medium	Low	Low	Low	Low	Low	Medium	Buck-boost
BMCI	High	High	Low	Low	Low	High	High	Low	Buck-boost

Chapter 3. MODELLING OF BOOST MULTILEVEL CASCADED INVERTERS

This chapter examines the structure and the operation of the boost multilevel cascaded inverter (BMCI). The converter circuit equations are used to construct a continuous-time model that can be used for numerical simulations, and then the large and small-signal analytical models are derived for use in control system design. The maximum voltage boost ratio is also analytically investigated.

3.1. PRINCIPLE OF OPERATION

The basic building block of the BMCI is the sub-module, which is made of a transistor full-bridge and a voltage-source energy storage element, i.e. capacitor, battery or another power converter. The transistor bridges are controlled with pulse-width modulation to vary the average ac-side voltage. The half bridge (HB) sub-module uses a single duty cycle $d_1 \in [0,1]$ while the full bridge (FB) has one for each transistor leg – $d_1 \in [0,1]$ and $d_3 \in [0,1]$, that can be represented as a single bipolar active duty cycle $d_a = d_1 - d_3$, $d_a \in [-1,1]$. The duty cycles are compared with a sawtooth (in the case of HB modules) and triangular (full-bridge) carriers according to (3-1):

$$f(d) = \begin{cases} 1, & d > carrier \\ 0, & d \le carrier \end{cases} \qquad (3\text{-}1)$$

The allowed switching states and the average voltage inserted by each sub-module can be found in Table 3-1 and Table 3-2, while the basic sub-module circuits, and associated waveforms, can be seen in Figure 3-1. It should be noted that for the same sub-module output switching frequency the FB carrier is at half the frequency of the HB converter.

Table 3-1 Switching states and average output voltage for a half-bridge sub-module

v_{SM}	Q1	Q2	$mean(v_{SM})$
0	0	1	$d_1 V_C$
$+V_C$	1	0	

Table 3-2 Switching states and average output voltage for a full-bridge sub-module

v_{SM}	Q1	Q2	Q3	Q4	$mean(v_{SM})$
0	0	1	0	1	$d_a V_C = (d_1 - d_3) V_C$
$+V_C$	1	0	0	1	
0	1	0	1	0	
$-V_C$	0	1	1	0	

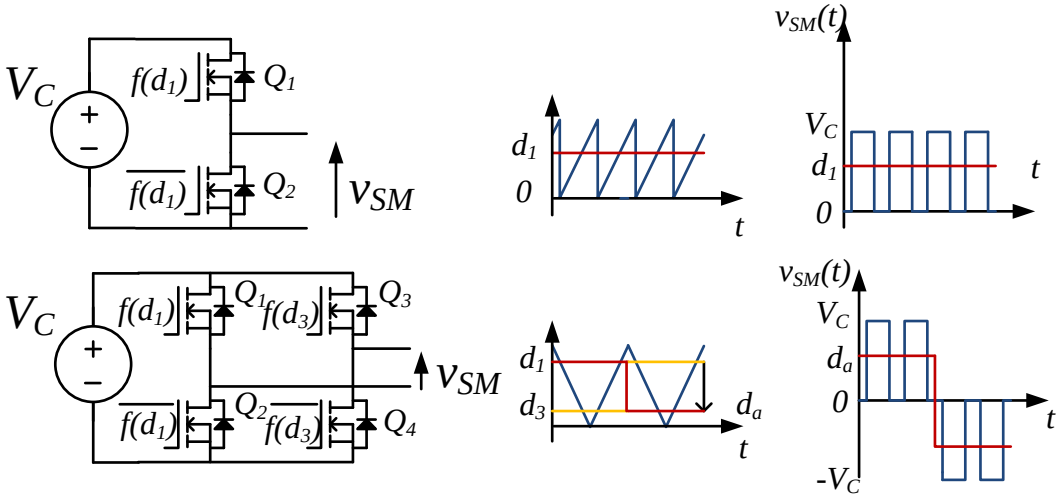

Figure 3-1 Half-bridge and Full-bridge sub-modules with their respective modulation and output waveforms

In an MCC *n* sub modules are connected in series with one another, forming a converter arm, and a single inductor. The inductor provides current filtering and allows the arm to function as a controlled voltage source, as shown in Figure 3-2.

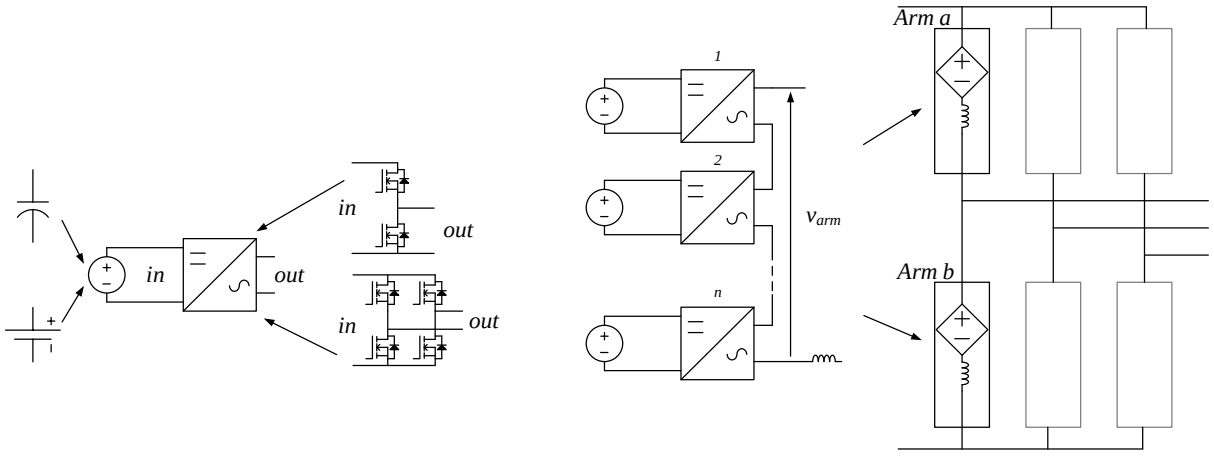

Figure 3-2 MCC building blocks

In a 3-phase dc-ac MCC a pair of converter arms form a phase leg, that functions as a single-phase voltage-source inverter. The output phase current is shared equally between the top and bottom arm, while the dc-side current is common to both, as indicated in (3-2):

$$i_{L,a,x} = \frac{i_{dc}}{3} + \frac{i_x}{2}$$
$$i_{L,b,x} = \frac{i_{dc}}{3} - \frac{i_x}{2} \qquad (3\text{-}2)$$

When operated with a balanced load, the dc-side current flows between the dc power supply and the converter arms, while the ac-side currents are sourced by the converter and pass through the 3-phase load, as illustrated in Figure 3-3.

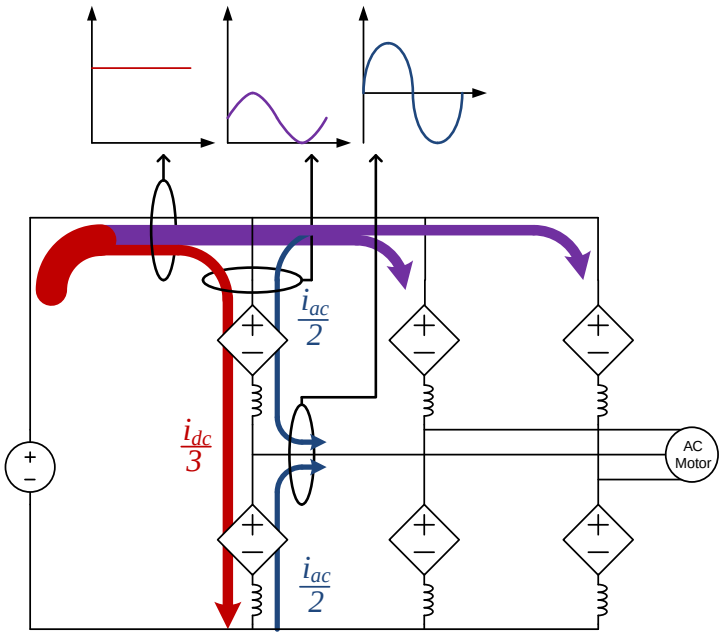

Figure 3-3 Schematic diagram for the current flow in MCCs

To achieve decoupled control of dc and ac currents, each converter arm has two separate control variables that are used to calculate the individual sub-module duty cycles – the dc duty cycle d_{dc} and the ac duty cycle d_{ac}. Assuming equal voltage V_C across all floating capacitors, the inserted voltages for each phase x= u, v, w, can be found using (3-3) and (3-4).

$$\begin{aligned} d_{a,x} &= d_{dc,x} - d_{ac,x} \\ d_{b,x} &= d_{dc,x} + d_{ac,x} \end{aligned} \tag{3-3}$$

$$\begin{aligned} v_{a,x} &= d_{a,x} n V_C = \left(d_{dc,x} - d_{ac,x}\right) n V_C \\ v_{b,x} &= d_{b,x} n V_C = \left(d_{dc,x} + d_{ac,x}\right) n V_C \end{aligned} \tag{3-4}$$

The dc-side and ac-side voltages become:

$$v_{dc,x} = v_{a,x} + v_{b,x} = 2 d_{dc,x} n V_C \tag{3-5}$$

$$v_{ac,x} = \frac{v_{b,x} - v_{a,x}}{2} = d_{ac,x} n V_C \tag{3-6}$$

In (3-5) the top and bottom arm voltages are complementary, and any large differences in the resultant dc voltage would cause high currents to be drawn from the

power supply. For a HB converter, many control schemes keep the average voltage level across the capacitors at $V_C = {V_{dc}}/{n}$, resulting in the inserted voltages:

$$\begin{aligned} v_a &= (d_{dc} - d_{ac}) n V_C = (d_{dc} - d_{ac}) V_{dc} \\ v_b &= (d_{dc} + d_{ac}) n V_C = (d_{dc} + d_{ac}) V_{dc} \end{aligned} \quad (3\text{-}7)$$

The ac-duty cycle $d_{ac,x}$ is calculated using the converter modulation index m, ac-side frequency ω, and phase shift φ_x:

$$d_{ac,x} = m \times \sin(\omega t - \varphi_x)(1 - d_{dc,x}) \quad (3\text{-}8)$$

Since the maximum duty ratio of a transistor is 100%, the arm duty cycle is limited to $d_{ac,x}(t) + d_{dc,x}(t) = 1$. For a HB sub-module there is the additional limitation $d_{ac,x}(t) + d_{dc,x}(t) \geq 0$. If the modulation index is set to 1, the peak ac-side voltage becomes dependent solely on the dc duty-cycle:

$$v_{ac,x} = d_{ac,x} n V_C = d_{ac,x} V_{dc} \quad (3\text{-}9)$$

$$v_{ac,x,peak} = 0.5 - |0.5 - d_{dc,x}| V_{dc} \quad (3\text{-}10)$$

From (3-12) it is clear that the maximum $v_{ac,x,peak}$ occurs at $d_{dc,x}=0.5$. The peak output line-to-line voltage range of the HB MCC is limited by the dc-supply. While this implies that the converter is a pure buck-type, this is not exactly the case. An analogy is a Cuk converter, where energy from the input is stored in a floating capacitor and then released into the load. One key difference is that the dc-ac energy transfer occurs over one cycle of the ac waveform instead of one cycle of the switching carrier. If the arm duty cycle can have a negative value, the phase ac voltage can go beyond the dc voltage rails, producing an ac voltage higher than the dc side, which is illustrated in Figure 3-4.

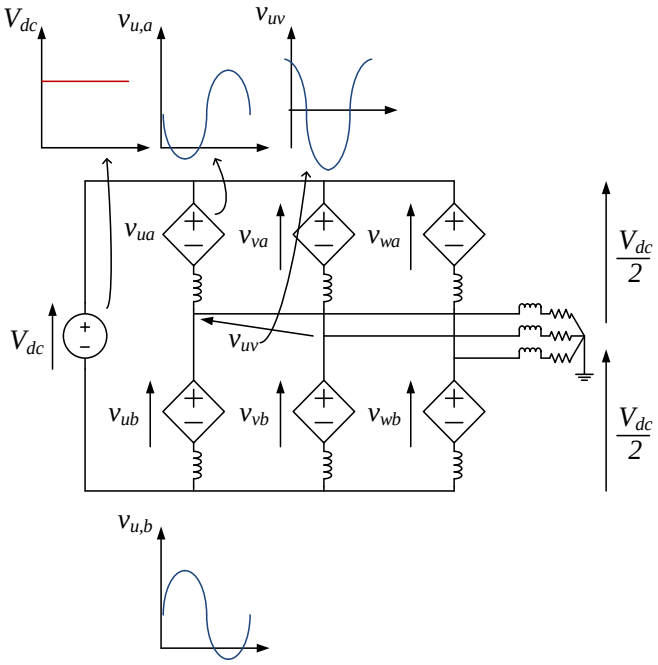

Figure 3-4 Boost function of the FB MCC

As the ac-side voltage is now dependent on the average capacitor voltage, the maximum peak phase voltage becomes:

$$v_{ac,x,peak} = \frac{(1-d_{dc,x})}{2d_{dc,x}} V_{dc} \qquad (3\text{-}11)$$

Equation (3-11) shows that as $d_{dc,x} \to 0$, $v_{ac,x,peak} \to \infty$. This is typical of boost and buck-boost converters. As such the MCC has a limit on the maximum achievable boost, that depends on the parasitic resistances.

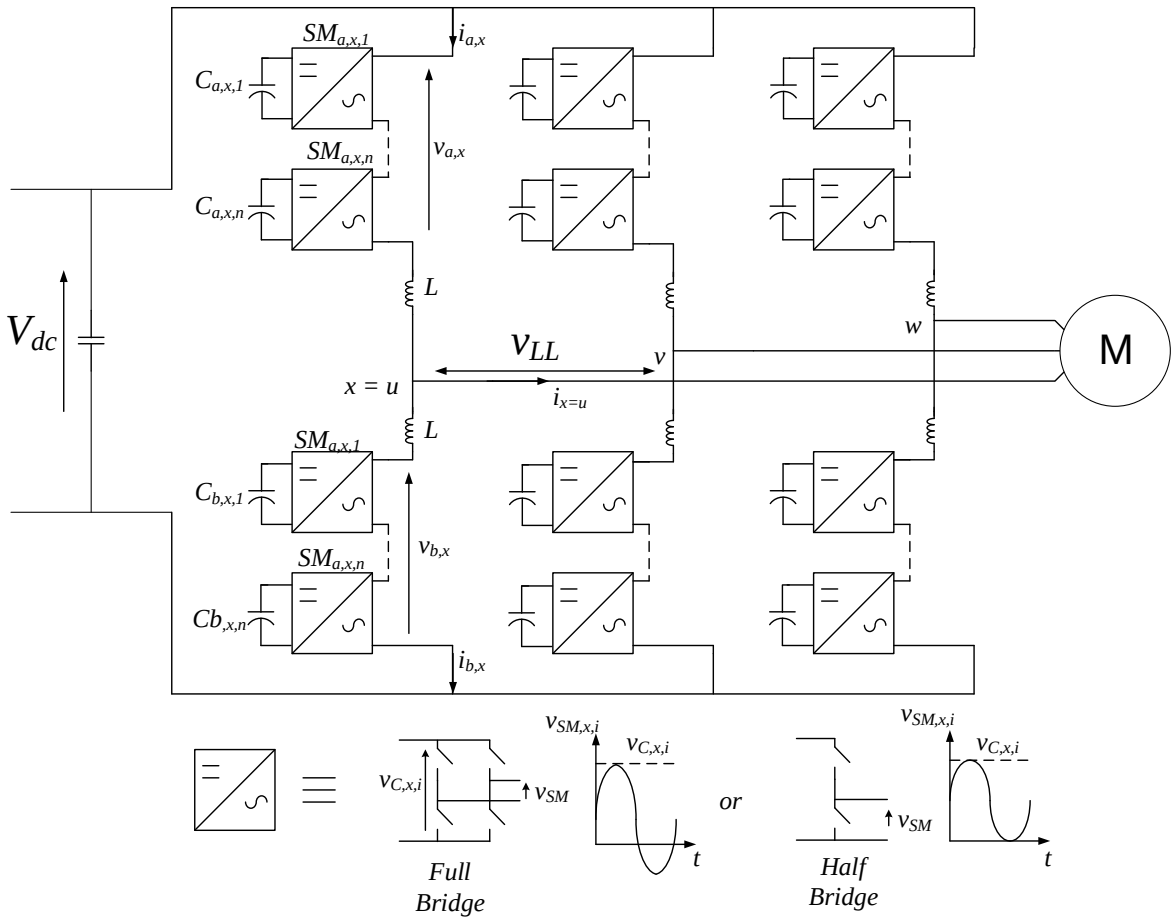

Figure 3-5 Structure of a general MCC and difference between full and half bridge sub-modules, with typical mean sub-module output voltages.

To summarise, the HB sub-module is limited by the unipolar nature of its ac voltage, while the FB sub-module, with its bipolar output, allows the FB MCC to produce both positive and negative voltages, that give boost functionality, shown in Figure 3-5. Therefore, the BMCI proposed in this thesis is based on FB (H-bridge) MCC topology.

3.2. MATHEMATICAL MODELLING

To get a better understanding of the converter dynamics, and to create a model for numerical simulation, the equations that describe the BMCI are derived. The type of semiconductor switches used can vary, depending on required current carrying capability. To simplify the modelling, the transistor switch is a MOSFET, as its ON characteristics can be modelled by a series resistor. The resistive qualities are also

favourable at low dc voltages, where the series connection of multiple IGBTs, and their saturation voltage drops, can cause severe loss of headroom. Switch current capacity can be increased by paralleling more MOSFETs, reducing power dissipation, per device, in a quadratic manner.

For this section, the circuit diagram of the BMCI contains the transistor, inductor, and capacitor parasitic resistances and is shown in Figure 3-6.

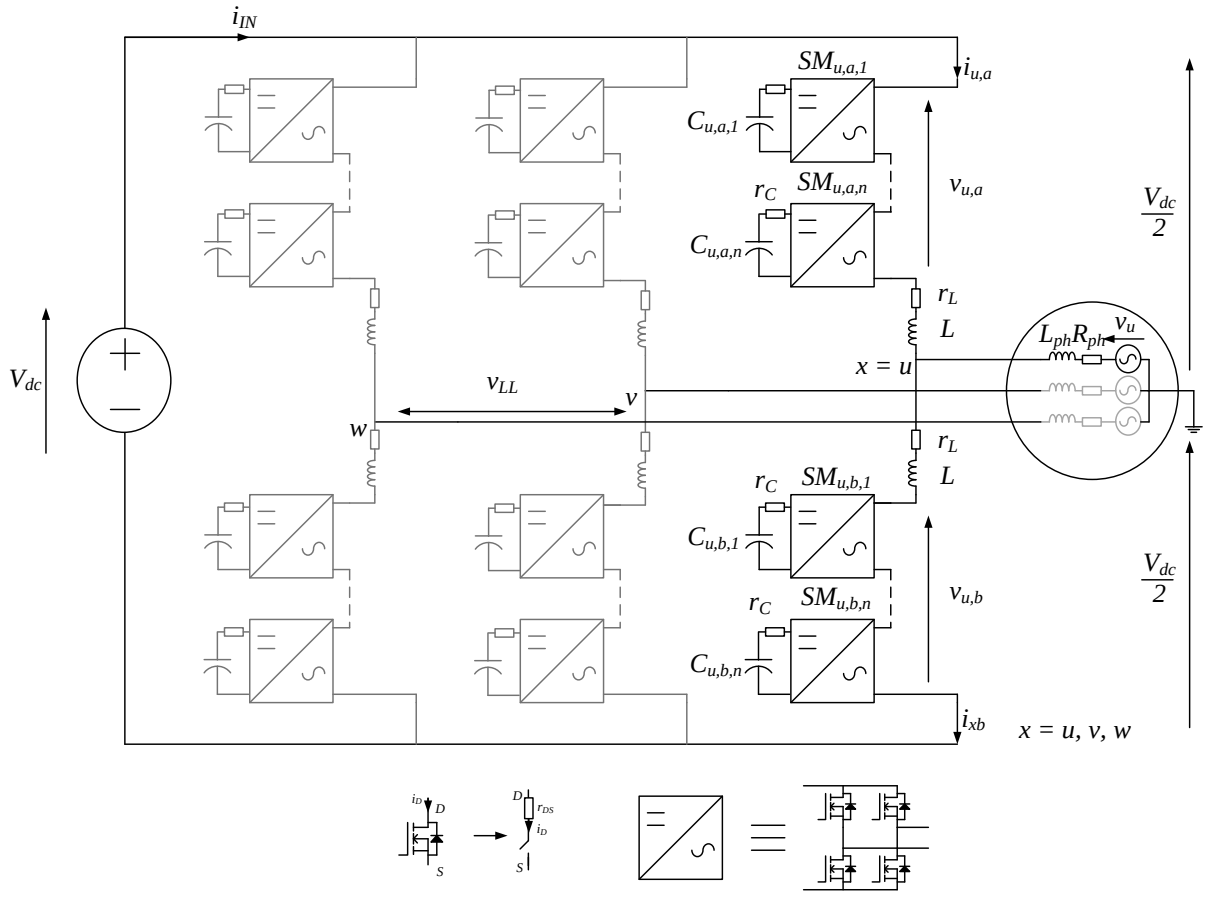

Figure 3-6 BMCI model including parasitic resistances

As the converter is driving a balanced passive load, with line inductance L_{ph} and resistance R_{ph}, the load star-point voltage is at exactly half the input dc voltage. Since each phase leg is effectively a single-phase inverter, only one pair of top and bottom arms, with their phase load, needs be analysed.

Each sub-module consists of 4 transistor switches and a floating capacitor, each having a series parasitic resistance, as shown in Figure 3-7. Parasitic inductances and switch

capacitances are ignored as they have negligible effect on the average converter operation.

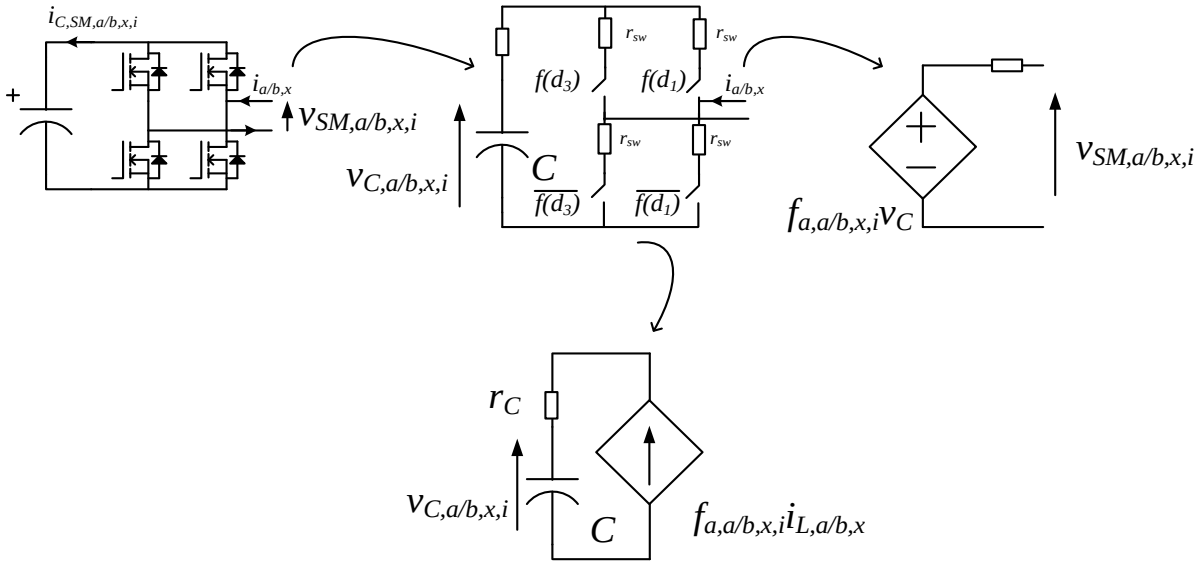

Figure 3-7 Generic sub-module and equivalent circuits used for modelling

The sub-module with capacitance C has two circuits associated with it – the one seen at its terminals and the internal capacitor circuit. Basically, the sub-module capacitor is seen as a switched voltage source from the rest of the converter, while the capacitor sees the switched arm current. The transistor states are controlled by the sub-module switching function $f_{a,a/b,x,i}$, which has an input $d_{a,a/b,x,I}$ and operates according to Table 3-2. The circuits can be described by:

$$v_{SM,a/b,x,i}(t) = f\left(d_{a,a/b,x,i},t\right)v_{C,a/b,x,i}(t) + \underbrace{\left(2r_{SW} + f\left(d_{a,a/b,x,i},t\right)\times r_C\right)}_{r_{SM,a/b,x,i}} \times i_{a/b,x}(t) \quad (3\text{-}12)$$

$$v_{C,a/b,x,i}(t) = \frac{1}{C}\int f\left(d_{a,a/b,x,i},t\right)\times i_{a/b,x}(t)dt \quad (3\text{-}13)$$

$$v_{a/b,x}(t) = \sum_{i=1}^{n} v_{C,a/b,x,i}(t) + \left(\sum_{i=1}^{n} r_{SM,a/b,x,i}(t)\right)\times i_{a/b,x}(t) \quad (3\text{-}14)$$

$$r_{SM,a/b,x,i}(t) = 2r_{SW} + f\left(d_{a,a/b,x,i},t\right)\times r_C \quad (3\text{-}15)$$

The load is modelled as a voltage source with a series inductance and resistance. This configuration is suitable for modelling traction motors, a 3-phase supply, or a passive load, if the 3-phase sources are set to 0. The phase inductance is a point of coupling between each pair of arm currents and must be included in each of the arm equations:

$$L\frac{di_{L,a,x}}{dt} + L_{ph}\frac{di_x}{dt} = -\left(r_L + \sum_{i=1}^{n} r_{SM,a,x,i}(t)\right)i_{L,a,x} - R_{ph}i_x - \sum_{i=1}^{n} d_{a,a,x,i}(t)v_{C,a,x,i}(t) + \left(\frac{V_{dc}}{2} - v_u(t)\right) \quad (3\text{-}16)$$

$$L\frac{di_{L,b,x}}{dt} - L_{ph}\frac{di_x}{dt} = -\left(r_L + \sum_{i=1}^{n} r_{SM,b,x,i}(t)\right)i_{L,b,x} + R_{ph}i_x - \sum_{i=1}^{n} d_{a,b,x,i}(t)v_{C,b,x,i}(t) + \left(-\frac{V_{dc}}{2} + v_u(t)\right) \quad (3\text{-}17)$$

$$\frac{di_x}{dt} = \frac{di_{L,a,x}}{dt} - \frac{di_{L,b,x}}{dt} \quad (3\text{-}18)$$

Using (3-13) through (3-18), the state-space model of the converter can be derived as follows:

$$M\,\dot{x} = Ax + Bu \qquad y = Cx \tag{3-19}$$

The converter state matrix and state feedback matrix become:

$$x = \begin{pmatrix} i_{L,a,x} \\ i_{L,b,x} \\ i_x \\ \sum_{i=1}^{n} v_{C,a,x,i} \\ \sum_{i=1}^{n} v_{C,b,x,i} \end{pmatrix} \tag{3-20}$$

$$A = \begin{pmatrix} -\left(r_L + \sum_{i=1}^{n} r_{SM,a,x,i}\right) & 0 & R_{ph} & \sum_{i=1}^{n} f\left(d_{a,a,x,i}\right) & 0 \\ 0 & -\left(r_L + \sum_{i=1}^{n} r_{SM,b,x,i}\right) & -R_{ph} & 0 & \sum_{i=1}^{n} f\left(d_{a,b,x,i}\right) \\ 0 & 0 & 0 & 0 & 0 \\ -\sum_{i=1}^{n} f\left(d_{a,a,x,i}\right) & 0 & 0 & 0 & 0 \\ 0 & \sum_{i=1}^{n} f\left(d_{a,b,x,i}\right) & 0 & 0 & 0 \end{pmatrix} \tag{3-21}$$

The state equation input matrix *B* and cross-coupling *M* are:

$$B = \begin{pmatrix} V_{dc} - v_x \\ -V_{dc} + v_x \\ 0 \\ 0 \\ 0 \end{pmatrix} \tag{3-22}$$

$$M = \begin{pmatrix} L + L_{ph} & 0 & 0 & 0 & 0 \\ 0 & L - L_{ph} & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{pmatrix} \tag{3-23}$$

This model is time-variant, as it depends on switching functions. While it cannot be directly solved analytically, it is well suited for numerical simulation in Matlab Simulink®.

3.3. AVERAGE-TIME MODEL

A BMCI can separately control the dc-side and ac-side currents, as it stores energy in its sub-module capacitors. The accurate design of the control systems requires an analytical model describing the converter dynamics at different operating conditions. To remove the instantaneous effects of the power transistor switching action state-space averaging can be used. It is a popular method that derives an equivalent linear time-invariant system and produces a transfer function, with which classical control methods can be used.

A single leg of an *n*-module converter phase leg has *n+2* energy storage elements, not including any load inductance. To simplify the model all capacitors, within the same arm, are lumped into one element, as it can be assumed that all sub-modules have equal capacitance, duty cycle, and mean capacitor voltages. This is justified as a real converter would have a control system dedicated to charge equalisation within the arm, and energy balance between top and bottom arms.

As the capacitors are the main energy storage elements, the dc-side current control system will be regulating the average sub-module capacitor voltage for each leg, while the ac-side currents are controlled by the motor vector controller. This setup is equivalent to a buck-boost converter cascaded with a voltage source inverter, where the dc-side converter is regulating the average capacitor voltage, and the inverter is fed, effectively, by a “stiff” dc-link.

Like section 3.1 the analysis of a single converter leg can be sufficient for modelling the converter. This is also a practical solution as there would be a separate controller regulating each leg’s average capacitor voltage. An equivalent circuit of a converter leg can be seen in Figure 3-8.

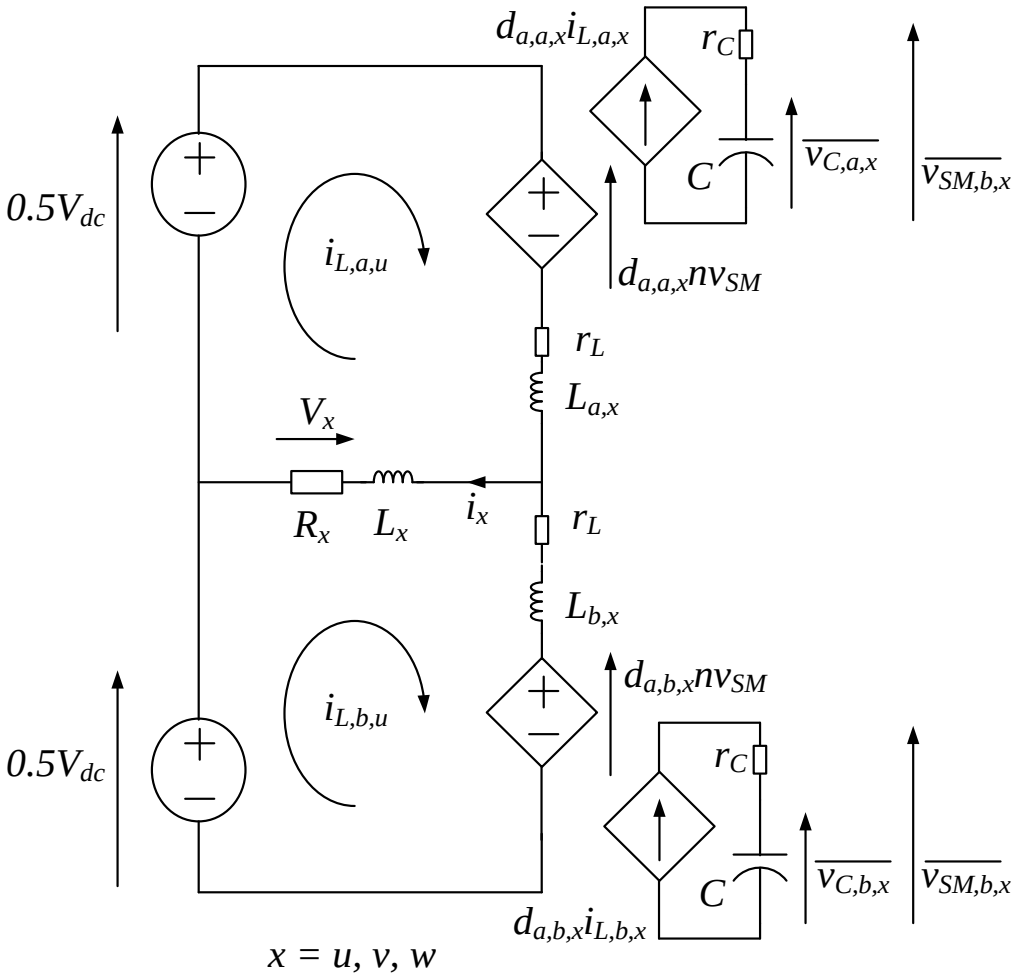

Figure 3-8 Equivalent circuit of an MCC leg

The switching functions are replaced by a continuous voltage equal to the arm's duty cycle multiplied by the corresponding average sub-module voltage. The voltage sources are averaged over one switching cycle of the semiconductor switches. The capacitor average voltage, however, is taken over one cycle of the ac-side waveform, as this period marks a complete energy transfer from the dc-side, to the converter's capacitors, and then to the ac-side.

The circuit in Figure 3-8 has two current loops and the corresponding equations are:

$$\frac{v_{dc}}{2} = v_{a,x} + r_L i_{La,x} + L\frac{di_{La,x}}{dt} + L_x\left(\frac{di_{La,x}}{dt} - \frac{di_{Lb,x}}{dt}\right) - R_x\left(i_{Lb,x} - i_{La,x}\right) \quad (3\text{-}24)$$

$$\frac{v_{dc}}{2} = v_{b,x} + r_L i_{Lb,x} + L\frac{di_{Lb,x}}{dt} - L_x\left(\frac{di_{La,x}}{dt} - \frac{di_{Lb,x}}{dt}\right) + R_x\left(i_{Lb,x} - i_{La,x}\right) \quad (3\text{-}25)$$

For proper inverter operation, the ac-side current must be sinusoidal, without any offset or low-frequency harmonics. It will have the form:

$$i_{ac,x} = I_x \sin(\omega t - \phi) = i_{La,x} - i_{Lb,x} \quad (3\text{-}26)$$

The ac-side current $i_{ac,x}$ will flow through the dc-side voltage source, but the average power it gives rise to is 0. Any arbitrary current, limited only by the arm impedances, can flow between the dc-side voltage source and the converter's equivalent voltage sources. However only a dc current would yield an average power to be drawn from the dc-side. Ignoring current and voltage harmonics, that do not result in net power flow between the dc source and the load, the dc-side current will be $i_{dc,x}$. Using (3-26), the converter and arm currents can be defined as:

$$i_{La,x} = i_{dc,x} + \frac{i_{ac,x}}{2} \quad (3\text{-}27)$$

$$i_{Lb,x} = i_{dc,x} - \frac{i_{ac,x}}{2} \quad (3\text{-}28)$$

If the load current is not shared equally between arms *a* and *b*, the resultant current will circulate power forward and backward between the dc source and the converter, without transferring it to the load resistor. Substituting with (3-27) and (3-28) in the sum of (3-24) and (3-25):

$$v_{dc} = v_{a,x} + v_{b,x} + 2r_L\left(i_{La,x} + i_{Lb,x}\right) + 2L\left(\frac{di_{La,x}}{dt} + \frac{di_{Lb,x}}{dt}\right) \quad (3\text{-}29)$$

The arm current equations can be rearranged, like (3-5)and (3-6), to get the dc-side and ac-side currents:

$$i_{dc,x} = \frac{i_{L,a,x} + i_{L,b,x}}{2} \quad (3\text{-}30)$$

$$i_{ac,x} = i_{L,a,x} - i_{L,b,x} \quad (3\text{-}31)$$

The dc source current flows through the outer current loop in Figure 3-8 and can be derived by adding (3-24) to (3-25), and substituting $i_{dc,x}$ with (3-30):

$$v_{dc} = v_{a,x} + v_{b,x} + 2r_L i_{dc,x} + 2L\frac{di_{dc,x}}{dt} \quad (3\text{-}32)$$

As the load current $i_{ac,x}$ is the difference between the two arm currents, it can be derived by subtracting (3-25) from (3-24), and using (3-31):

$$-\left(v_{a,x} - v_{b,x}\right) = \left(r_L + 2R_x\right)i_{ac,x} + \left(L + 2L_x\right)\frac{di_{ac,x}}{dt} \quad (3\text{-}33)$$

The resultant dc and ac voltages, (3-5) and (3-6), are compensated for the sub-module capacitor parasitic resistance using $v_{r_C,a/b,x,i} = r_C \times d_{a,a/b,x,i} \times i_{La/b,x}$, which affects the individual arm voltages:

$$
\begin{aligned}
v_{a,x} &= \left(d_{dc,x} - d_{ac,x}\right) \times n \times \left(\left(d_{dc,x} - d_{ac,x}\right)\left(i_{dc,x} + \frac{i_{ac,x}}{2}\right) r_C + \overline{v_{Ca,x}} \right) \\
&\quad + 2nr_{SW}\left(i_{dc,x} + \frac{i_{ac,x}}{2}\right) \\
v_{b,x} &= \left(d_{dc,x} + d_{ac,x}\right) \times n \times \left(\left(d_{dc,x} + d_{ac,x}\right)\left(i_{dc,x} - \frac{i_{ac,x}}{2}\right) r_C + \overline{v_{Cb,x}} \right) \\
&\quad + 2nr_{SW}\left(i_{dc,x} - \frac{i_{ac,x}}{2}\right)
\end{aligned}
\qquad \textit{(3-34)}
$$

$$
v_{a,x} = \left(d_{dc,x} - d_{ac,x}\right) n \overline{v_{Ca,x}} + n\left(d_{dc,x}{}^2 - 2d_{dc,x}d_{ac,x} + d_{ac,x}{}^2\right)\left(i_{dc,x} + \frac{i_{ac,x}}{2}\right) r_C + \\
+ 2nr_{SW}\left(i_{dc,x} + \frac{i_{ac,x}}{2}\right) \qquad \textit{(3-35)}
$$

$$
v_{b,x} = \left(d_{dc,x} + d_{ac,x}\right) n \overline{v_{Cb,x}} + n\left(d_{dc,x}{}^2 + 2d_{dc,x}d_{ac,x} + d_{ac,x}{}^2\right)\left(i_{dc,x} - \frac{i_{ac,x}}{2}\right) r_C + \\
+ 2nr_{SW}\left(i_{dc,x} - \frac{i_{ac,x}}{2}\right) \qquad \textit{(3-36)}
$$

Inside the sub-module, the average leg capacitor voltage and its dynamics can be described by:

$$v_C = \frac{\overline{v_{Ca,x}} + \overline{v_{Cb,x}}}{2} \tag{3-37}$$

$$C\frac{dv_C}{dt} = \frac{1}{2}\left(\frac{d\overline{V_{Ca,x}}}{dt} + \frac{d\overline{V_{Cb,x}}}{dt}\right) \tag{3-38}$$

$$\begin{aligned} C\frac{d\overline{v_{Ca,x}}}{dt} &= d_{a,a,x}i_{La,x} \\ C\frac{d\overline{v_{Cb,x}}}{dt} &= d_{a,b,x}i_{Lb,x} \end{aligned} \tag{3-39}$$

$$\begin{aligned} C\frac{d\overline{v_{Ca,x}}}{dt} &= d_{dc,x}i_{dc,x} + d_{dc,x}\frac{i_{ac,x}}{2} - d_{dc,x}i_{dc,x} - d_{ac,x}\frac{i_{ac,x}}{2} \\ C\frac{d\overline{v_{Cb,x}}}{dt} &= d_{dc,x}i_{dc,x} - d_{dc,x}\frac{i_{ac,x}}{2} + d_{dc,x}i_{dc,x} - d_{ac,x}\frac{i_{ac,x}}{2} \end{aligned} \tag{3-40}$$

$$C\frac{dv_C}{dt} = d_{dc,x}i_{dc,x} - d_{ac,x}\frac{i_{ac,x}}{2} \tag{3-41}$$

Equation (3-41) shows that the capacitor current can be separated into two components – one that transfers energy from the dc source, and one that delivers energy to the ac load, as illustrated in Figure 3-9. The ac quantities $d_{ac,x}$ and $i_{ac,x}$ are converted to their RMS values, as the output of the converter arm is sinusoidal.

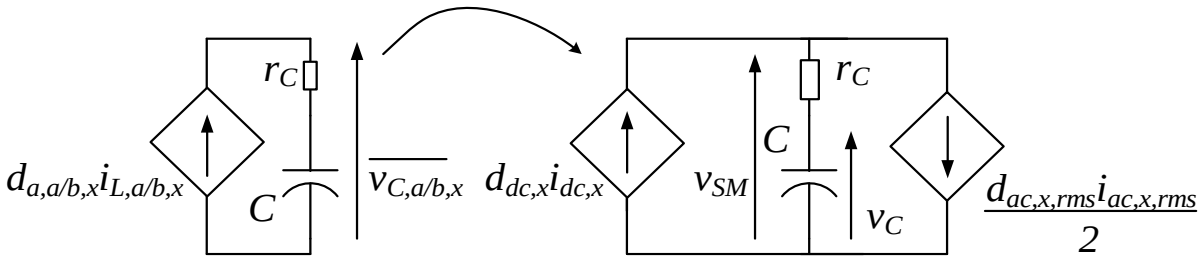

Figure 3-9 Equivalent circuit of a converter sub-module

The inserted dc and ac voltages become:

$$v_{dc,x} = 2n\left(d_{dc,x} v_C + \left(\left({d_{dc,x}}^2 + {d_{ac,x}}^2 \right) r_C + 2r_{SW} \right) i_{dc,x} - 2 d_{dc,x} d_{ac,x} \frac{i_{ac,x,rms}}{2} r_C \right) \quad (3\text{-}42)$$

$$v_{ac,x} = d_{ac,x} n v_C - n\left(\left({d_{dc,x}}^2 + {d_{ac,x}}^2 \right) r_C + 2r_{SW} \right) \frac{i_{ac,x,rms}}{2} + 2n d_{dc,x} d_{ac,x} i_{dc,x} r_C \quad (3\text{-}43)$$

According to equations (3-42) and (3-43) the inserted dc and ac side voltage sources can be modelled as a controlled voltage source, with an equivalent series resistance r_{SM}, equal to:

$$r_{SM} = \left({d_{dc,x}}^2 + {d_{ac,x}}^2 \right) r_C + 2r_{SW} \quad (3\text{-}44)$$

It should be noted that there is cross coupling, caused by the capacitor parasitic resistance, that can be represented as a voltage source in series with the inserted capacitor voltages:

$$\begin{aligned} v_{CC,ac} &= 4n d_{dc,x} d_{ac,x} \frac{i_{ac,x,rms}}{2} \\ v_{CC,dc} &= 2n d_{dc,x} d_{ac,x} \frac{i_{dc,x}}{2} \end{aligned} \quad (3\text{-}45)$$

With (3-42) through (3-45) the differential equations of the dc and ac currents are:

$$\frac{d i_{dc,x}}{dt} = -\frac{r_L + n r_{SM}}{L} i_{dc,x} - \frac{n}{L} d_{dc,x} v_C - \frac{1}{2L} v_{IN} + \frac{v_{CC,ac}}{L} \quad (3\text{-}46)$$

$$\frac{1}{2} \frac{d i_{ac,x,rms}}{dt} = -\frac{r_L + n r_{SM} + 2R_x}{L + 2L_x} \frac{i_{ac,x,rms}}{2} + \frac{n}{L + 2L_x} d_{ac,x,rms} v_C + \frac{v_{CC,dc}}{L + 2L_x} \quad (3\text{-}47)$$

The equivalent circuit of the averaged time model can be constructed using equations (3-41), (3-46), and (3-47) as shown in Figure 3-10.

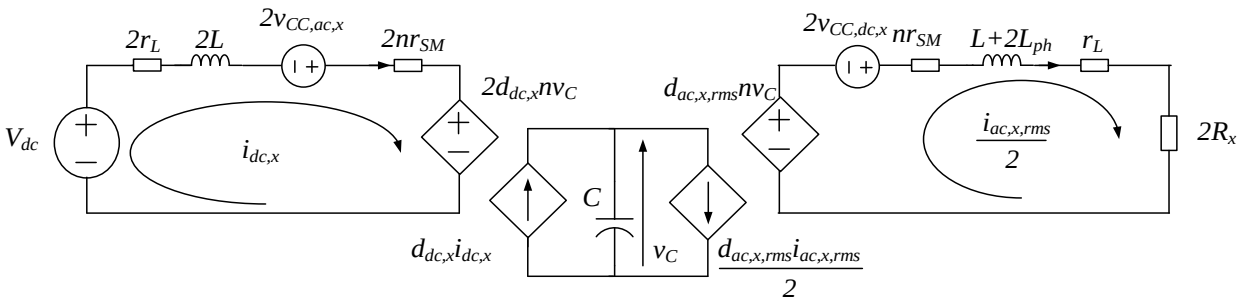

Figure 3-10 Equivalent circuit of the BMCI averaged-time model

The average time state-space model has the following form:

$$\begin{aligned} \dot{x} &= Ax + Bu \\ y &= Cx \end{aligned} \tag{3-48}$$

Where x is the state variable vector, u is the model input, A, B, and C, are matrices, and y is the model's output.

$$x = \begin{bmatrix} i_{dc,x} \\ v_C \\ \dfrac{i_{ac,x,rms}}{2} \end{bmatrix} \tag{3-49}$$

$$u = v_{IN}$$

The state variable matrix A, and input matrix B can be compiled from (3-46) and (3-47):

$$A = \begin{pmatrix} -\dfrac{r_L + nr_{SM}}{L} & -\dfrac{nd_{dc,x}}{L} & \dfrac{4n}{L} d_{dc,x} d_{ac,x,rms} r_C \\ \dfrac{d_{dc,x}}{C} & 0 & -\dfrac{d_{ac,x,rms}}{C} \\ \dfrac{4n}{L+2L_x} d_{dc,x} d_{ac,x,rms} r_C & \dfrac{nd_{ac,x,rms}}{L+2L_x} & -\dfrac{r_L + nr_{SM} + 2R_x}{L+2L_x} \end{pmatrix} \tag{3-50}$$

$$B = \begin{pmatrix} \dfrac{1}{2L} \\ 0 \\ 0 \end{pmatrix} \tag{3-51}$$

The output matrix C can have multiple forms, depending on the required output:

$$C_{Vc} = \begin{pmatrix} 0 & 1 & 0 \end{pmatrix} \quad (3\text{-}52)$$

$$C_{idc,x} = \begin{pmatrix} 1 & 0 & 0 \end{pmatrix} \quad (3\text{-}53)$$

$$C_{VRx} = \begin{pmatrix} 0 & 0 & 2R_x \end{pmatrix} \quad (3\text{-}54)$$

The dc current can be calculated using (3-53), the average sub-module capacitor voltage using (3-52), and the load voltage using (3-54)

3.3.1. Large signal model

The large signal model determines the dc operating point of the converter, around which the model is averaged. For an inverter with a sinusoidal output, this is a steady state condition for which the amplitude and phase of the output current are constant. The large signal model is constructed by setting all derivatives to 0. The steady-state state variables can be calculated by using the inverse of matrix *A* and solving:

$$\left.\begin{aligned} x &= A^{-1}Bu \\ y &= CA^{-1}Bu \end{aligned}\right\} \quad (3\text{-}55)$$

The dc transfer characteristics, i.e. the dc-side voltage to sub-module capacitor voltage transfer function, can be obtained by solving (3-55) using (3-52). The steady-state RMS ac duty cycle is defined as:

$$d_{ac,x,rms} = \frac{m\left(1 - d_{dc,x}\right)}{\sqrt{2}}, \quad (3\text{-}56)$$

, where *m* is the steady-state modulation index. To calculate the maximum gain of the converter for a certain dc duty cycle, *m* will be considered equal to 1. The transfer characteristics can now be calculated by substituting (3-50) to (3-52) in (3-55), and cycling through values of $d_{dc,x}$. At every iteration (3-56) and (3-50) must be updated.

3.3.2. Small signal model

The small signal model describes the dynamics of the converter around the steady-state operating point. The model gives information as to how the converter dc current and average capacitor voltage, change relative to changes in the control input – the dc duty cycle $d_{dc,x}$. This is achieved by introducing a small perturbation around the dc operating point, derived in the previous section. The "rms" subscript is omitted from small signal value of $i_{ac,x}$ for clarity.

$$\left.\begin{aligned} d_{dc,x} &= \tilde{d}_{dc,x} + D_{dc,x} \\ i_{dc,x} &= \tilde{i}_{dc,x} + I_{dc,x} \\ v_{dc} &= \tilde{v}_{dc} + V_{dc} \\ v_C &= \tilde{v}_C + V_C \\ \frac{i_{ac,x,rms}}{2} &= \frac{\tilde{i}_{ac,x}}{2} + \frac{I_{ac,x,rms}}{2} \\ d_{ac,x} &= D_{ac,x} \end{aligned}\right\} \qquad (3\text{-}57)$$

In (3-56) the ac duty cycle is related to the dc duty cycle and this equation defines $d_{ac,x}$ as a steady-state variable. Substituting with (3-57) in (3-42), (3-43), and (3-41), and removing any purely dc variables and cross-coupled components, the converter equations become:

$$\frac{d\tilde{i}_{dc,x}}{dt} = -\frac{r_L + nr_{SM}}{L}\tilde{i}_{dc,x} - \frac{n}{L}D_{dc,x}\tilde{v}_C - \frac{n}{L}V_C\tilde{d}_{dc,x} + \frac{4nD_{dc,x}D_{ac,x,rms}r_C}{L}\frac{\tilde{i}_{ac,x}}{2} + \frac{4nD_{ac,x,rms}r_C I_{ac,x,rms}}{2L}\tilde{d}_{dc,x} + \frac{\tilde{v}_{dc}}{2L} \quad (3\text{-}58)$$

$$\frac{d\tilde{v}_C}{dt} = \tilde{d}_{dc,x}\frac{I_{dc,x}}{C} + \frac{D_{dc,x}}{C}\tilde{i}_{dc,x} - \frac{D_{ac,x}}{C}\frac{\tilde{i}_{ac,x}}{2} \quad (3\text{-}59)$$

$$\frac{1}{2}\frac{d\tilde{i}_{ac,x}}{dt} = -\frac{r_L + nr_{SM} + 2R_x}{L + 2L_x}\frac{\tilde{i}_{ac,x}}{2} + \frac{n}{L + 2L_x}D_{ac,x,rms}\tilde{v}_C + \frac{4nD_{ac,x,rms}D_{dc,x}r_C}{L + 2L_x}\tilde{i}_{dc,x} + \frac{4nD_{ac,x,rms}r_C I_{dc,x}}{L + 2L_x}\tilde{d}_{dc,x} \quad (3\text{-}60)$$

Similar to the general model, the state-space matrices can be populated using the 3 differential equations that describe the converter. However, now there are two model inputs, i.e. $d_{dc,x}$ and v_{dc}.

The duty cycle $d_{dc,x}$ would be used for analysing the control-to-output characteristics. This gives rise to two additional B matrices, making the equations:

$$\left.\begin{aligned} \dot{\tilde{x}} &= A\tilde{x} + B_{IN}\tilde{u} + B_d\tilde{d} \\ \tilde{i}_{dc,x} &= C_{idc,x}\tilde{x} \\ \tilde{v}_C &= C_{Vc,x}\tilde{x} \\ \tilde{v}_{Rx} &= C_{VRx}\tilde{x} \end{aligned}\right\} \quad (3\text{-}61)$$

The matrices of the small-signal model are:

$$A=\begin{pmatrix} -\frac{r_L+nr_{SM}}{L} & -\frac{nD_{dc,x}}{L} & \frac{4n}{L}D_{dc,x}D_{ac,x,rms}r_C \\ \frac{D_{dc,x}}{C} & 0 & -\frac{D_{ac,x,rms}}{C} \\ \frac{4n}{L+2L_x}D_{dc,x}D_{ac,x,rms}r_C & \frac{nD_{ac,x,rms}}{L+2L_x} & -\frac{r_L+nr_{SM}+2R_x}{L+2L_x} \end{pmatrix} \quad (3\text{-}62)$$

$$B_d=\begin{pmatrix} \frac{4nD_{ac,x,rms}r_C I_{ac,x,rms}}{2L}-\frac{n}{L}V_C \\ \frac{I_{dc,x}}{C} \\ \frac{4nD_{ac,x,rms}r_C I_{dc,x}}{L+2L_x} \end{pmatrix} \quad (3\text{-}63)$$

$$B_{IN}=\begin{pmatrix} \frac{1}{2L} \\ 0 \\ 0 \end{pmatrix} \quad (3\text{-}64)$$

$$C_{Vc,x}=\begin{pmatrix} 0 & 1 & 0 \end{pmatrix} \quad (3\text{-}65)$$

$$C_{idc,x}=\begin{pmatrix} 1 & 0 & 0 \end{pmatrix} \quad (3\text{-}66)$$

$$C_{VRx}=\begin{pmatrix} 0 & 0 & 2R_x \end{pmatrix} \quad (3\text{-}67)$$

With the small-signal model completed, the converter dynamics can be finally modelled. To design the gain of a closed-loop controller, the required transfer function can be generated from (3-62)through (3-67), with the block diagram in Figure 3-11:

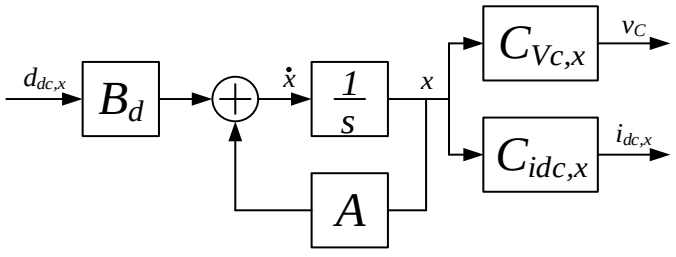

Figure 3-11 Average-time model block diagram with capacitor voltage and dc-side current outputs

Typical control systems for high-power converters use nested control loops, with an inner current and an outer voltage loop. This controller configuration allows for average current limiting and to be implemented, the required transfer functions are $d_{dc,x}$ to $i_{dc,x}$ and $d_{dc,x}$ to v_C:

$$\frac{\tilde{i}_{dc,x}(s)}{\tilde{d}_{dc,x}(s)} = C_{idc,x}(sI - A)^{-1}B_d u \qquad (3\text{-}68)$$

$$\frac{\tilde{v}_{C,x}(s)}{\tilde{d}_{dc,x}(s)} = C_{Vc,x}(sI - A)^{-1}B_d u \qquad (3\text{-}69)$$

3.4. SUMMARY

The goal of this chapter was to present the basic operating principle of the BMCI and elaborate on that with detailed modelling of the converter. The equations, that describe the continuous-time behaviour are derived to aid numerical simulation of the converter. These are used in Chapter 5 to create a *Simulink*® model. With the differential equations of the converter defined, the circuit is simplified to derive the dc transfer characteristics, which give information on the maximum achievable boost ratio and the effects of parasitic resistances on the converter performance. The simplified circuit is then used to create the small-signal model, which is necessary for the design of a stable control system.

An important conclusion is that the while the BMCI appears to be very complex, with multiple semiconductors bridges, inductors, and capacitors, the converter's actual response can be modelled as a 3-rd order system, with only 3 energy storage elements – inductor L, sub-module capacitor C, and ac inductance $L+2L_x$. This allows for conventional linear control techniques to be applied, simplifying the practical design of a BMCI.

Chapter 4. MODULATION AND CONTROL SYSTEM OF BMCIS

This chapter discusses the basics of BMCI modulation and the design of the converter control system. The modulation determines the transistor switching pattern and makes each converter arm appear as controlled voltage source. By calculating the appropriate voltage, the BMCI controller can maintain the required arm currents to transfer power from the dc-side source to the ac-side load.

The various systems that control the converter are analysed from the lowest level, i.e. controllers that operate on the converter's internal variables, up to the highest level – controllers that make the converter appear as a 2-terminal "black box". This chapter uses equations and models described in Chapter 3. A novel controller for sub-module capacitor voltage balancing is presented in 4.2.1.2, that avoids the need for gain tuning.

A controller design example for a prototype fuel cell BMCI drive can be found in Appendix B.

4.1. MODULATION

The BMCI's converter arms are essentially voltage source converters connected in series. In a similar manner to other voltage source converters, an inductance is required to limit the converter current and provide voltage boost or buck functions. To apply a more precise control to the inductor current, different modulation schemes can be employed.

4.1.1. Staircase modulation

The staircase method is the simplest modulation technique. It essentially samples the modulating waveform at discrete intervals, with the resolution depth equal to the number

of sub-modules n. An example for a converter with number of sub-modules $n = 3$, and $d_{dc} = 0.25$, is shown in Figure 4-1.

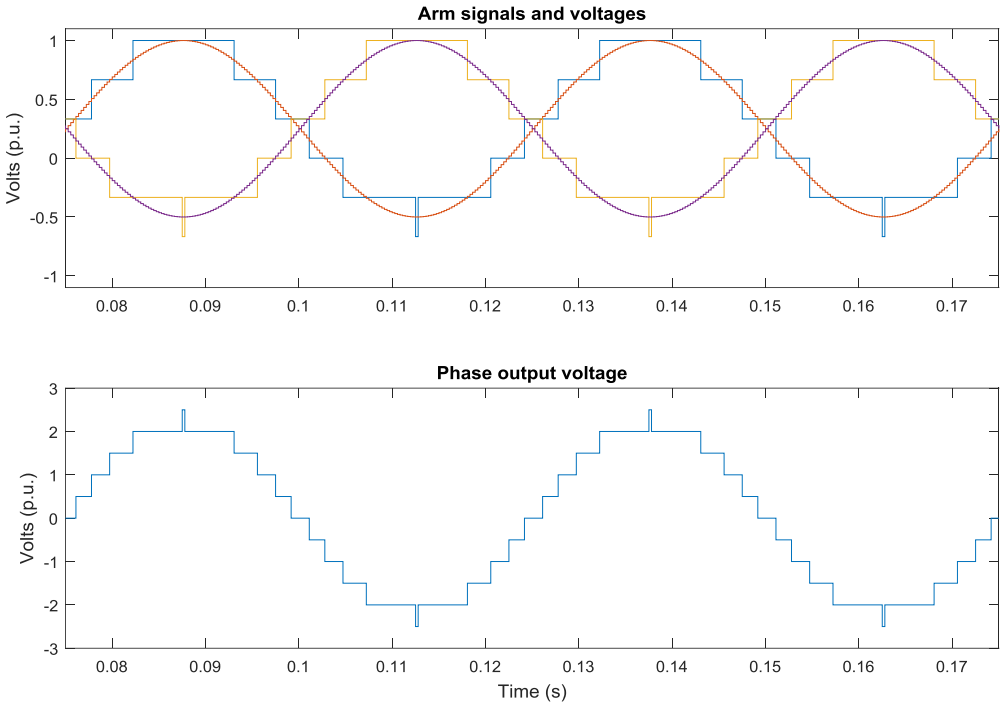

Figure 4-1 Staircase modulation for a BMCI with 3 sub-modules and d_{dc}=0.25

The offset in the modulated signal, equal to $d_{dc,x}$, causes the arm voltages to be asymmetric around the average value. This means in turn that the output phase switching levels increase. This is valid for converters with an inductive load, such as electric motors. The increase in the number of voltage levels is made possible by the two inductors in the converter leg. The difference between the dc-side voltage and the dc-component of the summed arm voltage is impressed across the two inductors. As this voltage has steps of V_C, the phase ac-side voltage will step in increments of ½ V_C.

This property can be better examined by first equating a full transistor bridge to a 3-pole switch arrangement, as shown in Figure 4-2:

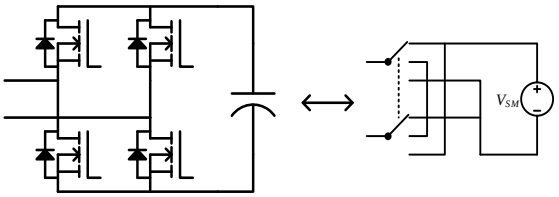

Figure 4-2 Equivalent switch circuit of a sub-module with a full-bridge of transistors

Each sub-module can either insert a positive, a negative voltage, or 0V. For achieving a certain phase voltage, the switching functions are defined by the modulation signal of each arm, as shown in Figure 4-1. Between two neighbouring levels, the circuit of a single converter leg is shown in Figure 4-3. As the two arms can be switched independently, the ac-side voltage is equal to a multiple of the submodule capacitor voltage or incremented by a half of it depending on whether the sum of the individual arm voltages is even or odd.

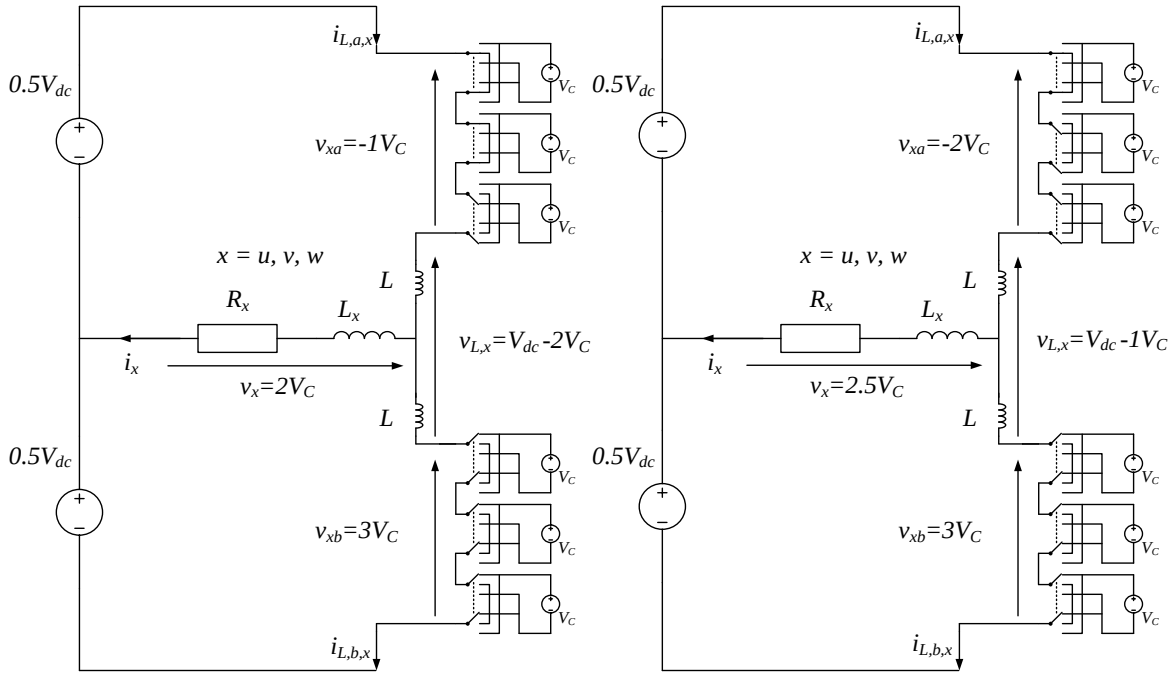

Figure 4-3 BMCI switching states for a single leg for two neighbouring voltage steps

Staircase modulation in general requires large inductors to limit the arm currents. Better performance is achieved with high values of *n,* where the voltage steps are sufficiently small. The staircase modulation method is unsuitable for BMCIs because to achieve stable operation, the dc duty cycle $d_{dc,x}$ must be divisible by *1/n*.

4.1.2. Pulse-width modulation (PWM)

With PWM the arm voltages switch between the two closest levels to the modulation signal value. This signal is compared to a triangular or saw-tooth waveform, and a comparator would generate the pulse signals for each transistor half-bridge. The carrier is oscillating at the fundamental transistor switching frequency $f_{sw,Q}$. In a half-bridge (HB) module, the control duty cycle is directly applied to the top transistor. In a full-bridge (FB) sub-module, two duty cycles are required, one for each transistor leg and the resultant sub-module output voltage v_{SM} will be switching at twice the individual leg switching frequency, $f_{sw,SM} = 2f_{sw,Q}$. The sub-module leg duty cycles are symmetric around *0.5* and the difference between them is equal to the active duty cycle d_a. This is shown in Figure 4-4:

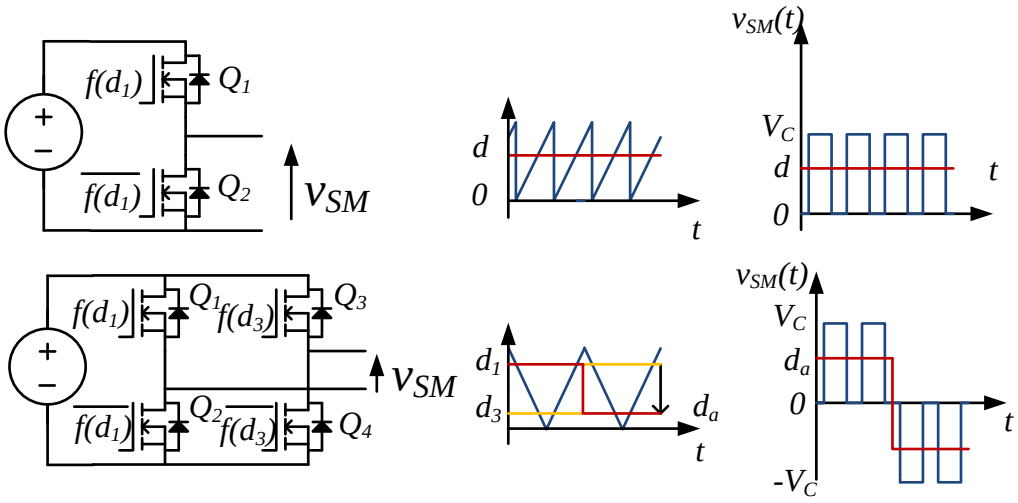

Figure 4-4 Half-bridge and full-bridge modules, their PWM modulation signals, and output voltages

For the same sub-module output voltage frequency, the half-bridge carrier must be oscillating at twice the frequency of the full-bridge carrier. As the control variable of each sub-module is the active duty cycle, that can be both positive and negative, the individual duty cycles d_1 and d_3 are equal to (4-1):

$$d_1 = \frac{1+d_a}{2}$$
$$d_3 = \frac{1-d_a}{2} \qquad (4\text{-}1)$$

The same voltage output, with duty cycle d_a can be produced if the sub-module uses one control signal and two carriers, as shown in Figure 4.5 a).

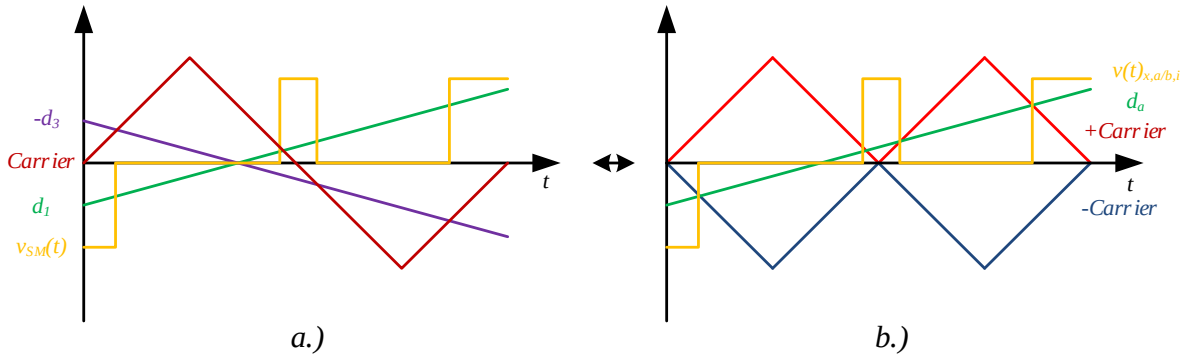

Figure 4-5 Two modulation schemes that produce the same output voltage

This modulation method, however, has each half-bridge either switching at twice the original carrier frequency, or being constantly off. In a real converter the modulation in Figure 4-5 b.) will result in higher variance in switching and conduction losses over one full cycle, as one transistor leg will be switching at $2f_{sw,Q}$, while in the other leg only one transistor will conduct, with no switching action.

The various methods for applying PWM to the whole of the converter can be classified in two general types – phase shifted, and level shifted. In phase shifted carrier schemes, the converter sub-modules are constantly switching with frequency equal to $2f_{sw,Q}$. Instead, level-shifted carrier schemes assume that only one sub-module's voltage, within an arm, is modulated at any given time, and the duty ratio cycles from 0 to 100% n-times as the control signal increases.

4.1.2.1. Phase shifted carrier (PSC)

When a phase shifted carrier is used, each sub-module generates its own carrier waveform. Each sub-module's carrier is phase shifted by 1/nth of the switching period of v_{SM}. With phase-shifted carrier modulation, the series connected sub-modules are interleaved. This results in an effective switching frequency equal to $2nf_{sw,Q}$, and similar to a parallel interleaved converter, as the modulation signal is varied, so does the duty cycle of the switching portion of the arm voltage. An example is shown in Figure 4-6, where the modulation signal $d_{ac,x}$ is varied.

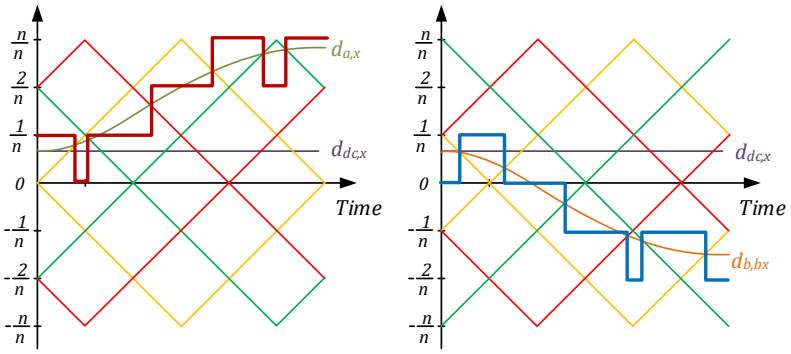

Figure 4-6 Modulation and carrier signals, with resultant arm voltages

The modular cascaded converter's duty cycle resets back to either the maximum or the minimum value as the arm's modulation signal crosses an intersection of the interleaved arm carriers. Effectively each intersection, at a value of *1/n*, defines an arm voltage level step. Thus, the phase shifted carrier modulation can be equated to a level shift scheme, the alternate phase opposition disposition carrier. The two waveforms produce the same arm voltage for all values of $d_{dc,x}$ and $d_{ac,x}$. A comparison between the two schemes is shown in Figure 4-7:

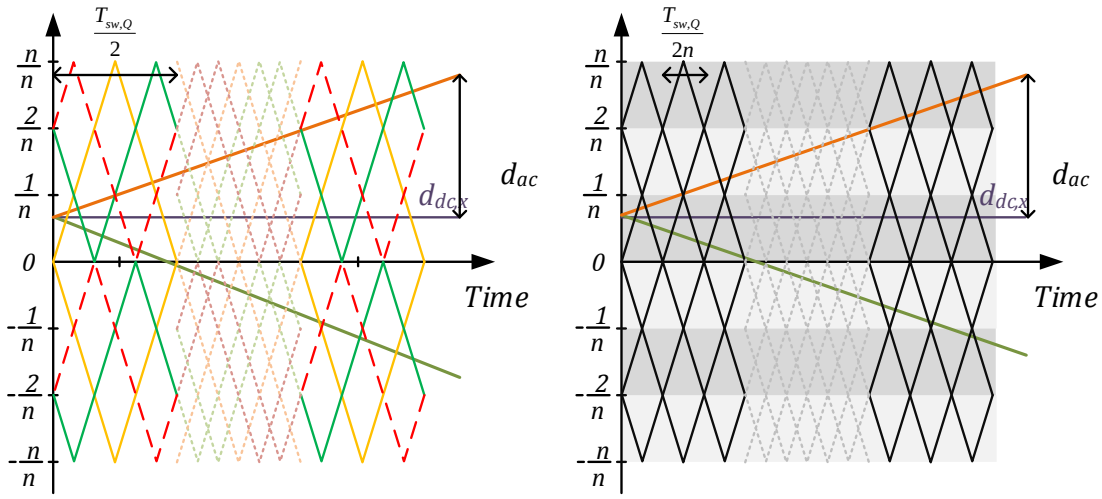

Figure 4-7 Phase shifted carrier and equivalent APOD carriers

Phase shifted carrier can be implemented with either a centralised carrier generator, or a localised sub-module carrier generator. The main benefit is that as for $|d_a|<1$, all sub-modules in the converter arm will have the same switching frequency.

4.1.2.2. Level shifted carrier

In a level-shifted carrier (LSC) scheme, each converter arm level has a corresponding carrier, oscillating at the same effective arm switching frequency as the PSC schemes – $2nf_{sw,Q}$. As the number of active, i.e. non-zero, inserted sub-modules increases, some sub-modules are in a static state of producing either $\pm V_{SM}$, or 0. For level shifted carrier schemes only one sub-module's voltage is being pulse-width modulated.

For this carrier type to be used, it has to be either generated in a single central controller, with the transistor signal sent directly to the sub-module transistor gate drivers, or if each sub-module has its own carrier, it has to be phase shifted by 180° for values of $d_{a/b,x}<0$.

4.1.2.3. Phase Disposition (PD)

In this modulation method all carriers have the same phase, for both positive and negative values of the modulation signals [151].

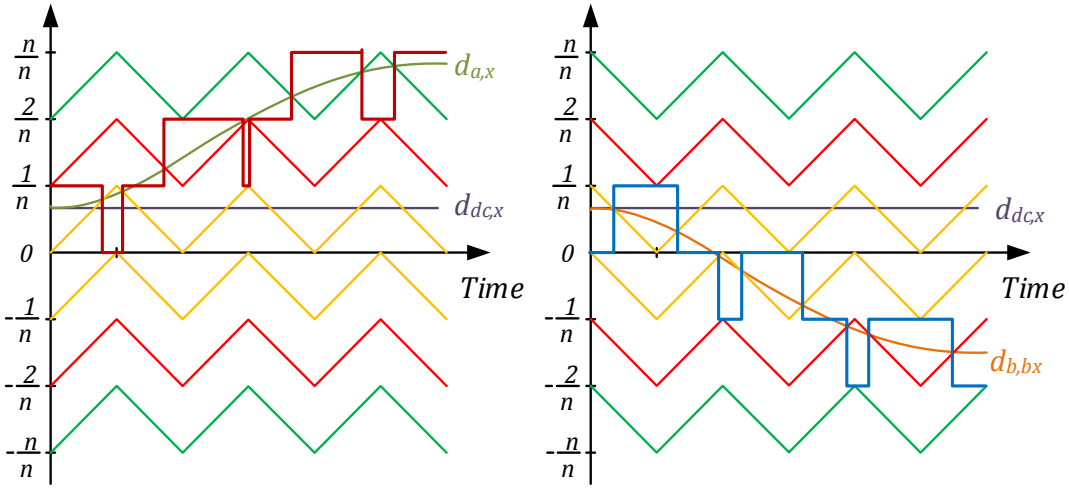

Figure 4-8 PD modulation

PD modulation for BMCI converters maintains the same direction of the pulse edges throughout the full range of duty cycle values, which will be shown in Chapter 5 to give low harmonic content for the dc-side voltage.

4.1.2.4. Phase Opposition Disposition (POD)

This carrier modulation method is similar to PD, with the key difference that for $d_{a/b,x}$<0, all carriers have a 180° phase shift [105]:

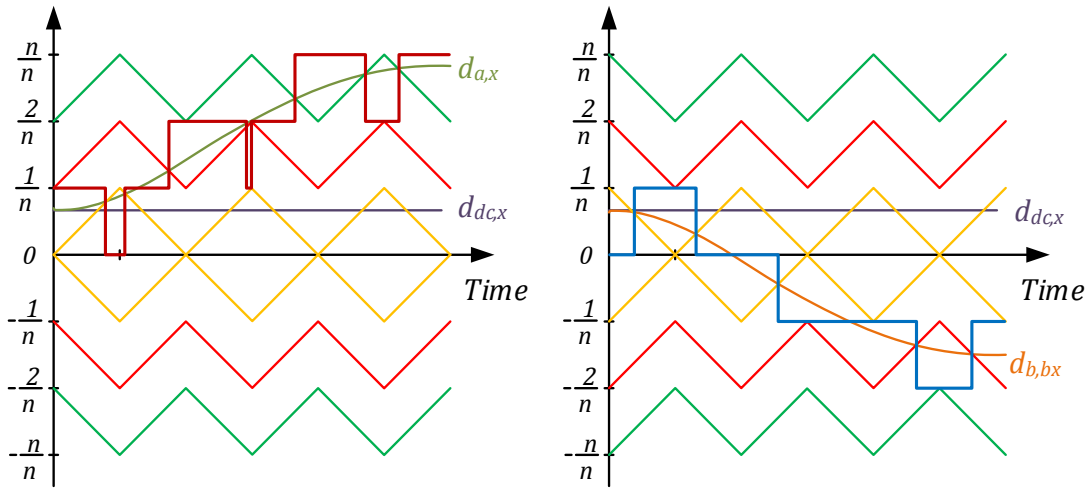

Figure 4-9 POD

With the POD scheme when the modulation signal of one arm enters the negative region, the alignment between the top and bottom arms changes, giving similar results to the APOD scheme, which is identical to the conventional PSC modulation. This modulation scheme has not been examined in detail and can be included in a future review.

4.1.3. Space-vector modulation

The biggest difference between space-vector modulation (SVM) and the previous two carrier-based techniques, is that space-vector modulation considers all 3 phases of the converter simultaneously. This method creates a vector space, with discrete switch states that correspond to fixed ac-side voltages. This modulation utilises the redundant states, i.e. different combinations that produce the same ac-side voltage, to reduce switching losses and ac-side harmonics.

SVM does not require the generation of PWM carriers and has intrinsic third harmonic injection. One drawback of SVM method is that the number of possible states increases exponentially with number of sub-modules, n, and can become computationally intensive.

The BMCI can potentially use a small *n*, such as the experimental prototype described in this thesis, that has a total of 12 cells. In such a case the complexity of the SVM would not be very high, and it is certainly a viable method that can be explored in future works.

4.2. CONVERTER CONTROL

The main tasks of the BMCI control system are to regulate the sub-module capacitor voltages to a desired value, maintain equal sub-module capacitor voltages across the converter, and to control the electric motor currents.

The converter controllers described below are standard Type 2 compensators, or otherwise known as Proportional Integral (PI) compensators, and the section covers the design process for a BMCI.

The novel contribution in this section is the voltage feedforward arm balancing algorithm, described in 4.2.1.2. The benefit of the proposed method is that no gain tuning is required, unlike proportional feedback controllers.

4.2.1. Sub-module capacitor voltage balancing

A key requirement for any MCC is that all sub-module capacitor voltages are equal. This condition is necessary to achieve high ac-side voltage quality, and consistent current ripple. Manufacturing difference between the sub-module capacitors can result in capacitance spread of ±20%. In a converter arm all sub-module transistor bridges have the same arm current flowing through them, and if they all operate with the same duty cycles, meaning equal capacitor currents, the differences in capacitance will result in unstable operations of the converter. For converter using a phase-shifted carrier, the individual sub-module duty cycle will be the same as the arm duty cycle:

$$\left.\begin{aligned} d_{a,x,i} &= d_{a,x} \\ d_{b,x,i} &= d_{b,x} \end{aligned}\right\} \tag{4-2}$$

The individual capacitor current thus becomes:

$$i_{C,a/b,x,i} = d_{a/b,x,i} i_{L,a/b,x} \tag{4-3}$$

$$\frac{d}{dt} V_{C,a/b,x,i} = \frac{1}{C_{a/b,x,i}} d_{a/b,x,i} i_{L,a/b,x,i} \tag{4-4}$$

For a level-shifted carrier, *m* sub-modules will have a 100% duty cycle, *l* sub-modules will have 0% duty, while 1 will have a duty cycle equal to the local duty:

$$\left.\begin{aligned} m &= floor\left(\left|nd_{a/b,x}\right|\right) \\ l &= n - m - 1 \\ d_{a/b,x,local} &= d_{a/b,x} - \frac{\left|nd_{a/b,x}\right|}{n} \end{aligned}\right\} \tag{4-5}$$

Unlike 2-level dc-dc converters, where the net power of a capacitor is 0 over one switching cycle, in an MCC the net power is 0 over one cycle of the output sinusoid. For this reason, the sub-module power can be considered continuous over one switching cycle, with capacitor current and power being:

$$i_{C,a/b,x,i} = d_{a/b,x,i} i_{L,a/b,x} \tag{4-6}$$

$$p_{C,a/b,x,i} = i_{C,a/b,x,i} v_{C,a/b,x,i} = d_{a/b,x,i} i_{L,a/b,x} v_{C,a/b,x,i} \tag{4-7}$$

$$\frac{d}{dt} V_{C,a/b,x,i} = \frac{1}{C_{a/b,x,i}} d_{a/b,x,i} i_{L,a/b,x} \tag{4-8}$$

The sub-module capacitor voltage $v_{C,a/b,x,i}$ must always be positive, as the converter uses transistors with anti-parallel diodes, and thus the capacitor power is dependent only on the arm current and the sub-module duty cycle. The arm duty cycle $d_{a/b,x}$ is used to

control the converter input, output, and leg currents, while the arm current is determined by the operating conditions of the BMCI.

To achieve an equal sub-module capacitor voltage across each converter arm, the only control variable is the individual sub-module duty cycle. How this is modified, from the value determined by the higher-level control system, is where different types of balancing algorithms can be applied.

4.2.1.1. Duty cycle modification with local feedback

When local feedback is used, the balancing duty cycle $d_{a/b,x,i,bal}$ is the output of a proportional controller. The controller input error is calculated from the average arm capacitor voltage minus the current sub-module voltage.

$$d_{bal,a/b,x,i} = k_{p,bal}\left(v_{C,nom} - v_{C,a/b,x,i}\right) \tag{4-9}$$

The average arm duty cycle can be calculated for each time period $T_{SW,Q} = 1/f_{sw,Q}$ using:

$$\overline{d_{a/b,x}} = \frac{\sum_{i=1}^{n} d_{a/b,x,i} + d_{bal,a/b,x,i}}{n} \tag{4-10}$$

The biggest drawback of this balancing controller is that the mean value of $d_{a/b,x}$ in (4-10), after the controller has been executed according to equation (4-9), will not always be equal to the original value of $d_{a/b,x}$. This will cause a disturbance that will affect the input and output currents of the BMCI.

The dynamics of this scheme can be evaluated using the fact that only d_{bal} will cause a dc change in arm capacitor voltage, as the energy stored in the arms caused by $d_{dc,x}$ and $i_{dc,x}$, is dissipated in the output load using $d_{ac,x}$ and $i_{ac,x}$:

$$sCv_{C,a/b,x,i} = d_{a/b,x,rms} i_{L,a/b,x,rms} \cos(\varphi_x) \times k_{p,bal} \left(\overline{v_{C,a/b,x}} - v_{C,a/b,x,i} \right) \quad (4\text{-}11)$$

$$v_{C,a/b,x,i} = \frac{1}{C\left(s + k_{p,bal} \frac{d_{a/b,x,rms} i_{L,a/b,x,rms} \cos\varphi_x}{C} \right)} k_{p,bal} \overline{v_{C,a/b,x}} \quad (4\text{-}12)$$

4.2.1.2. Duty cycle modification with sub-module voltage feedforward

This method scales the duty cycle of each converter sub-module based on the individual sub-module capacitor voltage. When the arm power is negative, i.e. the capacitor is discharging, the scaling factor of the *i*-th sub-module duty cycle is equal to the ratio of *i*-th capacitor voltage over the mean capacitor voltage for the whole arm:

$$d_{a/b,x,i} = d_{a,b/x} \frac{v_{C,a/b,x,i}}{\overline{v_{C,a/b,x}}} \quad for\ p_{a/b,x} \leq 0 \quad (4\text{-}13)$$

Since the total arm voltage equal to the sum of all sub-module voltages, and the scaling factors are proportional, the mean duty cycle of the whole arm remains equal to $d_{a/b,x}$ over a complete sub-module switching cycle. At the same time, the module with the highest voltage provides the highest power, while the one with the smallest charge supplies the lowest power.

When the arm power is positive, i.e. the capacitors are charging, the ratios need to be inverted. However, to maintain mean duty cycle equal to the command value, the scaling factors need to use the difference between twice the mean sub-module capacitor voltage and the voltage of the *i*-th sub-module:

$$d_{a/b,x,i} = d_{a,b/x}\frac{2\overline{v_{C,a/b,x}} - v_{C,a/b,x,i}}{\overline{\overline{v_{C,a/b,x}}}} \quad for\ p_{a/b,x} > 0 \tag{4-14}$$

Similar to the proportional feedback controller, the current that causes a change in the capacitor voltage is the difference between the sub-module current and the mean current:

$$sCv_{C,a/b,x,i} = d_{a/b,x,rms} i_{L,a,b,x,rms} \cos(\varphi_x) \times \left(1 - \frac{v_{C,a/b,x,i}}{\overline{\overline{v_{C,a/b,x}}}}\right) \tag{4-15}$$

$$v_{C,a/b,x,i} = \frac{1}{sC\dfrac{\overline{\overline{v_{C,a/b,x}}}}{d_{a/b,x,rms} i_{L,a/b,x,rms} \cos\varphi_x} + 1}\overline{v_{C,a/b,x}} \tag{4-16}$$

According to (4-16) the feed-forward balancing controller will also have a first-order system response, as does the proportional controller. The scaling term for each sub-module is:

$$k_{a/b,x,i} = \frac{v_{C,a/b,x,i}}{\overline{\overline{v_{C,a/b,x}}}} \tag{4-17}$$

The block diagram of the converter sub-module capacitor balancing control system is shown in Figure 4-10. The system used in this thesis is the feedforward control, discussed in section 4.2.1.2.

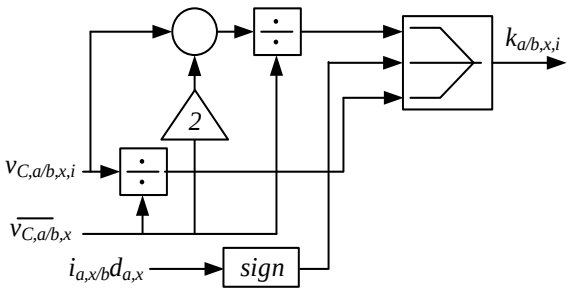

Figure 4-10 Feedforward balancing controller

4.2.1.1. Capacitor balancing using sorting algorithms

Another method for balancing the capacitor voltages is to use a sorting algorithm. The general idea is that at every switching instant, the control system evaluates all the sub-module voltages and chooses which one will produce 0 volts, i.e. neither charging or discharging, or $\pm v_C$, charging or discharging. As with the previous methods discussed, the rule changes depending on arm power flow, in other words it depends on whether the arm charges or discharges.

For positive power flow into the arm, $p_{a/b,x}>0$, the next sub-module to be inserted is the one with the lowest state of charge, and the one to be bypassed, is the one with the highest state of charge. For negative power flow, or arm discharging, the next module to be inserted is the one with the highest state of charge, while the next one to be bypassed is the one with the lowest state of charge.

Compared to the methods discussed in sections 4.1.2.3 and 4.1.2.4, sorting algorithms are more computationally intensive for high number of sub-modules. The rate at which the sorting algorithm is executed, f_{Sort}, can be either the same as $2f_{sw,Q}$, or lower. Making f_{Sort} much lower than $f_{sw,Q}$ will reduce the effectiveness of the balancing control system, and in addition f_{Sort} must be higher than the converter output frequency, $f_{OUT}=2\pi\omega_e$, in order to track the arm power polarity. The sub-module capacitance determines how quick the balancing action is, and thus higher capacity can use a lower f_{Sort}. As the module being modulated is the one with the highest or lowest charge, this method cannot guarantee uniform switching frequency for each sub-module, which can be a drawback.

4.2.2. Average leg sub-module voltage control

The goal of the balancing control systems in 4.2.1 and 4.2.2.3 is to only equalise the voltage across sub-modules in the same converter arm, converging to the mean arm voltages. When the converter is operating without a closed loop controller, the actual

capacitor voltage and output currents are determined by the modulation index and dc duty cycle $d_{dc,x}$, as well as the load resistance and converter parasitic elements.

Similar to 2-level dc-dc converters, the BMCI can use an outer voltage control loop and an inner current loop [73], [152]. This configuration allows for a more reliable performance, as a current limit can be programmed into the controller. Unlike conventional dc-dc converters, the BMCI has additional controllers to manage any voltage differences between arms *a* and *b* within the same arm, suppression of unwanted harmonics, and operating at low machine frequencies. Thus, a circulating current controller is necessary in all cases, and its current reference is derived from the outer voltage controllers.

4.2.2.1. Circulating current controller

The circulating current is common to both arms *a* and *b* and flows through the dc link of the converter, and controls the input power for the converter leg of phase *x*:

$$i_{dc,x} = \frac{i_{L,a,x} + i_{L,b,x}}{2} \tag{4-18}$$

$$p_{dc,x} = d_{dc,x} \sum_{i=1}^{n} \left(v_{C,a,x,i} + v_{C,b,x,i} \right) \times i_{dc,x} \tag{4-19}$$

In chapter 3 the mathematical large-signal and small-signal models are derived for a single converter leg. The control input to circulating current transfer function can be derived by converting the state-space model from equations (3-62) through (3-64), using the output matrix for the state variable $i_{dc,x}$ from (3-66):

$$\begin{aligned} \dot{x} &= Ax + B_d d_{dc,x} \\ y &= C_{idc} x \end{aligned} \qquad (4\text{-}20)$$

As the detailed model includes the dynamics of the ac circuit, the model is of the 3rd order, as it has 3 energy storage elements. This complicates the analysis and the design of the control systems. The phase inductance L_x and the load resistance introduce an additional pole in the system response. If that pole frequency is much higher than the natural frequency of the plant ω_n, the effect of the phase inductance becomes insignificant to the input current controller and can be removed from the state-space model. The phase resistive load can be replaced by equivalent sub-module resistive load $R_{x,SM}$. This approach is also used for simplified MCC models [153].

$$R_{x,SM} = \frac{2\frac{R_x}{\cos\varphi} + r_L + nr_{SM}}{nD_{ac,x,RMS}^{\ 2}} \qquad (4\text{-}21)$$

The simplified equivalent circuit leads to revised matrices A_2, B_{d2}, and C_{idc}:

$$A_2 = \begin{pmatrix} -\frac{r_L + nr_{SM}}{L} & -\frac{nD_{dc,x}}{L} \\ \frac{D_{dc,x}}{C} & \frac{1}{CR_{x,SM}} \end{pmatrix} \qquad (4\text{-}22)$$

$$B_{d,2} = \begin{pmatrix} -\frac{n}{L}V_C \\ \frac{I_{dc,x}}{C} \end{pmatrix} \qquad (4\text{-}23)$$

$$\left.\begin{aligned} C_{idc} &= \begin{pmatrix} 1 & 0 \end{pmatrix} \\ C_{vc} &= \begin{pmatrix} 0 & 1 \end{pmatrix} \end{aligned}\right\} \qquad (4\text{-}24)$$

The converter's dc duty cycle, $d_{dc,x}$, to circulating current, $i_{dc,x}$, transfer function can be extracted from the state space model using:

$$H_{idc}(s) = \frac{\tilde{i}_{dc,x}(s)}{\tilde{d}_{dc,x}(s)} = C_{idc}\left(sI - A_2\right)^{-1} B_{d2} \tag{4-25}$$

$$H_{idc}(s) = \frac{\tilde{i}_{dc,x}(s)}{\tilde{d}_{dc,x}(s)} = G_{idc}\frac{\frac{s}{\omega_z}+1}{\frac{s^2}{\omega_n^2}+\frac{2\zeta s}{\omega_n}+1} \tag{4-26}$$

, where G_{idc} is the dc current gain, ω_z is the plant zero, ω_n is the plant natural frequency, and ζ is the damping ratio. With the revised matrices, the model order is reduced to second, and the equations are identical to those of a conventional boost dc-dc converter. The equivalent zero frequency, natural frequency, and dc current gain for the BMCI are:

$$\omega_z = \frac{2}{R_{SM}C} \tag{4-27}$$

$$\omega_n = \sqrt{\frac{nR_{SM}d^2 + r_{arm}}{R_{SM}LC}} \tag{4-28}$$

$$G_{idc,x}(0) = -\frac{2nV_C}{nd^2R_{SM} + r_{arm}} \tag{4-29}$$

A standard design approach is to use a proportional-integral compensator to achieve a closed-loop crossover frequency equal to 1/10th of the converter's switching frequency. This is a compromise between sufficient attenuation of the switching action of the converter, stability over a wide range of loads, and converter response. To achieve stability, the open loop phase shift at the crossover frequency must be less than 180°, and a phase margin of more than 60° will avoid excessive setpoint overshoot. To maintain stability over a range of loads, and changes in leg inductance, a gain margin of at least 6dB is required.

As the control voltage of the BMCI is averaged over one cycle, of the effective switching frequency $f_{sw,eff}=2nf_{sw,Q}$, the arm duty cycle will be updated once per effective switching cycle, resulting in a discrete system. This effect can be modelled using a Zero Order Hold (ZOH) transfer function:

$$H_{ZOH} = \frac{1-e^{-\frac{s}{fsw,eff}}}{s} f_{sw,eff} \tag{4-30}$$

At the desired crossover frequency, equal to 10% of the open loop crossover frequency, the ZOH introduced 18° to the phase response, which is equivalent to a delay of one-half switching cycle. The 0dB crossover frequency of the open-loop current plant transfer function is:

$$\omega_{i,0dB} = \frac{\beta_{idc} G_{idc} \omega_n^{\,2}}{\omega_z} \tag{4-31}$$

Since the proportional gain coefficient, k_p, sets the crossover frequency of the cascaded controller and plant transfer functions:

$$k_{p,idc} = \frac{\omega_{i,CL}}{\omega_{i,0dB}} \tag{4-32}$$

The integrator gain, $k_{i,idc}$, is used to set the controller zero. Above the natural frequency, the magnitude response of the plant decreases with frequency at a rate of 20dB/decade, meaning the phase shift is 90°. Below the compensator zero frequency, $\omega_{z,comp}$ the phase shift is also 90°, while at the break frequency it reduces to 45°. The compensator zero $\omega_{z,comp}$ is set to one decade below the crossover frequency, so that it only adds a phase lag of 4°. The integrator gain becomes:

$$k_{i,idc} = k_{p,idc}\omega_{z,comp} = k_{p,idc}0.1\omega_{i,CL} \tag{4-33}$$

The compensator transfer function is:

$$G_{PI,idc} = \frac{sk_{p,idc} + k_{i,idc}}{s} \tag{4-34}$$

The open loop transfer function can be evaluated for crossover frequency, phase, and gain margin using the forward transfer function of the plant and compensator:

$$H_{idc,OL} = H_{idc} G_{PI,idc} \tag{4-35}$$

The simplified bode responses of the different transfer functions is shown in Figure 4-11:

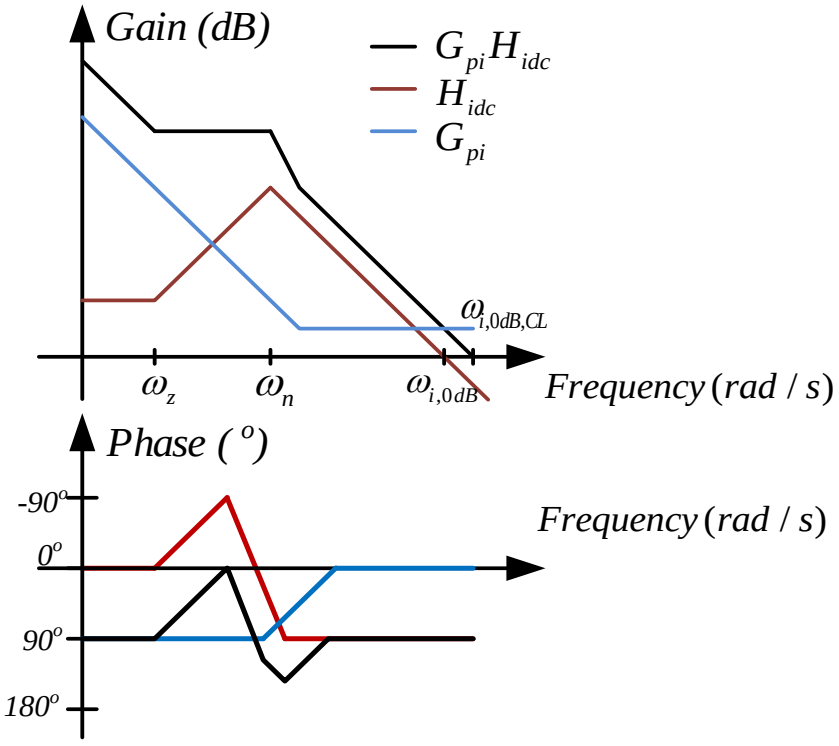

Figure 4-11 Simplified bode plot of current transfer function, controller, and combined model

The stability of the system can be evaluated by analysing the Nyquist plot of the cascaded open-loop – compensator transfer function. The closed loop gain of a stable system can be calculated using:

$$H_{idc,CL} = \frac{\tilde{i}_{dc,x}}{\tilde{i}_{ref,x}} = \frac{H_{idc,OL}}{1 + H_{idc,OL}} \tag{4-36}$$

, where $i_{ref,x}$ is the reference current variable. The compensator introduces additional gain below the natural frequency of the converter current transfer function, removing steady-state error. Thus, the transfer function of the closed loop current system can be approximated as a single-order system:

$$H_{idc,CL} \approx \frac{1}{\frac{s}{\omega_{0dB,CL}} + 1} \tag{4-37}$$

4.2.2.2. Average leg capacitor voltage control

The BMCI can operate with voltage mode control, with the control input being $d_{dc,x}$. The transfer function of duty cycle to capacitor voltage transfer function can be extracted from (4-22), (4-23), and (4-24):

$$H_{vc} = \frac{\tilde{v}_C}{\tilde{d}_{dc,x}} = G_{vc} \frac{\frac{s}{\omega_{RHP}} - 1}{\frac{s^2}{\omega_n^2} + \frac{2\zeta s}{\omega_n} + 1} \tag{4-38}$$

$$G_{vc} = -\frac{I_{dc,x} R_{SM} \left(n D_{dc,x}^2 R_{SM} - r_{arm} \right)}{r_{arm} + n D_{dc,x}^2 R_{SM}} \tag{4-39}$$

In section 4.2.2.1 the reference current to circulating current transfer function is derived. To design the capacitor voltage control system, the required transfer function is reference current $i_{ref,x}$ to sub-module capacitor voltage $v_{C,x}$. This can be found using equations (4-26), (4-37), and (4-38):

$$H_{vc,iref} = \frac{\tilde{v}_{C,x}}{\tilde{d}_{dc,x}} \frac{\tilde{d}_{dc,x}}{\tilde{i}_{dc,x}} \frac{\tilde{i}_{dc,x}}{\tilde{i}_{ref,x}} = \frac{H_{vc}}{H_{idc}} H_{idc,CL} \tag{4-40}$$

$$\frac{H_{vc}}{H_{idc}} = \frac{\tilde{v}_C}{\tilde{i}_{dc,x}} = \frac{G_{vc}\left(\frac{s}{\omega_{RHP}} - 1\right)}{G_{idc}\left(\frac{s}{\omega_z} + 1\right)} \tag{4-41}$$

$$\frac{G_{vc}}{G_{idc}} = \frac{nD_{dc,x}{}^2 R_{SM} - r_{arm}}{2nD_{dc,x}} \tag{4-42}$$

The right-hand plane zero frequency ω_{RHP} introduces an additional 90° phase shift, while adding a +20dB/decade slope. However, the closed-loop current controller allows for the transfer function to have a dominant pole that coincides with the current transfer function zero at ω_z. The right-hand plane zero is located at:

$$\omega_{RHP} = \frac{nD_{dc,x}{}^2 R_{SM} - r_{arm}}{L} \tag{4-43}$$

For most converters $\omega_{RHP} >> \omega_z$, and the bandwidth will be determined by the dominant pole at ω_z and the *0dB* crossover frequency for the voltage controller, $\omega_{v,0dB}$ can be found from (4-27) and (4-42), as long as the gain is more than 0dB:

$$\omega_{v,0dB} = \frac{G_{vc}}{G_{idc}} \omega_z \tag{4-44}$$

The proportional gain of the voltage controller can be calculated using the desired crossover frequency for the voltage controller, $\omega_{v,0dB,CL}$:

$$k_{p,vc} = \frac{\omega_{v,0dB,CL}}{\omega_{v,0dB}} \tag{4-45}$$

Since $d_{dc,x}$ is calculated by the current compensator, the converter delay is already taken into account. Moreover, the crossover frequency of the voltage control loop is much

lower than the sampling frequency and the compensator zero can be set an octave below ω_z. This is a sufficient margin that avoids excessive overshoot at lighter loads:

$$k_{i,vc} = \frac{\omega_z}{2} k_{p,vc} \tag{4-46}$$

$$G_{PI,vc} = \frac{sk_{p,vc} + k_{i,vc}}{s} \tag{4-47}$$

The Nyquist plot of the forward transfer function must be evaluated, as the right-hand plane zero can cause an instability if its frequency ω_{RHP} is too close to $\omega_{v,0dB,CL}$. The control system can be evaluated only at peak loading, as according to (4-43) ω_{RHP} increases with frequency. The open loop crossover frequency $\omega_{v,0dB}$ will remain relatively constant, as according to (4-27) the capacitor transfer function dominant pole frequency is inversely proportional to ω_z and the dc gain in (4-42) can be approximated to be proportional to ω_z, as long as $R_{SM} >> r_{arm}$, where $r_{arm} = r_L + nr_{SM}$. The open loop plant and compensator transfer function is:

$$H_{vc,OL} = H_{vc,iref} G_{PI,vc} \tag{4-48}$$

The simplified expected plot is visualised in

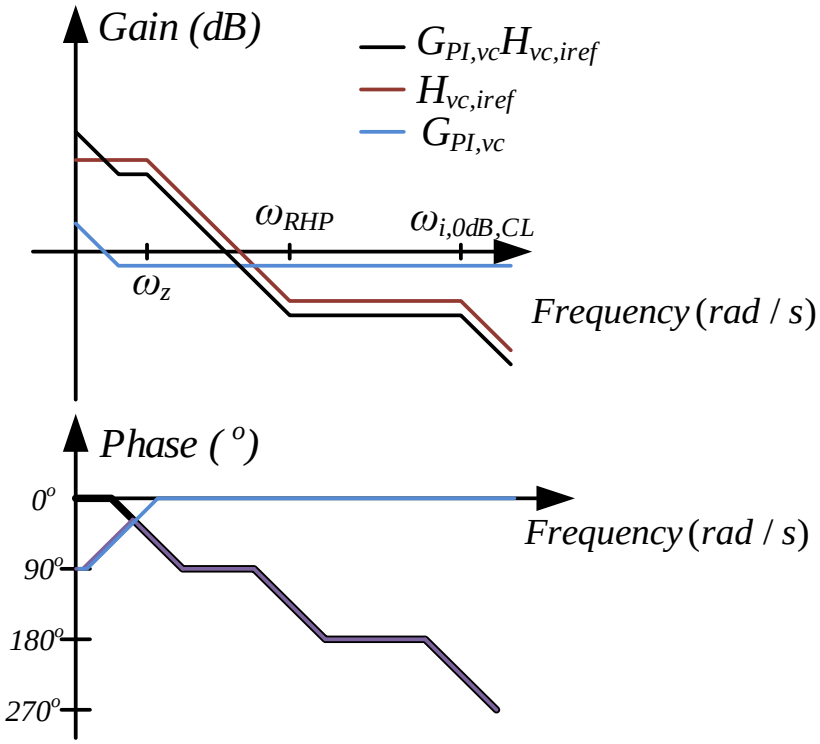

Figure 4-12 Simplified bode plot of voltage closed loop, open loop, and compensator transfer functions

4.2.2.3. Average arm sub-module voltage balancing

Differences in capacitance between all sub-modules can also cause steady-state voltage differences between the top and the bottom converter arms. This can be avoided by introducing an extra compensator, that maintains equal mean values of the top and bottom arm of the same leg. The error signal, that needs to be maintained at 0 is:

$$\Delta v_{C,x} = v_{C,a,x} - v_{C,b,x} \tag{4-49}$$

To transfer power between arms *a* and *b*, an extra current component needs to be injected. To avoid it flowing through the 3-phase load, this current needs to be common to both converter arms in the same leg. This can be achieved by adding another circulating current term, $i_{bal,x}$. The power transfer utilises the differential duty cycle $d_{ac,x}$, and $i_{bal,x}$ must be in phase with the 3-phase voltage waveforms:

$$i_{bal,x} = \frac{d_{ac,x,rms}}{Amplitude(d_{ac,x})} i_{bal,x}^{*} \qquad (4\text{-}50)$$

In equation (4-50) the ac duty cycle has been normalized to the amplitude of the ac duty cycle, which allows for constant controller gain over different values of the modulation index *m*. The balancing function can be modelled by the following transfer function:

$$v_{C,a/b,x}(s) = \frac{d_{ac,x,rms}}{sC} i_{bal,x}(s) \qquad (4\text{-}51)$$

The balancing transfer function only has a pole at the origin, which means it can use a proportional controller. Ignoring the limited bandwidth of the circulating current controller, the arm balancing control system should be unconditionally stable, as long as its crossover frequency is a decade below the circulating current loop bandwidth.

Since this system can use a proportional controller, its output must be multiplied by the ac duty cycle of each phase and this is achieved by multiplying its output by a waveform $y' = [d_{ac,u}, d_{ac,v}, d_{ac,w}]$.

4.2.2.4. Block diagram of average leg sub-module voltage controllers

The controllers discussed in section 4.2.2 are shown in a single block diagram in Figure 4-13:

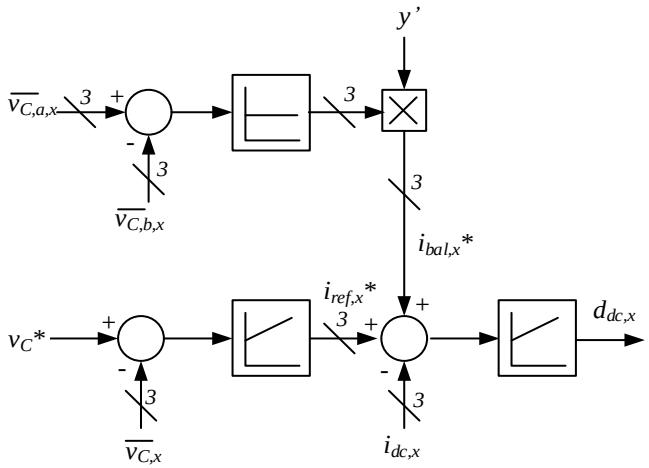

Figure 4-13 Leg sub-module voltage controller

4.2.3. 3-phase motor control

To implement 3-phase motor control the BMCI can use well established controllers, as the ac side of the converter is independent of the dc side, as long as the peak sum $d_{dc,x} + d_{ac,x} < 1$. For a traction drive, the control algorithm must implement field weakening to fully utilise the maximum power available from the converter and the prime mover, as well as third harmonic injection to achieve the maximum line-to-line voltage the converter can produce.

A key property of the asynchronous ac motor is the difference between rotor rotating frequency ω_r and 3-phase supply frequency ω_e, with a slip frequency ω_{slip} when the machine is mechanically loaded:

$$\omega_e = \omega_{slip} + \frac{p}{2}\omega_r \qquad (4\text{-}52)$$

When the motor is fed by a balanced 3-phase power supply, each phase will have the same current magnitude displaced by $2\pi/3$. At the steady state, the machine phase equivalent circuit can be simplified as:

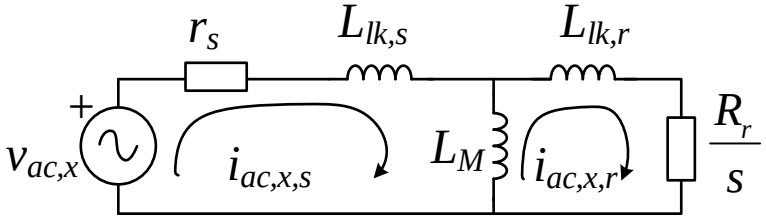

Figure 4-14 Induction machine per phase equivalent circuit

, where $i_{x,s}$ is the stator current and $i_{x,r}$ is the reflected rotor current. Each machine phase has a stator inductance $L_{lk,s}$, stator winding resistance r_s, magnetizing inductance L_M, primary reflected leakage rotor inductance $L_{lk,r}$ and resistance R_r, which is dependent on the slip of the machine:

$$s = \frac{\omega_e - \omega_r}{\omega_e} \qquad (4\text{-}53)$$

4.2.3.1. Vector control of Induction machine

The big advantage of vector control is that it can control an ac machine with similar torque dynamics as a dc-machine controller, while operating with a fixed PWM frequency. This can be done by expressing the asynchronous machine currents as a vector that is rotating at the machine synchronous electrical frequency ω_e.

i. Converting 3-phase stationary frame to 2-phase rotating frame

The Clark and Park transformations are standard tools used to convert the machine's 3-phase voltages in a stationary frame to an equivalent 2-phase frame, that is rotating at the synchronous frequency ω_e. For a matrix of 3-phase voltages $v_x = [v_u, v_v, v_w]$, they can be converted to an equivalent matrix of 2-phase voltages $v_{\alpha\beta}=[v_\alpha, v_\beta]$:

$$v_{\alpha\beta} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_u \\ v_v \\ v_w \end{bmatrix} \qquad (4\text{-}54)$$

$$\Gamma_{Clarke} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \qquad (4\text{-}55)$$

For 3 balanced currents, that also have no neutral leakage, $i_u + i_v + i_w = 0$, this transformation can be simplified for calculating $i_{ac,\alpha}$ and $i_{ac,\beta}$. The Clark transformation is the result of $i_{\alpha\beta} = i_{uvw}\Gamma_{Clarke}$:

$$\left.\begin{aligned} i_{ac,\alpha} &= i_u \\ i_{ac,\beta} &= \frac{2}{\sqrt{3}}\left(i_v - i_w\right) \end{aligned}\right\} \qquad (4\text{-}56)$$

Since the terms in the equations are also oscillating at ω_e, an additional transformation is required to refer the quantities to the rotating frame of reference. The park transform is used to calculate the direct and quadrature 2-phase rotating voltage matrix $v_{dq} = [\, v_d, v_q]$:

$$v_{dq} = \begin{bmatrix} \cos(\theta_e) & -\sin(\theta_e) \\ \sin(\theta_e) & \cos(\theta_e) \end{bmatrix}\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \qquad (4\text{-}57)$$

$$\Gamma_{Park} = \begin{bmatrix} \cos(\theta_e) & -\sin(\theta_e) \\ \sin(\theta_e) & \cos(\theta_e) \end{bmatrix} \qquad (4\text{-}58)$$

Using the conversion matrix in (4-58) the d and q currents can be calculated using $i_{dq} = \Gamma_{Park} i_{\alpha\beta}$:

$$\left.\begin{aligned} i_{ac,s,d} &= i_{ac,\alpha}\cos\left(\theta_e\right)+i_{ac,\beta}\sin\left(\theta_e\right) \\ i_{ac,s,q} &= i_{ac,\beta}\cos\left(\theta_e\right)-i_{ac,\alpha}\sin\left(\theta_e\right) \end{aligned}\right\} \quad (4\text{-}59)$$

ii. Asynchronous motor plant model

The per-phase model of the asynchronous motor can be derived from the per-phase equivalent circuit from Figure 4-14:

$$v_{ac,x} = i_{ac,x,s}R_r + L_{lk,s}\frac{di_{ac,x,s}}{dt} + L_M\frac{d\left(i_{ac,x,s}-i_{ac,x,r}\right)}{dt} \quad (4\text{-}60)$$

Applying the matrices Γ_{Clarke} and Γ_{Park} to (4-60), the per-phase stationary frame circuit is transformed into the 2-phase rotating frame circuits:

$$v_{ac,s,d} = r_s i_{ac,s,d} + L_{lk,s}\frac{d}{dt}i_{ac,s,d} + \frac{L_M}{L_r}\frac{d}{dt}\Phi_{r,d} - \omega_e L_{lk,s} i_{ac,s,q} \quad (4\text{-}61)$$

$$v_{ac,s,q} = r_s i_{ac,s,q} + L_{lk,s}\frac{d}{dt}i_{ac,s,q} + \omega_e\frac{L_M}{L_r}\Phi_{r,d} + \omega_e L_{lk,s} i_{ac,s,d} \quad (4\text{-}62)$$

, where $\Phi_{r,d}$ is the rotor *d* axis flux:

$$\Phi_{r,d} = L_r i_{ac,r,d} + L_M i_{ac,s,d} \quad (4\text{-}63)$$

The primary reflected rotor inductance L_r is:

$$L_r = L_M + L_{lk,r} \quad (4\text{-}64)$$

And the equation for the electromagnetic torque, T_{em} is:

$$T_{em} = \frac{p}{2}\Phi_{r,d}\frac{L_M}{L_r}i_{ac,s,q} \quad (4\text{-}65)$$

iii. Rotor flux observer

The rotor flux observer uses the stator current $i_{ac,s,d}$:

$$\frac{d}{dt}\Phi_{r,d} = \frac{L_M i_{ac,s,d}}{\tau_r} - \frac{\Phi_{r,d}}{\tau_r} \quad (4\text{-}66)$$

The slip frequency can be calculated from the rotor flux and stator current $i_{ac,s,q}$:

$$\omega_{slip} = \frac{L_M i_{ac,s,q}}{\Phi_{r,d}} \quad (4\text{-}67)$$

The electrical angle, used for the Clarke and Park transforms uses the rotor speed ω_r and motor pole pairs p:

$$\theta_e = \int \left(\omega_{slip} + p\omega_r \right) dt \quad (4\text{-}68)$$

iv. Controller design

The stator current models of the d and q axis, have cross-coupling components, containing the rotor flux and rotor flux derivative. The derivative of $\Phi_{r,d}$ is considered to be negligible and the control system can be compensated by the simplified terms:

$$v_{comp,d} = -\omega_e L_{lk,s} i_{ac,s,q} \quad (4\text{-}69)$$

$$v_{comp,q} = \omega_e \frac{L_M}{L_r} \frac{d}{dt}\Phi_{r,d} + \omega_e L_{lk,s} i_{ac,s,d} \quad (4\text{-}70)$$

Adding (4-69) and (4-70) to (4-61) and (4-62) respectively, results in the following differential equations for the stator currents:

$$L_{lk,s} \frac{d}{dt} i_{ac,s,d} = -r_s i_{ac,s,d} - \frac{L_M}{L_r} \frac{d}{dt}\Phi_{r,d} + v_{comp,d} \quad (4\text{-}71)$$

$$L_{lk,s} \frac{d}{dt} i_{ac,s,q} = -r_s i_{ac,s,q} - \omega_e \frac{L_M}{L_r} \frac{d}{dt}\Phi_{r,d} + v_{comp,q} \quad (4\text{-}72)$$

Since the machine voltages are generated by the BMCI, the d and q stator voltages can be replaced by:

$$\left.\begin{aligned} v_{ac,s,d} &= d_{ac,d} n V_C \\ v_{ac,s,q} &= d_{ac,q} n V_C \end{aligned}\right\} \tag{4-73}$$

The *d* and *q* duty cycles, $d_{ac,d}$ and $d_{ac,q}$, are generated by the outputs of the *d* and *q* axis current compensators, that have the following transfer functions:

$$d_{ac,d/q} = \frac{s k_{p,iac} + k_{i,iac}}{s} \tag{4-74}$$

To calculate the stator current compensator gains, $k_{p,iac}$ and $k_{i,iac}$, the transfer function of the motor is first required. As the BMCI is used in a traction converter, the rotor flux dynamics will be determined by the asynchronous motor's inertial load. For a vehicle application, the dynamics of the mechanical system will be several orders of magnitude slower than those of the electrical system. Thus, the flux dynamics are ignored for the small-signal model and it can be derived by substituting (4-73) in (4-71) and (4-72), and including the BMCI's output impedance:

$$\frac{i_{ac,s,d/q}(s)}{d_{ac,d/q}(s)} = \frac{n V_C}{L_{lk,s}\left(s + \omega_{z,s}\right)} = G_{iac} \frac{1}{s + \omega_{z,s}} \tag{4-75}$$

$$\omega_{z,s} = \frac{r_s + \frac{r_{arm}}{2}}{L_{lk,s}} \tag{4-76}$$

, where G_{iac} is the small-signal dc gain:

$$G_{iac} = \frac{n V_C}{r_s + \frac{r_{arm}}{2}} \tag{4-77}$$

The crossover frequency of the stator current plant can be calculated from the dc gain and the break frequency of the stator circuit:

$$\omega_{iac,0dB} = \beta_{iac} G_{iac} \omega_{z,s} \tag{4-78}$$

, where β_{iac} is the ac current feedback gain. As with the dc current controller, the closed loop bandwidth $\omega_{iac,0dB,CL}$ can be set by shifting the plant's crossover frequency using the compensator proportional gain:

$$k_{p,iac} = \frac{\omega_{iac,0dB,CL}}{\omega_{iac,0dB}} \tag{4-79}$$

The integrator gain can be set relative to $\omega_{iac,0dB,CL}$ to give a phase margin of 74°:

$$k_{i,iac} = 0.1\omega_{iac,0dB,CL} k_{p,iac} \tag{4-80}$$

The motor plant current transfer function is of the first order and the maximum phase shift is 90°. As with the dc current controller, the modulator delay is taken into account by using (4-30), and the forward transfer function is calculated:

$$H_{plant,ac} = \beta_{iac} H_{ZOH} H_{iac} \tag{4-81}$$

v. Converting 2-phase rotating frame voltages to 3-phase stationary frame voltages

The final step of the vector controller is to calculate the three ac duty cycles $d_{ac,x}$ that are used in the generation of the arm inserted voltage commands. This is done by executing the inverse of the transformations described in section i. The inverse Park transformation calculates the duty cycles $d_{ac,s,\alpha}$ and $d_{ac,s,\beta}$:

$$\left.\begin{aligned} d_{ac,s,\alpha} &= d_{ac,s,d}\cos(\theta_e) - d_{ac,s,q}\sin(\theta_e) \\ d_{ac,s,\beta} &= d_{ac,s,q}\cos(\theta_e) + d_{ac,s,d}\sin(\theta_e) \end{aligned}\right\} \tag{4-82}$$

The final step is the inverse Clark transformation:

$$\left.\begin{aligned} d_{ac,s,u} &= d_{ac,s,\alpha} \\ d_{ac,s,v} &= \frac{-d_{ac,s,\alpha} + \sqrt{3} d_{ac,s,\beta}}{2} \\ d_{ac,s,w} &= \frac{-d_{ac,s,\alpha} - \sqrt{3} d_{ac,s,\beta}}{2} \end{aligned}\right\} \quad (4\text{-}83)$$

4.2.3.2. Third harmonic injection and control system overview

Conventional 3-phase sinusoidal modulation allows for limited utilisation of the inverter's dc-link. Triangular third harmonic injection uses the 3-phase ac duty cycles, $d_{ac,s,x}$, to calculate a common mode signal, that does not require the phase angle θ_e.

$$d_{thi} = \frac{\max\left(d_{ac,s,u}, d_{ac,s,v}, d_{ac,s,w}\right) + \min\left(d_{ac,s,u}, d_{ac,s,v}, d_{ac,s,w}\right)}{2} \quad (4\text{-}84)$$

The resultant waveform is a triangular, and is oscillating at 3 times the frequency ω_e, and the peak phase-to-phase voltage is increased by 15.4% to achieve full utilisation of the available voltage from the capacitor sub-modules. The peak value occurs at values of θ_e divisible by 60°, as illustrated in:

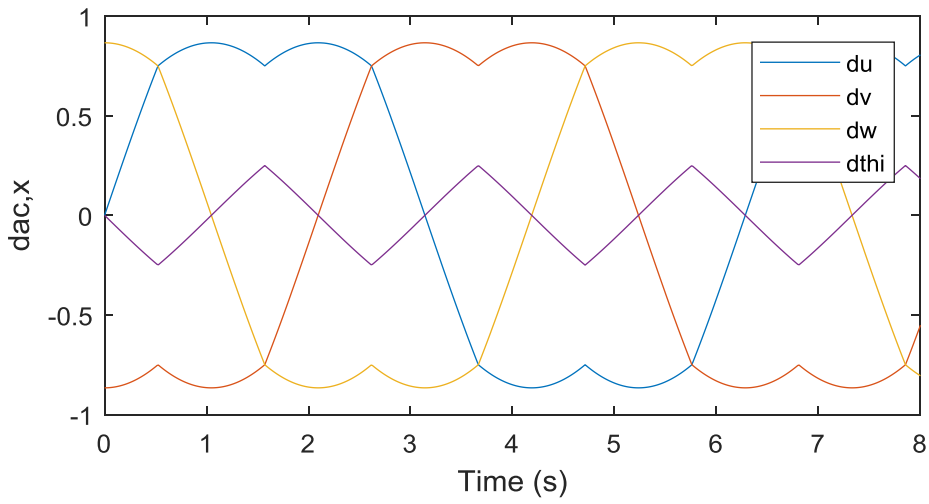

Figure 4-15 Third harmonic injection modulation waveforms

In Figure 4-15, the modulation duty cycles of each phase are shown and they are calculated by subtracting d_{thi} to the three values $d_{ac,s,x}$ to calculate the duty cycles $d_{ac,x}$:

$$d_{ac,x} = d_{ac,s,x} - d_{thi} \qquad ,x = u,v,w \tag{4-85}$$

4.2.3.3. Block diagram of induction motor controller

The block diagram is shown in Figure 4-16. The Clarke and Park transformations have been lumped into a single *abc/dq* block, while the inverse Park and Clarke transformations are represented by a *dq/abc* block.

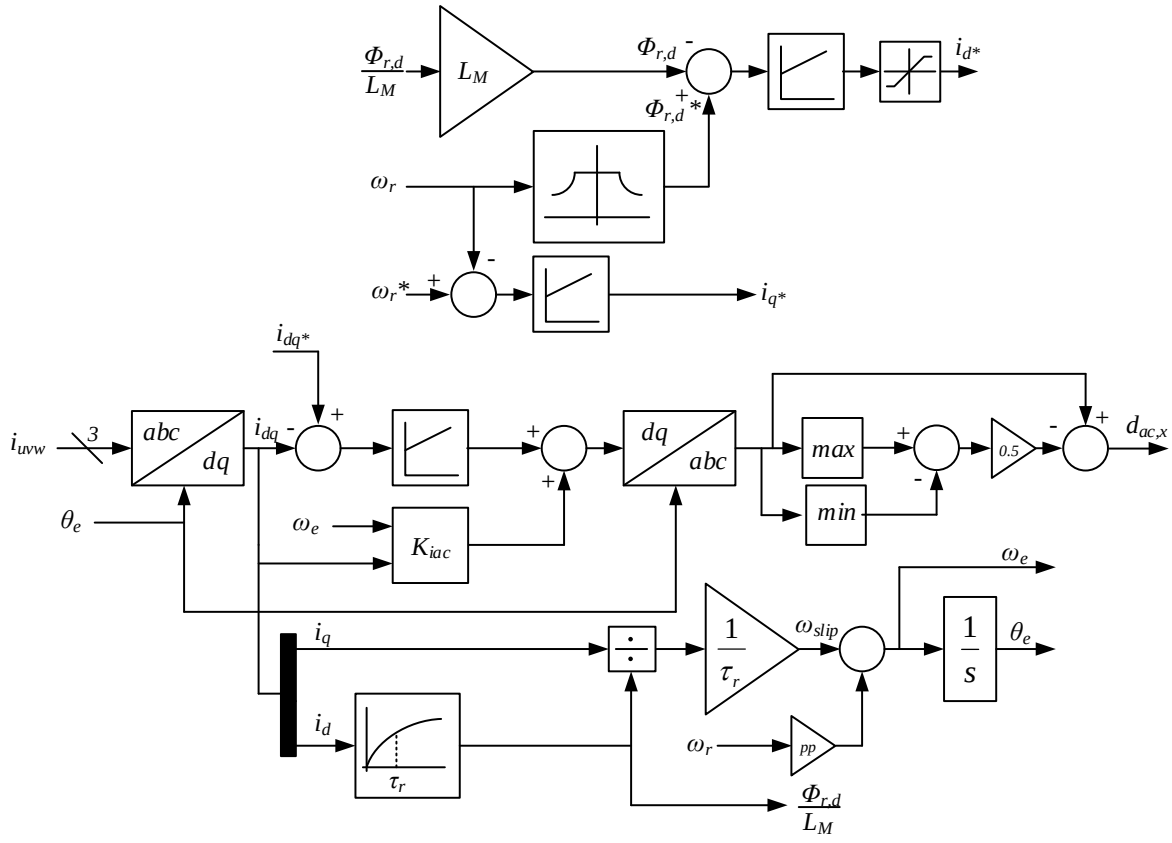

Figure 4-16 Control system of induction motor

According to equation (4-66), the flux can be modelled as a first order system with the input being the current i_d. This allows for the flux to be controlled by using the estimated flux as the feedback variable and i_d as the input. The flux controller bandwidth must be at least 10 times smaller as to not interfere with the current controllers.

4.2.4. Injected balancing power for low frequency compensation

When the BMCI is working with modulation index < 1, the available duty cycle, equal to $1-max(d_{ac,x})-d_{dc,x}$, can be used to balance the voltage between each pair of arms *a* and *b*. This balancing duty cycle d_{lf} is differential to arms *a* and *b*, the same as $d_{ac,x}$. For the balancing power to not flow through the load, d_{lf} is common to all three legs:

$$\left.\begin{aligned} d_{a/b,u} &= d_{dc,u} \mp d_{ac,u} \mp d_{lf} \\ d_{a/b,v} &= d_{dc,v} \mp d_{ac,v} \mp d_{lf} \\ d_{a/b,w} &= d_{dc,w} \mp d_{ac,w} \mp d_{lf} \end{aligned}\right\} \qquad (4\text{-}86)$$

$$\left.\begin{aligned} v_{uv} &= \frac{d_{b,u}-d_{a,u}}{2} - \frac{d_{b,v}-d_{a,v}}{2} = d_{ac,u} n V_C \\ v_{vw} &= \frac{d_{b,u}-d_{a,v}}{2} - \frac{d_{b,v}-d_{a,w}}{2} = d_{ac,v} n V_C \\ v_{wu} &= \frac{d_{b,w}-d_{a,w}}{2} - \frac{d_{b,u}-d_{a,u}}{2} = d_{ac,w} n V_C \end{aligned}\right\} \qquad (4\text{-}87)$$

Power transfer between arms *a* and *b* is achieved by injecting an additional circulating current $i_{lf,x}$, common to both arms, that is in phase with the common mode voltage, thus discharging the capacitors of one arm and charging those of the other one. The current $i_{lf,x}$ is specific to each phase leg, and unless all three currents sum up to 0, the compensation current will flow through the input power source.

$$p_{lf,x} = i_{lf,x} \times d_{lf} \times n V_C \qquad (4\text{-}88)$$

The power $p_{lf,x}$ must be alternating to achieve stability with capacitors in the sub-module capacitors. The frequency of oscillation can be chosen arbitrarily. It has to be lower than the transistor switching frequency f_Q, but high enough to cause a small ripple in the sub-module capacitor voltages. As the inserted voltage, proportional to d_{lf}, is controlled by the arms' switching functions, its rate of change is only limited by the switching speed of the transistors in each sub-module. This allows for the shape of d_{lf} to be that of a square waveform:

$$d_{lf} = sign\left[\sin\left(\omega_{lf} t\right)\right] \times \min(d_{dc,u}, d_{dc,v}, d_{dc,w}) \quad (4\text{-}89)$$

In an ideal case, the balancing current $i_{lf,x}$ would be also have a rectangular waveform. The amplitude of this waveform is determined by the arm balancing compensator. A diagram of the low-frequency arm balancing control system is shown in

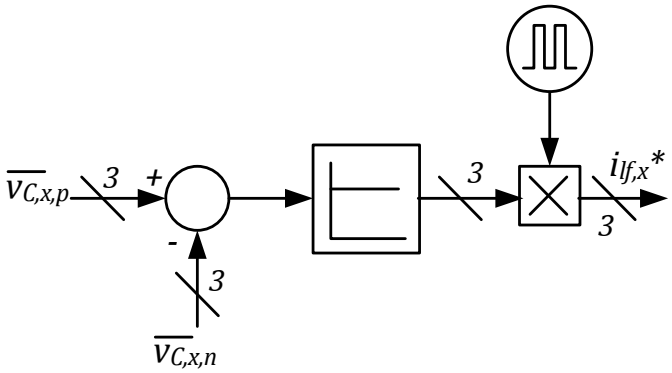

Figure 4-17 Diagram of low-frequency arm balancing compensator

The compensator in Figure 4-17 is a proportional type, as a dc value of i_{lf} will result in a voltage ramp across the capacitors. The gains can be set according to the model of the capacitor current transfer function:

$$v_{C,a/b,x}(s) = \frac{d_{lf}}{sC} i_{lf,x}(s) \quad (4\text{-}90)$$

The low-frequency balancing controller has similar plant model to the normal range arm balancing controller, and thus can use the same structure, with just a change in the balancing carrier waveform y':

$$y' = sign\left[\sin\left(\omega_{lf}\right)\right] \quad (4\text{-}91)$$

4.2.5. Converter control systems

The control systems for the full converter are grouped in two parts – dc-side and ac-side. The dc-side control system includes the circulating current controller, balancing controllers, and average capacitor voltage controllers, as shown in Figure 4-18:

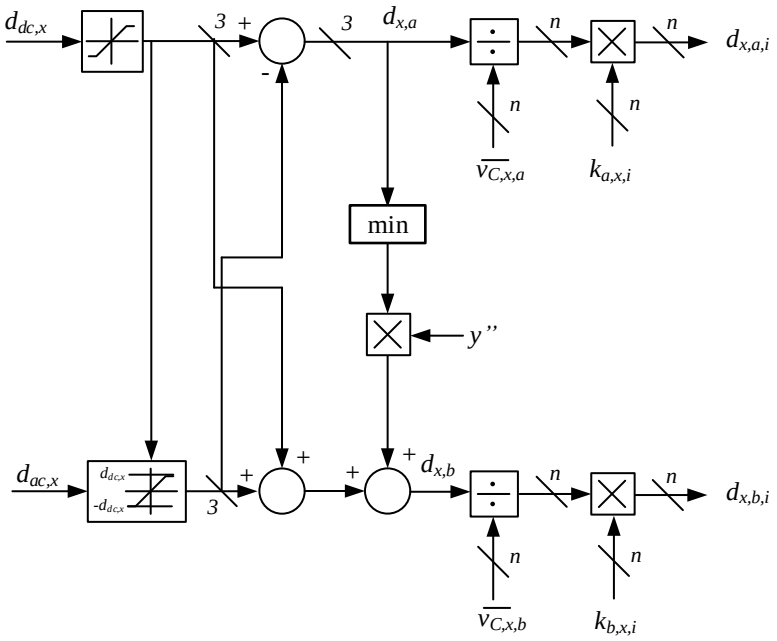

Figure 4-18 Converter arm control signals

4.2.5.1. Controller limits

The ac and dc duty cycles $d_{dc,x}$ and $d_{ac,x}$ must be complementary, but they control separate variables. To avoid interference between the dc-side and ac-side current controllers, the limits of the duty cycles must be carefully chosen.

For a vehicle, there will be two energy sources – the prime mover, connected to the dc-side of the converter, and the kinetic energy stored in the vehicle's mass. If the duty cycles are not limited, two scenarios can occur.

i. dac,x increases and causes da/b,x to saturate

When the ac duty cycle causes the arm duty cycles to saturate, for a BMCI with positive dc-side voltage, this will always occur at $d_{a/b,x}=1$. On the negative half-cycle, the converter will not be in saturation until $d_{ac,x} \geq 1+d_{dc,x}$ and at $d_{ac,x}=d_{dc,x}-d_{ac,x,max}$ the total inserted dc voltage will no longer be $2d_{dc,x}nV_C$ as shown in Figure 4-19. This offset can cause a very high current to be drawn from the dc power source.

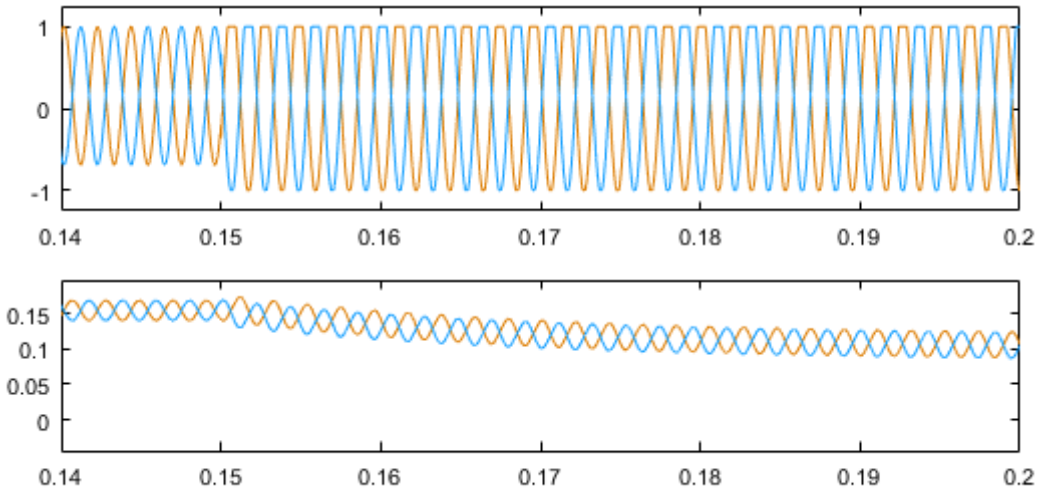

Figure 4-19 Effect of arm duty cycle saturation (above) on filtered arm voltage (below)

ii. $d_{dc,x}$ increases and causes $d_{a/b,x}$ to saturate

If the dc power source cannot absorb power under any circumstances, an unlimited closed-loop circulating current controller will keep increasing $d_{dc,x}$ until a value of 1 is reached. This will raise the value around which $d_{ac,x}$ is oscillating, clipping it at $d_{ac,x}=1-d_{dc,x,max}$. This asymmetry will occur during the next half-cycle as well, just in the other converter arm. The end result is a clipped ac voltage waveform. In a large traction motor, the winding resistance can be very small, and even a change of a few volts can cause a large current to flow, which in turn will apply a very high torque to the traction motor, causing it to decelerate rapidly.

iii. Proposed solution

Considering the two scenarios the strategy adopted is to use a variable limit for the ac duty cycle, set by the smallest of the three dc duty cycles:

$$\pm \lim_{d,ac} = 1 - \max\left(d_{dc,u}, d_{dc,v}, d_{dc,w}\right) \tag{4-92}$$

An important point is that the limit will clip $d_{ac,x}$ symmetrically. This strategy ensures that each leg can return power to the dc source or dissipate it in a braking chopper

resistor. The limits use the maximum value of the dc duty cycles of the whole converter to avoid any unbalanced voltages across the output.

4.3. SUMMARY

This chapter reviews the different modulation schemes used for MCCs and are applicable to the BMCI. The control systems required for the operation of the converter are also presented, together with the design methodology used for tuning.

Pulse-width modulation is the type used for this thesis, as it is readily available from commercial digital controllers. A phase-shifted carrier scheme is used, as it results in equal switching losses across all sub-modules, without intermittent peaks and troughs typical of level-shifted schemes.

A novel sub-module balancing strategy is presented and discussed. The proposed solution does not introduce an error between the arm command and the actual average of all sub-module duty cycles. However, more investigation is required to fully characterize it and compare to other state-of-the-art methods.

The BMCI current and voltage controllers are identical to those of a cascaded boost dc-dc converter and 3-phase inverter, and the different break frequencies required for the design of the compensator are extrapolated.

Chapter 5. GENERAL DESIGN FOR AN *N*-MODULE BMCI AND EXPERIMENTAL CONVERTER

This chapter describes the design procedure for an *n*-module boost multilevel cascaded inverter (BMCI). The relationships between number of sub-modules and ac-side voltage quality, and size of leg inductance are examined, as well as the effects of different modulation strategies. The converter design uses dc-side voltage, ac-side peak voltage, machine base frequency, and maximum capacitor voltage ripple as design parameters and the presented method is used to design the laboratory prototype, which is used in this work as proof of concept.

A design example for a fuel-cell BMCI drive can be found in Appendix A. The schematics of the 4 main PCBs of the prototype BMCI can be found in Appendix C.

5.1. GENERAL CONVERTER DESIGN

The design of the converter requires the definition of the number of sub-modules per arm n, the total leg inductance L_{Leg}, and the submodule capacitance C_{SM}. The number of sub-modules has a direct effect on the other two parameters and must be defined first. The capacitance and the inductance are then determined by the maximum allowable peak-to-peak voltage ripple and leg current ripple, respectively.

Following the same conventions as Chapter 3, the general converter diagram is shown in Figure 5-1:

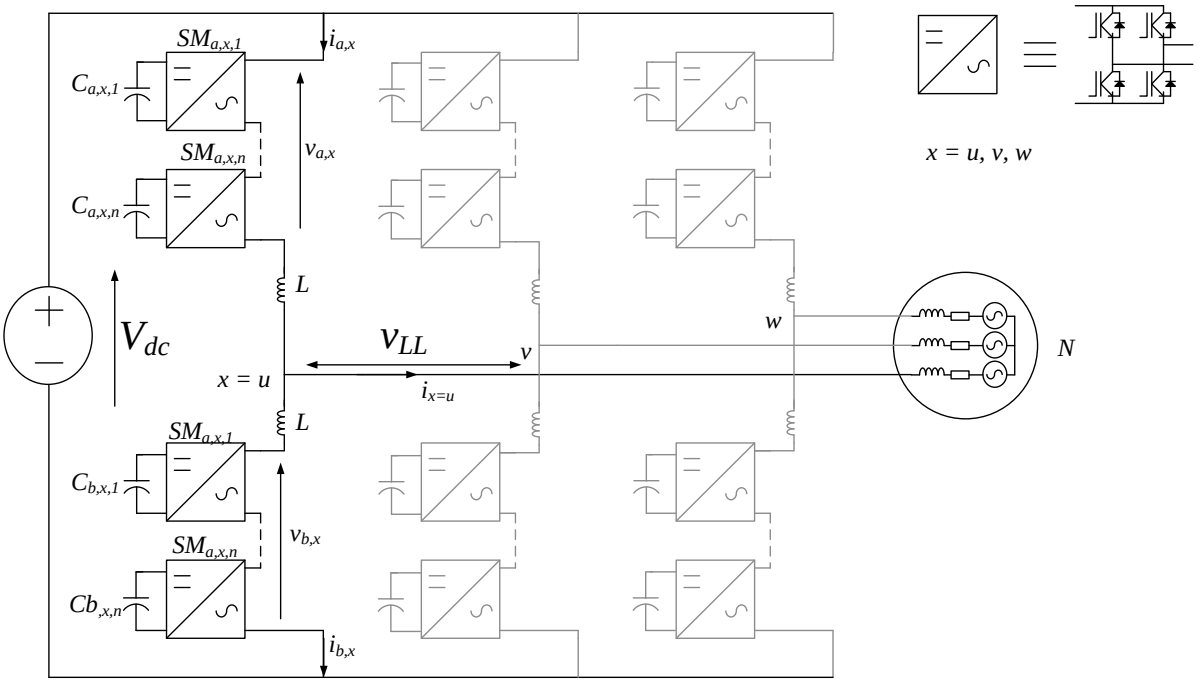

Figure 5-1 Basic BMCI structure

The converter's dc-side voltage is v_{dc}, top arm inserted voltage is $v_{a,x}$, bottom arm inserted voltage is $v_{b,x}$, where x is the phase designator, equal to u, v, or w. The sum of each pair of converter arms produces a dc voltage $v_{dc,x}$, and the difference produces the phase-to-neutral voltage v_x:

$$v_{dc,x} = v_{a,x} + v_{b,x} \tag{5-1}$$

$$v_x = \frac{v_{b,x} - v_{a,x}}{2} \tag{5-2}$$

For an ideal converter the inserted dc-side voltage $v_{dc,x} \rightarrow v_{dc}$, and the phase voltage v_x is a sinusoid with amplitude V_x, and for a 3-phase output each leg will have a displacement angle $\varphi_x = 0$, $-2\pi/3$, and $-4\pi/3$, for $x = u$, v, and w, respectively:

$$v_x = V_x \sin(\omega_x t - \phi_x) \tag{5-3}$$

The arm voltages are calculated from:

$$\left.\begin{aligned} v_{a,x} &= v_{dc,x} - v_x \\ v_{b,x} &= v_{dc,x} + v_x \end{aligned}\right\} \qquad (5\text{-}4)$$

The top and bottom arm currents are $i_{a,x}$ and $i_{b,x}$. The sum of these two currents results in the leg circulating current $i_{dc,x}$, the difference forms the line current, and the sum of the three circulating currents is the BMCI's input current:

$$i_{dc,x} = \frac{i_{L,a,x} + i_{L,b,x}}{2} \qquad (5\text{-}5)$$

$$i_x = i_{L,a,x} - i_{L,b,x} \qquad (5\text{-}6)$$

$$i_{IN} = \sum_{x=u,v,w} i_{dc,x} \qquad (5\text{-}7)$$

5.1.1. Choice of number of sub-modules n and inverter waveform levels

The modular cascaded converter (MCC) was developed for use in high-voltage dc (HVDC) substations. With transmission line voltages in the range of tens to hundredths of kVs, there is no single device that can withstand the full dc-link voltage, and a high number of sub-modules becomes a necessity.

In comparison traction drives in the railway sector work with peak ac-side voltages between 750V and 3.5kV, requiring IGBT collector-emitter voltages rated between 1.2kV and 6.5kV. In the automotive market the choice of transistors increases even further when the dc-link voltage is between 300 and 700V.

Thus, for a low-voltage MCC-type converter, the required ac-side voltage is not the only design parameter, that determines the number of sub-modules *n,* and factors such as leg inductance and ac-side voltage distortion become more dominant. High values of *n*

however increase the converter's complexity, as more gate drivers and voltage transducers are required.

The maximum dc-side voltage and the peak line-to-line output determine the maximum voltage each converter arm must produce:

$$\max(v_{a/b,x}) = \frac{\max(V_{LL} - V_{IN})}{2}, \qquad (5\text{-}8)$$

, where V_{LL} is the amplitude of the line-to-line voltage, and V_{IN} is the maximum dc-side voltage. This value is for a converter using third harmonic injection, as sinusoidal PWM does not utilise the full voltage available from the capacitors. Equation (5-8) shows that as the converter dc-side voltage reduces, the required maximum arm voltage relaxes. The minimum number of sub-modules becomes:

$$n = \frac{\max(v_{a/b,x})}{V_{C,nom}}, \qquad (5\text{-}9)$$

, where $V_{C,nom}$ is the nominal sub-module capacitor voltage. The arm in the (BMCI) uses full-bridge (FB) sub-modules, and can produce both positive and negative voltages. The number of voltage steps in each arm, n_{arm}, is $2n+1$ as a maximum, which is achieved at dc duty cycles $d_{dc}<0.5/n$. With every increment of d_{dc} by $0.5/n$, n_{arm} decreases by 1. The number of phase voltage levels, n_x, is dependent on n_{arm}, as v_x is derived from (5-2). It should be noted that the voltage v_x is measured between the load neutral and the common connection between the two leg inductors.

For comparison a conventional modular cascaded converter (MCC), with half-bridge (HB) sub-modules, the number of output levels for each arm, n_{arm} is $n+1$, with $d_{dc}=0.5$. For a BMCI an increment of d_{dc} by $0.5/n$, n_{arm} decreases by 1, resulting in:

$$n_{arm} = 2n + 1 - round\left(n \times d_{dc,x}\right), \tag{5-10}$$

, where *round()* is a rounding function. The output of (5-10) is independent on the type of modulation employed, however the phase voltage levels, n_x, is not.

Chapter 4 examines the control implications of two modulation schemes - (PSC) and Phase disposition carrier (PDC), shown in Figure 5-2:

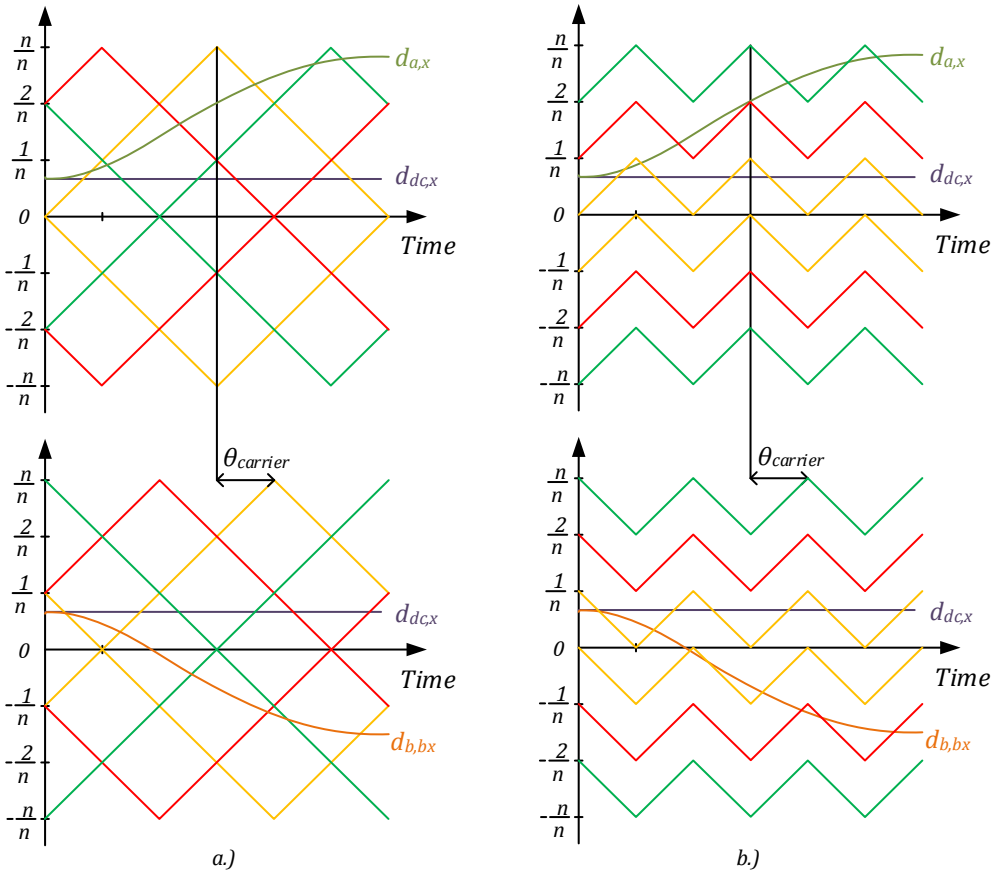

Figure 5-2 Modulation for top and bottom converter arms, Phase shifted carrier a.), and Phase disposition carrier b.)

Each carrier in Figure 5-2 a.) oscillates at frequency $2f_{sw,Q}$, which is twice the individual transistor switching frequency $f_{sw,Q}$, while the carriers in Figure 5-2 b.) oscillate at nf_{sw}. However, the effective arm switching frequency is the same for both cases, as the PSC carriers are interleaved, and produce the same switching frequency $f_{arm}=nf_{sw}$.

To compare the effects of the two modulation schemes more easily, the PSC modulation can be represented as alternate phase opposition disposition which will

produce the same arm voltage waveform [151]. APOD is simpler to analyse, as each modulation carrier corresponds to a single level and oscillates at the effective arm switching frequency, which is the same condition as the PDC modulation:

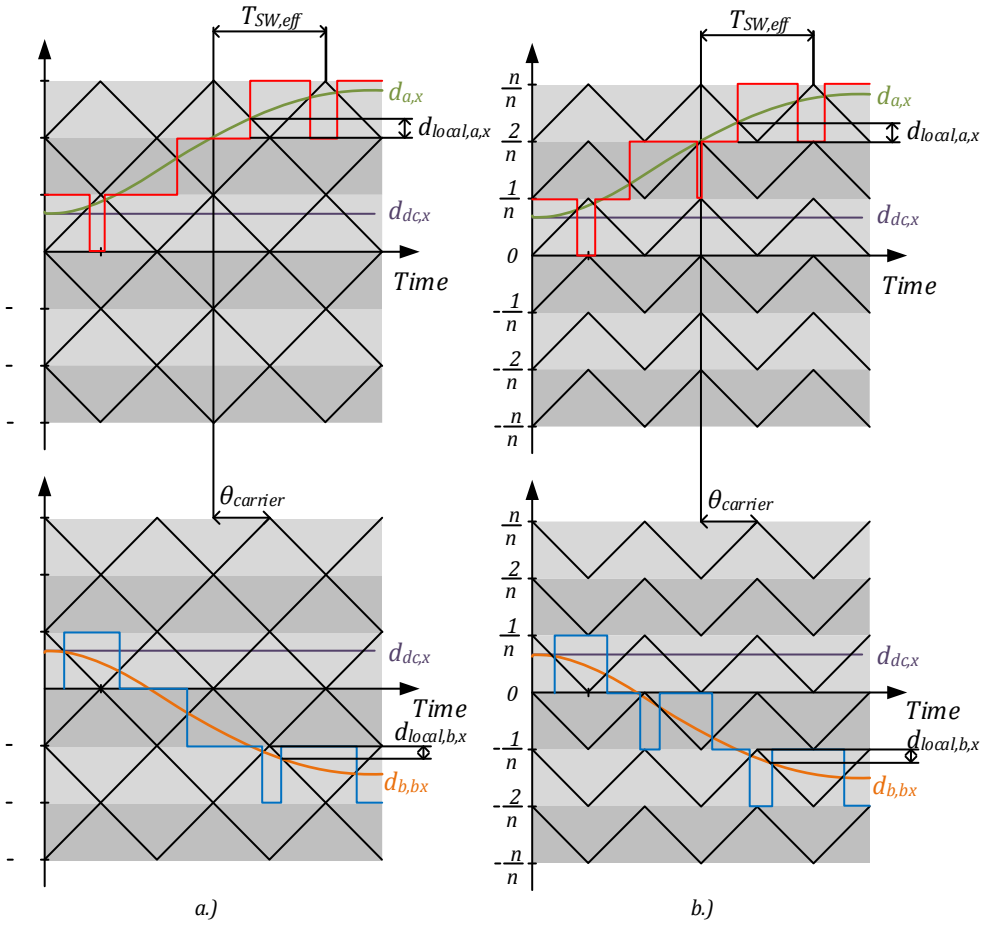

Figure 5-3 PWM modulation using APOD carriers a.) and PDC carriers b.)

With each carrier localised at a certain arm level, the PWM waveform will have a local duty cycle $d_{local,a/b,x}$, which cycles from 0 to 100% every time the arm modulation signal increases or decreases by $1/n$. When the arm duty cycle becomes negative, the local duty cycle is the fraction of the switching cycle. The voltage is most negative during the active portion of the duty cycle.

Since each arm has its own set of carriers, arm a and arm b carriers can be offset by an angle $\vartheta_{carrier}$, also shown in Figure 5-2 and Figure 5-3. The effect of $\vartheta_{carrier}$ is more pronounced at values of $d_{dc,x}$ that are divisible by $0.5/n$, where the local arm duty cycles

are complementary. When a rising edge from arm *b* aligns with a falling edge from arm *a*, the voltage step of v_x is equal to $V_{C,nom}$ and has a switching frequency $f_{sw,eff}$. In the opposite condition, the two pulses are effectively interleaved and the resultant v_x has voltage steps of $V_{C,nom}/2$, with switching frequency $2f_{sw,eff}$. An example, using PSC modulation and $d_{dc,x} = 1/n$, is shown in Figure 5-4:

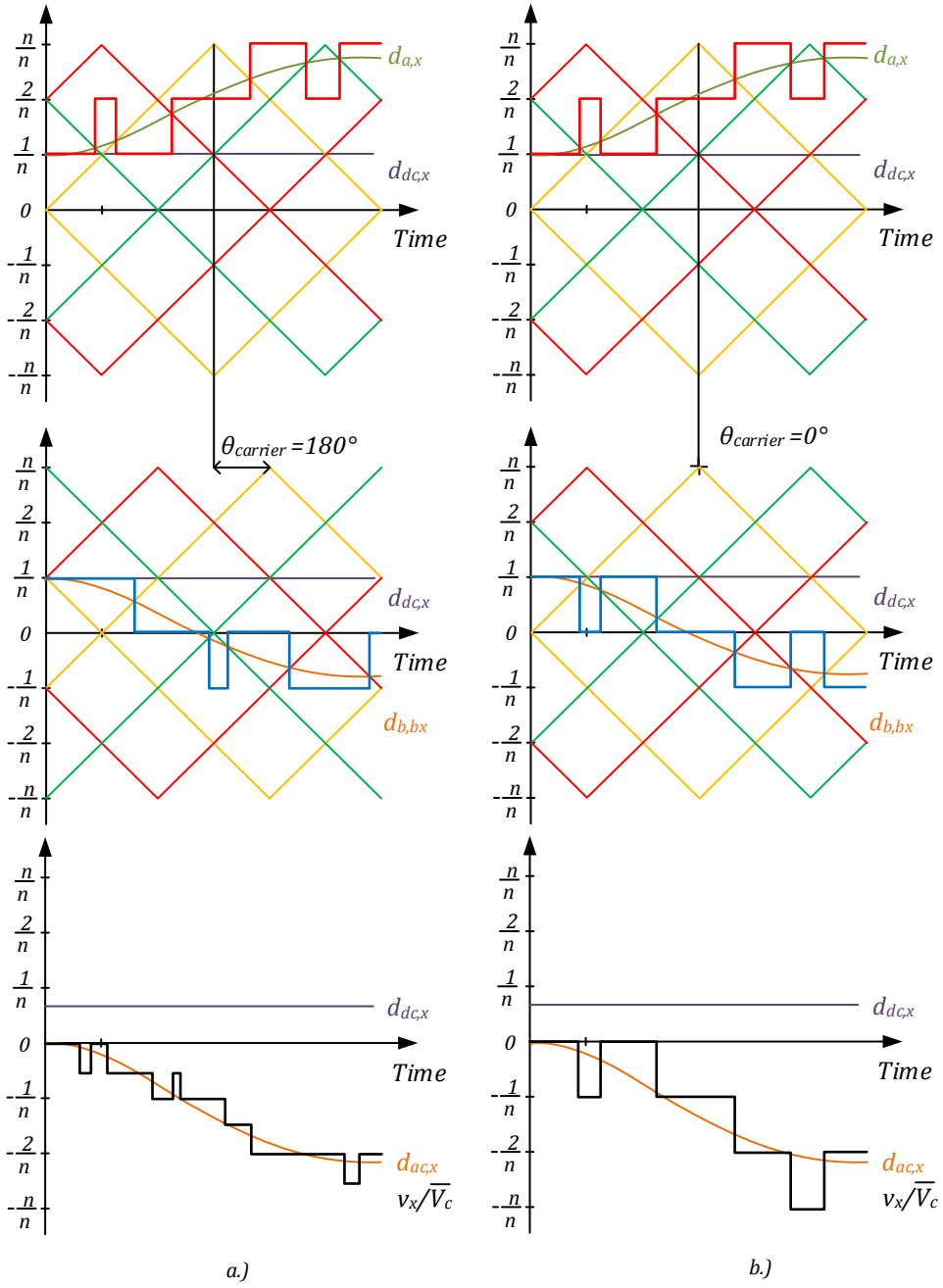

Figure 5-4 Pulsed waveforms of arm and phase voltages, with carrier phase shift of 180° a.) and 0° b.)

The relationship between ac-side voltage levels and phase shift is also different for odd or even number of sub-modules. This is due to the position of $d_{dc,x}$ relative to the local carrier. The relationship between n, $\vartheta_{carrier}$, and $d_{dc,x}$ is summarised in Table 5-1:

Table 5-1 BMCI phase voltage levels with different carrier phase shift

	$\theta_{carrier}=0$	$\theta_{carrier}=\frac{\pi}{2n}$
Number of sub-modules	n	
Number of active arm levels n_{arm}	$2n+1-floor\left(\frac{nd_{dc,x}}{0.5}\right)$	
Number of phase voltage levels n_x for $d_{dc}\rightarrow k/n$, for $k=0, 1, 2, \ldots, n$	n_{arm}	$2n_{arm}-1$
Number of phase voltage levels n_x for $d_{dc}\rightarrow (k+0.5)/n$, for $k=0, 1, 2, \ldots, n$	$2n_{arm}-1$	n_{arm}

Since the dc duty cycle d_{dc} introduces an offset, around which the sinusoidal d_{ac} oscillates, over the range from 0 to 1 there are $2n$ operating points, where the modulated signal produces symmetrical waveforms in each arm. These are the boundary conditions described in Table 5-1. For values of d_{dc} between these boundaries, the arm pulses are not symmetric between the top and the bottom arms, but this asymmetry repeats each half-cycle, making the ac-side voltage free of second order harmonics. At the phase output, this gives rise to additional switching actions, resulting in a waveform that oscillates between 3 levels over one carrier cycle. Compared to a conventional multilevel inverter, i.e. floating

capacitor or diode-clamped inverter, the phase voltage always switches between two neighbouring levels:

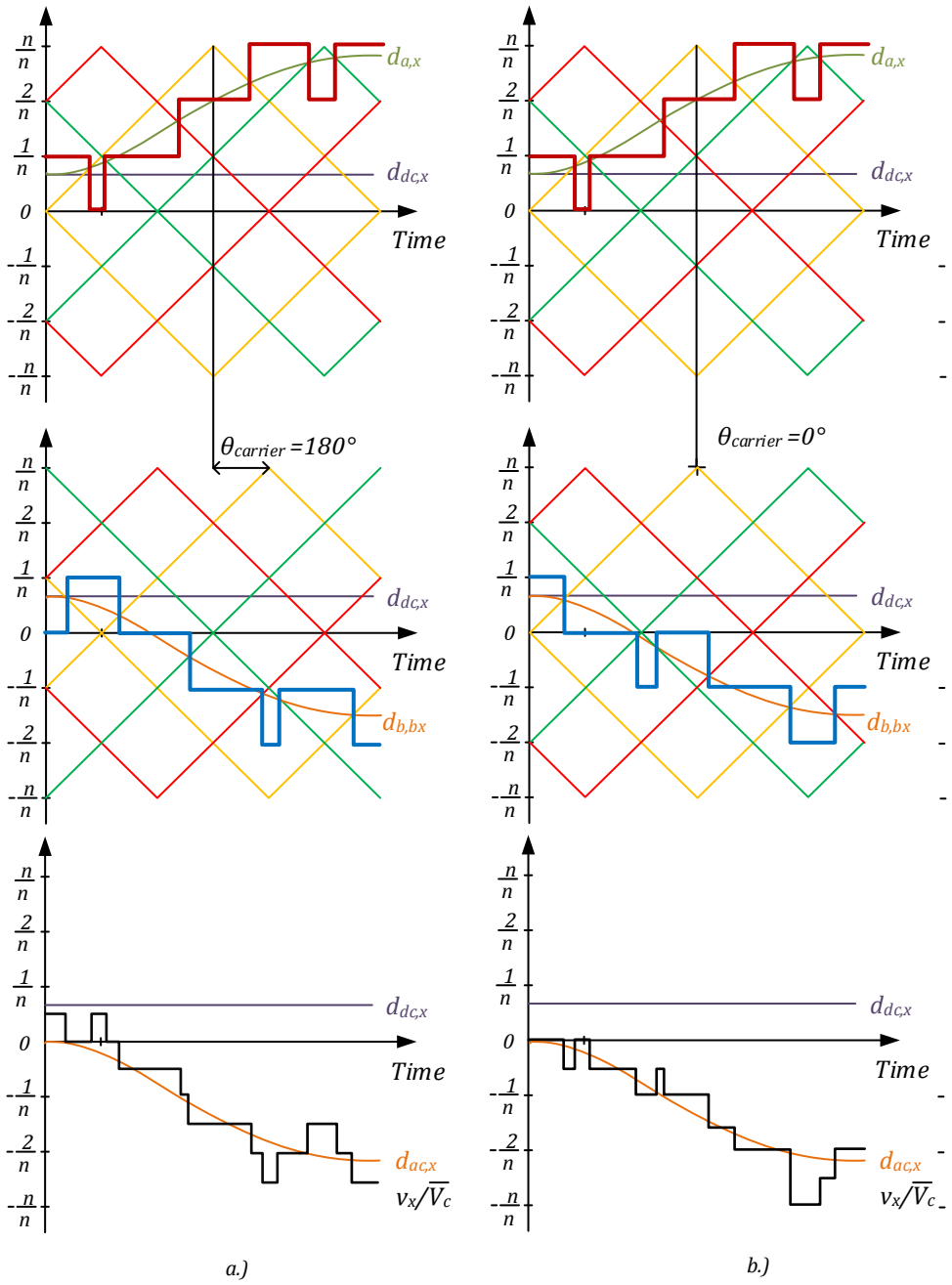

Figure 5-5 Arm and phase voltage waveforms with $0.5/n < d_{dc,x} < 1/n$, and $\vartheta_{carrier} = 180°$ a.) or $\vartheta_{carrier} = 0°$ b.)

The two normalised phase voltage waveforms, from Figure 5-5, are both formed of half and full-steps. A judgment cannot be made as to the inverter levels. Since the dc duty cycle is between two boundary conditions, the performance is expected to be "in between" the effective output levels, and switching frequency. To better compare the inverter harmonic

performance the Total Harmonic Distortion (THD) is evaluated for several cases, using the first 100 harmonics:

$$THD = \frac{1}{V_1}\sqrt{\sum_{i=2,3,\ldots}^{100} V_i^2} \qquad (5\text{-}11)$$

The THD is evaluated for a converter with $n=3$, in 4 cases, by keeping the modulation index at maximum, $M = 1\text{-}d_{dc,x}$. The dc duty cycle $d_{dc,x}$ is increased by $0.1/n$ from $1/n$ to $1.5/n$:

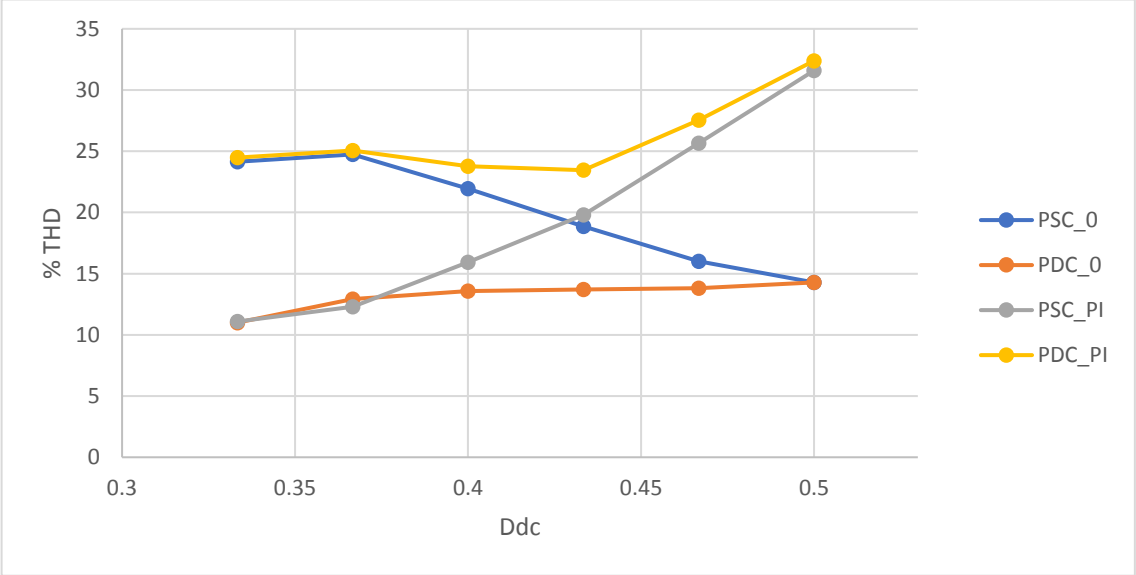

Figure 5-6 THD results at maximum modulation index, for PSC, $\vartheta_{carrier}$= 0°, PDC, $\vartheta_{carrier}$= 0°, PSC, $\vartheta_{carrier}$= 180°, PDC, $\vartheta_{carrier}$= 180°

At the two boundary conditions the THD is equal for PSC and PDC modulation, when $\vartheta_{carrier}$ takes opposite values. As $d_{dc,x}$ increases, the number of arm voltage levels goes down, causing harmonic distortion to increase. However, when $\vartheta_{carrier} = 0$ for the PSC modulation, THD decreases as the converter moves from $n_x \rightarrow n_{arm}$ to $n_x \rightarrow 2n_{arm} - 1$.

Overall, the BMCI can achieve a higher number of levels, than the buck MCC, for the same n. However, the waveform will not be as well-defined as a conventional multilevel inverter with the same number of levels. For example, a converter with $n=2$, operating with a voltage boost of 2, i.e. $d_{dc}=0.33$, can have between 4 and 7 voltage steps. The highest

number of voltage steps is achieved when $d_{dc} \to 0$, but this results in voltage gain $G_V \to \infty$ and input current $I_{dc} \to \infty$, which is impractical. Conventional non-isolated boost converters are designed for voltage gains between *2* and *5*, as is the experimental prototype used for validation.

The value of $d_{dc,x}$ can be chosen based on the required voltage gain:

$$d_{dc,x} = \frac{2\sqrt{2}V_{LL}}{V_{IN}} \qquad (5\text{-}12)$$

5.1.2. Inductance design

The inductor design for 2-level boost converters is a function of boost ratio, dc-side voltage, system power, and switching frequency. The process is simple, as under any steady-state condition, the inductor voltage has constant amplitude and frequency.

In a BMCI the inductor voltage varies over the cycle of the ac-side voltage waveform, in terms of both frequency and amplitude. For this reason, analysis is necessary to find the highest volt-seconds product, that will give the largest current ripple.

The converter's 6 inductances limit the arm current ripple and are necessary to achieve boost operations. As they carry dc current, the inductors need to have an air gap, or be made of low permeability material. In any case, the size and the weight of the inductor are proportional to the energy stored. The choice of inductance value is made by evaluating the maximum volt-seconds across the leg inductor, and the peak current ripple, $\Delta i_{dc,x}$:

$$\Delta i_{dc,x} = \frac{1}{L_{leg}} \max\left(\int_0^{T_{SWeff}} \left(v_{IN} - \left(\frac{v_{a,x} + v_{b,x}}{2} \right) \right) dt \right) \qquad (5\text{-}13)$$

As the dc-side voltage v_{dc} is a constant, the inductor volt-seconds are a function of the sum of the arm voltages. This is similar to the instantaneous phase voltage, and the phase shift angle $\vartheta_{carrier}$ also has to be taken into account.

5.1.2.1. Effects of $\theta_{carrier}$ on inductor voltage

Using the same arm voltage waveforms from Figure 5-4, the voltage $v_{dc,x}$ for $d_{dc,x}=1/n$ is shown in Figure 5-7:

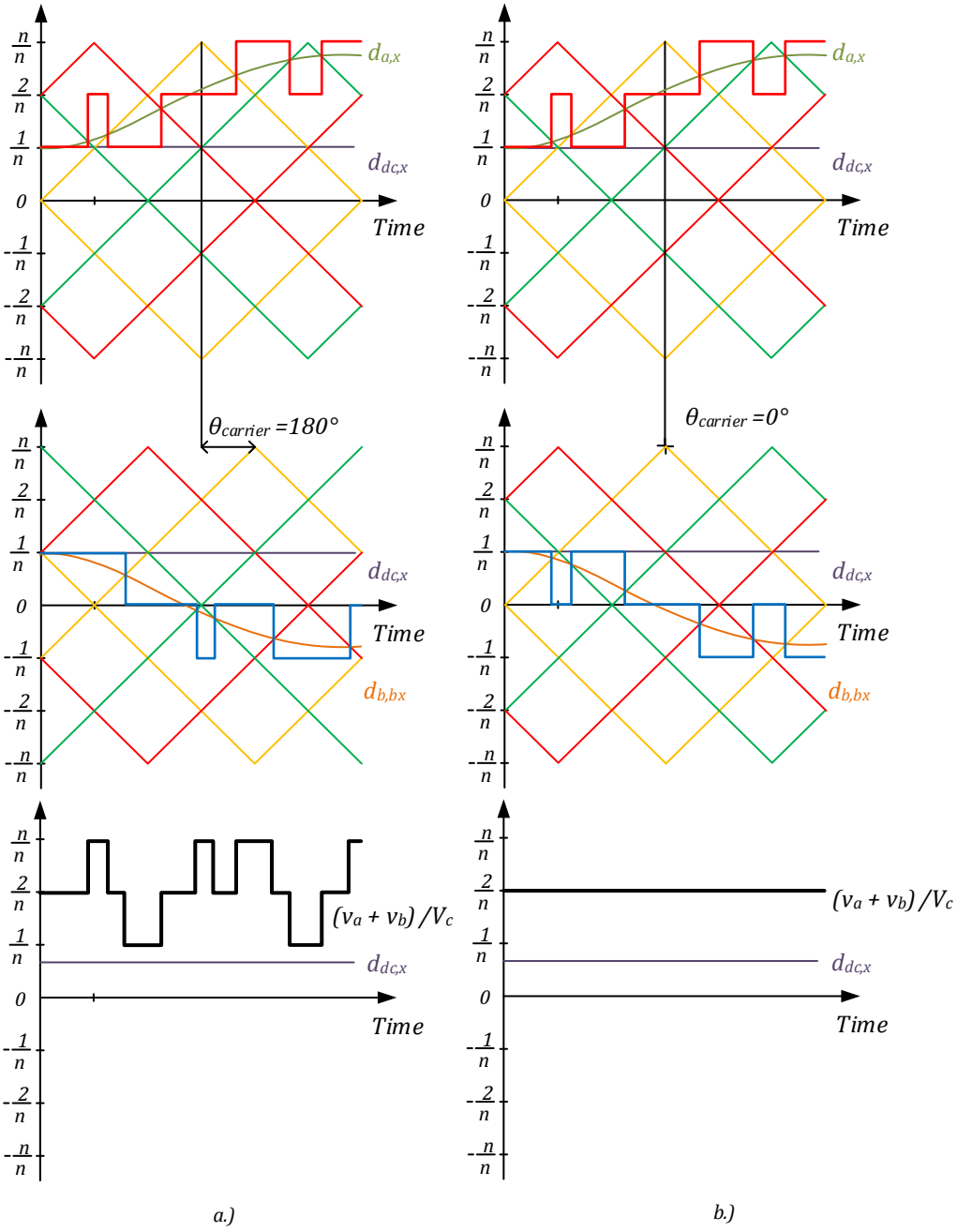

Figure 5-7 Instantaneous arm voltages and resultant sum for $\vartheta_{carrier} = 180°$ a.) and $\vartheta_{carrier} = 0°$ b.)

When $\vartheta_{carrier} = 0°$ the two waveforms are complementary and sum-up to a constant value, resulting in cancelation of the switching waveforms. With $\vartheta_{carrier} = 180°$ the summed dc voltage $v_{dc,x} = v_{a,x} + v_{b,x}$ is switching by voltage steps of $\pm V_C$ around the nominal point. These oscillations appear for both cases of $\vartheta_{carrier}$ when $d_{dc,x}$ is not divisible by $1/n$. The difference between the carrier angles is not as well defined for an example with $1/n < d_{dc,x} < 2/n$:

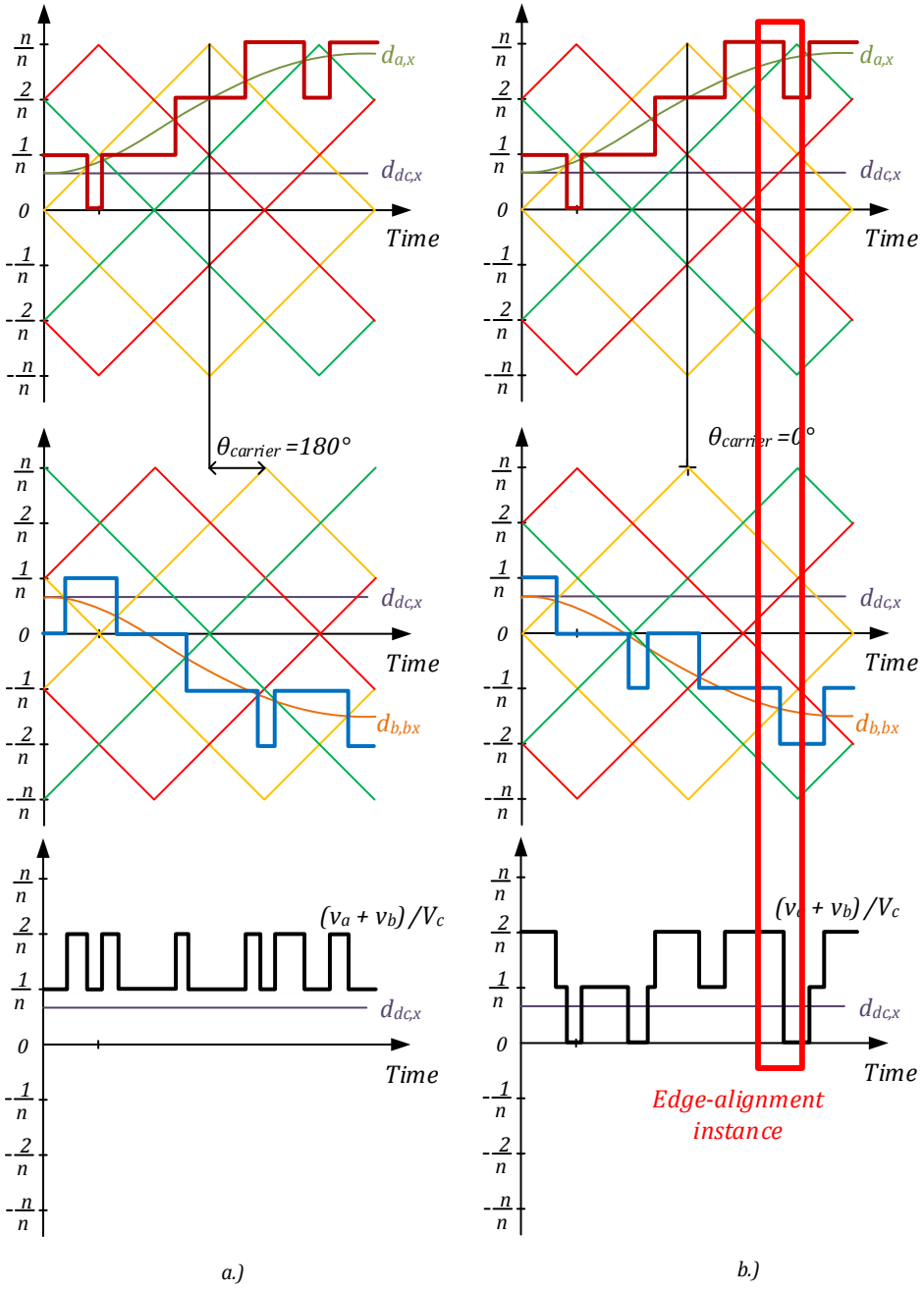

Figure 5-8 Arm and dc voltage waveforms with $0.5/n < d_{dc,x} < 1/n$, and $\vartheta_{carrier} = 180°$ a.) or $\vartheta_{carrier} = 0°$ b.)

The dc voltage now oscillates either between two levels, V_C/n and $2V_C/n$, or between 3 levels – 0, V_C/n, and $2V_C/n$. In Figure 5-8 b.) the point at which the top and bottom arm switching edges align has been highlighted, where the arms a and b's waveforms switch with the same polarity. The calculation of the exact volt-seconds product is difficult by observation and a simplified method is presented next.

5.1.2.2. Analysis of arm switching waveforms

In the examples so far, the ratio of effective switching frequency to modulated signal frequency, $k_f = 2\pi fsw/\omega$, has been kept low, so that the pulses are clearly visible. Under this condition, however, the local duty cycles do not pass through all possible values between 0 and 100%, due to the discrete nature of the modulation. The effect of utilising all possible duty cycles, is examined in Figure 5-9:

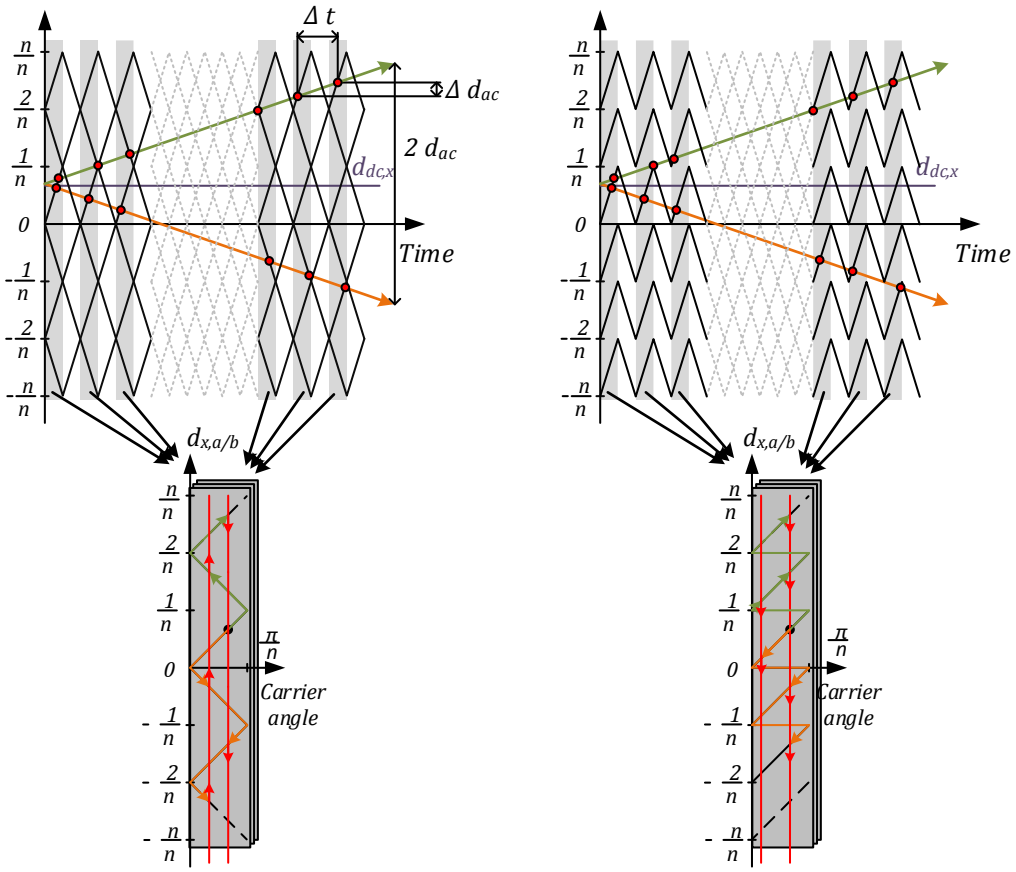

Figure 5-9 Construction of arm duty cycle trajectory for APOD (left) and PCD(right) modulation

By establishing that $k_F \to \infty$, the intersection between the modulation signals of arms a and b, and the respective local carrier, occur at time intervals $\Delta t \to 0$. By increasing the ac control signal $d_{ac,x}$ and overlaying the point of each leading edge in the effective switching period, the actual trajectories of the two arm duty cycles can be traced. When the arm a and b duty cycles align vertically, i.e. the switching edges occur at the same carrier angle,

either a summation or subtraction occurs. The direction of the switching edge is inferred from the slope of the local duty cycle: positive cycle (increasing with carrier angle) results in a falling edge, regardless polarity. A negative slope indicates a rising edge.

5.1.2.3. Peak inductor current for PSC and APOD modulation

In Figure 5-10 the effects of $d_{dc,x}$ and $\vartheta_{carrier}$ are shown in 4 particular cases: complete pulse cancellation in $v_{dc,x}$ for $\vartheta_{carrier}=0$, complete pulse cancellation for $\vartheta_{carrier}=180°$, edge coincidence for $\vartheta_{carrier}=0°$ and $\vartheta_{carrier}=180°$, with $0.5/n < d_{dc,x} < 1/n$:

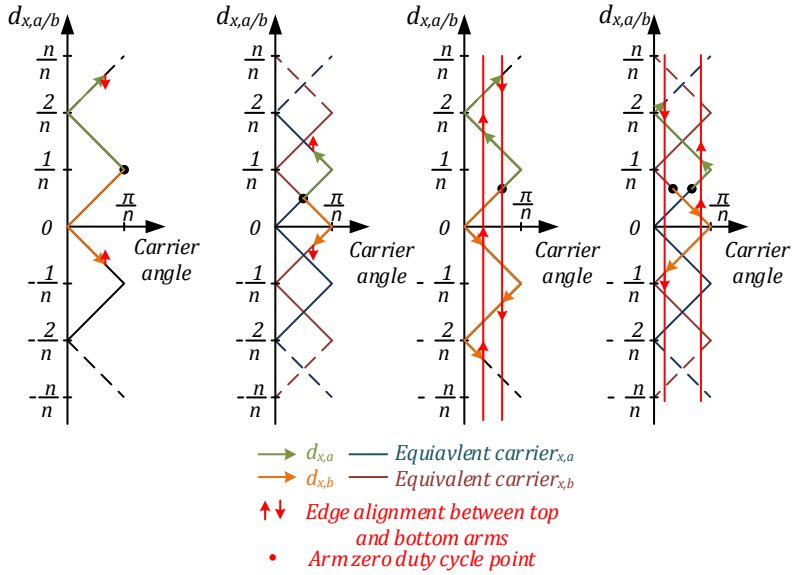

Figure 5-10 Duty cycle trajectories for PSC and APOD modulation

With $d_{dc,x}$ is not a multiple of $1/n$ or $0.5/n$, the pulse edges of the two converter arms only align once per increment of $d_{ac,x}$ by $1/n$. When the direction of the edges coincides, the resultant $v_{dc,x}$ pulse has twice the amplitude, i.e. $2V_C$, and a switching period of $T_{sw,eff}=1/f_{sw,eff}$. At other values of $d_{ac,x}$ the waveform of $v_{dc,x}$ switches either between 2 or 3 levels, but will have smaller volt-seconds product over a period of $T_{sw,eff}$. Using Figure 5-10, the duty cycle, at point of coincidence is:

$$\left.\begin{aligned} d_{coinc} &= nd_{dc,x} - floor(nd_{dc,x}), && \theta_{carrier} = 0^{\circ} \\ d_{coinc} &= nd_{dc,x} - round(nd_{dc,x}) + 0.5, && \theta_{carrier} = 180^{\circ}, d_{dc,x} > \frac{0.5}{n} \\ d_{coinc} &= \frac{d_{dc,x} + 0.5}{n}, && \theta_{carrier} = 180^{\circ}, d_{dc,x} < \frac{0.5}{n} \end{aligned}\right\} \quad (5\text{-}14)$$

As the arm local duty cycle repeats over every change by 1/n, the instantaneous inductor voltage duty cycle becomes only a function of the ac component of $v_{dc,x}$, with peak-to-peak value of either V_C or $2V_C$. The ripple current amplitude, at point of edge coincidence, is:

$$\Delta i_{dc,x} = \frac{1}{L_{leg}} d_{coinc}(1 - d_{coinc}) 2V_C T_{sw,arm} \quad (5\text{-}15)$$

5.1.2.4. Peak inductor current for PDC modulation

Similar observations can be made for the PDC scheme:

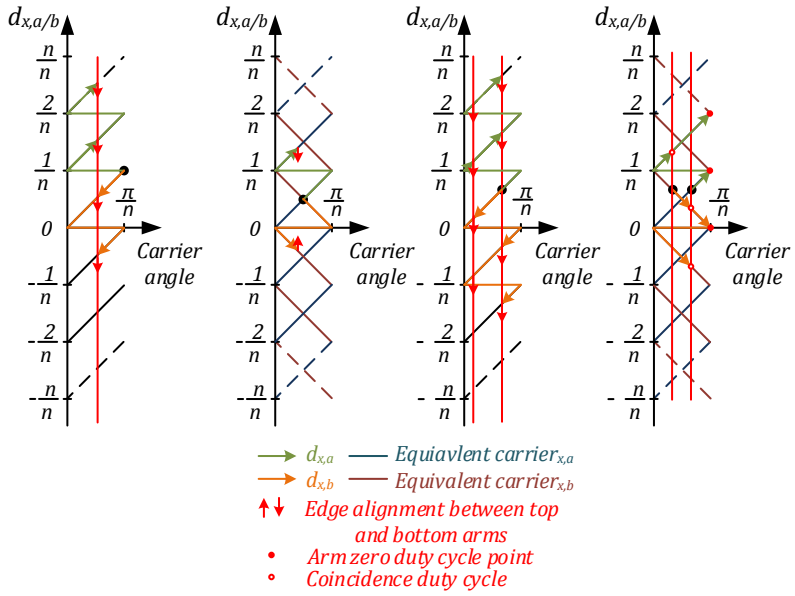

Figure 5-11 Duty cycle trajectories for PDC modulation

The key difference in the PDC case is that complete pulse cancellation only occurs when $\vartheta_{carrier}=180°$ as only that angle allows for symmetric switching actions for the two

arms. For $\vartheta_{carrier}=0$ there are pulse coincidences, resulting in pulses with amplitude of $2V_C$ twice per level. The peak current ripple will be caused by the higher of the two coincidence duty cycles. When $\vartheta_{carrier}= 180°$, and $d_{dc,x}$ is not divisive by $0.5/n$, there are no coincidences between the top and bottom arm pulses and the peak volt-seconds product will occur when one arm voltage has no pulsed component, while the other one still does. At these points the voltage step is equal to V_C, and the switching period is $T_{sw,eff}$. The duty cycles that causes the highest current ripple for the PDC case are:

$$\left.\begin{aligned} d_{coinc,1} &= nd_{dc,x} + 0.5 - floor(nd_{dc,x} + 0.5), && \theta_{carrier} = 0^\circ \\ d_{coinc,2} &= nd_{dc,x} - floor(nd_{dc,x}), && \theta_{carrier} = 0^\circ \\ d_{coinc} &= 2\left(nd_{dc,x} - floor(nd_{dc,x})\right) - 1, && \theta_{carrier} = 180^\circ, d_{dc,x} > \frac{0.5}{n} \\ d_{coinc} &= 2\left(nd_{dc,x} - floor(nd_{dc,x})\right), && \theta_{carrier} = 180^\circ, d_{dc,x} < \frac{0.5}{n} \end{aligned}\right\} \quad (5\text{-}16)$$

This results in the peak current ripple:

$$\left.\begin{aligned} \Delta i_{dc,x} &= \frac{1}{L_{leg}} 2V_C T_{sw,eff} \max\left(d_{coinc1}\left(1-d_{coinc1}\right), d_{coinc2}\left(1-d_{coinc2}\right)\right), && \theta_{carrier} = 0^\circ \\ \Delta i_{dc,x} &= \frac{1}{L_{leg}} d_{coinc}\left(1-d_{coinc}\right) V_C T_{sw,eff}, && \theta_{carrier} = 180^\circ \end{aligned}\right\} \quad (5\text{-}17)$$

5.1.2.5. Inductor voltage frequency spectrum

The design method proposed in this work chooses the inductance value based solely on the peak current ripple amplitude, over one modulation waveform cycle. Another important aspect is the frequency spectrum of the converter current, as this has direct effect on the electro-magnetic interference (EMI) filters required for a finished product.

The frequency spectrum of the circulating current, of one phase leg, is examined through an example, using the following converter parameters:

Table 5-2 Converter parameters for evaluation of circulating current spectrum

Parameter	**Value:**
L_{Leg}	100uH
f_{sw}	1kHz
$\vartheta_{carrier}$	*0°, 180°*
V_C	300V
n	3
$d_{dc,x}$	0.45
Voltage boost ratio	2

The dc current level is removed to accentuate the spectrum of the ac components. The case for $\vartheta_{carrier} = 0°$ is shown in Figure 5-12:

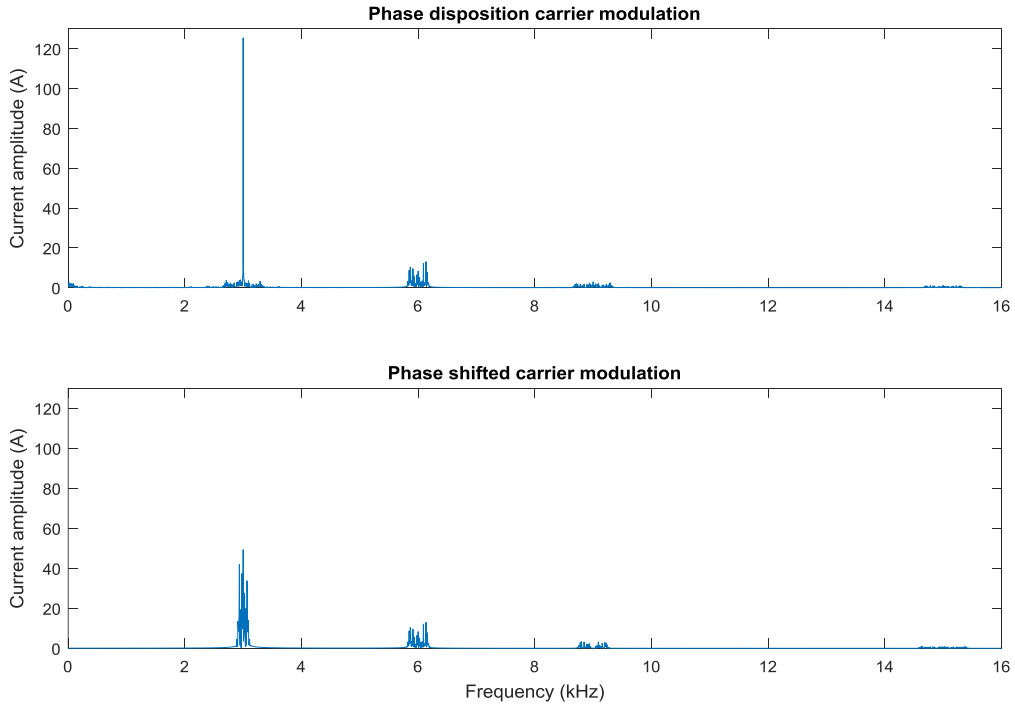

Figure 5-12 Circulating current spectrum for PSC and PDC modulation, $\vartheta_{carrier} = 0°$

The spectrum of the PDC case has a very strong component at the arm effective switching frequency $f_{sw,eff}$. For PSC modulation, the harmonics with the highest amplitude are also at same frequency, but with lower value. The lower ripple for the PDC case is also reflected in the calculating peak current ripple, using (5-15) and (5-17). The results are 355A for the PSC case, and 370A for the PDC one. This ripple amplitude values are very similar, and even though the peak amplitude of the PSC case is higher, the PDC scheme's highest harmonic is much larger.

By changing $\vartheta_{carrier}$ to $180°$ it is expected that the current ripple will reduce, as $d_{dc,x}$ is closer to $1/n$ than $0.5/n$:

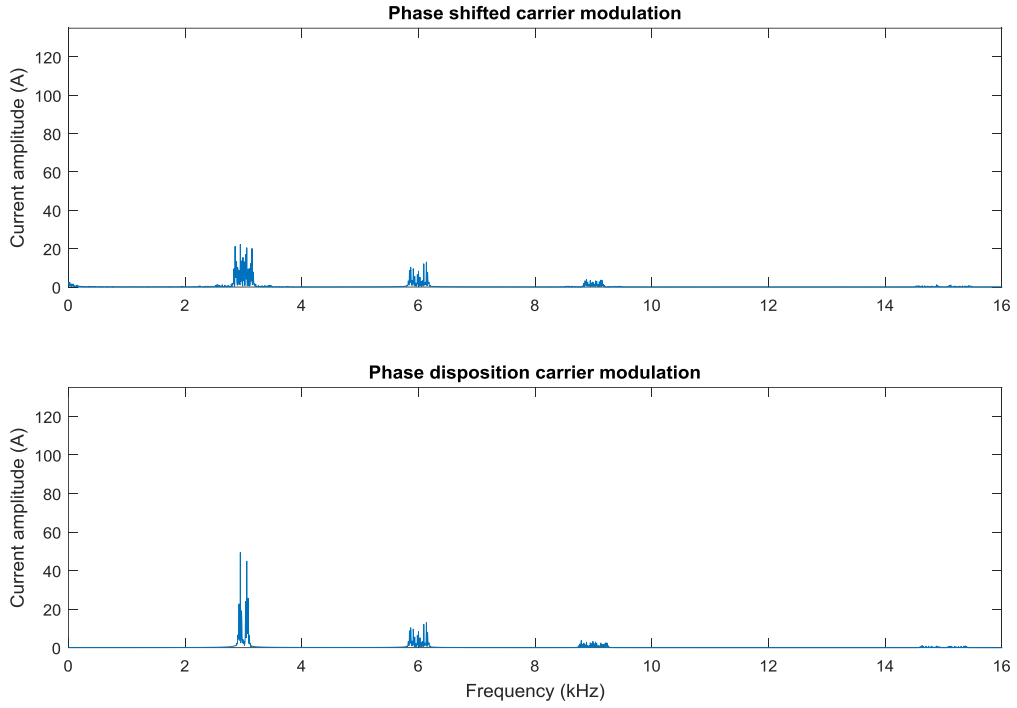

Figure 5-13 Circulating current spectrum for PSC and PDC modulation, $\vartheta_{carrier} = 180°$

The peak current ripple calculated is 355A for the PDC case and 258A for the PSC scheme. Like the previous case, the scheme with the lower harmonic amplitude has the higher peak current ripple, but the second harmonic, of the arm effective frequency, is identical.

Even though the peak current ripple for PDC modulation with $\vartheta_{carrier} = 180°$, is as high as the $\vartheta_{carrier} = 0°$ case, the harmonic spectrum is less populated, and would consequently be easier to filter.

5.1.2.6. Physical design of leg inductors

The physical design of the leg inductors is based on the total energy stored in them. The inductor energy is dependent on the peak arm current, which is:

$$W_{L,leg} = \frac{L\left(\max\left(i_{a/b,x}\right)\right)^2}{2} \qquad (5\text{-}18)$$

Individual leg inductors increase the BMCI's output inductance. However, a traction motor has a relatively high leakage inductance, and any additional phase inductance is undesirable.

If each pair of leg inductors are lumped into a single centre-tapped inductor, with high coupling factor between the two windings, both inductor energy and output inductance can be lowered, as the magnetic flux established in the core will be only due to the dc component of the current. The ac components create effectively cancel out. The size of the coupled inductor only depends on the peak circulating current $i_{dc,x}$, and is not affected by the ac output current $i_{ac,x}$. The two possible inductor configurations are shown below:

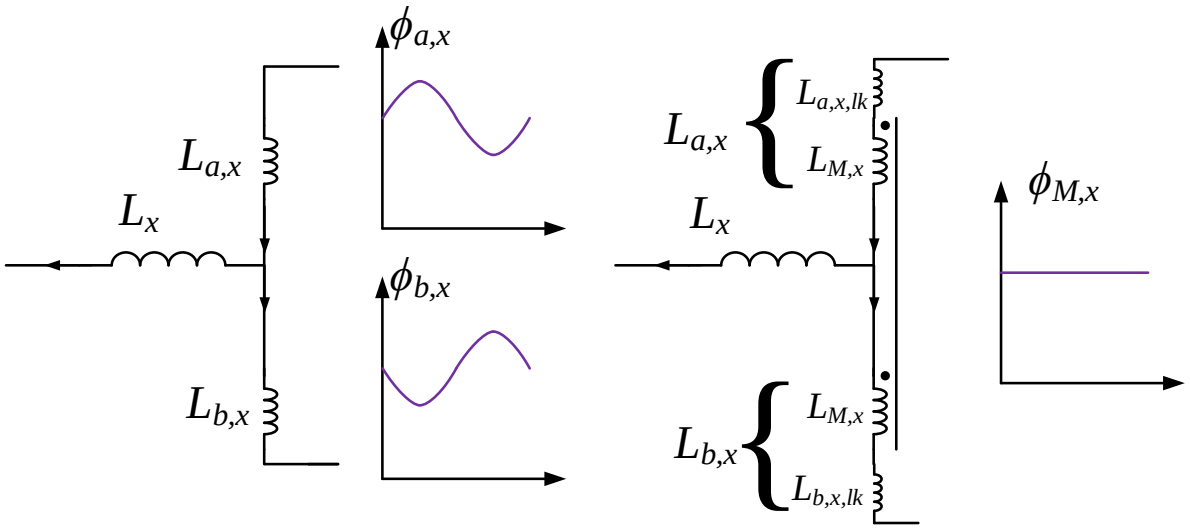

Figure 5-14 Circuit and core flux for two separate leg inductors (left) and a single centre-tapped inductor (right)

In the case of the centre-tapped inductor, the two windings will not have a unity coupling factor and there will be some leakage flux for each one. This is accounted for by the leakage inductance, $L_{a/b,x,lk}$, which however does not influence energy stored in the core air gap. It does appear, however at the output of the converter as $L_{out,x}$ and is added to L_x to form the total line inductance.

For the two separate leg inductors case, the values are calculated by using:

$$L_{a,x} = L_{b,x} = \frac{L_{leg}}{2} \tag{5-19}$$

$$W_{L,x,\max} = 2 \times \frac{L_{a/b,x}}{2} \left(I_{dc,x} + \frac{I_{ac,x}}{2} \right)^2 \tag{5-20}$$

$$L_{out,x} = \frac{L_{a/b,x}}{2} \tag{5-21}$$

For the single centre-tapped inductor, the value of the magnetizing inductance L_M, i.e. the open circuit inductance of one winding, is calculated from:

$$L_{M,x} \approx \frac{L_{leg}}{4} \tag{5-22}$$

$$W_{L,x,\max} = \frac{4L_{M,x}}{2} I_{dc,x}^{\ 2} \tag{5-23}$$

$$L_{out,x} = \frac{L_{a/b,x,lk}}{2} \tag{5-24}$$

The magnetizing inductance $L_{M,x}$ should be slightly smaller than the value calculated in (5-22), as the leakage inductances are added to the total leg inductance.

5.1.3. Capacitor design

Energy stored in each arm depends on $v_{dc,x}$, v_x, fundamental load frequency ω , voltage boost ratio $G_{V,dc}$, and instantaneous arm powers $p_{x,a}$ and $p_{x,b}$. The converter voltage gain is controlled by the dc duty cycle $d_{dc,x}$. The steady-state output conditions of the BMCI are:

$$v_x(t) = V_x \sin(\omega t) = m\,(1-d_{dc,x}) \times n\, v_C \times \sin(\omega t) \tag{5-25}$$

$$v_{dc,x}(t) = V_{dc} = 2 d_{dc,x} n\, V_C \tag{5-26}$$

$$i_x(t) = I_x \sin\left(\omega t - \varphi\right) \tag{5-27}$$

, where m is the modulation index, φ is the current displacement angle, and I_x is the magnitude of the output current. The design parameters are the total arm capacitance C_{arm}, the capacitor voltage $V_{Cx,a/b}$, and the total arm energy, which are given by the following equations:

$$C_{arm} = \frac{C}{n} \tag{5-28}$$

$$V_{Cx,a/b} = nV_{C,nom} \tag{5-29}$$

$$w_{x,a/b} = \frac{1}{2} C_{arm} v(t)^2_{Cx,a/b,i} \tag{5-30}$$

Since the output power is pulsating at the load frequency, the stored arm energy varies over one cycle, with peak fluctuation, Δw_c, causing a voltage ripple of $\Delta V_{Cx,a/b}$ on top of the average dc voltage:

$$\begin{aligned} \Delta w_{x,a/b} &= \frac{1}{2} C_{arm} \left[\left(V_{Cx,a/b} + 0.5\Delta v_{Cx,a/b} \right)^2 - \left(V_{Cx,a/b} - 0.5\Delta v_{Cx,a/b} \right)^2 \right] \\ &= 4\, C_{arm}\, V_{Cx,a/b}\, \Delta v_{Cx,a/b} \end{aligned} \tag{5-31}$$

From (5-31) the minimum capacitance, for achieving a certain ripple, becomes:

$$C_{arm} \geq \frac{\Delta w_{x,a/b}}{4\Delta v_{Cx,a/b} \times V_{Cx,a/b}} \tag{5-32}$$

The peak energy fluctuation can be found by integrating the instantaneous arm power:

$$\Delta w_{x,a/b} = \max\left(\int_0^T p_{x,a/b}(t) dt \right) - \min\left(\int_0^T p_{x,a/b}(t) dt \right) \tag{5-33}$$

, where the instantaneous arm power can be obtained from the arm voltages and currents:

$$v_{x,a/b}(t) = \frac{V_{IN}}{2} \mp V_x \sin(\omega t) = d_{dc,x} n V_C \tag{5-34}$$

$$i_{x,a/b}(t) = I_{dc,x} \pm \frac{I_x}{2} \sin(\omega t - \phi) \tag{5-35}$$

$$\begin{aligned} p_{x,a/b}(t) &= \left[\frac{V_{dc,x}}{2} \mp V_x \sin(\omega t) \right] \times \left[I_{dc,x} \pm \frac{I_x}{2} \sin(\omega t - \varphi) \right] \\ &= \underbrace{\frac{V_{dc,x} I_{dc,x}}{2}}_{0.5P_{dc,x}} \pm \frac{V_{dc,x} I_x \sin(\omega t - \varphi)}{4} \mp V_x I_{dc,x} \sin(\omega t) \\ &\quad \underbrace{- \frac{V_x I_x}{4} \cos(\varphi)}_{0.5P_{ac,x}} + \frac{V_x I_x}{4} \cos(2\omega t - \varphi) \end{aligned} \tag{5-36}$$

According to (5-36), the top and bottom arm powers differ in the oscillating components, that are in counter phase. Thus, only the top arm power is used for the following the analysis. The arm power contains two dc-components and 2 oscillatory components - at the fundamental and twice the fundamental frequency. The only difference between arms *a* and *b* is the phase of the fundamental component and further analysis will only examine the power of one converter arm. Over time the net capacitor power must be 0, and by using $P_{ac,x} = P_{ac,x}$, the arm power can be reduced to:

$$p_{x,a}(t) = \pm \frac{V_{dc,x} I_x \sin(\omega t - \phi)}{4} \mp V_x I_{dc,x} \sin(\omega t) + \frac{V_x I_x}{4} \cos(2\omega t - \phi) \tag{5-37}$$

The dc and phase voltage amplitudes in each arm are produced by the converter's capacitor voltages. Substituting with (5-25) - (5-27) in (5-37), the arm power can be made a function of the average capacitor voltage, the dc duty cycle $d_{dc,x}$, and the modulation index *m*:

$$p_{x,a}(t)=\frac{d_{dc,x}\times n\,V_C\;I_x}{2}\sin(\omega t-\varphi)-m^2\frac{\left(1-d_{dc,x}\right)^2}{2d_{circ,x}}\times n\,V_C I_x\cos(\varphi)\sin(\omega t)+ \\ +\frac{m\left(1-d_{circ,x}\right)\times n\,v_C I_x}{4}\cos(2\omega t-\varphi) \tag{5-38}$$

Additionally, by defining the apparent power S_{OUT} and the voltage boost ratio as:

$$\begin{cases} S_{OUT,x}=V_{x,rms}\times I_{x,rms}=\dfrac{m\,(1-d_{dc,x})\times n\,v_C}{\sqrt{2}}\times\dfrac{I_x}{\sqrt{2}} \\ G_{V,dc}=\dfrac{1-d_{circ,x}}{d_{circ,x}} \end{cases} \tag{5-39}$$

, equation (5-36) becomes:

$$p_{x,a}(t)=\frac{S_{OUT,x}}{MG_{V,dc}}\sin(\omega t-\varphi)-m\,S_{OUT,x}G_{V,dc}\cos(\varphi)\sin(\omega t) \\ +\frac{S_{OUT,x}}{2}\cos(2\omega t-\varphi) \tag{5-40}$$

There are two power components in(5-40), that can be denoted as $S_{1,x}$, with phase $\phi_{1,x}$, and $S_{2,x}$, with phase $\phi_{2,x}$:

$$\begin{cases} S_{1,x}=\sqrt{\left[\dfrac{S_{OUT,x}\cos(\varphi)\left(1-mG_{V,dc}^2\right)}{mG_{V,dc}}\right]^2+\left[\dfrac{S_{OUT,x}}{mG_{V,dc}}\sin(\varphi)\right]^2} \\ \varphi_{1,x}=\tan^{-1}\left[\dfrac{\sin(\varphi)}{\cos(\varphi)\left(1-mG_{V,dc}^2\right)}\right]=\tan^{-1}\left[\dfrac{\tan\left(\varphi\right)}{1-mG_{V,dc}^2}\right] \end{cases} \tag{5-41}$$

$$\begin{cases} S_{2,x}=\dfrac{S_{OUT,x}}{2} \\ \varphi_{2,x}=\varphi \end{cases} \tag{5-42}$$

Substituting (5-40) - (5-42) into (5-33), the peak energy fluctuation for arm *a* becomes:

$$\Delta w_{x,a} = \max\left[-\frac{S_{1,x}}{\omega}\cos\left(\omega t-\varphi_{1,x}\right)+\frac{S_{2,x}}{2\omega}\sin\left(2\omega t-\varphi_{2,x}\right)\right] - \min\left[-\frac{S_{1,x}}{\omega}\cos\left(\omega t-\varphi_{1,x}\right)+\frac{S_{2,x}}{2\omega}\sin\left(2\omega t-\varphi_{2,x}\right)\right] \quad (5\text{-}43)$$

Evaluating the peak arm energy, for a given frequency can now give an arm capacitance value by substituting (5-43) in (5-32). For a traction converter, the submodule capacitance should be designed according to the peak energy fluctuation over the full speed range of the converter, including field weakening, where the converter is operating at constant output power. This can be achieved by ramping output frequency, output power, and dc-gain up to base speed, and then keeping power and voltage gain constant, while increasing frequency, simulating the constant torque and power regions:

$$C \geq n \times \frac{\max\left[\Delta w_{x,a/b}\left(S_x(\omega), G_{V,dc}(\omega), \omega, \phi\right)\right]}{4\Delta v_{Cx,a/b} \times V_{Cx,a/b}} \quad (5\text{-}44)$$

As an example, the peak energy fluctuation was evaluated for a laboratory prototype, using the parameters in Table 5-3:

Table 5-3 Design parameters for experimental converter

Converter apparent power amplitude	$\lvert S_x \rvert$	
Power factor	cosϕ	0.74
Maximum voltage gain	$G_{V,dc}$	5
Base frequency	f_{base}	25 Hz

The converter arm energy fluctuation is simulated and a surface plot of the resulting peak-to-peak ripple, as a function of output frequency and power factor, can be seen in Figure 5-15.

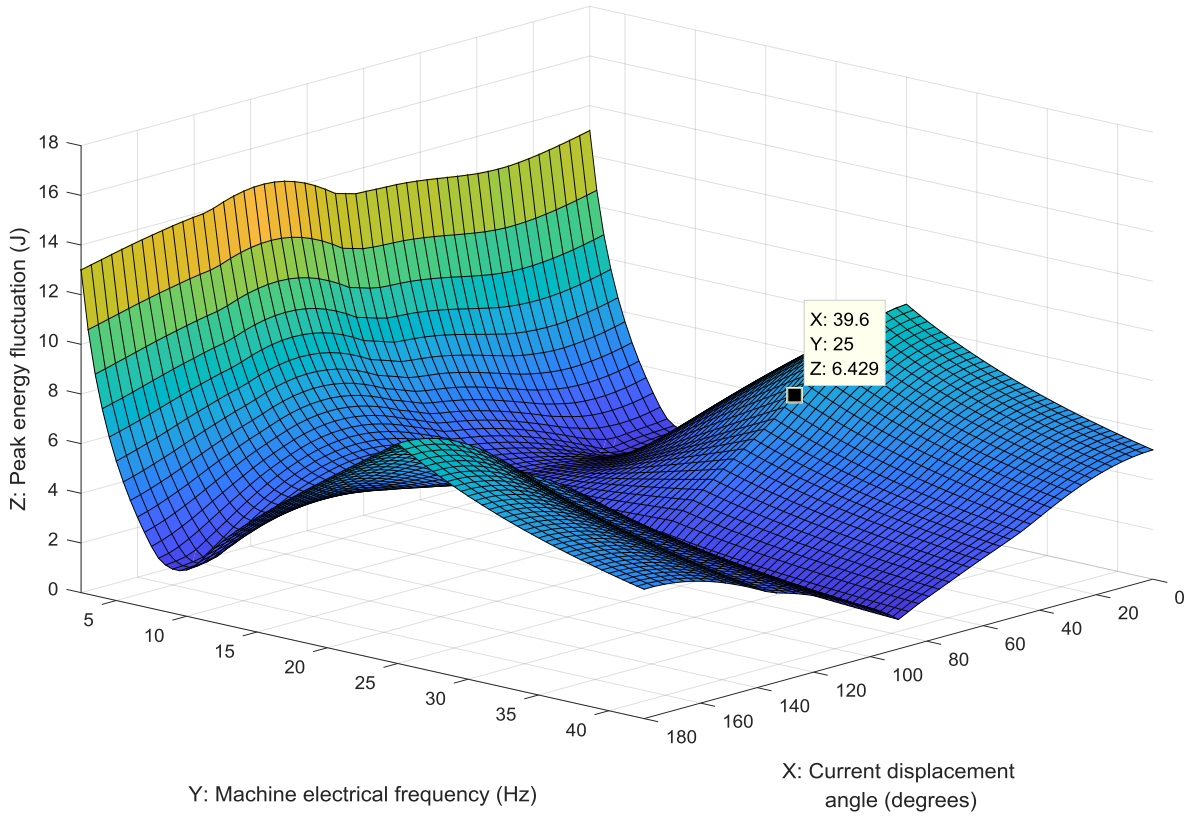

Figure 5-15 Sub-module arm energy fluctuation for experimental prototype converter, with value at the converter's operating point

The peak energy demand is close to 0 Hz output as capacitors cannot carry a dc current. However, the ripple-reduction control system can provide full compensation at low frequency, and now the peak energy demand can be shifted to the chosen base machine speed. Thus, the converter capacitance can be designed according to:

$$C \geq n \frac{\max\left[\Delta w_{x,a/b}\left(S_x\left(2\pi f_{base}\right), G_{V,dc}\left(2\pi f_{base}\right), 2\pi f_{base}, \phi\right)\right]}{4\Delta v_{Cx,a/b} \times V_{Cx,a/b}} \qquad (5\text{-}45)$$

It is important to note in (5-31) that the capacitor voltage ripple is defined to be symmetrical around the nominal operating point. In practice due to the second harmonic in the arm power fluctuation, (5-40), the nominal capacitor will be in the range defined in (5-31), but with an error from the desired average voltage V_C. This error has been shown to be small during motoring operation in [154], with current displacement angles

between 0 and π/2. Thus, the method presented in this paper is valid for the design of the capacitance.

5.2. ELECTRONICS DESIGN OF PROTOTYPE CONVERTER

The general structure of the converter is divided in 3 sections – master controller, routing section, and power circuit, consisting of the power sub-modules, floating capacitors and power inductors. A high-level schematic of the converter power stage can be seen in Figure 5-16.

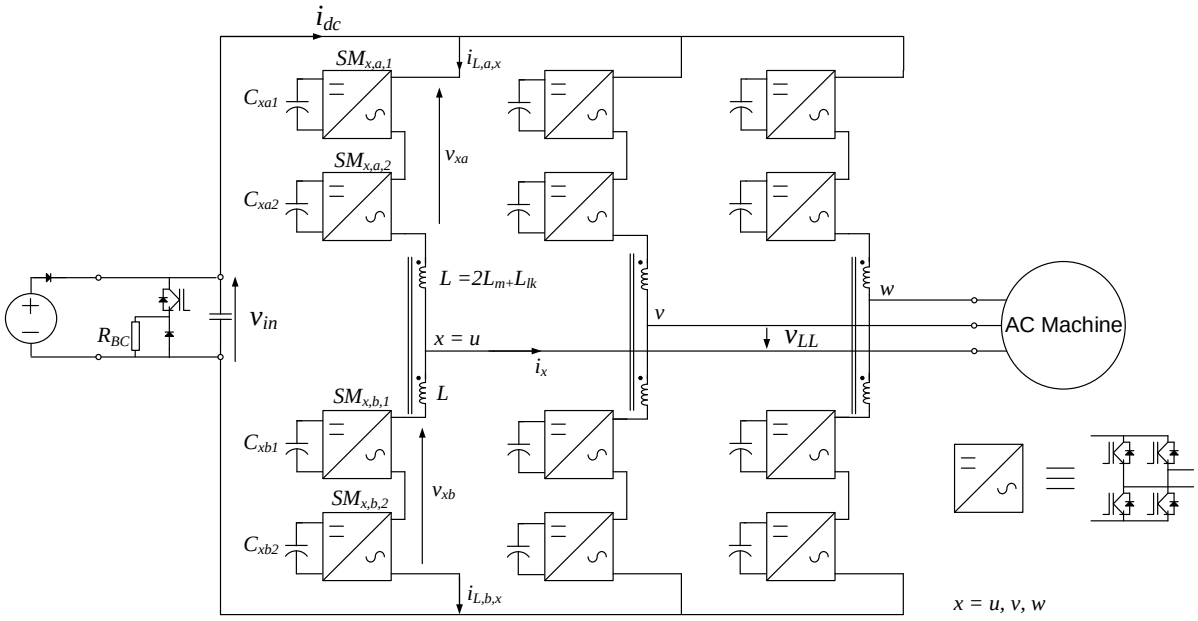

Figure 5-16 High level diagram of prototype converter

The leg inductors are magnetically coupled and connected in such a way as to maximize the inductance seen by the circulating current and minimize the converter's output inductance. The parameters of the components, and the test setup, are summarised in Table 5-4.

Table 5-4 Main parameters of the components of the prototype MCC

Parameter	Symbol	Value
Total leg inductance (measured at 20kHz, ΔV_L=100V)	L_{leg}	1.3mH
Leakage inductance, per winding	L_{lk}	150µH
Magnetizing inductance	L_M	250µH
Sub-module capacitance	C_{SM}	2.2mF
IGBT module rated current	$I_{C,nom}$	50A
IGBT rated voltage	V_{CE}	650V
Supply voltage range	V_{in}	0 – 60V
Output line-to-line voltage range	$V_{line\text{-}to\text{-}line,peak}$	0 – 250V
Device switching frequency	f_{sw}	5kHz

5.2.1. Design of converter sub-module

One of the design goals is to have flexibility in the converter so that only few hardware changes would be needed if more functionality was required. Each sub-module assembly consists of two parts – power PCB and control PCB. The power PCB carries the power transistors, floating capacitor, gate driver circuits, isolated driver power supplies, and the isolated voltage transducer, used for feedback.

The sub-module was designed with 3 transistor legs, so that an energy source can be connected to one leg, while the other two are part of the BMIC. This source can be either a low-voltage battery or supercapacitor module and an inductor will be required to achieve boost operation. The basic diagram is shown in Figure 5-17:

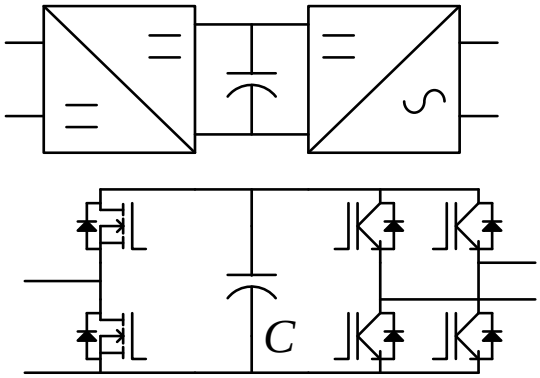

Figure 5-17 Prototype sub-module high-level diagram

The main transistor bridge, that is part of the BMCI, uses a quad IGBT module from POWERX, supplied by Mitsubishi Corp., that is a partner on this project. While the transistors might be considered oversized for a small laboratory prototype, they are housed in a robust package and facilitate PCB and heat-sink mounting. A single sub-module can be seen in Figure 5-18.

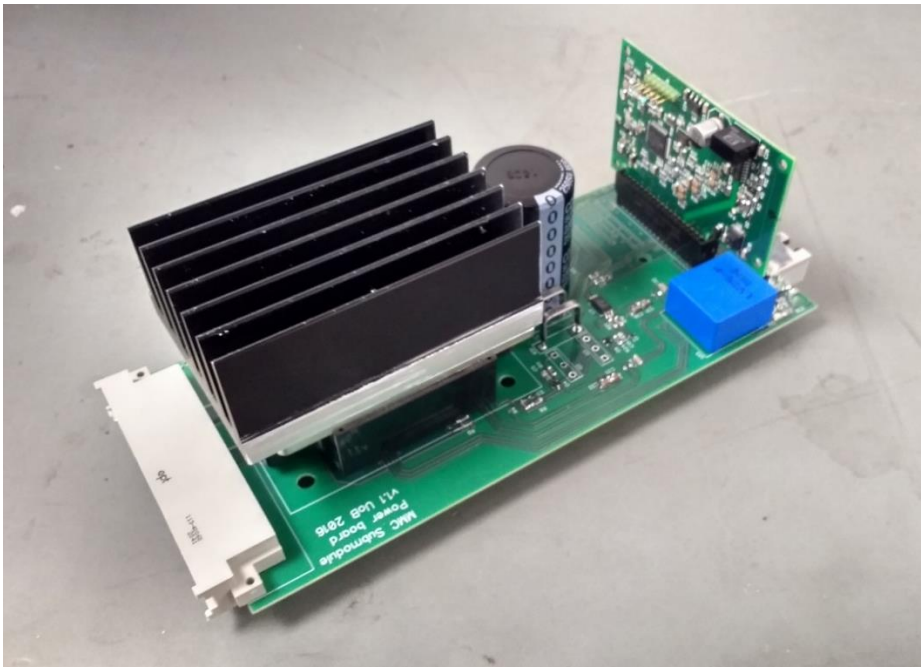

Figure 5-18 Single converter sub-module showing power PCB with IGBT power module and control card with microcontroller. The MOSFET leg is not mounted on the PCB.

5.2.1.1. Gate driver design

Each power transistor gate is controlled by an isolated gate driver, with a high current output, part number Si8261-BAD. The chip uses a modulated RF-carrier for signal transmission over the isolation barrier. The gate driver can source 1.8A peak, and sink 4A peak current, which makes them well suited to driving large capacitive loads. The IGBT module used is not a latest generation device and it has a relatively large total input capacitance of 6.6nF, with reverse transfer capacitance of 1nF at 10V collector-emitter voltage. To avoid any Miller turn-on, the converter uses a bipolar gate drive, producing a ±15V gate-emitter signal. The gate driver includes the option for an external capacitor to be connected across the gate terminals. This can be used if additional reduction of Miller current effects. To protect the IGBTs, a pair of Zener diodes is also connected in parallel with each gate, clamping the voltage to roughly ±(15V + 0.7V).

The gate driver's internal MOS transistors have typical internal resistance of $R_L = 0.8\Omega$ for sinking, and $R_H = 2.6\Omega$ for sourcing, current. To ensure reliable operation the peak

output current of the gate driver must be limited to the rated value. This can be done by analysing the circuit in Figure 5-19:

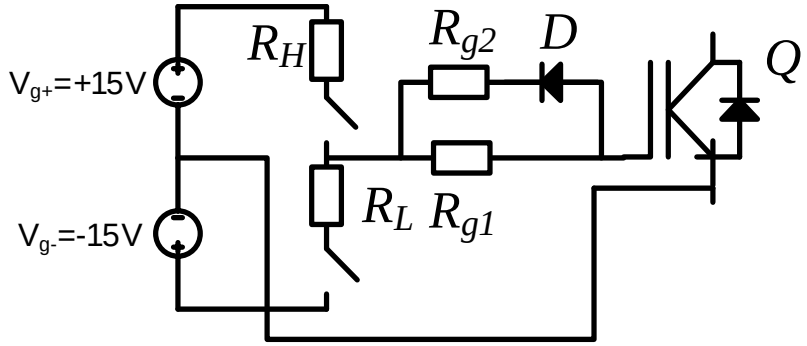

Figure 5-19 Equivalent circuit of IGBT gate driver

The peak turn-on current is determined by selecting the value of R_{g1}. With a bipolar gate drive, the IGBT input capacitance will be charged from -15V to +15, making the initial voltage across R_{g1} and R_H equal to 30V:

$$R_{g1} \geq \frac{V_{g+} - V_{g-}}{I_{H,peak}} - R_H = \frac{30V}{1.8A} - 2.6\Omega = 14.066\Omega \qquad (5\text{-}46)$$

During turn-off the gate driver has to sink both the gate current as well as the Miller capacitor current that is caused by the high dv/dt seen by the gate-collector junction. To fully utilise the gate driver's sinking current capability, the turn-off gate resistance can be lowered by introducing R_{g2} and a series diode. This makes the turn-off gate resistance equal to the parallel combination of R_{g1} and R_{g2}:

$$R_{g1} \| R_{g2} \geq \frac{V_{g+} - V_{g-}}{I_{L,peak}} - R_L = \frac{30V}{4A} - 0.8\Omega = 6.7\Omega \qquad (5\text{-}47)$$

By choosing Rg1 and Rg2 both equal to 15Ω the turn-on and turn-off currents are limited to 1.705A and 3.614A, respectively. The schematic of the gate driver circuit used

can be seen in figure 5-20:

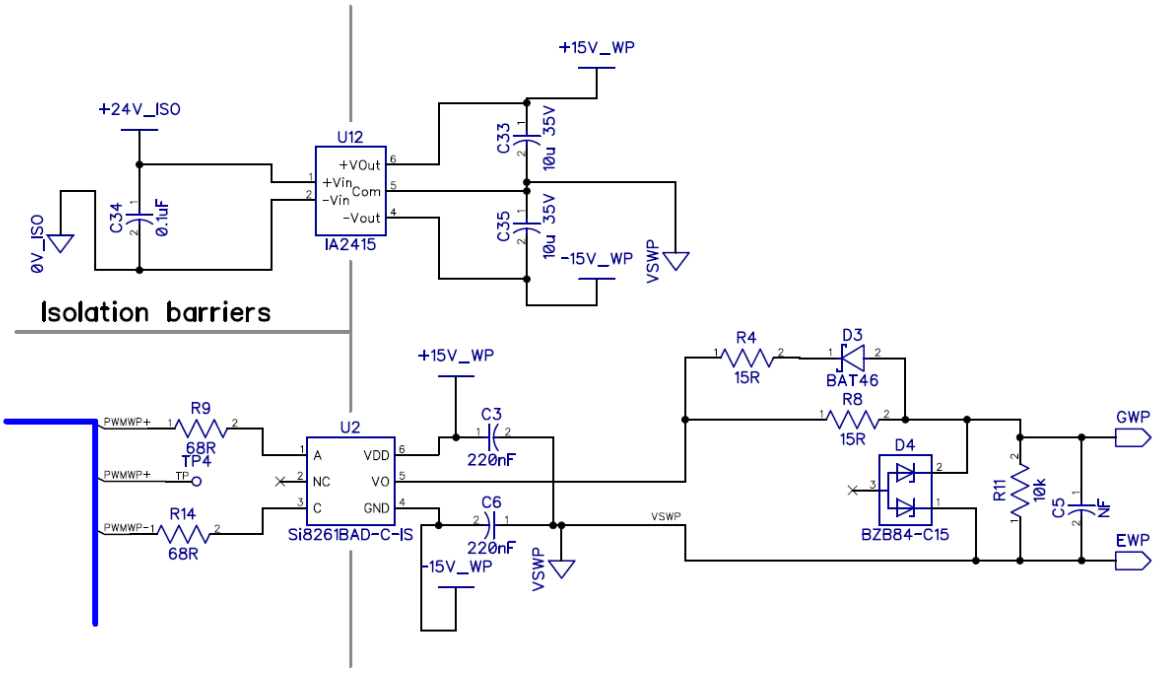

Figure 5-20 Isolated bipolar gate driver with separately isolated power supply

5.2.1.2. Control card design

The BMCI prototype was designed with future work in mind. One of these project uses a supercapacitor energy storage element, interfaced via a boost converter. When in use this boost converter must regulate the sub-module capacitor voltage, monitor supercapacitor voltage, and introduce limits to the energy storage element's current. This functionality requires two voltage sensors and one current sensor. To reduce the number of signals measured by the high-level master controller, which would require isolation, a control PCB card was designed. This card also has an isolation barrier, realised by using a 4-channel digital isolator, which has a much lower cost than an isolated voltage or current transducer. The control card is fitted with a *dsPIC33EP512GM604* digital signal controller (DSC), with up to 8 PWM outputs,4 integrated operational amplifiers (op-amps), and 12 analogue inputs.

The 4 digital isolator channels are connected to 4 PWM outputs of the DSC and, when the control card is inserted in the power board, to the isolated gate driver input, as shown in Figure 5-21:

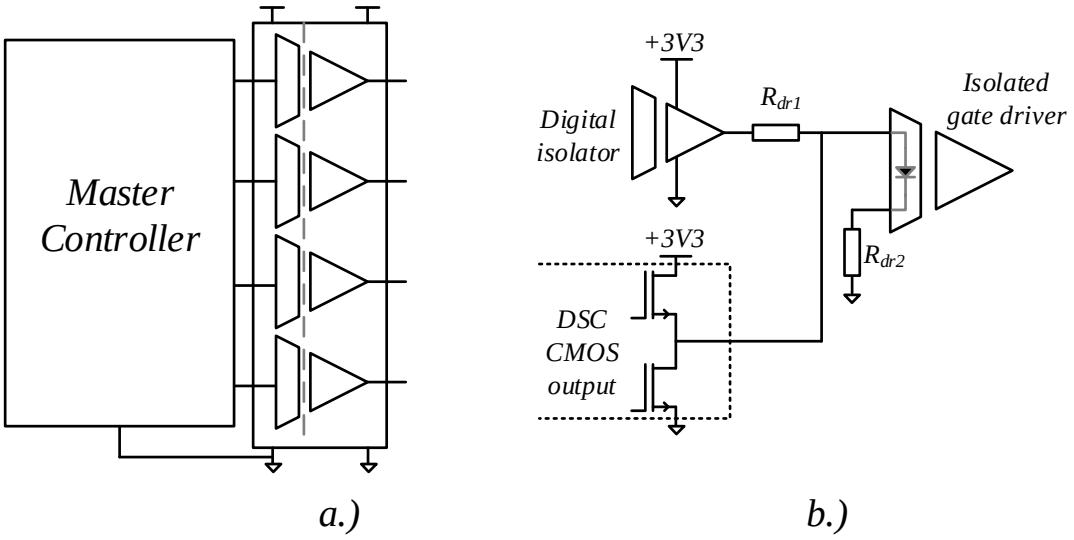

Figure 5-21 Digital isolators a.) and drive of gate driver input b.)

The DSC output can be configured either as a normal CMOS output, an open-drain output, or disabled. When configured as a normal output, the DSC controls the gate driver, with its input current limited by R_{dr2}. When configured as an open drain, the top transistor in the output stage is disabled, and R_{dr1} functions as a pull-up resistor. In this state the DSC output functions as an *enable* signal. Both modes can be used to bypass the master controller output in case of a fault, e.g. output short circuit or sub-module overvoltage.

To measure the sub-module currents 2 of the internal op-amps are configured in a difference amplifier configuration. This circuit measures the voltage across a 5mΩ current sensing resistor, v_{Rsense}, and produces a voltage v_{ADC}, centred around +1.5V. The transfer characteristics of the amplifier, with $R_1 = R_4$, and $R_2 = R_5$, are:

$$v_{ADC} = 1.5V + \frac{R_2}{R_1} v_{Rsense} \qquad (5\text{-}48)$$

To reduce the effects of the parasitic inductance of the current sensing resistor, and to reduce circuit noise, the amplifier is fed by a low-resistance common-mode and differential-mode filter. The circuit of the amplifier can be seen in Figure 5-22:

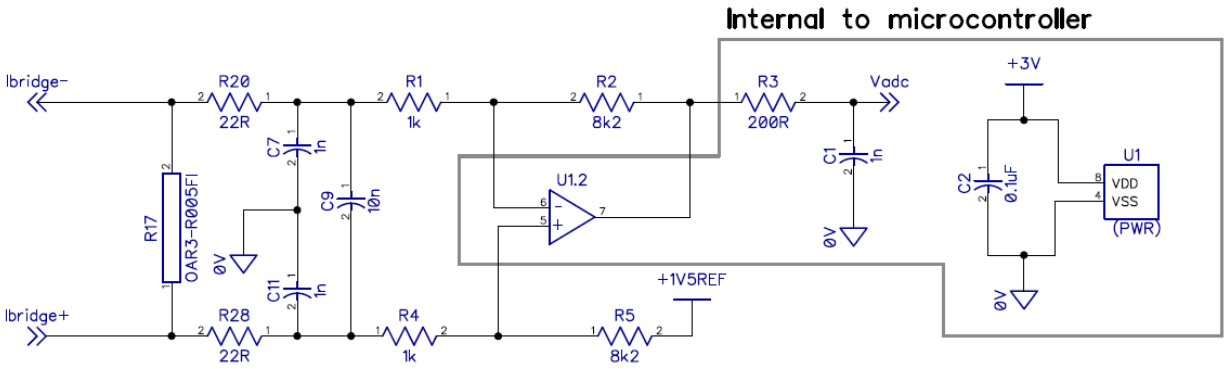

Figure 5-22 Difference amplifier circuit with current sensing resistor R17

The voltage sensing amplifiers use a conventional voltage-follower op-amp configuration and can only measure a positive voltage.

5.2.2. Current sensor card design

The control system requires 6 current measurements – one for each arm. The laboratory prototype uses isolated closed-loop current transducers, part number *LA25-NP*. Each sensor is configured with 3 primary turns, giving a measurement range of ±12A. The sensor functions as an ideal current transformer, with *dc* to *100kHz* bandwidth, and transfer ratio of *3:1000.* The sensor is powered by a ±15V isolated power supply and can produce an output voltage in the range of ±6.48V when loaded by a 180Ω load resistor.

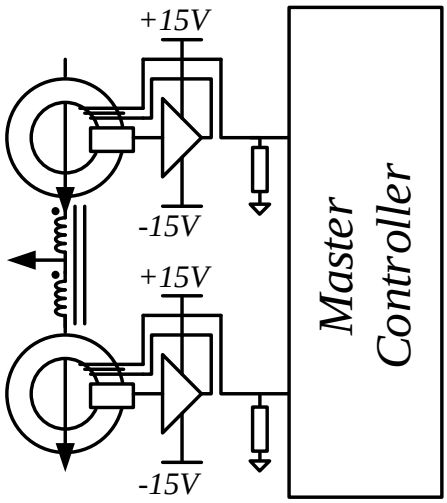

Figure 5-23 Current sensor design and placement with leg inductor

5.2.3. Routing card design

To manage all the connections between the master controller, the 12 sub-modules, and other sensors, 2 routing PCBs were designed. Each routing card connects to two OPAL-RT digital output modules, and one analogue input module, using a 38-pin ribbon cable for each connection. These connections are routed to 6 sub-modules PWM signals and voltage measurements, and up to two sensor cards, allowing for 4 sensor signals per routing card. The converter only uses 6 current transducers, which makes one sensor card slot available, which is available for additional voltage measurements.

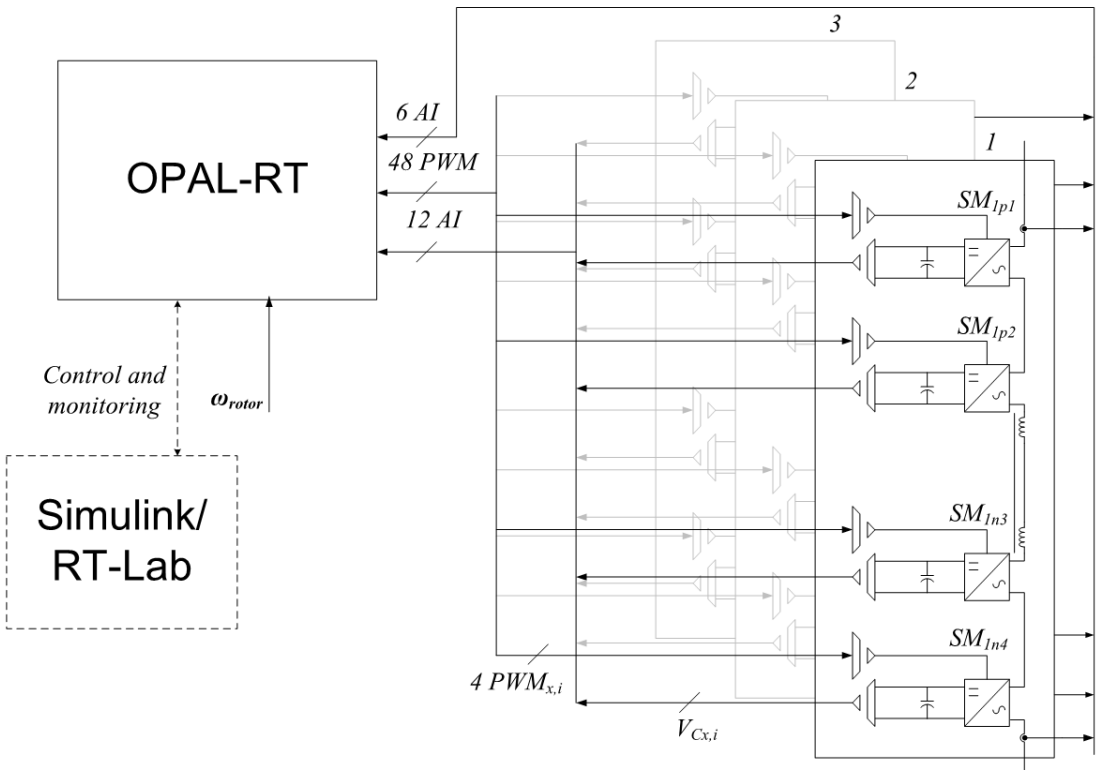

Figure 5-24 Connections between the power stages and the controller. Dashed connections are virtual.

5.2.4. Master controller

The master controller is programmed on an OPAL-RT OP5600 Real-time digital simulator. This computer has 4 blocks that provide both digital and analogue inputs/outputs. The high-speed controllers are implemented on an FPGA chip inside the OP5600, while user controls are accessible through a desktop computer running Simulink/RT-LAB. A diagram showing the connections between the power stage and the master controller can be seen in Figure 5-24.

The converter power stages, routing PCBs, and OPAL-RT controller are all housed in a standard 19" rack and the three-phase output terminals are connected to either a 3-phase variac and a static load or the induction motor.

5.3. SUMMARY

This chapter covered the design of a BMCI including the choice of number of sub-modules *n*, calculation of total leg inductance and sub-module floating capacitance. The

number of sub-modules has a direct effect on the inverter ac-side voltage THD, with higher values of n giving lower distortion. When operating in boost mode ($d_{dc,x}<0.5$), with maximum modulation index, the BMCI performs better than a conventional buck MCC, as the converter can produce more discrete voltage steps, for the same number of sub-modules.

The type of modulation scheme also has an effect, and PSC and PDC modulation are examined. The main difference is that PDC modulation gives more consistent THD over a range of $d_{dc,x}$ values, while PSC varies between the boundary points in Table 5-1.

Higher values of n increase the voltage steps in the output, reducing dV/dt, common mode currents, and THD of voltage at motor terminals. This in turn has a beneficial effect on motor efficiency, as iron losses are reduced. The size of the leg inductance also reduces, while total arm capacitance remains constant for a given power level and base speed.

Chapter 6. SIMULATION OF A BMCI FOR A HYDROGEN TRAM

This chapter shows the application of a BMCI in a light rail vehicle with a Hydrogen Proton Exchange Membrane (PEM) fuel cell. Sub-module capacitance and leg inductance values have been calculated using the methods described in Chapter 5 and the converter is simulated in Simulink using the continuous time model derived in Chapter 3.

To evaluate the practical implementation of a boost modular cascaded inverter (BMCI), the simulated converter used in Chapter 6 is compared to a state-of-the-art solution using a voltage-source inverter with a cascaded boost converter (BVSI). The criteria used are energy stored in capacitors and power inductors, total semiconductor power rating required, converter efficiency, and total harmonic distortion. Catalogue capacitor and inductor energy densities and specific energies are used to estimate the volume and weight of each system's energy storage.

6.1. SIMULATION SETUP

Due to their high efficiency, the Proton Exchange Membrane (PEM) hydrogen fuel cells have become a viable technology for the transport industry. This type of fuel cell also benefits from temperature operation below 100°C. The BMCI proposed in this work is a boost-buck dc-ac converter. The capability to convert a variable dc voltage to a lower or higher ac voltage can be useful for drives powered by a hydrogen fuel cell as PEM fuel cells are characterised by a relatively high output resistance, which causes the terminal voltage to vary over a wide range [155]. The BMCI can be used to compensate for this reduction in stack output voltage and to interface the fuel cell directly to the traction motor, thus replacing a standard boost converter – inverter drive.

6.1.1. Vehicle model

Most trams are powered by an overhead line, but the high cost of extending electrified lines has created a niche for autonomous vehicles that carry the power source on board. This has created a potential market for hydrogen fuel cell trams. The simulated BMCI has been designed for a vehicle based on a CAF Urbos 3 tram [156], comprising of 7 articulated carriages, with parameters listed in Table 6-1

Table 6-1 Tram parameters

Figure 6-1 A Midland Metro Urbos tram (source: Railwaygazette.com)

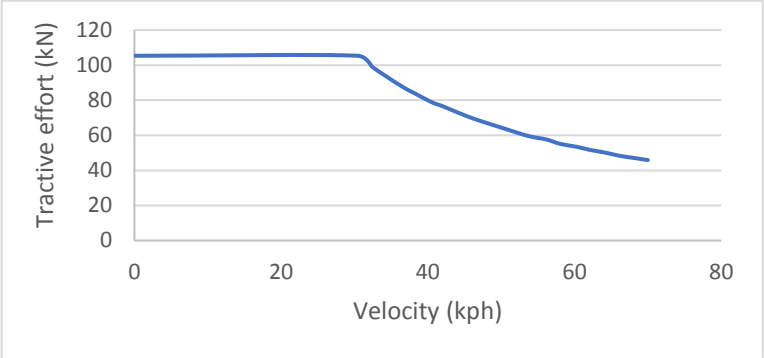

Figure 6-2 Urbos 3 tram tractive effort chart

The vehicle data includes the train resistance, according to the Davis formula [157], with parameters for rolling resistance *A*, speed dependent resistance *B*, and aerodynamic resistance *C*.

Table 6-1 Tram parameters

Traction motors	P_{MOT}	*12 x 80kW*
DC-link voltage	V_{DC}	*750V*
Mass, loaded	*m*	*80 tonnes*
Rolling resistance	*A*	*1084.81 N*
Speed dependent resistance	*B*	*142.89 N/kph*
Aerodynamic resistance	*C*	*10.98 N/kph²*
Maximum speed	vel_{max}	*70 kph*
Maximum tractive effort	TE_{max}	*105kN*
Mechanical drivetrain efficiency	η_{mech}	*94.16%*

The exact details of the traction motors used in an Urbos 3 tram are not published and are extrapolated from dc-link voltage and power rating. The synchronous frequency, slip, power factor, and number of poles are chosen based on published data from traction motor manufacturers [35], [158]. The Urbos 3 has 12 asynchronous ac motors, each rated at 80kW continuous power. Standard practice in railway vehicles is to have one traction inverter feeding two asynchronous motors, and for the simulation two machines are lumped into one with twice the power rating with details listed in Table 6-2.

Table 6-2 Traction motor parameters

Nominal Voltage	*532 V_{RMS}*
Nominal current	*204 A_{RMS}*
Nominal Power factor	*0.85*
Base Frequency (maximum power)	*100 Hz*
Base Motor speed	*1980 rpm*
Torque	*772 Nm*
Slip	*1%*

The vehicle mechanical model can now be constructed, using Table 6-1 and Table 6-2, with a diagram shown in Figure 6-3:

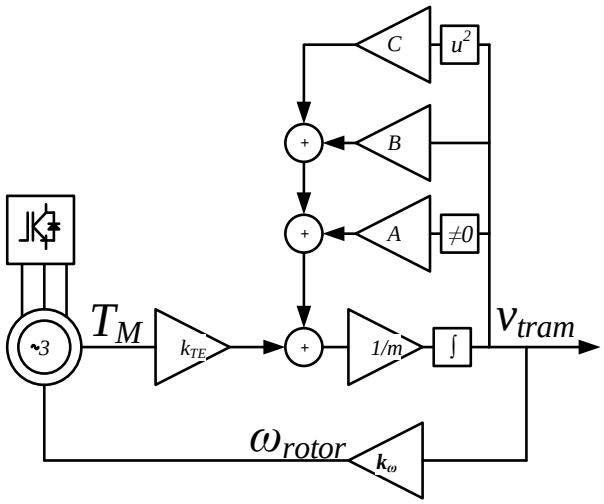

Figure 6-3 Tram mechanical model

The model input is motor torque, T_M, which is converted to tractive effort, *TE*, using the coefficients k_{TE} *and* k_ω. The rated speed is inferred from Figure 6-2 as *30 kph*, with rated tractive effort Table 6-1.

$$k_{TE} = \frac{TE_{\max}}{T_{M,\max}} = \frac{105 \times 10^3 N}{772 Nm} \quad (6\text{-}1)$$

$$k_{\omega} = \frac{30 kph}{207.34 rads^{-1}} \quad (6\text{-}2)$$

6.1.2. Fuel cell stack model

The PEM fuel cell consists of seven basic elements, as illustrated in Figure 6-4. The fuel cell generates electrical power from the chemical reaction of hydrogen and oxygen by "routing" hydrogen electrons via the electric circuit connected to its output, while the resultant hydrogen ions travel through the membrane.

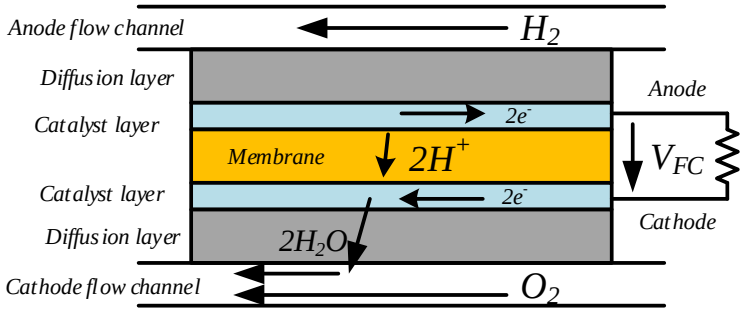

Figure 6-4 Basic structure of a PEM fuel cell

Without a load connected to the output, the charge build-up between the cathode and the anode produces an ideal open-circuit voltage E^0, that is described by [155]:

$$E^0 = 1.23 - k_E (T_{FC} - 298.15) + \frac{RT_{FC}}{2F} \times \left(\frac{P_{H_2} P_{O_2}^{0.5}}{100^{o1.5}} \right), \quad (6\text{-}3)$$

, where T_{FC} is the absolute fuel cell temperature in Kelvin, P_{H2} is the hydrogen absolute pressure in kPa. P_{O2} is the oxygen absolute pressure, also in kPa, k_E is temperature coefficient for liquid water, and R is the ideal gas constant.

When the fuel cell is loaded, the terminal voltage drops due to three main mechanisms: activation loss, ohmic loss, and concentration loss [159], [130], [160]. The resultant fuel cell terminal voltage can be expressed as:

$$V_{FC} = E^0 - (R_{Act} - R_{\Omega} - R_{Conc})I_{FC}, \tag{6-4}$$

, where V_{FC} is the fuel cell terminal voltage, R_{Act} is the activation loss resistance, R_{Ω} is the ohmic resistance, R_{Conc} is the concentration resistance, and I_{FC} is the fuel cell output current.

At high currents, the fuel cell concentration resistance increases exponentially due to mass transport, with terminal voltage eventually reaching 0. In a vehicle application, the fuel cell stack rated power would be somewhere below the peak power, where output voltage drop is dominated by activation losses, as increasing the current any further risks pushing the whole power system into an unstable condition.

The detailed model of the fuel cell stack requires parameters such as temperature during operation, hydrogen and air pressures, and other data specific to the manufacturer. This information is not readily available and instead a simplified model is used, as shown in Figure 6-5.

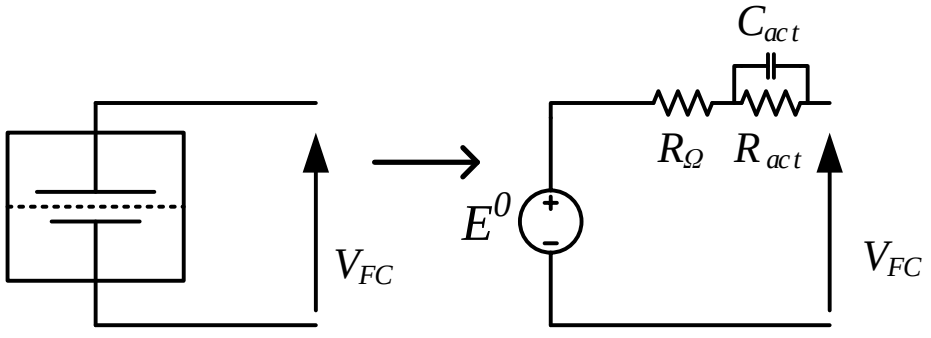

Figure 6-5 Simplified equivalent circuit model of a fuel cell stack

Since the fuel cell would be operated only in its stable region, non-linearities at high output current can be ignored. Below that region the fuel cell can be modelled as a voltage

source, with a series resistance and a parallel capacitance, to account for the transient response. It should be noted that the simplified circuit model does not consider the chemical and mechanical dynamics of the fuel cell power and assumes static resistances.

The simulated fuel cell stack is based on 2 Hydrogenics HD90 [161] units connected in parallel, that can supply up to 198kW of continuous power. The actual fuel cell parameters are unknown and are extrapolated from data found in literature [162] and [163], shown in Table 6-3. The ohmic and anode resistances are chosen to be 10% of the total series resistance each. The capacitance of the cell is related to the fuel cell active area and is thus extrapolated by scaling proportionally to cell current.

Table 6-3 Simulated fuel cells tack parameters

Parameter	*Symbol*	*Value*
Stack rated power	P_{FC}	2 x 99kW
Stack open circuit voltage	$V_{FC,OC}$	360V
Terminal voltage at rated power	V_{FC}	220V
Stack rated current	$I_{FC,rated}$	2 x 550A
Ohmic resistance	R_{Ohm}	13mΩ
Activation resistance	R_{act}	123mΩ
Activation capacitance	C_{act}	9.1mF

A plot of the static V-I characteristics, at dc, of the simulated stack are shown in Figure 6-6:

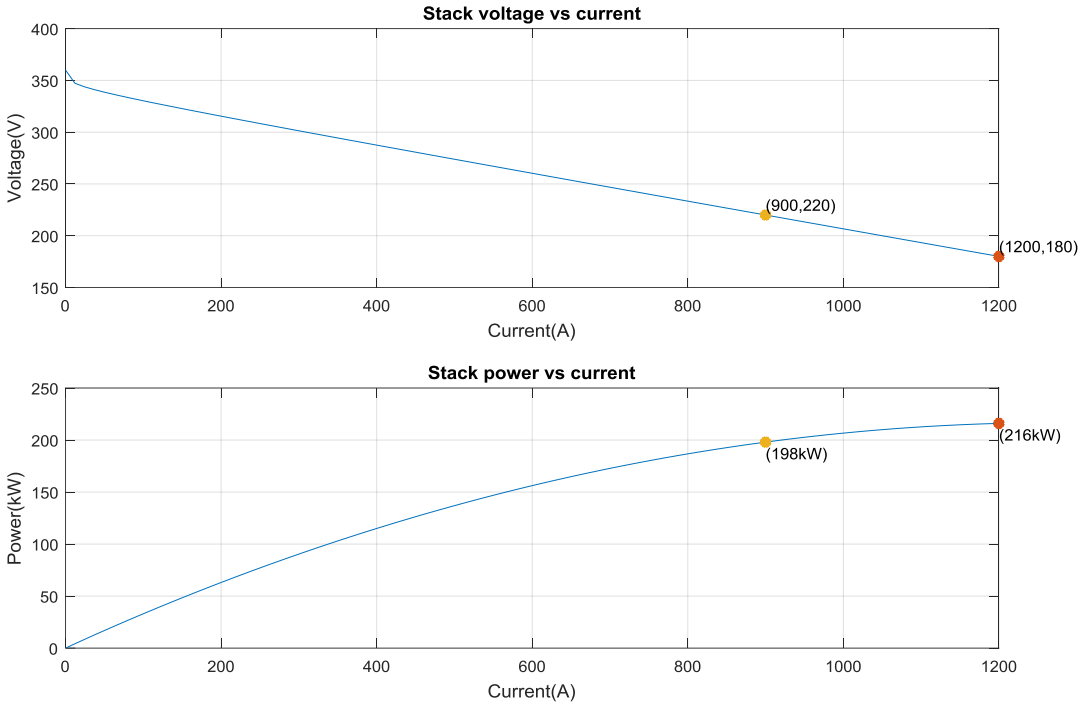

Figure 6-6 Simulated fuel cell stack voltage-current characteristics

6.1.3. BMCI model

The converter is designed as a drop-in replacement for a conventional tram inverter drive, producing the same peak line-to-line motor voltage, but drawing power from a hydrogen fuel cell. During braking the energy, recovered by the converter, is dissipated into a braking chopper resistor. This design uses no energy storage and the fuel cell is designed to supply the peak power demand of the system, including auxiliary loads.

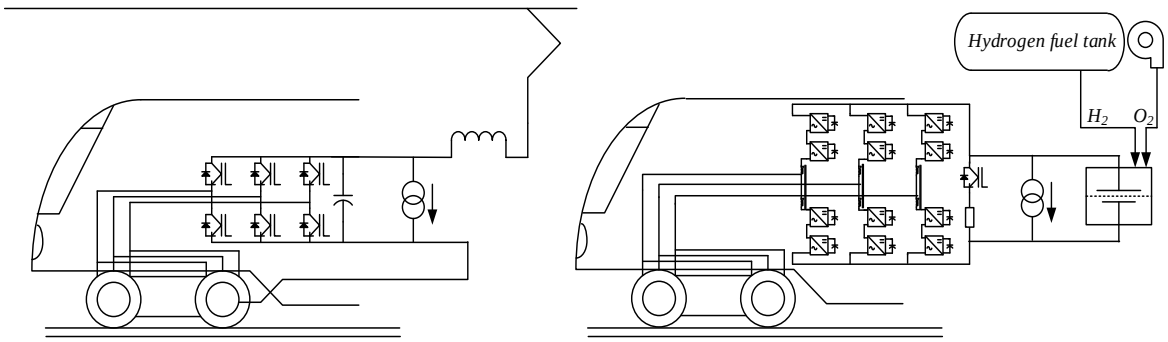

Figure 6-7 Conventional motor drive (left) and proposed BMCI fuel cell drive (right)

The numerical simulation model uses the continuous time equations derived in Chapter 3, that describe the system. The converter inputs and outputs are maintained by the control systems, described in Chapter 4, with the addition of a speed controller to simulate a tram driver. The BMCI is designed using the design methodology in Chapter 5. The converter parameters can be found in Table 6-4:

Table 6-4 Simulated BMCI parameters

Parameter	*Value*
Sub-module mean capacitor voltage	300V
Sub-module capacitance	10mF
Sub-module capacitor ESR	5mΩ
Leg inductance	62μH
Transistor collector-emitter resistance	2mΩ
Transistor switching frequency	4kHz
Low-speed ripple compensation injected frequency	180Hz

The switches in the simulated model have the same series resistance as a FF300R07ME4_B11 transistor half-bridge module [164].

6.2. BMCI DRIVE

The operations, of the proposed BMCI, are examined using a basic acceleration – cruising – braking traction cycle. The simulated induction motor drive accelerates the vehicle up to 50kph, which is a typical maximum speed for an urban tram, and brakes back to a standstill. During this cycle all power is provided by the hydrogen fuel cell stack, while braking energy is dissipated through a braking resistor.

6.2.1. Overall performance

The BMCI – fuel cell drive, with all control systems operating, is simulated for a full traction cycle, displayed in Figure 6-8. The figure shows the speed trajectory of the BMCI powered tram, as well as fuel cell stack terminal voltage and output current, motor torque, and the boost ratio, that the converter is operating at.

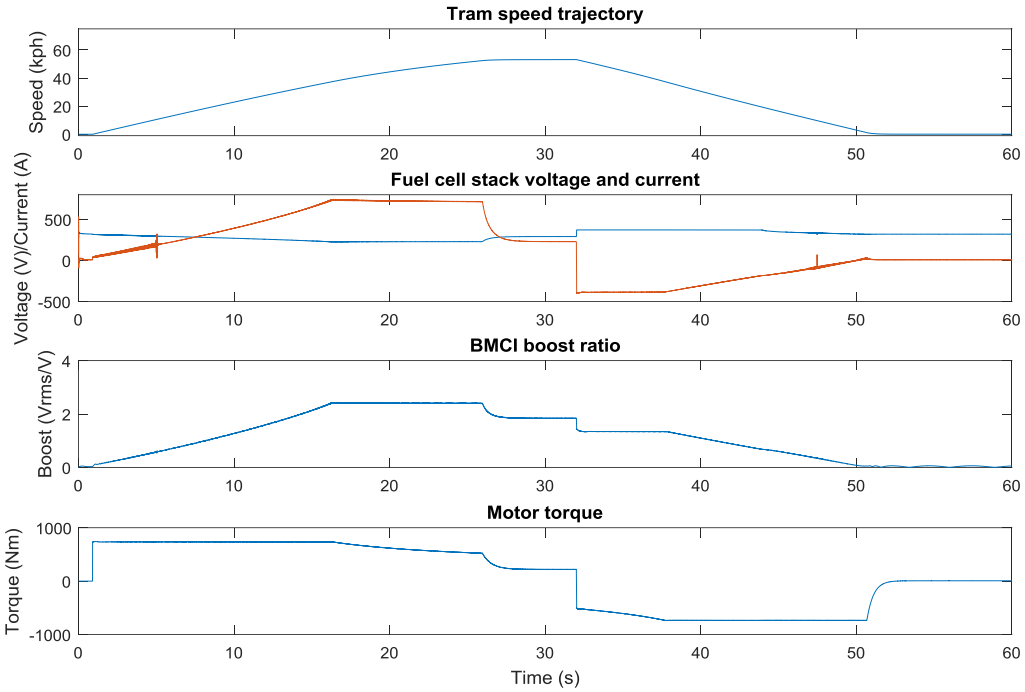

Figure 6-8 Tram acceleration - cruising - braking cycle

During the initial acceleration, the BMCI is operating in voltage buck mode. At this point the fuel cell stack voltage is at its highest, while the output voltage is at its lowest. Up to a speed of roughly 7km/h the converter is working with capacitor ripple compensation, required to operate with low output frequency. The current ripple caused by small unbalances in the compensation currents between phase legs can be seen to cause voltage ripple at the fuel cell terminal.

The converter's boost ratio increases in a non-linear fashion, as the fuel cell voltage drops while output power increases. The highest boost ratio achieved is about 3.125, and

it occurs when the converter is operating with a constant power output. As input power reduces, fuel cell stack voltage increases, reducing the boost requirement. While the converter can be controlled with variable sub-module capacitor voltage, in the scheme presented here it is kept constant to reduce capacitor voltage ripple amplitude. In Figure 6-9 the average arm sub-module voltages, motor current, and leg circulating currents are shown.

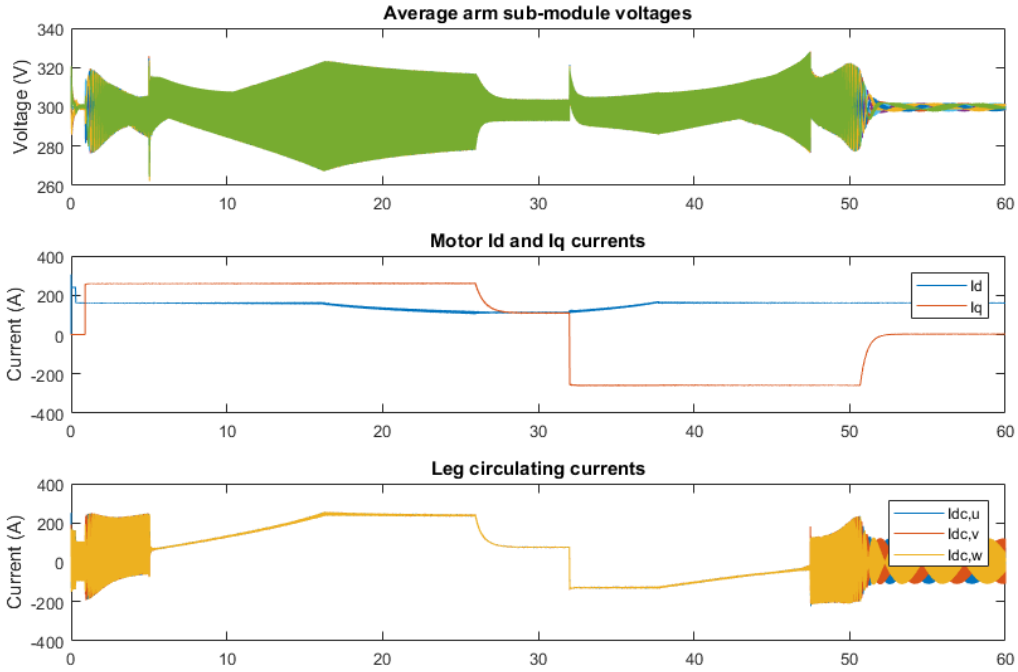

Figure 6-9 Feedback values for the BMCI during a traction cycle

At start up the converter arm currents have a high amplitude, due to the injected common-mode currents. At *t=5s* the converter the low-frequency compensation scheme is disabled, and the second harmonic suppression controller is engaged, which accounts for the disturbance to the capacitor voltage ripple. However, the converter input current in Figure 6-8, has a much lower current ripple, as the large oscillations are circulated in the converter circuit.

During the whole traction cycle the peak-to-peak sub-module capacitor voltage ripple is kept below 60V, which is 20% of the nominal value.

6.2.2. Operation at low-speeds

When the vehicle is moving in the low-frequency region, which for the studied example is for an output frequency below 28Hz, the BMCI inserts in each leg a differential voltage and injects a common mode current at the same frequency. The inserted voltage must be the same for all converter legs so as not to appear across the fuel cell stack or the motor terminals.

By zooming in at the start of the cycle, shown in Figure 6-1, converter terminal voltages and currents can be better examined in Figure 6-10. It can be observed that the motor voltage has relatively low quality, as the voltage steps consist of more than one level.

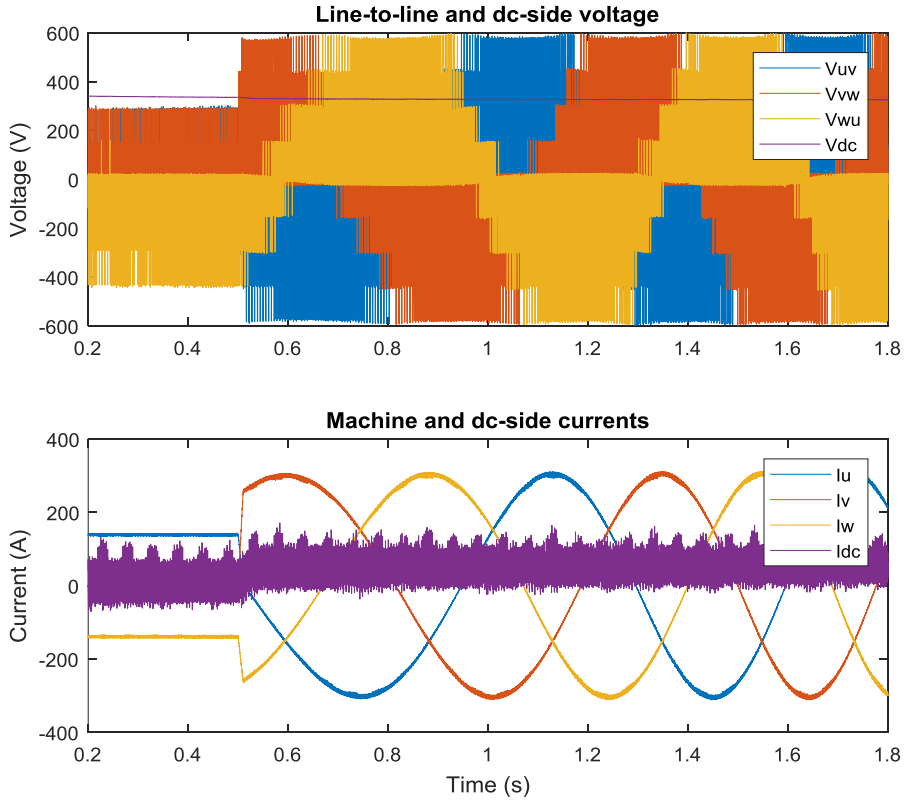

Figure 6-10 Converter voltages and currents at start of acceleration showing low distortion machine current

Before start-up, at standstill, the inverter is maintaining constant field current to avoid charging the magnetizing inductance during the traction cycle. When a torque command is applied, the inverter produces slip, at which point the vehicle starts accelerating. The PWM waveform pulses cannot be distinguished due to the high frequency ratio f_{PWM}/f_{field}. A further magnification of the converter operation around *t=0.95s* shows the dc-side current ripple and the shape of the ac-side voltage pulses, as Figure 6-11 shows.

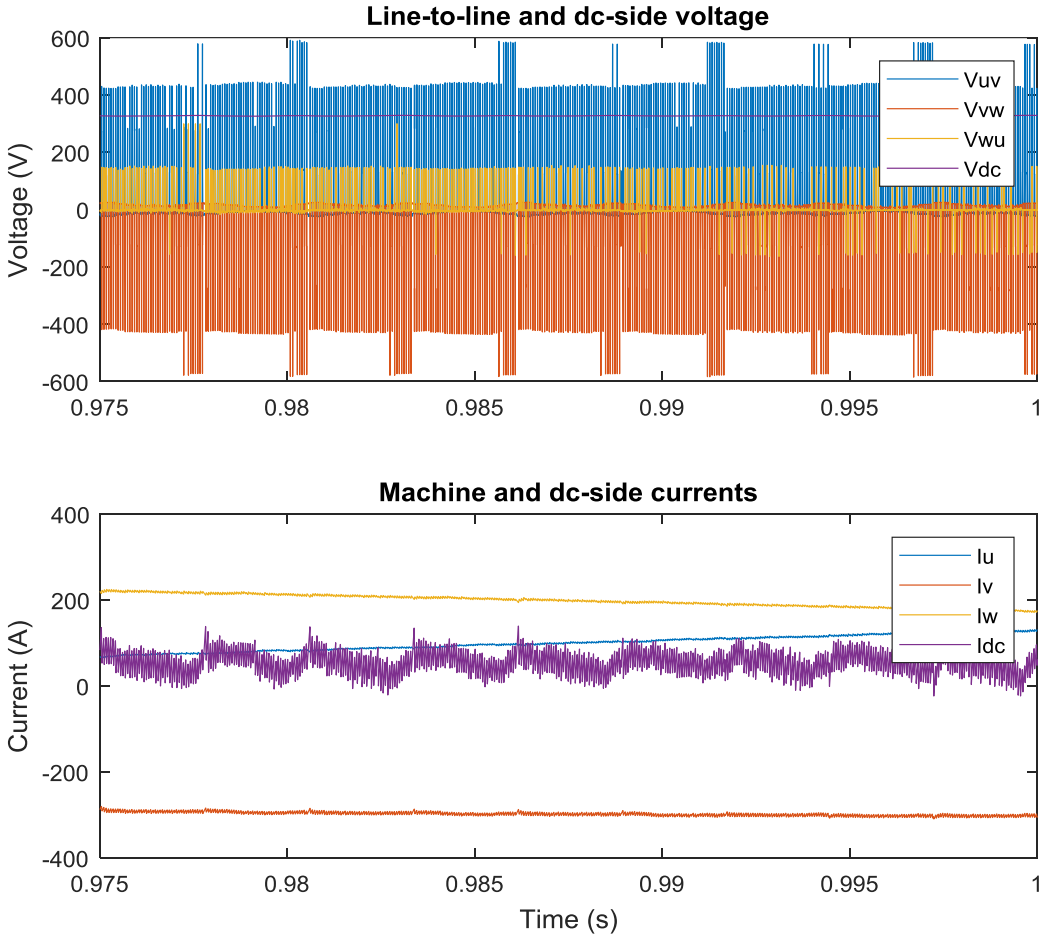

Figure 6-11 Zoomed in capture at t=0.975s, showing dc current ripple caused by the low-frequency arm-balancing currents; motor currents only show small spikes from the arm voltage step switching

The BMCI input current contains both switching ripple and the injected compensation current at 400Hz, with the latter becoming more visible as frequency increases. This is due to the decreasing ratio of converter output frequency and compensation frequency.

6.2.2.1. Capacitor voltage ripple and circulating current

The goal of the low-frequency compensation scheme is to limit the voltage ripple across the sub-module capacitor for each arm. Figure 6-12 shows how the common mode current is injected in each arm current, effectively chopping the phase current. The component that accounts for energy transfer between the top and bottom arms appears as an overlap between their respective currents.

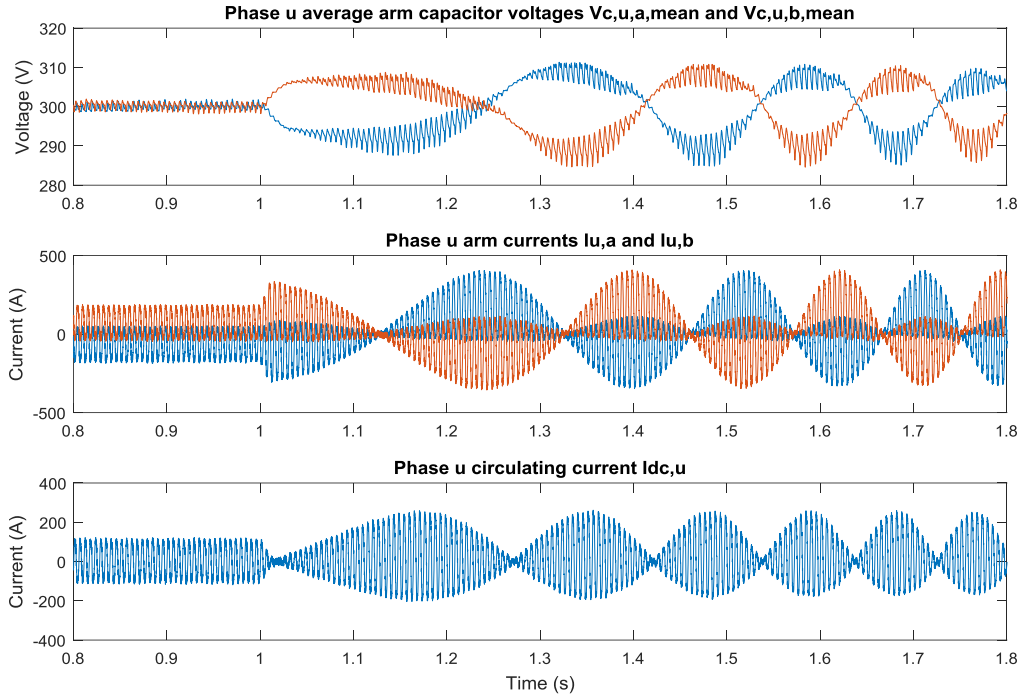

Figure 6-12 Arm capacitor voltage, arm currents, and circulating current at low machine frequency

The demand for the compensating current is highest at start-up, as at that point there is little power drawn from the fuel cell, its voltage being close to the maximum value, and the voltage ripple is at a low frequency. The simulation shows that even in demanding condition the converter compensates the capacitor voltage fluctuation without overshooting the design's maximum peak-to-peak value or the peak arm current value.

6.2.3. Constant torque region

In the constant torque region, the converter initially bucks and then boosts the ac-side voltage, while maintaining constant output current amplitude.

6.2.3.1. Ac-side voltage buck

With the peak line voltage less than the fuel cell terminal voltage, the modulation index M is less than the dc duty cycle d_{dc}, and the number of effective output levels is low, reducing the motor voltage distortion. The converter voltages and currents, at the time of transition out of the low-frequency compensation mode, is shown in Figure 6-134.

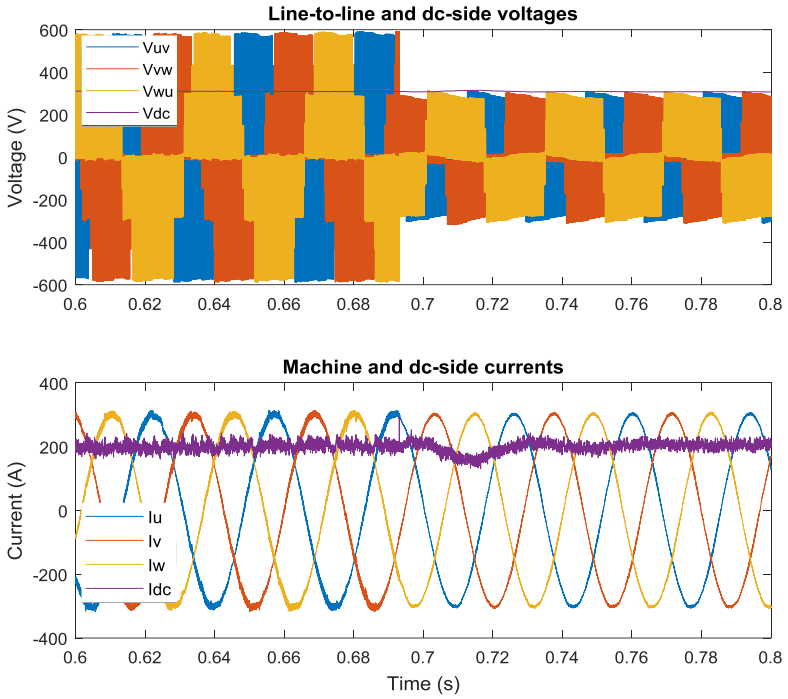

Figure 6-13 Converter in the constant torque region, with ac-side voltage buck

Before the point of transition, the BMCI dc-side current has a peak-to-peak ripple of 80A at 400Hz. When the output frequency is high enough and the ripple compensation is no longer required, the converter returns to its normal operations. The initial disturbance is due to the activation of the circulating current harmonic suppression controller. Also, it can be noticed that the phase current has much lower current ripple as the phase voltages

no longer have the higher voltage steps caused by the low-frequency ripple compensation scheme.

6.2.3.2. Ac-side voltage boost

Referring to Figure 6-8, the converter enters boost operation at roughly *t=8s.* After this point the converter ac-side voltage gains additional steps and the waveform quality improves, as shown in Figure 6-14:

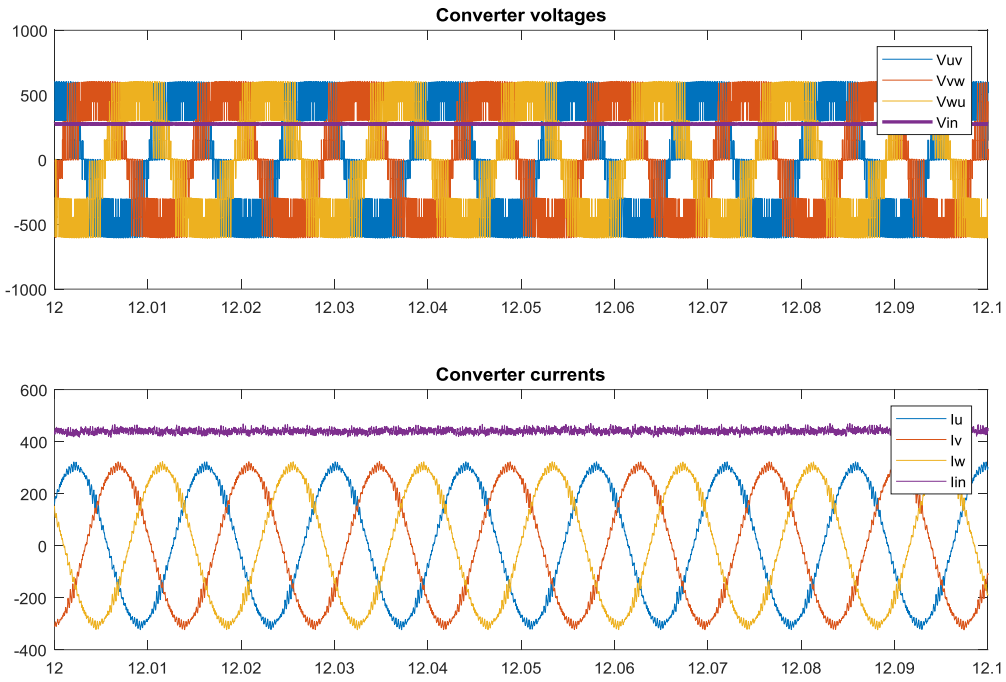

Figure 6-14 BMCI under ac-side voltage boost operation

6.2.4. Constant power region

In the constant power region, the BMCI is operating at fixed boost ratio, with constant ac-side voltage amplitude, but with increasing machine slip. The ac-side voltage waveform has the maximum number of levels, for the appropriate dc duty cycle. A zoomed-in view of the waveform from the converter traction cycle is displayed in Figure 6-15.

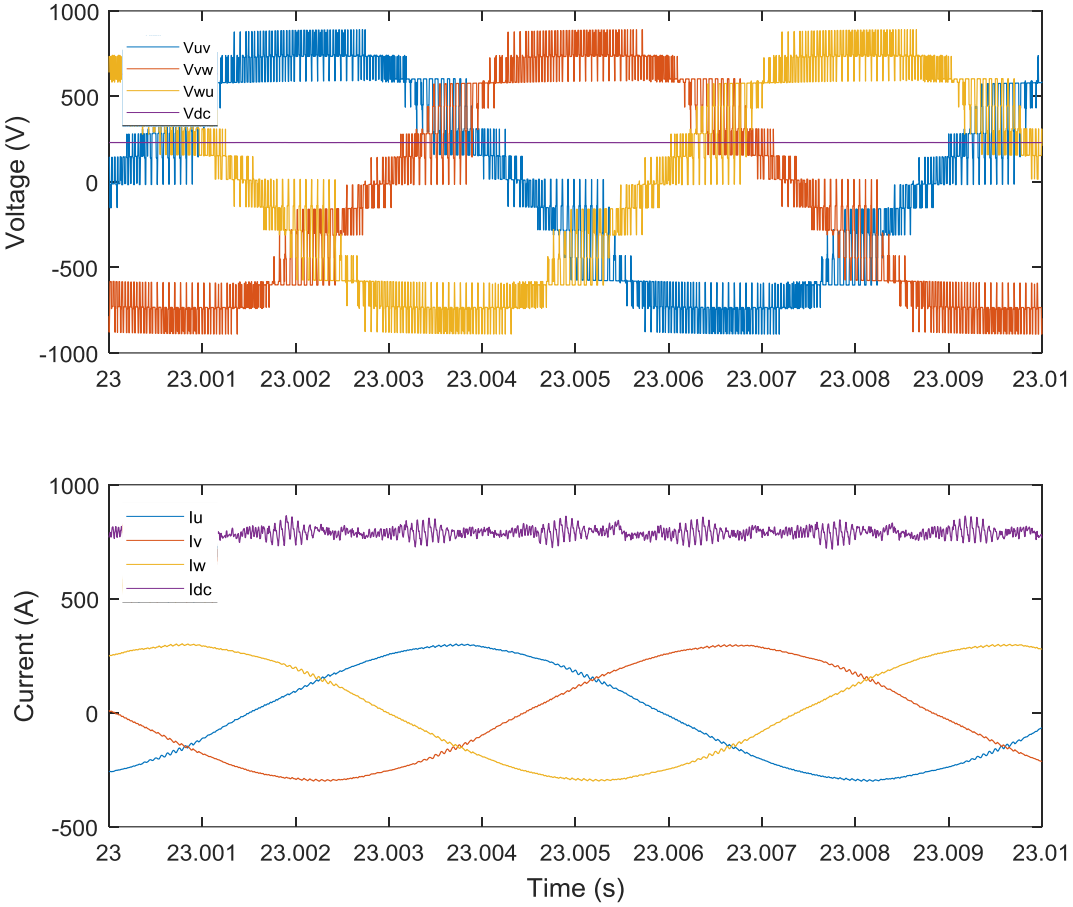

Figure 6-15 BMCI terminal voltages and currents at constant output power

At constant power the fuel cell is producing 220V, with an output current of 700A, and the dc duty cycle $d_{dc} \approx 0.191$. The voltage of a leg inductor, and its frequency spectrum are shown in Figure 6-16:

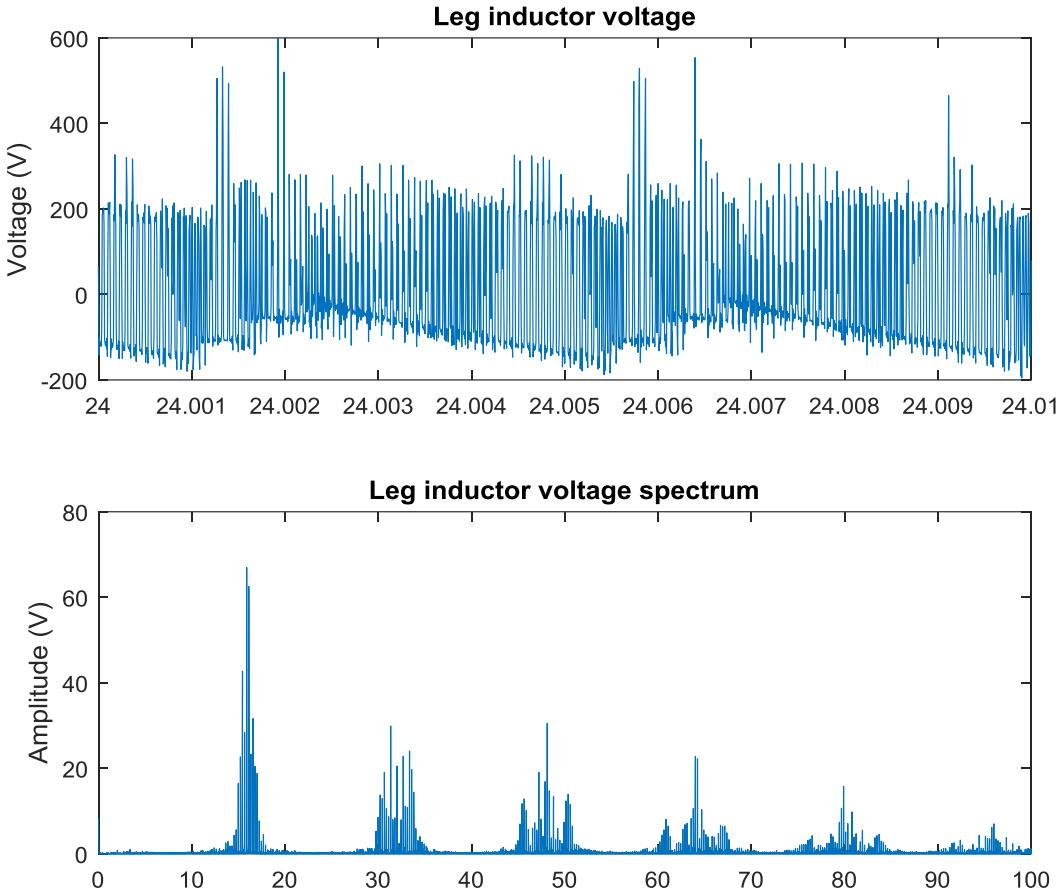

Figure 6-16 Leg inductor voltage and its frequency spectrum during vehicle acceleration; peak component is at the arm switching frequency

The figure shows that the leg inductor voltage switching step is only one sub-module voltage, with only a few cycles of 2-step switching. The frequency spectrum shows that most of the harmonic energy is around $2n$ times the device switching frequency f_{sw}, and that there are relatively wide side-bands due to intermodulation.

6.2.5. Regenerative braking

During regenerative braking the BMCI works at the lowest boost factor, as it draws no power from the fuel cell stack while energy is dissipated by the braking resistor. This condition determines the maximum required sub-module capacitor voltage. Another change is that during braking d_{dc} remains constant and is different form the value during

acceleration. This change in dc duty cycle affects both input current ripple and output THD performance. A zoomed in capture at the start of regeneration is shown in Figure 6-17.

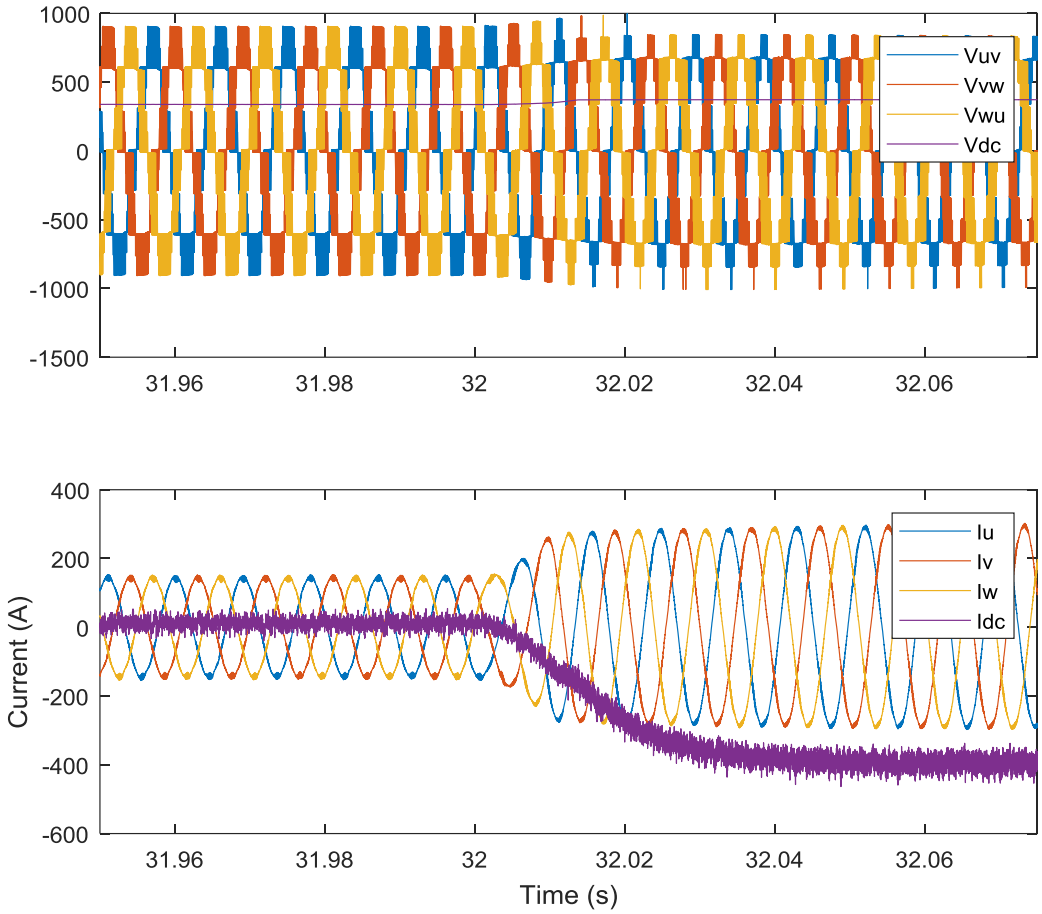

Figure 6-17 Converter currents and voltage at start of braking; ac-side voltage waveform changes as converter is regenerating power and dc duty-cycle steady-state value is different

After a reverse torque step at *t=32s* the converter input current is reversed to -390A at 375V, regenerating 146.25kW. The input current peak-to-peak ripple is 80A, at d_{dc}*=0.315.* The spectrum of the voltage across one phase inductor is shown in Figure 6-18.

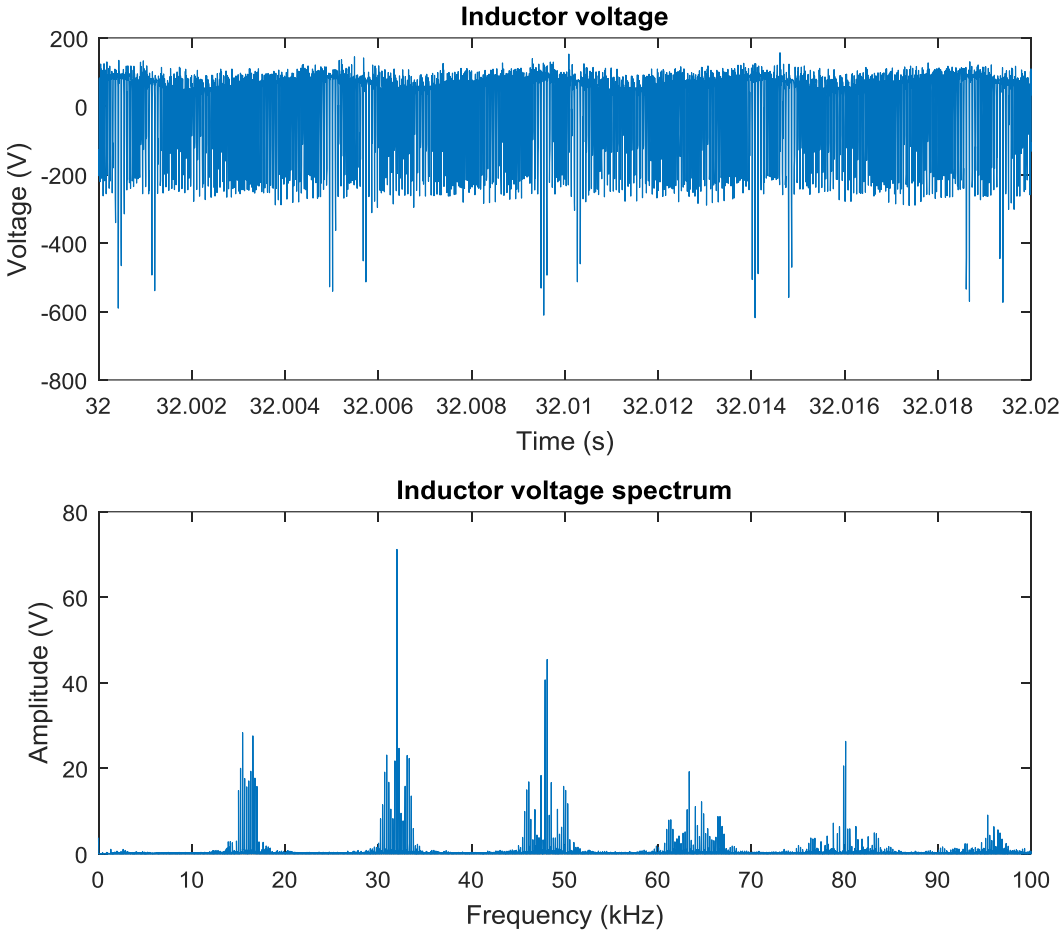

Figure 6-18 Phase leg voltage and its FFT spectrum during vehicle braking

Similar to the acceleration phase, the inductor voltage waveform is also switching with 1 voltage step and a few pulses of 2-step. The frequency spectrum, however, is different, with lower energy around the $2nf_{sw}$ point (4^{th} harmonic), and more energy shifted to 8^{th} harmonic. With the converter ac-side voltage having roughly the same amplitude, the change in harmonic performance is mainly due to the considerable shift in d_{dc}.

6.3. COMPARATIVE STUDY

In order to assess the practical viability of the proposed converter, a comparative study has been undertaken, based in the same fuel cell tram drive as in the rest of this chapter. It compares the BMCI with the state-of-the-art topology of a boost inverter (BVSI), composed of an interleaved boost dc-dc converter and a traditional VSI. Both

topologies are designed for the same traction motor, and fuel cell parameters, as listed in Table 6-2 and Table 6-3. The comparison has been based on total semiconductor apparent power, mass and volume of energy storage components, efficiency and weighted total harmonic distortion (WTHD), as these parameters are important for a traction system.

The passive components for the two systems have been designed based on the assumption that the converters are lossless. As semiconductor packaging can be optimized for a specific application, the power density and weight of the power electronics is not evaluated. Gate driver losses are also ignored, as they are part of the system realization and can be difficult to predict. However, they are accounted for in the parameter '*system complexity'.*

In part 6.3.5 system efficiency and weighted total harmonic distortion (WTHD) are evaluated. To achieve static conditions, the simulated load inertia is set to be 1000-times higher, resulting in constant machine speed for the duration of the numerical simulations. The WTHD is calculated using the following equation [165]:

$$WTHD = \frac{\sqrt{\sum_{n_{harm}=2,3,\ldots}^{\infty} \left(\frac{V_{nharm}}{n_{harm}} \right)^2}}{V_{fund}} \qquad (6\text{-}5)$$

, where V_{fund} is the amplitude of the fundamental and n_{harm} is the number of the harmonic, and V_{nharm} is its amplitude.

6.3.1. Switch apparent power requirement

6.3.1.1. BMCI

The worst-case arm current occurs at rated power, and unlike voltage-source inverters, the BMCI switches do not need to be rated for the peak machine current at standstill – the dc-side current at that point is very small. Instead, the arm RMS current at rated output power is used.

$$S_{arm} = I_{arm,rms} \times \sum_{i=1}^{n} V_{C,i} = \sqrt{I_{dc,x}{}^2 + \left(\frac{I_{ac,x}}{2}\right)^2} \times n\left(V_C + \frac{\Delta v_C}{2}\right) \quad (6\text{-}6)$$

$$S_{sw,total} = 6 \times 4 S_{arm} \quad (6\text{-}7)$$

Results for simulated drive (*n = 2, $I_{dc,x}$=250A, $I_{ac,x}$=289A, $I_{a/b,x}$=288.5A$_{RMS}$, G_V=3.4, V_C=300, Δv_C=60*):

$$S_{arm} = I_{arm,rms} \times \sum_{i=1}^{n} V_{C,i} = 288.5 \times 2 \times 330 = 190.4kVA \quad (6\text{-}8)$$

$$S_{sw,total} = 6 \times 4 S_{arm} = 6 \times 4 \times 190.4kVA = 4.57MVA \quad (6\text{-}9)$$

6.3.1.2. BVSI

The boost converter devices must be rated for the full-power fuel cell current. The total boost converter rating is independent of the number of interleaved phases.

The voltage-source inverter must be rated for the peak machine current, as the system must be able to operate down to 0Hz motor frequency, with the full rated stator current.

$$S_{boost} = 2 \times V_{dc} \times I_{dc} = 2 \times 800 \times 750 = 1.2MVA \quad (6\text{-}10)$$

$$S_{vsi} = 6 \times V_{dc} \times I_{ac,x} = 6 \times 800 \times 288 = 1.38MVA \quad (6\text{-}11)$$

$$S_{sw,total} = S_{boost} + S_{vsi} = 1.2MVA + 1.38MVA = 2.58MVA \quad (6\text{-}12)$$

An important note is that the BVSI S_{boost} is for a diode and transistor combination, and S_{vsi} is for a pair of transistors + freewheeling diode switches.

6.3.2. Comparison of total capacitor energy

The BMCI capacitance is designed for 20% voltage ripple, while the boost-voltage source inverter dc-link capacitor is designed for 1% voltage ripple. This is mainly a function of the required capacitor ripple current and less so of dc-link voltage stability requirement.

6.3.2.1. BMCI

The BMCI capacitor energy, $W_{C,BMCI}$, can be calculated as:

$$W_{C,BMCI} = 6nC\frac{V_{C,nom}{}^{2}}{2} = 5.4kJ \qquad (6\text{-}13)$$

This energy is relatively high, because each converter leg is a dc to single-phase converter, with the largest oscillating power component being at the fundamental machine frequency.

6.3.2.2. BVSI

The BVSI capacitor energy, $W_{C,BVSI}$, can be calculated as:

$$W_{C,BVSI} = \frac{1.1\times10^{-3}\times800^{2}}{2} = 352J \qquad (6\text{-}14)$$

As the dc-link capacitor is common to all 3-phases of the inverter, and the two phases of the boost-converter, the required capacitance is much lower. In addition, the boost converter PWM carrier can be shifted, so that it is complementary with the inverter dc-side current pulses. This configuration reduces the capacitor RMS current.

6.3.2.3. Capacitor energy density (J/m^3) and specific energy (J/kg)

A survey of different manufacturers [166], [167], [168], of capacitors for traction applications is shown below:

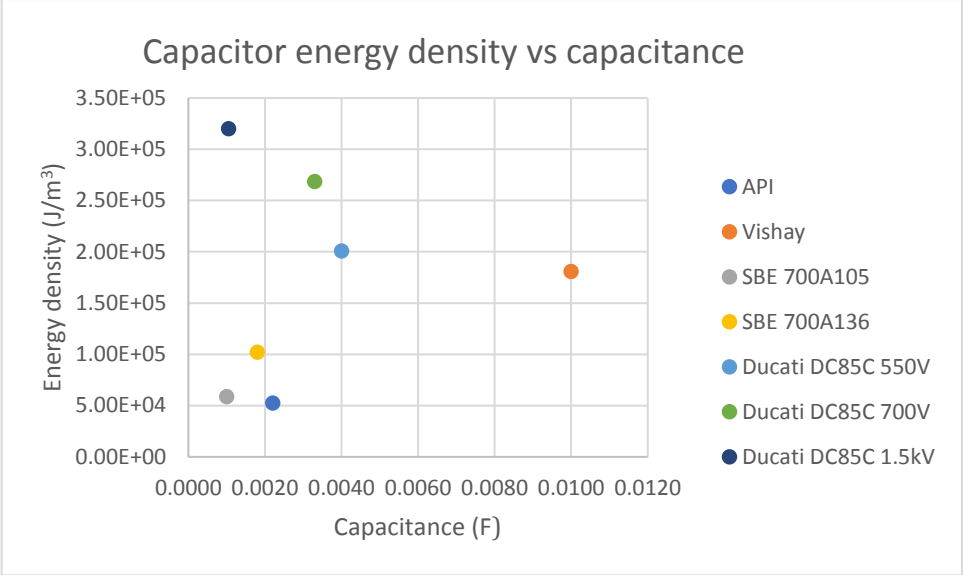

Figure 6-19 Capacitor energy density survey

As one would expect, the highest energy density is achieved by high-voltage electrolytic capacitors, where increasing the voltage by a factor of 2.14 gives an increase of 20%, which means a single large capacitor will be a denser solution, than multiple lower-voltage capacitors.

The specific energy of the same capacitors is shown in Figure 6-20. The data for some capacitors was not available.

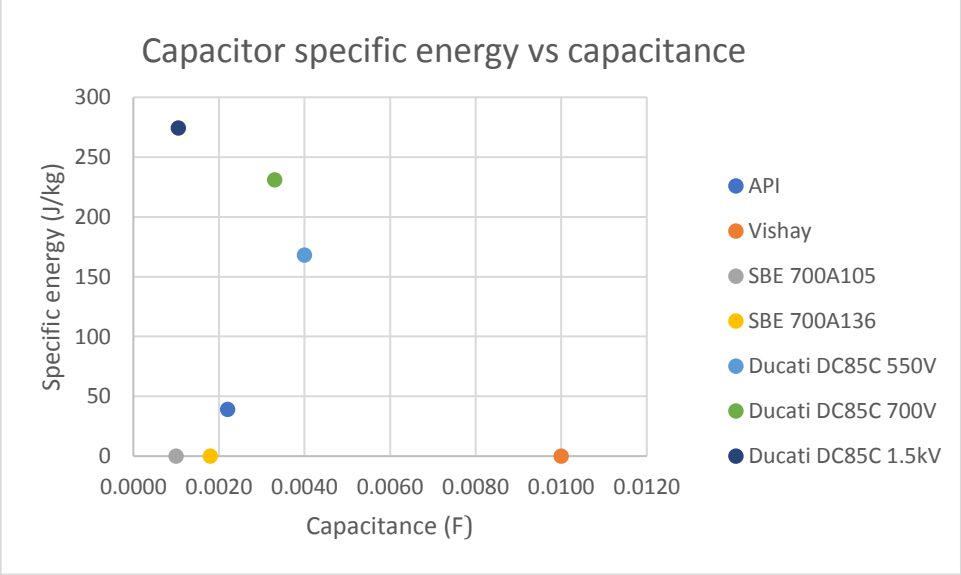

Figure 6-20 Capacitor specific energy survey

6.3.2.4. Converter capacitor bank energy

Using the DC85C series capacitors, from Figure 6-19, the total capacitor bank weight and volume are estimated for each converter. These capacitors were chosen, as they represent typical parts used for energy storage and filtering applications in power converters: they have high ac-ripple current ratings and are characterised for the working voltage, instead of the maximum rating.

i. BMCI

The BMCI requires 12 capacitors with total energy stored of 5.4kJ. Using the energy density of the 550V DC85C capacitors, the total capacitor bank volume is:

$$Vol_{C,BMCI} = \frac{5.4kJ}{2.01\times10^5\ J/m^3} = 0.027m^3 = 27l \qquad (6\text{-}15)$$

The total capacitor mass is calculated using data from Figure 6-20:

$$mass_{C,BMCI} = \frac{5.4kJ}{195.56\ J/kg} = 27.6kg \qquad (6\text{-}16)$$

ii. BVSI

The BVSI uses only one capacitor, but it requires lower voltage ripple, and a higher voltage. The estimated capacitor volume is:

$$Vol_{C,BVSI} = \frac{352J}{3.2\times10^5\ J/m^3} = 0.0011m^3 = 1.1l \qquad (6\text{-}17)$$

The capacitor bank mass becomes:

$$mass_{C,BVSI} = \frac{352J}{274.2\,J/kg} = 1.28kg \qquad (6\text{-}18)$$

Compared to the BMCI, the BVSI capacitor bank will be roughly 6 times smaller and 5 times lighter.

6.3.3. Comparison of total inductor energy and inductor losses

The governing parameter for leg or phase inductance are the peak-to-peak ripple currents $\Delta i_{L,leg}$ and $\Delta i_{L,phase}$, for the BMCI and BVSI respectively. They are designed to be 20% of the dc current at peak system power.

6.3.3.1. BMCI

Using the constraints above and the tram data from Table 6-1, the dc-current, phase dc-current, current ripple, and leg inductance are:

$$I_{dc} = 750A \qquad \therefore I_{dc,x} = 250A, \Delta i_{dc,x} = 50A \qquad L = 62\mu H \qquad (6\text{-}19)$$

From which the peak energy stored in each of the three leg inductors is:

$$W_{L,x} = 3\frac{L_{leg} \times \left(I_{dc,x} + \frac{\Delta i_{dc,x}}{2} \right)^2}{2} = 7.03J \qquad (6\text{-}20)$$

$$\Delta i_{dc} = 100A_{pk-pk} \qquad (6\text{-}21)$$

The BMCI current ripple is not constant over time, and the peak value is maintained only for a certain portion of the output waveform cycle. Thus, inductance can be optimized for either waveform quality or loss.

6.3.3.2. BVSI

Repeating the design procedure for the BVSI, and with the same constraints as for the BVSI, the dc-side current, phase dc current, current ripple and phase inductance are:

$$I_{dc} = 750A \qquad \therefore I_{dc,phase} = 375A, \Delta i_{dc,phase} = 75A \qquad L_{phase} = 570\mu H \tag{6-22}$$

From which the peak energy stored in each of the phase inductors is:

$$W_{L,x} = 2\frac{L_{phase} \times \left(I_{dc,phase} + \frac{\Delta i_{dc,phase}}{2} \right)^2}{2} = 96.9J \tag{6-23}$$

$$\Delta i_{dc} = 48A_{pk-pk} \tag{6-24}$$

The interleaved boost converter reduces the total dc current ripple to 64% of the amplitude of each phase, compared to the BMCI, where it was measured as twice the leg value.

6.3.3.3. Inductor energy density (J/m^3) and specific energy (J/kg)

Power inductors can occupy half of the converter volume and can account for most of the system weight and cost [41], [76], [169]. This is reflected in their poor energy density and specific energy. A survey of manufacturers of high-current power inductors, [170] and [171], is shown in Figure 6-21. The inductors were chosen to have a low inductance drop with dc-bias (<30%).

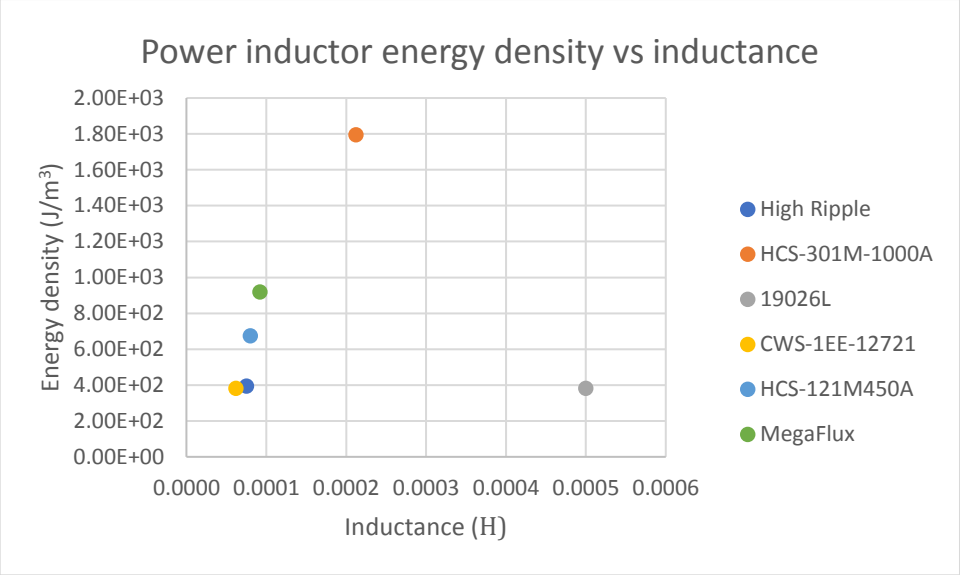

Figure 6-21 Inductor energy density survey

The specific energy, of the inductors in Figure 6-21, is shown in Figure 6-22:

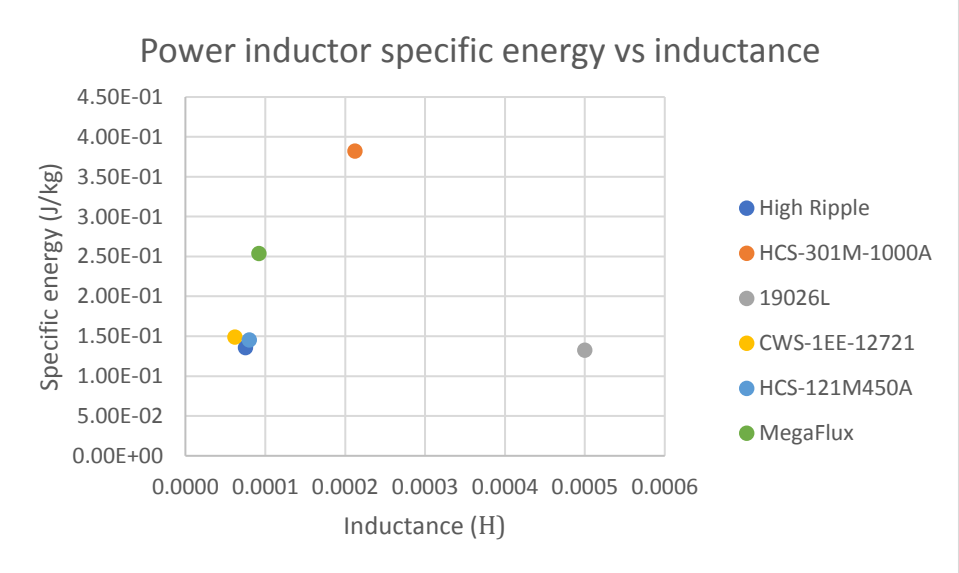

Figure 6-22 Inductor specific energy survey

6.3.3.4. Converter power inductor volume and weight

To compare the two systems, in terms of total weight and volume of all inductors, the calculations are done using data from Figure 6-21 and Figure 6-22.

i. BMCI

The BMCI uses 3 inductors with total energy of 7.03J. Using the *CWS-1EE-12721* inductor from Figure 6-21, the total volume becomes:

$$Vol_{L,BMCI} = \frac{7.03J}{0.382 \times 10^3 \, J/m^3} = 0.0184 m^3 = 18.4 l \qquad (6\text{-}25)$$

The total inductor weight will be:

$$mass_{L,BMCI} = \frac{7.03J}{0.169 \, J/kg} = 41.59 kg \qquad (6\text{-}26)$$

ii. BVSI

The cascaded boost converter and voltage source inverter require total inductor energy storage of 42.54J, which results in total volume and weight of:

$$Vol_{L,BVSI} = \frac{96.9J}{1.79 \times 10^3 \, J/m^3} = 0.0541 m^3 = 54.1 l \qquad (6\text{-}27)$$

$$mass_{L,BMCI} = \frac{96.9J}{0.374 \, J/kg} = 259.1 kg \qquad (6\text{-}28)$$

6.3.4. Inductor specific resistance (Ω/J)

When inductors are utilized for power converters, their design is a balancing act between ac and dc winding losses, mainly due to the proximity effect losses. To evaluate the dc conduction losses, for the power inductors surveyed, the ESR of each part is plotted in Figure 6-23:

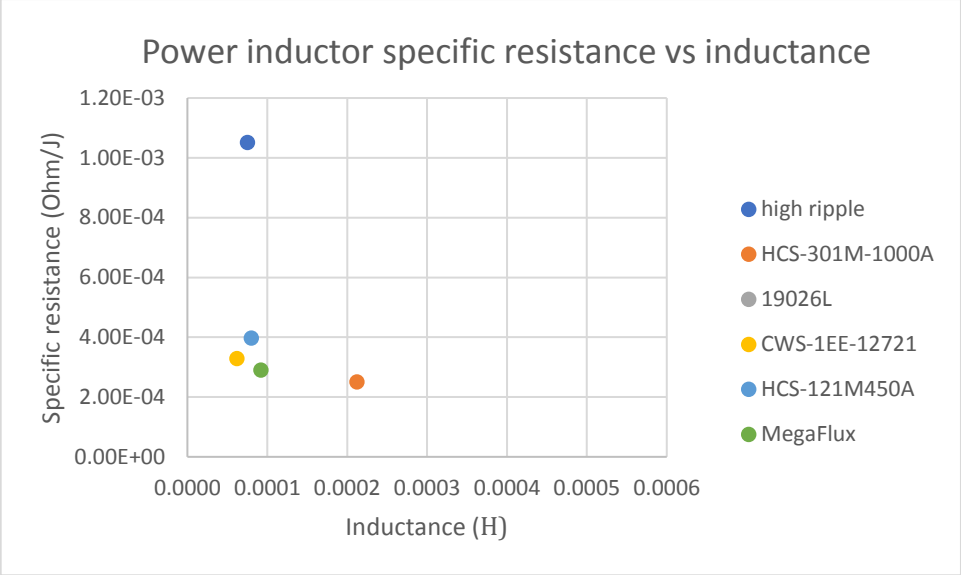

Figure 6-23 Specific resistance as a function of inductance

These values are used to extrapolate the inductor ESR for the efficiency calculations in part 6.3.5.

6.3.5. Converter design values, efficiency, and THD

The efficiency of each converter has been calculated by simulating the converter and measuring the dc-side and ac-side voltages and currents. As the 3-phase voltage has a switching component, a low-pass filter is used to calculate the average value of the efficiency.

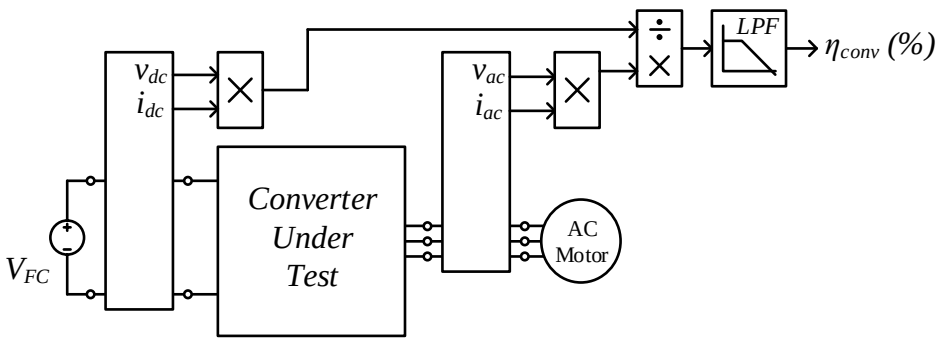

Figure 6-24 Converter efficiency measurement setup

6.3.5.1. BMCI

i. Designed BMCI

The BMCI design values are summarised in Table 6-5, and the converter schematic is shown in Figure 6-25. The inductor properties are extrapolated from the values for part CWS-1EE-12721:

Table 6-5 Designed BMCI values

Parameter	**BMCI value**
Sub-modules per arm	*2*
Power transistor module	*FF300R07ME4_B11*
Total number of switches	*48*
Converter legs/phases	*3*
Transistor switching frequency	*4kHz*
Sub-module capacitor	*069.416.85, 4off 2.35mF 320V*
Leg/phase dc current	*250A*
Leg inductor	*High flux, 62µH @ 280A, 4mΩ*

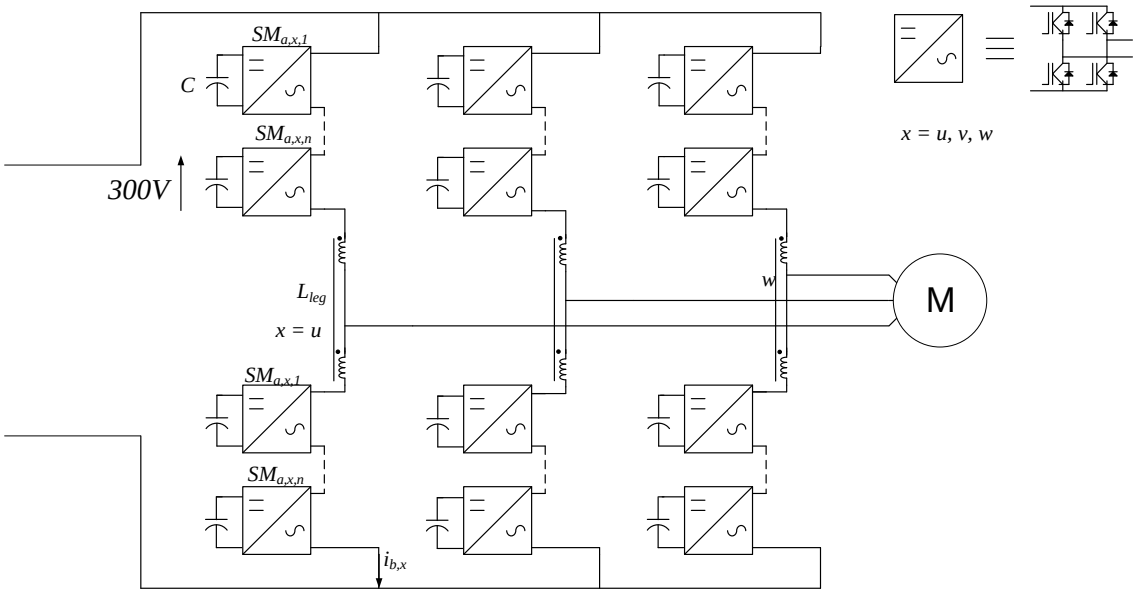

Figure 6-25 Simulated BMCI

ii. BMCI loss modelling

The BMCI numerical simulation model considers conduction losses in the power inductors, sub-module capacitors, and semiconductor switches, as well as transistor switching loss. Power inductor ac-resistance and core losses are not accounted for, as there is no data available from the manufacturers surveyed. Transistor and diode conduction losses are modelled as an ideal voltage source in series with a parasitic resistance, while the switching losses are modelled as a controlled current source, in parallel with the sub-module capacitor. A simplified diagram is shown in Figure 6-26:

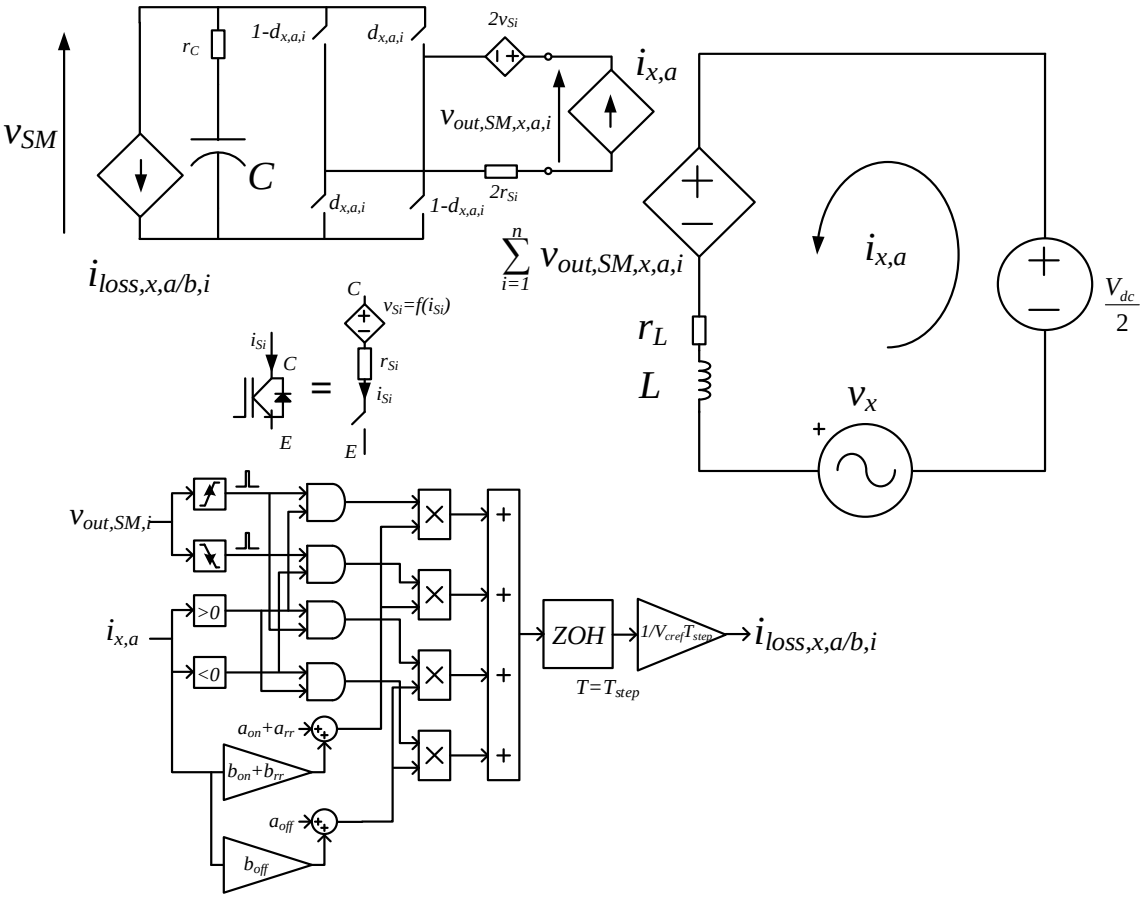

Figure 6-26 Lossy BMCI model for a top arm with IGBT switches.

The sub-module switching loss equivalent current $i_{loss,x,a/b,I}$ is simulated as current pulses, scaled by the switch current, and triggered by a rising or a falling edge of the sub-module ac-side voltage $v_{out,SM,x,a/b,i}$. The transistor and diode conduction loss are accounted for by an equivalent semiconductor resistance and a controlled voltage source v_{Si}:

$$v_{Si} = sign(i_{Si}) \times V_{sat} \qquad (6\text{-}29)$$

, where i_{Si} is the semiconductor switch current, and V_{sat} is the junction saturation voltage, which is assumed to be equal for the IGBT and the diode.

To simplify the simulation of the switching losses, instead of a quadratic fit the switching energies are approximated as offsets and proportional scaling factors:

$$i_{loss,x,a/b,i}(t) = \frac{a_{on} + a_{rr} + i_{x,a/b,i}(b_{on} + b_{rr})}{V_{CE,ref}} T_{step} \quad v_{out} \uparrow, i_{x,a/b} > 0 \, or \, v_{out} \downarrow, i_{x,a/b} < 0 \qquad (6\text{-}30)$$

$$i_{loss,x,a/b,i}(t) = \frac{a_{off} + i_{x,a/b,i} b_{off}}{V_{CE,ref}} T_{step}, v_{out} \uparrow, i_{x,a/b} < 0 \, or \, v_{out} \downarrow, i_{x,a/b} > 0$$

$$a_{on}(i_{x,a/b}) = E_{on}(0)$$
$$b_{on}(i_{x,a/b}) = \frac{E_{on}(I_{CE,ref}) - E_{on}(0)}{I_{CE,ref}} \qquad (6\text{-}31)$$

$$a_{rr}(i_{x,a/b}) = E_{rr}(0)$$
$$b_{rr}(i_{x,a/b}) = \frac{E_{rr}(I_{CE,ref}) - E_{rr}(0)}{I_{CE,ref}} \qquad (6\text{-}32)$$

$$a_{off}(i_{x,a/b}) = E_{off}(0)$$
$$b_{off}(i_{x,a/b}) = \frac{E_{off}(I_{CE,ref}) - E_{off}(0)}{I_{CE,ref}} \qquad (6\text{-}33)$$

, where E_{on} is the turn-on energy, E_{off} is the turn-off energy, and E_{rr} is the diode reverse recovery energy, which can be found in most device datasheets. The coefficients a_{on}, a_{rr} and a_{off} are the intersection between the loss curve and the *y-axis*, while b_{on}, b_{rr} *and* b_{off} are the proportional coefficient that account for the losses' dependency on switch current. $V_{CE,ref}$ and $I_{CE,ref}$ are the collector-emitter voltage and collector current used in the manufacturer's tests, and T_{step} is the discrete time step used in the numerical simulation.

The simulated BMCI efficiency was measured to be $\boldsymbol{\eta_{BMCI} = 92.5\%}$. Of the pproximately 13kW losses, 11.1kW are semiconductor conduction losses, 900W are switching losses, and the remaining 1kW is losses in inductors and the capacitors.

iii. BMCI Weighted Total Harmonic Distortion

The WTHD level was simulated at rated power with frequency ratio of 36 for both the BMCI converter and the BVSI system, resulting in electrical frequency of roughly 111Hz.

The BMCI line-to-line voltages, and phase currents, are show in Figure 6-27:

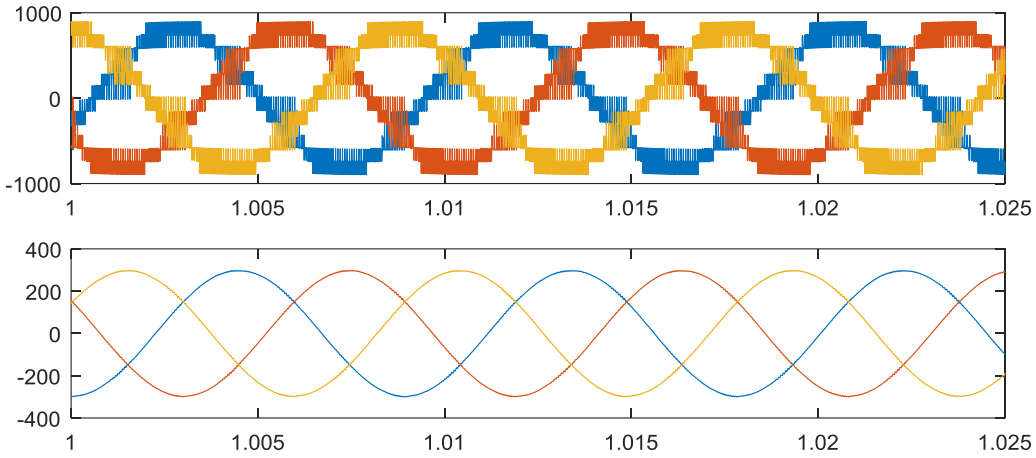

Figure 6-27 BMCI phase-to-phase voltages and line currents

The phase-to-phase voltage WTHD was measured to be $WTHD_{BMCI} = 0.4\%$.

6.3.5.2. BVSI

i. Designed BVSI

The designed BVSI parameters are summarized in Table 6-6. The inductor is extrapolated from the part HCS-301M-100A.

Table 6-6 Designed BVSI values

Parameter	**BVSI value**
Inverter transistor module	*FF300R12ME4B11*
Boost converter module	*FD400R12KE3*
Total number of switches	*10*
Converter legs/phases	*2*
Leg/phase inductance	*500μH*
Transistor switching frequency	*4kHz*
Sub-module/dc-link capacitance	*385.416.85, 1.15mF@850V*
Leg inductor	*Iron Powder, 570μH @ 412A, 6mΩ*

ii. BVSI loss modelling

The simulated BVSI losses are simulated the same way as in the BMCI case, with the switching loss current being drawn from the dc-link reservoir capacitor, shown in Figure 6-28:

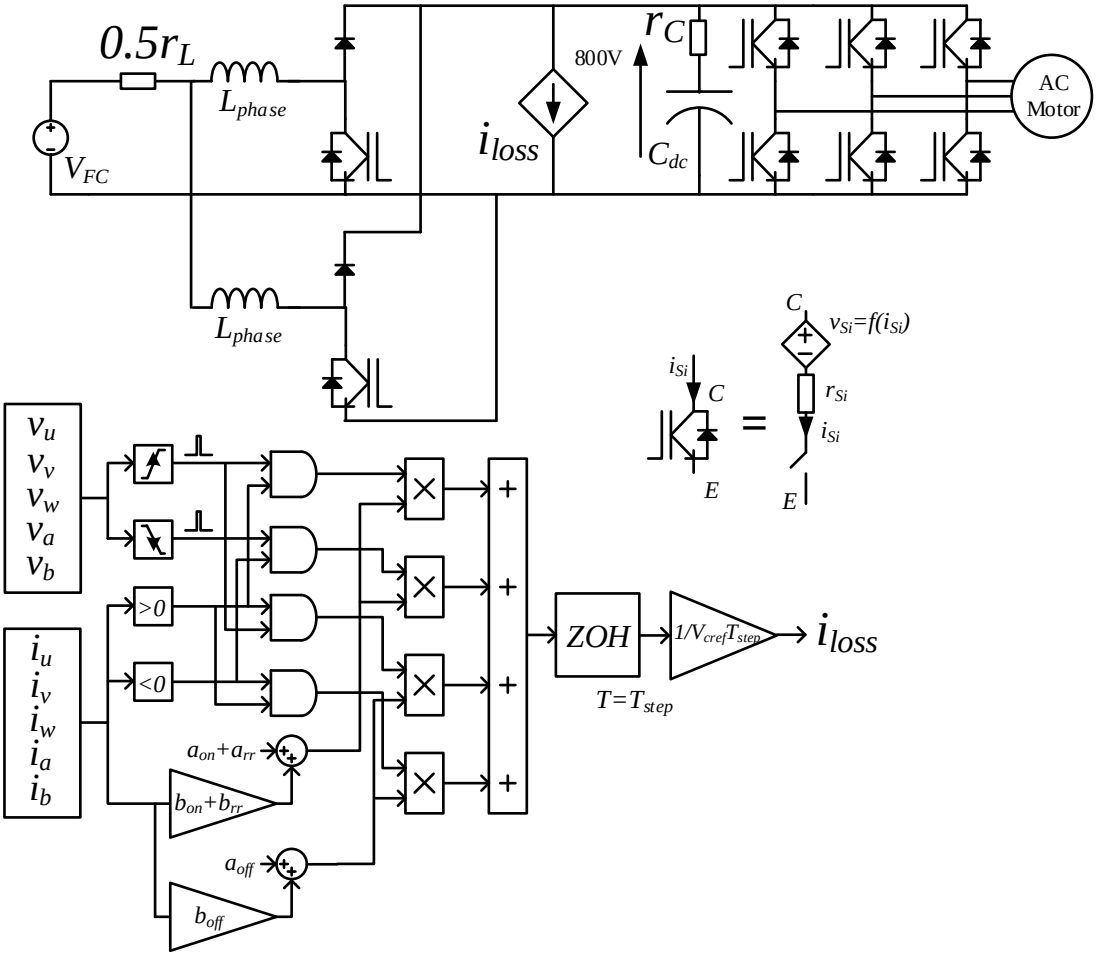

Figure 6-28 BVSI model including conduction and switching losses

The simulated BVSI efficiency was measured to be η_{BVSI}**=97.0%.** The approximately 5.2kW loss breaks down into 1.1kW of switching losses, 3kW of inductor loss, and the remaining 1.1kW is attributed to

iii. BVSI weighted total harmonic distortion

The 2-level voltage source inverter was measured to be $WTHD_{BVSI}$ *= 1.5%*, which results in higher machine ripple current. The BVSI ac-side voltages and currents are shown in Figure 6-29:

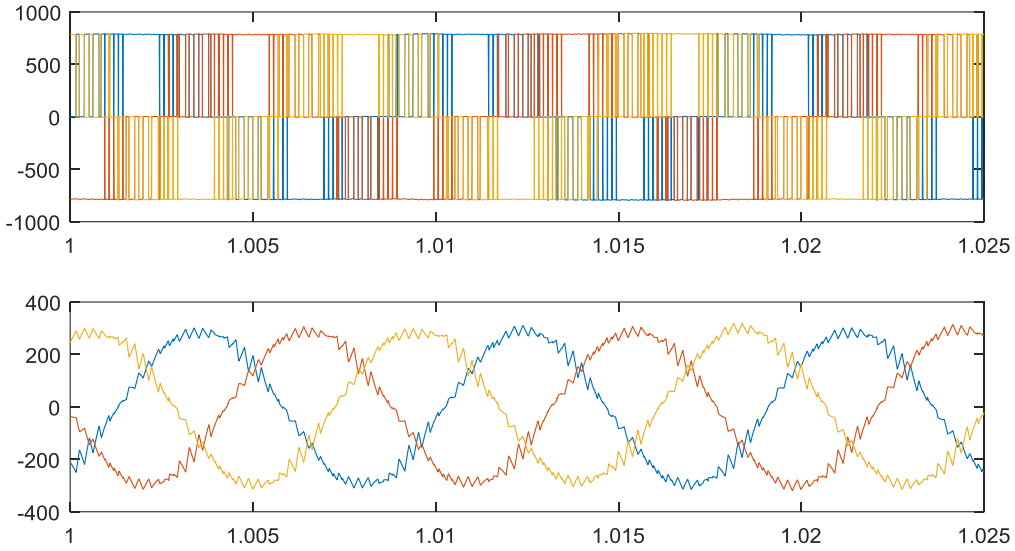

Figure 6-29 BVSI phase-to-phase voltages and line currents

6.3.6 Summary of the comparison

The results of the comparison show that the BMCI's inductors are much smaller than the BVSI ones, even though the required capacitance is much larger. Therefore, the BMCI system total energy storage components are smaller and considerably lighter, fulfilling one of the most stringent requirement of traction systems. The main drawback of the BMCI is its lower efficiency at full load, resulting in a larger cooling system that would partly reduce the gains of smaller energy storage components. The much lower machine WTHD achieved with the BMCI is expected to improve machine efficiency. However more work is required to conduct an analysis at a system level.

The resultant parameters of the two converters are summarised in Table 6-7.

Table 6-7 Comparison between simulated BMCI and BVSI

Parameter	Symbol	BMCI	BVSI
Switch rating	$S_{sw,total,}$	*4.57MVA*	*2.58MVA*
Capacitor energy	$W_{C,total}$	*5.4kJ*	*352J*
Capacitor volume	$Vol_{C,total}$	*27l*	*1.1l*
Capacitor mass	$mass_{C,total}$	*27.6kg*	*1.28kg*
Inductor energy	$W_{L,total}$	*7.03J*	*42.5J*
Inductor volume	$Vol_{L,total}$	*7.33l*	*39l*
Inductor weight	$mass_{L,total}$	*21.3kg*	*91.29kg*
Energy storage volume	Vol_{C+L}	*34.33l*	*40.1l*
Energy storage mass	$mass_{C+L}$	*48.9kg*	*92.57kg*
Efficiency	η	*92.5%*	*97.0%*
THD	*WTHD*	*0.4%*	*1.5%*
System complexity		*HIGH*	*LOW*

6.4. SUMMARY

This chapter has presented a numerical model for a fuel cell tram with a BMCI induction motor drive. The converter is put through a traction cycle to demonstrate operation in all modes required for an electric vehicle: constant torque, constant power, and regenerative braking. The converter operates at output frequencies from 0 to beyond rated speed, with a constant current amplitude in the linear power range, and with constant I_q component in the field weakening region.

To get a better understanding of how a BMCI compares to a state-of-the-art solution, a BVSI system is also designed and simulated. The two converters are then compared in terms of energy storage volume and weight, total switch apparent power needed,

efficiency, and harmonic distortion. The BMCI is shown to have the advantage of significant reduction in energy storage component weight and electric motor current WTHD, which can reduce the chance of machine insulation failure and increase its efficiency. The main disadvantage is the lower peak efficiency, although a more accurate analysis would be needed to evaluate the impact on the total energy lost in a practical traction cycle and the actual average thermal load of the cooling system.

Chapter 7. EXPERIMENTAL VALIDATION

This chapter presents experimental data from the prototype BMCI. Initial tests have been carried out without feedback of currents or voltages, to validate the basic working principle and verify the boost characteristics. The converter has been then connected to an induction motor to demonstrate operations over the full speed range required by an electric vehicle, with the converter's ac-side RMS voltage higher than the dc source. The schematic of the prototype converter is shown in Figure 7-1.

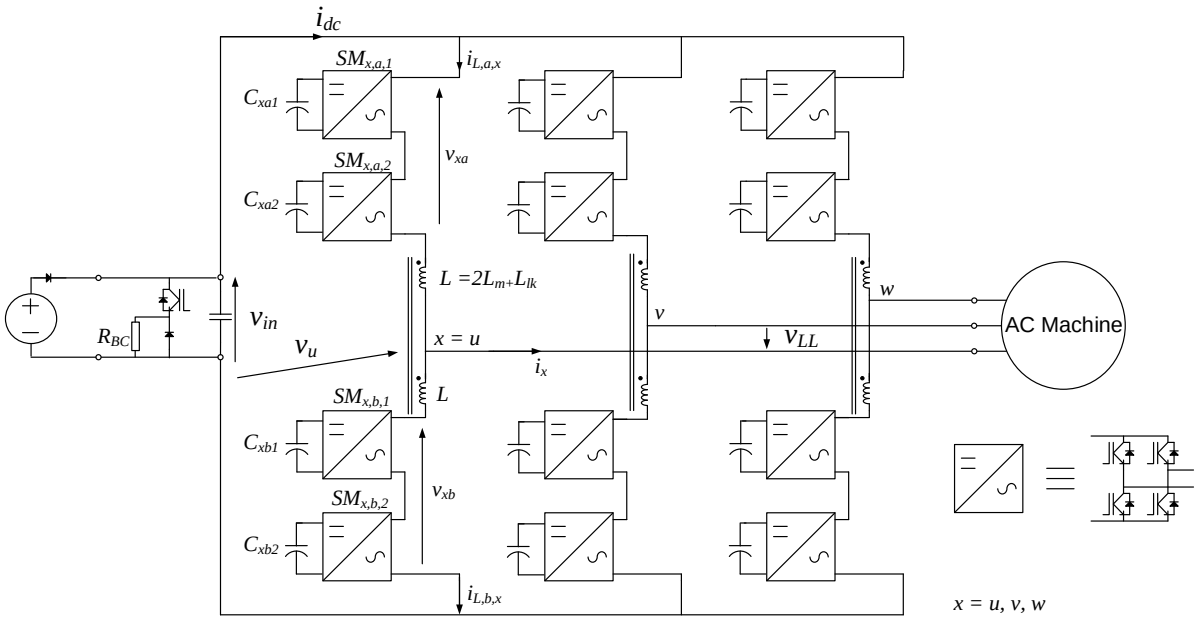

Figure 7-1 Schematic of prototype BMCI

The dc-source voltage v_{dc} is varied between different tests to avoid the bench power supply going into power limitation mode. Open-loop tests examine the maximum boost characteristics and at very low dc duty cycle the dc-side current is limited by the power supply current limit, output load, and converter parasitic resistances. When the converter is used with the induction motor, the dc-side voltage can be raised, as the maximum dc source power can be controlled by adjusting the machine base frequency for field

weakening mode. A photograph of the hardware setup, showing the converter, OPAL-RT controller, induction machine rig, and variac, is shown in Figure 7-2.

Figure 7-2 Final setup of the converter prototype with a variac load, induction motor load, and dc power supply.

7.1. OPEN LOOP CONTROL WITH PASSIVE LOAD

To check the basic operations of the prototype converter, initial tests were carried out with open loop control – a fixed duty cycle d_{dc}, fixed output frequency f_{out}, and fixed amplitude of the ac duty cycle d_{ac}. The only closed-loop controller that a modular cascaded converter requires is the arm-balancing algorithm that ensures all capacitors, within the same arm, have equal voltages.

The converter feeds a passive resistive load, connected in delta configuration. To achieve a variable load, the resistors are connected to the converter by a 3-phase variable auto-transformer. The variac is configured so that the load voltage/converter dc to ac-side voltage ratio, G_{variac} can be varied between 0 and 100%. At 0% the only load seen by the converter is the variac magnetising inductance, which corresponds to a minimum load. Maximum load is achieved when the autotransformer output is set for 100%, in which case the per-phase resistance seen by the converter is equal to a third of the power resistors, or 1.867Ω.

7.1.1. Initial validation of the basic operations of the converter

For this part of the experiment, the converter waveforms are examined in 3 cases of d_{dc}: *0.3*, *0.5*, and *0.*1. For each case the load is adjusted to achieve output current amplitude of *2A* peak. To avoid core saturation of the variac, the output frequency f_{out} is set to 208.33Hz. The value was chosen to get an integer number of PWM pulses per cycle. With a switching frequency $f_{carrier}$ of 5 kHz per transistor, the frequency ratio, $f_{carrier}/f_{out}$ is equal to 24. However, the effective switching frequency is 4 times higher, as the sub-module carriers are interleaved.

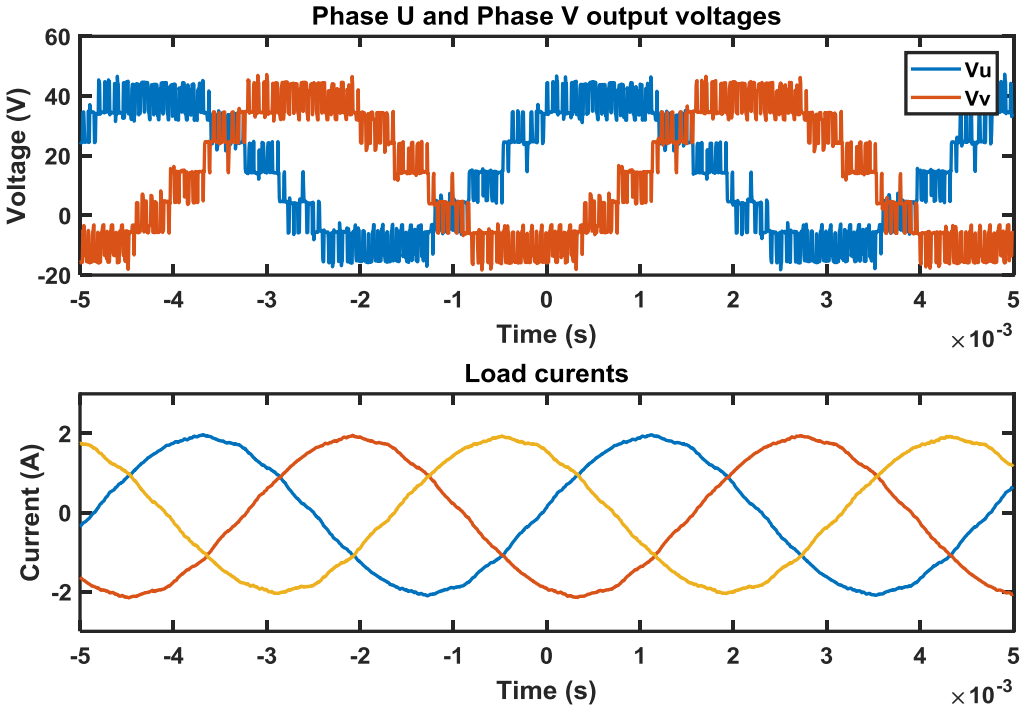

Figure 7-3 Converter phase voltages, referenced to power supply 0V, and output currents

Figure 7-3 shows the converter running with $d_{dc}=0.3$, $d_{ac}=0.7\times\sin(2\pi\times208.33\times t)$, and $G_{variac}=0.325$. The variac leakage inductance, together with the changed ratio of passive resistance to inductance, can clearly be seen, as the switching harmonics are not visible and the current waveform, and the currents have considerable displacement angle. As the dc-side power supply is fixed at 30V the BMCI is operating with a low voltage-boost factor $G_v=V_{ll,RMS}/V_{in}=1.2$. The primary reflected load resistance is calculated using (7-1), and is equal to 16.25Ω.

$$R_{load}'=\frac{R_{load}}{G_{variac}} \qquad (7\text{-}1)$$

The oscilloscope capture shows the output phase voltages *Vu,* and *Vv.* The voltages are offset by one half of the dc-side voltage, 15V, and a total of 7 levels can be seen, with a step of about 12V. The arm voltages of phase *u*, as well as the arm currents, are shown in Figure 7-4 and the average capacitor voltage was measured to be about 22V, by compensating

for the IGBT saturation voltage drop. Each arm can produce 4 switching levels at maximum modulation index. These results conform to the predictions made in Chapter 5.

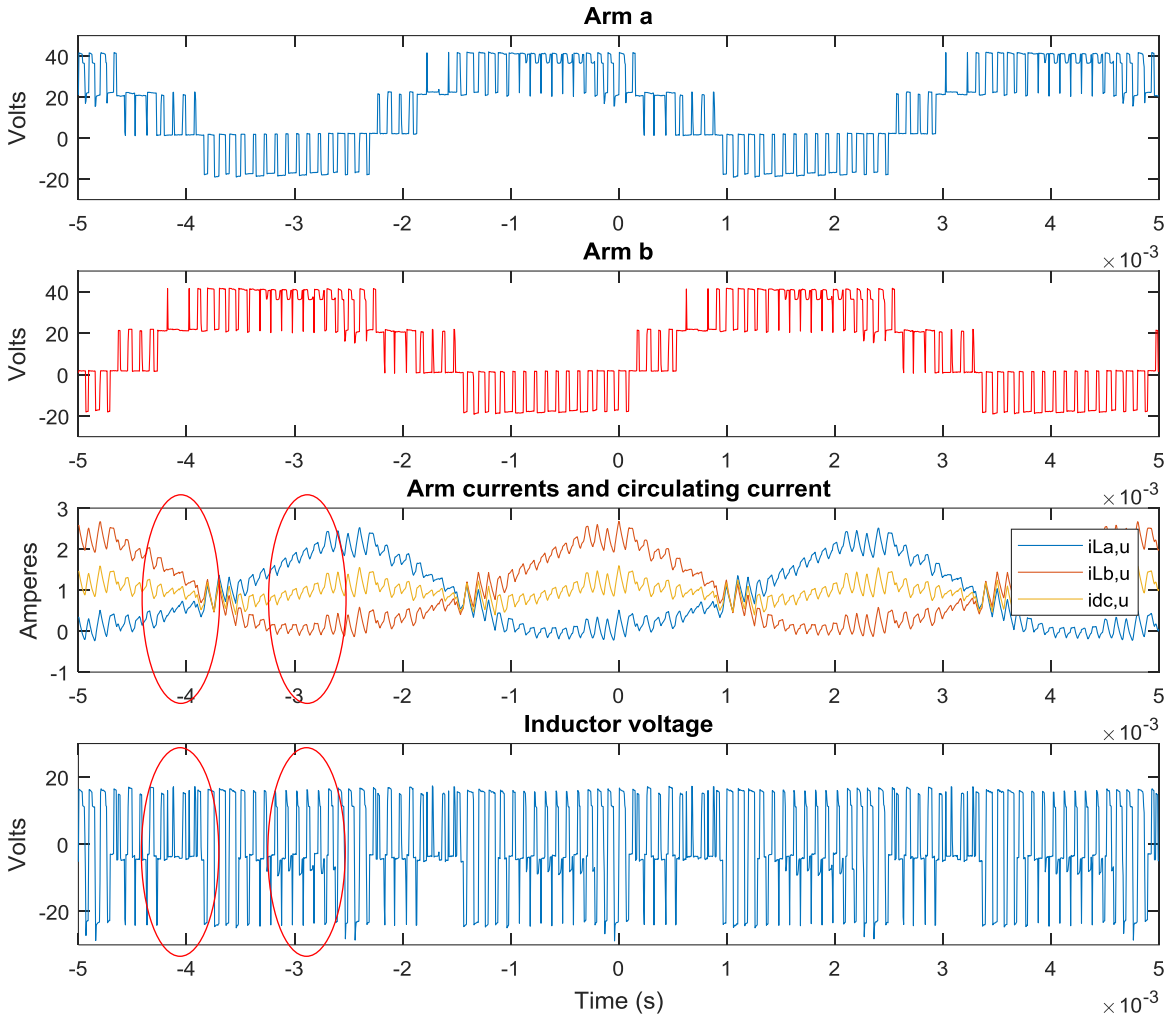

Figure 7-4 Arm voltages and currents at d_{dc}=0.3, with maximum current ripple

In Figure 7-4 the arm currents are composed of a dc component, a fundamental harmonic and a second harmonic that is clearly visible in the circulating current.

The peak current ripple occurs when edges of the top and bottom arm switching waveforms align. At these intersections the leg inductor waveform switches at frequency $f_{sw,eff}=n\times2\times f_{carrier}$ and has a voltage step equal to $2\times V_C$. This can be observed in Figure 7-4, at every crossing and peak of an arm current waveform. It should be noted that the arm current peaks do not align with the peak voltage, as the load is inductive.

The next step looks at the converter operating at $d_{ac,max}=d_{dc}$. In this condition, the BMCI operates as a conventional buck MCC. As the carrier shift is 0 between the two arms, the pulses at the phase terminal align and the voltage step is equal to V_C, with operation equivalent to a conventional 3-level inverter. The voltage waveforms and ac-side currents can be seen in Figure 7-5.

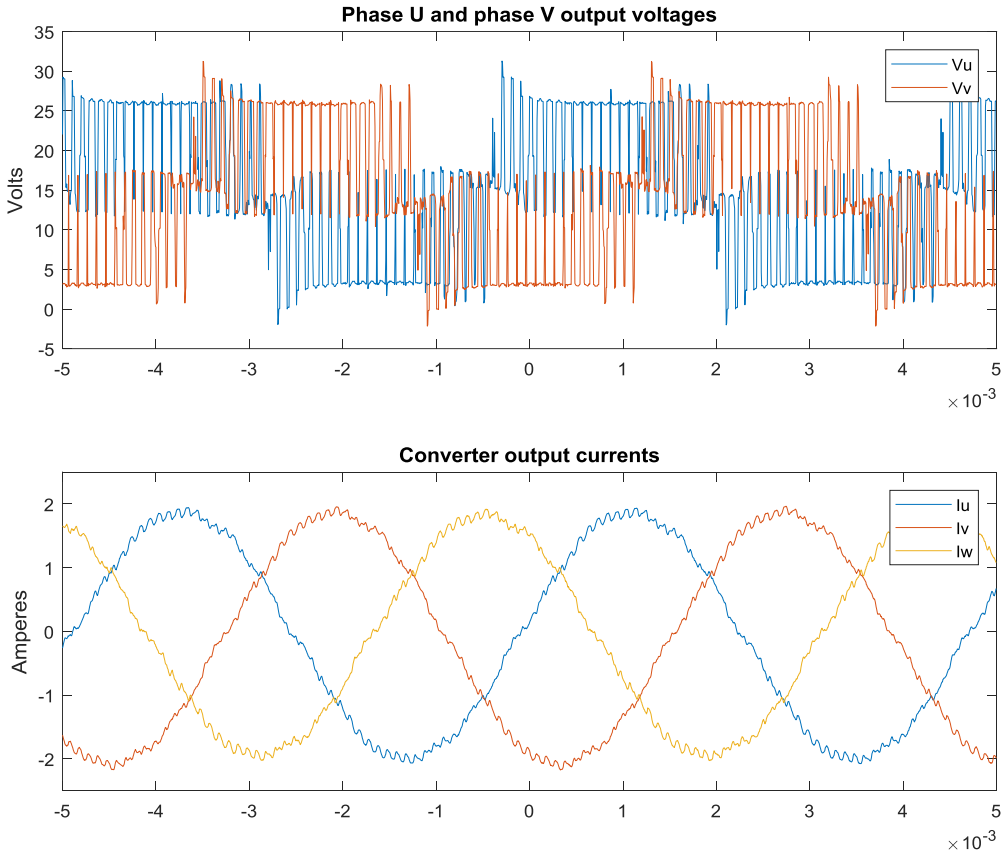

Figure 7-5 Converter phase voltages, referenced to power supply 0V, and output currents, at $d_{dc}=0.5$

The low number of voltage levels causes a higher ac-side current ripple, compared to the case of $d_{dc}=0.3$. However, the dc-side current ripple is lower as every rising edge from the top arm should be matched by a falling edge in the bottom arm, and vice versa. In practice, this condition cannot be guaranteed, as differences in capacitance between the sub-modules will cause different instantaneous duty cycle for each module, to maintain equal voltage. In addition, the top and bottom arm voltages are not equal at all times, and,

even with a perfect edge match, there will be a small voltage applied across the inductor. This can be observed in Figure 7-6, specifically between *t=-3.5ms* and *t=-2.5ms,* and every fundamental half-cycle afterwards.

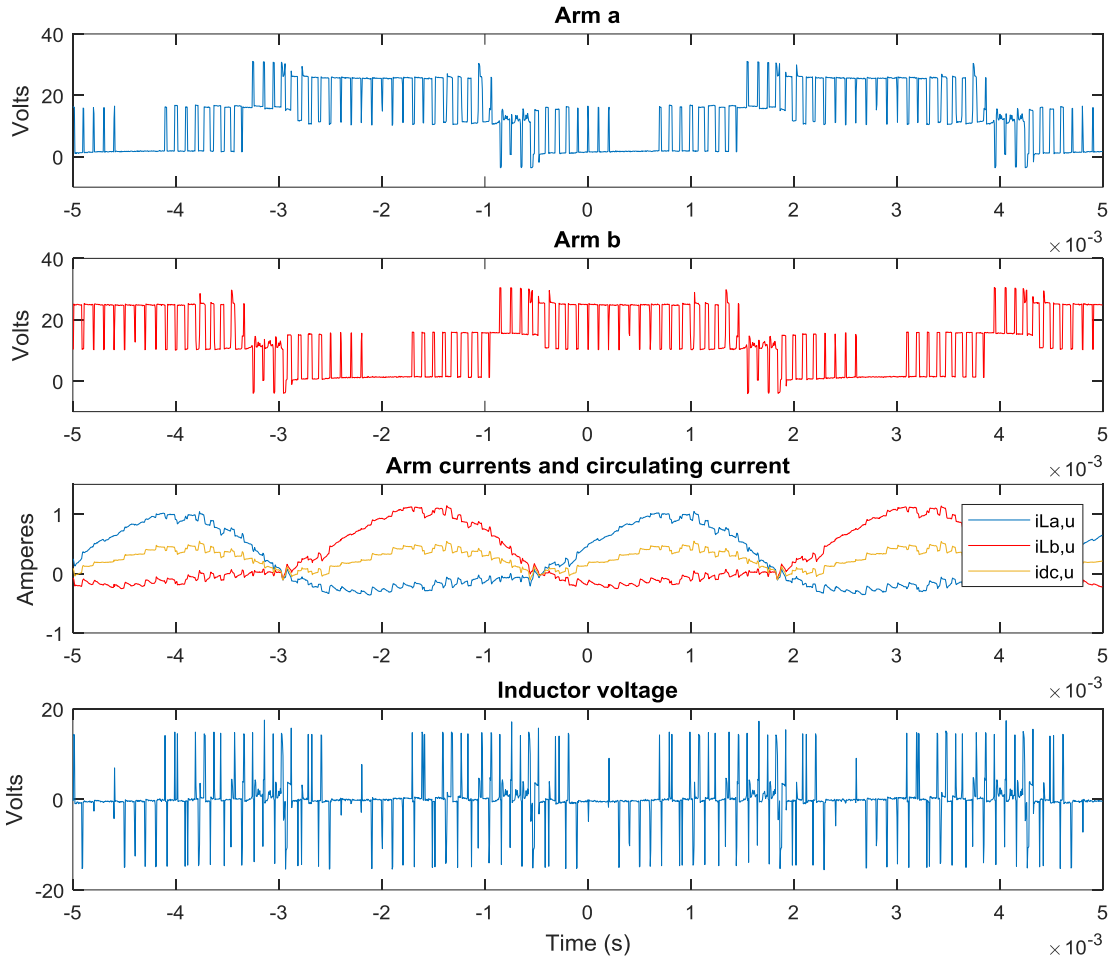

Figure 7-6 Arm voltages and currents for d_{dc}=0.5

The circulating current's switching ripple is only visible at the peaks of the arm currents. The voltage spikes in the inductor voltage waveform are due to the arm voltage balancing controller. This effect depends on the direction of current flow, and the polarity of the arm voltage. Investigation of this effect is left for future work as the pulses have very low volt-seconds and have a negligible impact on ripple current.

When the converter is pushed into a deeper boost, with $d_{dc}<1/2n$, the converter achieves the maximum possible number of output steps, as the modulation signal will pass through all carrier levels.

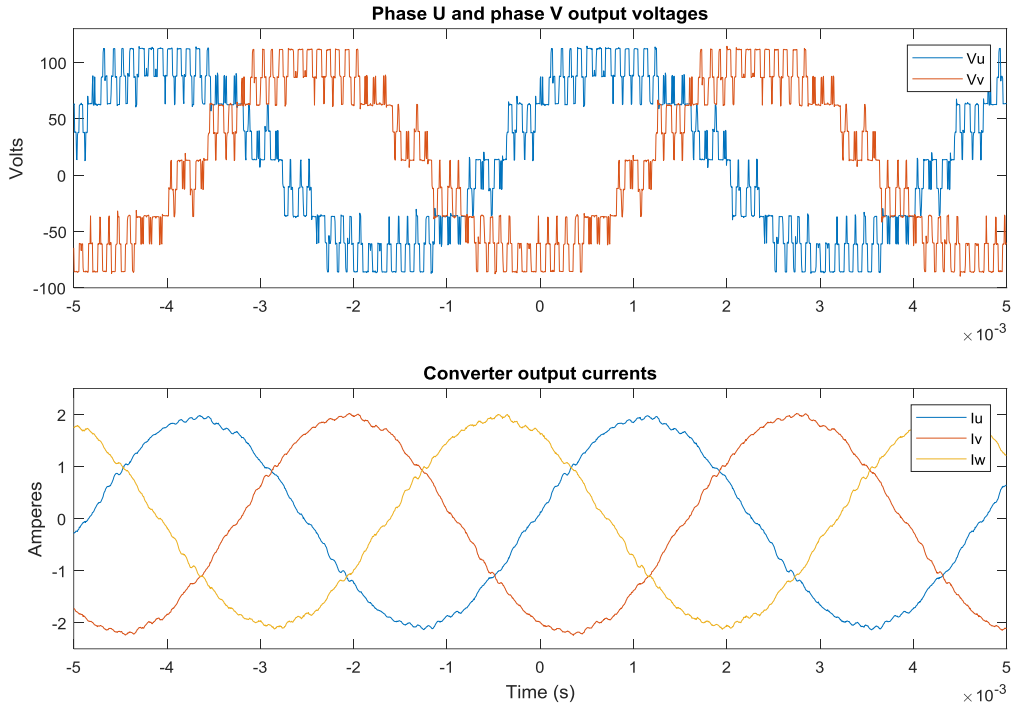

Figure 7-7 Converter phase voltages, referenced to power supply 0V, and output currents, at d_{dc}=0.1

Under these conditions the BMCI produces phase waveform with 9 voltage steps of $½×V_c$, but in most regions the voltage is switching between 3-states. The arm voltages have 5 levels, cycling from $-2V_C$ to $+2V_C$. The arm voltages, currents, and inductor voltage are shown in Figure 7-8. The inductor waveform's switching frequency is either $8×f_{carrier}$ or $4×f_{carrier}$, depending on the value of the modulated ac signal, with peak ripple current occurring when a rising edge from the top arm coincides with a rising edge from the bottom arm and the inductor voltage has a step of $2V_c$. The other condition for high ripple current is also visible, between t=-3.5ms and t=-3ms, where only one of the two switching edges coincide, and the top and bottom arm pules are back-to-back. At this point the voltage steps is only V_C, but the switching period is $T_{SW}=1/4f_{carrier}$.

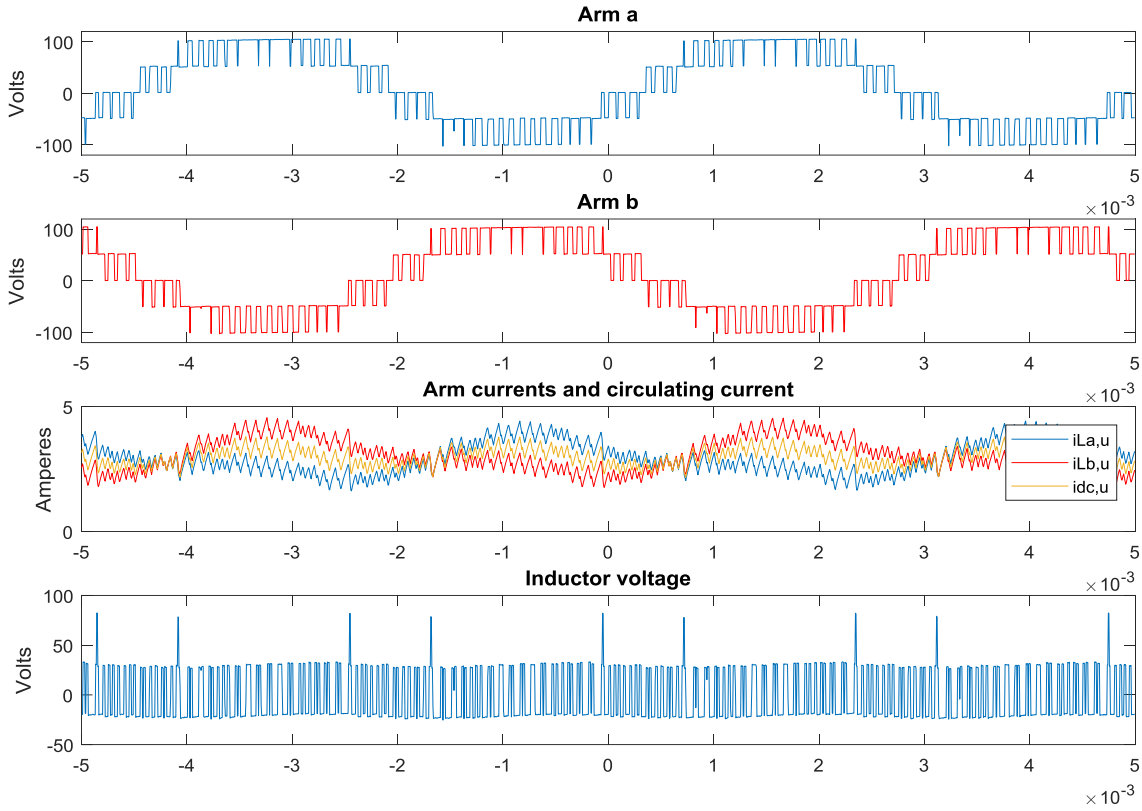

Figure 7-8 Arm voltages and currents for ddc=0.1

As the boost ratio is G_V=*3.833*, the arm currents are always positive, and each arm discharges when the inserted voltage is negative, regardless of current displacement angle.

7.1.2. Maximum boost characteristics

To investigate the maximum boost ratio of the converter the load resistance and dc-side voltage are held constant, while the d_{dc} is cycled from 0.075 to 0.6. The amplitude of d_{ac} is always equal to *1*-d_{dc}.

Table 7-1 Experimental setup parameters for deriving maximum boost characteristics

Parameter	Symbol	Test value
Dc-side voltage	V_{dc}	30 V
Autotransformer output ratio	G_{variac}	0.2
Primary reflected load resistance	R_{load}'	47 Ω
Device switcihg frequency	$f_{carrier}$	5 kHz
Bottom arm carrier phase displacement	$\vartheta_{carrier}$	0
Output frequency	f_{out}	208.33 Hz

A sweep of d_{dc} from 0.075 to 0.60 can be seen in Figure 7-9 through Figure 7-11, demonstrating both ac-side voltage boost and buck. Maximum ac voltage is achieved with $d_{dc}=0.075$, i.e. the smaller the dc duty cycle, the higher the gain. The data shows the line-to-line voltage V_{ll}, dc voltage V_{dc}, and floating capacitor voltage V_{cap}.

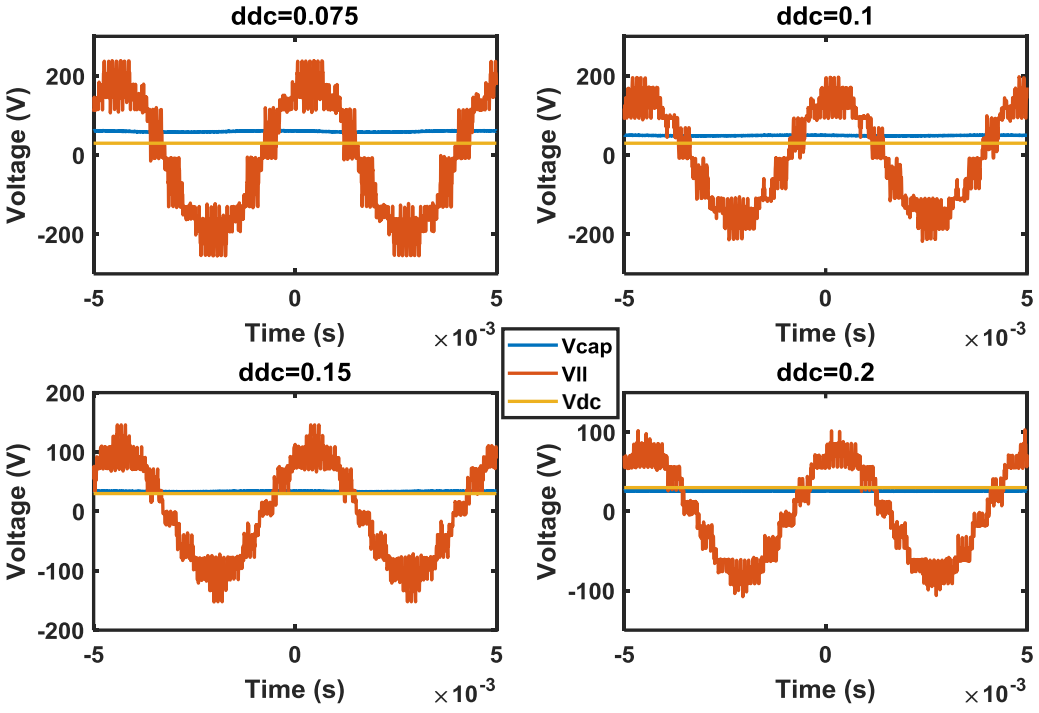

Figure 7-9 Sub-module capacitor voltage, line-to-line voltage, and dc-side voltage for d_{dc}=0.075 through 0.2

For values of $d_{dc}<0.2$ the submodule capacitor voltage is larger than the dc-side voltage, which is specific to the particular number of submodules per arm. With these low duty cycle values, the modulated ac waveform's zero-crossings are close to 0, which is one point where minimum dc-side current ripple occurs. As discussed in Chapter 5, achieving the minimum dc-side current ripple, and utilizing the maximum converter number of output levels, are mutually exclusive conditions. It is expected for the number of discrete levels to increase, as the duty cycle approaches 0.25. This can be observed in Figure 7-10. It may appear that at $d_{dc}=0.3$ the ac-side waveform is cleaner, but what may look like measurement noise is in fact pulses that skip to a neighbouring level.

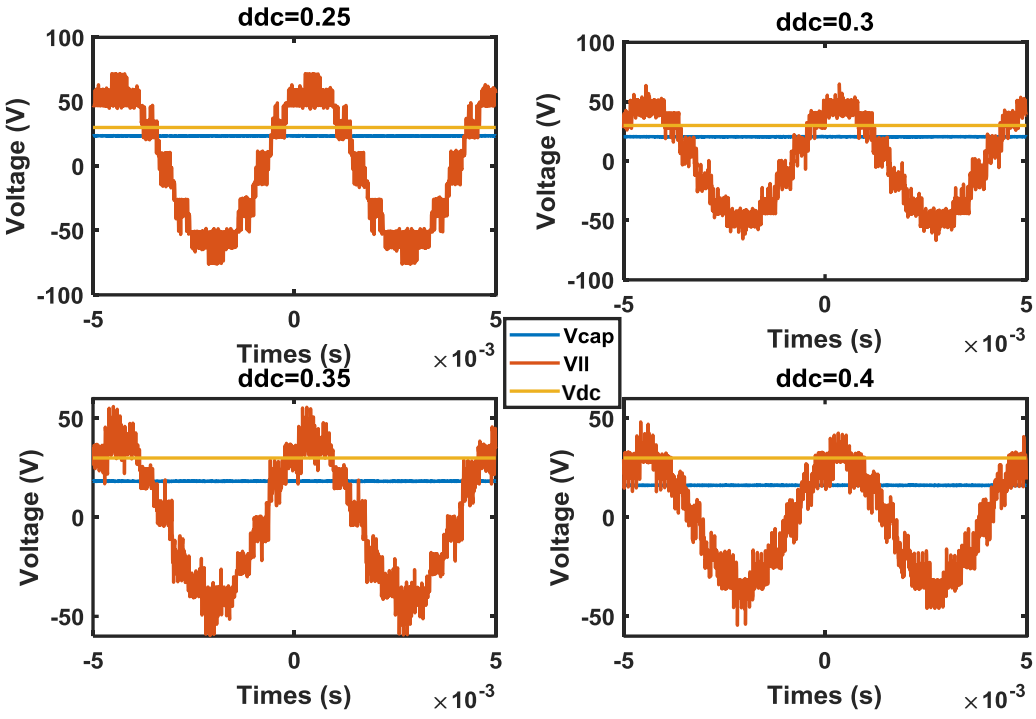

Figure 7-10 Sub-module capacitor voltage, line-to-line voltage, and dc-side voltage for ddc=0.25 through 0.4

As the duty cycle approaches another point of minimum dc-side current ripple, $d_{dc}=0.5$, the number of ac-side voltage levels reduces, and the line-to-line voltage has more pulse alignments, thus having less defined voltage levels. This is shown in Figure 7-11:

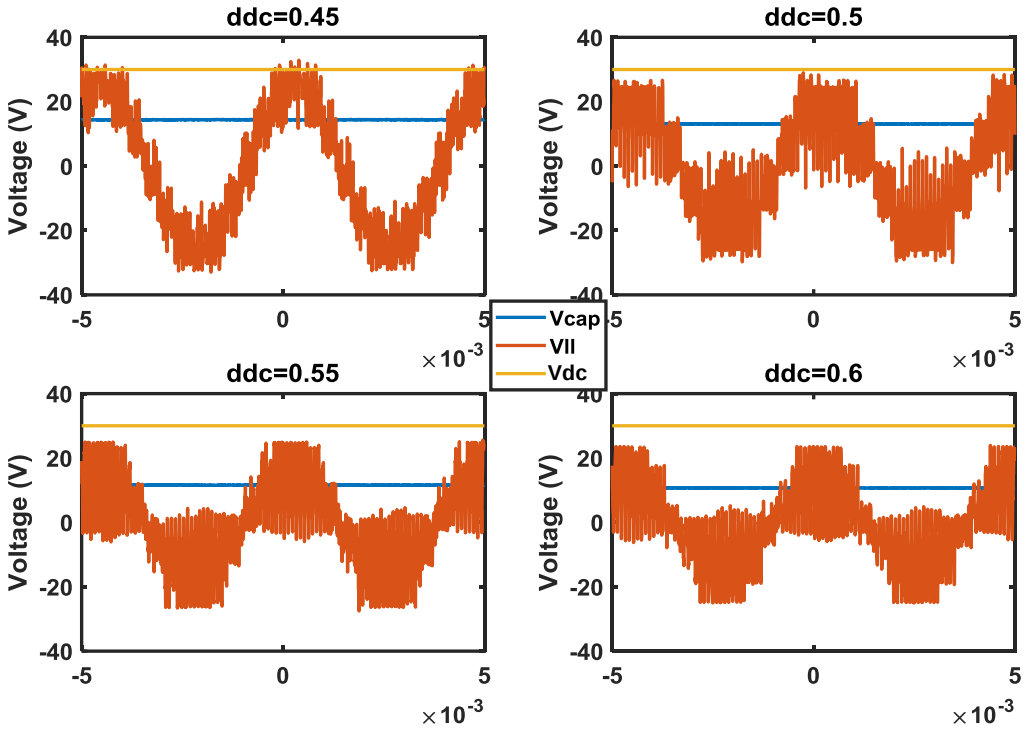

Figure 7-11 Sub-module capacitor voltage, line-to-line voltage, and dc-side voltage for ddc=0.45 through 0.6

The experimental results are compared to the large-signal model and ideal model in Figure 7-12. They show good agreement with the analytical model.

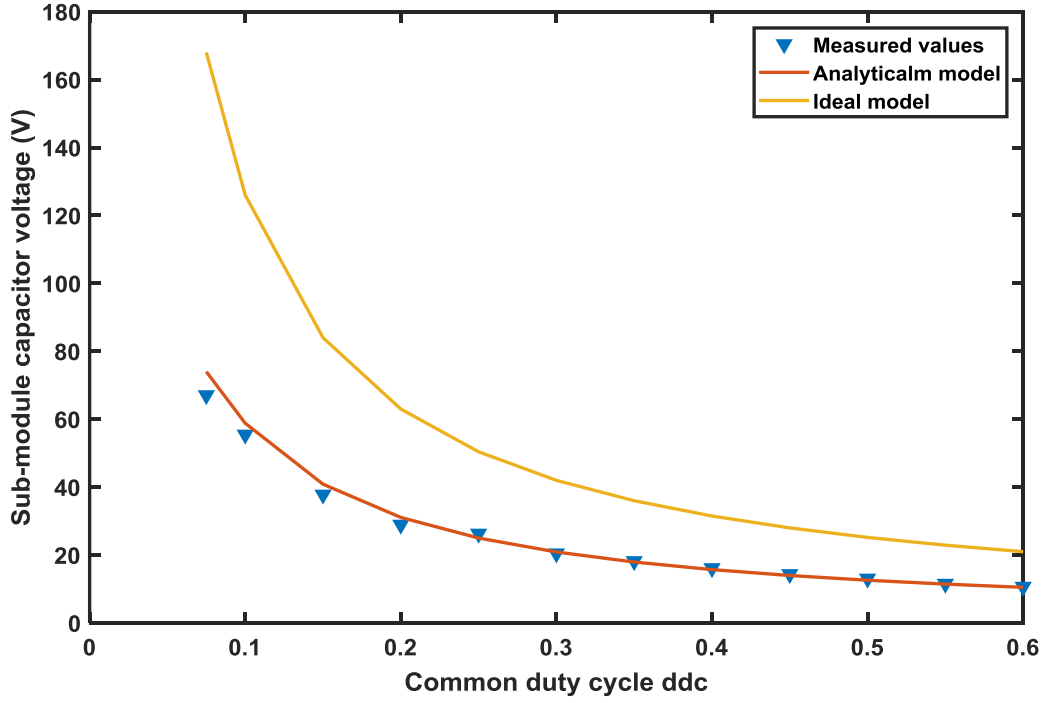

Figure 7-12 Comparison between maximum ac-side voltage boost between hardware prototype and analytical model

The voltage gain is lower than the ideal case, which is due to the voltage drops across the IGBTs, the parasitic resistance of the capacitors, and the internal impedance of the voltage source. With two arms connected in series and two devices per sub-module always conducting at the same time, assuming $v_{FWD}=v_{IGBTsat}$, the dc-side voltage is reduced by 5.6 V. In the experiment the main reason for keeping the dc-side voltage low is the transistor rating of the braking chopper used for protection is 100 V.

7.2. OPERATION OF INTERNAL CONTROLLERS

For normal operations, the converter requires that the average capacitor voltages are all equal. This condition is maintained by a set of 3 closed loop controllers that undertake the following functions: sub-module balancing, arm balancing, and average leg capacitor balancing. It is important for all of them to function under dynamic conditions and their operations are examined using the traction cycle defined in the previous section.

At the end of the section the converter is tested at low frequency, demonstrating the efficacy of the low-frequency algorithm.

7.2.1. Sub-module balancing controller

Spread in capacitance between different capacitors with the same part number can be as high as 20%. To maintain the sub-module capacitor voltage below a maximum rated value, the duty cycle of each floating capacitor must be slightly different. Figure 7-13 shows the capacitor voltages of two arms.

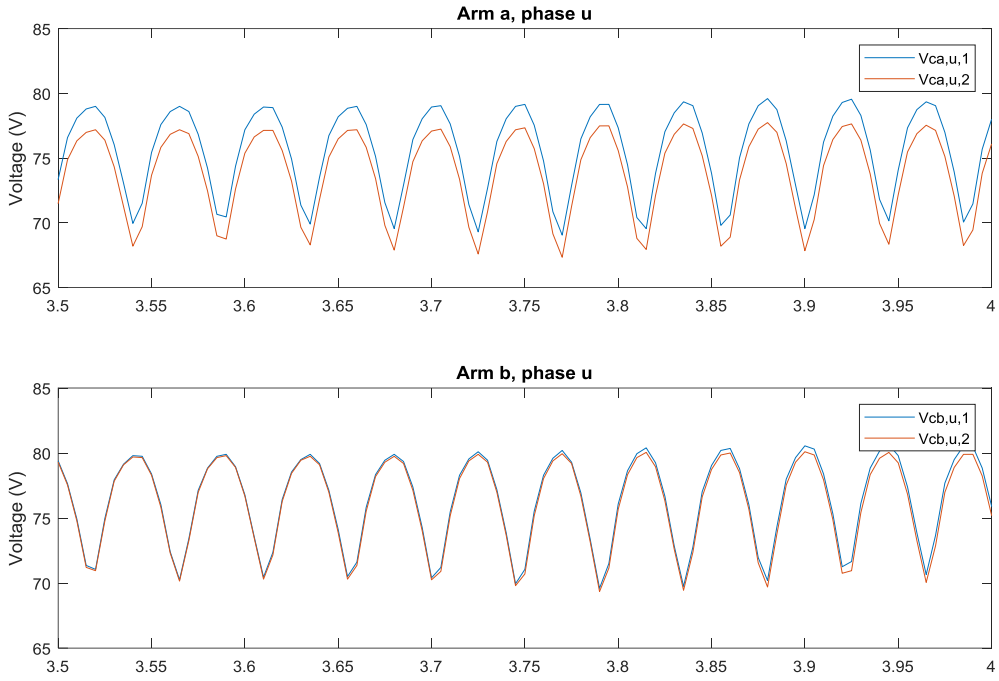

Figure 7-13 Submodule voltages for the top and bottom arm of one converter leg.

The voltages of arm *a* have an offset of about 2 volts. This is due to offsets in the internal voltage transducers as well as the probe used for the measurement.

7.2.2. Arm balancing controller

The arm balancing controller needs to maintain the difference between the top and bottom arm average capacitor voltages equal to 0. They can be observed, during a transient, in Figure 7-14:

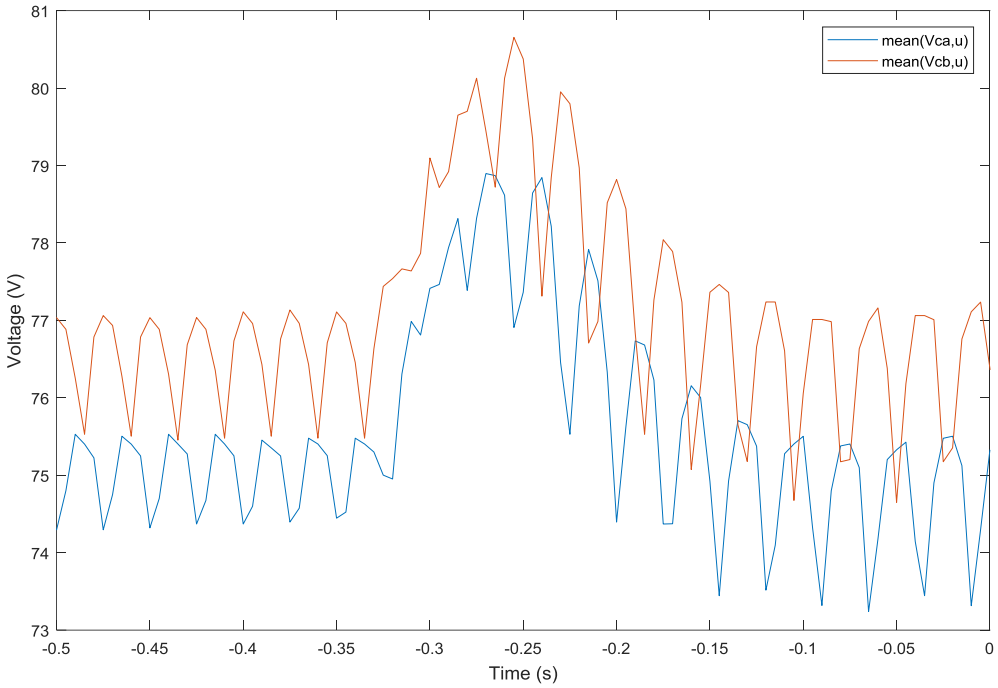

Figure 7-14Average top and bottom arm capacitor voltages during a transient

The offset between the two arms is small, but remains constant, as it is due to measurement errors.

7.2.3. Average leg capacitor voltage regulator

Each arm's voltage regulator maintains the average voltage equal to the reference. This method uses a single controller to maintain both the dc value, as well as achieve balancing between the converter legs. Figure 7-15 shows capacitor voltage before and after a step in the voltage reference from 40V to 60V.

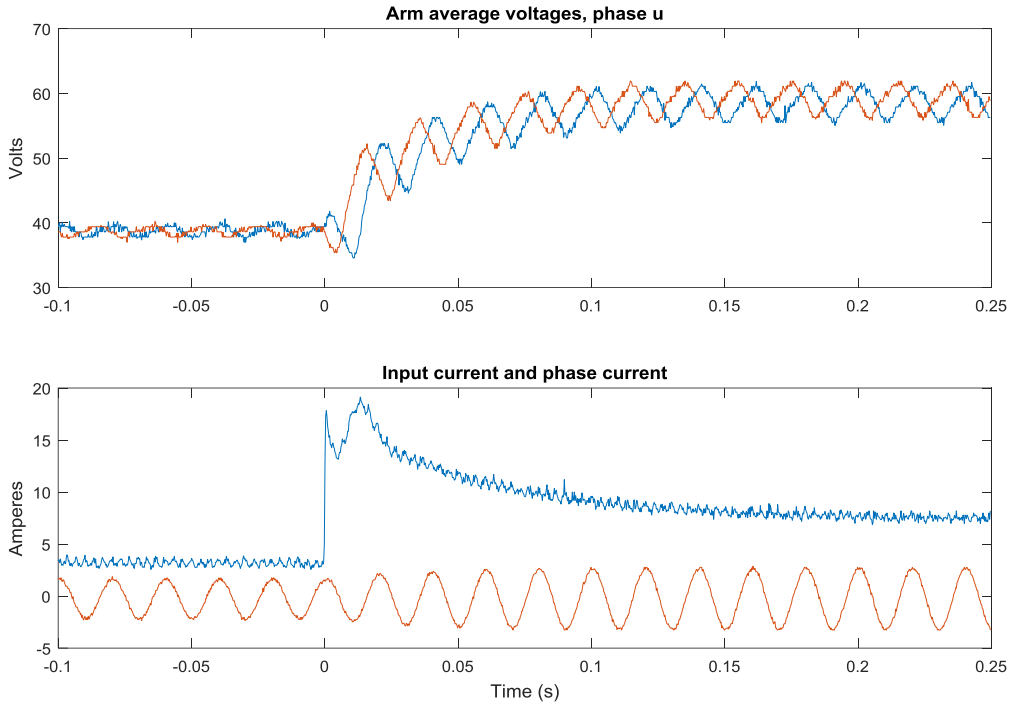

Figure 7-15 Step response of capacitor voltage reference; average arm capacitor voltages (top) and dc-side and phase currents (bottom)

The figure shows the effectiveness of the controller and that it is capable of balancing the sub-module capacitor voltages during a transient. The modulated signal is kept constant at m and the output current increases accordingly. During the initial response the dc power supply goes into current limiting, causing a small oscillation at the start of the transient.

7.2.4. Low-frequency operations

When the converter output frequency falls below 5 Hz the capacitor ripple starts increasing. Without additional measures the ripple can reach an infinitely high value at 0 Hz. As this makes the converter unstable, a capacitor voltage ripple compensator has been introduced. This compensator aims at maintaining the top and bottom arms balanced by inserting a common mode component at 100 Hz. Figure 7-16 shows the transient of sub-module capacitor voltage, converter dc-side current, and phase u output current at start of acceleration, where a step output reference is applied:

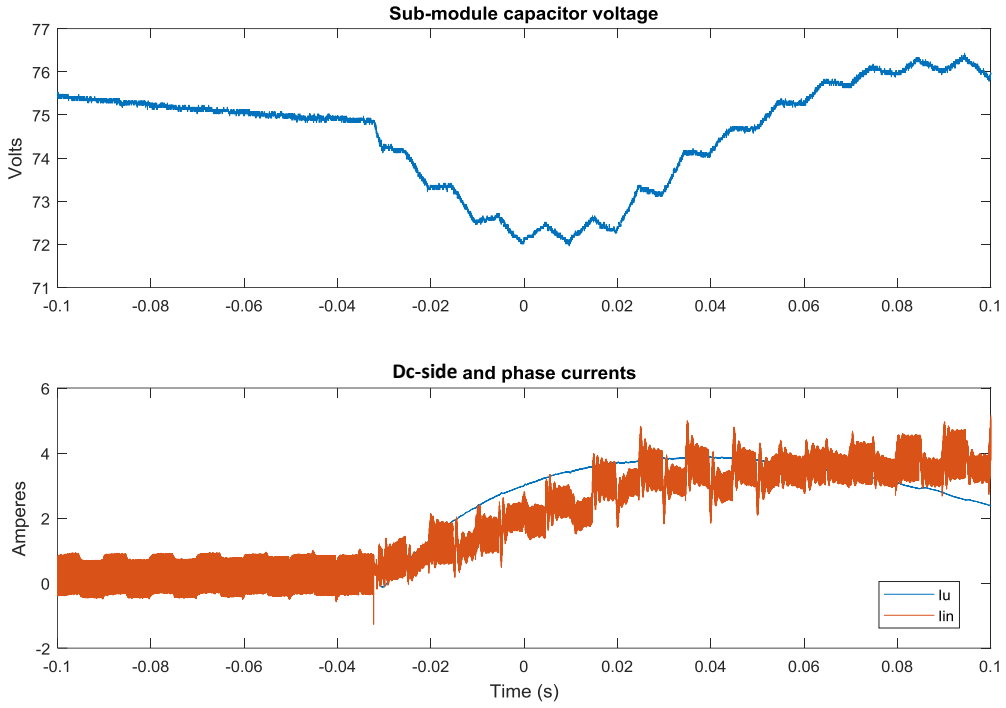

Figure 7-16 Response to an output current step at f_{out}=1Hz

The 100 Hz ripple is clearly visible on the waveform of the capacitor voltage and the ripple is less than 5V. The dc-side current also has a small 100 Hz component that has to be provided by the dc source. In Figure 7-17 the arm currents can be seen, where the 100Hz component is much larger, but as discussed previously only a fraction of it is supplied by the dc-side source:

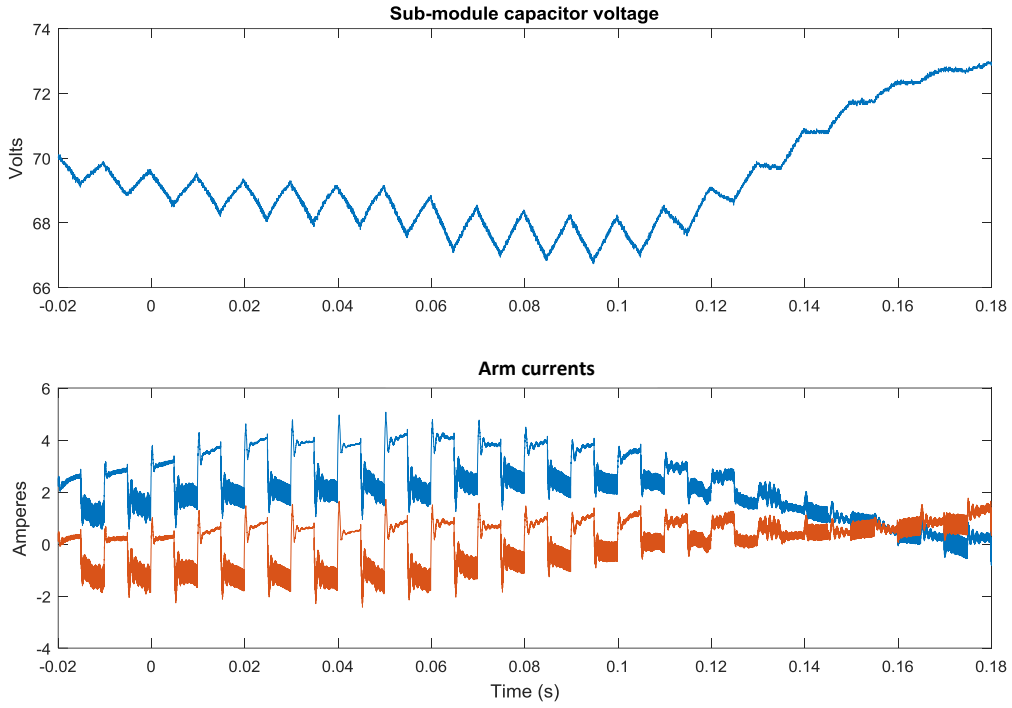

Figure 7-17 Sub-module voltage and arm currents with approximate f_{out}=2Hz

7.3. EXPERIMENTS WITH CONVERTER DRIVING A SIMULATED TRACTION LOAD

The converter has been connected to an induction motor coupled to a flywheel simulating a traction load with the main objective of demonstrating 4-quadrant operations. During these experiments, the average floating capacitor voltage has been kept constant by a voltage controller at 80 V, while the machine current is controlled by a field-oriented control (FOC) system. Internal balancing controllers maintain the same average capacitor voltages across all the sub-modules. At low frequency, the BMCI uses an arm balancing algorithm to reduce capacitor voltage ripple.

The ratio of field current and torque current has been adjusted to achieve field weakening at a base speed lower than the actual rated speed of the motor, so that the converter boost ratio stays within the stable region. The test setup and induction motor parameters are reported in Table 7-2.

Table 7-2 Experimental setup parameters

Power supply power limit	$P_{dc,max}$	420 W
Dc-side voltage	V_{dc}	45 V
Induction motor rated voltage	V_{LL}	230V_{RMS} @ 50Hz, delta connection
Power factor	$cos\varphi$	0.74
Induction motor field weakening speed	n_{FW}	750 rpm
Motor line current	I_{LINE}	2.33 A_{RMS}
I_d current reference	I_d*	1.51 A_{RMS}
I_q current reference	I_q*	1.77 A_{RMS}
Floating capacitor voltage reference	V_C*	80 V
Stator parasitic resistance	R_s	8.63 Ω
Stator leakage inductance	L_s	50.26 mH

The converter torque reference is generated by a closed-loop speed controller, with torque limited to the motor's rated value. The ratio of I_d/I_q was adjusted to achieve approximately 400 W maximum dc power, with acceleration time of less than 9 seconds.

7.3.1. Traction cycle test

To simulate a realistic electric vehicle, a traction cycle has been designed with acceleration up to a target speed of 1200 rpm, cruising, and braking to standstill. During

this cycle, the converter's line-to-line voltage, dc voltage, phase current, and dc-side current are monitored. The waveforms are displayed in Figure 7-18. The dc-side power increases linearly during constant torque operations, while it remains roughly constant during field weakening. The overshoot of the dc-side power is attributed to the delay of the speed measurement.

When the converter starts braking the induction motor, the tachometer delay causes the wrong electrical angle to be calculated. As the measured motor speed is not the true speed, the actual machine slip is different from the calculated one. The motor voltage amplitude has a smaller gradient, but there is an increase from the value at cruising speed..

To gather all the measurements the experiment is ran in two parts – acceleration to a constant speed, then braking from a constant speed. The results are then concatenated to get a single traction trajectory. The effective converter switching frequency is in the range of 20-40 kHz, and each experiment part lasts 10s; the voltage waveforms are low-pass filtered to show only the fundamental harmonic. The voltage boost ratio, G_V, is calculated using a moving RMS window, whit a fixed window length, which causes artefacts, which do not represent real oscillations.

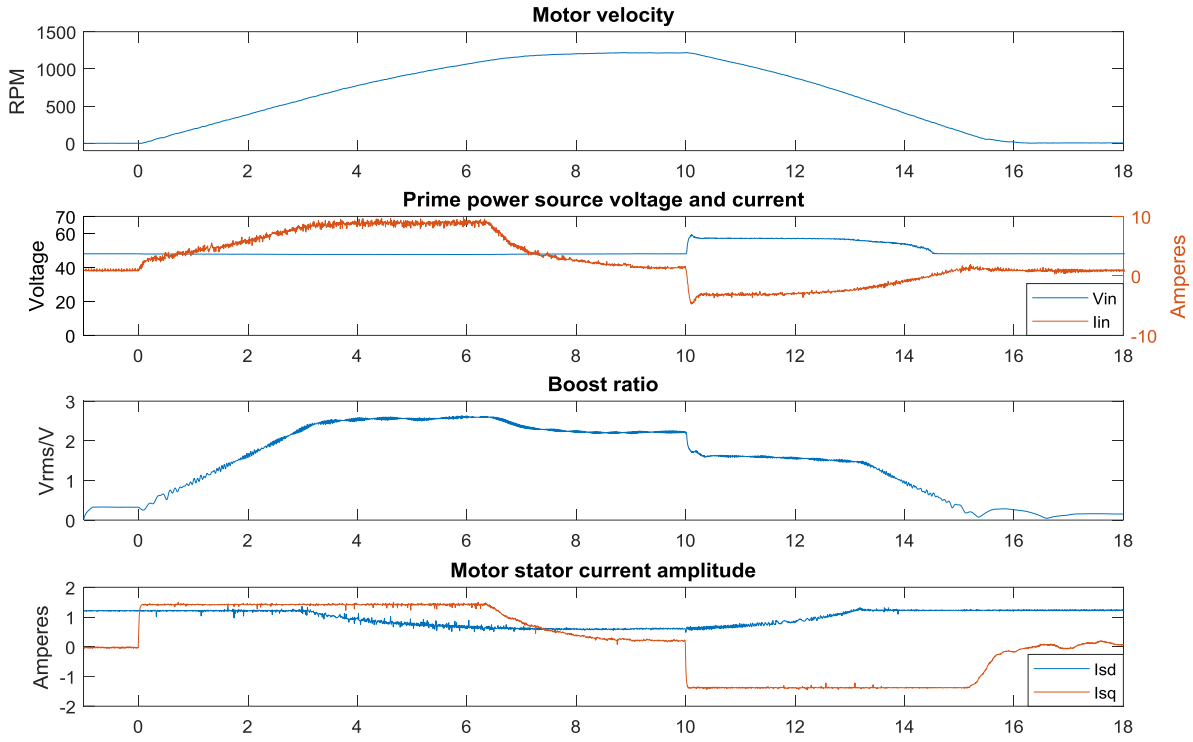

Figure 7-18 Converter operation during an acceleration-cruising-braking traction cycle

During the initial acceleration, the drive is operating in constant torque mode, with the output current having a constant amplitude. The ac-side voltage increases linearly, after an initial step to overcome the stator resistance. When the machine enters field weakening mode, the ac-side rms voltage remains constant until the torque reduces at *time=7s*. The braking starts at *time=10s*, with a torque command step. At that point, the converter starts regenerating the flywheel energy and dissipates it in the braking chopper. This is apparent as the dc-side voltage raises to roughly 53V. At *time=15s*, the drive can no longer regenerate any energy, and power from the dc supply is required to brake the machine further. From the analysis of the traction cycle, the peak dc power is 380 W, while the maximum braking power is 265 W.

Throughout the traction cycle the average capacitor voltage is 80V and is kept constant, while the voltage ripple varies with the output frequency, as shown in Figure 7-19.

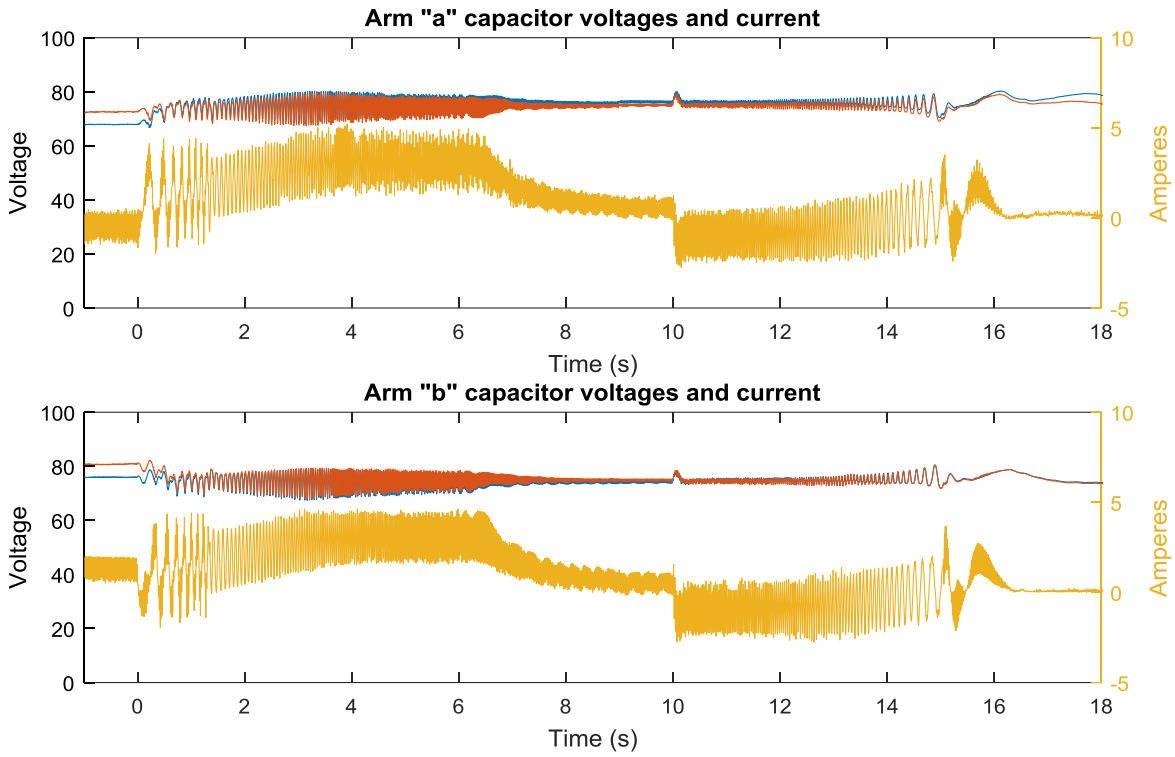

Figure 7-19 Arms a *and* b *capacitor voltages and currents during the traction cycle*

At stand-still the converter output power is very low, and the finite precision of the arm current measurement cause larger voltage errors in the steady-state. However, with higher power throughput the balancing systems maintain equal voltages between sub-module capacitors across the converter.

The following sections examine the converter's voltages and currents by zooming into Figure 7-18. Special attention is payed to operations with output frequency below 5 Hz during acceleration and braking.

7.3.1.1. Acceleration

Before acceleration begins the motor flux is maintained constant. This avoids the need of excessive slip at start-up, which would be the case if the motor magnetizing inductance is not charged. With a constant current i_d in the stationary state, the converter is producing a dc output current, which is impossible without a low-frequency compensation scheme. At start-up the induction motor speed is 0 and vector control

algorithm introduces a slip to start acceleration and the converter output electrical frequency is approximately 2.8Hz, as shown in Figure 7-20:

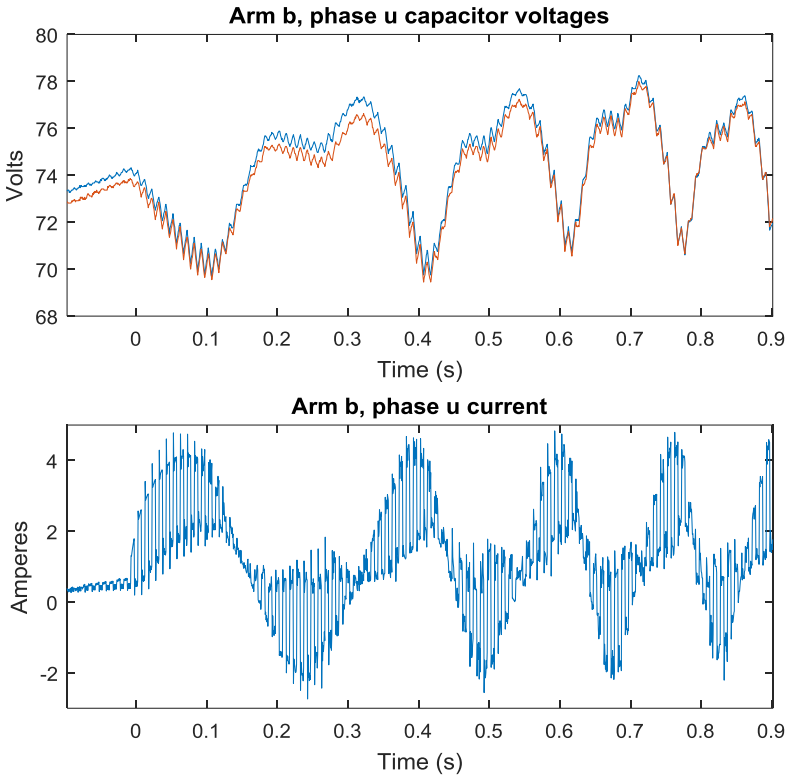

Figure 7-20 Converter capacitor voltages (top) and arm current (bottom) at start of acceleration

At higher frequencies the converter is supplying power to the electric motor and in the constant power region operates with a fixed boost ratio. A zoomed capture of the waveforms in this condition is shown in Figure 7-21:

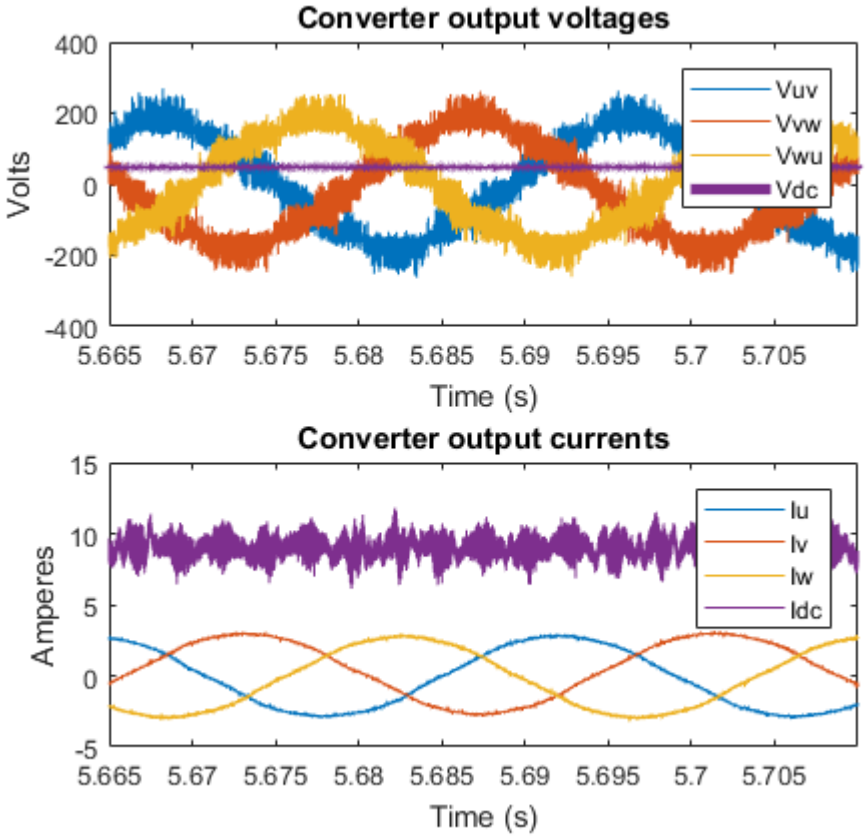

Figure 7-21 Converter voltages and currents during motoring

The high effective switching frequency is difficult to capture, but the line-to-line voltage steps can be clearly seen. The converter operates with a high boost ratio, with the peak voltage being 4 times higher than the dc source. At the same time the dc-side current has consistent ripple amplitude. The cause for the small oscillations in the dc-side current are unknown at this point, but are suspected to be caused by the OPAL-RT digital controller measurement.

7.3.1.2. Braking operation

During braking, the BMCI must invert the motor i_q current and starts recovering part of the kinetic energy of the flywheel. An oscilloscope capture is shown in Figure 7-22:

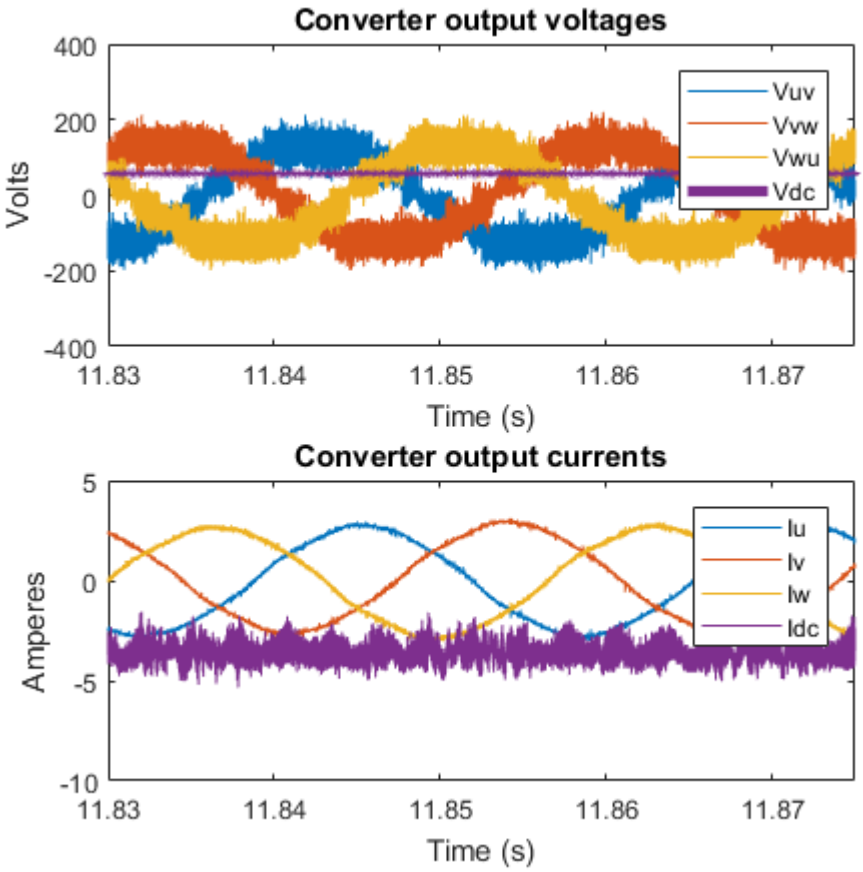

Figure 7-22 Converter voltages and currents during dynamic braking

The braking power is dissipated in a braking chopper connected to the dc terminals of the converter. Before and immediately after the start of braking the converter is operating with a voltage boost, but a lower factor than during acceleration. The dc-side current ripple has similar ripple amplitude.

When the converter frequency goes below 5Hz the low-frequency balancing control system is enabled and the 100Hz balancing current is injected, as shown in Figure 7-23. The arm current before the transition has very small dc value, as the losses in the electric motor do not allow for much energy to be regenerated. In addition, the 5Hz point was chosen as practically at this frequency the peak capacitor voltage ripple was equal to the maximum design value.

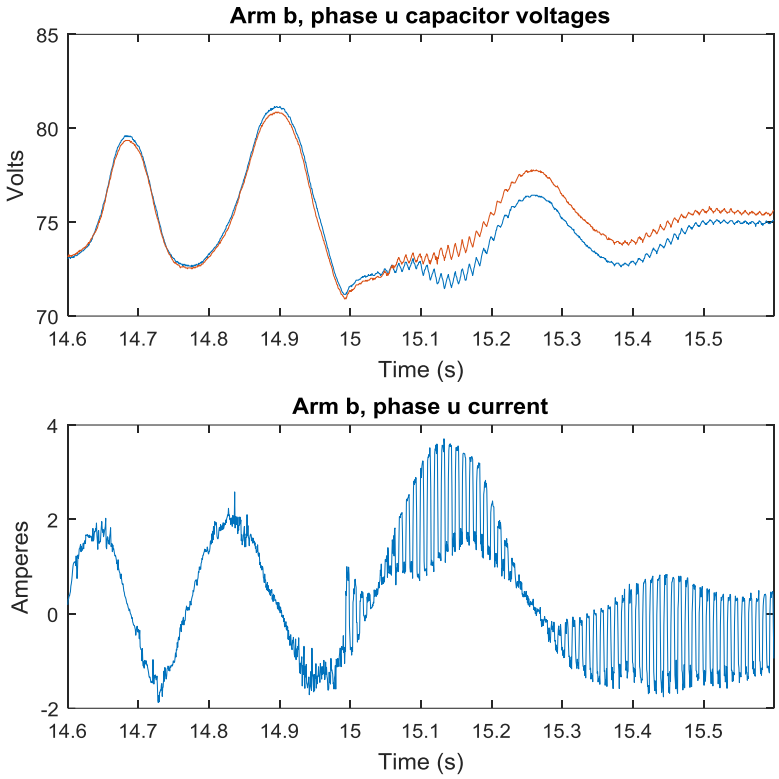

Figure 7-23 Transition from normal operation to low-frequency ripple compensation mode

7.3.1.3. Sub-module capacitor voltage ripple

The capacitor voltage ripple is directly affected by the motor rated power and base frequency. In Figure 7-24 another traction cycle is shown, together with the voltage of a single sub-module capacitor:

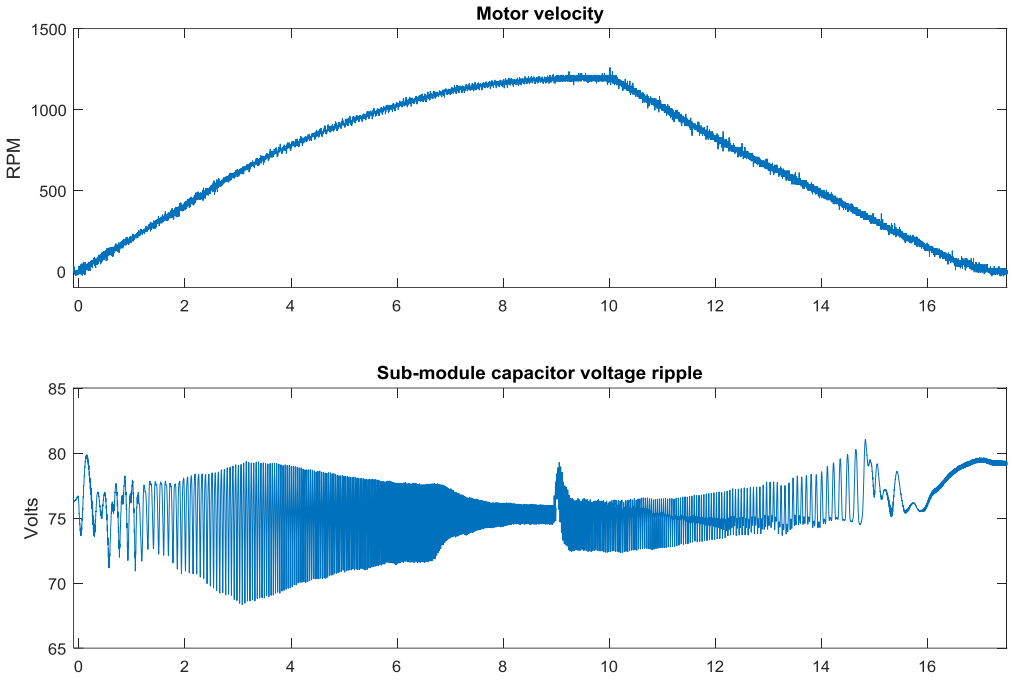

Figure 7-24 Motor speed and capacitor voltage ripple

The converter is operating in low-frequency mode up to *time = 1.146s*, where the stator frequency is below 8 Hz. After the initial response to the motor torque step at *t=0s*, the ripple in that region is less than the peak value of the cycle. Maximum ripple occurs at *t=3s,* where the BMCI enters field weakening mode. After this point the amplitude of the capacitor instantaneous power stays constant, while frequency increases, thus reducing the peak-to-peak voltage ripple. The maximum value measured is *10.5V*. Using the methods described in Chapter 5, the ripple was estimated to be *9V* peak-to-peak, as displayed in the surface plot in Figure 7-25. Therefore, the experimental results confirm the validity of the theoretical analyses and the practicality of the proposed converter as a traction drive.

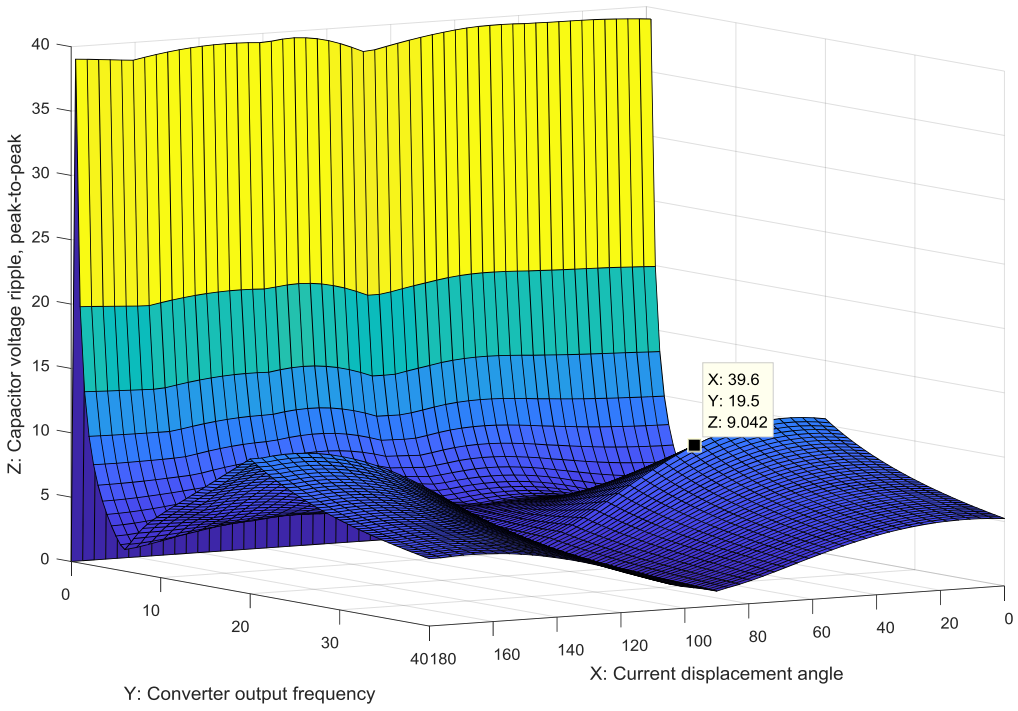

Figure 7-25 Surface plot of capacitor voltage ripple as a function of power factor and output frequency

7.4. SUMMARY

This chapter has been focussed on the experimental validation of the proposed converter. The hardware that has been designed for the project has been presented as a test rig with both passive and active loads. The experiments show a very good agreement with the analytical model and the numerical simulations and demonstrate that the BMCI is attractive for traction drives of electric vehicles, especially those with a low voltage dc power supply.

Experiments with a variable passive load show the basic operations of the converter with and without closed-loop control, exploring in detail the buck-boost characteristics of the converter at both nominal frequency of 50Hz and at low frequencies.

The converter has been then connected to an induction motor and measurements have been presented for acceleration and braking cycles for all 4 quadrants of operation. These experiments show that the converter can operate in the full speed range required by a traction motor, while operating at maximum torque and providing voltage boost ratios up

to 4.5. The converter shows superior voltage waveforms, compared to those of a 2-level converter, even though it uses only 2 sub-modules per arm, while showing lower capacitor voltage ripple at low frequencies, compared to a HB MMCC. At full power, the converter has very low circulating current ripple, even though it uses a relatively small inductance per phase, thanks to proposed modulation technique of the sub-modules.

While low-frequency operations introduce a higher dc-side current ripple, this effect can be mitigated by using some form of energy storage either at the converter's dc-side or integrated in each sub-module. This would likely be the case of hydrogen fuel cell vehicles, as energy storage would be determinant to reduce the peak power and, hence, the cost of the fuel cell stack. The proposed converter would be then particularly useful for this application, as the presence of low voltage sub-modules with floating capacitors is particularly suited for the connection of low voltage dc energy storage like electrochemical batteries or electrochemical capacitors.

Chapter 8. CONCLUSION AND FUTURE POSSIBILITIES

This thesis has been focussed on the analysis of the Boost Modular Cascaded Inverter for railway traction systems. The converter topology is essentially identical to a basic full-bridge modular cascaded converter. However, this PhD project has explored a completely new way of using this circuit – as a traction inverter with buck and boost voltage operations.

The principle of operation of the converter has been described in details and the mathematical model has been derived analytically. This work has presented the detailed dc transfer function of the BMCI that has been validated using open-loop experiments, showing the natural response of the converter. As conventional MCCs are used as buck converters or they are used to interface networks with fixed voltages, the maximum boost characteristics have been ignored in previous studies.

It has also been shown that the BMCI can be modelled as a combination of a cascaded boost converter and a 3-phase inverter, which facilitates the design of the main control systems. This project has also developed a new balancing algorithm for the sub-module capacitors that shows improved performance during converter transients in comparison with the current state of the art.

A converter design methodology has also been proposed to calculate the required converter inductance on the basis of the modulation scheme, the number of sub-modules, and the mean capacitor voltage. This has been used to design a 160 kW BMCI asynchronous motor drive that can be used for a fuel-cell powered tram. This setup is simulated for a typical traction cycle formed by an acceleration-cruising-braking periods with the aim of analysing converter performance.

Finally, the thesis has presented the experimental results from a laboratory prototype of the converter. The small-scale BMCI has been setup to drive an asynchronous machine with a peak line-to-line voltage of 200 V, while drawing power from a 50 V dc power supply. To simulate a traction load, the electric motor's shaft has been mechanically coupled to a solid steel flywheel. This setup simulates an inertial load and provides roughly 6-7 seconds of acceleration time at 500 W machine power. The logged data has been analysed and the following conclusions and recommendations can be made.

8.1. CONCLUSIONS

8.1.1. Suitability of BMCI as a boost traction inverter

This thesis has shown that the experimental prototype can operate in all 4 quadrants, i.e. it can both supply and recover power from the mechanical load. During the acceleration, the converter maintains constant current amplitude, while increasing line-to-line voltage. Above the asynchronous machine base frequency, the converter adjusts the field current to achieve constant power output achieving the required field-weakening. When a braking command is applied, the BMCI reverses the power flow, starting from the field-weakening region and moving to the constant torque region below the base frequency. The most challenging operation point for the BMCI occurs when the rotor frequency is close to 0, where $\omega_e \rightarrow 0$, and capacitor voltage ripple increases significantly. The experimental results show that the BMCI can compensate for the voltage ripple with appropriate control of the zero-sequence voltage and the peak-to-peak value is within the maximum limits.

8.1.2. Predictions of the BMCI large signal model

As with any other type of boost converter, the BMCI parasitic resistances need to be taken into account in order to define the correct steady-state gain and to avoid unstable

boost operations. The analytical model shows that large parasitic resistance can severely limit the maximum boost ratio. The model has been validated using practical experiments, using a known passive resistive-inductive load. As expected, the converter voltage gain is substantially smaller than the ideal value, as the prototype converter uses overrated transistors and high capacitor ESR.

8.1.3. Impact on the dc-side voltage on the modulation index

The research has found that the maximum required capacitor voltage is not defined by the minimum dc-side voltage, but by the maximum. The experimental converter operates with a boost ratio of roughly *0.14* during motoring, and *0.18* during regenerative braking. As the sub-module capacitor voltages are regulated to a constant value, the modulation index has more headroom during motoring, where dc-side voltage is lower. This counterintuitive result makes the BMCI suitable for applications like dc-powered rail vehicles, where intermittent line voltages are often encountered. In such circumstances, the high converter capacitance can be utilised to maintain constant output power.

8.1.4. Link between passive elements and motor parameters

Chapter 5 has presented the methodology for the design of the converter. It is shown that the total converter capacitance is dependent only on the boost ratio and the machine base frequency. For comparison, in a 2-level inverter it is instead dependent on the transistor switching frequency, the power factor, and the motor current amplitude.

High speed motor drives are an area where multilevel inverters are preferred, as they typical 2-level inverters operate with switching frequencies as low as 500Hz. The BMCI is particularly well suited to such applications, as the converter effective frequency is multiplied by the number of levels n.

8.1.5. Influence on inductance and output THD

The BMCI produces a higher quality voltage waveform, compared to an MCC with the same number of sub-modules, *n*, but lower than a flying capacitor or neutral point clamp multilevel inverter. However, the BMCI also removes the need for a boost converter, and reduces the required inductance, as it is inversely proportional to approximately the square of the number of sub-modules. Thus, the BMCI can be a power dense solution for certain applications and it can also achieve higher efficiency and better motor performance.

8.2. FUTURE WORK

Due to time restrictions, multiple topics have not been covered, or explored in sufficient depth. Some of the more interesting ones are indicated in the following.

8.2.1. BMCI for permanent magnet drives

Permanent magnet synchronous motors offer slightly higher efficiency and power density than asynchronous induction machines. If the inverter dc link of a traditional 2-level inverter collapses the voltage induced by the magnet can be harmful for the power electronics. The BMCI is capable of operating with 0 dc-side voltage, as long as there is a power source connected to the 3-phase side like the case of permanent magnet motor drives and, hence, there would not be issues in case of a dc-link fault;

8.2.2. Capacitor voltage ripple reduction

A recent paper has shown that this current component can be injected to reduce capacitor voltage ripple, resulting in smaller capacitance requirement for the converter. The proposed study will have to investigate the maximum 2^{nd} harmonic current amplitude that does not violate the peak arm current requirement. This value will determine the maximum capacitor voltage compensation that can be achieved.

8.2.3. Trade-off between dc current ripple and ac voltage THD

0 has explored the effects of the phase shift angle between the carriers of arm *a* and that of arm *b*, $\theta_{carrier}$. It has been shown that, depending on number of sub-modules, the converter can achieve either *m* or *2m-1* output levels. However, the value of $\theta_{carrier}$ that achieves the lowest inverter ac-side voltage THD causes the highest current ripple in the circulating current. Further work is required to fully describe the performance of popular modulation schemes under different values of $d_{dc,x}$.

8.2.4. Optimum carrier modulation to reduce the leg inductance

This thesis has described the effects of conventional modulation methods on the design of the leg inductor. Depending on the chosen scheme, the frequency spectrum of the circulating dc current shows different power spread. As conventional MCCs are buck converters, they use $d_{dc,x} = 0.5$, resulting in a boundary condition for the modulation waveforms. The effect of dc duty cycle that is not divisible by *n* have not yet been explored. Moreover, there are other modulation methods, where the PWM carriers have variable phase, dependent on modulation depth. Future work can explore optimum PWM carrier generation for a BMCI.

8.2.5. BMCI power density

Traction converters must achieve both high power density and high efficiency. Typical power inductors for traction are large, heavy and have a high cost. The proposed BMCI can reduce the required inductance by increasing the number of sub-modules, but the total converter capacitance will be higher than a 2-level inverter with the same power rating. A detailed model of BMCI power density must be constructed in order to estimate a realistic power density figure for a traction converter using the proposed topology.

8.2.6. BMCI efficiency and device power dissipation

Efficiency of the converter has not been investigated. With a conventional boost converter, high boost ratios result in high converter losses, as the transistors switch high currents at a high voltage. In a BMCI, the number of sub-modules is arbitrary, and the sub-module voltage can be chosen. For example, low-voltage MOSFETs can achieve very low drain-source resistance. As it increases at a quadratic rate with transistor blocking voltage an *n*-module converter, with *2n* devices, can have a lower on resistance than a transistor with voltage rating *n* times higher.

A comprehensive analysis of converter can show how efficiency scales with different number of sub-modules, taking into account the type of device, required blocking voltage per device, required inductance, and required capacitance.

8.2.7. Effects of ddc,x on device utilisation and ac voltage waveform

The effects of dc duty cycle $d_{dc,x}$ on ac voltage THD must be explored further. Lower $d_{dc,x}$ increases voltage boost and the number of effective inverter ac-side voltage levels, and results in lower THD. At the same time, however, one cross-pair of transistors in a sub-module bridge will have much longer conduction times and any distortion, caused by switch dead-time, will become more prominent.

8.2.8. BMCI used as DC-traction power supply

DC traction power supplies always require a power electronics converter. As this is a very high current application, diode rectifiers are a very popular solution due to the low power dissipation, low voltage drop and high power factor. However, diode rectifiers have a regulation effect due to the dc-side inductance and they require very comprehensive output short circuit protection, as diodes are not controllable devices. Thyristors, on the

other hand, offer reverse blocking capabilities, but introduce high number of harmonics into the 3-phase power supply and reactive power when the voltage output is regulated.

A BMCI converter can be used as an active rectifier, that offers both high power factor and fault management capability. A power electronics converter can implement arbitrary fault responses and the system current limit can be set to a much lower value than that for diode rectifiers. As an additional functionality, a BMCI traction rectifier will allow for bidirectional power flow, where braking energy from a train slowing down can be returned to the grid.

8.2.9. Hybrid traction drive using embedded energy storage

The BMCI is a modular structure, consisting of many identical modules. Several papers have shown that MCC converters can integrate energy storage devices like batteries and supercapacitors, separately controlling energy stored, and power drawn from the dc-link. This principle can be applied to a BMCI hydrogen-battery hybrid drive that does not require a battery management system and can fully utilise the energy stored in the battery banks.

Examining this application will require incorporating a battery model into the model described in chapter 3. The control system of the BMCI must be modified to manage the energy stored in the batteries, and the sub-module voltage balancing must be converted to the state of charge balancing of battery cells.

The design of a hybrid BMCI drive would be a very interesting topic. While it has been shown that an MCC can have a sub-module for every battery, such a converter with a standard voltage of 300V will require hundredths of sub-modules. Moreover, the device utilisation will be poor, as a typical lithium-ion battery cell has a terminal voltage that varies between 3.5V and 4.2V. At the same time commercial low-voltage/high-current MOSFET brake-down voltages are 30V or higher. As an example, to fully utilise a 30V

transistor, the BMCI sub-module will require 4 batteries, producing up to 16.8V. This allows sufficient margin for a fast high-current semiconductor. The hybrid BMCI must be designed according to a predetermined traction cycle, in order to set the maximum stored energy requirement. The same amount of energy can be stored in either low number of battery cells with high capacity, or a high number of low-capacity cells. From the results of this project, it would be possible to determine the optimum number of battery cells, and sub-modules that can achieve balance between converter efficiency, complexity, and power density.

The BMCI must also control the dc-side current to be always positive, which is a requirement of hydrogen fuel cells. A braking chopper could be used to limit the peak battery power during regenerative braking but is expected that it will not be required.

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Appendix A. BMCI DESIGN

This appendix details the design of a BMCI for an urban tram. The converter capacitance is designed according to the machine parameters from Table 6-2 and fuel-cell stack parameters from Table 6-3.

The induction machine line-to-line voltage is $532V_{RMS}$, which results in required peak ac-side voltage of at least 750V line-to-line. From equation (5-8) the required arm voltage is:

$$\max(v_{a/b,x}) = \frac{750-198}{2} = 552V \tag{A-1}$$

To allow for some headroom, the maximum design voltage is 300V. For a small number of sub-modules, with derating the converter can use 600 or 650V transistors and a total of *n=2* sub-modules per arm. These are industry standard voltages and there are multiple possible choices for transistors, both IGBTs and MOSFETs. The peak transistor current is:

$$\max(i_{L,a/b,x}) = I_{dc,x,\max} + \frac{I_{ac,x,peak}}{2} = 366.7A + 143A = 510.52A \tag{A-2}$$

The transistors chosen are FF600R07ME4_B11 and a usable switching frequency is 1kHz, giving $T_{sw,eff}=0.25ms$.

The minimum dc duty cycle is:

$$d_{dc,x} = \frac{V_{IN}}{2\sqrt{2}V_{LL}} = 0.132 \tag{A-3}$$

The arm dc current can be inferred from the fuel cell output current rated power:

$$I_{dc,x} = \frac{I_{in}}{3} = 366.7A \tag{A-4}$$

The coincidence duty cycle can be calculated from (5-16), for $d_{dc,x}<0.5/n$:

$$d_{coinc} = 2\left(nd_{dc,x} - floor(nd_{dc,x})\right) = 0.528 \tag{A-5}$$

Setting a design limit of <20% current ripple, equal to roughly 75A per leg, and with interleaved arm *a* and *b* carriers, using equation (5-17) the required inductance becomes:

$$L_{leg} = \frac{1}{\Delta i_{dc,x}} d_{coinc}\left(1 - d_{coinc}\right) V_C T_{sw,eff} \approx 249\mu H \qquad (A\text{-}6)$$

The leg inductor is centre-tapped to reduce the converter output inductance, and the required magnetizing inductance is $L_M = 64.25\mu H$. The inductor air gap needs to be sufficiently large to maintain the designed L_M at current equal to the peak dc current. The effect of the ac current on inductor flux is cancelled, as it is differential.

Appendix B. CONTROL SYSTEM DESIGN

The control system of the BMCI is designed according to the parameters found in Table 6-4. The converter operating point was found in Chapter 7 to be $d_{dc,x}=0.165$ and $D_{ac,x} = 0.8$. The sub-module resistance r_{SM} is found using (3-44):

$$r_{SM} = \left(d_{dc,x}{}^2 + d_{ac,x}{}^2\right) r_C + 2r_{SW} = 63.1m\Omega \tag{B-7}$$

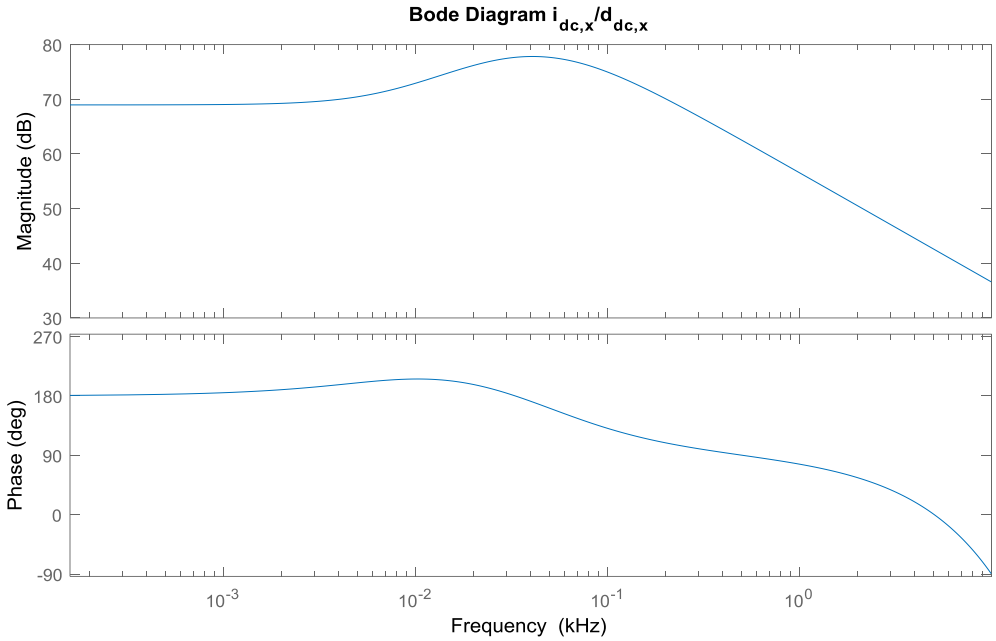
The phase resistance R_x can be derived from the motor rated voltages and currents, as well as power factor:

$$R_x = \frac{V_{ll,RMS}}{\sqrt{3} PF\, I_{RMS}} \approx 1.6105\Omega \tag{B-8}$$

The equivalent sub-module resistance R_{SM} is equal to:

$$R_{x,SM} = \frac{2\dfrac{R_x}{\cos\varphi} + r_L + nr_{SM}}{nD_{ac,x,RMS}{}^2} = 3.52\Omega \tag{B-9}$$

The bode plot of the transfer function, including zero-order hold delay, of the circulating current $i_{dc,x}$ with input dc duty cycle $d_{dc,x}$, equation (4-26), is shown below:



From equations (4-27) through (4-29) the zero frequency, natural frequency, and dc gain are found to be:

$$\omega_z = \frac{2}{R_{SM}C} = 56.73 rad/s \qquad (B\text{-}10)$$

$$\omega_n = \sqrt{\frac{nR_{SM}d^2 + r_{arm}}{R_{SM}LC}} = 270.53 rad/s \qquad (B\text{-}11)$$

$$G_{idc,x}(0) = -\frac{2nV_C}{nd^2R_{SM} + r_{arm}} = 3.17\times10^3 A/V \qquad (B\text{-}12)$$

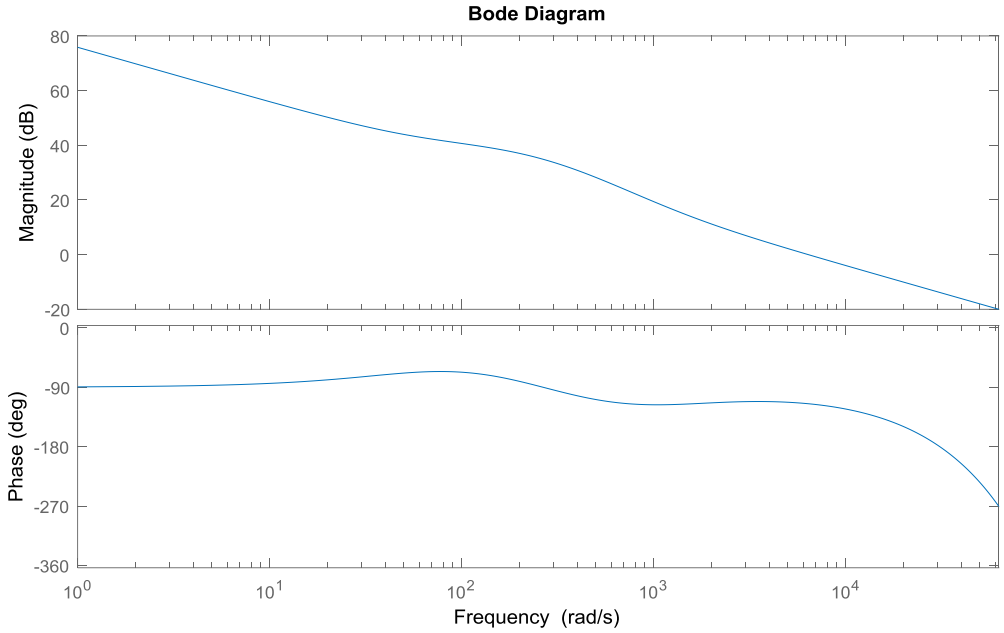
The effective switching frequency of the converter is $f_{sw,eff}=2nf_{sw,Q}=4kHz$, giving a closed loop bandwidth $\omega_{0dB,CL}=2\pi400\ rad/s$. The current compensator gains $k_{p,i}$ and $i_{i,i}$ are designed using (4-31), (4-32), and (4-33) to be:

$$\omega_{i,0dB} = \frac{\beta_{idc} G_{idc} \omega_n^{\,2}}{\omega_z} = 4.09 \times 10^6 \, rad/s \qquad \textit{(B-13)}$$

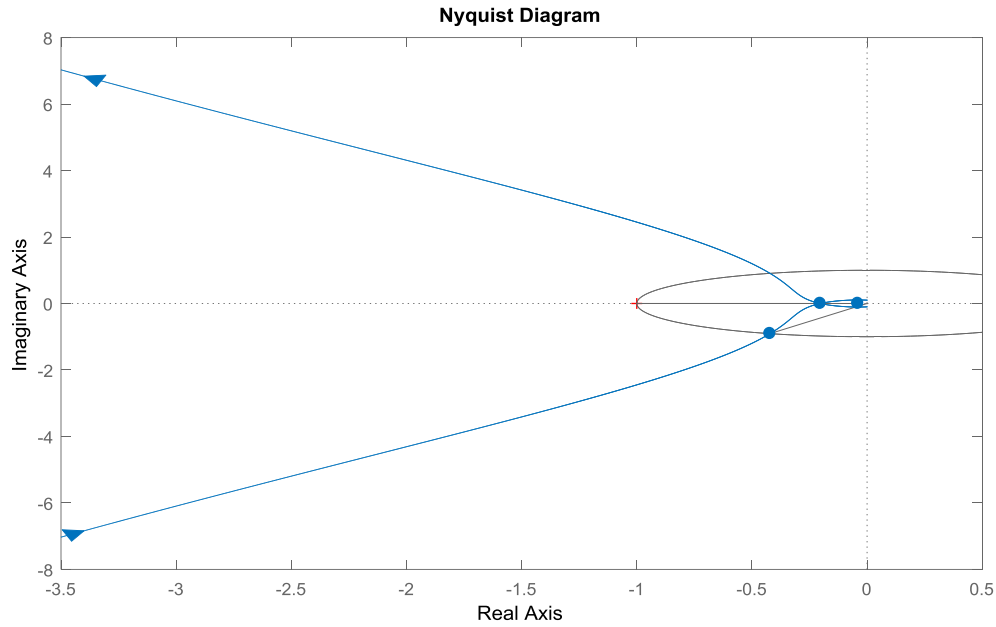
$$k_{p,idc} = \frac{\omega_{i,CL}}{\omega_{i,0dB}} = -0.0015 \qquad \textit{(B-14)}$$

$$k_{i,idc} = k_{p,idc} \omega_{z,comp} = k_{p,idc} 0.1 \omega_{i,CL} = -1.9302 \qquad \textit{(B-15)}$$

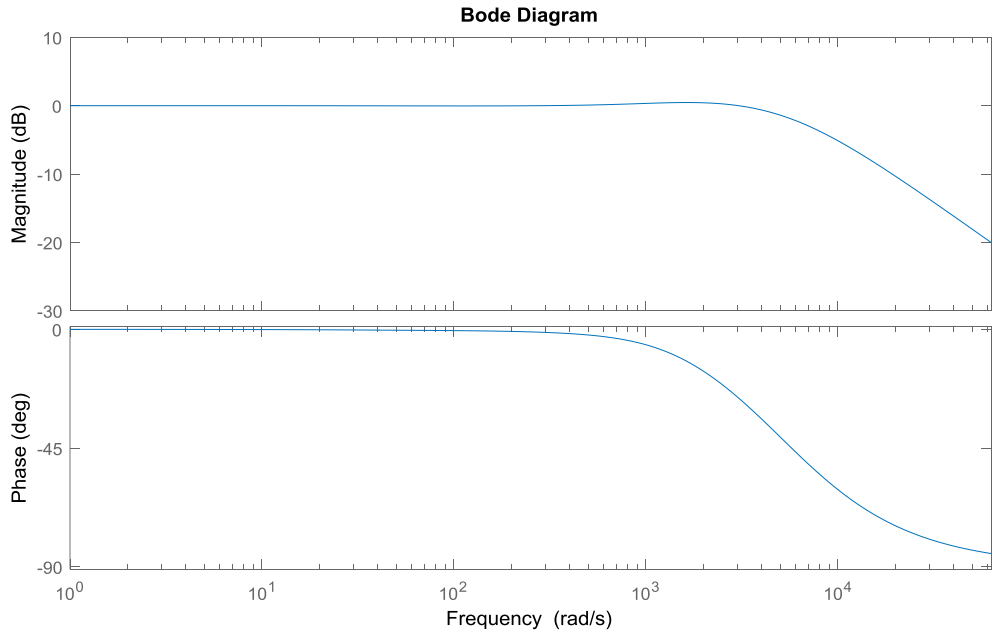
The bode plot of the open loop transfer function can be seen in :



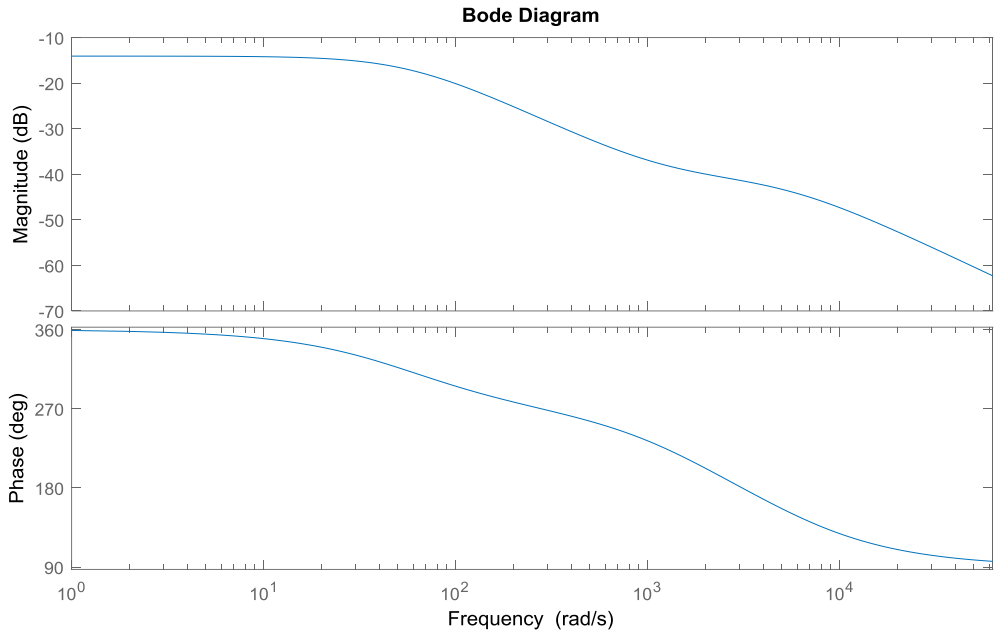
The stability of the system is checked by evaluating the open loop Nyquist response:



The Nyquist plot shows that the system is stable, with phase margin of 65° and gain margin of 13.8dB. The plot of the closed-loop transfer function is shown below:



The bode response of capacitor voltage transfer function from equation (4-41) can now be plotted:



The dc gain is calculated using equation (4-42):

$$\frac{G_{vc}}{G_{idc}} = \frac{nD_{dc,x}{}^2 R_{SM} - r_{arm}}{2nD_{dc,x}} = 0.1980V / A \qquad (B\text{-}16)$$

The dc-gain of the capacitor transfer function is less than 0dB, but equation (4-44) computes the asymptotic intersection of the break frequency and the 0dB line. Thus, the effective crossover frequency can still be used for compensator design:

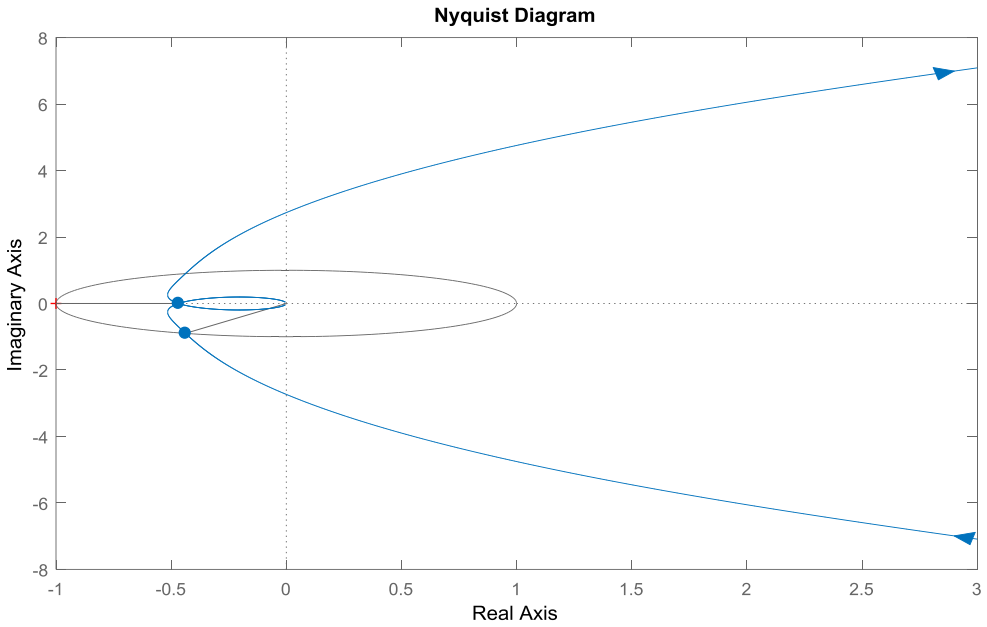
$$\omega_{v,0dB} = \frac{G_{vc}}{G_{idc}} \omega_z = 114.17 rad / s \qquad (B\text{-}17)$$

The closed-loop crossover frequency of the voltage loop is set one decade below that of the current controller, and the compensator gains , using (4-45) and (4-46), are:

$$k_{p,vc} = \frac{\omega_{v,0dB,CL}}{\omega_{v,0dB}} = 55.03 \qquad (B\text{-}18)$$

$$k_{i,vc} = \frac{\omega_z}{2} k_{p,vc} = 317.32 \qquad (B\text{-}19)$$

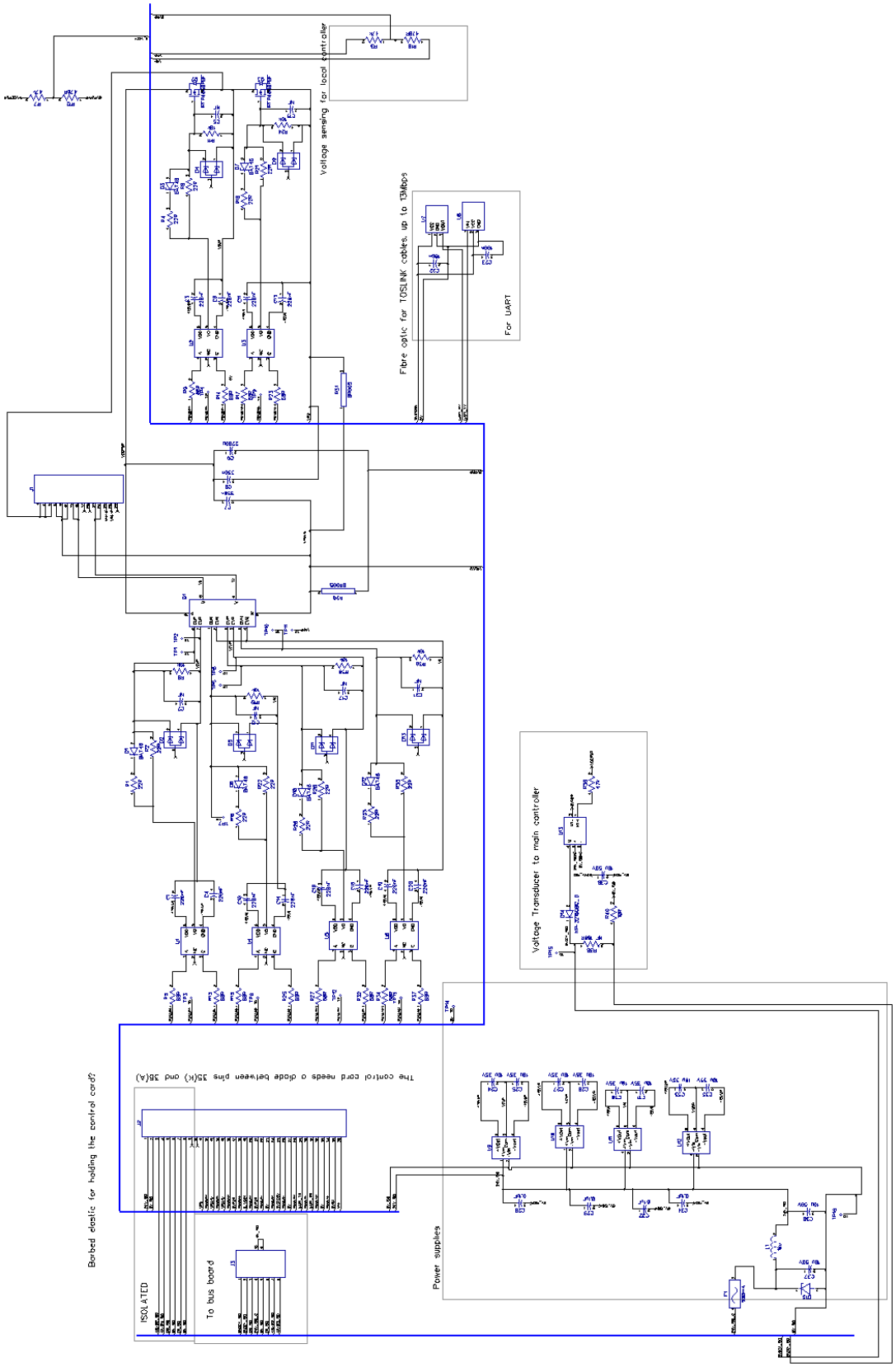
The stability of the system can be evaluated using a Nyquist plot:



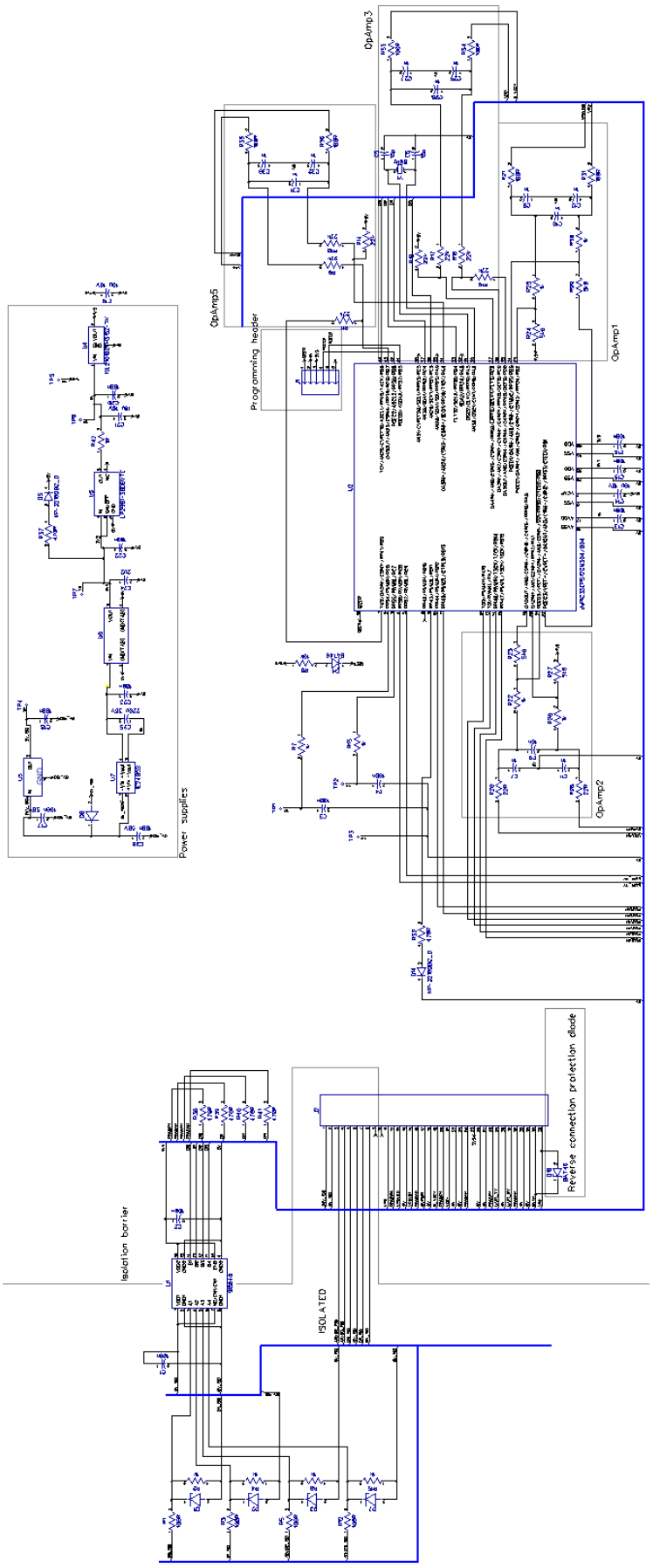
The phase margin was found to be 64 degrees and the gain margin of 6.5dB.

Appendix C. CONVERTER PCB SCHEMATICS

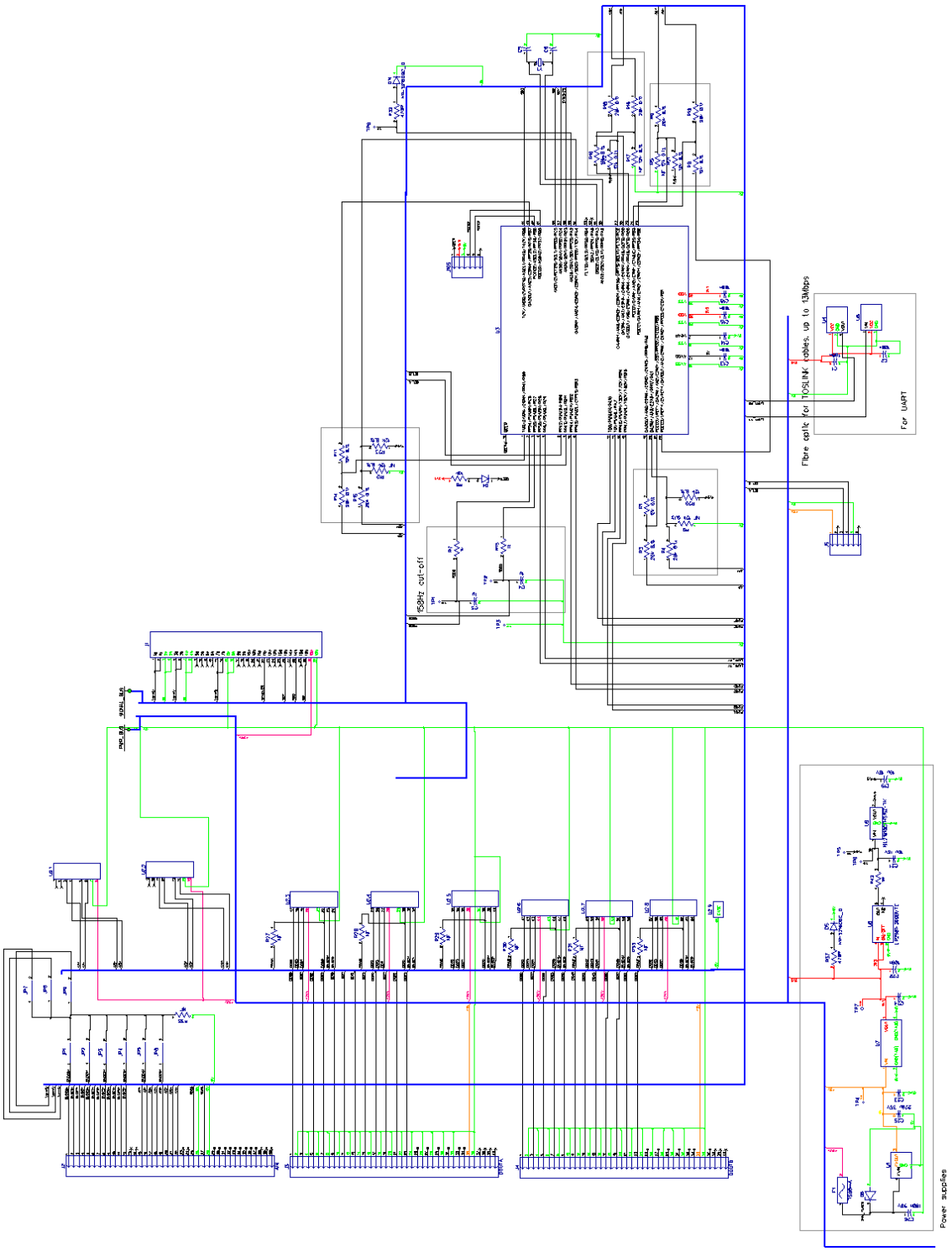
Sub-module Power PCB



Control card PCB



Routing card PCB



Current sensor PCB card