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Digital CMOS ISFET Architectures and Algorithmic Methods for Point-of-Care Diagnostics

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Statement of Originality

I, Miguel Cacho Soblechero, declare that this thesis titled, “Digital CMOS ISFET Architectures and Algorithmic Methods for Point-of-Care Diagnostics” and the work presented in it is my own, and all material presented which is not my own work has been properly acknowledged.

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Miguel Cacho Soblechero

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Abstract

Over the past decade, the surge of infectious diseases outbreaks across the globe is redefining how healthcare is provided and delivered to patients, with a clear trend towards distributed diagnosis at the Point-of-Care (PoC). In this context, Ion-Sensitive Field Effect Transistors (ISFETs) fabricated on standard CMOS technology have emerged as a promising solution to achieve a precise, deliverable and inexpensive platform that could be deployed worldwide to provide a rapid diagnosis of infectious diseases. This thesis presents advancements for the future of ISFET-based PoC diagnostic platforms, proposing and implementing a set of hardware and software methodologies to overcome its main challenges and enhance its sensing capabilities.

The first part of this thesis focuses on novel hardware architectures that enable direct integration with computational capabilities while providing pixel programmability and adaptability required to overcome pressing challenges on ISFET-based PoC platforms. This section explores oscillator-based ISFET architectures, a set of sensing front-ends that encodes the chemical information on the duty cycle of a PWM signal. Two initial architectures are proposed and fabricated in AMS $0.35\mu m$, confirming multiple degrees of programmability and potential for multi-sensing. One of these architectures is optimised to create a dual-sensing pixel capable of sensing both temperature and chemical information on the same spatial point while modulating this information simultaneously on a single waveform. This dual-sensing capability, verified *in silico* using TSMC $0.18\mu m$ process, is vital for DNA-based diagnosis where protocols such as LAMP or PCR require precise thermal control.

The COVID-19 pandemic highlighted the need for a deliverable diagnosis that perform nucleic acid amplification tests at the PoC, requiring minimal footprint by integrating sensing and computational capabilities. In response to this challenge, a paradigm shift is proposed, advocating for integrating all elements of the portable diagnostic platform under a single piece of silicon, realising a “Diagnosis-on-a-Chip”. This approach is enabled by a novel Digital ISFET Pixel that integrates both ADC and memory with sensing elements on each pixel, enhancing its parallelism. Furthermore, this architecture removes the need for external instrumentation or memories and facilitates its integration with computational capabilities on-chip, such as the proposed ARM Cortex M3 system.

These computational capabilities need to be complemented with software methods that enable

sensing enhancement and new applications using ISFET arrays. The second part of this thesis is devoted to these methods. Leveraging the programmability capabilities available on oscillator-based architectures, various digital signal processing algorithms are implemented to overcome the most urgent ISFET non-idealities, such as trapped charge, drift and chemical noise. These methods enable fast trapped charge cancellation and enhanced dynamic range through real-time drift compensation, achieving over 36 hours of continuous monitoring without pixel saturation.

Furthermore, the recent development of data-driven models and software methods open a wide range of opportunities for ISFET sensing and beyond. In the last section of this thesis, two examples of these opportunities are explored: the optimisation of image compression algorithms on chemical images generated by an ultra-high frame-rate ISFET array; and a proposed paradigm shift on surface Electromyography (sEMG) signals, moving from data-harvesting to information-focused sensing. These examples represent an initial step forward on a journey towards a new generation of miniaturised, precise and efficient sensors for PoC diagnostics.

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‘We cannot change the inevitable. The only thing we can do is play on the one string we have, and that is our attitude. I am convinced that life is 10% what happens to me and 90% of how I react to it. And so it is with you... we are in charge of our Attitudes’

Charles Swindoll

Cuando emprendas tu viaje a Itaca
pide que el camino sea largo,
lleno de aventuras, lleno de experiencias.
No temas a los lestrigones ni a los cíclopes
ni al colérico Poseidón,
seres tales jamás hallarás en tu camino,
si tu pensar es elevado, si selecta
es la emoción que toca tu espíritu y tu cuerpo.
Ni a los lestrigones ni a los cíclopes
ni al salvaje Poseidón encontrarás,
si no los llevas dentro de tu alma,
si no los yergue tu alma ante ti.

Pide que el camino sea largo.
Que muchas sean las mañanas de verano
en que llegues -¡con qué placer y alegría!-
a puertos nunca vistos antes.
Detente en los emporios de Fenicia
y hazte con hermosas mercancías,
nácar y coral, ámbar y ébano
y toda suerte de perfumes sensuales,
cuantos más abundantes perfumes sensuales puedas.
Ve a muchas ciudades egipcias
a aprender, a aprender de sus sabios.

Ten siempre a Itaca en tu mente.
Llegar allí es tu destino.
Mas no apresures nunca el viaje.
Mejor que dure muchos años
y atracar, viejo ya, en la isla,
enriquecido de cuanto ganaste en el camino
sin aguantar a que Itaca te enriquezca.

Itaca te brindó tan hermoso viaje.
Sin ella no habrías emprendido el camino.
Pero no tiene ya nada que darte.

Aunque la halles pobre, Itaca no te ha engañado.
Así, sabio como te has vuelto, con tanta experiencia,
entenderás ya qué significan las Itacas.

Konstantino Kavafis

Contents

Abstract	ii
Acknowledgements	v
List of Figures	xvii
List of Tables	xxiii
Abbreviations	xxv
1 Introduction	1
1.1 Motivation	1
1.2 Research Objectives	2
1.3 Thesis Organisation	3
1.3.1 Chapter 2: ISFETs at the Point-of-Care: State-of-the-Art and Challenges	3
1.3.2 Chapter 3: Oscillator-based ISFET Architectures	4
1.3.3 Chapter 4: Towards a Diagnosis-on-a-Chip: Digital ISFET Sensor	4
1.3.4 Chapter 5: Software methods for adaptability enhancement of ISFET PoC Platforms	4
1.3.5 Chapter 6: Software Opportunities for ISFET Sensing and beyond	5

2	ISFETs at the Point-of-Care: State-of-the-art and Challenges	7
2.1	Introduction	7
2.2	Point-of-Care Devices	10
2.2.1	Elements of Point-of-Care Devices	11
2.2.2	PoC Devices Classification	21
2.3	ISFET at the Point-of-Care	24
2.3.1	ISFET Sensing Principle	25
2.3.2	ISFET Challenges	27
2.3.3	ISFET Sensing Front-End	35
2.3.4	ISFET applications	42
2.4	Summary	45
3	Oscillator-based ISFET Architectures	57
3.1	Introduction to Oscillator-based Architectures	57
3.2	Preliminary analysis	58
3.2.1	8-Stage Sawtooth Oscillator: Principle of operation	59
3.2.2	Chemically Controlled Ring Oscillator (CCRO): Principle of operation	61
3.2.3	Fabricated System - LEGOLAS	63
3.2.4	Electrical and Chemical Characterization - 8-Stage Sawtooth Oscillator Pixel	65
3.2.5	Electrical and Chemical Characterization - CCRO Pixel	70
3.2.6	Architecture Comparison	73
3.3	Dual-Sensing ISFET Array	74

3.3.1	Chemical Sensing - Principle of operation	74
3.3.2	Thermal Sensing - Principle of operation	77
3.3.3	System-Level Architecture	79
3.3.4	Fabricated System - Black Pearl	80
3.3.5	Experimental Results: Chemical Sensor	83
3.3.6	Experimental Results: Temperature Sensor	89
3.3.7	Experimental Results: Thermo-Chemical Cross-Sensitivity	90
3.3.8	Experimental Results: On-Chip LAMP DNA Amplification and Detection	92
3.3.9	Final Remarks	92
3.4	Future Perspectives on Oscillator-Based ISFET Architectures	94
3.4.1	Ultra-Low Power ISFET Pixel Architecture	94
3.4.2	Quad-Sensing ISFET Array: Simultaneous Sensing of Ions, Temperature, Fluid Presence and Light	99
3.5	Summary	107
3.6	Publications	108
4	Towards a Diagnosis-on-a-Chip: Digital ISFET Sensor	115
4.1	PoC Diagnostics in a Pandemic situation	115
4.2	Introduction to In-Pixel ADC Architectures	116
4.3	Digital ISFET Sensor	119
4.3.1	Pixel Operation	121
4.3.2	System Architecture & Performance	124
4.4	Processing Elements integration for a Diagnosis-on-a-Chip	129

4.5	Summary	131
4.6	Publications & Awards	132
5	Software methods for adaptability enhancement of ISFET PoC Platforms	135
5.1	Motivation	135
5.2	instantDNA: A versatile PoC platform for ISFET sensing	137
5.2.1	System Level Architecture	137
5.3	Trapped charge compensation through 2-steps adaptive controller	140
5.4	Resolution enhancement using extended time sampling window	142
5.4.1	Experimental Setup & Results	143
5.5	Real-time drift compensation for ISFET-based long-term monitoring	145
5.5.1	Principle of operation	146
5.5.2	Experimental Results	147
5.6	Summary	156
5.7	Publications	157
6	Software Opportunities for ISFET Sensing and beyond	160
6.1	Algorithmic methods on e-Health Solutions	160
6.2	JPEG Deployment and Optimisation for Chemical Image Compression	161
6.2.1	Introduction to Image Compression	161
6.2.2	JPEG Architecture	162
6.2.3	Real-Time Lab-on-Chip Platform	165
6.2.4	A Bio-Inspired JPEG Compression Optimization	165
6.2.5	Results	168

6.3	4-Channels sEMG Architecture with On-Chip Feature Extraction	169
6.3.1	From Data-Harvesting to Information-Focused: a novel approach for sEMG architectures	170
6.3.2	sEMG Channel Architecture	173
6.3.3	System Architecture	177
6.3.4	Simulation Results	178
6.4	Summary	181
6.5	Publications	182
7	Conclusion	187
7.1	Overview	187
7.2	Contributions	188
7.2.1	How can we develop ISFET-based PoC platforms more adaptable to both non-idealities and external conditions?	188
7.2.2	How can we reduce ISFET-based platforms footprint at a system level to enhance their deliverability to the PoC?	189
7.2.3	How can novel data-driven methods help enhance the PoC sensors' sens- ing capabilities?	190
7.3	Recommendations for Future Work	191
7.3.1	Sense-Aware ISFET Array	191
7.3.2	Deployment of Diagnosis-on-a-Chip	191
7.3.3	Detection of slow ion variation during long-term monitoring	192
7.3.4	Information-Based Compression of chemical videos	192
7.4	Thesis Discussion and Outlook	192

A	Chip Gallery	196
B	Algorithmic Methods Flowcharts	200
C	Full list of Publications	202
C.1	Chapter 3	202
C.2	Chapter 4	203
C.3	Chapter 5	203
C.4	Chapter 6	203
C.5	Additional Publications	203

List of Figures

1.1	Scientific challenges affecting ISFET-based PoC Platforms	2
2.1	Current Health Expenditure (CHE) Analysis	9
2.2	Schematics illustrating elements composing a standard Point-of-Care device . . .	12
2.3	MOSFET structure and its ISFET counterpart as initially envisioned by P. Bergveld [81]	24
2.4	ISFET Implementation in CMOS [84] (© 2020 IEEE), and macromodel [85] (© 2003 IEEE)	25
2.5	Trapped Charge Analysis	28
2.6	Drift Analysis	30
2.7	Noise Analysis performed by Liu et al. [100] (© 2011 IEEE)	31
2.8	Temperature influence on ISFETs characteristic response [101]	32
2.9	Encapsulation examples	32
2.10	Previous ISFET Point-of-Care Platforms	34
2.11	Foundations of ISFET instrumentation	35
2.12	Extended input range ISFET architectures	38
2.13	Gate Modulations Approaches	39
2.14	Multisensing pixel proposed by Constandinou et al. [126] (© 2010 IEEE)	41

2.15	Multisensing opto-chemical output proposed by Huang et al. [127] (© 2015 IEEE)	41
2.16	ISFET PoC Applications and their R&D Cycle	44
3.1	ISFET Systems as Point-of-Care Platforms - Main Challenges and Barriers . . .	57
3.2	Sawtooth Oscillator Architecture [16] (© 2019 IEEE)	59
3.3	Chemically Controlled Ring Oscillator (CCRO) Architecture [16] (© 2019 IEEE)	62
3.4	Experimental setup for sensor characterisation [16] (© 2019 IEEE)	63
3.5	Schematic of the acquisition platform [16] (© 2019 IEEE)	64
3.6	Sawtooth Oscillator Characterization Results [16] (© 2019 IEEE)	65
3.7	Standard calibration curve [16] (© 2019 IEEE)	66
3.8	Drift and Noise Analysis for Sawtooth Architecture with $I_{Bias} = 1\mu A$ [16] (© 2019 IEEE)	68
3.9	Sawtooth Oscillator V_{Ext} characterisation [16] (© 2019 IEEE)	69
3.10	Chemically Controlled Ring Oscillator Characterization Results [16] (© 2019 IEEE)	70
3.11	Sawtooth Oscillator High Level Schematic [31] (© 2020 IEEE)	75
3.12	Simulation of linear OTA current under different biasing conditions [31] (© 2020 IEEE)	76
3.13	Simulation of Sawtooth Oscillator under different pH conditions [31] (© 2020 IEEE)	78
3.14	BlackPearl System Architecture [31] (© 2020 IEEE)	80
3.15	Measurement setup for characterisation of silicon prototype	81
3.16	Pixel Characterisation Curve [31] (© 2020 IEEE)	84
3.17	Characterization Analysis obtained from pixel characterisation curves	85

3.18	Chemical Sensor Characterization [31] (© 2020 IEEE)	86
3.19	Trapped Charge Calibration Results	88
3.20	Thermal Sensor Characterisation	89
3.21	Cross-Sensitivity Analysis	91
3.22	Lambda DNA amplification and detection, qPCR vs LoC	93
3.23	Ultra Low Power Pixel Architecture [50] (© 2020 IEEE)	95
3.24	Ultra Low Power Pixel Transient Signals [50] (© 2020 IEEE)	96
3.25	Ultra Low Power Architecture - Pixel Analysis [50] (© 2020 IEEE)	97
3.26	Quad-Sensing Pixel - Sensing elements cross-section [57] (© 2021 IEEE)	100
3.27	Quad-Sensing Pixel Architecture [57] (© 2021 IEEE)	101
3.28	Quad-Sensing System Architecture [57] (© 2021 IEEE)	104
3.29	Sensitivity Simulation Results [57] (© 2021 IEEE)	105
4.1	Schematic representation of a Diagnosis-on-a-Chip (DoC)	116
4.2	Digital Pixel Sensor (DPS) concept	118
4.3	Frame Rate Comparison based on the pixel architecture and # pixels [9]	119
4.4	Digital ISFET Sensor (DIS) pixel overview	120
4.5	Digital ISFET Sensor (DIS) pixel operation diagram	122
4.6	Digital ISFET Sensor (DIS) 8-T Compact Memory Architecture for In-Pixel Storage	123
4.7	Digital ISFET Pixel Calibration Architecture	124
4.8	Digital ISFET Sensor (DIS) Sensitivity Curves obtained with the two calibration modes [17] (© 2021 IEEE)	125
4.9	DIS Pixel and System-Level architecture and layout [17] (© 2021 IEEE)	128

4.10	ARM Top Level Architecture	130
4.11	Full System-on-Chip Integration	131
5.1	InstantDNA System Level Architecture	137
5.2	3D model of instantDNA chip cartridge	138
5.3	InstantDNA PCB with highlighted blocks	139
5.4	instantDNA General User Interface (GUI) example screens	140
5.5	InstantDNA Prototype	141
5.6	Trapped Charge Compensation Controller Architecture	141
5.7	Trapped Charge Calibration Results	142
5.8	PSD Analysis for different biasing conditions	144
5.9	Real-Time Drift Compensation Controller Architecture	147
5.10	Electrical Sensitivity using Real-Time Drift Compensation	148
5.11	Chemical Sensitivity using Real-Time Drift Compensation	149
5.12	Long-Term Monitoring Analysis without Real-Time Compensation	150
5.13	Long-Term Monitoring Analysis with Real-Time Compensation	151
5.14	36-Hour Exponential Fitting	154
5.15	160-Hour Exponential Fitting	155
6.1	JPEG Compression and Decompression Architecture	163
6.2	Real-Time Lab-on-Chip Platform, as presented in [13] (© 2021 IEEE)	165
6.3	Optimisation function results on a Δ PSNR and Δ CR space	167
6.4	Particle Swarm Optimisation Results [13] (© 2021 IEEE)	168
6.5	sEMG System High Level Architecture [46] (© 2021 IEEE)	172

6.6	sEMG Input Stage Architecture [46] (© 2021 IEEE)	174
6.7	sEMG Second Order Gm-C Low Pass Filter [46] (© 2021 IEEE)	175
6.8	Raw sEMG Frequency Response after conditioning stages	176
6.9	sEMG Envelop Detector [46] (© 2021 IEEE)	176
6.10	sEMG Channel Layout [46] (© 2021 IEEE)	178
6.11	Simulation Results from sEMG channel, as presented in [46] (© 2021 IEEE)	178
6.12	sEMG System Layout	180
A.1	LEGOLAS Chip - Winter 2018	196
A.2	BLACKPEARL Chip - Summer 2018	197
A.3	Goku Chip - Winter 2021	198
A.4	Himalaya Chip - Winter 2021	199
A.5	Multisensing Array - Pending of Fabrication	199
B.1	Trapped Charge Compensation Flowchart	200
B.2	Resolution Analysis Flowchart	201

List of Tables

2.1	Non-available Bio-fluids Analysis	18
2.2	Available Bio-fluids Analysis	19
2.3	ISFET Response under different operating conditions	26
3.1	Sawtooth Oscillator Performance Analysis [16] (© 2019 IEEE)	69
3.2	Sawtooth Oscillator Trade-off Analysis [16] (© 2019 IEEE)	70
3.3	CCRO Performance Analysis [16] (© 2019 IEEE)	73
3.4	CCRO Trade-off Analysis [16] (© 2019 IEEE)	73
3.5	Characterization Results [31] (© 2020 IEEE)	84
3.6	System Performance Summary [31] (© 2020 IEEE)	90
3.7	State-of-the-art Performance Comparison - ISFET Arrays [31] (© 2020 IEEE)	94
3.8	System Performance Summary [57] (© 2021 IEEE)	106
4.1	Digital ISFET Sensor - Simulated System Performance [17] (© 2021 IEEE)	126
4.2	Digital ISFET Sensor - State-of-the-art Comparison [17] (© 2021 IEEE)	126
4.3	ARM Cortex M Comparison [24]	129
5.1	Electrical characteristics for various biasing conditions	144
5.2	Limit of Detection Results	145

5.3	Long-term Monitoring Results	149
6.1	Optimisation Result Summary [13] (© 2021 IEEE)	168
6.2	Comparison between sEMG wearable platforms [46] (© 2021 IEEE)	178
6.3	Simulated System Performance [46] (© 2021 IEEE)	179

Abbreviations

ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
ALD	Atomic Layer Deposition
AI	Artificial Intelligence
APS	Active Pixel Sensor
CCO	Current Controlled Oscillators
CCRO	Chemically Controlled Ring Oscillator
CDs	Chronic Diseases
CHE	Current Health Expenditure
CKDs	Chronic Kidney Diseases
CMOS	Complementary Metal–Oxide–Semiconductor
CRDs	Chronic Respiratory Diseases
CR	Compression Ratio
DCT	Discrete Cosine Transform
DIS	Digital ISFET Sensor
DNA	Deoxyribonucleid Acid
DOC	Diagnosis on a Chip
DPCM	Differential Pulse-Code Modulation
dPCR	Digital Polymerase Chain Reaction
DPS	Digital Pixel Sensor
DNA	Deoxyribonucleic Acid
ELISA	Enzyme-Linked Immunosorbent Assay
FPN	Fixed Pattern Noise
FPU	Floating Point Unit
GUI	General User Interface
IC	Integrated Circuit
IoT	Internet of Things
ISF	Interstitial Fluid

ISFET	Ion-Sensitive Field Effect Transistor
JPEG	Joint Photographic Experts Group
LAMP	Loop-Mediated Isothermal Amplification
LBP	Low Back Pain
LoC	Lab-on-Chip
LoD	Limit of Detection
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MCU	Micro-Controller Unit
ML	Machine Learning
NAT	Nucleic Acid Test
NTC	Non-template control
OSR	Over-Sampling Ratio
OTA	Operational Transconductance Amplifier
PCR	Polymerase Chain Reaction
PG	Programmable Gate
PoC	Point of Care
PoCT	Point of Care Testing
PSNR	Peak Signal-to-Noise Ratio
PTAT	Proportional To Absolute Temperature
PVT	Process Voltage & Temperature
PWM	Pulse Width Modulation
RLE	Run-Length Encoding
RMS	Root Mean Square
RNA	Ribonucleic Acid
RPA	Recombinase Polymerase Amplification
sEMG	Surface Electromyography
SIMD	Single Instruction Multiple Data
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
TB	Tuberculosis
TC	Trapped Charge
TC-TI	Transconductance-Transimpedance
TTP	Time To Positive
UHC	Universal Health Cover
VCO	Voltage Controlled Oscillator
WHA	World Health Assembly
WHO	World Health Organisation

ZC Zero Crossing

Chapter 1

Introduction

1.1 Motivation

The recent wave of pandemics caused by infectious diseases since 2010, from MERS-CoV and Ebola to the most recent COVID-19, have exposed the vulnerabilities of healthcare systems across the globe while further widening the wealth gap between developed and developing countries. The challenges associated with the spread control of such diseases have catalysed a change in paradigm on diagnostics, moving from centralised facilities to the Point-of-Care (PoC).

In this context, precise, deliverable and inexpensive sensors are fundamental for developing such PoC platforms. This thesis focuses on a specific chemical sensor that has the potential to change the current PoC diagnostic landscape: Ion-Sensitive Field Effect Transistor, usually known as ISFET. First envisioned by Piet Bergveld in 1972 [1] and later fabricated in standard CMOS technology by Bausells et al. in 1999 [2], ISFETs have evolved over the last decade from single sensor configuration to massively-parallel arrays applied to DNA sequencing, integrating both sensing capabilities and instrumentation onto the same die. Leveraging on the benefit provided by CMOS technology in terms of size and cost, ISFET chemical imaging arrays have been recently incorporated onto portable diagnostic platforms for infectious diseases detection [3] and wearable platforms with multi-ion analysis potential [4, 5].

Despite this accelerated development, a set of technical and scientific challenges limits ISFETs' suitability and applicability for PoC diagnosis, as illustrated in Figure 1.1. These challenges can be classified into three groups: In the first place, the extensively studied ISFET non-idealities [6] resulted from standard CMOS fabrication, such as trapped charge and drift, establish strict requirements to ISFET instrumentations and restrain its limit-of-detection. Secondly, performing Deoxyribonucleic Acid (DNA) amplification detection and quantification on portable

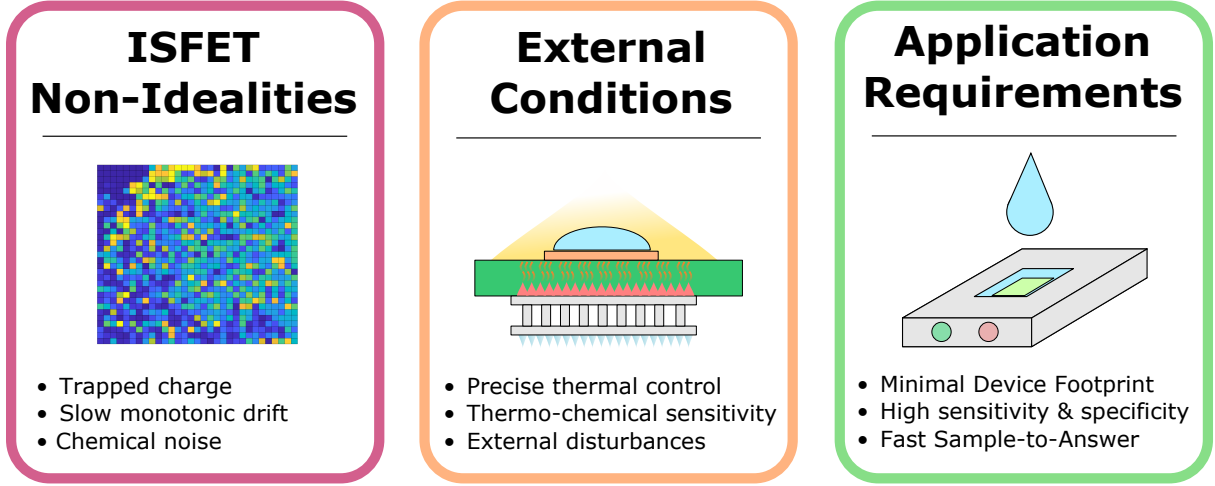


Figure 1.1: Scientific and technical challenges affecting the applicability of ISFET-based diagnosis platforms at the Point-of-Care

ISFET arrays require precise thermal control, minimal thermo-chemical cross-sensitivity and sensor resilience to changes on external conditions to maximise its accuracy. Finally, the requirements associated with its deployment at the PoC set a limit on the device footprint and power consumption to ensure test deliverability while requiring high sensitivity and specificity to the target pathogen.

Beyond these scientific challenges, there are additional barriers in diverse areas such as system integration, re-usability of device, chip manufacturing and encapsulation, or logistics. These barriers will need to be addressed for a successful commercial deployment of a PoC solution, but such solution is still requires scientific development to become a reality. These non-scientific challenges will remain out-of-the-scope of this thesis.

Hence, a new set of pixel architectures, design practices, adaptive algorithms and data-driven capabilities must be envisioned to overcome these challenges. These solutions should enhance ISFET PoC platforms' precision, deliverability, and adaptability to a wide range of applications while enabling operation under changing conditions. Such platforms would represent an invaluable tool to achieve rapid control of the spread of infectious diseases, moving another step closer on the quest towards a healthier and fairer world.

1.2 Research Objectives

With this motivation in mind, this thesis presents a vision for the next generation of ISFET-based PoC platforms, aiming to tackle the need for precise, inexpensive and deliverable tests as outlined by the WHO [7]. To achieve this vision, the thesis presents novel chemical pixel architectures and algorithmic methods with the potential to enhance adaptability and precision

without sacrificing form factor. The 3 key challenges to address in this thesis are illustrated in Figure 1.1.

The main research questions addressed throughout this thesis can be summarised as follows:

Question 1: How can we develop ISFET-based PoC platforms more adaptable to both non-idealities and external conditions?

Question 2: How can we reduce ISFET-based platforms footprint at a system level to enhance their deliverability to the PoC?

Question 3: How novel data-driven methods can help enhance the sensing capabilities of PoC sensors?

Each of these questions is mapped to the contents of each chapter.

1.3 Thesis Organisation

The multidisciplinary nature of the proposed questions requires the convergence of various research fields on a single solution. The structure of this thesis reflects this journey, with five chapters addressing the different angles of the research questions:

1.3.1 Chapter 2: ISFETs at the Point-of-Care: State-of-the-Art and Challenges

Chapter 2 reviews the theoretical background and the state-of-the-art on Point-of-Care devices. This chapter starts by introducing the potential impact of Point-of-Care Testing (PoCT) in the context of e-Health, deep-diving onto the elements forming each PoC device: Bio-markers, sample and transducers. Based on this review, I propose a classification for PoC devices based on its application context and requirements.

In this context, I introduce Ion-Sensitive Field Effect Transistor (ISFET) chemical imaging platforms. Throughout this section, I review sensor operation, non-idealities and the platform challenges for its deployment at the PoC. Based on the research focus of the different architectures proposed over the last decade, I identify three main trends, serving as the classification caveat and setting the scene for the proposed approach in Chapter 3.

1.3.2 Chapter 3: Oscillator-based ISFET Architectures

Chapter 3 addresses the question:

How can Oscillator-based ISFET architectures enhance pixel adaptability?

In this chapter, I present novel Oscillator-based ISFET architectures that provide both programmability and multi-sensing capabilities to enhance adaptability at a pixel level. These novel pixels are integrated as part of a large-scale ISFET array, demonstrating a dual-sensing operation by extracting thermal and chemical information from the same spatial point. Furthermore, the pixel operation point can be modified through off-pixel programmability, opening the doors for adaptability-focused software methods described later in Chapter 5.

1.3.3 Chapter 4: Towards a Diagnosis-on-a-Chip: Digital ISFET Sensor

Chapter 4 provides a vision on the question:

How can we further integrate ISFET sensing elements and processing capabilities to reduce platform footprint and enhance deliverability?

Motivated by the recent COVID-19 pandemic situation, this chapter introduces the concept of “Diagnosis-on-a-Chip”, urging to blend sensing and computational capabilities further, leveraging CMOS technology’s potential for platform miniaturisation to achieve a highly deliverable PoC device. I proposed a novel Digital ISFET Sensor, merging sensing elements, ADC, and memory blocks on a single pixel. This highly parallel architecture increases the system scalability to large arrays, eliminating bulky memories and acquiring the entire frame on a single ADC cycle. Furthermore, I illustrate the integration of this architecture with computational capabilities through an example implementation with an ARM Cortex M3, realising the proposed concept of “Diagnosis-on-a-Chip”.

1.3.4 Chapter 5: Software methods for adaptability enhancement of ISFET PoC Platforms

Chapter 5 focus on the following research question:

How can we enhance sensor adaptability by using software methods to control pixel programmability?

Leveraging on the programmable capabilities presented in Chapter 3, this chapter explores a set of controllers and digital signal processing techniques to overcome the limitations imposed by ISFET non-idealities and electrochemistry effects. For this purpose, I developed a portable platform to enable prototyping of software methods emulating the conditions present at the Point-of-Care.

1.3.5 Chapter 6: Software Opportunities for ISFET Sensing and beyond

Chapter 6 covers the last of the proposed research questions:

How novel data-driven methods can help enhance the sensing capabilities of PoC sensors?

This broader analysis explored the opportunities arising from incorporating data-driven models to the sensing domain for overcoming the state-of-the-art challenges present on PoC devices. In this chapter, I explore two systems to exemplify these opportunities: Firstly, the performance on an ultra-high frame rate ISFET array is improved by developing a custom compression algorithm through learning-based optimisation. Secondly, a novel approach to surface electromyography sensing is proposed to enhance system scalability based on the insight provided by data-driven models. These two examples serve as proof of concept of this promising research approach.

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Chapter 2

ISFETs at the Point-of-Care: State-of-the-art and Challenges

2.1 Introduction

In 2005, all state members of the World Health Organisation (WHO) signed the World Health Assembly (WHA) resolution, which represented a commitment of every state to achieve Universal Health Coverage (UHC) [1]. This commitment represented “a collective expression of the belief that all people should have access to the health services they need without the risk of financial ruin or impoverishment” [2].

This resolution established the concept of e-Health as a critical element in modern healthcare systems and one of the highest priorities for the WHO [2]. e-Health refers to the use of information and telecommunication technologies to support healthcare services. e-Health includes the devices, analytics, infrastructure and connectivity technology that makes possible the remote delivery of healthcare services. Leveraging recent developments in connectivity, e-Health systems would enable physicians to access patients’ medical history and health status, facilitating remote healthcare (also known as telehealth or telemedicine). Furthermore, e-Health would provide patients with evidence-based quantitative data, supporting patients’ health and wellness and empowering them to make the right choices [3].

The deployment of e-Health as part of modern healthcare systems is likely to impact three key areas:

1. **Medical:** Healthcare systems are currently struggling to provide rapid diagnosis and continuous monitoring of patients health conditions due to its current diagnostic model, based on centralised laboratories. This model leads to poor prognosis due to late diagnosis,

especially significant on chronic diseases [4, 5], and a slow response to health emergencies such as the recent COVID-19 outbreak [6, 7].

Hence, reducing time-to-diagnosis and enabling real-time or periodic patient monitoring is crucial to enable a timely and personalised treatment and precise control of the disease. e-Health systems would overcome current limitations by providing remote access to medical history while enabling patient health monitoring and treatment compliance. Furthermore, e-Health would open new opportunities for e-prescribing and e-booking.

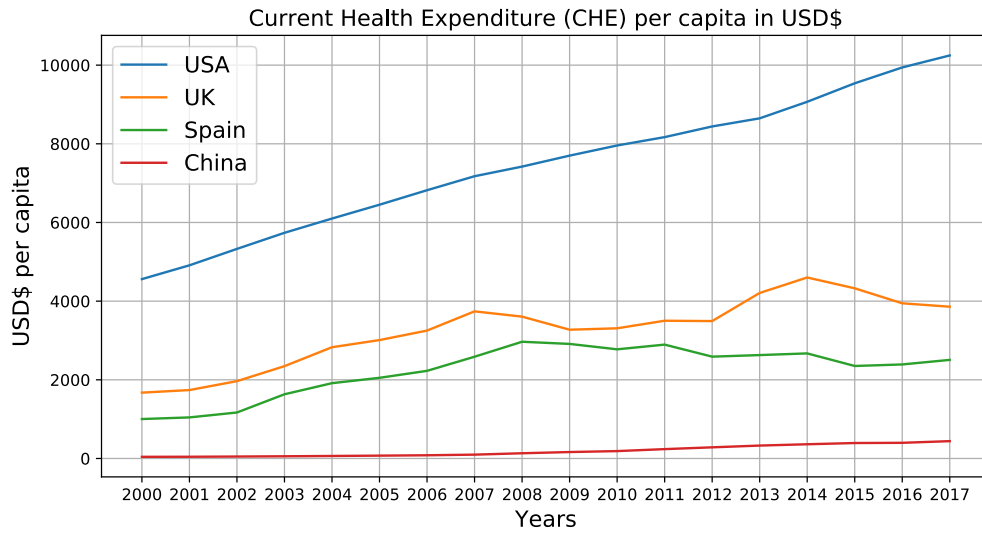
2. **Economic:** The increasing cost of national health systems is raising concerns over its long-term economic viability. Figure 2.1 presents this cost evolution, illustrated both through the Current Health Expenditure (CHE) per capita [8] (Fig. 2.1a) and CHE in % of Gross Domestic Product (GDP) [9] (Fig. 2.1b). The WHO estimates that over 7.2 trillion US\$ were invested in 2015 on healthcare systems across the globe, the equivalent to 10% of the global GDP [10].

To ensure the financial viability of healthcare systems, improvements in health efficiency need to be explored without compromising the quality of healthcare services. e-Health systems have the potential to improve healthcare delivery through the early diagnosis and control of diseases. This approach would potentially lead to fewer hospital admissions, reduced length of hospital stays and optimised drug treatments while improving physicians productivity through e-appointments [11]. These e-appointments would also reduce the number of nonattendance and no-shows without degrading the health service quality.

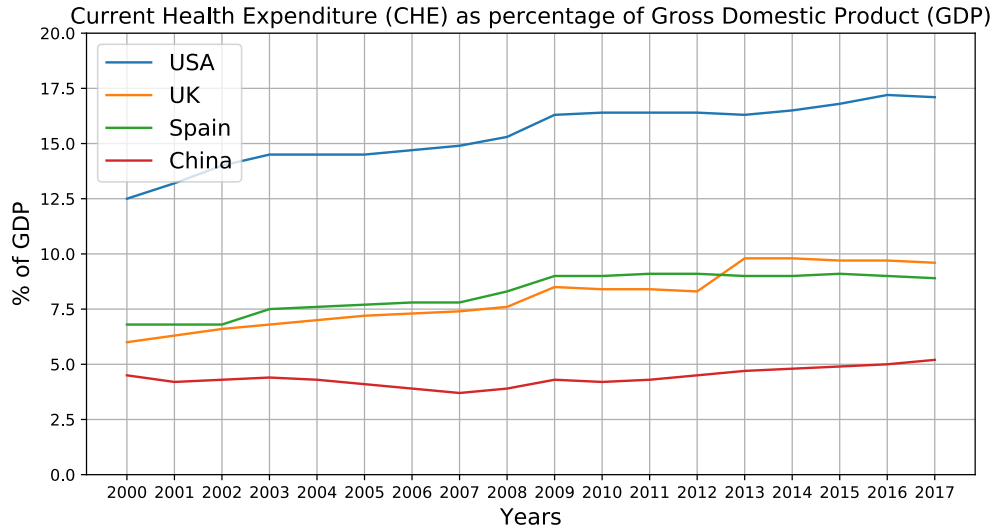
3. **Social:** The current centralised model for healthcare delivery creates social differences in the availability and quality of healthcare services. A recent study showed that the centralised model leads to a “distance decay association” [12], confirming a correlation between the distance from healthcare centres and the health outcomes. 77% of the studies analysed showed that greater distance to the nearest healthcare centre leads to worse health outcomes. This imbalance is especially significant in rural areas and developing countries, where healthcare services are inconvenient or inaccessible to a large proportion of the population.

Furthermore, recent studies have shown that the prevalence of infectious diseases in specific regions is closely linked with inequality and economic development [13, 14]. Hence, a distributed healthcare model, where medical and diagnostic capabilities are accessible on smaller clinics, can significantly impact the medical outcomes and wealth distribution worldwide. e-Health is expected to be the catalyst of this paradigm shift, providing small clinics and remote communities with the capability to provide quality health services.

The design and implementation of e-Health on healthcare systems require the cooperation of multiple stakeholders and social agents, overcoming barriers in diverse fields such as law,



(a) National expenditure in US\$ per capita [8]



(b) National expenditure in % of Gross Domestic Product (GDP) [9]

Figure 2.1: Current Health Expenditure (CHE) Analysis

economics, or technology [2]. In the first part of this chapter, I analyse the technological advances that can enable the adoption of e-Health systems.

The accelerated development of consumer electronics and telecommunications, fuelled by Moore's law, has established the foundations for the technological deployment of e-Health systems. The international roll-out of telecommunications technologies, such as 4G or more recently 5G, enables ubiquitous connectivity. Leveraging on this connectivity network, e-Health elements such as high quality conferencing for e-appointments or advanced databases techniques for medical record storage are technologically possible [15].

However, to deliver quality healthcare services, medical doctors require clinically relevant information from the patient to provide diagnosis and subsequent treatment. As an e-Health system cannot rely on centralised laboratories to provide accurate diagnostic information, new diagnostic approaches must provide clinical information near or at the patient's Point-of-Care (PoC).

2.2 Point-of-Care Devices

These e-Health diagnostic platforms, usually referred to as Point-of-Care (PoC) devices or Point-of-Care Testing (PoCT), bring clinical testing closer to the patient, enabling the rapid acquisition of clinically relevant information to provide a diagnosis and subsequent treatment [11]

PoC devices must meet certain distinct specifications to be considered as such. The ASSURED criterion was initially proposed by the World Health Organisation [16] as a framework for PoCT, and since then, different criteria have been presented to address this evolving concept [11, 15, 17]. The most common characteristics highlighted for PoCT are the following:

- Quick response, with a maximum response time of 1 hour
- Accurate and precise, yielding robust results with high sensitivity and specificity
- Low-to-moderate cost, both individual tests and result reader (if required). The exact value varies depending on the economical setting, ranging from < \$1 to around 10\$
- Monolithic structure, capable of performing the entire test from untreated samples without external equipment
- Simple-to-use, suitable for being operated by untrained or minimally trained personnel
- Portability and robustness, as the tests should be carried in the field or at small clinics
- Minimal involvement from the user. The user should only be expected to provide the sample or wear the device
- Long term stability of sensing element, enabling extended self-time before delivery
- Use minimally invasive methods to obtain the biological fluid
- Multiplexing capabilities, capable of detecting and distinguishing multiple analytes on a single test

- Provide relevant clinical information, with a validated relationship between the biomarker and the condition under test
- Connectivity to common devices, such as smartphone or PC, and to the cloud for rapid and secured transmission of clinical data

These characteristics are seldom achieved by any PoC device, with different devices focusing on specific aspects. To further understand the nature of these trade-offs, the different elements that compose PoC devices are now analysed in detail.

2.2.1 Elements of Point-of-Care Devices

The essential elements forming most PoC devices are illustrated in Figure 2.2. Each of these elements is now analysed in detail along with its state-of-the-art.

Bio-markers

When analysing or designing a PoCT device, the first element to consider is the bio-marker used to understand the clinical condition. A biomarker is commonly defined as “objective indications of medical state observed from outside the patient which can be measured accurately” [18]. This broad definition includes a range of medical signs: from blood pressure to pathogen nucleic acids in the bloodstream. However, for a biomarker to be useful for clinical purposes, it must consistently predict or indicate a clinical condition or outcome, either beneficial or detrimental for the patient [18].

In PoCT devices, a range of bio-markers have been explored to predict the clinical outcome. The most relevant bio-markers are:

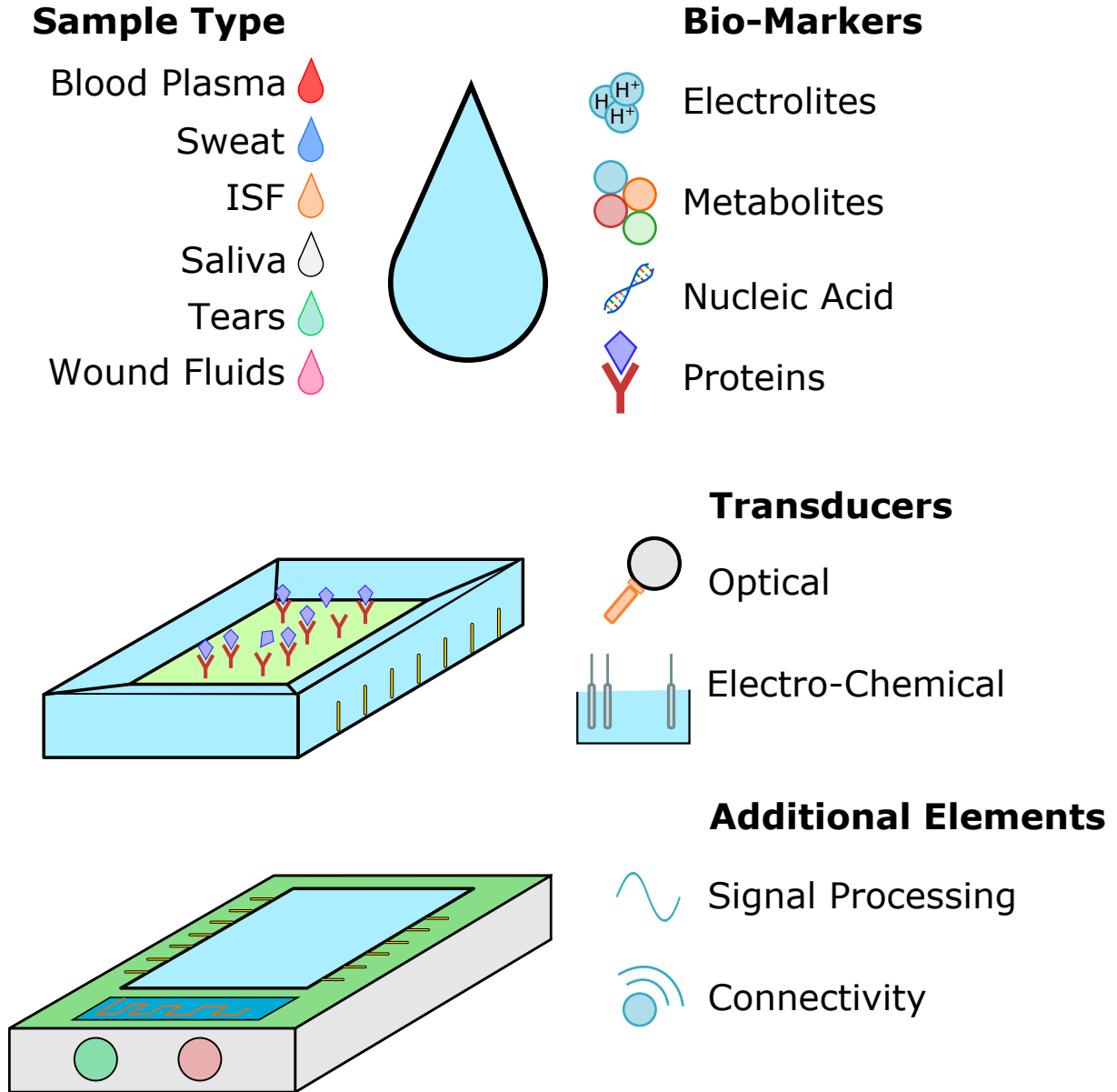


Figure 2.2: Schematic illustrating the elements composing a standard Point-of-Care device, highlighting (from top to bottom, left to right) the different sample types, the various biomarkers that can be analysed from a sample, the transducer modalities used at the Point-of-Care to be detected and the additional elements that could be included on such systems

- **Electrolytes** \Rightarrow Electrolyte refers to any charged ion present of our body fluids. The concentration of the electrolytes of our body, such as Na^+ [19, 20], Ca^{2+} [21], Cl^- [20, 22], K^+ [19] or pH [21, 22], have been extensively explored as indicators of various diseases, such as Cystic Fibrosis (CF) [20] or renal failure [23], as well as dehydration [19] or blood acidosis [21, 22]. However, it needs to be noted that these electrolytes can rarely point to a single clinical outcome [24].

Finally, the concentration of these electrolytes can be used as the complementary biomarker

to detect other bio-markers. An example of this is the detection of Nucleic Acids through DNA amplification, which utilise variations of pH concentration to determine the presence of the target DNA sequence [25].

- **Metabolites** \Rightarrow Metabolite refers to any molecule used, involved or produced in a metabolic process. Abnormal concentrations of body metabolites are tightly linked with chronic diseases such as diabetes [20]. For this purpose, metabolites such as glucose [20, 22], lactate [22] and uric acid [26] are used as biomarkers of these diseases.
- **Nucleic Acids** \Rightarrow Nucleic acids are large polymers used to create, encode and store information of every living cell. They are formed by monomers called nucleotides, constructed by a phosphate, a sugar and a base. Depending on the sugar structure, nucleic acids can be deoxyribonucleic acid (DNA) or ribonucleic acid (RNA). Nucleic acid bases can take four different forms: Adenine (A), Guanine (G), Cytosine (C) and Thymine (T) on DNA / Uracil (U) on RNA.

The molecular analysis of nucleic acids targets a DNA sequence characteristic of a specific pathogen. Target nucleic acid can be detected rapidly with high sensitivity and specificity employing amplification protocols, such as Polymerase Chain Reaction (PCR) [27] or more recently Loop-Mediated Isothermal Amplification (LAMP) [28] and Recombinase Polymerase Amplification (RPA) [29]. These protocols replicate the target RNA or DNA, amplifying the detectable signal. This set of techniques has been extensively used on PoCT devices to detect infectious diseases [25, 30–32] and tumoural markers [33, 34].

More recently, circulating microRNA present on extracellular fluids has been explored as a promising biomarker [35]. MicroRNA, or miRNA, refers to non-coding RNA molecules with small sizes regularly released to extracellular environment for cell-to-cell gene expression regulation [30, 36]. A recent study has established a link between circulating miRNA levels to Tuberculosis (TB) infection [37], and it has also been explored as a potential cancer biomarker [36]. However, miRNA analyses still lack the sensitivity and specificity required for clinical diagnosis [36].

The main drawback of using Nucleic Acids on PoCT is the sample preparation performed to extract the target nucleic acids from the sample, which required cell filtration and lysis. Furthermore, protocols such as PCR requires thermal cycling through different temperatures, increasing the cost, the size and the complexity of the system [31]. A solution for this would be using isothermal amplification protocols such as LAMP, whose patent protection expired in 2019 [31].

- **Proteins** \Rightarrow Proteins are large bio-molecules formed by long chains of amino acids. Biological systems rely on proteins for performing a wide range of functions - from forming cell structures and enabling movement to catalyse metabolic reactions. Hence, proteins represent a powerful bio-marker candidate for the detection of different health conditions.

Proteins detection has been integrated on PoCT devices to perform two functions. Firstly, enzymes are employed on electrochemical sensing devices as reactions catalyst, as well as required reagents for Nucleic Acid amplification protocols [31]. Furthermore, leveraging on the availability of highly sensitive and specific immunoassays [38, 39], proteins have been widely explored as biomarkers for early diagnosis of infectious diseases [30], diagnosis and monitoring of chronic diseases [4], and cardiovascular diseases [5]. Last but not least, these immunoassays have been applied for the detection of inflammation markers [40], tumour markers [41], and markers of neurological disorders such as stress or depression [42].

Sample

The choice of the sample fluid, also known as biofluid, for Point-of-Care Testing is determined by a wide range of conditions, such as the bio-marker under test, the sample availability or continuous monitoring requirements. This choice would determine the necessary steps for sample preparations required, as well as the expected correlation and time lag with blood levels [43].

The most commonly used biofluids are now analysed:

- **Blood plasma:** Blood plasma is considered the reference bio-fluid, as its composition and analyte concentrations are tightly linked with clinical conditions and clinical outcomes.

For blood plasma to be used for Point-of-Care Testing, it needs to be extracted in an easy and minimally invasive way. For this purpose, sampling methods based on finger pricks and heel pricks have been extensively used on commercially successful products such as glucose monitoring. More recently, methods based on micro-needles [44] have been proposed to reduce patient discomfort and infection risk.

However, blood plasma composition is one of its main drawbacks, usually requiring sample preparation steps to enable reliable sensing of specific bio-markers [32].

- **Sweat:** Sweat refers to the fluid secreted by the sweat glands, located mostly at the epidermis. Sweat is secreted for temperature control purposes, allowing the control of body temperature through the secretion of water to the skin. This secretion ranges between 0.1 and $2 \mu L \cdot min^{-1} \cdot cm^{-2}$ [43], and can be stimulated through iontophoresis to enhance the biofluid sample rate [45].

Different molecules are incorporated into the sweat flow throughout the secretion process that can be used as a biomarker. Electrolytes such as Na^+ , K^+ , and Cl^- are present in high concentrations on sweat [46], and larger metabolites like glucose and lactate can be found in smaller concentrations. However, these analytes present a poor correlation with the concentrations found in blood, presenting a significant dependency on the sweat

rate. Techniques that promote localised and controlled sweat secretion even for resting individuals like iontophoresis, while integrating it side-by-side with sensing elements [45], have the potential improve this correlation. Larger hormones such as cortisol present a better correlation with blood levels [47], showing potential for further hormone sensing in sweat [43].

Despite sweat being readily available on human skin, the sample volume represents a major challenge. A controlled, stable flow rate is vital to avoid dilution effects on analytes concentrations. To extract this sweat and transport it to the sensing element reliably, a wide range of solutions have been explored based on patches, badges and tattoos in direct contact with the skin [19–21, 48–50]. Most recently, a range of microfluidic devices to capture and store sweat have been proposed, reducing the sample required for sensing [22, 51].

- **Interstitial Fluid (ISF):** The Interstitial Fluid, or ISF, refers to every fluid that surrounds our cells. For the purpose of biofluid sampling, ISF sampled from the epidermis cells is the most commonly used. Analytes enter ISF following three main mechanisms: transcellular, which refers to the diffusion through the capillary plasma membrane; paracellular, which is the diffusion through the space between cells; and transcytosis, which englobes the vesicular transport through the cell.

Thanks to these various entry routes available for analytes to enter ISF from capillary blood, ISF presents a high analyte concentration correlation with blood plasma. This correlation is especially significant for small molecules, such as electrolytes like Na^+ or K^+ [52] or small metabolites like lactate or glucose. When moving to larger molecules, such as proteins, the ISF/plasma correlation ratio follows an inverse logarithmic trend with the molecular weight of the analyte [53] due to the filtering effect from blood to ISF [43].

The ISF diffusion mechanisms create a lag in the analyte concentration on ISF, which is estimated to be from 5 to 10 minutes [43]. To enable ISF extraction, techniques such as microdialysis or reverse iontophoresis have been explored and applied to commercial glucose monitoring such as GlucoDay CGM and GlucoWatch CGM, respectively. However, these methods present several limitations. In the case of microdialysis, the need for mechanical elements and the required sample extraction time limit the portability and increase the lag; and the use of currents in the reverse iontophoresis can lead to skin irritation during long term monitoring. To overcome these limitations, micro-needles arrays have been proposed. This array pierces the skin and creates a channel through which analytes can flow to an ex vivo sensor [54]. This solution positions ISF as a promising biofluid for continuous monitoring of analytes, especially on wearable solutions [43].

- **Saliva:** Saliva refers to the heterogeneous fluid secretion generated by the salivary glands

in the oral cavity, composed of a range of biomarkers that could potentially be used for sensing. Electrolytes on saliva have been extensively studied as a marker for hydration status, but their concentration presents a large variability [55] that difficult its usability. Larger metabolites such as glucose or lactate present a better correlation with blood samples [56], but fasting conditions are required to avoid food contamination. Hormones are also explored on saliva, presenting a good correlation with the unbound fractions in blood plasma on unstimulated conditions. However, under stimulated flow, these concentrations become quite dependent on the saliva release rate [43]. Similar effects are present on antibodies sensing with concentration levels significantly lower than plasma, although certain pathogen-specific antibodies (such as HIV) [57, 58] remain at detectable levels for laboratory or point-of-care diagnosis.

One of the main benefits of saliva as a bio-fluid is the relatively easy sample collection mechanism and lack of preparation requirements [43]. However, it presents several limitations due to the sample heterogeneity caused by in-mouth mixing of saliva from different sources, as well as variability due to the sensing location. The salivary composition generated on each saliva gland present significant differences, with additional heterogeneity due to subject age, gender or stimulus [59]. Furthermore, the secretion rate presents a large dynamic range (from 500 mL up to 1.5L a day) with wide variations between day and night flow rate and highly influenced by sensory stimulation [60]. The saliva generated during stimulation periods also vary in concentration depending on stimulation source and saliva rate [60]. For this reason, most diagnostic mechanisms rely on unstimulated saliva to achieve consistent sensing.

- **Tears:** Tears refers to the bio-fluid secreted by the lacrimal glands, whose primary function is eye hydration and lubrication while removing irritants. Tears composition is directly diffused from blood, leading to a high correlation between blood and tear concentrations [49]. This correlation has been demonstrated in both electrolytes and metabolites like glucose [61]. Furthermore, large molecules have been explored to diagnose both eye conditions and whole-body conditions [62, 63].

Tears can be acquired and integrated with sensing elements through contact lenses, enabling non-invasively continuous monitoring. However, tears present similar problems as sweat, as the tear samples are small, and variations in tear production create changes in the analyte concentrations. Furthermore, the lack of control over tear production through stimulation and the rapid evaporation of these small volumes makes tear sensing challenging.

- **Wound fluids:** Wound fluids refers to any fluid generated by or around a wound, usually on the epidermis. Wound fluids are usually utilised to assess and monitor the wound status through local biomarkers, such as pH, uric acid or bacterial metabolites.

To retrieve these biomarkers from the wound without interfering with the healing process, sensing elements and sample collection methods are integrated with bandages and wound dressing [41].

Tables 2.1 & 2.2 summarises the characteristics, requirements and applications of these biological fluids, separating them onto non-available and available fluids. In addition to these classical sample types, the recent COVID-19 pandemic has shown that nasal swabs can be key for pathogen detection. However, this sample type is specific to pulmonary-related diseases, narrowing its wider applicability.

Table 2.1: Non-available Bio-Fluids Analysis

Bio-Fluid	Sample Rate	Lag time	Extraction Techniques	Bio-fluid benefits	Bio-fluid limitations	Biomarkers present	Concentrations	References
Blood plasma	-	-	Finger prick Heel prick Microneedle Microdialysis	High Clinical Value	Requires sample preparation steps Requires invasive sample extraction	Electrolytes	7.36 - 7.44	[4, 30, 36, 39, 43]
						>PH	1.36 - 145 mM	
						>Na ⁺	98 - 107 mM	
						>Cl ⁻	3.3 - 5 mM	
						>K ⁺	2 - 2.6 mM	
						>Ca ²⁺	3.3 - 6.7 mM	
						Metabolites	0.36 - 1.3 mM	
						>Glucose	200 - 400 uM	
						>Lactate		
						>Uric acid		
						Nucleic Acids		
						Proteins		
						>Cortisol	30 - 160 ng/mL	
						>Dopamine	0 - 0.25 nM	
						>Neuropeptide-Y	0.14 - 0.6 pM	
Sweat	0.1 to 2 uL/(min * cm ²)	1 - 10 minutes	Absorption pad Iontophoresis	No sample preparation required Suitable for continuous monitoring	Low samples volume Affected by evaporation Unclear correlation with blood concentrations	>Electrolytes (IL-6)	0 - 4.3 pg/mL	[15, 43, 48-50, 64]
						>PH	3.0 - 8.0	
						>Na ⁺	10 - 100 mM	
						>Cl ⁻	10 - 100 mM	
						>K ⁺	1 - 18.6 mM	
						>Ca ²⁺	0.41 - 12.4 mM	
						Metabolites		
						>Glucose	10 - 200 uM	
						>Lactate	5 - 20 mM	
						>Uric acid	2 - 10 mM	
						Proteins		
						>Cortisol	8 - 141.7 ng/mL	
						>Neuropeptide-Y	0.8 - 2.9 pg/mL	
						>Cytokines (IL-6)	8 - 140 ng/mL	
Interstitial Fluid	~10 uL/(min * cm ²)	5 - 15 minutes	Microneedle Reverse iontophoresis	No sample preparation required Good correlation with blood concentrations	Require invasive sample extraction	Electrolytes	135 - 145 mM	[43, 49]
						>Na ⁺	3.3 - 5 mM	
						Metabolites		
						>Glucose	4.1 - 6.9 mM	
						>Lactate	0.5 - 10 mM	

Table 2.2: Available Bio-fluids Analysis

Bio-fluid	Sample Rate	Lag time	Extraction Techniques	Bio-fluid benefits	Bio-fluid limitations	Biomarkers present	Concentrations	References
Tears	~1 uL/min	-	In-eye direct contact Microcapillary tube	No sample preparation required Suitable for continuous monitoring	Unclear correlation with blood concentrations Challenging integration of multiplexing capabilities	Electrolytes		[43, 49, 64]
						>pH	6.5 - 7.8	
						>Na+	80 - 161 mM	
						>Cl-	106 - 130 mM	
						>Ca2+	0.4 - 1.1 mM	
						Metabolites		
						>Glucose	0.2 - 1 mM	
						>Uric acid	200 - 400 uM	
						>Urea	32.8-138.5 mg/100 ml	
						Proteins		
Saliva	~10-100 uL/min	10 minutes	In-mouth direct contact Spitting Suction	No sample preparation required	Require patient compliance for sample extraction	>Cytokines (IL-6)	100 - 200 pg/mL	[15, 43, 49, 64]
						Electrolytes		
						>pH	6.2 - 7.6	
						>Na+	20 - 80 mM	
						>Cl-	20 - 100 mM	
						>K+	30 - 100 mM	
						Metabolites		
						>Glucose	0.22 - 0.72 mM	
						>Lactate	0 - 0.4 mM	
						>Uric acid	11 - 250 uM	
Wound fluids	-	None	Microcapillary Absorption pad	No sample preparation required Simple sample collection Integration with drug delivery	Low volumes captured Local assessment only Unclear relationship between wound status and biomarkers	Proteins		[49, 64]
						>Cortisol	0.05 - 0.5 mg/dL	
						>Neuropeptide-Y	10 - 12 mM	
						Electrolytes		
						>pH	7.15 - 8.9	
Wound fluids	-	None	Microcapillary Absorption pad	No sample preparation required Simple sample collection Integration with drug delivery	Low volumes captured Local assessment only Unclear relationship between wound status and biomarkers	Metabolites		[49, 64]
						>Lactate	>7 mM	
						>Uric acid	250 - 750 uM	

Transducer

The transducer element converts the original signal generated by the biomarker to a processable signal on another domain. The output domain must facilitate the signal acquisition, interpretation and storage. The main transducers modalities explored for Point-of-Care applications are optical and electrical transducers, which are the focus on this review. Other modalities, such as cantilever [65] or piezoelectric [66, 67], have less penetration on the field of PoCT devices and remain out of the scope of this thesis.

- **Optical:** Optical refers to any transducer element that produces changes in its optical properties when the target biomarker is present. The most common modalities of optical transduction are:
 - Colorimetry: Modification of light absorbance based on the concentration of an analyte. This technique is used on wearable devices [22] and on paper-based PoCT platforms [31, 41]
 - Fluorescence: Emission of light in the presence of the target analyte. This technique is widely established as the golden standard for nucleic acid tests based on DNA amplification [31, 39] and has been integrated on both paper-based and microfluidic platforms [41].
- **Electrochemical:** Electrochemical transducers convert the concentration of a target analyte to a modulated electrical signal. Several configurations of electrochemical sensors have been explored in the literature:
 - Potentiometry: Measure the potential created by the difference in concentration between a reference electrode and an ion-selective electrode. This method is used to detect electrolytes such as Na^+ or K^+ in a wearable manner [21, 51]
 - Cyclic voltammetry: Measure the current response to a cyclic sweep of the reference electrode. This current will peak at a specific voltage, indicating the analyte and its concentration [66]
 - Amperometry: A fixed potential is applied to the reference electrode, creating a current between the working and the counter electrode proportional to the concentration of the target analyte. Different electrolytes have been detected in a wearable way using this sensing mechanism [50], as well as metabolites such as glucose [54].
 - Impedance Spectroscopy: More recently, electrochemical impedance spectrography has risen as a promising sensing modality to detect analytes with well-defined charges, thanks to novel materials that provide promising Limit-of-Detection [68]. This sensing modality measures variations in resistance or capacitance in the presence of certain biomarkers [69].

2.2.2 PoC Devices Classification

Various classifications have been proposed in the literature to categorise Point-of-Care devices. The most popular classification is the division by usability between “Portable” and “Wearable” devices, used in most of the recent reviews [41, 49]. However, this classification disregards both the target application and its socio-economic and geographical context, creating a false impression of homogeneity of requirements between all devices categorised as portable or wearable. On the other hand, Nayak et al. [39] proposed an alternative approach focused on use cases on different setups, categorising the devices based on budget and level of infrastructure required for operation.

Here I propose an application-driven classification of Point-of-Care devices, looking at the context in which each PoC device is required and its implications on the designed solutions.

Health and well-being

Over the last decade, a wide range of devices has been proposed to monitor human health status, both for well-being tracking and athletic performance. The overwhelming majority of these devices are envisioned to be used in the developed world, mainly adopting optical transducers when deployed on commercial solutions.

The success of these PoC devices has widened the sensing scope, targetting additional biomarkers beyond physiological signals that could enable further insights into human biochemical processes. However, these devices are constrained by certain specifications particular to this application:

- **Continuous monitoring:** The changing nature of human health require continuous monitoring to enable the assessment of long-term evolution of well-being - or performance in the case of athletes.
- **User comfort and wearability:** To achieve continuous monitoring, these devices require adaptation to dynamic activities, which is best achieved through the integration as part of wearable structures.
- **Analyte Multiplexing:** To enable a comprehensive analysis of healthcare, multiplexing of different target biomarkers have been extensively explored.

Following the need for user comfort, non-invasive samples such as sweat and saliva have increased in popularity, collected directly from skin or mouth [49]. The wearability of these devices is achieved by using flexible substrates [19, 20, 22, 42, 50] to ensure skin conformity, or

readily-available devices such as mouth-guards [26], or retainers [70]. Colourimetric recognition elements or printed electrodes have been integrated into these structures to perform multi-sensing analysis of several analytes. The measurements obtained from these sensors are either read by a smartphone camera [22] or directly acquired and transmitted via Bluetooth [20].

Diagnosis & Monitoring of Chronic Diseases

The prevalence of Chronic Diseases (CDs) has experienced a rapid increase over the last decades, especially in developed countries. Studies in the United States of America estimated that 45% of the population suffer at least one chronic disease [71], becoming one of the leading causes of death worldwide. This prevalence leads to large expenditures in healthcare, with over 50% of the total health expenditures related to CDs [4]. The most prominent conditions are chronic respiratory diseases (CRD), diabetes, Low Back Pain (LBP) and chronic kidney diseases (CKD).

The early diagnosis and regular monitoring of these diseases can help to improve their management and potentially prevent their progression. PoCT devices for CDs screening and monitoring share several conditions:

- **Rapid response:** To monitor these diseases efficiently and enable early detection of condition deterioration, a rapid sensor response is required.
- **Easy-to-use:** As the management of these diseases usually needs to be performed routinely by the patient, the devices require to be relatively easy to use, although some familiarity with the sensing mechanisms can be assumed.
- **Long-term stability:** These devices are expected to accomplish high precision over a long time, even if that is achieved at the expense of some user discomfort from minimally invasive sampling methods. Furthermore, the sensing element needs to maintain consistent sensitivity throughout its useful life, as this element usually represents the weakest system element. Hence, the target electrochemistry of the sample needs to be considered when designing the transducer.

The most successful example of a Chronic Disease management device is the glucose monitoring device from ISF, already in the commercialisation phase.

For pathogen detection, conventional tests such as Enzyme-Linked Immunosorbent Assay (ELISA) for protein detection have been adapted to micro-fluidic Point-of-Care devices. Leveraging on the miniaturisation of these devices, these Lab-on-a-Chip presented promising results in terms of cost, test speed, and throughput [4].

Diagnosis of Infectious Diseases

Infectious diseases are one of the primary causes of mortality in developing countries, impacting the young population where more than half of the deaths are related to these diseases [30, 72]. A timely, portable and affordable diagnosis has been highlighted as key to alleviate this burden [16, 72–74].

Various PoCT devices have been recently explored to address this urgent need, aiming for on-the-field diagnosis of the most prevalent infectious diseases: Malaria, Dengue & Ebola, Zika, TB and HIV. The conditions at which these tests need to be performed have determined the specifications:

- **Inexpensive:** The economic context of these countries establish limits on the cost per test of these devices.
- **Portable and disposable:** The lack of infrastructure of the testing context requires portable solutions that can be readily used and easily disposed.
- **Sample-to-answer Requirements:** The shortage in trained personnel and specialised equipment requires new design considerations that ensure correct diagnosis when used by untrained individuals.

To overcome these limitations, two main solutions have been explored. Firstly, the integration of precise Nucleic Acid Tests (NAT) on portable platforms, leveraging the recent development of isothermal amplification protocols [31]. The elimination of the thermo-cycling instrumentation required for PCR protocols has facilitated the integration of sensing systems on compact form factors. Secondly, microfluidic technologies hold great promise to perform various lab functions, such as sample preparation, cell sorting or reagent mixing, in a precise manner using inexpensive and disposable materials [30].

Other applications

Other applications have been explored for PoCT devices, such as cancer diagnosis [33, 36, 75], environmental testing or law enforcement [39]. These applications, despite their importance, are beyond the scope of this thesis.

2.3 ISFET at the Point-of-Care

In the context of accelerated development of Point-of-Care devices driven by applications in various fields, Ion-Sensitive Field Effect Transistors (ISFETs) are considered one of the most promising solutions to achieve versatile platforms that fulfil most of the requirements for PoCT in various applications.

Proposed by Piet Bergveld more than 45 years ago [76], the ISFET was initially envisioned to replace glass electrodes for electrophysiological and environmental sensing. Whilst initially underappreciated by the scientific community [77], the interest in ISFETs resurfaced in 1999 when Bausells et al. fabricated the first ISFET on unmodified CMOS technology [78]. Leveraging the benefits of CMOS fabrication technology, ISFETs became a promising candidate to bridge electronics and chemical sensing in a scalable, miniaturised, robust and inexpensive way. These benefits enabled its successful integration on commercial pH meters such as Sentron probes.

Over the 2010 decade, ISFETs were employed for the first time for label-free non-optical nucleic acid detection and sequencing [79, 80]. By arranging ISFET sensors on large arrays with thousands of pixels, high-throughput sequencing became possible while driving the cost per genome down thanks to the scalability of CMOS technologies. Since then, the interest in ISFET technology has continued to grow steadily, flourishing promising applications beyond the initial laboratory setting.

This section presents an overview of ISFET technology, starting from its sensing principles and challenges at both sensor and system level, followed by an analysis of the state-of-the-art solutions to address these challenges. This section concludes with a discussion on the recent developments in ISFET technology applied to PoCT platforms.

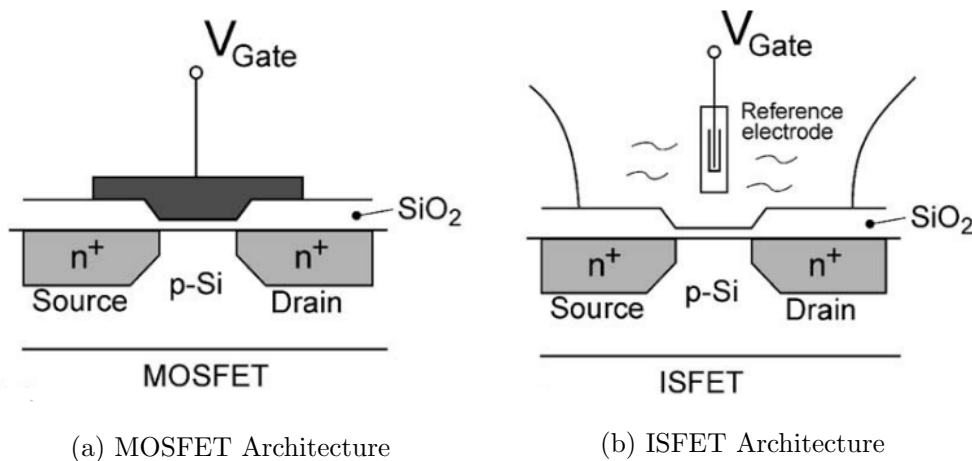


Figure 2.3: MOSFET structure and its ISFET counterpart as initially envisioned by P. Bergveld [81]

2.3.1 ISFET Sensing Principle

The ISFET is a solid-state device with a similar structure to a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) but with its gate detached and immersed into a solution as an Ag/AgCl reference electrode. The potential of this reference electrode is coupled back to the MOSFET gate through the solution and a sensing membrane. This membrane modulates the gate potential based on the ion concentration of the solution. Figure 2.3 exemplifies this concept as initially conceived by P. Bergveld [76, 81], showing a MOSFET (Fig. 2.3a) and its equivalent architecture as ISFET (Fig. 2.3b).

This structure is implemented in standard CMOS by extending the gate connection to the top metal and using the native Si_3N_4 passivation as a sensing membrane sensitive to proton concentration, also known as pH (Figure 2.4a). The interaction of the Si_3N_4 sensing membrane with the ion concentration of the solution is explained by the site binding model described in Chan et al. [82], while a double layer capacitor is formed at the surface of the sensor with a Helmholtz plane and a Gouy-Chapman layer [83].

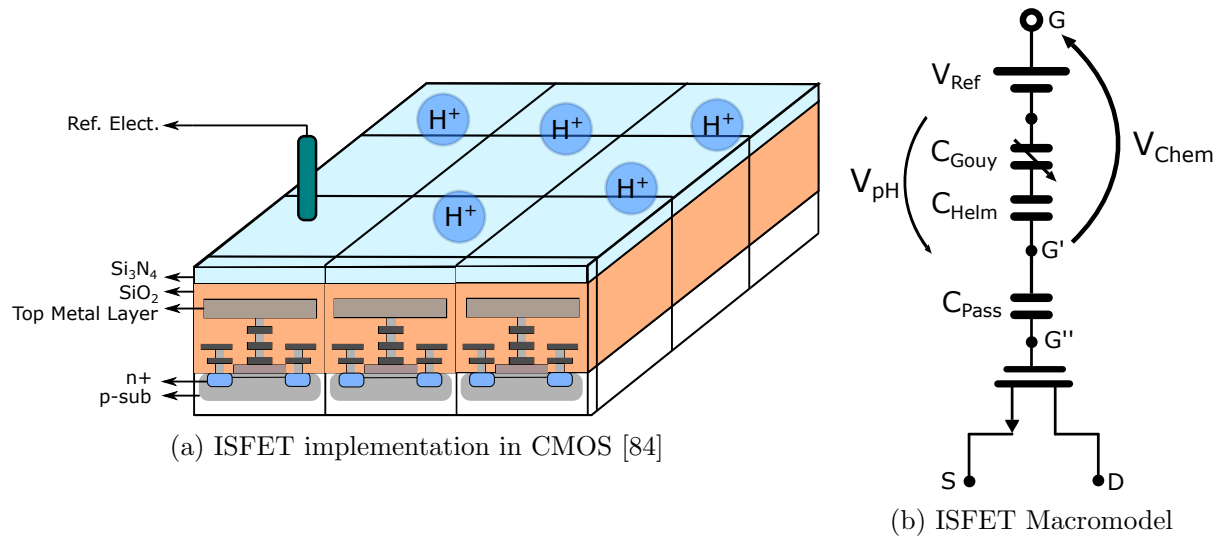


Figure 2.4: ISFET Implementation in CMOS [84] (© 2020 IEEE), and macromodel [85] (© 2003 IEEE)

These interactions are mathematically represented by Eq. 2.1, modelling the ISFET characteristic response. For simplicity, all chemically dependent terms are grouped under V_{Chem} (Eq. 2.2).

$$V_{ov_{ISFET}} = V_{Chem} + V_{ov_{MOSFET}} \quad (2.1)$$

$$V_{Chem} = \gamma + \alpha S_N \log[a] \quad (2.2)$$

The term γ groups all chemical offsets independent to the target species, S_N is the Nernstian sensitivity which represents the theoretical maximum sensitivity - approximately 59 mV/decade at room temperature - and $\log[a]$ is the logarithmic response to changes in the target specie a concentration. α groups all attenuation effects that reduce the sensor sensitivity, ranging from 0 to 1. Throughout this thesis, ISFETs are implemented in standard CMOS and the target analyte a is proton concentration $[H^+]$ unless stated. However, it needs to be noted that recent works have shown the possibility of expanding this analyte sensitivity to various electrolytes by the use of polymer membranes on unmodified CMOS [86]. Furthermore, when ISFETs are arranged in an array, they share a resemblance with optical images. Following this resemblance and to ensure clarity, each individual ISFET sensing element in such arrays would be called “pixel”, and ISFET arrays would be referred as “ISFET imagers” or “chemical imagers” throughout this thesis.

Following these equations, Daniel et al. [85] proposed a macromodel for ISFET architectures that utilises a MOSFET with a series of gate capacitances to describe surface effects, as well as the capacitance attenuation discussed later in Section 2.3.2. Variations on ion concentrations in the solution are modelled as a shift on the ISFET gate voltage. This model is illustrated in Fig.2.4b along with an schematic of an ISFET implemented in unmodified CMOS in Fig. 2.4a.

Using this macromodel, the standard modelling techniques developed for MOSFETs can be applied to ISFETs architectures. Table 2.3 summarises the characteristic response based on the different operating point, merging MOSFET standard equation with Eq. 2.1 and 2.2. However, as discussed in Section 2.3.2, the ideal response presented so far in this section is modified by several non-idealities introduced during CMOS fabrication that set limitations to the sensor performance.

Table 2.3: ISFET Response under different operating conditions

Region	I-V Response
Weak Inversion [87]	$I_D = I_0 \exp \frac{V_{GS} - \gamma - \alpha S_N pH}{nU_t}$
Linear Region	$I_D = K \frac{W}{L} (V_{GS} - \gamma - \alpha S_N pH - V_{th}) V_{DS} - \frac{V_{DS}^2}{2}$
Saturation Region	$I_D = \frac{1}{2} K \frac{W}{L} (V_{GS} - \gamma - \alpha S_N pH - V_{th})^2$
Velocity Saturation [88]	$I_D = v_{sat} C_{ox} W [(V_{GS} - \gamma - \alpha S_N pH - V_{th}) - \frac{V_{DS,sat}}{2}]$

2.3.2 ISFET Challenges

Non-idealities generated during unmodified CMOS fabrication and the challenges associated with the sensing environment and the electrochemical interactions with CMOS standard passivation modify the behaviour presented in the previous section, setting hard constraints to ISFET performance [89]. Furthermore, due to ISFET's integration on Point-of-Care platforms, a new set of challenges has emerged, narrowing the applicability of ISFET-based Point-of-Care Testing. This section describes these two groups of challenges in detail.

Sensing Challenges

ISFETs suffer from various non-idealities due to their fabrication on unmodified CMOS and their sensing environment. Here, these different phenomena are analysed, as well as their impact on ISFET instrumentation specifications.

- **Capacitive division:** The use of native passivation from CMOS processes for pH sensitivity introduces an additional capacitance at the floating gate, named in the macromodel as C_{Pass} (Fig. 2.4b). This C_{Pass} attenuates any chemical signal through a capacitance division with the MOSFET capacitance. Assuming oxide (C_{ox}) and depletion capacitances (C_d) as dominant:

$$V_{G''} = V_{G'} \frac{C_{Pass}}{C_{Pass} + (C_{ox}C_d)/(C_{ox} + C_d)} \quad (2.3)$$

The value of C_{Pass} is a function of the capacitances generated by both Si_3N_4 and SiO_2 due to their thicknesses $t_{Si_3N_4}$ and t_{SiO_2} and dielectric constant ε , as well as the dimensions of the sensing area WL_{chem} , as follow:

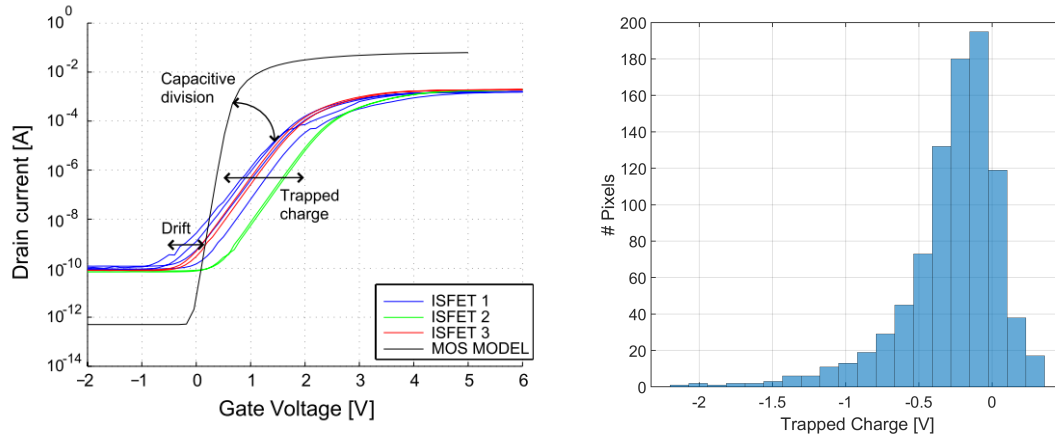
$$C_{Pass} = (WL)_{chem} \varepsilon_0 \frac{\varepsilon_{Si_3N_4} \varepsilon_{SiO_2}}{\varepsilon_{Si_3N_4} t_{SiO_2} + \varepsilon_{SiO_2} t_{Si_3N_4}} \quad (2.4)$$

These equations unveil various mechanisms to improve the attenuation performance to approximate the capacitance division as close as possible to 1.

1. *Reduce MOSFET size*, minimising C_{ox} and C_d contributions
2. *Increase pixel size*, enhancing C_{Pass}
3. *Improving passivation quality*, by either modifying the material or by reducing its thickness
4. *Scaling to smaller nodes*, minimising C_{ox} and C_d contributions. However, this might also have an effect on the noise performance.

Various analyses on the topic have highlighted the favourable performance of smaller technology nodes in terms of attenuation [90, 91], leveraging the reduced MOS capacitances and the thinner passivation. Other approaches, leveraging on the increased C_{Pass} value for larger pixels, have increased the sensing area by introducing logic elements such as memory inside the pixel [25]. Finally, etching the Si_3N_4 layer has been previously applied to reduce capacitive attenuation, improving sensitivity and SNR [92].

- **Trapped charge (TC):** As a result of the deposition of the passivation layers (SiO_2 and Si_3N_4) over the floating gate, charges accumulate between the materials. The potential created by these charges, commonly referred to as “trapped charge”, introduces large offsets on the ISFET gate voltage $V_{G''}$, leading to mismatches between pixels on array configurations. Furthermore, its wide range (typically from -4V to -1V [93]) and the large variability between processes, dies and pixels [89] impose large input ranges on subsequent instrumentation. Figure 2.5a represents the effect of trapped charge on the characteristic curve of an ISFET, and Figure 2.5b shows the distribution of trapped charge across a large array.



(a) Effect of trapped charge on ISFET characteristic response [89, 94]

(b) Histogram presenting the trapped charge distribution across a large ISFET array [84]

Figure 2.5: Trapped Charge Analysis: Effect on ISFET characteristic response [87, 89] (© 2009 IEEE) and its distribution across 1024 pixels [84] (© 2020 IEEE)

Various solutions have been proposed to mitigate the TC effect, both through die processing or architecture compensation. Exposure to UV [93] or the injection of hot-electron injection [95] were proposed to homogenise the threshold levels, achieving consistent results. CMOS passivation etching were explored as well to mitigate trapped charge, reducing the spread from 1.24V to 0.28V by eliminating $5\mu m$ of Si_3N_4 [92]. However, these solutions require post-processing steps that remain unsuitable for large arrays on unmodified CMOS. To overcome this, Georgiou et al. proposed a Programmable Gate (PG) [94] to capacitively couple a fixed potential to the floating gate of each ISFET pixel.

Using this mechanism, each pixel TC could be compensated at the expense of reduced sensitivity due to a capacitive division. This technique has been extensively used across the literature for large array TC compensation [88] and floating gate modulation [96]. More recently, gate reset techniques [97] and source modulation [25] have been proposed.

- **Drift:** Drift refers to the slow monotonic temporal change of the ISFET response due to the interaction of the solution with the sensing membrane, which traps ionic charges on the insulator.

Jamasb et al proposed a physical model of the drift behaviour [98], associating the rate of hydration of Si_3N_4 at the presence of an aqueous solution with drift's temporal evolution. According to this study, Si_3N_4 surface in contact with the solution suffers a slow transformation to hydrated SiO_2 , altering the overall insulator capacitance which in turn modifies the inversion charge sensed by the ISFET. This is modelled through a hopping and trap-limited transport mechanisms, leading to the following drift expression:

$$\Delta V_{GS}(t) = -(Q_D + Q_I + Q_{inv}) \left[\frac{1}{C_I(t)} - \frac{1}{C_I(0)} \right] \quad (2.5)$$

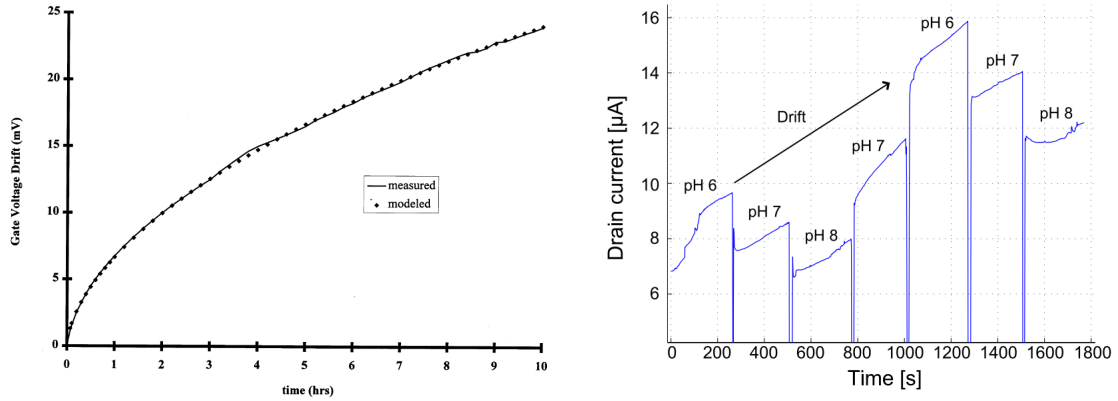
where Q_I represents the effective charge per unit area in the Si_3N_4 , Q_D is the charge stored on the depletion layer, Q_{inv} the correspondent on the inversion and C_I is the effective capacitance of the insulator at the initial sample $t = 0$ and at a time t . By assuming C_I is composed by 3 layers with different capacitance values depending on the hydration level, and applying Fick's first law of diffusion to consider the time dependence of this hydration, the following drift expression can be achieved:

$$\Delta V_{GS}(t) = -(Q_D + Q_I + Q_{inv}) \left[\frac{\varepsilon_{ins} - \varepsilon_{SL}}{\varepsilon_{ins}\varepsilon_{SL}} \right] x_{SL}(\infty) \{1 - \exp -(t/\tau)^\beta\} \quad (2.6)$$

This model predicts an exponential decay of the drift trend. This behaviour is validated with experimental results and matches the observed tendency on large arrays, as presented in Fig. 2.6a & 2.6b.

Although the merits of this approach are undeniable, this model assumes that both temperature, pH and reference electrode potential are held constant. No model so far has achieved a unified mathematical expression that accounts for these experimental conditions for CMOS ISFET platforms. Hence, any drift compensation technique relies on empirical knowledge or a short-term understanding of drift trends. However, this degrades ISFETs' Limit of Detection (LoD) for slow chemical reactions, where both reaction and drift share frequency bands.

Different solutions have been explored to reduce this drift by considering the electrochemical sensing material at the surface. One of the most promising is the replacement



(a) Modelled drift behaviour proposed by Jamasb et al. [98] (© 1998 IEEE) (b) Observed drift on large arrays [89] (© 2016 IEEE)

Figure 2.6: Drift Analysis

of the standard CMOS passivation by alternative materials, etching the initial layer of Si_3N_4 [92] and depositing new sensing layer using Atomic Layer Deposition (ALD). The etching process on its own improves the SNR in 10dB while reducing the drift by 60%, and the deposited materials, such as Ta_2O_5 or Al_2O_3 , provide a near-Nernstian sensitivity and reduced drift [99]. However, these techniques come at the expense of post-processing steps, leading to higher fabrication costs.

- **Noise:** The Limit-of-Detection (LoD) of ISFET devices is determined by their noisy sensing environment. Recent analyses on ISFET noise performance presented by Liu et al. [100] have demonstrated the dominance of chemical noise over electrical noise over an order of magnitude. Figure 2.7 presents these chemical and electrical noise contributions, which were later validated by Moser et al. [25]

The influence of chemical flicker noise is especially significant due to the slow nature of chemical changes on solutions, hampering the recovery of signals with overlapping frequency spectrum. Limited information is presented in the literature regarding the contribution of thermal noise, although Moser et al. [25] result indicates a smaller gap between chemical and electrical thermal noise.

- **Temperature influence:** ISFET architectures, as any solid-state device based on semiconductor technology, are affected by temperature variations. Previous analyses through simulation of this thermal sensitivity reported around 1pH every 7K [85]. Figure 2.8 presents this thermal dependence of the I-V curves [101]

In addition to the thermal effect on MOSFET transconductance, several non-linear thermal effects modify the properties of the different elements of the chemical setup. Firstly, the pH present in the solution can suffer variations due to changes in the redox equilibrium. Furthermore, the interaction of the sensing passivation with the electrochemical

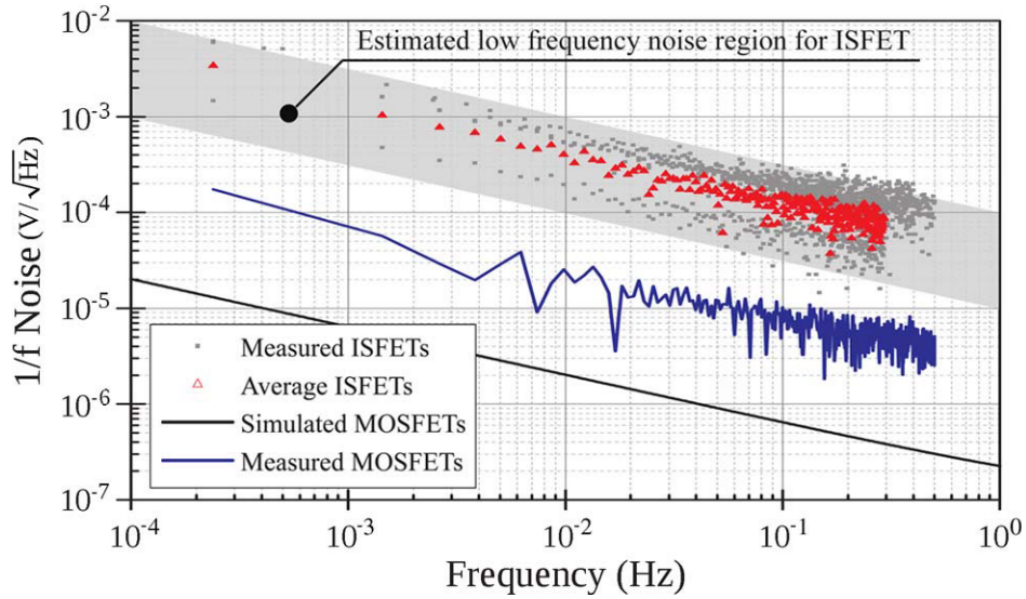


Figure 2.7: Noise Analysis performed by Liu et al. [100] (© 2011 IEEE), showing an order of magnitude between chemical and electrical noise

reaction and the reference electrode is disturbed, leading to variations in sensitivity and attenuation. However, these effects are usually not accounted for in ISFET literature by establishing an experimental setup with a constant temperature, which in turn leads to a lack of unified models for thermal sensitivity on ISFETs.

Point-of-Care Platform Challenges

The application of ISFET arrays as a sensing element of PoCT platforms has unveiled various challenges over the last decade due to the peculiarities of the previously discussed applications. This section reviews these challenges.

- Chip encapsulation:** The use of biological fluid samples on ISFET arrays establishes additional requirements for the chip encapsulation. The chip bonds required for operation must be shielded from the fluid sample to avoid shorts between connections. These shielding mechanisms need to be bio-compatible, ideally causing no interference with sample bio-markers, and should present long term stability in aqueous environments, with minimal fluid diffusion through the material. This encapsulation has been previously achieved through microfluidic devices on large arrays [79], or by covering the bonding area with bio-compatible epoxy [102–104], as shown in Figure 2.9.

Proper bonding design can alleviate some of these encapsulation requirements, as previous ISFET architectures have demonstrated [25, 105]. Placing all bonding connections on one

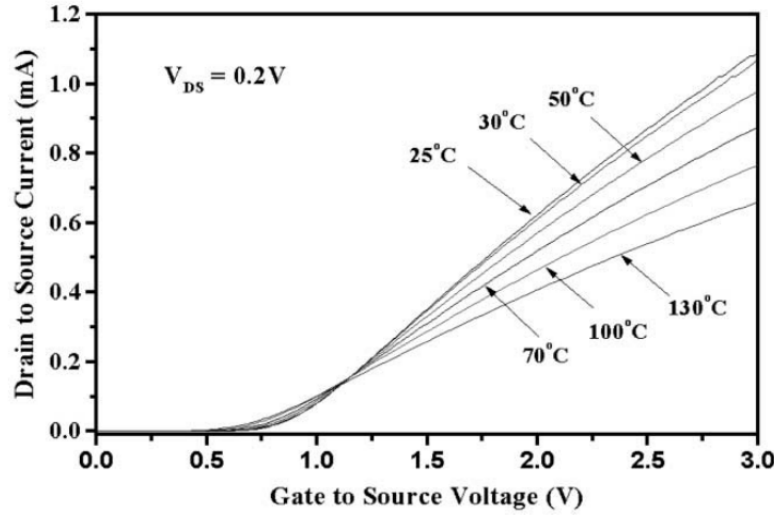
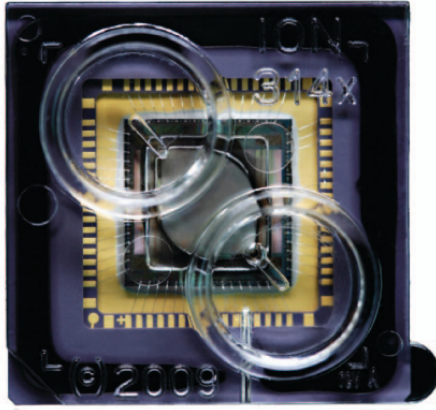
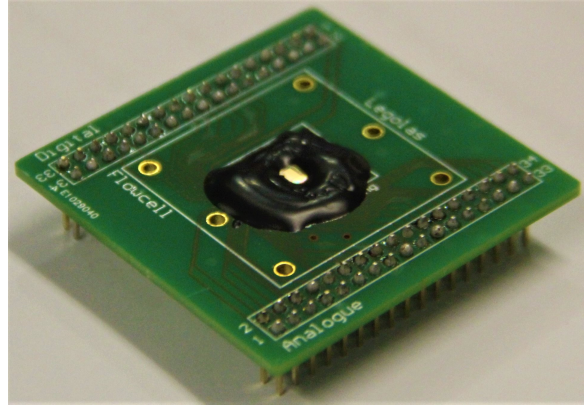


Figure 2.8: Temperature influence on ISFETs characteristic response [101]



(a) Ion Torrent microchip on ceramic packaging with fluidic chambers for reagent flow [79]



(b) Epoxy encapsulation of ISFET chip, covering both metal contacts and bonds [102] (© 2019 IEEE)

Figure 2.9: Encapsulation examples

side enables direct and stable contact of the chip surface with the sample handling devices, isolating the sensing area.

- **Sample requirements:** As discussed in Section 2.2.1, the sample selected for the chosen application establishes both the sample extraction procedure and the sample preparation steps. For the integration of ISFETs as part of a PoCT platform, only blood [34, 106] and sweat [107] have been tested as potential biosamples.

Blood samples have been used for applications that utilise nucleic acids as biomarkers, such as detection and quantification of infectious diseases [106] and tumour mutations [34]. These techniques rely on sample preparation steps for DNA extraction, inevitably involving additional equipment for its potential deployment in small clinics or the field.

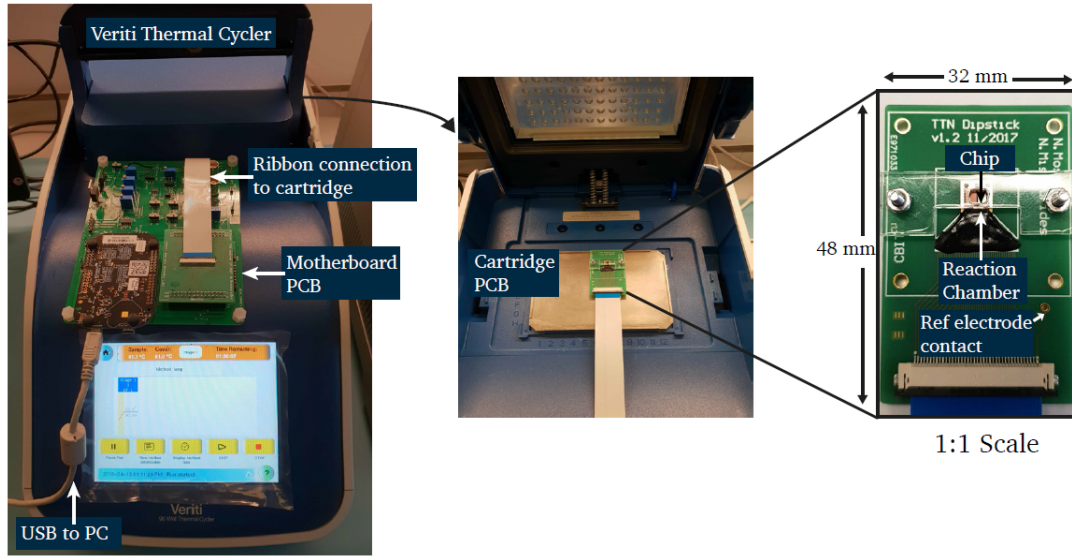
Furthermore, the extracted sample need to be placed inside a reaction chamber. This reaction chamber, usually implemented as a microfluidic device, is sealed to avoid contamination and leakage. Various architectures have been proposed across the literature, such as laser-cut disposable manifolds [25], flow cells [88], or direct ink writing microfluidics [108]

On the other hand, electrolyte sensing on sweat does not require any sample preparation. However, the limited volume acquired, the risk of contamination and evaporation, and the lack of effective extraction methods prevent its deployment as part of wearable devices for well-being monitoring.

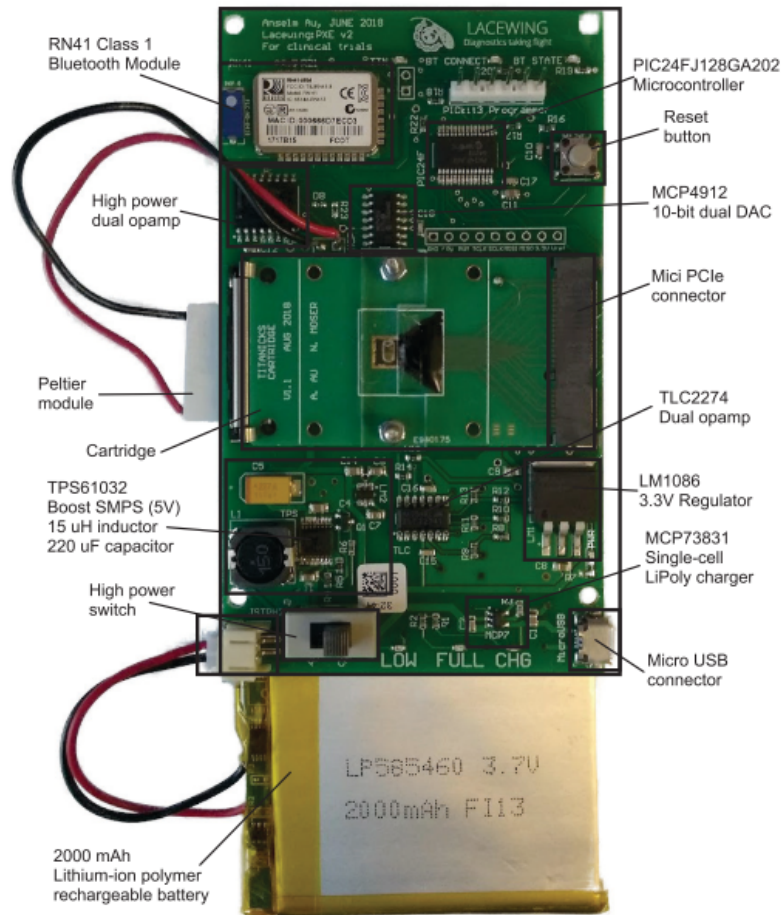
- **Long-term monitoring:** Health and well-being applications require chemical monitoring over long periods without the need for re-calibration. The presence of monotonic drift on ISFET sensors establishes limitations on the monitoring time, set by the architecture Analog-to-Digital Converter (ADC) range. However, a wide ADC input range usually comes at the expense of reducing the resolution and the pH Limit-of-Detection of these devices. These trade-offs establish an irreconcilable dichotomy between long term monitoring and high-resolution measurement.
- **Platform calibration:** ISFET non-idealities such as trapped charge and drift affect the calibration requirements for these sensors. As the exact correspondence between ion concentration and sensor output varies over time, an initial flow of buffers with known concentrations is required to enable absolute concentration measurements [86, 103]. However, the automation of this process remains challenging, especially for its integration on portable and wearable platforms. On the other hand, calibration-less platforms provide differential measurements from a concentration baseline, retrieving only information on the relative change rather than the absolute value [84, 105].
- **Affordability:** Power, biasing and processing requirements of state-of-the-art ISFET architectures are fulfilled by its integration as part of larger platforms, usually implemented on rigid PCBs with sockets for ISFET cartridges. Figure 2.10 presents two examples of these platforms.

These platforms operate as a bridge between ISFET and a processing hub, usually a smartphone or a desktop PC, that extracts the sensing information. These requirements reduce the affordability of PoC platforms, with a specially significant impact on developed countries with limited economic resources.

- **Power supply:** Portability requirements posed over PoC devices set strict limits over the platforms' power consumption. In this context, energy harvesting solutions have been explored as a promising alternative to batteries for wearable devices [107]. However, limitations such as source instability and limited supply current generated are currently refraining from its integration as part of larger systems.



(a) Benchtop PoC platform presented by Miscourides et al [109] (© 2019 IEEE)



(b) Portable PoC platform proposed by Moser et al [99]

Figure 2.10: Previous ISFET Point-of-Care Platforms

- **Surface Lifetime:** The degradation of the electrochemical sensing element, both during wet operation and shelf-time, remains one of the biggest challenges, shortening the device's useful life and incorporating an important source of performance uncertainty. Even though the electro-chemical degradation during active use has been extensively studied (i.e. drift) [110–112], the approach is usually electronic-centric, overseeing the fundamental principles behind this drift and its effect in the long term. Furthermore, the performance evolution of ISFET sensors after long periods of shelf-time hasn't attracted much attention in the literature, while it is a crucial challenge for its commercial viability.

2.3.3 ISFET Sensing Front-End

The limitations and challenges described in Section 2.3.2 have steered the focus of various research groups towards specific challenges. This section covers the evolution of ISFET architectures from single-pixel devices to complex arrays, with a final focus on the most recent and relevant advances on ISFET sensing.

In the early days of ISFET instrumentation, front-end architectures were primarily implemented using discrete components [81]. One of the first examples of ISFETs instrumentation designed as an Integrated Circuit (IC) is the architecture presented by Wang et al. in 1989 [113], where the authors utilised a differential measurement between ISFETs to shield it from temperature variations. This architecture and the single-ended drain and source followers presented by P. Bergveld [81] are considered the foundations of ISFET instrumentation. Figure 2.11 illustrates these two architectures.

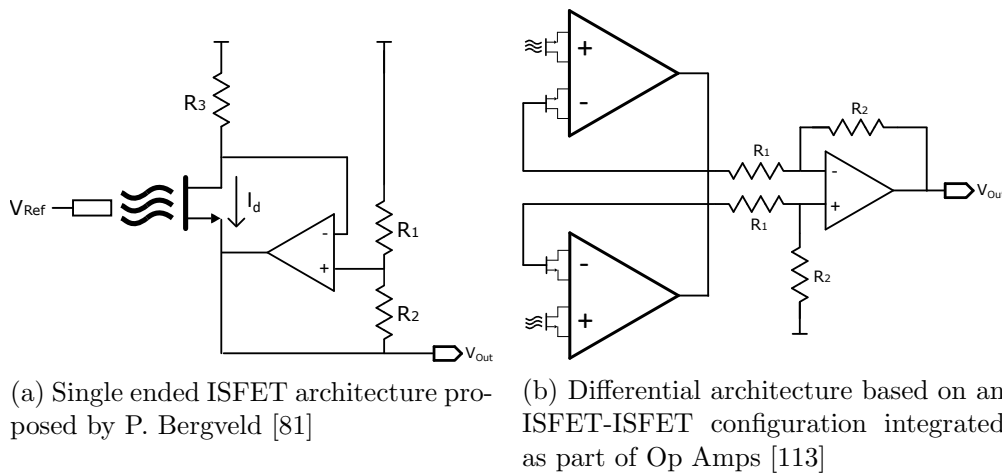


Figure 2.11: Foundations of ISFET instrumentation

The decade of the 2000s witnessed the rise of array configurations to the detriment of single-pixel devices with discrete components, moving from ISFET sensing to ISFET imaging. Several potential benefits drove the interest for array configurations in recent times:

- **Enhancement of noise performance:** Array configurations can achieve lower LoD by averaging the signal obtained from smaller sensors, rather than a single, larger device [114]. This phenomenon is based on the fact that individual pixels can be considered independent, and the noise of each sensor can be assumed as uncorrelated. By averaging N pixels with uncorrelated noise, a resolution enhancement of \sqrt{N} is achieved.
- **Multiplexing:** The opportunity for sensing multiple biomarkers on a single device would be beneficial for PoC applications, as discussed in Sect.2.2.2. By arranging ISFETs on an array configuration, different areas of the imager could be dedicated to analysing different bio-markers. The feasibility of this approach has been recently demonstrated by Moser et al. [86] by placing different sensing membranes on different array areas.
- **Understanding of Spatio-temporal effects:** Chemical diffusion effects can provide insights into the reaction mechanics. Imaging these effects can potentially enhance the sensor's LoD while also provide early detection of such events.
- **Sensing robustness:** The significant disparity of the values of non-idealities such as trapped charge and drift can place individual sensors outside their operating points. By arranging these sensors as array configurations, additional robustness is introduced to ensure that sensors on the reaction area are active.
- **Potential for learning algorithms:** The recent and accelerated development of learning algorithms can enhance the sensing capabilities leveraging the availability of large datasets that enable the discovery of reproducible patterns [115]. By extracting large datasets from dense arrays, we open the doors to new opportunities for non-idealities dynamic compensation and LoD improvements, as well as unveiling hidden dynamics on chemical reactions.

Over the last decade, the flourishing field of ISFET architectures has experienced rapid development, exploring novel sensing domains to enable fast acquisition and high resolution sensing on large ISFET arrays while exploiting the scalability benefits of CMOS technologies. Based on this evolution, I have identified three trends in the literature that focus on distinct aspects of ISFETs potential:

- Firstly, the limitations established by the CMOS fabrication have motivated the development of a wide range of pixel architectures with integrated compensation capabilities and in-pixel quantisation, aiming to exploit the benefits of CMOS scalability to achieve low noise ion sensing.
- Secondly, ISFET imagers have aligned with the current trend of CMOS imagers towards high-resolution arrays with highly parallel readouts to achieve ultra-high frame rate imaging

of chemical reactions. These architectures aim to unravel previously unseen insights on ion diffusion and chemical reactions by acquiring large datasets through minimal-footprint pixels.

- Finally, the disruption created by external conditions and the need to sensing features beyond ion concentration on PoC platforms have driven the development of arrays with multiple sensing modalities, both at a system level or inside each pixel, that aspire to enhance the robustness and versatility of the system.

The following subsections analysed the recent developments on each trend.

Focus on adaptability

Adaptability refers to the sensor's ability to modify its operating point to provide robust sensing output under a range of conditions. These conditions include both internal, such as different trapped charge distributions and drift trends, and external, such as different temperatures, light conditions, humidity levels and power supply variations.

The development of in-pixel compensation structures to enhance systems adaptability has been the dominant and most prolific trend over the last decade, encapsulating the vast majority of the publications. The motivation behind this trend is associated with the challenges of implementing large arrays in CMOS technology, requiring either a wide input range on ADCs to accommodate for pixel-to-pixel variation or compensation of mismatches.

Milgrew and Cummings [93] initially proposed using UV light on ISFET arrays to converge threshold voltage and match trans-conductance between devices across the array. Unfortunately, this technique requires openings in the passivation layer and relies on post-processing steps. To preserve the benefits of unmodified CMOS technology in terms of scalability and cost, the research focused on developing novel schemes to mitigate and potentially eliminate the effect of non-idealities at a pixel level.

For this purpose, various schemes explored ways of extending the input range by implementing multi-transistor input stages. An example of this is the architecture proposed by Liu et al. [116], which utilises an inverter coupled with an external sawtooth waveform to encode chemical information on a Pulse Width Modulation (PWM) signal. This architecture achieves a wide dynamic range with minimal footprint by leveraging both PMOS and NMOS operating ranges. A similar idea was recently proposed by Duan et al. [104], which selects either PMOS or NMOS readout to enhance input range. This enhancement of dynamic range comes at the expense of increasing capacitive attenuation compared with single-device readouts due to both PMOS and NMOS parasitics.

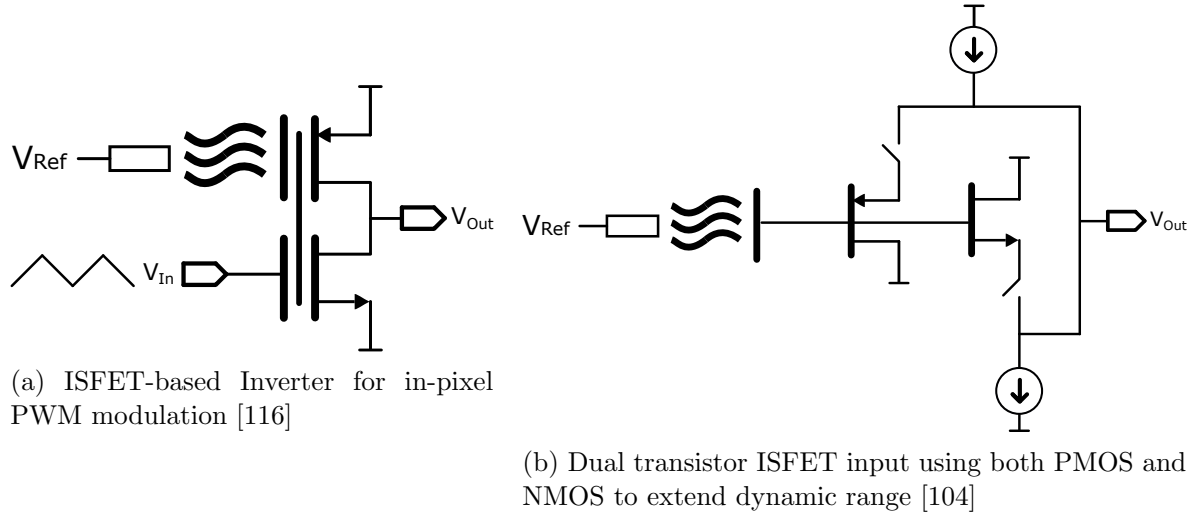


Figure 2.12: Extended input range ISFET architectures

An alternative approach focuses on deploying compensating schemes in-pixel by modulating the gate potential or modifying the readout biasing point. Georgiou et al. initially envisioned this first option [94], proposing a Programmable Gate (PG) to capacitively couple the floating gate potential with an off-pixel voltage at the expense of reduced sensitivity. This mechanism was first implemented on an array in [117] and later validated for trapped charge compensation on large arrays by Miscourides et al. [105], while Liu et al. [96] demonstrated its potential to modulate the floating gate potential with an external waveform.

This floating gate modulation was utilised by Hu et al. [97, 118] in a feedback loop through a low leakage switch, enhancing capacitive attenuation and compensating for both trapped charge and accumulated drift. However, the electrical drift caused by leakage at the gate switch limits this architecture's performance. This drift is further intensified with temperature, making it unsuitable for PoC platforms that require temperature regulation.

Alternative modulation schemes beyond analogue domain were explored by Moser et al. [25], achieving a scalable and robust sensing architecture by leveraging time-domain encoding benefits. This architecture quantises the chemical information in-pixel to enhance its Signal to Noise Ratio (SNR) while compensating trapped charge through the ISFET source terminal, eliminating the need to access the floating gate. Furthermore, the introduction of SRAM cells in-pixel under the chemical area led to an improvement in attenuation. Jiang et al. [119] presented a similar time-domain approach, measuring the charge accumulated on a capacitance.

Kalofonou et al. [120] addressed the challenges of chemical drift by utilising differential reaction chambers connected to a Gilbert cell, achieving drift compensation and low power operation. This work introduces differential architectures as a potential solution to achieve stable sensing against Process, Voltage and Temperature (PVT) variations.

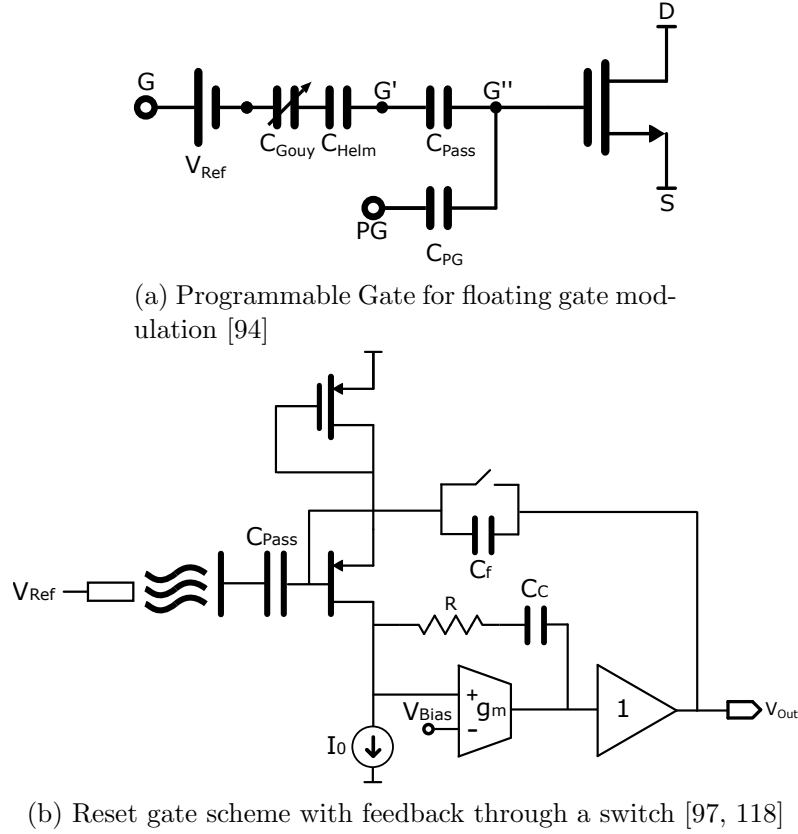


Figure 2.13: Gate Modulations Approaches

More recently, Douthwaite et al. merged the trend towards wearability and power harvesting with ISFET technology [107], presenting a thermally powered architecture that transmits wirelessly ISFET information. Furthermore, this work demonstrated the potential for low noise measurements through array averaging.

This adaptability trend has focused chiefly on trapped charge and capacitive attenuation correction, with limited papers addressing drift and its consequences for long-term monitoring. Furthermore, limited solutions on LoD enhancement have been reported - either due to the lack of positive results or the focus on new passivation materials. Lastly, with the integration of ISFET sensors as part of PoCT platforms, mechanisms to react or mitigate the sensitivity to changes in external conditions such as temperature are becoming increasingly important to maintain high accuracy and enhance usability and versatility of these devices.

Focus on frame rate

The field of CMOS imaging has been a fruitful source of inspiration for ISFET imagers when realising large and dense arrays in unmodified CMOS. One of the most relevant trends imported from CMOS imagers is the drive towards high spatial resolution, high frame rate arrays,

leveraging noise reduction techniques through spatial averaging to overcome the attenuation increase.

The idea of high frame rate imagers was initially proposed by Shields et al. [121], achieving a frame rate of 333 fps on a 16x16 array with a pixel pitch of 14 μ m. This initial example targeted the analysis of diffusion profiles of analytes on a solution with high granularity.

The race towards the highest frame rate has accelerated over the past few years, leveraging developments made on high throughput CMOS imagers such as column-level ADC or massively parallel readouts [122]. In 2019, both Liu et al. [96] and Lee et al. [123] presented two high frame rate architectures, achieving 1000 fps and 1933 fps, respectively. To further enhance the frame rate, Zeng et al. [103, 124] combined ultra-fast column-level readout architectures with high-speed PCIe readout, overcoming the transmission bottleneck.

The main limitation of these platforms remains the compensation mechanisms, relying on ADCs with large input range or gate modulation techniques. Furthermore, the elevated frame rate is achieved at the expense of power consumption and system complexity, limiting the versatility of these devices. Lastly, no clear application has been proposed for ultra-high frame rate systems, as chemical reactions usually occur in seconds or even minutes and the utility of diffusion effects to gain insights into reaction outcome is yet to be demonstrated.

Addressing the limitation of versatility, Miscoirides et al. [88, 105, 125] envisioned the first portable platform for moderate frame rate, powered by an inexpensive and compact Raspberry Pi.

Focus on multi-sensing

The multi-dimensional nature of chemical reactions and the versatility required for ISFET-based PoC devices have been recently recognised and addressed in the literature. The opportunity to integrate monolithically additional sensors on the same substrate has enabled multi-modal arrays targeting various sensing modalities. These architectures aim to understand the sensing conditions better, better characterising electrochemical reactions occurring at the surface, enhancing the system precision and expanding functionality by eliminating additional external sensors.

An initial example of ISFET multi-sensing was proposed by Constandinou et al. [126], envisioning a pixel that integrates optochemical imaging in-pixel, along with magnetic actuators for closed-loop neural tissue stimulation. Figure 2.14 presents this concept, showing a pixel formed by an ISFET active area, an APS circuit and a magnetic coil targeting Transcranial Magnetic Stimulation.

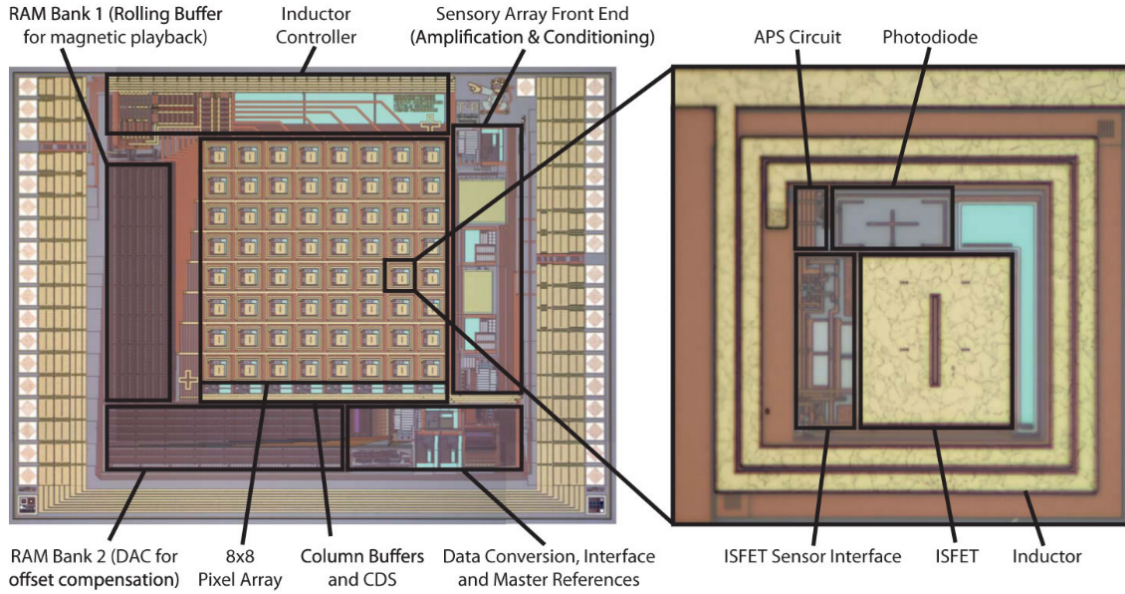


Figure 2.14: Multisensing pixel proposed by Constandinou et al. [126], presenting both chemical and optical sensors and in-pixel actuators for closed-loop operation (© 2010 IEEE)

This blend of optical and chemical sensors was explored by Huang et al. [127], showing the potential for sensor fusion approaches to enhance the precision of ISFET sensing. By spatially locating DNA beads on the array surface, the risk of detecting a false pH reaction is decreased by discarding any output variation on uncovered areas. Figure 2.15 illustrates this concept.

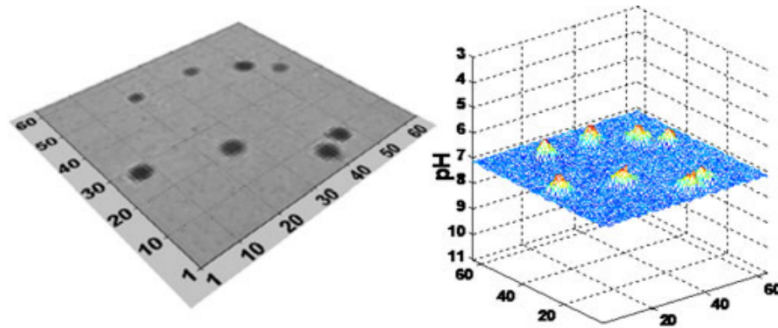


Figure 2.15: Multisensing opto-chemical output proposed by Huang et al. [127], showing both chemical and optical sensors results during nucleic acids sequencing (© 2015 IEEE)

More recently, Hsu et al. leveraged ISFET light sensitivity to achieve dual-sensing on a single ISFET device [128]. By merging machine learning algorithms with optochemical sensitivity, both light and ion concentration variations were distinguished. However, this approach requires extensive calibration under controlled conditions and does not consider trapped charge or drift, raising questions on its suitability for large array configurations.

The integration of ISFET architectures as part of PoC platforms for DNA amplification brought new challenges such as thermal regulation of solution. Previously, this regulation was achieved

through either external equipment or external sensors. To address this issue, Moser et al. [25] proposed the substitution of chemical pixels for temperature pixels, enabling spatial sensing of thermal distribution across the array.

Despite the potential of multi-sensing architectures, several challenges are currently posed over their development. Until now, all architectures sacrifice spatial resolution to achieve multi-sensing capabilities, either by increasing circuit components or by reducing the array resolution. Furthermore, two independent ADC conversions are needed to digitise the signal, narrowing the bandwidth and increasing circuit complexity. Finally, the lack of understanding of the effect of external conditions on the chemical sensing prevents the definition of precise specifications and subsequent compensation mechanisms. Overcoming these limitations is key to the development of these PoCT systems.

2.3.4 ISFET applications

Five main applications have driven the exponential growth of PoC platforms that incorporate ISFET imagers.

- **pH Probes:** ISFET-based portable pH probes have flourished over the last decade, leveraging on the cost-effectiveness and compact form factor of ISFET sensors. Companies like Oakton [129], Sentron or Thermo Fisher [130] are developing compact and versatile pH probes. However, calibration routines to obtain absolute pH measurements remains one of its biggest challenges.
- **DNA Sequencing:** The development of ISFET-based DNA sequencing by Rothberg et al. [79], later branded as Ion Torrent, represented a game-changer on next-generation sequencing technologies, leveraging for the first time on Moore's law to drive down the price per genome. Thanks to label-free single nucleotide detection, large ISFET arrays could be developed to achieve high throughput sequencing. Since its discovery, DNA sequencing has been the most popular application of ISFET technology, and a wide range of architectures have been proposed to enhance precision and functionality [93, 127, 131, 132], as well as successful start-ups such as Ion Torrent (acquired by Thermo Fisher for \$750M) [133] and LiDia-SEQ from DNA-e [134].
- **DNA Amplification Detection:** Shortly after the demonstration of DNA sequencing capabilities utilising CMOS-based ISFET arrays, Toumazou et al. [80] presented a method for DNA amplification and detection using ISFET arrays. This technique has been deployed at the PoC through portable platforms to diagnose infectious diseases, such as the ones reported in [106, 125, 135, 136]. Furthermore, its application on methylation

detection for epigenetic analysis of tumour progression [33, 75] represents a promising application for early detection and treatment at the PoC. This trend is starting to spin-out from academic research, with devices like Lacewing [135] or companies like Proton-Dx [137] or DNANudge with their COVID Bubble Test [138], offering nucleic acid tests (NATs) at the PoC.

- **Electrolyte sensing:** Real-time tracking of the evolution of electrolytes on a bio-sample has been extensively explored, with potential applications as PoCT as discussed previously in Section 2.2.2. However, examples in the literature have focused on test-bench setups to demonstrate multi-electrolytes imaging [86], bacterial [119] and extracellular imaging [139].
- **Cell Culture Monitoring:** The importance of real-time, non-invasive cell culture respiration and acidification monitoring has motivated the development of both single-sensor [140] and array-wide [139, 141] ISFET platforms, enabling cell growth directly over the chip surface.

These applications and its position in the R&D cycle are illustrated in Figure 2.16



Figure 2.16: ISFET PoC Applications and their R&D Cycle, highlighting both research technologies and spin-outs / products that are commercially available or are moving towards commercial launch

2.4 Summary

In this chapter, the global trend towards E-Health was established as the driving force for developing affordable, portable, reliable, precise and simple-to-use Point-of-Care devices. These Point-of-Care devices are envisioned to be critical enablers for remote diagnosis on an e-Health system, and their deployment has far-reaching implications for both healthcare systems and the wider society.

PoC devices were analysed in detail, focusing on three key aspects: the biomarkers required to determine a medical condition, its presence in the different biological fluids and the transduction elements that enable its detection. Recent developments on these three elements have catalysed the development of novel PoC devices with distinct characteristics and specifications based on their target application.

In this context, ISFET technologies are considered a promising candidate to overcome the trade-offs established by state-of-the-art PoC applications. Leveraging on the benefits of CMOS processes, ISFETs have already disrupted various fields such as DNA sequencing, thanks to its benefits in low cost, scalability, and monolithic integration. Recent developments and remaining challenges were described, as they remain the main limitation for the widespread use of this technology. Finally, the applications proposed so far for these platforms were discussed.

Over the next decade, numerous new ISFET platforms applications at the PoC are expected to be discovered. The coincidence of ubiquitous connectivity, societal changes driven by artificial intelligence, growing demand for healthcare solutions, and decreasing silicon technologies price establish an ideal context for ISFET platforms to flourish. However, for this ISFET-based healthcare revolution to occur, the remaining issues of these platforms need to be addressed and mitigated, and novel applications for this technology need to be explored. This thesis makes a humble contribution towards this goal.

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Chapter 3

Oscillator-based ISFET Architectures

3.1 Introduction to Oscillator-based Architectures

Chapter 2 introduced ISFET technology in standard CMOS and its challenges and limitations both as a sensing platform and as part of a Point-of-Care device. To realise the potential for ISFET platforms as a versatile sensor beyond a single application, four main aspects need to be addressed, as highlighted in Figure 3.1.

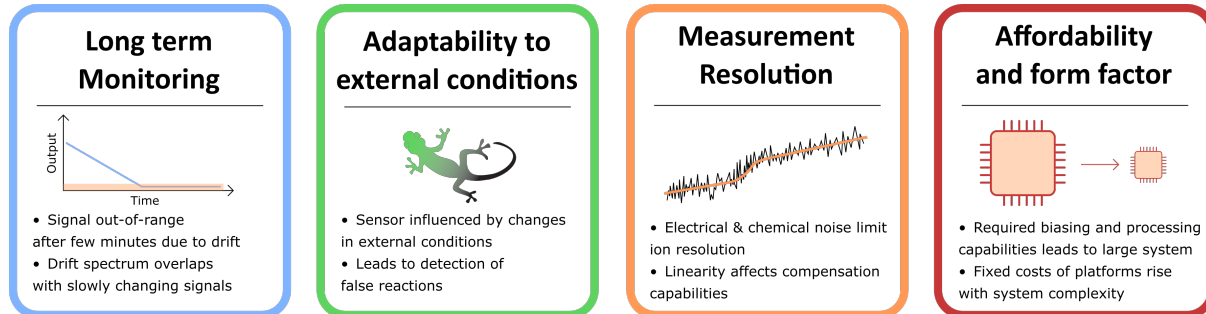


Figure 3.1: ISFET Systems as Point-of-Care Platforms - Main Challenges and Barriers

To address these challenges, I looked for inspiration on state-of-the-art architectures that have successfully overcome similar limitations on their particular sensing domain: Voltage Controlled Oscillators (VCOs). These architectures utilise an oscillator controlled by an external potential, modifying its frequency, duty cycle, or phase. Applied to sensing, these systems shift the sensed signal from the original analogue domain to the time or frequency domain, leveraging its suitability for deep sub-micron technologies [1–3] and its versatility for integration in multiple scenarios, such as audio ADCs [4], biomolecules detection [5], MEMS Inertial Sensors [6] or Wheatstone bridge-based sensing [7–9].

These architectures present attractive benefits to overcome ISFET challenges:

- **Noise Performance:** Frequency modulation provides inherent quantisation noise capabilities, while Duty Cycle modulation has the potential for filtering through window sampling [10]. Furthermore, phase noise can be easily minimised through appropriate sizing, trading with power and sampling rate [11–13]. These strategies open a range of opportunities for improving the ISFET noise performance by minimising the quantisation noise while enhancing the LoD.
- **Adaptability:** Oscillator-based architectures, especially those designed based on relaxation oscillators [7], provide additional programmability to adapt the sensor response to the sensing conditions. This programmability is especially important for enhancing ISFET adaptability to external phenomena and enabling long-term monitoring through real-time compensation.
- **Highly linear sensitivity:** Although this is usually dependent on the specific modulation mechanism of the VCO, these architectures introduce minimal linearity distortion, as presented in [9, 10, 14]. Linearity has been previously demonstrated as desirable for ISFET architecture by Miscourides et al. [15]
- **PVT robustness:** By arranging compact oscillators differentially, Process, Voltage and Temperature (PVT) variations as well as external conditions influence could be minimised [8]. This resilience is crucial for integrating ISFET platforms with temperature-dependent protocols.
- **Integration with digital processing:** The trend towards higher integration between ISFET architectures and processing elements to reduce platform cost and footprint favours solutions that can directly interface digital elements. In this context, oscillator-based architectures can provide a digitised output that requires no ADC for its processing on an MCU.

This chapter adapts this VCO-based approach to ISFET architectures.

3.2 Preliminary analysis

Time-domain encoding using VCO architectures provides numerous potential benefits in node scalability, programmability, noise and power. This section merges VCOs with ISFET sensors, exploring two oscillator-based architectures: An ISFET-Based Sawtooth Oscillator and a Chemically Controlled Ring Oscillator (CCRO). These architectures, illustrated in Figures 3.2a and 3.3a, encode the ion concentration into the duty cycle of a digital clock, outputting a pH-dependent PWM signal with a device-level programmable response. This section describes the principle of operation of these two architectures in detail.

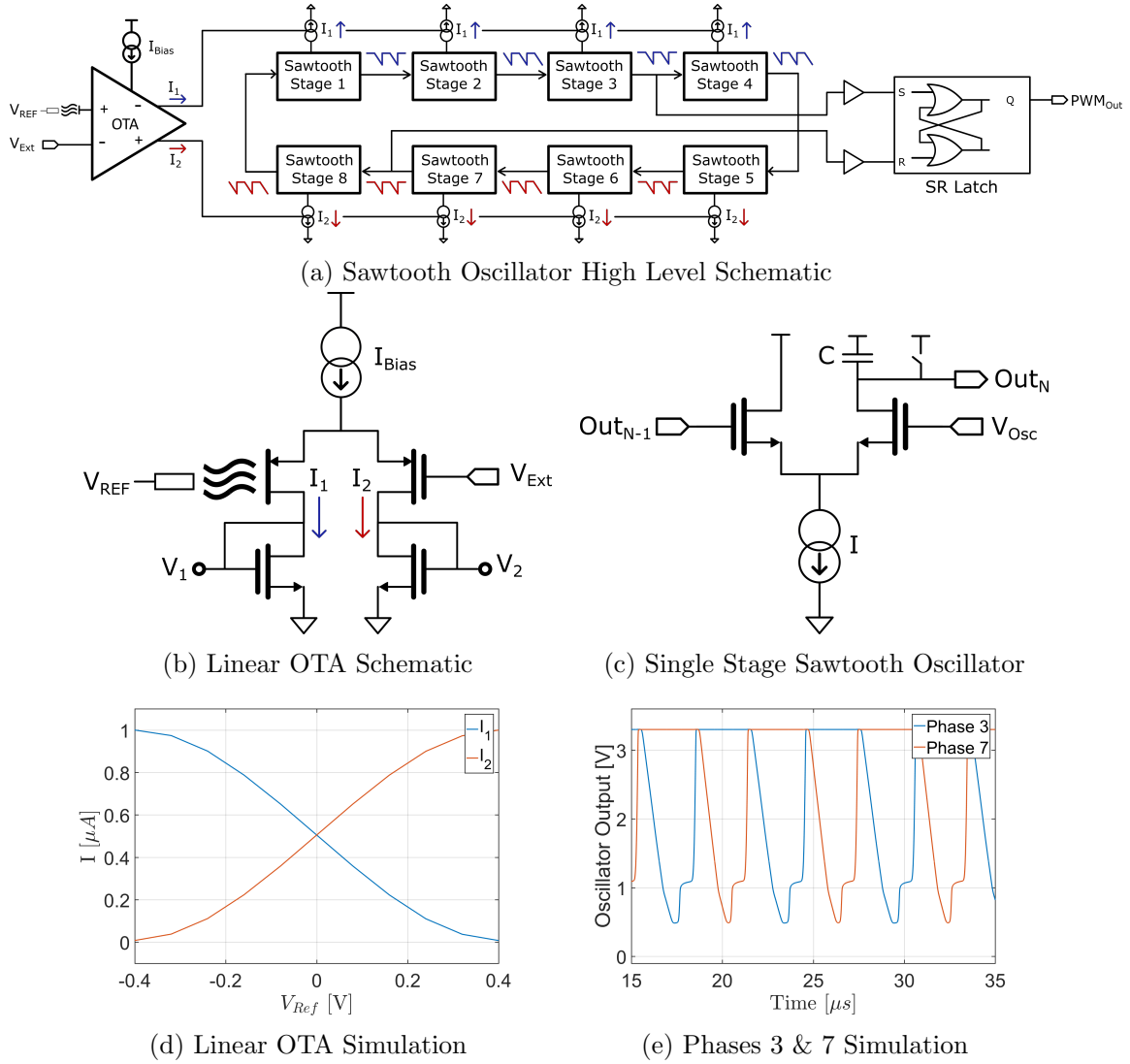


Figure 3.2: Sawtooth Oscillator Architecture [16] (© 2019 IEEE)

3.2.1 8-Stage Sawtooth Oscillator: Principle of operation

The Sawtooth Oscillator architecture converts a pH change at the ISFET into differential currents, which modulate the stages' delay of a Relaxation Oscillator. This delay difference at the oscillator stages creates a PWM signal with a chemically controlled duty cycle. Illustrated in Figure 3.2a, it is composed of two blocks:

- A linear Operational Transconductance Amplifier (OTA), modulating the chemical input into a differential current
- An 8-stage Sawtooth Oscillator & a latch, integrating the generated differential current and converting it into a PWM signal with a variable duty cycle

This architecture leverages the linearity of both blocks to achieve a highly linear sensor response. Additionally, the use of differential measurements increases the robustness to PVT (Process, Voltage and Temperature) variations, while the OTA enables several degrees of sensor programmability by tuning I_{Bias} and V_{Ext} . The two blocks are now described in detail.

Linear OTA

The linear OTA converts any differential voltage at the input to a differential current at the output, as shown in Figure 3.2b. To make this structure pH-sensitive, one of the MOSFETs of the differential pair is replaced with an ISFET, while the second branch is biased with an external voltage V_{Ext} . These two voltages, V_{ISFET} and V_{Ext} , control the behaviour of the linear OTA as follows:

$$I_{Bias} = i_1 + i_2 \quad (3.1)$$

$$i_1 - i_2 = 2g_m(V_{ISFET}(pH) - V_{Ext}) \quad (3.2)$$

Eq. 3.1 and 3.2 show that any pH variation sensed by the ISFET would trigger a change on the currents i_1 and i_2 . However, these equations are valid whilst the differential pair operates in the linear region. This linear region, controlled by g_m , establishes the sensor's range and electrical sensitivity. This g_m is set through transistor sizing and I_{Bias} tuning.

Therefore, two OTA's inputs can be used to control its sensing behaviour:

- V_{Ext} , setting the equilibrium point of the OTA. This external voltage has the potential to compensate both trapped charge and monotonic drift present in standard CMOS ISFETs [17]
- I_{Bias} , establishing the OTA's input range and electrical sensitivity

Figure 3.2d presents simulated data of the evolution of i_1 and i_2 with any difference between V_{ISFET} and V_{Ext} . These output currents are mirrored to the next stage, modifying the oscillator's behaviour as described in the next subsection.

8-stage Sawtooth Oscillator

The designed sawtooth oscillator is a variation of the relaxation oscillator proposed in [7–9], known for exhibiting high linearity control and robustness to voltage supply and temperature

variations. The number of stages are selected for optimal phase noise and linearity control, at the expense of power consumption. The stages of these oscillators are current-starved by the differential currents generated on the linear OTA, as shown in Figure 3.2c. The capacitor at each stage is reset to V_{DD} at the beginning of each phase and discharged linearly, integrating the mirrored current generated in the OTA. This architecture is illustrated in Figure 3.2e, creating a delay defined by:

$$T_{discharge} = \frac{V_{Osc} * C}{I(pH)} \quad (3.3)$$

being V_{Osc} an externally-controlled fixed voltage, C the value of the stage's capacitor and I the current fed into the stage. Using this approach, i_1 and i_2 set the $T_{discharge}$ of the stages, slowing half of the oscillator and accelerating the other half. By connecting two opposite phases (Stages 3 and 7 in Figure 3.2a) to a latch, the $T_{discharge}$ of both phases are compared, and a PWM signal with variable duty cycle is obtained. Theoretically, if $i_1 = i_2$ a 50% duty cycle PWM signal is output, and any difference between i_1 and i_2 modulates the duty cycle value.

3.2.2 Chemically Controlled Ring Oscillator (CCRO): Principle of operation

The Chemically Controlled Ring Oscillator (CCRO) is a standard Ring Oscillator with one inverter replaced by an inverting ISFET-based delay cell, as illustrated in Figure 3.3a. The architecture is constructed using only digital gates, making it suitable for deep sub-micron technologies. Additionally, this architecture can be operated at reduced supply voltages, allowing ultra-low power consumption while achieving high resolution.

The key component of this architecture is the ISFET-based delay cell. This ISFET delay cell comprises a Programmable-Gate ISFET [18] connected to a standard inverter, chemically modulating the gate voltage through capacitive division.

$$V_{g''} = \frac{C_{Pass}}{C_{PG} + C_{Pass}} V_{g'} + \frac{C_{PG}}{C_{PG} + C_{Pass}} V_{PG} \quad (3.4)$$

The value of C_{Pass} is estimated as:

$$C_{Pass} = (W * L) \frac{\epsilon_{SiO_2} \epsilon_{Si_3N_4}}{\epsilon_{Si_3N_4} t_{SiO_2} + \epsilon_{SiO_2} t_{Si_3N_4}} \quad (3.5)$$

where $W * L$ represents the active area of the pixel, t represents the thickness of the dielectric layers, SiO_2 and Si_3N_4 , and ϵ the electrical permittivity of these materials[17].

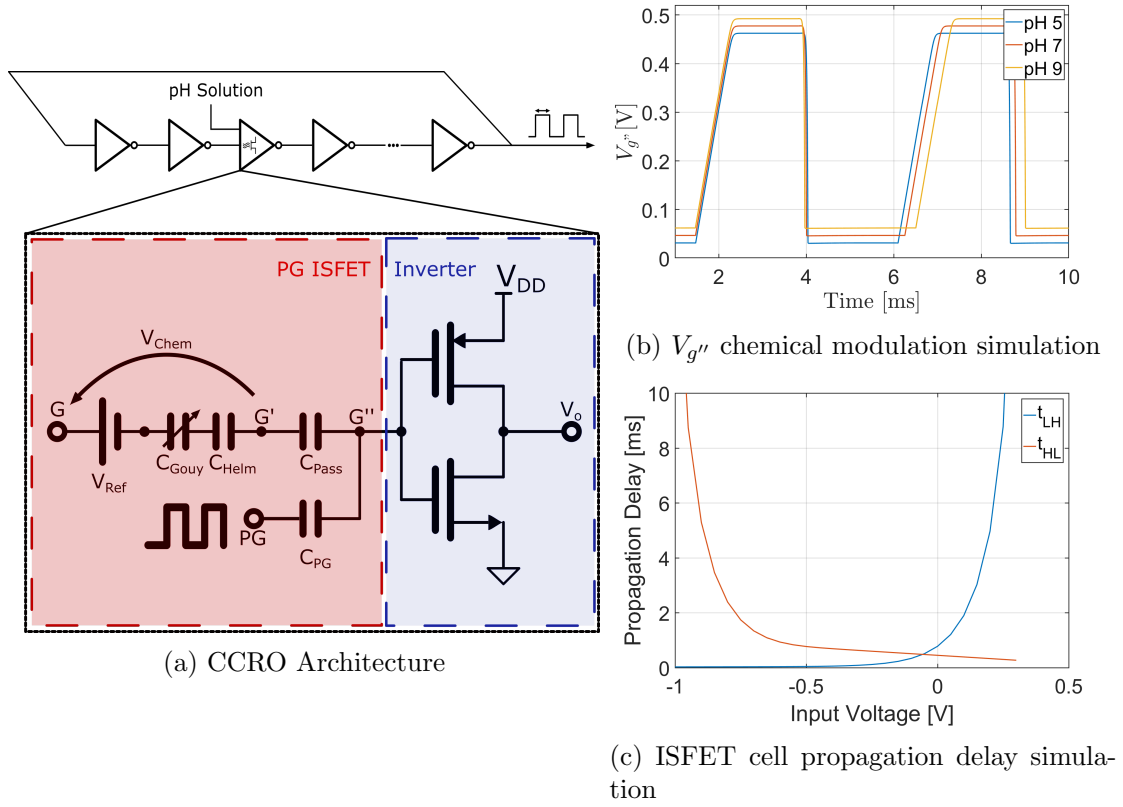


Figure 3.3: Chemically Controlled Ring Oscillator (CCRO) Architecture [16] (© 2019 IEEE)

The chemical modulation of the gate, illustrated in Figure 3.3b, alters the switching current of the inverter. Setting a capacitive ratio of $C_{PG} = 2C_{Pass}$, the maximum current during switching assuming strong inversion is:

$$I_{HL} = k_n \left(\frac{1}{3} (V_{gs} - (\gamma + \alpha S_{NpH})) + \frac{2}{3} V_{DD} - V_{th} \right)^2 \quad (3.6)$$

$$I_{LH} = k_p \left(\frac{1}{3} (V_{sg} + (\gamma + \alpha S_{NpH})) - V_{th} \right)^2 \quad (3.7)$$

The propagation delay of an inverter (t_{pd}) is determined by the capacitive load, the maximum supply voltage V_{DD} and the switching current, as follows:

$$t_{pd} = 0.7 \cdot \frac{C_L V_{DD}}{I_D} \quad (3.8)$$

From Eq. 3.6, 3.7 and 3.8, it is clear that any variation on the pH would create a change in the propagation delay, with a differential effect between the rise and the fall time: when t_{HL} increases, t_{LH} decreases and vice versa. Figure 3.3c presents this evolution of both t_{LH} and t_{HL}

at the ISFET inverter.

When this delay cell is integrated into the ring oscillator presented in Figure 3.3a, a chemically controlled PWM signal is generated. The difference in propagation delay created by the ISFET delay cell modulates both the oscillation frequency and the duty cycle of the generated clock.

3.2.3 Fabricated System - LEGOLAS

This section describes the testbench built for sensor characterisation, as well as the resources and algorithms employed.

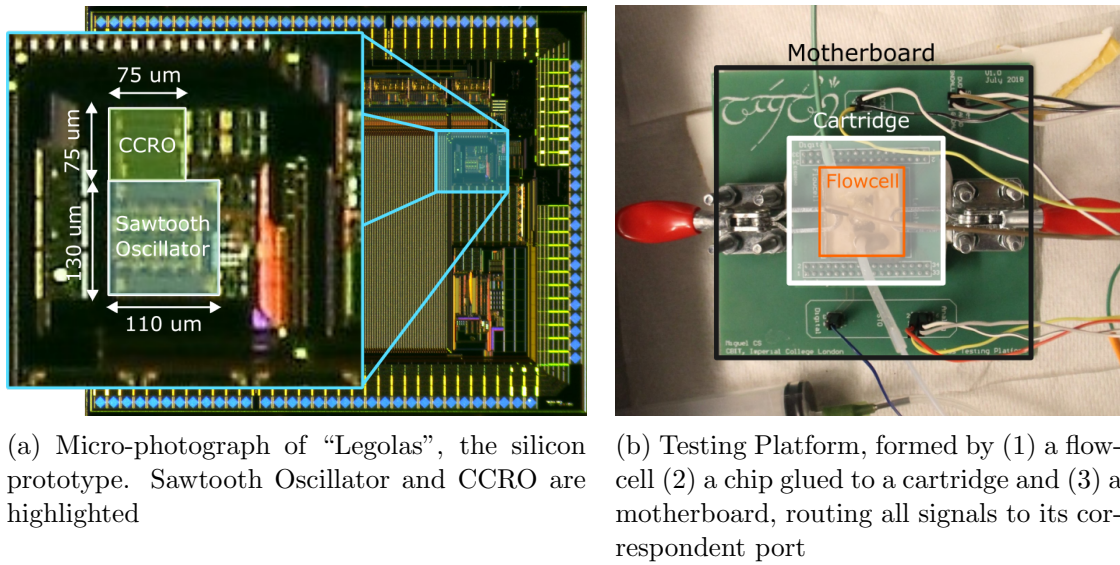


Figure 3.4: Experimental setup for sensor characterisation [16] (© 2019 IEEE)

Silicon Prototype

Figure 3.4a shows a microphotograph of the silicon prototype. The chip was fabricated in AMS 0.35 μm 2P4M CMOS technology. This technology was selected based on its maturity and cost-effectiveness, ideal for architecture prototyping on the analogue domain to establish a baseline for future scaling to state-of-the-art nodes.

The passivation layer used for pH sensing is Si_3N_4 , the standard passivation for this technology, allowing chemical sensing using unmodified CMOS fabrication process. The Sawtooth Oscillator occupies $110 \times 130 \mu m^2$, while the CCRO uses $75 \times 75 \mu m^2$. Their ISFET active area is $42.2 \times 18.2 \mu m^2$ and $65.1 \times 14.825 \mu m^2$ respectively, ensuring minimal oscillation coupling to the floating gate while maximising the sensitive area to reduce capacitive attenuation.

Cartridge, Chip Packaging And Testing PCB Board

The chip was placed onto the PCB cartridge shown in Figure 3.4b. This cartridge contains a large ground plane, where the silicon prototype is glued using conducting silver epoxy. The chip contacts were wire bonded to the cartridge and covered with bio-compatible epoxy.

This cartridge was mounted onto a testing motherboard, which routes and extracts the signals required for the architecture characterisation. Additionally, fixing clamps were included to attach the flow cell onto the cartridge, allowing the solution to flow over the chip without leakage.

Data Acquisition System

Four elements form the end-to-end acquisition schematic: A Keithley 4200A-SCS Parameter Analyser, the presented testing motherboard PCB, an FPGA Development Platform terasIC DE2i-150 and a desktop PC. The connections between these blocks are illustrated in Figure 3.5.

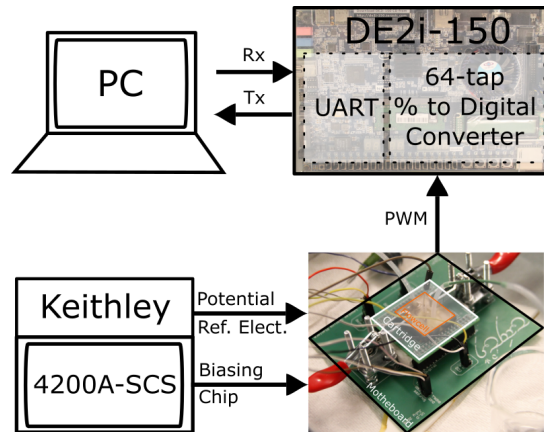


Figure 3.5: Schematic of the acquisition platform [16] (© 2019 IEEE)

The Keithley Parameter Analyser provides the biasing conditions required for the chip characterisation to both the motherboard PCB and the Ag/AgCl reference electrode attached to the flowcell. The PWM signals generated by the chip are connected through the motherboard to the FPGA Development Platform, which demodulates the Chemically Controlled Duty Cycle of the selected platform. This duty cycle demodulation is performed by sampling the PWM signal and storing the value of two counters: one accumulates the number of logical '1', and the second counts the number of samples on one period.

To enhance the resolution of this “Duty Cycle-to-Digital filter”, two improvements are included:

- The standard FPGA 50MHz clock is replaced by an internal FPGA PLL, locked at 175MHz, reducing the quantisation noise by improving the Over-Sampling Ratio (OSR)
- Filter counters sample the PWM signal for 64 periods, effectively implementing an averaging 64-taps FIR filter with decimation.

The data generated at the FPGA is transferred to a MatLab interface on a desktop computer for storage and data visualisation of the obtained measurements.

3.2.4 Electrical and Chemical Characterization - 8-Stage Sawtooth Oscillator Pixel

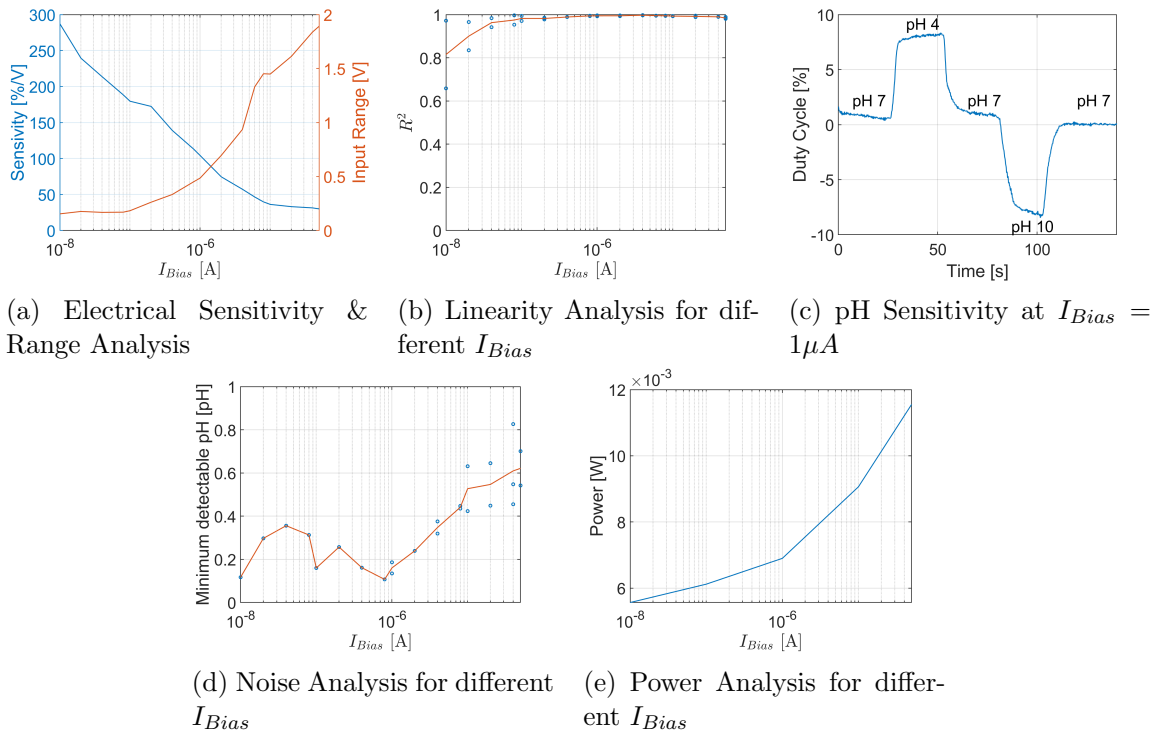


Figure 3.6: Sawtooth Oscillator Characterization Results [16] (© 2019 IEEE)

The characterisation assessed the Sawtooth Oscillator performance under different I_{Bias} conditions while maintaining V_{Ext} and V_{Osc} at a constant voltage, using the testbench described in Section 3.2.3. This parametric search was established empirically, upper-bounded by the power requirements and lower-bounded by both linear range and linearity performance.

Electrical Sensitivity & Range Analysis

The starting point was the electrical characterisation of the ISFET sensitivity. The electrical sensitivity characterisation was achieved by sweeping the potential of the Ag/AgCl reference electrode across the entire sensing range, increasing the voltage every second by a defined step. The size of the step was tailored to each scenario to reduce the time required to obtain the calibration curve, minimising the effect of temporal monotonic drift. Figure 3.7 provides an example of the calibration curve, where the Input Range was defined as the difference between the maximum and the minimum reference electrode voltage, and the Electrical Sensitivity was calculated by measuring the duty cycle change achieved throughout the Input Range.

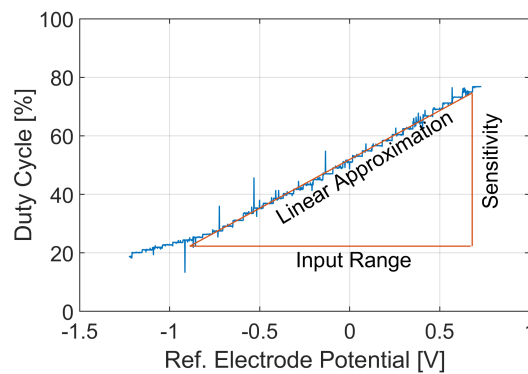


Figure 3.7: Standard calibration curve [16] (© 2019 IEEE)

As discussed in Section 3.2.1, the biasing current I_{Bias} determines the sensor's input range and electrical sensitivity. To characterise this dependency, calibration curves were obtained for a range of biasing currents, from $50\mu A$ to $10nA$. Figure 3.6a presents the results obtained, showing that by tuning I_{Bias} the system can control the behaviour of the architecture: large I_{Bias} provides a wide sensing range whereas small I_{Bias} enhances the pixel's sensitivity.

Linearity Analysis

One of the main benefits mentioned in Section 3.2.1 is the Sawtooth Oscillator's high linearity control. The importance of linearity on sensor applications has been highlighted throughout the literature [19–21], as it simplifies compensation schemes, prevents signal distortion and reduces post-processing steps.

The linearity of the sensor was evaluated by measuring the coefficient of determination (R^2) of its electrical sensitivity curves against a linear fit, obtaining a value of 0.9945 when $I_{Bias} = 1\mu A$.

This analysis was expanded to different I_{Bias} to understand the evolution of this linearity across a range of biasing points, obtaining the results shown in Figure 3.6b. These results

confirmed that the architecture maintains a good linearity performance across a range of biasing conditions, with a slight decay for low values of I_{Bias} .

pH Sensitivity

Next, the architecture's capability to sense pH was tested, defining the relationship between duty cycle variations and pH changes. To test this sensitivity, the architecture was biased at $I_{Bias} = 1\mu A$ and calibrated to an output duty cycle of 50% to ensure maximum dynamic range, and a set of pH buffers of known value - pH 4, 7 and 10 - were sequentially injected into the flowcell. These pH buffers created sharp transient changes at the system's output, as presented in Figure 3.6c. Note that chemical drift was estimated and subtracted from this figure as a post-processing step.

Using the electrical sensitivity values measured in Section 3.2.4, a pH sensitivity of 26.6mV/pH was obtained. This value is similar to the ones reported in the literature [22] [19] and proves that the architecture can detect changes in the ion concentration of a solution.

Chemical Drift

ISFETs implemented in unmodified CMOS technology suffer from a long-term monotonic drift at the output. In order to characterise this phenomenon, the chip was exposed to a pH 7 solution with a constant reference electrode potential and a calibrated duty cycle of 50%. Figure 3.8a shows the recorded temporal variation at the output. For a biasing current of $I_{Bias} = 1\mu A$, the average drift was 0.3567mV/s with a standard deviation of 0.46mV/s. This high standard deviation value indicates a large variability of the drift value due to its long-term exponential behaviour, which has been previously proven to be dependent on various factors such as time, trapped charge, and reference electrode potential [23, 24], highlighting the importance of compensation mechanisms capable of adapting to this uncertain phenomena.

Noise Analysis

To evaluate the combination of chemical and electrical noise present at the sensor, the chip was exposed to a pH 7 solution, recording the temporal evolution of the output. Using the sensor's sensitivity, the input-referred Noise Power Spectral Density (PSD) plot was obtained from these samples, as shown in Figure 3.8b.

The sensor's resolution was inferred from this plot by integrating the PSD between 10 mHz and 8 Hz, following the same criteria used in [25]. Using this methodology, an average minimum

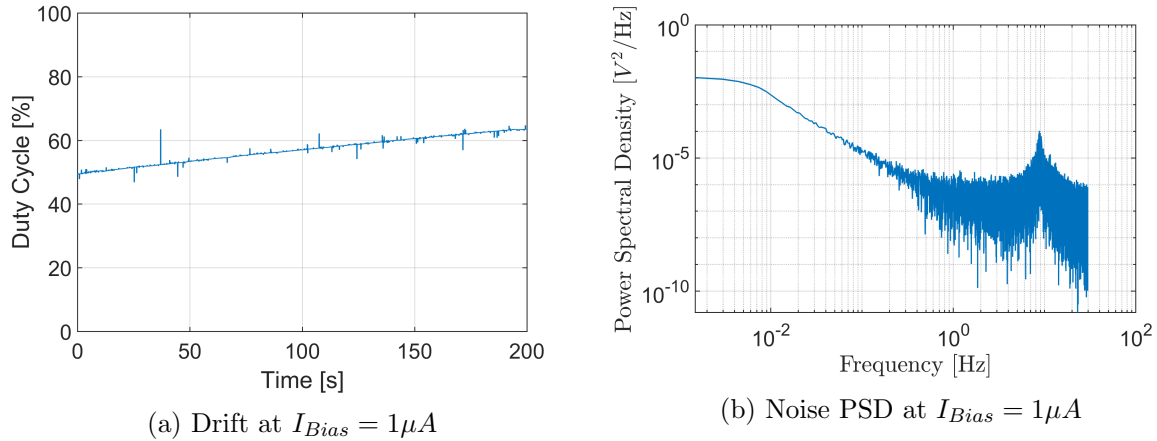


Figure 3.8: Drift and Noise Analysis for Sawtooth Architecture with $I_{Bias} = 1\mu A$ [16] (© 2019 IEEE)

detectable pH of 0.1604 pH units was calculated, with a standard deviation of 0.0365 pH units for a biasing current of $I_{Bias} = 1\mu A$. The reason behind this decrease in resolution compared with the state-of-the-art is believed to be the sum of two phenomena: firstly, the significant drift reported was reflected on the PSD as more prominent flicker noise, raising the noise floor. Secondly, the reduced transconductance of the input stage, the Linear OTA, further degraded the noise performance.

The effect of I_{Bias} on noise was then studied by running this experiment across a range of bias currents. Figure 3.6d presents the results obtained, showing an increment on the noise floor at high values of I_{Bias} . An increase in the quantisation noise causes this rise, as any increment in I_{Bias} would raise the oscillating frequency, decreasing the Over-Sampling Ratio (OSR). Regarding the oscillatory behaviour at lower I_{Bias} , this is an experimental artifact due to mismatch between drift rate on different experiments.

Power Performance

The power consumption was evaluated under different biasing conditions, as presented in Figure 3.6e. The power consumption followed I_{Bias} trend due to the correlation between the biasing current and the oscillation frequency, achieving 6.9mW for $I_{Bias} = 1\mu A$. The baseline of this trend is mainly determined by the number of stages on the Sawtooth Oscillator.

V_{Ext} Compensation

One of the main benefits of this architecture is the possibility of using an external potential V_{Ext} to set the operating point of the OTA. This operation was tested by setting $I_{Bias} = 1\mu A$ and

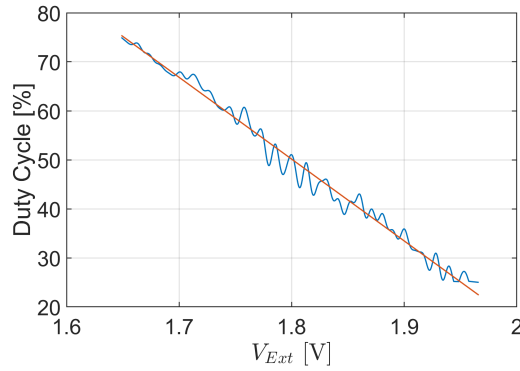


Figure 3.9: Sawtooth Oscillator V_{Ext} characterisation [16] (© 2019 IEEE)

establishing a constant reference electrode potential while sweeping the value of V_{Ext} throughout the sensor's range. Figure 3.9 presents the curve obtained, confirming the programmability of this architecture through its external terminal. This scheme has a compensation range of 2.7564V, comprising the voltages between PMOS V_{th} and ground, and a linear range of 0.3174V, determined by the OTA's Linear Range. This compensation mechanism has the potential to correct the sensor's trapped charge and monotonic drift using a programmable DAC, homogenising the sensor's response across devices and enhancing the reproducibility of the measurements carried on this sensor.

Additionally, using Figure 3.9 it was possible to measure the capacitive attenuation by comparing OTA's Input Range of the electrical input, V_{Ext} , with the chemical input, V_{Ref} . For $I_{Bias} = 1\mu A$, their input range were 0.3174V and 0.4860V respectively, obtaining an attenuation value of 0.6531.

Analysis and trade-offs on architecture operation

Based on the presented results, the influence of the programmable parameter I_{Bias} on the architecture performance can be analysed. Table 3.1 includes a summary of these results, Table 3.2 highlights the observed trade-offs.

Table 3.1: Sawtooth Oscillator Performance Analysis [16] (© 2019 IEEE)

I_{Bias} [A]	E. Sensitivity [%/V]	Range [V]	Linearity [R^2]	Resolution [pH]	Power [mW]
$50\mu A$	30.02	1.90	0.98	0.62	11.6
$10\mu A$	36.28	1.45	0.99	0.53	9.1
$1\mu A$	104.21	0.49	0.99	0.16	6.9
$100nA$	179.68	0.18	0.98	0.16	6.1
$10nA$	287.29	0.15	0.82	0.12	5.6

From these tables, it can be derived that this architecture presents a multi-dimensional trade-off: any decrease in I_{Bias} would positively impact both the minimum detectable pH and power, whereas any I_{Bias} increase would improve both dynamic range and linearity. Furthermore,

Table 3.2: Sawtooth Oscillator Trade-off Analysis [16] (© 2019 IEEE)

Parameter	$\uparrow I_{Bias}$
E. Sensitivity	\downarrow
Range	\uparrow
Linearity	\uparrow
Resolution	\downarrow
Power	\uparrow

this architecture presents a significant baseline power consumption, with over 5 mW per pixel with the smallest I_{Bias} . This is associated to the high number of oscillatory stages and would represent a significant scalability barrier when moving to highly parallel arrays, and will be revisited in Section 3.3.

Taking into account the trade-offs, biasing conditions around $I_{Bias} = 1\mu A$ are considered balanced options, as they share good sensitivity and reasonable power consumption while maintaining good linearity and a wide input range.

3.2.5 Electrical and Chemical Characterization - CCRO Pixel

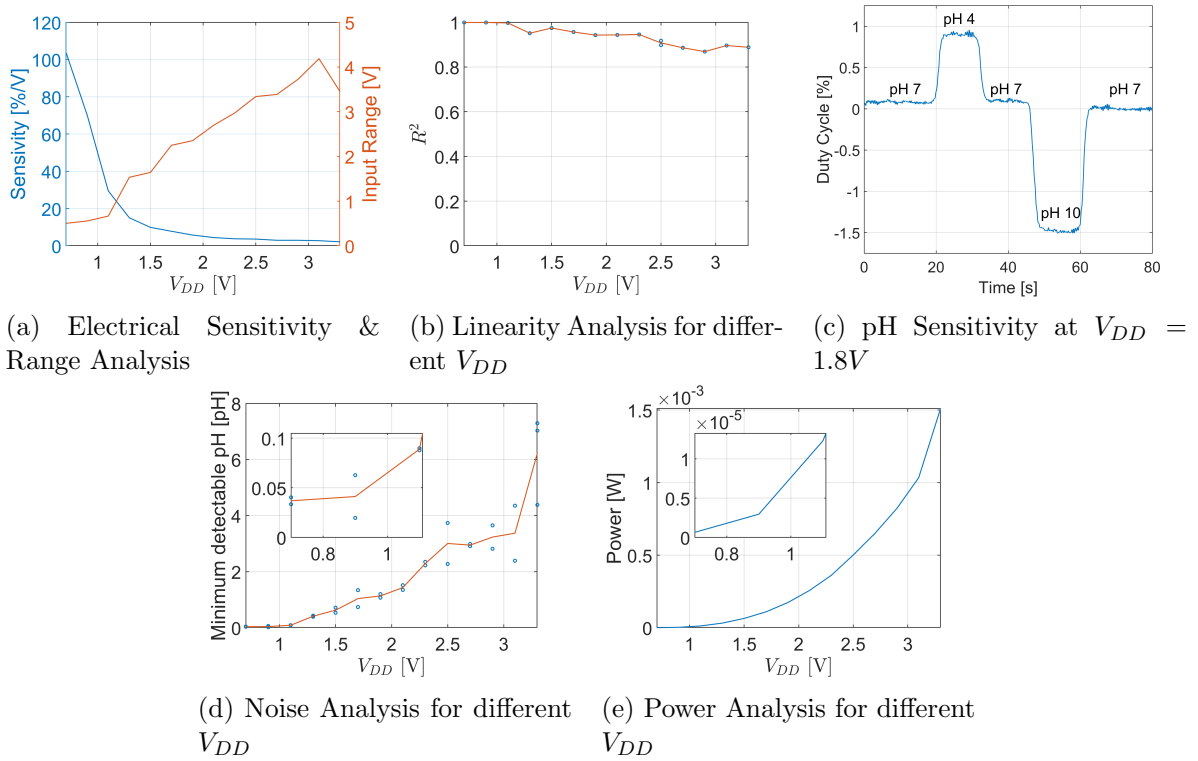


Figure 3.10: Chemically Controlled Ring Oscillator Characterization Results [16] (© 2019 IEEE)

The performance of the second architecture, the Chemically Controlled Ring Oscillator (CCRO), was characterised for different supply voltages V_{DD} . The test methodology was identical to the

one presented in Section 3.2.4, using the testbench described in Section 3.2.3. The parametric search for ideal biasing was established by the maximum VDD for this technology, and the smallest voltage supply that the acquisition system could recover.

Electrical Sensitivity & Range Analysis

The electrical sensitivity of the architecture was obtained by sweeping the Ag/AgCl reference electrode and measuring the PWM output, resulting in curves like the one presented in Figure 3.7. Section 3.2.2 described the possibility of tuning both the input range and the electrical sensitivity by modifying the supply voltage of the sensor. To confirm this statement, calibration curves were obtained for a range of supplies voltages, from 3.3 to 0.7V, showing an exponential increase of the electrical sensitivity with a decrease of V_{DD} as presented in Figure 3.10a, with a linear decrease of the input range.

The behaviour of these two parameters is explained by Eq. 3.4, 3.6 and 3.7 in Section 3.2.2: The voltage range at $V_{g''}$ decreases linearly with V_{PG} , which in turn depends linearly on the power supply. On the other hand, the electrical sensitivity increases following the quadratic behaviour of I_{LH} and I_{HL} , thus decreasing V_{DD} would lead to an increase in the sensor's sensitivity. Therefore, the trade-off between input range and electrical sensitivity is controlled directly by the supply voltage, eliminating the need for additional external bias. Furthermore, the architecture can operate at a wide range of supply voltages, making it suitable for deep submicron technologies.

Linearity Analysis

As discussed in Section 3.2.4, sensor's linearity is crucial to achieving scalable and robust systems. The linearity of the sensor response was assessed by the coefficient of determination (R^2) of the calibration curve's linear fit. This R^2 coefficient was calculated for every calibration curve at different supply voltages, characterising the effect of V_{DD} on the curve's linearity. Figure 3.10b shows these results, illustrating an increase in linearity when low power supplies are applied. An example of this is the linearity at $V_{DD} = 0.7V$, where $R^2 = 0.9992$.

pH Sensitivity

The capability of the chip of sensing pH changes was proven in Section 3.2.4, and these results were verified on this architecture, as shown in Figure 3.10c.

Chemical Drift

Chemical drift was evaluated for the CCRO following the methodology described in Section 3.2.4. In this architecture, for a $V_{DD} = 0.7V$, we obtained an average drift of $4.7297\mu V/s$ with a standard deviation of $3.2673\mu V/s$.

Noise Analysis

Following the procedure explained in Section 3.2.4, Input-referred Noise PSD plots were obtained for different V_{DD} values. Integrating this Input-referred noise from 10 mHz to 8 Hz [25], the minimum detectable pH for each supply voltage was inferred, resulting in Figure 3.10d.

For a voltage supply of $V_{DD} = 0.7V$, an average minimum detectable pH of 0.0369 pH with a standard deviation of 0.0049 pH was obtained, achieving a resolution comparable to the state-of-the-art [25, 26].

However, this noise performance was degraded for high values of V_{DD} . This noise floor increase is associated with the variation of the oscillation frequency and the supply voltage: as the supply increases, the oscillator frequency also increases, leading to higher phase noise and reduced OSR. Along with a smaller electrical sensitivity, this leads to a reduced SNR. On the other hand, a reduction of the power supply would decrease the oscillating frequency, boosting the OSR ratio, the oscillator's phase noise performance and, ultimately, the pH resolution of the sensor [12] [13]. These variations would need to be verified in a test device, decoupling the device noise contributions from the chemical noise contributions. This remains future work for this thesis.

Power Performance

The use of the supply voltage as a tuning parameter of electrical sensitivity would affect the evolution of power consumption. Figure 3.10e shows this power evolution, achieving $655nW$ at $V_{DD} = 0.7V$, the same biasing point where high resolution and high electrical sensitivity were obtained.

Analysis and trade-offs on architecture operation

The obtained results allow the comparison of the architecture performance for different supplies voltages, assessing its trade-offs. For this purpose, Table 3.3 shows the evolution of the main performance metrics with V_{DD} , with Table 3.4 summarizing the trade-offs.

Table 3.3: CCRO Performance Analysis [16] (© 2019 IEEE)

V_{DD} [V]	E. Sensitivity [%/V]	Range [V]	Linearity [R^2]	Resolution [pH]	Power [mW]
3.3	2.20	3.45	0.89	6.24	1.5
2.7	3.02	3.39	0.89	2.95	0.65
2.1	4.47	2.70	0.94	1.43	0.26
1.5	9.95	1.64	0.97	0.63	0.065
1.1	29.55	0.67	1.00	0.09	0.012
0.7	103.66	0.50	1.00	0.04	0.00065

Table 3.4: CCRO Trade-off Analysis [16] (© 2019 IEEE)

Parameter	$\uparrow V_{DD}$
E. Sensitivity	\downarrow
Range	\uparrow
Linearity	\downarrow
Resolution	\downarrow
Power	\uparrow

From this table, it is clear that reducing V_{DD} improves the performance in terms of sensitivity, linearity, resolution and power, at the expense of a reduced input range. This analysis indicates that this architecture should be operated at the lowest possible V_{DD} , an ideal characteristic for scalable sensors implemented on deep submicron technologies where reduced supply voltages are required.

3.2.6 Architecture Comparison

These architectures present a programmable electrical sensitivity, allowing the sensor to adapt to the application requirements. Using a tailored electrical sensitivity, the sensor's response can be modified through external circuits to overcome fabrication mismatches and adapted to specific scenarios and external conditions. Additionally, programmable schemes can be easily implemented on-chip in a scaling-friendly manner, ideal for portable sensing applications.

Individually, each architecture offers unique benefits that make them suitable for specific scenarios. On the one hand, the Sawtooth Oscillator stands out for its robustness and programmability at different levels. The possibility of modifying the linear OTA equilibrium point through an external voltage V_{Ext} could potentially be used to compensate trapped charge and monotonic drift beyond the standard calibration schemes presented in the literature [27] [28]. This scheme, along with the programmable sensitivity, can enhance the robustness and reproducibility of the sensor's response, establishing homogeneous and consistent sensing conditions between sensors in the same chip and between chips. However, this architecture suffers from large power consumption, limited resolution and occupies a large area, and its scalability to deep sub-micron processes is limited by the noise floor [29].

On the other hand, the Chemically Controlled Ring Oscillator (CCRO) benefits from this node scalability to achieve high electrical sensitivity and low power consumption. By scaling this architecture with Moore's law to deep submicron processes, the architecture performance

would be augmented by reducing its size, decreasing the power consumption and enhancing its sensitivity, forming a compact, low power pixel that could be easily integrated on a portable, fully digital system. However, this front-end lacks calibration and compensation mechanisms for ISFET's non-idealities, making it vulnerable to trapped charge and drift variations.

The potential for long-term monitoring thanks to the various degrees of programmability makes the Sawtooth Oscillator a more attractive option for developing large ISFET arrays with embedded adaptability to external and internal conditions. Furthermore, a reduction in the number of stages can enhance its performance in terms of power consumption and pixel area while maintaining its linearity and resolution. Last but not least, this architecture has the potential to encode both temperature and chemical information in the same waveform, enabling the development of a dual-sensing array as described in the following section.

3.3 Dual-Sensing ISFET Array

The attractive benefits in terms of programmability and versatility for addressing ISFET limitations regarding robustness and long-term monitoring and its potential for multi-variable modulation prompt me to select the 8-stage Sawtooth Oscillator as the best architecture for developing a large ISFET array.

However, limitations in area, resolution and power consumption needed to be addressed to achieve a compact pixel suitable for precise sensing on portable platforms. Hence, I reduced the initial 8-stage architecture to a fully differential 2-stage Sawtooth oscillator, following the approach proposed in [9, 30], overcoming both power and area consumption barriers. Furthermore, this architecture could sense and encode ion concentration and solution temperature into a single PWM output signal, achieving dual-sensing thermo-chemical measurement. Hence, the output PWM signal has two modulated variables: the ion concentration sensed by the ISFET is encoded into the duty cycle, leveraging on a differential sensing approach to achieve robustness, linearity and programmability; and the solution temperature is modulated onto the frequency of the PWM signal, benefiting from large dynamics and quadratic sensitivity. This pixel was integrated as part of a 32x32 array, demonstrating its suitability for large ISFET imagers. This section analyses in detail this architecture.

3.3.1 Chemical Sensing - Principle of operation

The architecture presented in Figure 3.11 encodes the ion information sensed by the ISFET into the duty cycle of a PWM signal. This sensing scheme is composed by two sub-blocks:

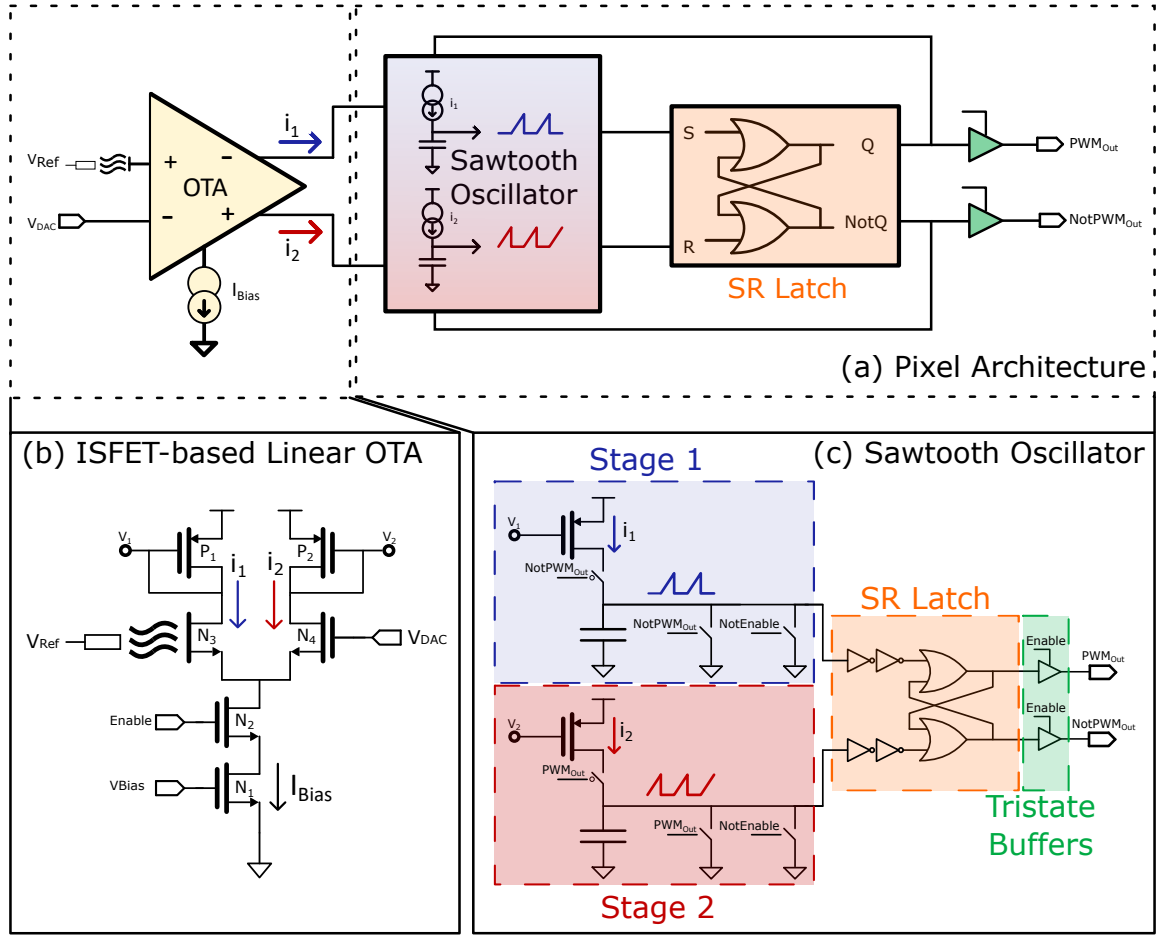


Figure 3.11: Sawtooth Oscillator High Level Schematic showing (a) Overall pixel structure, composed by (b) ISFET-based Linear OTA transforming input differential voltages V_{ISFET} and V_{DAC} into differential currents i_1 & i_2 which will be mirrored to (c) 2-Stage Sawtooth Oscillator, creating a PWM signal from the mirrored currents i_1 & i_2 by charging capacitors alternatively [31] ((© 2020 IEEE))

ISFET-based Linear OTA

The ISFET-Based Linear OTA creates a differential output current from a differential input voltage. An ISFET replaces one of the MOSFET at the differential pair, providing pH sensitivity, while the second branch is biased through an off-pixel voltage, V_{DAC} . When this differential pair is operating at the linear region, any variation at the ISFET gate would trigger a change in the differential currents i_1 and i_2 . Assuming the differential pair is matched ($g_{m3} = g_{m4} = g_m$), these current differences can be described as Eq. 3.9 and 3.10:

$$I_{Bias} = i_1 + i_2 \quad (3.9)$$

$$i_1 - i_2 = \frac{g_m}{2}(V_{ISFET}(pH) - V_{DAC}) \quad (3.10)$$

where $V_{ISFET}(pH) = V_{g''}$ and $g_m \propto I_{Bias}$ for a constant V_{ov} . From Eq. 3.9 and 3.10, two externally programmable parameters can tune the sensor's behaviour:

- I_{Bias} controls the linear range and the sensitivity. This current can be set using an external current source or a biasing voltage.
- V_{DAC} sets the equilibrium point of the linear OTA

This programmability was simulated to confirm the equations. Figure 3.12 presents simulated results of the evolution of i_1 with any difference between V_{ISFET} and V_{DAC} . The differential currents generated in this stage are mirrored to the sawtooth oscillator, modulating its PWM response.

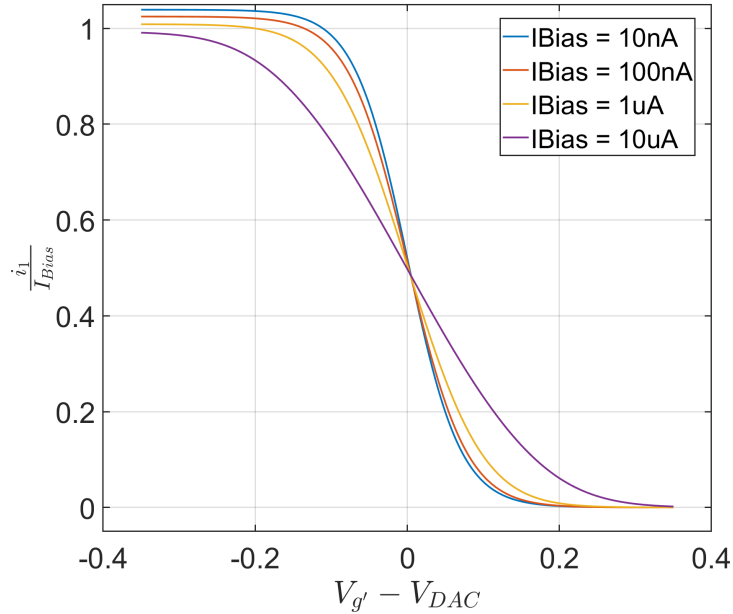


Figure 3.12: Simulation of linear OTA current under different biasing conditions [31] (© 2020 IEEE)

2-stage Sawtooth Oscillator

Sawtooth Oscillators are a type of relaxation oscillator that creates a PWM waveform by charging alternatively two capacitors [9, 30]. These oscillators, previously used for sensing purposes in [7–9, 16], are known for exhibiting high linearity control and low phase noise.

To chemically modulate the oscillator's duty cycle, the capacitor at each stage is charged linearly by the differential currents generated on the ISFET-Based OTA, integrating the input signals over the charging phase. This charging phase alternates between stages, with only one capacitor charging at a time. When the charging capacitor reaches the inverter threshold voltage, the SR latch toggles the oscillator polarity, inverting the charging process: the previous capacitor discharges, and the second capacitor starts accepting current. This charging process creates a delay on each stage defined by:

$$T_{charge} \propto \frac{V_{th_{Inv}} \cdot C}{I(pH, V_{DAC})} \quad (3.11)$$

being $V_{th_{Inv}}$ the inverter threshold voltage, C the value of the stage's capacitor and I the current fed into the stage, either i_1 or i_2 . From T_{charge} , the duty cycle is defined as follows:

$$PWM_{DutyCycle} = \frac{T_{charge_{S2}}}{T_{charge_{S1}} + T_{charge_{S2}}} \quad (3.12)$$

$$PWM_{DutyCycle} \propto \frac{i_1}{i_1 + i_2} \quad (3.13)$$

Eq. 3.13 shows that any difference between these differential currents i_1 and i_2 creates a difference in the delay time of each stage, hence modulating the duty cycle of the output PWM signal. Figure 3.13 presents a simulation of this phenomenon, showing both the charging waveforms and the generated PWM signal.

3.3.2 Thermal Sensing - Principle of operation

The integration of ISFET imagers as part of DNA-based Point-of-Care platforms have created the need for thermal sensing on the target solution to enable precise temperature control, a critical element when running PCR or LAMP protocols. In this context, uneven heat transmission from the heating element might cause spatiotemporal reaction dynamics, which would influence the ISFET sensor response. If no thermal sensing is introduced in each pixel, these thermal-induced dynamics would couple directly to each ISFET sensor as chemical changes, potentially leading to misleading results. Hence, in order to mitigate this thermo-chemical cross-sensitivity, this pixel architecture introduces in-pixel thermal sensing leveraging the underlying physics of the MOSFET devices, without impacting the pixel footprint.

Each pixel encodes its local temperature into the frequency of the output PWM signal, obtaining spatial information of the distribution of temperatures across the array. This frequency

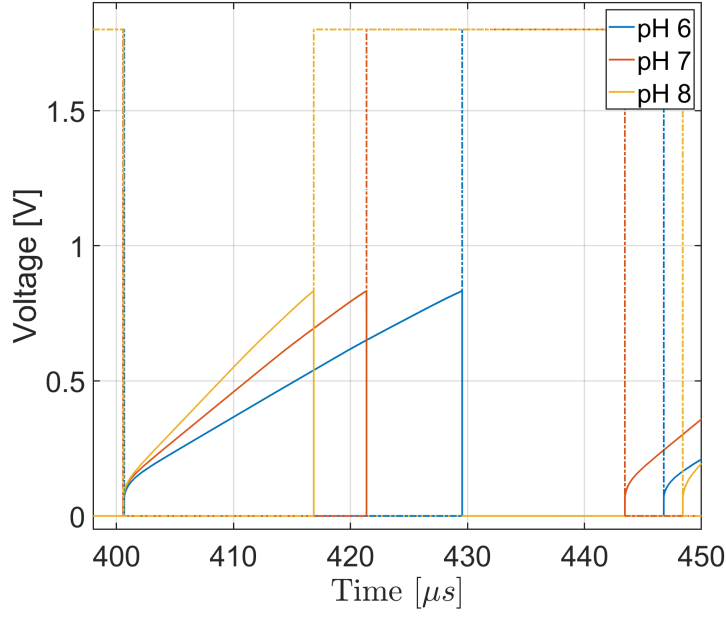


Figure 3.13: Simulation of Sawtooth Oscillator under different pH conditions, assuming a sensing layer sensitivity of 30 mV/pH and $I_{Bias} = 10nA$ [31] (© 2020 IEEE)

modulation scheme leverages the thermal sensitivity of N1 when operated on the weak inversion region, creating a variation on the biasing current that increases the oscillator frequency. This biasing current thermal sensitivity can be modelled as follows [32]:

$$I_{ds_{ub}}(T) = I_0(T) \exp \frac{V_{gs} - V_{th}(T)}{nkT/q} \left(1 - \exp \frac{-V_{ds}}{kT/q} \right) \quad (3.14)$$

where $I_0(T)$ is a technology-specific parameter with a thermal dependency expressed in Eq.3.15, and V_{th} is the thermally controlled threshold voltage as shown in Eq.3.16.

$$I_0(T) = \mu_0 C_{ox} \frac{W}{L} e^{1.8} (kT/q)^2 \quad (3.15)$$

where μ_0 is the zero bias carrier mobility, C_{ox} the gate oxide capacitance and W and L the transistor sizes.

$$V_{th}(T) = V_{th0} + \left(K_1 + \frac{K_2}{L} + K_3 V_{bs} \right) \left(\frac{T}{T_0} - 1 \right) \quad (3.16)$$

where V_{th0} refers to the threshold at T_0 , K_1 is the temperature coefficient of the threshold voltage, K_2 is the channel-length coefficient of the threshold voltage, K_3 is the bulk-bias coefficient of the threshold voltage and V_{bs} is the bulk-source potential.

Assuming that $V_{ds} > 4U_t$, the thermal dependency of the biasing current can be simplified to:

$$I_{d_{sub}}(T) = K_\alpha T^2 \exp \frac{-K_\beta}{T} \quad (3.17)$$

with K_α and K_β defined as:

$$K_\alpha = \frac{\mu_0 C_{ox} \frac{W}{L} e^{1.8 \left(\frac{k}{q} \right)^2}}{\exp \frac{K_1 + \frac{K_2}{L} + K_3 V_{bs}}{T_0 n k / q}} \quad (3.18)$$

$$K_\beta = \frac{-V_{gs} + V_{th0} - K_1 - \frac{K_2}{L} - K_3 V_{bs}}{n k / q} \quad (3.19)$$

This relationship is complex and includes several quadratic and exponential terms. However, as discussed in Section 3.3.6, the transfer function can be later approximated as a quadratic relationship for the input range of our application.

Despite its non-linear behaviour, this approach is optimal for this scenario, limiting the pixel footprint by leveraging the device's physics. Alternative thermal sensors, such as the Proportional To Absolute Temperature (PTAT) architecture, would require additional pixel space, dedicated readout and biasing as well as wiring and power overhead - undesirable effects for achieving linearity at the sensor level.

3.3.3 System-Level Architecture

The pixel architecture was integrated into a system composed of 3 blocks, described hereafter.

ISFET Array

The 32x32 ISFET array was created using dual-sensing pixels. Each pixel contains under its active area a linear OTA, two current mirrors, two $31 \times 4 \mu m^2$ capacitors yielding 65fF each, control switches, an SR latch and tristate buffers. The capacitors' value, implemented using the Metal-Insulator-Metal architecture, were maximised to achieve good output OSR while maintaining the compact pixel form factor of $40 \times 40 \mu m$. The pixels are uniquely addressed using Row and Column signals, activating only one pixel at a time. All pixels share a global V_{DAC} input and the PWM_{Out} & $NotPWM_{Out}$ datapath, as illustrated in Figure 3.14a. In-pixel tristate buffers perform the output datapath control, allowing only one pixel to transmit.

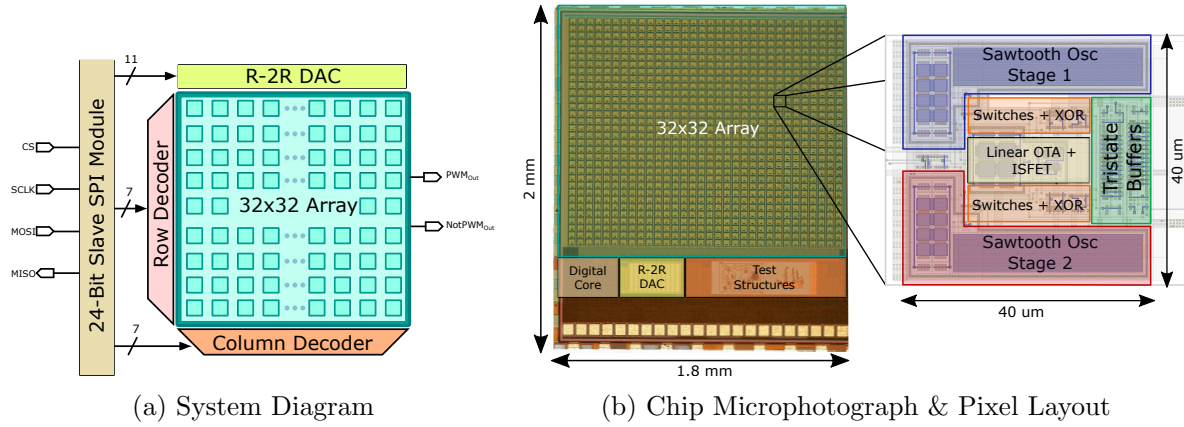


Figure 3.14: BlackPearl System Architecture illustrating (a) the high-level system architecture, presenting the different blocks and their interconnections with the 32x32 array, and (b) silicon prototype of this system, with the detail portraying the pixel layout and its internal structure [31] (© 2020 IEEE)

On-Chip DAC

The global on-chip R-2R 11-bit DAC enables pixel-wise programmability of operation point by generating a V_{DAC} signal. The DAC input code is generated externally and transmitted through Serial Peripheral Interface (SPI). This value can be tailored for each pixel to compensate for trapped charge and other non-idealities. Global DAC approach was selected over column-, block- or pixel-wise DAC to maximise ISFET sensing area, as multiple DAC blocks would require large silicon area, additional digital circuitry and multiple IO pads for parallel readout.

SPI Interface and Row/Column Decoders

The 24-bit slave SPI unit serves as a standard interface with external devices. The SPI message provides the digital code for the DAC as mentioned earlier (V_{DAC}) and selects a target pixel through Row and Column decoders.

3.3.4 Fabricated System - Black Pearl

This section describes the test elements used to characterise the array and the resources and algorithms employed.

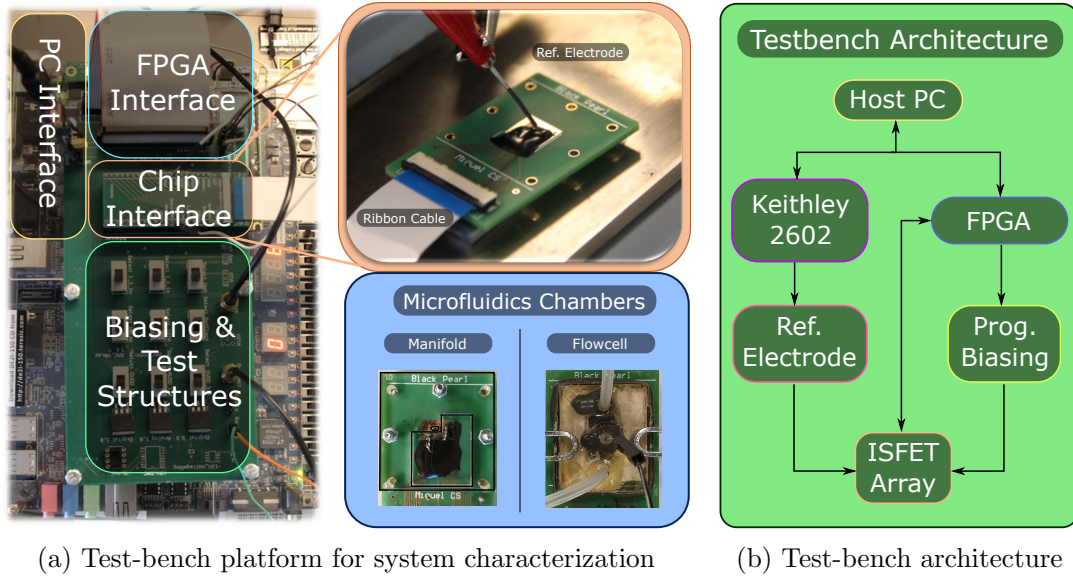


Figure 3.15: Measurement setup for characterisation of silicon prototype. (a) Motherboard architecture, with details on chip interface and microfluidic chambers utilised. (b) Communication structure between different testbench blocks [31] (© 2020 IEEE)

Silicon Prototype & Testing Platform

The chip was fabricated in TSMC $0.18\mu\text{m}$ M6 CMOS technology, using its standard passivation (Si_3N_4) for pH sensing. The choice of TSMC and $0.18\mu\text{m}$ process node for this chip was based on commercial agreements at the time of fabrication, as AMS shifted their focus towards industrial applications and eliminated their academic offering. Furthermore, the node choice was a trade-off between performance, cost-effectiveness and shared needs across the team.

The entire system occupies $1.8 \times 2 \text{ mm}^2$, where each pixel occupies $40 \times 40 \mu\text{m}^2$ with a matching active area. Furthermore, an M4 layer connected to ground shields this active area from oscillatory disturbances. Figure 3.14b shows a microphotograph of the silicon prototype, highlighting all relevant blocks.

The testing platform built to characterise the silicon prototype performance was composed of 5 elements.

- **Cartridge** \Rightarrow A compact cartridge was designed to interconnect the silicon prototype to the testing platform, as presented in Figure 3.15a. The chip was attached to the ground plane using conductive epoxy (EPO-TEK H20E), and all bond pads were covered using electrically insulating epoxy (EPO-TEK T7139). The cartridge was connected to a testing platform through a ribbon cable.
- **Testbench PCB** \Rightarrow The testing PCB handled the powering, biasing and communication between the control devices and the silicon prototype.

- **FPGA Platform** \Rightarrow The FPGA Development Platform terasIC DE2i-150 handled the SPI communication with the cartridge platform and the sampling and digitisation of the output PWM signal. Furthermore, the FPGA platform stored in memory the DAC values required for the pixel-wise calibration, allowing trapped charge compensation and drift cancellation. The FPGA system was connected to the host PC through a serial interface, executing pre-programmed actions upon PC request.
- **Keithley 2602** \Rightarrow The Keithley, controlled by the Host PC, provided the Ag/AgCl reference electrode potential.
- **Host PC** \Rightarrow The Host PC provided a MatLab-based user interface that coordinates the different tests, displaying the status of the experiments and storing its results.

Figure 3.15b illustrates the architecture and the communications interfaces required for this platform to operate.

Microfluidic Components

Three strategies have been followed to enable solution compartment during experimentation.

- The first and simplest, presented in the top right of Figure 3.15a, placed a small sample of the solution on the surface of the chip. However, this strategy was only valid for initial functional verification as the sample quickly evaporates.
- The acrylic manifold was utilised as a reaction chamber, preventing sample leakage and evaporation, as well as ensuring consistent testing conditions across experiments. The manifold was screwed to the cartridge, exposing only a reduced chip area and holding a reaction volume of $4.41\mu L$.
- The flowcell performed sequential flow of different pH buffers, enabling the verification of the architecture pH sensitivity. This flowcell was attached to the cartridge using fixing clamps, and the reference electrode was inserted through the central opening.

Figure 3.15a presents these two microfluidic devices.

Buffer preparation

In order to assess the pH sensitivity of the architecture, a set of pH buffers (6, 7 & 8) were prepared. Firstly, a background solution was prepared with 1M Tricine (Sigma Aldrich T0377),

3M KCl (Sigma Aldrich 60137) and de-ionised water. The pH of this background solution was adjusted by adding either 1M HCl (Sigma Aldrich 318949) or 1M NaOH (Sigma Aldrich 71463), monitoring the exact pH value using Sentron SI400 pH meter.

Temperature Characterization & Control

The temperature of the platform was regulated using a Veriti 96-Well Thermal Cycler (Applied Biosystems). This strategy enabled precise temperature control to evaluate the sensor performance under different thermal conditions and perform LAMP DNA amplification experiments.

3.3.5 Experimental Results: Chemical Sensor

This section presents the results obtained from the electrical and chemical characterisation of the ISFET. Unless stated, these experiments were performed under $I_{Bias} = 10nA$.

Characteristic Response Analysis

The ISFET array characterisation analysis was obtained by immersing the Ag/AgCl reference electrode into a pH 7 solution and sweeping its potential throughout the sensing range while maintaining V_{DAC} a constant voltage. By observing the output change to this reference electrode sweep for each pixel, the Input Range, Electrical Sensitivity, Linearity and Trapped charge across the array were evaluated. Figure 3.16 presents an example of the duty cycle response obtained on each pixel, defining the linear range between 15% and 85%. From this curve, the pixel parameters were obtained following equations 3.20, 3.21 & 3.22.

$$InputRange = \max(Ref.Elect.) - \min(Ref.Elect.) \quad (3.20)$$

$$S_{Elect} = \frac{\max(PWM) - \min(PWM)}{\max(Ref.Elect.) - \min(Ref.Elect.)} \quad (3.21)$$

$$TrappedCharge = Ref.Elect.(PWM = 50\%) \quad (3.22)$$

Figure 3.17a & 3.17b provide the distribution of sensitivities and trapped charge across the array. This characterisation experiment was replicated for different chips to evaluate the effect of process variations on the architecture. Figure 3.17c presents the obtained results and Table 3.5 summarises the mean value of the parameters along with the standard deviation between

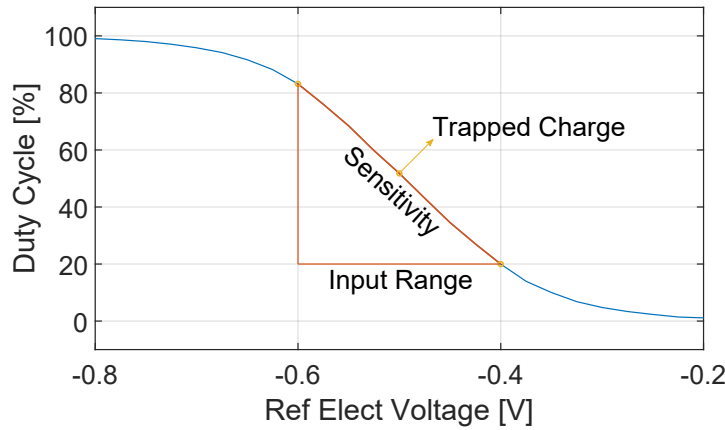


Figure 3.16: Pixel Characterisation Curve [31] (© 2020 IEEE)

pixels, showing consistent sensitivity across chips. The small values of standard deviation on sensitivity and linearity prove the robustness of this architecture, achieving a homogeneous and highly linear characteristic response across the array. The robustness of the sensitivities is tested through a unpaired T-Test, obtaining a p-value $\gg 0.05$ and confirming that all chips' sensitivity distributions yield equal means. The distribution of trapped charge is in line with previously reported values in the literature [25, 33]

Table 3.5: Characterization Results [31] (© 2020 IEEE)

Parameter	Mean	Std. Dev.
S_{Elect} [%/V]	321.65	0.18
Range [V]	0.20	0.019
Linearity [R^2]	0.99	0.0037
Trapped Charge [V]	-1.30	1.01

Programmable Sensitivity

The input signal I_{Bias} tunes the linear range and the sensitivity of the architecture. This programmability was tested by observing the characterisation curves for different I_{Bias} values, obtaining the results presented in Figure 3.17d. A trade-off between range and sensitivity was observed: higher I_{Bias} achieve a more extensive input range by decreasing the sensitivity and vice-versa. Furthermore, an increase on I_{Bias} will also affect the oscillation frequency, negatively impacting the Over-Sampling Ratio (OSR).

Attenuation Analysis

Due to the additional capacitance introduced at the floating gate on standard CMOS fabrication, the chemical signal is attenuated through a capacitive division [17]. The characterisation curves can be compared with a sweep in V_{DAC} voltage using a constant reference electrode

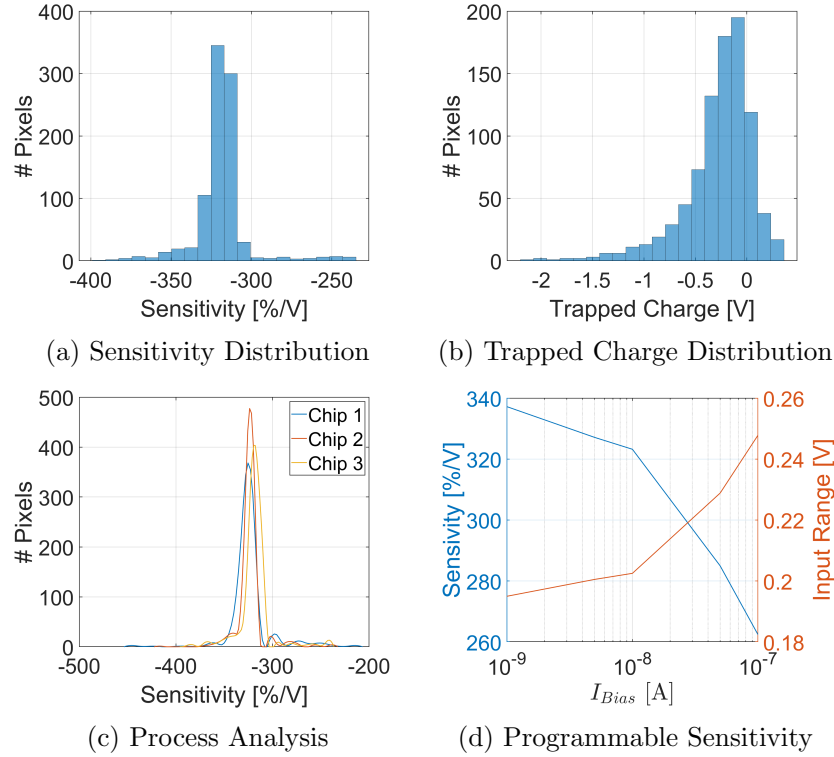


Figure 3.17: Characterization Analysis obtained from pixel characterisation curves, extracting (a) Sensitivity distribution across the array, (b) Trapped Charge distribution and (c) Sensitivity distribution for 3 different chips. Figure (d) shows the programmability of this architecture and the associated trade-off between input range and sensitivity [31] (© 2020 IEEE)

potential, assessing this attenuation. As V_{DAC} directly modifies the potential at the gate, this response can be regarded as the characterisation curve in the absence of capacitive attenuation. Hence, the capacitive attenuation value can be obtained by calculating the ratio between these sensitivities.

For this experiment, a sweep across V_{DAC} range was performed while maintaining the reference electrode potential constant, and each pixel's response was recorded. These results were compared with the characterisation curves of each pixel, obtained following the same experimental setup and analysis presented in the Characteristic Response Analysis. The ratio between the two slopes was calculated for each pixel, obtaining the attenuation distribution presented in Figure 3.18a with a mean of 0.4819 and a standard deviation of 0.0159.

pH Sensitivity

The pH sensitivity of the native CMOS passivation layer, Si_3N_4 , was verified by sequentially flowing different pH buffers over the surface of the chip. After each step, a pH 7 solution was inserted to provide a reference to measure differences between buffers. The influence of

the monotonic drift was regarded as linear for the experiment duration, allowing its removal through linear interpolation.

Figure 3.18b presents the response to the pH changes. Any pH variation triggered a modification of the floating gate potential of the ISFET, leading to a duty cycle change at the output following the electrical sensitivity obtained on the Characteristic Response Analysis. Using this result, the pH sensitivity was calculated using Eq. 3.23.

$$S_{pH} = \frac{\Delta\%}{\Delta pH} \cdot \frac{1}{S_{Elect}} \quad (3.23)$$

The obtained data yielded a pH sensitivity $S_{pH} = 11.8mV/pH$, a sensitivity value aligned with previously reported CMOS-based ISFET architectures [19, 25]. Considering this pH sensitivity and an expected pH step between 0.5 and 2.2 pH units [19, 25] on LAMP DNA amplification, the dynamic range reported is suitable for monitoring on-chip DNA reactions.

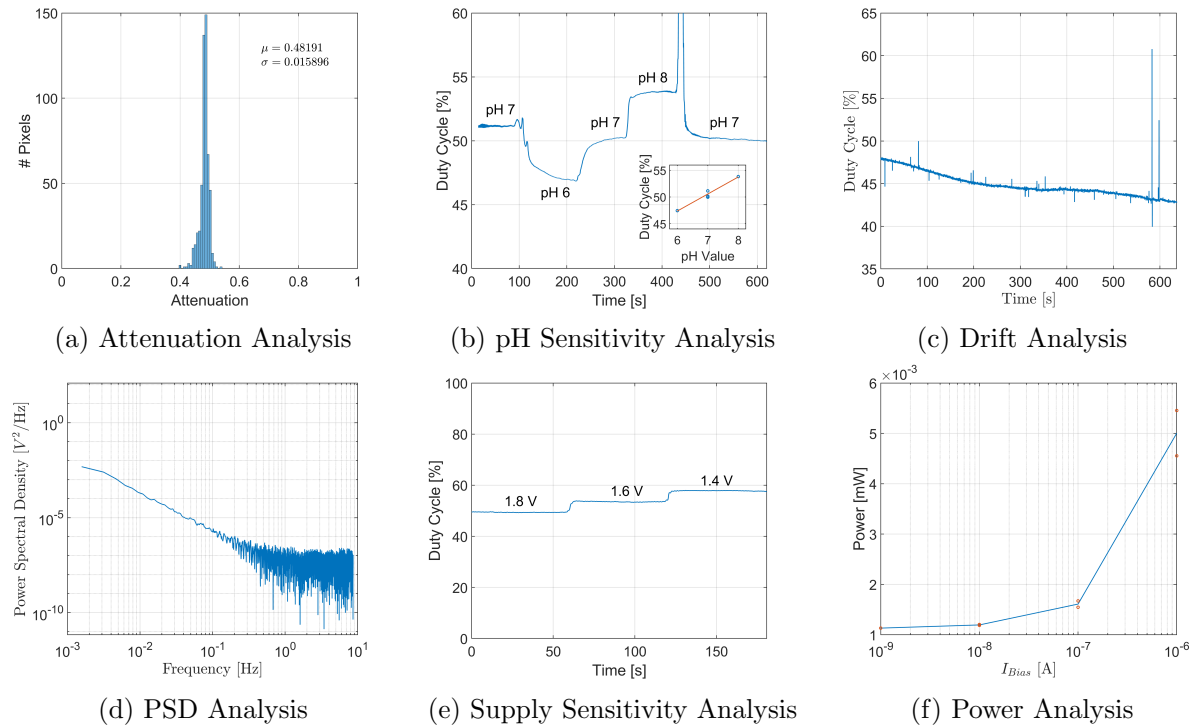


Figure 3.18: Chemical Sensor Characterization [31] ((© 2020 IEEE)

Chemical Drift & Noise Analysis

The native CMOS passivation, Si_3N_4 , undergoes a hydration process when immersed in a solution, creating a hydrated SiO_2 layer which modifies the insulator capacitance value [24].

This variation at the superficial layer is reflected at the output as a slow and monotonic drift following a negative exponential trend [23].

The drift present in the system was characterised by exposing the array to a pH 7 buffer and monitoring the output evolution. One single chemical pixel was calibrated to maximise sampling rate and monitored for 10 minutes, obtaining the monotonic drift presented in Figure 3.18c. From this curve and the sensitivity results obtained on the Characteristic Response Analysis, a drift rate of 3.8 mV/min was calculated.

Using this drift measurement, the pH resolution of the architecture was estimated by calculating its Power Spectral Density (PSD), presented in Figure 3.18d, and integrating it over the frequency range of interest, which for DNA amplifications is established between 10 mHz and 8 Hz [16, 25]. Following this criterion, a pH resolution of 0.1105 pH was obtained. This pH resolution value indicates the suitability of this architecture for LAMP DNA amplification detection, considering reported pH changes on LAMP reactions range between 0.5 and 2.2 pH steps [19, 25]

Two phenomena bound this pH resolution: Firstly, due to the slow time constant of pH changes and DNA amplification reactions, the chemical information spectral bandwidth overlaps with flicker noise, preventing post-processing filtering. Secondly, this chemical flicker noise has been demonstrated to be at least one order of magnitude higher than the MOSFET counterpart [34], limiting pH resolution.

Variable Supply Operation

Over the last few years, ISFET arrays have been integrated into portable [35] and wearable [36] platforms. These platforms were powered by batteries or power harvesting techniques, requiring architectures to operate at scenarios where power budget and supply levels are vital factors.

To assess the architecture suitability to different supply levels, the operation of the architecture under three supply voltages - 1.4V, 1.6V & 1.8V - was evaluated. During the experiment, the pixel was calibrated, and the output duty cycle was monitored for 3 minutes while maintaining V_{DAC} and I_{Bias} at a constant value through external power sources. Every minute, the supply voltage value was decreased by 0.2V, as presented in Figure 3.18e. The offset generated between the different supply levels was calculated using these results, yielding -21.28 %/V.

Power Consumption

The impact of I_{Bias} on the power consumption was analysed by measuring power measurements under different biasing conditions. Figure 3.18f provides the results of this experiment, where the power consumption followed I_{Bias} trend due to the exponential correlation between the biasing current and the oscillation frequency. For the standard $I_{Bias} = 10nA$ at room temperature, a power consumption of 1.19 mW was obtained.

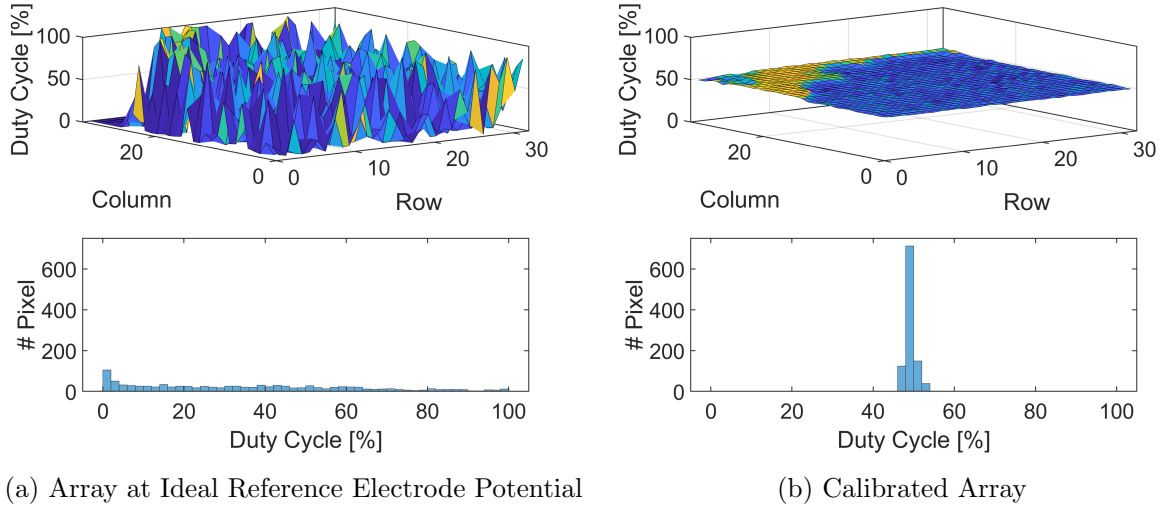


Figure 3.19: Trapped Charge Calibration Results, presenting the raw array output (above) and the subsequent pixel output distribution (below) at different stages of the calibration. Figure (a) presents the array output after the completion of Step 1 of the calibration, while Figure (b) presents the calibrated response of the array [31] (© 2020 IEEE)

Trapped Charge Compensation

Standard CMOS fabrication creates a significant mismatch between pixels across the array due to trapped charge accumulated at the floating gate [37]. This pixel-to-pixel mismatch needs to be compensated to maximise the pixels' dynamic range.

As introduced in Section 3.3.1, the terminal V_{DAC} from the linear OTA can be used for this purpose, compensating for trapped charge on a pixel-by-pixel basis by balancing the input voltages V_{ISFET} and V_{DAC} . For this purpose, a 2-step calibration scheme was developed, detailed in Section 5.3. Figure 3.19 provides an example of the results achieved with this algorithm. This example shows how the first calibration step distributed the pixels uniformly throughout the active dynamic range, while the compensation stage set all pixels at the dynamic range midpoint, with a mean value of 49.97% and a standard deviation of 1.76%. This process yielded 99.5% of active pixels calibrated at the target duty cycle range, homogenising pixel response across the array.

3.3.6 Experimental Results: Temperature Sensor

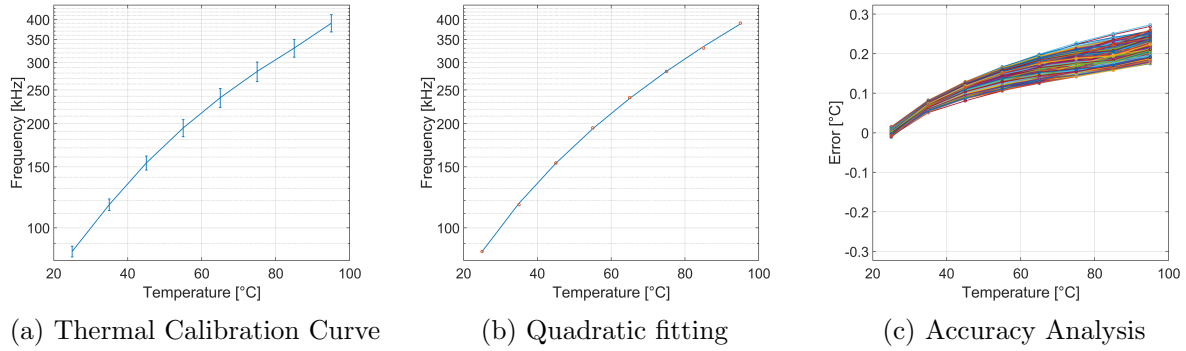


Figure 3.20: Thermal Sensor Characterisation (a) Evolution of pixel frequency with temperature. Curve represents mean frequency value, and error bars represent standard deviation. (b) Quadratic fitting based on mean value of frequency characterisation curves. (c) Pixel-by-pixel accuracy analysis, showing the thermal error between the pixel fitting curve and the sensed frequency [31] (© 2020 IEEE)

Section 3.3.2 presented the equations governing the thermal sensitivity of the architecture. This section presents the results obtained during the pixel characterisation as a frequency-modulated temperature sensor. To assess the sensor performance, the pixel was calibrated to 50%, V_{DAC} was maintained constant, and V_{Bias} was biased through an external voltage source.

In this experiment, the array was exposed to different temperatures, from $25^{\circ}C$ to $95^{\circ}C$ in $10^{\circ}C$ steps, and the PWM signal frequency was measured, generating Figure 3.20. Figure 3.20a presents the characterisation of this sensor, plotting the evolution of the pixel frequency with every increase in temperature, as well as the standard deviation presented across the array. Secondly, the results presented in Figure 3.20b confirmed the quadratic relationship between temperature and frequency described in Section 3.3.2. Performing this quadratic fitting to the data-set, the following transfer function was obtained.

$$f(T) = 18.21 \cdot T^2 + 2140.05 \cdot T + 2041.7 \quad (3.24)$$

Figure 3.20b also includes this fitting, validating the approximation described in Section 3.3.2. To evaluate the sensor's accuracy, a quadratic fitting for each pixel was obtained, and its measurement error was evaluated at each thermal point, as presented in Figure 3.20c. This analysis yields a maximum accuracy of $0.23^{\circ}C$.

Finally, the system's resolution and suitability for LAMP applications were evaluated by sampling the thermal sensor's output for 10 minutes at $63^{\circ}C$, LAMP's reaction temperature. Using this data and the procedure described in the Drift and Noise Analysis, a resolution of $0.9282^{\circ}C$

was obtained. These results confirm the dual-sensing nature of this pixel architecture, achieving both chemical and thermal sensing, and validate the viability of this sensor for monitoring LAMP amplifications, where reactions occur between 60 and 65°C [38]

Table 3.6 provides a summary of the thermo-chemical performance of the system.

Table 3.6: System Performance Summary [31] (© 2020 IEEE)

Parameters ($I_{Bias} = 10nA$)	Spec
Technology	TSMC 0.18 μm M6
System Size	2mm x 1.8mm
Pixel Size	40 μm x 40 μm
Fill Factor	98.4%
Array Size	32x32
Sensing Domain	Ion Concentration \Rightarrow Duty Cycle Temperature \Rightarrow Frequency
Supply Voltage	1.8V
Pixel Performance	
Chemical Sensor	
E. Sensitivity	321.65 %/V
Linear Range	0.2025 V
Linearity [R^2]	0.9986
Attenuation	0.4819
pH Sensitivity	11.8 mV/pH
pH Resolution	0.1105 pH
% Calibrated pixels	99.5%
System Power Consumption	1.19 mW
Thermal Sensor	
Center Frequency	85.45 kHz
Thermal Sensitivity (@ 35 °C)	3.41 kHz/°C
Resolution	0.9282°C
Accuracy	0.273°C

3.3.7 Experimental Results: Thermo-Chemical Cross-Sensitivity

As both thermal and chemical sensing information are encoded into the same signal and sense the same spatial point, cross-sensitivities are likely to affect the measurement, becoming a critical element to account for to separate both sensing modalities. For this purpose, the cross-sensitivity of both sensors were analysed individually in detail.

Chemical influence on thermal sensing

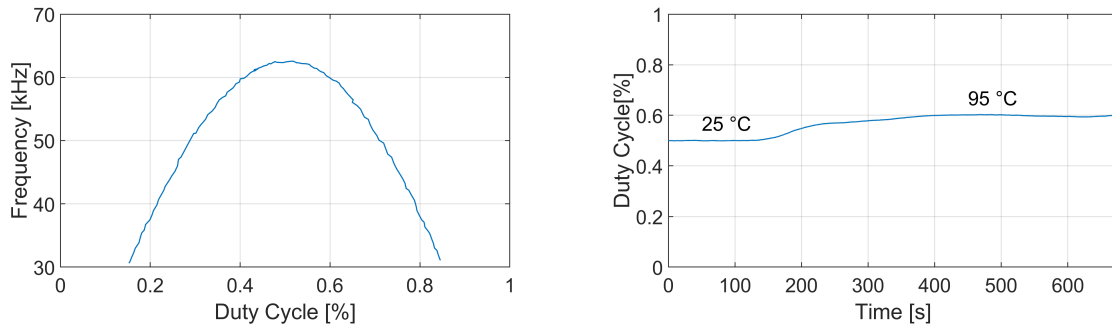
The effect of chemical variations on the thermal output was analysed by sweeping the reference electrode over the chemical input range at a constant room temperature, monitoring the PWM frequency. Figure 3.21a presents the result of this analysis, showing a parabolic sensitivity to chemical variations.

The nature of this cross-sensitivity is associated with the non-ideal switching between phases. This non-ideal switching creates large current transients when the oscillator changes phases, leading to an irregular charging of the capacitor whose effect becomes increasingly significant at higher frequencies.

Thermal influence on chemical sensing

To understand the effect of temperature on chemical sensing, a single-pixel response was monitored for 10 minutes while the temperature varies from 25°C to 95°C. The biasing current I_{Bias} required for the pixel operation was established using the Keithley 2602 as a current source to remove changes in sensitivity due to variations in biasing current. The temperature control was performed using a thermocycler.

Figure 3.21b presents the result of this experiment, obtaining a thermal sensitivity of 0.0363 pH/°C. The promise of thermal insensitivity of this differential architecture, proposed in [7–9], can only be fulfilled when the OTA's differential input voltage is balanced. Simulations demonstrated that this equilibrium point, which on standard linear OTAs would be at 50%, presents an offset and varies from pixel to pixel due to mismatches on the passivation capacitance C_{Pass} and trapped charge. Hence, pixel-by-pixel calibration at different temperatures would be required, and even then, a variation on sensitivities due to changes in biasing current would disrupt the measurement.



(a) Chemical influence on thermal measurements (b) Thermal influence on chemical measurements

Figure 3.21: Cross-Sensitivity Analysis. Figure (a) presents the evolution of the frequency of the PWM signal with variations on the chemically modulated duty cycle. Figure (b) present the thermal sensitivity of the chemical signal through a transient analysis

Cross-Sensitivity Discussion

The cross-sensitivity analysis indicates that, despite the dual-sensing capabilities, simultaneous sensing of thermal and chemical information is impossible without additional compensation techniques to ensure cross-sensitivities are reduced to the minimum. A solution addressing this need is later described in Section 5.5.

Alternatively, both sensors can be operated separately on different sensing phases: if the array acts as a thermal controller, the pixels' duty cycle should be locked to 50%, minimising distortion. When the array expects chemical information to be acquired, each pixel would be biased

with the trapped charge calibration values.

3.3.8 Experimental Results: On-Chip LAMP DNA Amplification and Detection

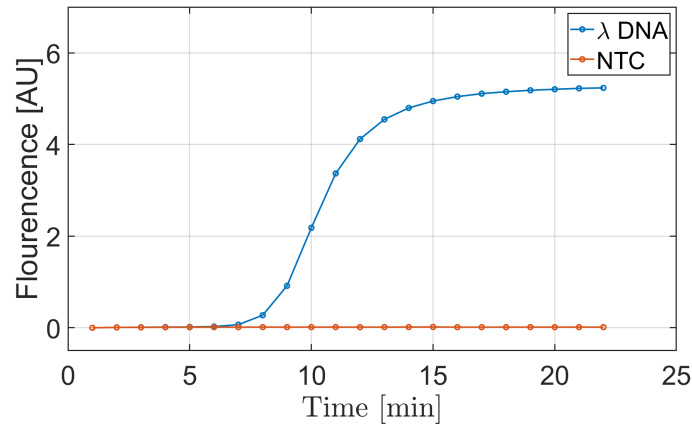
This section demonstrates the feasibility of the Lab-on-Chip platform comprising the dual-sensing ISFET array for real-time DNA amplification and detection using LAMP. An acrylic manifold was placed on top of the ISFET array for this experiment, creating a reaction chamber where the LAMP reaction will occur. LAMP DNA amplification occurs at constant temperature (typically 63 °C) and requires 4 to 6 primers for amplification to occur, achieving high amplification speed (< 20 min) and high amplification efficiency producing around $> 10^9$ copies of the targeted DNA fragment at the end of the reaction[39].

DNA isolated from bacteriophage lambda (#N3011S, New England BioLabs) was diluted to a final concentration of $1 \cdot 10^6$ copies per reaction and used as the target for DNA amplification. LAMP primers for specific detection of phage lambda DNA were used as described in [40]. Real-time DNA amplification experiments were performed in parallel in a commercial qPCR instrument (LightCycler 96, Roche Instruments) and on the Lab-on-Chip platform (LoC).

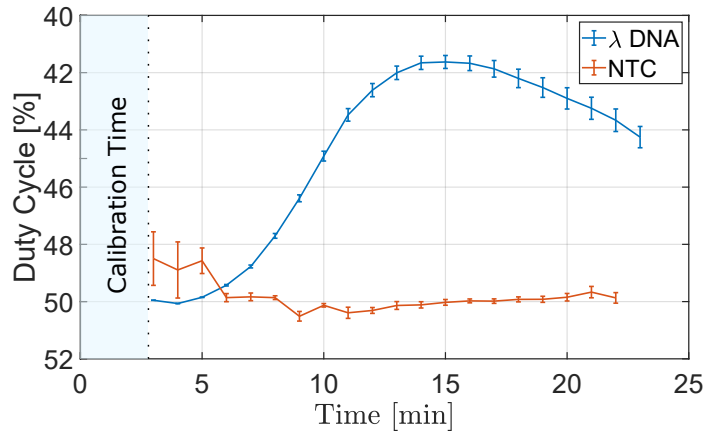
Fig. 3.22 presents the results of both the Lab-on-a-Chip platform and the benchmark instrument, where a non-template control (NTC) and a positive reaction were included as the sample set. Fig. 3.22b shows the results obtained with the LoC platform. By the end of the experiment, the solution pH decreased by 2.16 pH units due to the proton release during DNA amplification. The reaction time-to-positive (TTP) was calculated using a threshold of 1.5% duty cycle change after monotonic drift removal. Using this method, the estimated time-to-positive (TTP) was 7.71 ± 1.47 min. Decay after minute 15 is associated to the variation of drift due to the pH change. The same reactions were carried out in a conventional qPCR instrument, and the results are presented in Fig. 3.22a where the y-axis corresponds to fluorescence (AU) and the x-axis to time. The obtained average TTP was 7.76 ± 0.40 min. The TTP of the reaction on the qPCR instrument was calculated using the cycle-threshold method, C_t [41], setting a threshold at 0.2 of normalised output data.

3.3.9 Final Remarks

In this section, a dual-sensing 32x32 ISFET array capable of detecting on-chip DNA amplification reactions has been presented. The pixel senses both ion activity and temperature, encoding them into the duty cycle and the frequency of the output PWM signal, respectively. This dual-sensing architecture eliminates the need for extra on-chip temperature pixels, enhancing spatial



(a) Amplification curve of synthetic lambda DNA at 10^6 copies per reaction carried-out in a commercial qPCR instrument. A non-template control (NTC) was included



(b) Amplification curve of synthetic lambda DNA at 10^6 copies per reaction carried-out in the Lab-on-Chip platform. A non-template control (NTC) was also included. Curve represents mean pixel value, and error bars represent standard error.

Figure 3.22: Lambda DNA amplification and detection on a commercial qPCR instrument and on the Lab-on-Chip platform [31] (© 2020 IEEE)

resolution. Furthermore, the pixel architecture, composed by a linear OTA connected to a 2-stage sawtooth oscillator, leverages on a differential approach to achieve resilience to process variations and is capable of operating at different voltage supplies, becoming a suitable candidate for low power applications, such as battery-powered or power-harvested portable platforms. The system presents several degrees of programmability, enabling the modification of the sensor characteristic response and operation point to compensate for ISFET non-idealities. To demonstrate this programmability, pixel-to-pixel mismatches due to trapped charge were corrected using the programmable terminals, achieving a homogeneous response across the array.

Table 3.7 provides a comparison with the state-of-the-art. This pixel architecture is the first

example of dual thermo-chemical sensing in a single pixel, presenting good robustness and programmability while maintaining a compact form factor and pH resolution. The presented pixel programmability and versatility can be key to mitigating further ISFET non-idealities such as drift, eliminating the monotonic output change in real-time, and facilitating the early detection of both pH changes and DNA on-chip amplification reactions.

Table 3.7: State-of-the-art Performance Comparison - ISFET Arrays [31] (© 2020 IEEE)

Parameters	This Work	[42]	[25]	[19][15]	[43]	[44]
Sensing Domain	Duty Cycle	Time	Time	Current	Voltage	Voltage
Process	180nm	180nm	350nm	350nm	180nm	350nm
Supply Voltage	1.8 V	1.8 V	3.3 V	3.3 V	3.3 V	3.3 V
Pixel Size	40 x 40 μm^2	26 x 26 μm^2	37 x 31 μm^2	6.5 x 7.8 μm^2	10 x 10 μm^2	50 x 50 μm^2
Array Size	32x32	32x32	78x56	64x200	64x64	8x8
pH Sensitivity	11.8 mV/pH	30mV/pH	11.74 mV/pH	24.1 mV/pH	26.2 mV/pH	57mV/pH ‡
pH Resolution	0.1105 pH	0.013 pH	0.017 pH	0.101 pH	-	-
% Calibrated pixels	99.5%	100%	95%	-	-	100%
Power Consumption	1.19 mW	11.286 mW	7.5 mW	150 μW	105.6 mW	-
Multi-Sensing	✓ Ion & Temperature	✗	✓ †	✗	✓ Ion & Light	✓ Ion & Light
Operated at Variable Supply	✓	✗	✗	✗	✗	✗
Programmable	✓	✗	✓	✓	✗	✓

† Ion & Temperature are separate pixels

‡ Gain of 10

3.4 Future Perspectives on Oscillator-Based ISFET Architectures

The dual-sensing ISFET architecture presented in Section 3.3 highlights the benefits that oscillators provide for novel ISFET architectures, with a focus on two aspects:

- **Multi-sensing, highly programmable architectures:** PWM encoding enabled by oscillator-based architectures provides multi-sensing applications with the ideal channel for single-wire modulation. Furthermore, programmability can be integrated at the sensing level without overhead, providing pixel adaptability as discussed later in Section 5.
- **Low Power Consumption through Reduced Power Supply:** Oscillator-based architectures can trade frame rate for power consumption by reducing the supply voltage, as discussed in Section 3.2.5.

This section presents two different architectures that address these opportunities.

3.4.1 Ultra-Low Power ISFET Pixel Architecture

The recent integration of ISFET sensors as part of portable diagnostic platforms [35, 45, 46] and wearable devices [47] is reviving the interest in low-power architectures that can be scaled

to large arrays and operate with minimal supplies for long periods of time.

In previous sections, oscillator-based architectures were functionally validated under various supply voltages. However, as highlighted by De Smedt et al. [29], sawtooth oscillators based on time-domain modulation suffer from noise degradation when scaling to smaller process nodes. In order to reap the scaling benefits in terms of power, ISFET-based architectures need to reduce the total pixel area occupied by analogue components [48, 49].

This section proposes a highly digital Ion-to-Frequency ISFET architecture to overcome these limitations, using a sensing scheme that transforms the chemical measurement into a frequency-encoded signal. Leveraging weak inversion operation and a reduced voltage supply, this architecture minimises the pixel's power consumption while achieving exponential sensitivity.

Pixel Architecture and Operation

The proposed pixel architecture, illustrated in Figure 3.23, comprises a capacitor, two sets of inverters, a NAND SR latch and an ISFET. Oscillator initial conditions and sensor control is achieved through the "Enable" signal, controlling both SR latch input and tri-state buffers.

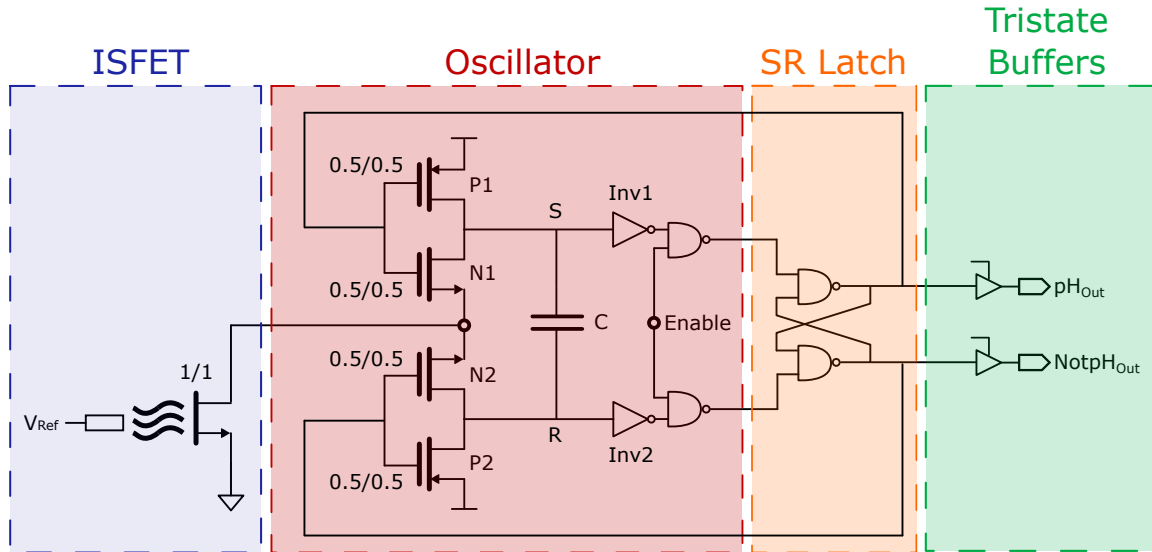


Figure 3.23: Ultra Low Power Pixel Architecture [50] (© 2020 IEEE)

The operation of this architecture can be divided into 4 phases, as illustrated in Figure 3.24:

- **Phase 1** ($pH_{Out} = 0$; $R > V_{th_{Inv2}}$): The node S is forced to V_{DD} , and the charge accumulated in the R node discharges through N2 at a rate set by the ISFET's current.
- **Phase 2** ($pH_{Out} = 0$; $R \leq V_{th_{Inv2}}$): When the potential at R crosses the inverter's switching point, the SR latch inverts the pH_{Out} value to 0 to 1.

- **Phase 3** ($pH_{Out} = 1$; $S > V_{th_{Inv1}}$): The node R is forced to V_{DD} , and the charge accumulated in the S node discharges through N1 at a rate set by the ISFET's current.
- **Phase 4** ($pH_{Out} = 1$; $S \leq V_{th_{Inv1}}$): When the potential at S crosses the inverter's switching point, the SR latch inverts the pH_{Out} value, completing a full oscillatory cycle.

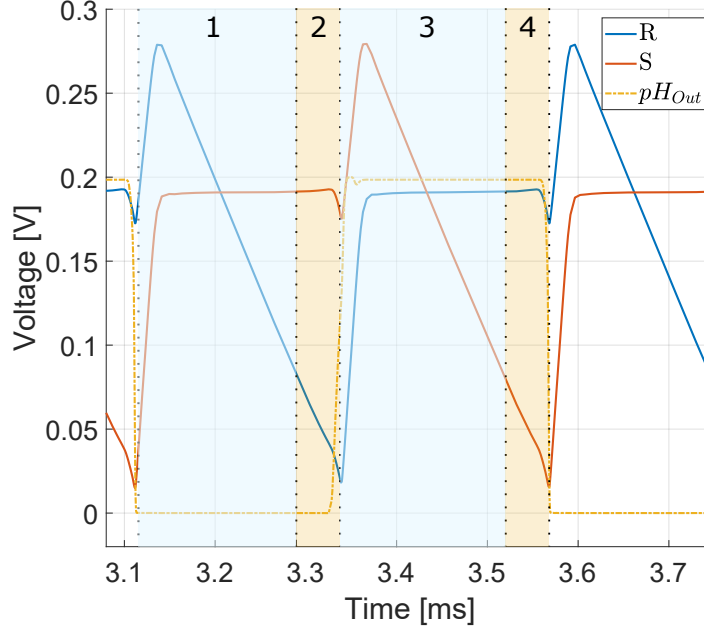


Figure 3.24: Ultra Low Power Pixel Transient Signals, with the different phases highlighted [50] (© 2020 IEEE)

The pixel parameters determine the frequency of the generated output signal $V_{ph_{Out}} [f_{pH}]$ as follows:

$$f_{pH} = f_{pH_7} + G \cdot \Delta f_{pH} \quad (3.25)$$

$$f_{pH} \propto \frac{1}{V_{th_{Inv}} \cdot C} \cdot (I_{ISFET_{pH_7}} + \Delta I_{ISFET_{pH}}) \quad (3.26)$$

being $V_{th_{Inv}}$ the inverter's threshold voltage, C the capacitance value and I_{ISFET} the ISFET current, which defines the centre frequency f_{pH_7} and the modulation component Δf_{pH} with sensitivity G .

The ISFET is biased in weak inversion, an operating region where the charge carrier dynamics in the channel are controlled by diffusion instead of drift due to the low $V_{g's}$ compared with V_{th} [22]. By operating the ISFET in this region, the power consumption and the oscillation frequency can be minimised thanks to the low current operation while maximising the sensor's

sensitivity to small chemical changes thanks to the higher transconductance to current ratio. Using the MOS weak inversion model, I_{ISFET} is defined as:

$$I_{ISFET} = I_0 \cdot \exp\left(\frac{V_{g''s}}{n \cdot U_t}\right) \cdot \left[1 - \exp\frac{-V_{ds}}{U_t}\right] \quad (3.27)$$

Using ISFET's V_{Chem} relationship with pH (Eq. 2.2) and assuming $V_{g''s} \propto V_{Chem}$, and considering that V_{ds} is always pre-charged to $V_{dd} - V_{ds_{NX}}$ and independent to V_{Chem} , I_{ISFET} can be simplified to Eq. 3.28 [25]. Merging Eq. 3.26 and 3.28, it can be derived that the frequency f_{pH} is modulated through I_{ISFET} .

$$I_{ISFET} \propto I_0 \exp\left(\frac{\alpha S_N pH}{n U_t}\right) \quad (3.28)$$

$$f_{pH} \propto \frac{I_0}{V_{th_{Inv}} \cdot C} \cdot \exp\left(\frac{\alpha S_N (pH_7 + \Delta pH)}{n U_t}\right) \quad (3.29)$$

The validity of this exponential relationship is verified now by simulation.

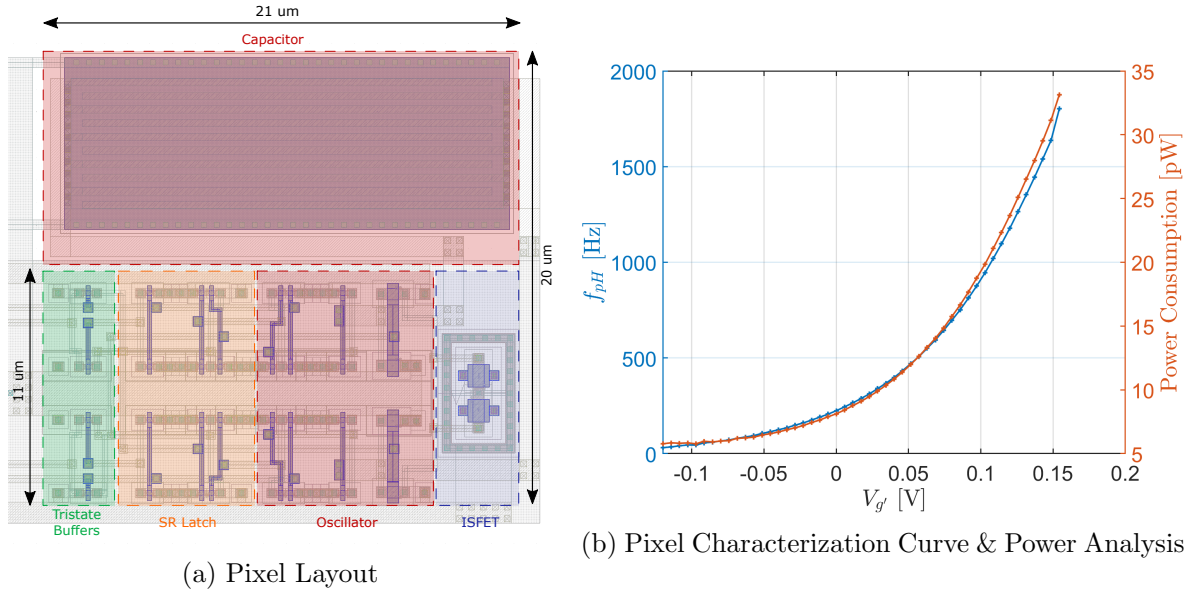


Figure 3.25: Ultra Low Power Architecture - Pixel Analysis [50] (© 2020 IEEE)

Pixel Performance and Discussion

The presented pixel was designed for fabrication in standard CMOS TSMC 180nm process, and Fig. 3.25a presents its layout. The design considerations and pixel performance are now

analysed in detail. Throughout this analysis, a pH sensitivity of 30mV/pH is used for simulation purposes.

Sensitivity & Modulation Range Analysis The pixel sensitivity proposed in Eq. 3.29 was confirmed by Fig. 3.25b, following the exponential curve determined by the weak inversion region. This biasing region I_{ISFET} is typically in the order of nano-amps, pushing the centre frequency $[f_{pH7}]$ towards low frequencies and hence reducing the oscillator carrier power. Additionally, this region provides a large transconductance to current ratio, enhancing its sensitivity to 286.58 Hz/pH at $f_{pH7} = 697Hz$.

The maximum modulation range was determined by $P1$ & $P2$, which controls the charging speed of nodes S & R, respectively. These transistors were appropriately sized to achieve an input range of 9.15 pH units, a range suitable for our target applications.

Power Consumption The proposed pixel architecture was simulated with a 0.2V supply to minimise the power consumption, obtaining the performance presented in Fig. 3.25b. Based on this simulation, the expected maximum power consumption was 33pW.

Area Considerations The pixel occupied $20 \times 21 \text{ } \mu m^2$, using minimal area while maintaining a suitable input range and oscillation frequency. The pixel's active area covered only $11 \times 21 \text{ } \mu m^2$, avoiding the capacitor area to prevent oscillatory coupling to the floating gate [17]. The form factor of this pixel is limited by the Metal-Insulator-Metal capacitor, whose value is critical for achieving good OSR, establishing its center frequency f_{pH7} , but also affects the maximum chemical sensing area. Hence, a critical area trade-off of this pixel is between OSR and pixel size, and in this case I prioritised pixel size as critical due to its importance in highly dense ISFET arrays, where power improvements are more urgent.

Noise Performance The resolution of the architecture was evaluated to assess its minimum detectable pH. This analysis was performed by running a transient noise analysis and extracting the Power Spectral Density (PSD). By integrating the obtained PSD between the frequency of interest, which has been regarded between 10 mHz and 8Hz [16], a resolution of 0.0119 pH was obtained assuming a pH sensitivity of 30 mV/pH. This result should be regarded as the lower bound for the noise performance of this architecture, as the chemical noise is likely to still be dominant over electrical noise [51].

Discussion The analysed architecture represents the lowest reported power consumption per pixel, to the best of my knowledge. By adopting both weak inversion operation and low sup-

plies, this architecture reduces the current flowing through the pixel while maintaining a large transconductance-to-current ratio, enhancing the sensitivity. The reduced power requirements of the ISFET sensor and its scalability to deep sub-micron technologies makes this architecture a suitable candidate for applications with strict power budget such as power harvesting platforms [47], opening a new horizon for portable and wearable ISFET-based devices. These benefits come at the expense of a reduced sampling rate due to slow oscillation, a minor limitation considering the slow nature of chemical reactions.

3.4.2 Quad-Sensing ISFET Array: Simultaneous Sensing of Ions, Temperature, Fluid Presence and Light ¹

The integration of ISFET ion imaging arrays as part of portable diagnostic platforms for infectious diseases has broadened the range of conditions at which an ISFET pixel needs to operate. The importance of these external conditions has been already described in the literature, such as drift [23, 52] and light [53], and has been mitigated through computationally expensive processing and Machine Learning (ML) models that reconstruct the sensing information. Simultaneously sensing these external effects would provide the means to further understand surface interactions under a various range of conditions, provide the means for empirical verification of analytical models and achieve pixel-level adaptability required to enhance its resilience to external conditions, as illustrated in previous research on in-pixel thermo-chemical [54], optochemical [43], and most recently opto-thermo-chemical sensing [55].

The inclusion of additional sensors at the pixel level would enable novel applications. Firstly, distinguishing the exact location of a reacting primer using both pH and light would lead to faster reaction detection, reducing both Time-to-Positive (TTP) while avoiding cross-sensitivity errors between pH and light, as described in Section 5.5 and illustrated in Hsu et al [53]. Additionally, simultaneous light and ion detection would enable primer multiplexing on-chip, facilitating the detection of various pathogens on a single PCR/LAMP amplification through differences in both fluorescence and pH, using ML models already validated in light-based dPCR [56].

With these promising applications in mind, oscillator-based ISFET architectures provide a perfect opportunity to explore this multi-sensing approach. This section presents a multi-sensing pixel capable of sensing ion concentration, temperature, fluid presence, and light from the same spatial point. This pixel is composed of Section 3.3 dual-sensing ISFET architecture integrated with a photodiode and a novel fluid detection sensor, all implemented in a compact pixel. All sensing modalities are acquired simultaneously and modulated onto a single waveform us-

¹The circuit and simulations presented in this section were designed and performed by Qirui Hua under the direct supervision of Miguel Cacho Soblechero.

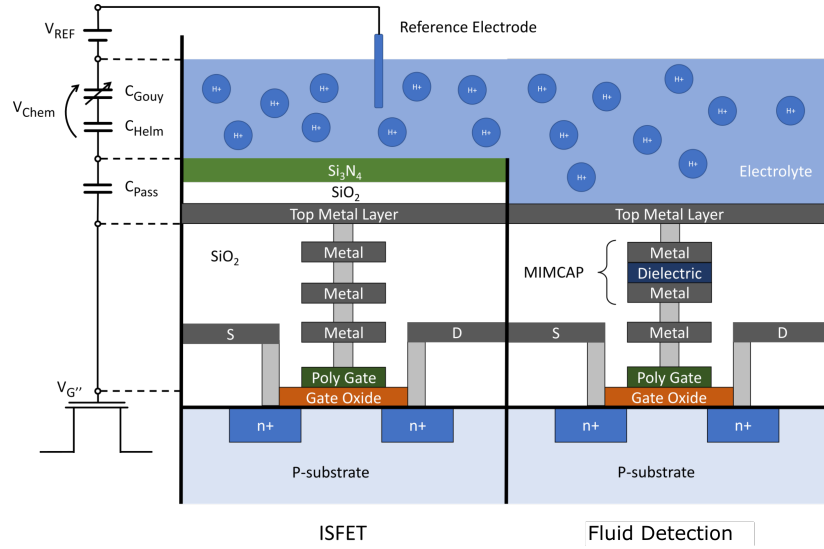


Figure 3.26: Sensing elements cross-section showing standard CMOS ISFET (left) and fluid detection sensor (right) [57] (© 2021 IEEE)

ing multi-frequency PWM modulation, overcoming the associated transmission overhead while preserving pixel programmability for non-idealities compensation. Moreover, dark current influence is mitigated through a reference photodiode, further reducing the pixel light resolution. The following section provides an initial analysis of this architecture, both from the functional and the performance perspectives.

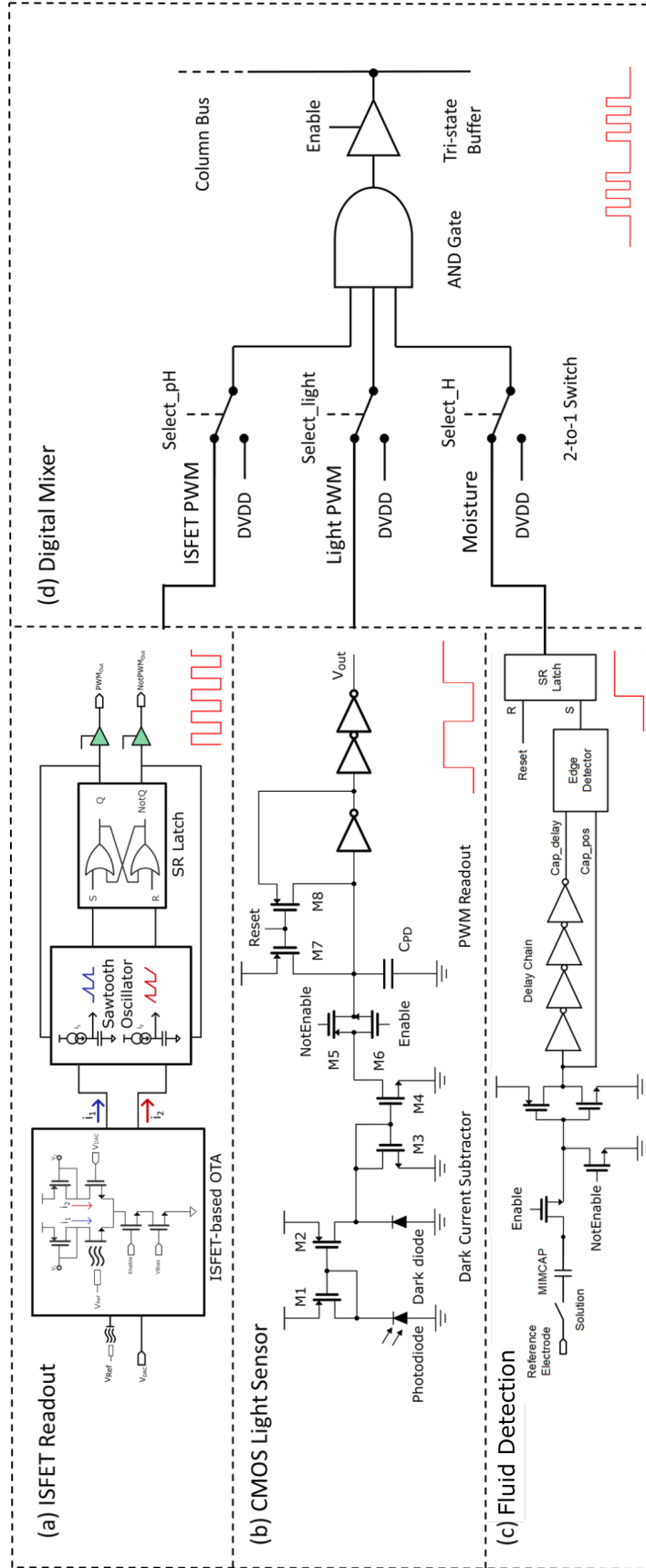


Figure 3.27: Quad-Sensing Pixel Architecture, composed by (a) a Dual Mode Thermal-Chemical ISFET Readout, (b) a CMOS Light Sensor, (c) a Fluid Detection Sensor, (d) a Digital Mixer [57] (© 2021 IEEE)

Pixel Architecture and Operation

The proposed pixel, named quad-sensing pixel, is composed of 4 sensing modalities modulated simultaneously on a single waveform. Figure 3.26 illustrates the physical architecture of these sensors, and Figure 3.27 presents the quad-sensing pixel architecture. The exact functionality of each modality is now described in detail.

Thermo-Chemical Sensing The thermo-chemical sensing structure is identical to the one presented in Section 3.3.

Light Sensing A photodiode is integrated to measure the incident light at the individual pixel. The sensed light is encoded into a PWM signal, modulating the light intensity in time and facilitating simultaneous multi-signal modulation on a single wire.

This PWM modulation is achieved by controlling the pixel's capacitor discharge rate through the sensed photocurrent I_f [58], as illustrated in 3.27(b). The time required for the capacitor voltage to drop below the inverter's threshold voltage V_{th} , defined as τ_{off} , determines the PWM duty cycle interval:

$$\tau_{off} = (V_{int,0} - V_{th}) \cdot \frac{C_{PD}}{I_f} \quad (3.30)$$

The maximum discharging time (τ_{tot}) controls the dynamic range. This τ_{tot} is programmable through an off-pixel reset signal. As all generated PWM signals are modulated and transmitted over a single wire, both the maximum discharging time (τ_{tot}) and the time constant (τ_{off}) are sized to avoid overlap between the light sensor PWM frequency spectrum and the thermal oscillation frequency, achieving minimal cross-sensitivity during modulation. This spectrum separation is achieved by appropriate capacitor C_{PD} sizing, implemented using MOS-Cap for better area-efficiency, and using an n-well/p-sub type photodiode to optimise sensitivity and SNR [59].

Under low lighting conditions, photodiodes produce dark current due to thermal excitation [60], limiting its resolution. This phenomenon is especially significant under high temperatures due to the thermal dependency of dark current intensity. As this multi-sensing platform needs to operate under a wide range of temperatures, dark current compensation must ensure high light resolution and minimal optothermal cross-sensitivity. For this purpose, a differential current subtractor is introduced to remove the temperature-sensitive current, as shown in Fig. 3.27(b). This compensation mechanism assumes that the reference photodiode and light sensor would present similar dark current, subtracting them in the current domain [61].

Fluid Detection Sensor Solution leakage between wells remains one of the main issues at Lab-on-a-Chip platforms, but the lack of real-time leakage monitoring through the device is preventing its analysis. Currently, leakage is assessed by sweeping the reference electrode potential and measuring the responding pixels, a process that disrupts both drift tendency and the ongoing reaction and makes it suitable for initial and final validation, preventing real-time monitoring. Real-time monitoring of leakage conditions would help assess the different microfluidic solutions and inform the system of potential leakage during the reaction.

For this purpose, a novel sensing scheme is proposed, presented in Fig.3.26. This structure, created by removing the Si_3N_4 passivation layer and exposing the top metal connection, measures either the presence or absence of fluid by evaluating the direct connection between the Ag/AgCl reference electrode and the top metal layer. If the sensor is in contact with a solution, the potential at the reference electrode would couple to the floating node at the inverter's gate, triggering the inverter's output value. If no fluid is present, no coupling will occur, and the inverter's value would remain unchanged. Fig.3.27(c) presents the fluid detection readout circuitry that achieves this functionality, where the solution is illustrated as a switch.

If the reference electrode potential moves to ranges unsuitable for this technology, the gate voltage can couple and potentially damage the floating node. To avoid this situation and protect the readout, a metal-insulator-metal capacitor (MIMCAP) is inserted between the top metal layer and the floating node at the inverter's gate. This capacitor couples the reference electrode signal to the inverter node while active, while protecting this node from excessive voltages (beyond the range 0-1.8V of the technology) during inactivity periods. This protection is achieved by fixing the inverter node and the lower cap plane to a fixed voltage, mitigating the effect of the reference electrode at the inverter node.

Digital Mixer The signals generated by each sensor are modulated onto a quad-sensing PWM signal by a digital mixer for transmission and subsequent analysis [62]. Thanks to the careful design of non-overlapping frequency ranges, both light and thermal information can be modulated onto a single waveform with minimal cross-sensitivity. Using this scheme, the fast pulses from the thermo-chemical sensor sample the slow pulses from the light sensor, as shown in Fig.3.27(d), creating two overlapping signals. In this context, the fluid presence signal is treated as an enable logic signal, allowing the modulation only when fluid is in contact with the pixel. External commands can override all these modulation signals for debugging purposes.

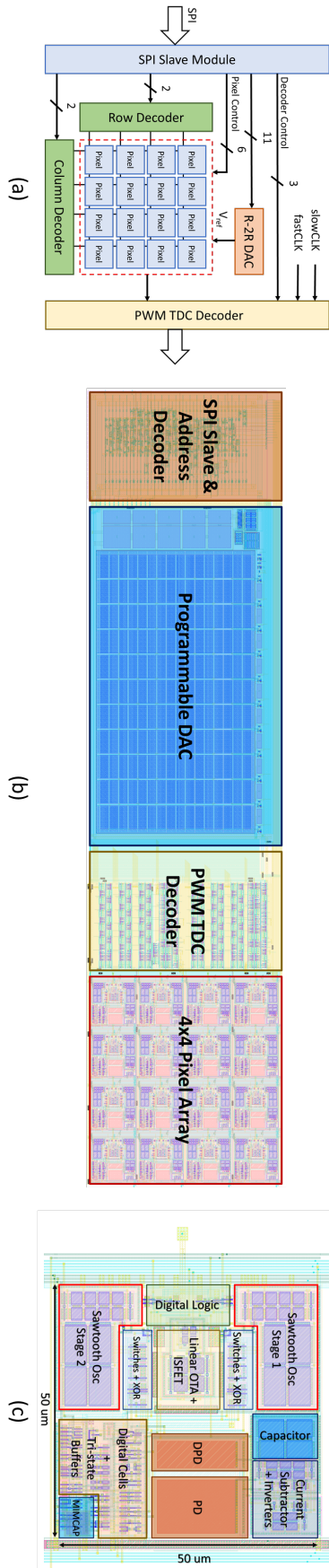


Figure 3.28: Quad-Sensing System Architecture (a) Overall system architecture, (b) System layout, (c) Pixel layout [57] (© 2021 IEEE)

System Architecture

The multi-sensing platform is composed of four blocks, which are listed as follows:

- **4x4 Multi-sensing Pixel Array:** A 4x4 array of multi-sensing pixels was implemented. Each pixel occupies $50 \times 50 \mu m^2$, integrating all four modalities. All pixels share the same output bus, enabling only one transmission at a time.
- **PWM TDC Decoder:** A counter-based TDC decoder converts the PWM signals into digital code.
- **SPI Interface and Row/Column Decoder:** The slave SPI translates the off-chip control signals into digital bits for the system operation. Based on the address message from the SPI interface, the row/column decoder enables one single pixel in the array.
- **Programmable R-2R DAC:** Controlled through SPI, the DAC generates the compensating voltage for ISFET trapped charge compensation.

The overall system architecture is described in Fig. 3.28(a) with the layout of the system and individual pixel presented in Fig. 3.28(b) and Fig. 3.28(c)

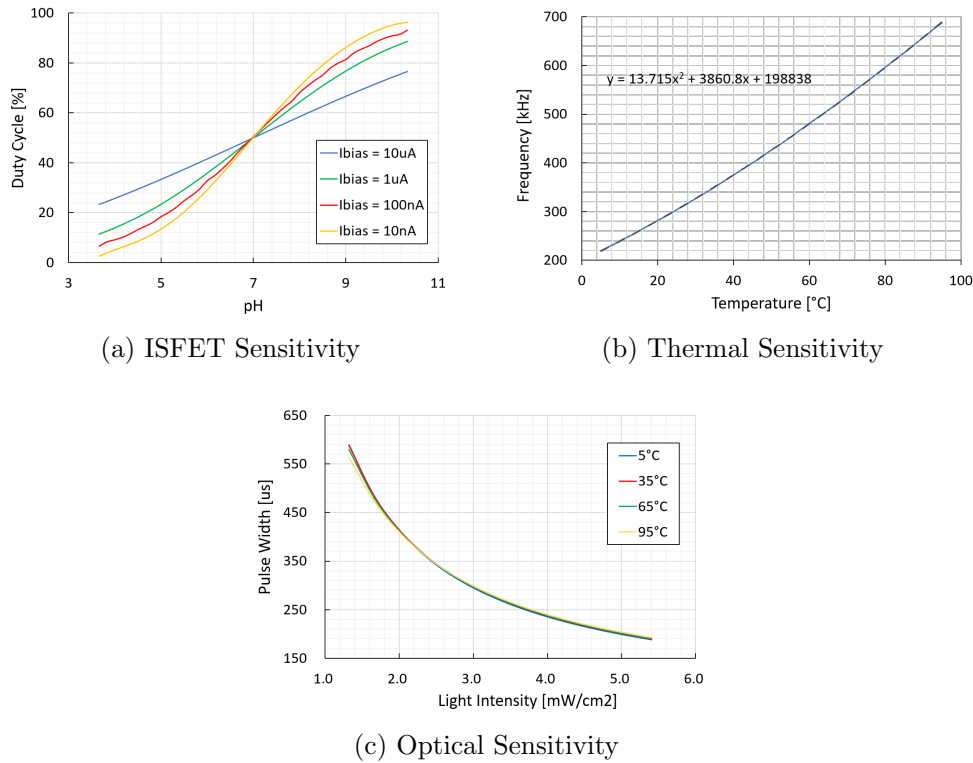


Figure 3.29: Sensitivity Simulation Results [57] (© 2021 IEEE)

System Performance and Discussion

The proposed multi-sensing system was designed in TSMC 180nm CMOS technology, yielding both the system and the pixel layout presented in 3.28(b) and (c), respectively. Assuming the sensitivity of ISFET was 30 mV/pH and the responsibility of the photodiode was 0.378 A/W with a worst-case dark current of 50 pA [59], simulated sensitivity curves of multiple features were obtained as shown in Fig. 3.29, along with an opto-thermal cross-sensitivity analysis.

Table 3.8 summarises the performance achieved. These simulation results indicate that the quad-sensor oscillator-based architecture can modulate all four sensing domains on a single pixel and transmit it through a single wire with minimal cross-sensitivity. Blending programmability and differential sensing, both fabrication mismatch and non-idealities effects can be mitigated, enhancing sensing capabilities on a compact form factor. These sensing capabilities comes at the expense of larger area and higher pixel complexity, hence a single-wire interface is implemented to minimise overhead. The potential benefits provided by this quad-sensing approach would offset the complexity increase, representing a promising step towards sense-aware platforms capable of sensing and adapting to changing external conditions. These benefits will be verified *in-silico* upon fabrication.

Table 3.8: System Performance Summary [57] (© 2021 IEEE)

Parameters ($I_{Bias} = 10nA$)	Spec
Technology	TSMC 0.18 μm M6
System Size	890 μm x 230 μm
Pixel Size	50 μm x 50 μm
Array Size	4x4
Sensing Domain	Ion Concentration \Rightarrow Duty Cycle Temperature \Rightarrow Frequency Light \Rightarrow Time Fluid Detection \Rightarrow Digital
Supply Voltage	1.8V
Power Consumption	26.85 μW
Pixel Performance	
Chemical Sensor	
pH Sensitivity	14.6 %/pH
Linear Range	± 3.39 pH
pH Resolution	0.1105 pH
pH Fill Factor	78.94%
Thermal Sensor	
Thermal Center Frequency	85.45 kHz
Thermal Sensitivity (@ 27 °C)	5.23 kHz/°C
Resolution	0.9282°C
Accuracy	0.273°C
Light Sensor	
Light Center Frequency	1000 Hz
Light Sensitivity	221.6 $\frac{\mu s}{mW \cdot cm^{-2}}$
Light Fill Factor	7 %
Fluid Detection Sensor	
Fluid Detection Sensitivity	Binary Output

3.5 Summary

This chapter introduced the concept of oscillator-based ISFET architectures, leveraging the benefits of frequency and duty cycle encoding to overcome ISFET limitations in scalability, multi-sensing, adaptability to external conditions and low power operation.

As an initial approach to the field, I proposed two ISFET architectures that utilise duty cycle PWM modulation to encode ion information. Fabricated in AMS 350nm process, the Chemically Controlled Ring Oscillator (CCRO) provided a highly digital architecture suitable for deep submicron processes. At the same time, the 8-stage Sawtooth Oscillator enabled several degrees of programmability, providing compensation for trapped charge and adapting both sensitivity and dynamic range to the application requirements.

On the one hand, the 8-stage Sawtooth Oscillator was optimised to a 2-stage oscillator for compactness and fabricated using TSMC 180nm technology as part of a 32x32 array to detect DNA amplification. The various degrees of programmability present in the architecture enabled a tailored operation based on sensing conditions, enhancing its adaptability. This adaptability will be revisited in Chapter 5, where this programmability will be coupled with software methods. Furthermore, the multi-sensing capabilities of this architecture eliminated the need for external sensors to monitor the solution's temperature. The limit of these multi-sensing capabilities was explored by expanding the sensing modalities in-pixel, developing a quad-sensing pixel featuring ion sensing, temperature, light and fluid detection modulated over a single PWM signal. Preliminary simulation results suggested that this multi-sensing integration can be achieved with minimal cross-sensitivity between modalities.

On the other hand, the low power consumption and scalability of CCRO made the architecture attractive for battery-powered applications. Inspired by this concept, a highly digital architecture capable of operating at ultra-low power supplies was simulated. The initial results indicated that this architecture could reduce the power consumption per pixel to the order of pico-Watts.

These architectures illustrate the benefits that oscillator-based architectures provide to ISFET arrays, modulating the target signal in either frequency or duty cycle domains. This modulation schemes enhance front-end flexibility and reconfigurability, making them adaptable to changes in sensing conditions, while providing intrinsic filtering on PWM signals and high suitability for low supplies [3]. This work represents the first stone towards autonomous, asynchronous and adaptable ISFET pixels, which I expect to be a fruitful field in the years to come.

Despite the merits of these architectures, their integration with on-chip computational capabilities is capped by the need for additional memories for storage, post-processing and transmission, and the frame rate does not scale with array size, setting a limit to their spatial scalability.

The next chapter focuses on overcoming these challenges, moving towards the development of a Digital ISFET Sensor.

3.6 Publications

Several publications arose from the content of this chapter.

- [57] Q. Hua, M. Cacho-Soblechero et al. "A Multi-sensing ISFET Array for Simultaneous In-pixel Detection of Light, Temperature, Moisture and Ions" In: *2021 IEEE International Symposium on Circuits and Systems (ISCAS)* (2021), pp. 1–5
- [50] M. Cacho-Soblechero et al. "An Ion-to-Frequency ISFET Architecture for Ultra-Low Power Applications" In: *2020 IEEE International Symposium on Circuits and Systems (ISCAS)* (2020), pp. 1–5
- [31] M. Cacho-Soblechero et al. "A Dual-Sensing Thermo-Chemical ISFET Array for DNA-Based Diagnostics". In: *IEEE Transactions on Biomedical Circuits and Systems* 14.3 (2020), pp. 477–489.
- [16] M. Cacho-Soblechero et al. "Programmable ion-sensing using oscillator-based ISFET architectures". In: *IEEE Sensors Journal* 19.19 (2019), pp. 8563–8575.
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- [64] M. Cacho-soblechero, T. S. Lande, and P. Georgiou. "A fully-digital ISFET front-end with In-Pixel Sigma-Delta Modulation". In: *2018 IEEE Biomedical Circuits and Systems Conference (BioCAS)* (2018), pp. 2–5.

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Chapter 4

Towards a Diagnosis-on-a-Chip: Digital ISFET Sensor

4.1 PoC Diagnostics in a Pandemic situation

On the 31st of December of 2019, the Wuhan Municipal Health Commission reported to the World Health Organisation (WHO) a new type of pneumonia in Wuhan, Hubei [1]. This new type of coronavirus, named COVID-19, spread worldwide within few months and, at the time of writing of this thesis, it is still causing thousands of deaths every day across the globe [2].

During this pandemic, Point-of-Care diagnosis became a key element in the fight against the spread of the disease, with unparalleled development of diagnostic devices [3–5] to address critical limitations on existing standard methods [6]. These novel diagnostic devices aim to achieve a rapid, reliable and accurate diagnosis at the Point-of-Care in an inexpensive manner and with minimal sample preparation. Furthermore, this pandemic unveiled two additional aspects that I argue to be key for this and any upcoming pandemic:

- **Deliverable tests:** All-in-one tests with the potential of being delivered to the population by post. To achieve this, PoC tests would require an ultra-compact form factor and low manufacturing and deployment cost.
- **Connected tests:** COVID tracking apps have flourished during this pandemic. Coupling these tools with PoC diagnostic tests can enhance our understanding of disease spread, assisting in developing tailored health policies.

In this chapter, I propose a change in paradigm on the development of ISFET-based LoC diagnostic platforms, realising a “Diagnosis-on-a-Chip” (DoC). This novel concept encompasses

systems that integrate sensing, processing elements, diagnosis algorithms, ML models, and communication protocols on a single substrate, providing an accurate and deliverable diagnosis while minimising the need for off-chip components to only on-PCB antennas and batteries. This concept is illustrated in Figure 4.1.

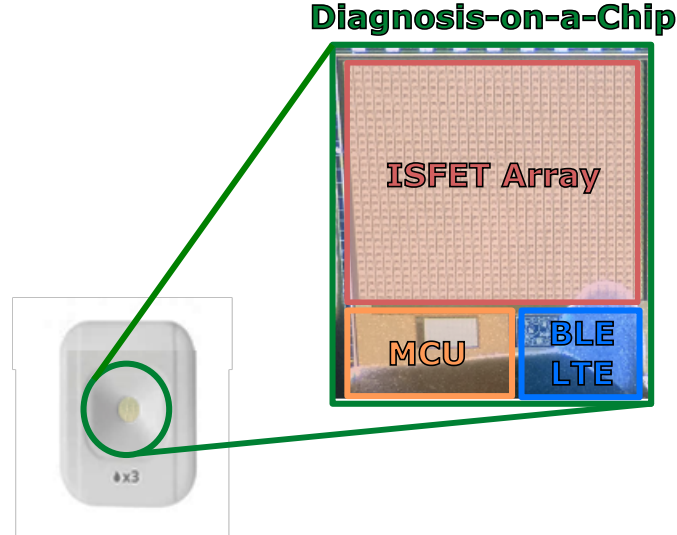


Figure 4.1: Schematic representation of a Diagnosis-on-a-Chip (DoC)

By integrating the entire diagnostic pipeline on a single device, DoC platforms leverage the intrinsic benefits of CMOS technology in terms of minimal power consumption and reduced cost thanks to economies of scale. Furthermore, the minimal form factor enhances its deliverability, potentially enabling postal delivery while providing connectivity through Internet of Things communication protocols, such as LTE (Long Term Evolution), Nb-IoT (Narrowband Internet of Things) or BLE (Bluetooth Low Energy).

In order to seize this opportunity, ISFET architectures must be adapted to the DoC requirements. I propose a new approach to ISFET front-end design throughout this chapter, bringing sensing, conditioning, digitisation, and storage inside each pixel to reduce overall platform footprint and enable a single-device, monolithic diagnostic test.

4.2 Introduction to In-Pixel ADC Architectures

Chapter 3 introduced Oscillator-based ISFET architectures, highlighting its main benefits to enhance sensing capabilities towards programmable and multimode architectures. However, this sensing flexibility was achieved at the expense of certain drawbacks intrinsic to oscillators:

- **Reduced Frame Rate:** These architectures enable only 1 pixel at a time, limiting the system parallelisation and, ultimately, its frame rate. Enhancing this parallelisation

would require careful design to avoid oscillator cross-talk and substrate-induced frequency locking, as well as additional biasing and programmable DACs that require extra area and power consumption.

This reduced frame rate becomes especially significant when developing datasets for Machine Learning (ML) models that unveil further reaction insights. A lower frame rate leads to reduced training data, potentially yielding slower convergence and an inferior generalisation.

- **Digital Processing Integration:** Oscillator-based architectures achieved a straightforward integration with MCU, requiring no additional ADC but a simple counter. However, the data generated still needs to be stored in an off-pixel memory, which could represent a significant portion of highly constrained embedded units. Furthermore, if programmability is also included for non-idealities compensation, the compensation value of each pixel would need to be stored as well, adding extra memory elements and further limiting the scalability of such systems.

Achieving memory integration with sensing elements is vital to develop budget-constrained and highly portable devices, where memory elements usually consume a large portion of commercial MCU, increasing its price and footprint. An example of these requirements can be found in Moser et al. [7], who previously demonstrated compensation value storage in-pixel to enable automated on-chip trapped compensation without sacrificing chemical sensing area.

These requirements are similar to the ones faced by CMOS Imagers over the last decades. In 1999, Abbas El Gamal presented the concept of Pixel-Level Processing in his review “Pixel Level Processing - Why, What and How?” [8], predicting the transition from an Active Pixel Sensor (APS) to a Programmable Digital Pixel, later renamed as Digital Pixel Sensor (DPS). This transition was envisioned based on deep submicron CMOS technology evolution, postulating that the trend towards increasingly smaller feature sizes that would enable integrating more transistors and functionality in the same silicon area. Under this assumption, each pixel could potentially integrate both an ADC, memory elements and computational capabilities, performing signal conditioning, digitisation and digital signal processing at the pixel level. This approach offers benefits in terms of power and frame rate, enabling the early detection of image features without requiring data transmission off-array. Figure 4.2 offers a schematic of this vision.

In this initial paper, Abbas El Gamal proposed an in-pixel ADC architecture where both a ramp and a digital code were broadcast to every pixel on the array [8]. The DAC signal was compared at the pixel level through a simple comparator, which triggers a latch if the sensed signal exceeds the ramp potential, saving the DAC code on a small in-pixel memory. El Gamal

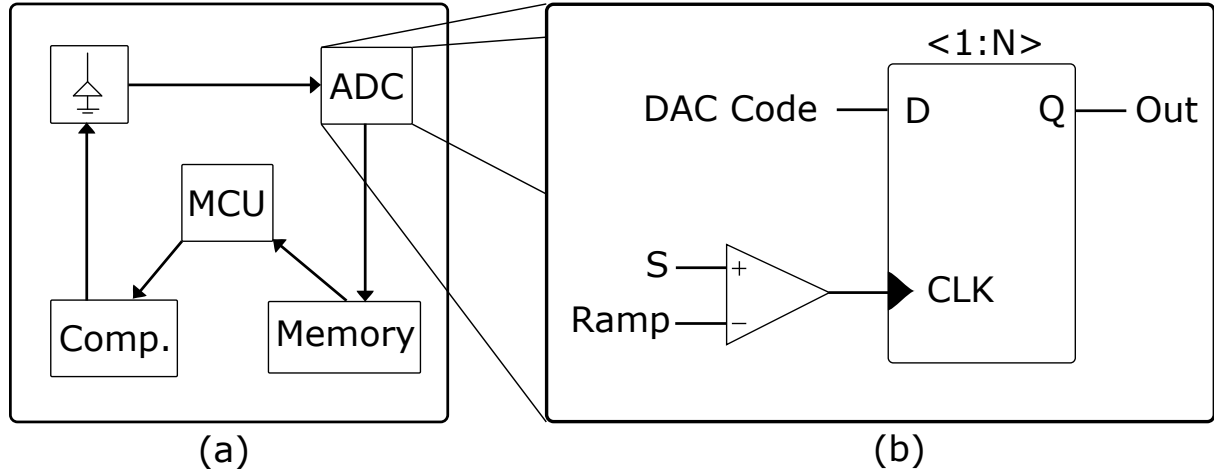


Figure 4.2: Digital Pixel Sensor (DPS) concept, containing (a) an illustrative schematic, and (b) a proposed initial ADC architecture, adapted from Abbas El Gamal [8]

proposed that these memory elements could later be used for subsequent digital processing at the pixel or the neighbourhood level.

This paper is considered one of the initial inspirations of a fruitful trend that flourished over the last decade, fueled by the booming market of imaging consumer products. Branded as “vision chips”, these architectures presented neighbourhood and pixel-level processing that sacrifices fill factor to achieve ultra-high frame rate [10, 11] and local processing [12–15] for computer vision time-critical applications, leveraging on a highly parallel Single Instructions Multiple Data (SIMD) architecture. This increase in frame rate is especially significant in small arrays, where the gain in speed offset the readout overhead associated with pixel-level storage [9]. Figure 4.3 represents this concept [9], where the frame rate and the array size are compared for different acquisition strategies: the Global ADC approach (one ADC for the entire image sensor), Column parallel ADC (one ADC per array column), and the discussed DPS.

The benefits provided by the DPS architecture on CMOS Imagers have the potential to overcome the current limitations of ISFET architectures and, more specifically, the highlighted drawbacks of Oscillator-based ISFET architectures. Furthermore, the on-chip image segmentation and object detection achieved by “vision chips” [11] serves as inspiration for the development of ISFET architectures that enable the realisation of a “Diagnosis-on-a-Chip”.

These architectures presents two main drawbacks. Firstly, these pixels present a higher constrain on the spatial resolution achievable - as more logic is included inside the pixel, its footprint would increase. However, as we discussed in Section 3.3, a pixel size below $50 \times 50 \mu\text{m}^2$ would still satisfy the requirements for DNA-amplification detection using ISFET arrays, as this application does not require high spatial resolution. Secondly, digital pixels usually embed algorithms at a pixel level, enhancing speed but limiting its versatility. To demonstrate the feasibility of this initial architecture, all processing will be integrated at a chip level, and

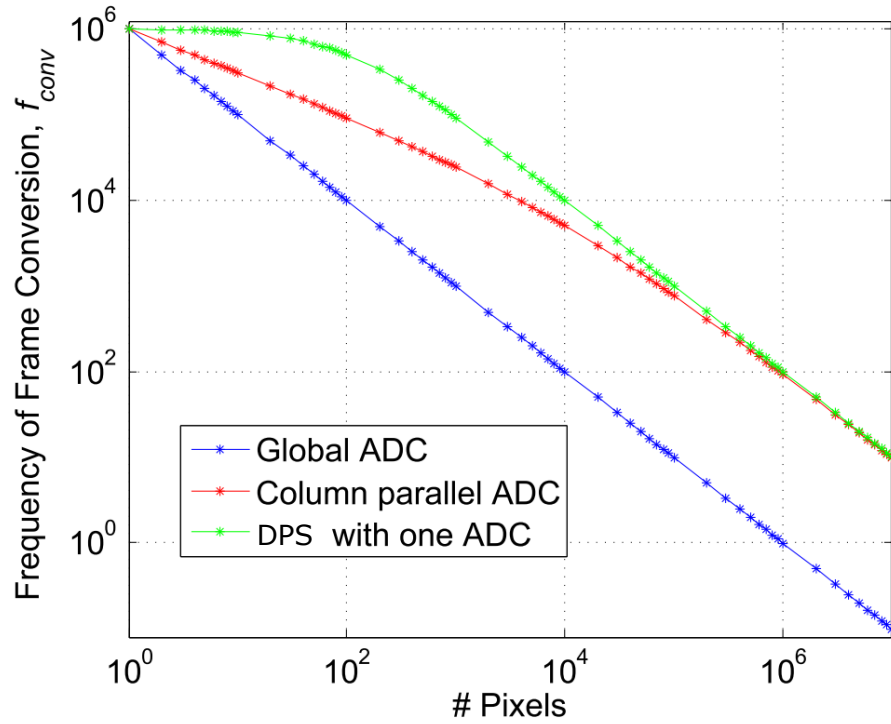


Figure 4.3: Frame Rate Comparison based on the pixel architecture and # pixels [9]

in-pixel algorithm integration will remain subject to future work.

4.3 Digital ISFET Sensor ¹

Inspired by this DPS architecture, this section presents a novel Digital ISFET Sensor (DIS) pixel and its system-level architecture. This pixel architecture, illustrated in Figure 4.4, contains an ISFET-based comparator and a latch, forming an In-Pixel ADC; and a memory bank to store the obtained results locally. Each pixel in this architecture receives a global DAC signal and its associated digital code, comparing this signal with the ISFET gate voltage ($V_{g''}$) and latching and storing the digital code when $V_{DAC} > V_{g''}$. This single-slope, comparator-distributed ADC strategy achieves full-frame sampling using a single ADC cycle.

To accommodate trapped charge variations produced during the CMOS fabrication process, a Programmable Gate [16] provides bias compensation for pixel mismatch. To enable wide dynamics at the Programmable gate, each pixel includes a gate-bootstrapping mechanism that generates negative voltages, enhancing the input range of the sensor. The binary calibration value is also stored in-pixel and only needs to be loaded once, eliminating the need for memory refreshing and calibration overhead.

¹The circuit and simulations presented in this section were designed by Jinzhao Han under the direct supervision of Miguel Cacho Soblechero.

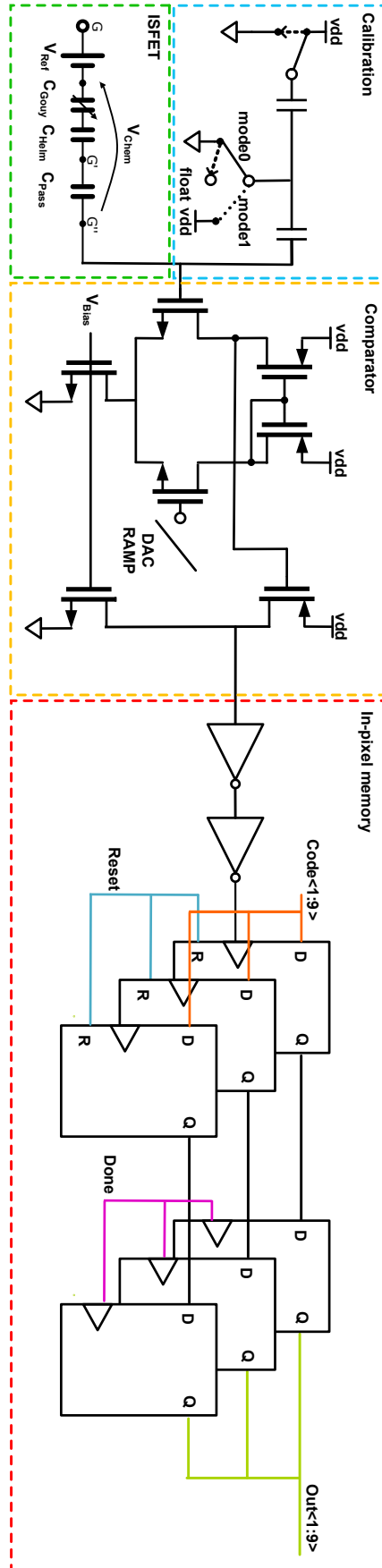


Figure 4.4: Digital ISFET Sensor (DIS) pixel overview, composed by (Blue) Programmable Gate Bootstrapping Calibration block, (Green) CMOS ISFET Macromodel, (Yellow) Comparator and (Red) In-pixel Memory block [17] (© 2021 IEEE)

4.3.1 Pixel Operation

The designed Digital ISFET Sensor architecture comprises two blocks: the In-Pixel ADC, which converts the sensor signal into a digital code and stores it in-pixel; and the Programmable Gate Bootstrapping, which provides the compensation mechanisms to accommodate the pixel input range for trapped charge variations.

In-Pixel ADC

The In-Pixel ADC architecture, presented in Figure 4.4, uses a single-slope strategy with a chip-level DAC, with a comparator and a memory bank inside each pixel. This comparator contains an ISFET in one of its branches and it is connected to a 2x9-bit in-pixel memory block, which stores the global DAC value. The calibration block determines the exact biasing point of this comparator. The In-Pixel ADC operation can be divided into three phases:

- **Reset Phase:** In this phase, the ISFET biasing point calibration potential is loaded and maintained at V_{PG} , while any previously sampled conversion is cleared from memory asynchronously through the *Reset* signal.
- **Sampling Phase:** During this phase, the off-pixel Digital Control Unit enables a global counter, transmitting the count value to both each pixel and the global DAC simultaneously. The DAC potential generated is broadcast to every pixel. At each DAC step, the in-pixel comparator determines whether the DAC potential V_{DAC} is greater than the sensed chemical potential at $V_{G''}$. When this occurs, the associated DAC value is latched and stored in the first 9-bit memory bank.
- **Done Phase:** Once the counter generated at the Digital Control Unit reaches its maximum value, the signal *Done* is broadcast to all pixels, triggering the storage of the conversion result on the second 9-bit memory bank. This operation enables simultaneous sensing and reading operation, enhancing parallelisation.

A flow diagram detailing the signals involved in each phase is provided in Figure 4.5. This operation can be performed array-wise simultaneously at all pixels, requiring one single ADC cycle to obtain an entire frame and enhancing the sampling rate.

Special attention was paid to the memory design to achieve a minimal footprint while preserving non-volatile storage and parallel Read-Write operation. The designed memory architecture is presented in Figure 4.6, inspired by the finding published by Zhang et al. [14].

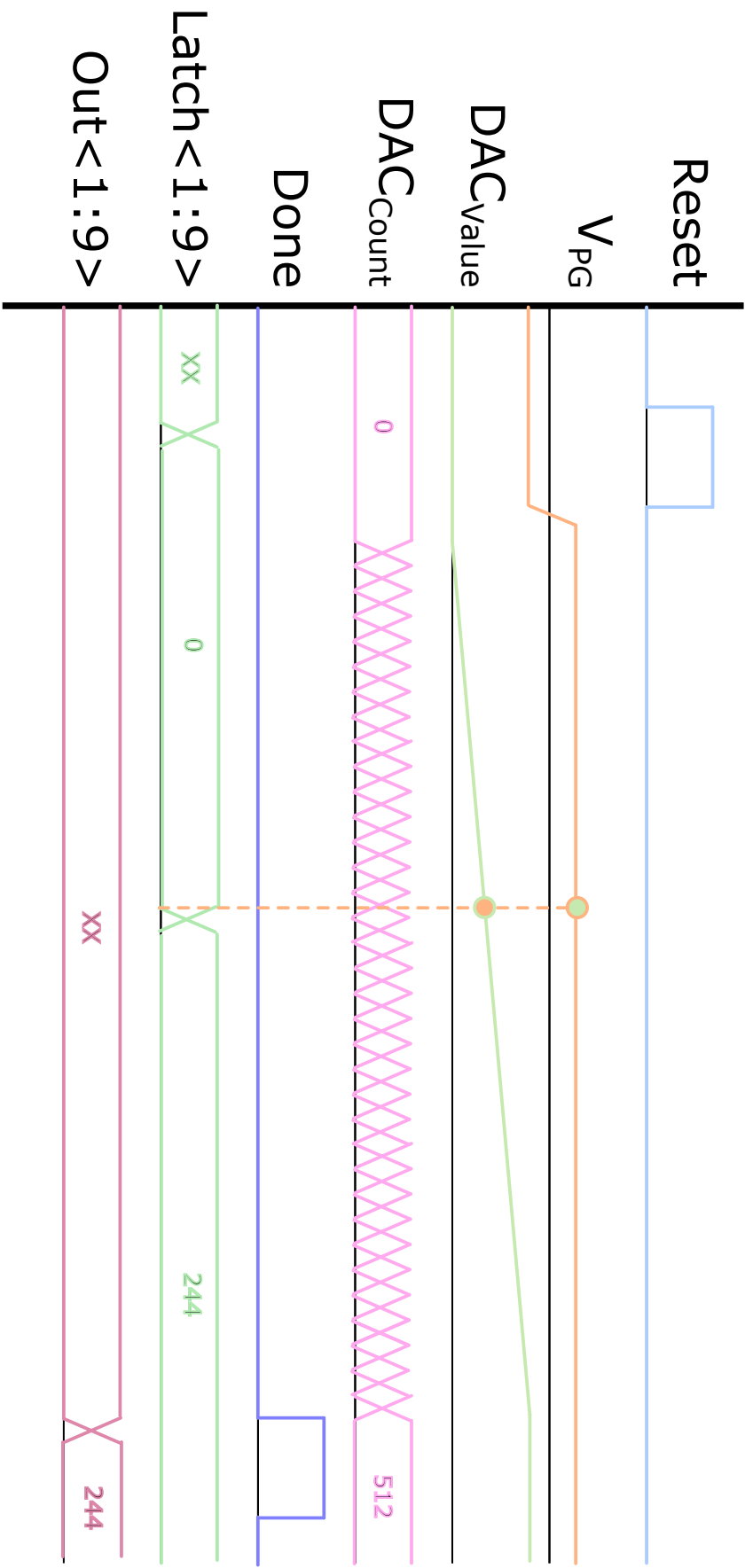


Figure 4.5: Digital ISFET Sensor (DIS) pixel operation diagram, illustrating all signals involved during *Reset*, *Sampling* and *Done* phases. In this graph, it is assumed compensation Mode 1 preloaded inside the in-pixel memory.

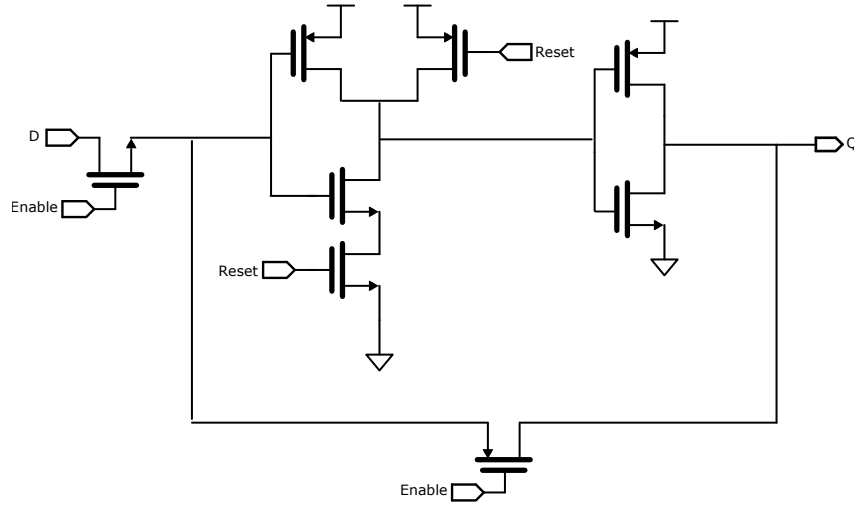


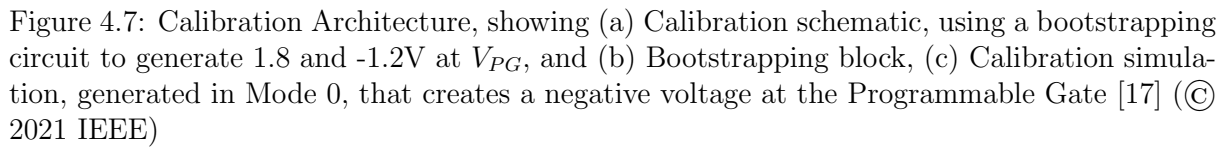
Figure 4.6: Digital ISFET Sensor (DIS) 8-T Compact Memory Architecture for In-Pixel Storage

Programmable Gate Bootstrapping

As highlighted in Section 2.3.2, trapped charge introduced during CMOS fabrication leads to a mismatch between the pixels, expanding the ADC dynamic range required to accommodate this variability. To enhance pixel adaptability to various trapped charge conditions without impacting the limited input range of the system, a novel compensation method is presented, utilising a Programmable Gate (PG) and a Bootstrapping circuit to create two biasing points on the pixel, as illustrated in Figure 4.7. To enhance V_{PG} dynamic range, a bootstrap circuit is included to create a high impedance node even at voltages below the rail with minimal leakage. This compensation mechanism consists of two biasing modes selected and stored in-pixel through a 1-bit memory.

- **Mode 0** - $V_{PG} = -1.2V$: Mode 0 activates the bootstrapping circuit [18], which precharges the node V_{Boots} to V_{DD} , and the programmable gate voltage V_{PG} to ground. At the falling edge of *Reset*, C_{Boots} polarity is inverted, pushing V_{PG} to a negative potential of around $-1.2V$, as shown in Figure 4.7c. After *Reset* falling edge, the bootstrapping circuit sets the PMOS gate at V_{DD} to avoid leakage at V_{PG} during the sampling phase.
- **Mode 1** - $V_{PG} = 1.8V$: Mode 1 connects directly the ISFET PG to the highest voltage. In this process, the maximum V_{DD} is $1.8V$

The effect of these two modes in the calibration curves is shown in Figure 4.8, creating two sensitivity curves with an offset that enlarges the input range. The corresponding mode on each pixel is derived from an initial calibration phase, where the trapped charge across the array would be analysed.



The proposed DIS pixel architecture was integrated as part of a larger System-on-a-Chip, composed of three blocks:

- *16x16 DIS Array* \Rightarrow A 16x16 array was formed using the Digital ISFET Sensor (DIS). All pixels share signal buses, V_{DAC} and DAC count buses, as well as individual Row/Column selection signals for calibration storage and output readout. This array creates a 16x16 array of single-slope in-pixel ADCs coordinated by a global DAC and a Digital Control System.
- *Rail-to-Rail 9-bits Global DAC* \Rightarrow A DAC generates the sampling ramp, global to the entire array. The DAC was implemented using an R-2R architecture, and an output

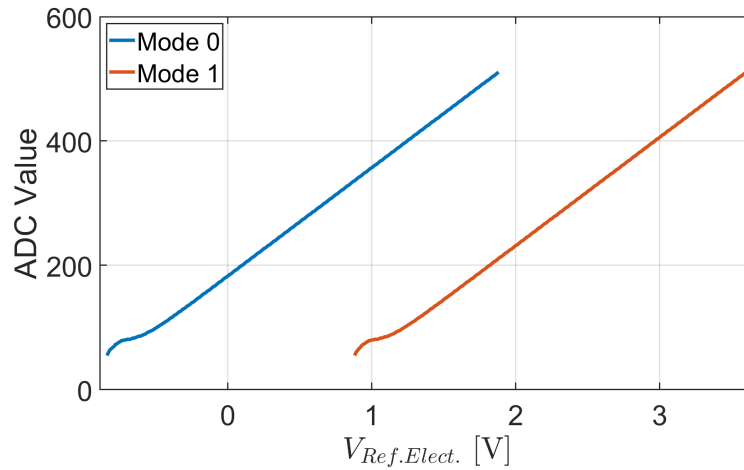


Figure 4.8: Digital ISFET Sensor (DIS) Sensitivity Curves obtained with the two calibration modes [17] (© 2021 IEEE)

rail-to-rail buffer was included to minimise signal delay due to array load.

- *Digital Control System* \Rightarrow A Digital Control Unit provides array signalling for operation, triggering calibration, reset, and done phases, as well as the digital counter requirement for DAC broadcasting and system operation. Furthermore, an SPI interface enables communications with off-chip components.

This architecture was implemented in TSMC 180nm technology and submitted for fabrication. The complete system occupied 1.2×0.7 mm, where each pixel represents $45 \times 44 \mu m^2$. Figure 4.9a and 4.9b provides both pixel- and system-level layout, respectively, Table 4.1 summarises its simulated performance. A sampling clock of 10 MHz was assumed for simulation, a conservative frequency suitable for functional verification.

Table 4.2 compares the simulated performance with the State-of-the-Art. This comparison highlights the following characteristics from this architecture:

- **Single ADC Cycle Frame Acquisition:** The DIS system requires one single ADC cycle to obtain a complete frame. This sampling methodology overcomes the trade-off between the frame rate and the number of column-level ADC channels, establishing the frame rate as a function of the ADC clock and the reading process. Assuming a conservative ADC clock frequency (f_{ADC}) of 10MHz, the DIS array obtained a frame every $51.2 \mu s$, potentially yielding over 19000 frames/s and moving the sampling bottleneck from sensing to transmission. Furthermore, this pixel architecture could be scaled to larger arrays without any instrumentation overhead, pushing the scalability bottleneck towards data extraction process from the array.

Table 4.1: Digital ISFET Sensor - Simulated System Performance [17] (© 2021 IEEE)

Digital ISFET Sensor - Simulated Performance <i>Assuming pH sensitivity = 30 mV/pH</i>	
Performance parameter	Value
Pixel Size	44 x 45 μm^2
Sensing domain	Voltage
Input Range	4.45 V
Resolution	0.1766 pH
Linearity (R^2)	0.9987
Sampling Time (@ 10 MHz)	51.2 μs /frame
Pixel Power consumption	10.15 μW
System - Simulated Performance	
System Size	1200 x 700 μm^2
Array Size	16x16 pixels
Technology	TSMC 180nm
Supply Voltage	1.8V
Off-chip Interface	SPI
Total power consumption	4.26 mW
DIS Array	2.56 mW
Rail-to-Rail DAC	676 μW
SPI & Digital Control	1.03 mW

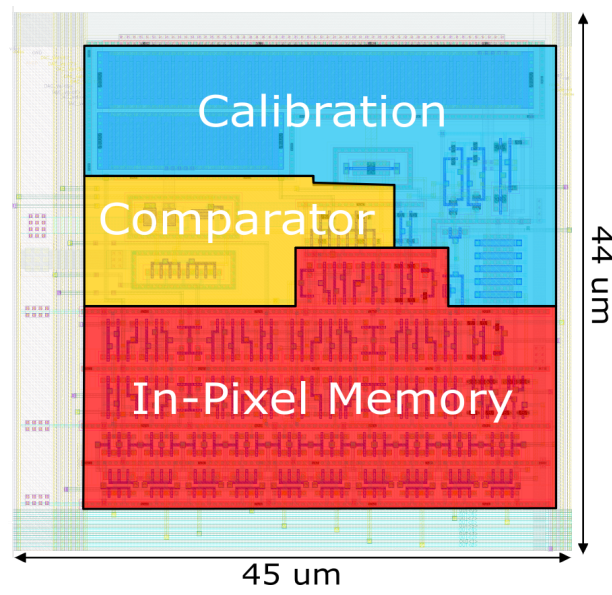
Table 4.2: Digital ISFET Sensor - State-of-the-art Comparison [17] (© 2021 IEEE)

Specification	This Work	[7]	[19]	[20]	[21]	[22]
Technology	0.18 μm	0.35 μm	0.35 μm	0.18 μm	0.18 μm	0.18 μm
Supply [V]	1.8	3.3	3.3	1.8	1.8	1.8
Sensing Domain	Voltage	Time	Current	Time	Duty Cycle	Voltage
Pixel pitch [μm^2]	44x45	37x31	18x12.5	26x26	40x40	50x50
Input Range	4.45 V	-	100 μA	± 7 V	0.2025 V [†]	7.1 V
Resolution [pH]	0.1766	0.017	-	0.08	0.11	0.014
Sampling Time	51.2 μs /frame	-	333 μs /frame	1 ms/frame	100 ms/frame	25.6 ms/frame
Pixel Power Consumption	10.15 μW	99 μW	-	0.01 μW	-	-
ADC Strategy	In-Pixel	Global	Column-Level	Column-Level	Global	Global

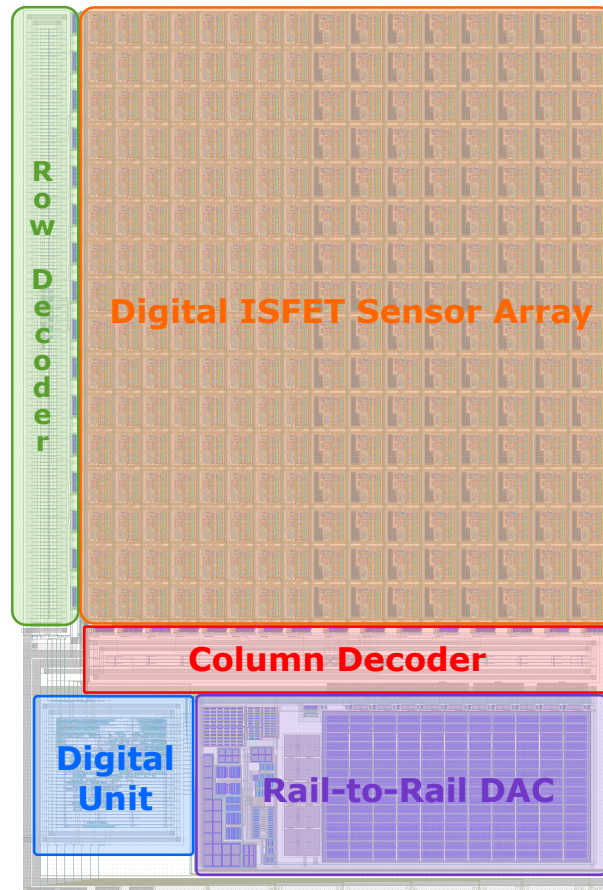
[†] Not taking into account trapped charge compensation

- **Integration with Processing Elements:** By eliminating the need for external memories to store the conversion result, the system could be integrated with processing elements at the pixel level, providing functionality for computer vision algorithms on-chip such as filtering, image segmentation or object tracking [11, 15, 23]. Furthermore, no additional memory elements would be required for sensing storage, integrating non-volatile memories in-pixel.
- **Large Input Range through Bootstrapping Gate:** One of the main challenges for in-pixel ADC is trapped charge compensation, as all pixels are addressed and sampled simultaneously. Hence, the proposed bootstrapping mechanisms enable an expansion on the sensor input range while requiring only 1 bit of in-pixel storage, accommodating trapped charge variations at a pixel level.

These characteristics make this architecture an ideal candidate for its integration with processing capabilities, a critical feature to achieve a “Diagnosis-on-a-Chip”. This sensing-processing integration process is explored in the next section, blending the architecture with an ARM Cortex M3 through an Advanced High-performance Bus (AHB) interface.



(a)



(b)

Figure 4.9: Pixel and System-Level architecture and layout, showing (a) Pixel Layout formed by calibration, comparator (containing ISFET) and In-Pixel Memory, (b) System level architecture [17] (© 2021 IEEE)

4.4 Processing Elements integration for a Diagnosis-on-a-Chip ²

The recent success of IP-based advanced MCU architectures, fueled by the high demand for Internet of Things (IoT) devices, has catalysed the accelerated development of compact and low power processing units integrated with sensing capabilities, developing the so-called "Smart sensors". The MCUs market powering these smart sensors is mainly dominated by ARM and their Cortex-M series, which provides minimal footprint and power consumption for IoT applications. In this section, I leverage these ARM Cortex-M architectures to provide a Proof-of-Concept of the proposed paradigm shift, illustrating how to achieve a Diagnosis-on-a-Chip by integrating processing elements with the Digital ISFET Sensor array at the system level. Although trivial from the research perspective, the development, integration and debugging of this End-to-End architecture represents a significant technical challenge, key for the deployment of such system as a Diagnosis-on-a-Chip.

ARM M-Series portfolio offers a wide variety of features targeting different requirements and IoT applications. A summary of these MCUs, along with the distinct provided features, is provided in Table 4.3 [24]. For the initial realisation of a Diagnosis-on-a-Chip, an ARM Cortex M3 was selected for integration with DIS array, trading computational performance for low power and silicon area. If floating-point operations would be needed or DSP algorithms would be required, an ARM Cortex M4 with Floating Point Unit support should be considered instead, at the expense of silicon area. The architecture presented in this section applies both to Cortex M3 and M4 options.

Table 4.3: ARM Cortex M Comparison [24]

Series-M MCU	M0	M0+	M3	M4
Instruction Set Architecture	Armv6-M	Armv6-M	Armv7-M	Armv7-M
Multiplication Capabilities	32 bits	32 bits	32/64 bits	32/64 bits
Hardware Divide	✗	✗	✓	✓
Floating Point Support	✗	✗	✗	✓
Digital Signal Processing (DSP) Support	✗	✗	✗	✓
Maximum # External Interrupts	32	32	240	240
Bus Protocol	AHB Lite	AHB Lite	AHB Lite	AHB Lite
TrustZone Support	✗	✗	✗	✗
Estimated Area @ 40nm Process	0.00073 mm ²	0.0066 mm ²	0.024 mm ²	0.028 mm ²
DMIPS/MHz	0.87	0.95	1.25	1.25
Target Applications	Lowest cost and low power	Highest energy efficiency	Performance efficiency	Mainstream control and DSP

ARM Cortex-M3 standard architecture is composed of the following elements:

- **ARM Core:** Main Processing Unit, in charge of code execution
- **AHB Buses:** Connecting the core with high latency peripherals, such as instruction and data memories and critical interfaces. ARM Cortex-M3 architecture contains 2 AHB

²The circuit and simulations presented in this section were designed by Jinzhao Han under the direct supervision of Miguel Cacho Soblechero.

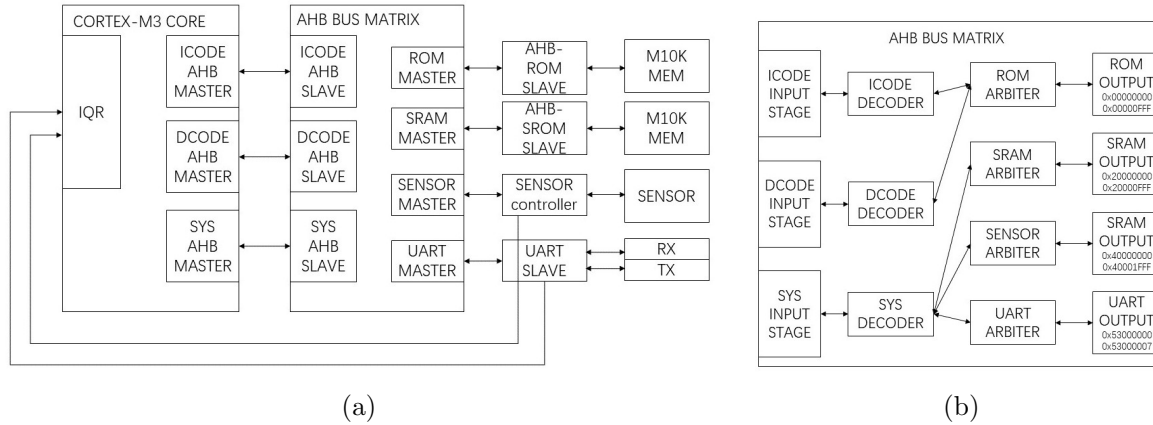


Figure 4.10: ARM Top Level Architecture, presenting (a) Interconnections between ARM Cortex M3 and peripherals through AHB bus, (b) AHB Bus Architecture

buses, code bus and peripherals bus, to avoid delayed code execution due to peripherals latency.

- **APB Buses:** APB, or Advance Peripheral Bus, connects the core with low latency peripherals. This bus is required when many peripherals are connected, avoiding congestion on the AHB bus. This situation was not an issue in our example design.
- **RAM/ROM/Flash Memories**
- **Peripherals:** Connects the code with different elements on the SoC, ranging from sensing elements to communication interfaces. Each peripheral requires specific memory mapping, bus arbiters, and a separate AHB/APB interface to bridge the peripheral physical layer and the AHB bus logic.

The proposed SoC contained two memory peripherals - ROM/Flash for instructions, RAM for execution data - and two high latency peripherals: The DIS array, interfaced through a custom AHB controller, and a UART interface to provide off-chip communication. This architecture is illustrated in Figure 4.10a, with the bus architecture presented in detail in 4.10b. Two additional interrupts were included from both UART and DIS interface to ensure fast response to bus requests.

Figure 4.11 presents the entire system architecture, highlighting internal connections and external interfaces. The connectivity between the ARM Cortex M3 Core and the sensing system was achieved through SPI for functional validation upon DIS system fabrication. However, this interface could be removed by integrating the AHB interface with the Digital Control Unit on-chip.

This system's initial functional verification was performed on an FPGA board, synthesising the proposed architecture with a DIS array behavioural model. This analysis validated the

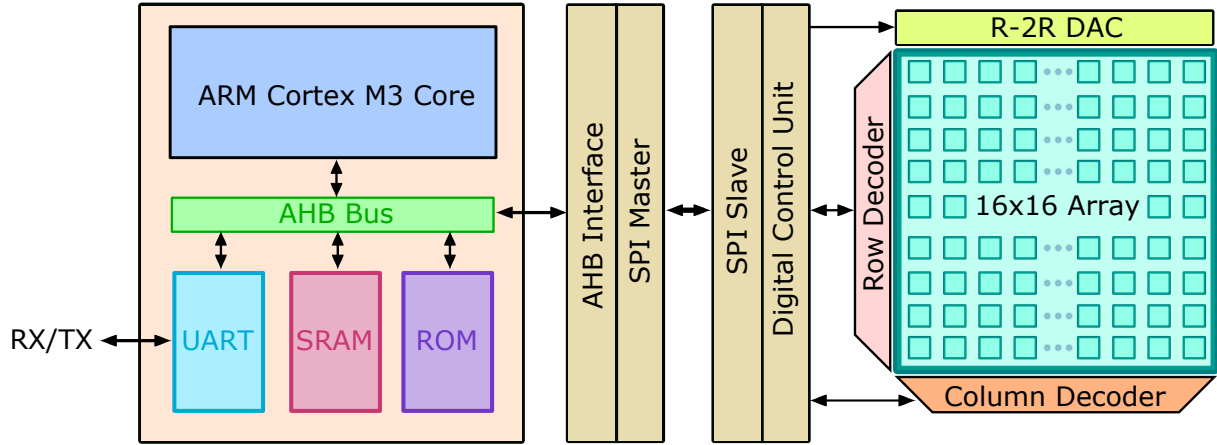


Figure 4.11: Full System-on-Chip Integration

feasibility of integrating computational capabilities with sensing elements on-chip and opens the doors for further sensing-processing combination on-chip that enable a more affordable, precise and deliverable diagnosis at the Point-of-Care.

At the date of writing of this thesis, the Digital ISFET Sensor array is under fabrication. Upon arrival, *in silico* verification would take place, evaluating both the performance of this array and the proposed connectivity with an FPGA board. This validation would set the ground for future work on full integration as a "Diagnosis-on-a-Chip".

4.5 Summary

This chapter introduced a novel concept of "Diagnosis-on-a-Chip", a paradigm shift on ISFET-based diagnostic platform development. This idea proposed integrating sensing capabilities with processing elements and communications on-chip, leveraging the recent development of MCUs and highly accurate ML models to provide a precise diagnosis without requiring additional equipment.

For ISFET architectures to achieve a "Diagnosis-on-a-Chip", I looked for inspiration on CMOS Imagers, where processing elements on-chip have been widely explored for high latency, low-resolution applications. Based on these "Vision Chips", I proposed and implemented a Digital ISFET Sensor (DIS), a novel ISFET architecture with in-pixel processing, digitisation and storage. This pixel was highly scalable to large arrays, requiring only one ADC cycle to obtain an entire frame and compensating in-pixel for trapped charge non-idealities. Furthermore, no external memories were required to keep the sensing values for post-processing, as each pixel stored the more recent sensed result. This pixel architecture was integrated as part of a 16x16 array, achieving high frame rates and wide input dynamics in a compact form factor.

This array was then integrated into a System-on-Chip using an ARM Cortex M3, merging computational and sensing elements. This Proof-of-Concept system, verified on an FPGA for functional validation, showcases the feasibility of this paradigm and represents the first step towards the full integration of the End-to-End diagnosis process on a single silicon die.

I envision that a “Diagnosis-on-a-Chip” can significantly benefit PoC diagnosis in terms of deliverability and cost, critical aspects in pandemic situations like the recent COVID-19, where a fast, affordable and widespread diagnosis is critical for the early control of the virus transmission.

However, to fully realise this concept, exploring hardware innovation would not be enough. Designers and researchers should develop effective software methods and predictive ML models that enable accurate diagnosis while facing the challenge of highly constrained systems such as IoT devices. In the following chapters, I investigate ISFET-oriented software methods and ML opportunities to enhance ion-imaging sensing capabilities.

4.6 Publications & Awards

The following publication arose from the content of this chapter.

- [17] J. Han, M. Cacho-Soblechero et al. “A Digital ISFET Sensor with In-Pixel ADC”. In: *2021 IEEE International Symposium on Circuits and Systems (ISCAS)* (2021), pp. 1–4.

The concept and the architecture presented in this chapter was awarded the **Qualcomm Innovation Fellowship**

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Chapter 5

Software methods for adaptability enhancement of ISFET PoC Platforms

5.1 Motivation

The urgent need for portability of Point-of-Care devices and their requirements regarding adaptability to various external conditions have driven the recent trend towards integrating ISFET sensing platforms with versatile computational elements to enable their use for PoCT [1–3]. These devices leverage recent advances on compact, affordable and ultra-low power Micro-Controller Units (MCUs) to extract sensing information and send it wirelessly for post-processing to high-end devices such as smartphones.

Furthermore, the recent development of portable single-board computers, such as Raspberry Pi [4], or Rock64 [5], enable the integration of computational methods at the Point-of-Care to enhance the adaptability of these platforms. In synergy with the programmability available on the dual-sensing oscillator-based architecture described in Section 3.3, these capabilities open a wide range of opportunities to overcome the current limitations of ISFET-based sensing platform at the Point-of-Care through software methods. Moreover, emerging ISFET-based diagnostic paradigms such as the “Diagnosis-on-a-Chip” presented in Chapter 4 require intelligent algorithms for an End-to-End automated diagnosis.

This chapter presents a portable platform, named “instantDNA”, that enables the deployment, validation and evaluation of software methods at the PoC to enhance the functionality and versatility of ISFET arrays. Leveraging the computational capabilities of a Raspberry Pi blended with a custom PCB platform, I address the following state-of-the-art ISFET platforms challenges:

- **Rapid compensation of trapped charge:** The wide input range imposed by charges trapped on the ISFET passivation in standard CMOS technologies sets strict constraints to the input range of the ADC. For this purpose, compensation techniques have been proposed to mitigate the effect of trapped charge across the array, homogenising the pixels' response [6–9]. These algorithms require precise control, avoiding Fixed Pattern Noise (FPN) across the array, covering a large TC range, and rapidly achieving this calibration to enhance versatility. For this purpose, I propose a 2-step rapid calibration to mitigate the effect of trapped charge across the array rapidly.
- **Chemical resolution enhancement:** The presence of chemical noise superimposed to the electrical noise limits the LoD of ISFET arrays. This chemical noise requires developing techniques that enable signal filtering without area, power and system complexity overhead. Leveraging on the intrinsic oscillatory capabilities of the architecture presented in Section 3.3, I explore a novel method for enhancing the pixel LoD performance by modifying its biasing point and consequently its oscillation frequency. A reduction on this LoD would have far-reaching benefits on most ISFET-based Point-of-Care applications, potentially increasing the device's reliability and opening new application opportunities that require high pH resolution at a low sampling rate.
- **Long-term monitoring through drift mitigation:** Drift refers to a monotonic change at the ISFET output due to the hydration effect on the passivation surface, as described in detail in Section 2.3.2. This drift enforces broad input ranges on the pixel ADC to accommodate monotonic change over long periods. Hence, overcoming the drift limitation is critical to enable long-term monitoring of ion concentration using CMOS-based ISFETs, with various applications at the Point-of-Care. Leveraging on the real-time programmability of the oscillator-based architectures described in Section 3.3, I propose a novel drift compensation approach to extend the dynamic range through algorithmic methodologies. Using this real-time compensation methodology, large datasets of drift evolution can be acquired, potentially serving as the basis for predictive models that forecast the evolution of this low-frequency noise.

This chapter is organised as follows: I first explain the architecture of the proposed portable platform, which I refer to as “instantDNA”, highlighting the capabilities that enable a flexible and versatile analysis of software methods. Then, I present an analysis of the computational methods and the consequences of these results for deploying ISFET arrays as part of Point-of-Care applications.

5.2 instantDNA: A versatile PoC platform for ISFET sensing

A self-contained portable platform, named “instantDNA”, was developed to serve as a versatile test-bench to explore software methods that can enhance the adaptability and performance of ISFET platforms. In comparison with previous platforms, such as the one presented by Miscourides et al [10] or Lacewing, presented by Moser et al [1, 2] and now part of ProtonDx [11], instantDNA represents a monolithic solution that requires no external device to operate (i.e. smartphone) while maintaining a compact form factor to enable portability. Initially envisioned as a versatile testing platform for ISFET arrays, instantDNA was recognised as a potential solution for PoC diagnosis, awarded as Best Demo 2019 at BioCAS 2019 [12]. This section describes the architecture of this PoC platform in detail.

5.2.1 System Level Architecture

Inspired by vintage video consoles such as the GameBoy, instantDNA was envisioned as a platform where ISFET chip cartridges could be connected in a versatile and intuitive way for fast prototyping and experimentation. This inspiration led to the creation of the architecture illustrated in Figure 5.1, showing the three main system components.

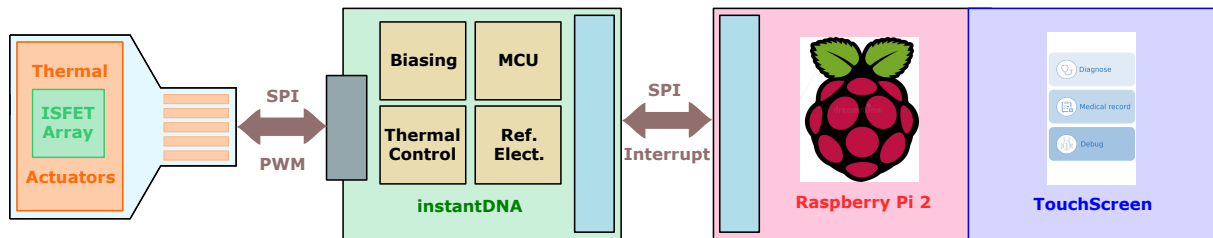


Figure 5.1: InstantDNA System Level Architecture

Chip Cartridge

The chip cartridge, designed as a mini PCIe connector, has three main functions: Firstly, it routes all required signals for sensing operation from the ISFET chip to the PCB platform. Secondly, it contains a coil directly patterned on PCB and a large golden plate on its backside, enabling the thermal actuators for implementing both heating and cooling controllers required on DNA-based diagnosis. Finally, the PCB provides an opening for reference electrode soldering. Figures 5.2a & 5.2b presents a 3D model of this cartridge, both front and back, showing the components used for thermal control: on-PCB coil and Au plate for a Peltier module.

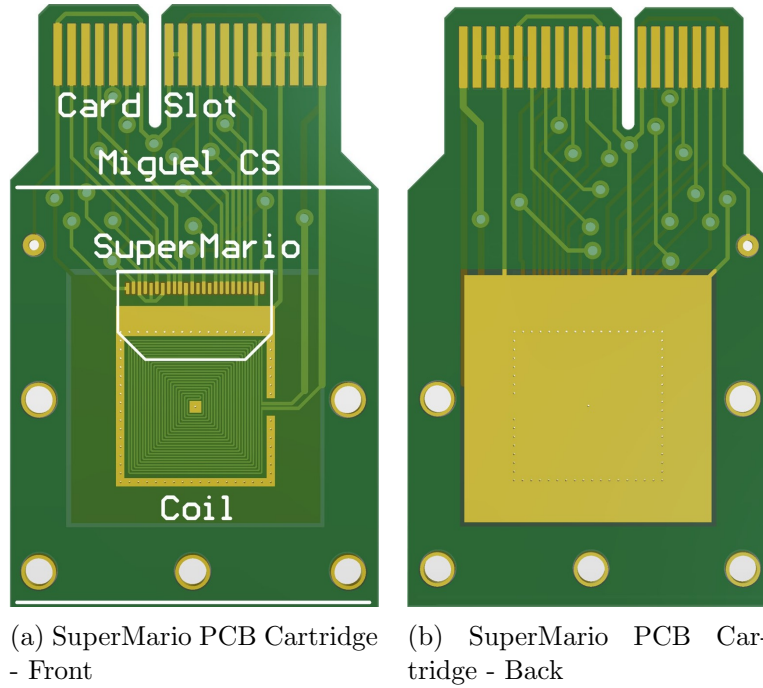


Figure 5.2: 3D model of chip cartridge, showing both front and back view. Figure (a) presents the front view, where the ISFET array is glued to the coil's surface used for heating on the thermal controller. Figure (b) illustrates the back of the cartridge, where a large Au plane is introduced to enhance thermal conduction during the cooling process of the thermal controller.

instantDNA PCB board

The instantDNA PCB serves as the bridge between the sensing elements and General User Interface (GUI), mapping high-level operations provided by the user to the low-level signalling. As illustrated in Figure 5.1, the board is divided into 4 different functionalities, which are mapped to the instantDNA board as shown in Figure 5.3:

- **Platform Controller:** The platform controller oversees and controls the biasing conditions of every element on the board. Its main component is an STM32F4 MCU, which provides communication through SPI to all components, timers for PWM signal acquisition from chip and DACs for additional biasing and debugging.
- **Biasing and Level Shifter Elements:** Level shifters between the board and the ISFET cartridge are required (SN74AVC4) due to the diversity in voltage levels. Furthermore, programmable biasing is provided through SPI controlled DACs (DAC7311).
- **Dual-Voltage Reference Electrode:** This block provides -5/5V input range for the reference electrode voltage, enabling wide trapped charge compensation swing as required for the proposed TC compensation in the Section 5.3

- **Thermal Control System:** The platform provides support for two thermal actuators, an on-PCB coil and a Peltier module for controlling the temperature of the chip. The on-PCB coil enables heating capabilities through PWM control over a power NMOS, and the Peltier module delivers cooling control by tuning the current provided.

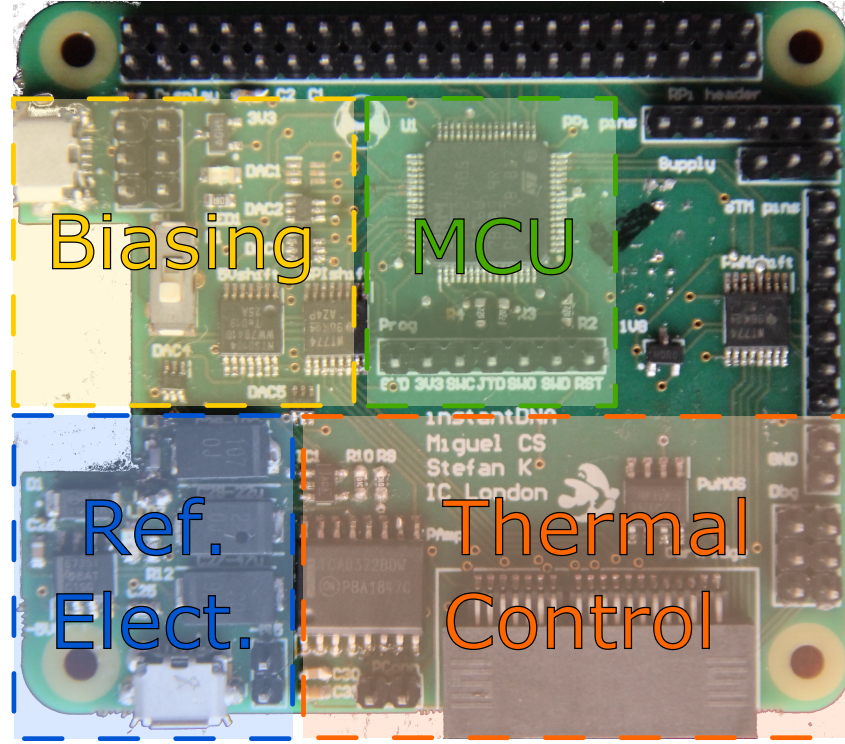


Figure 5.3: InstantDNA PCB with highlighted blocks

Raspberry Pi & Touchscreen

Single-board computers are becoming increasingly attractive for Point-of-Care applications, thanks to their computational capabilities and their reduced size at an affordable price. For these reasons, a Raspberry Pi 2 was selected for our platform to provide an intuitive GUI to the potential user and the computational means to perform our software methods locally.

The native Raspberry Pi touchscreen was integrated to provide a familiar user experience, enhancing its versatility and enabling the use of instantDNA by non-experts users. An associated GUI was designed, covering all the clinical steps required for screening and diagnosis using instantDNA. An example of various screens on this GUI is presented in Figures 5.4a, 5.4b & 5.4c.

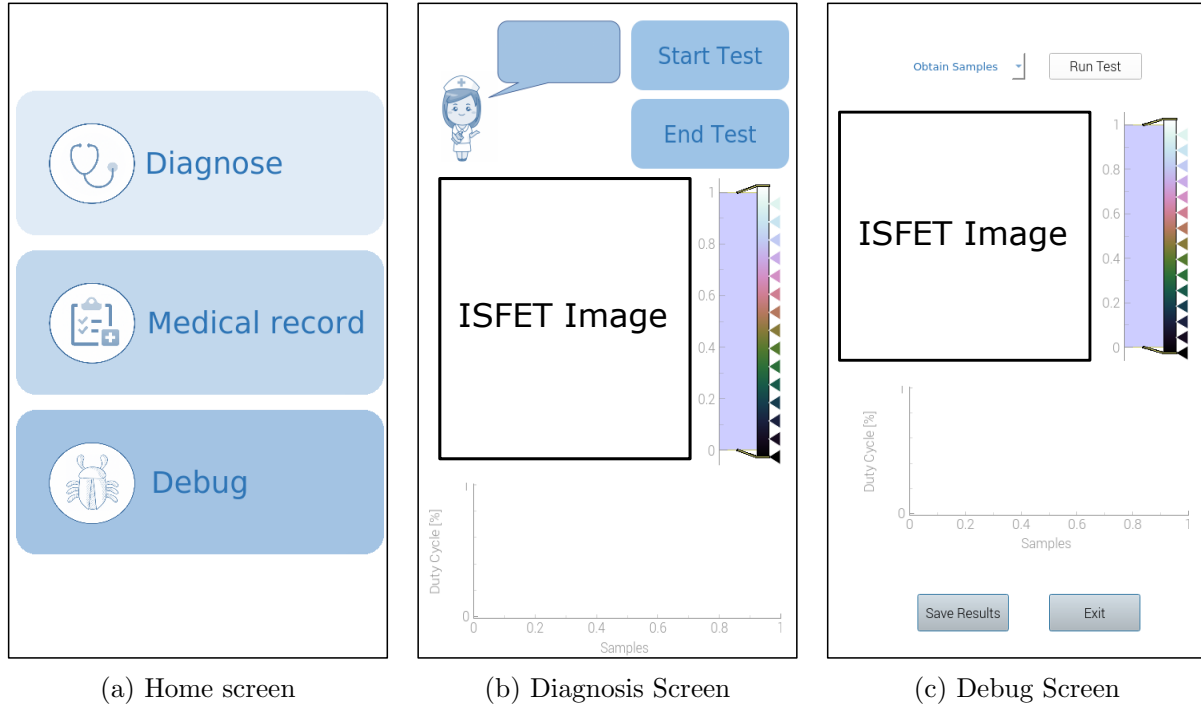


Figure 5.4: instantDNA General User Interface (GUI) example screens. Figure (a) presents the Home Screen, where the user can either start a new diagnosis, check previous medical records or debug the platform. Figure (b) shows the last screen of the diagnosis process, where the information from the ISFET is displayed and a final diagnosis decision is provided. Figure (c) presents the interface used throughout the debug process

Device Encapsulation

All components are integrated on a single device, inspired by the classic Game-Boy. A picture of the resulting case is provided in Figure 5.5. This prototype was presented at the Biomedical Circuits and Systems Conference 2019 (BioCAS 2019) on the demonstration session, achieving the Best Demo Award BioCAS 2019.

5.3 Trapped charge compensation through 2-steps adaptive controller

Following the discussion and results presented in Section 3.3.5, I now analyse in detail the trapped charge algorithm proposed for rapid trapped charge compensation. This methodology is composed of two calibration steps:

1. **Step 1 - Reference Electrode Potential Sweep:** The objective of this step is to find



Figure 5.5: InstantDNA Prototype

the reference electrode potential at which a maximum number of pixels are active. For this purpose, the Ag/AgCl reference electrode potential is set to ground (0 V), recording an initial frame. Based on the number of pixels below and above 50% duty cycle, the polarity of the optimal potential is inferred (positive potential or negative potential). The reference electrode potential is then swept, analysing the number of active pixels at each step - this is, pixels with an output duty cycle between 15% and 85%. When the increment of active pixels between two consecutive frames is negative, it is assumed that the optimal potential is reached.

2. **Step 2 - Trapped Charge Compensation:** Once the reference electrode potential is established, the next step focuses on finding the optimal voltage value V_{DAC} for setting the OTA described in equilibrium. For this purpose, a Proportional controller takes the difference between the target duty cycle range - 48% to 52% - and the measured value. This controller generates a new value for V_{DAC} for each pixel after each array scan, applied in the next iteration. The compensation process for each pixel repeats until either all pixels are within the target duty cycle, V_{DAC} is out of range or after a specific number of iterations. Figure 5.6 illustrates this second step of the controller.

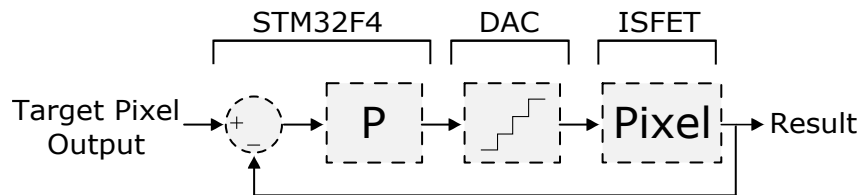


Figure 5.6: Trapped Charge Compensation Controller Architecture

The flowchart illustrating this algorithm in detailed can be found in Appendix B, Figures B.1a and B.1b. This methodology ensures that a maximum of 50 frames is required to achieve a complete calibration cycle by establishing hard limits on the number of iterations. Step 1 can take a maximum of 40 steps until reaching its maximum ($\pm 4V$), and Step 2 limit is set at 10.

Figures 5.7a & 5.7b provide the results after steps 1 & 2. In Figure 5.7a, the first calibration step distributes the pixels uniformly throughout the active range, while the compensation stage sets all pixels at the dynamic range midpoint, with a mean value of 49.97% and a standard deviation of 1.76%. This process yield 99.5% of active pixels calibrated at the target duty cycle range, homogenising pixel response across the array.

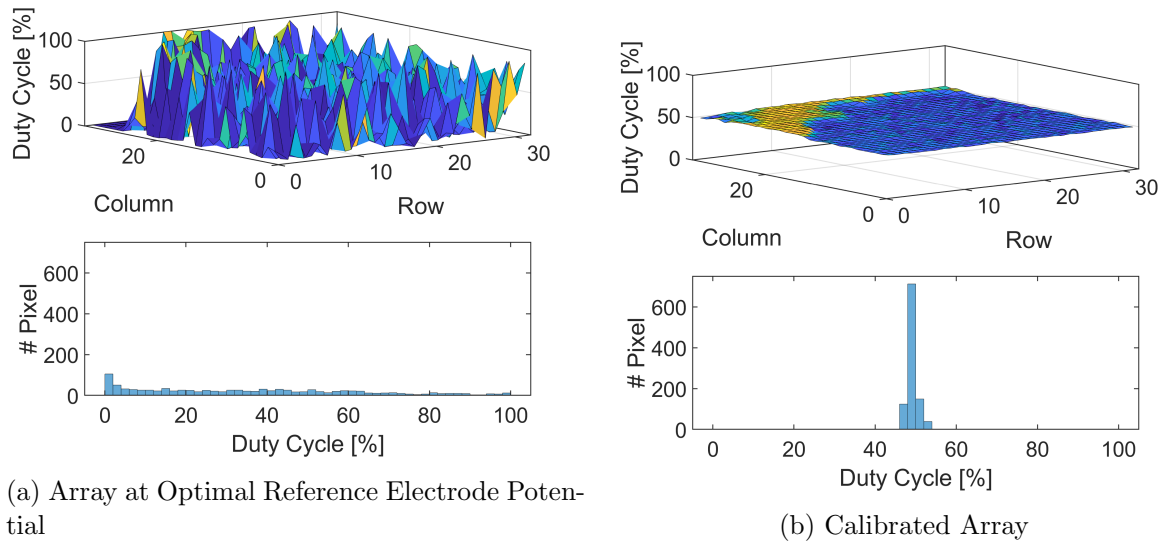


Figure 5.7: Trapped Charge Calibration Results, presenting the raw array output (above) and the subsequent pixel output distribution (below) at different stages of the calibration. Figure (a) presents the array output after the completion of Step 1 of the calibration, while Figure (b) presents the calibrated response of the array [13] (© 2020 IEEE)

The controller developed in this section serves as the basis for real-time drift calibration in Section 5.5.

5.4 Resolution enhancement using extended time sampling window

Chemical noise remains one of the main challenges for ISFET-based platforms, raising these platforms LoD and limiting its applicability in scenarios where a high resolution on slowly changing reactions is required. For this reason, enhancing noise performance is a crucial chal-

lence with growing importance over the last decade, with various works exploring and validating its nature [9, 14].

The pixel architecture described in Section 3.3 opens up an opportunity for improving the noise performance of ISFET platforms taking advantage of the oscillatory behaviour of the pixel. By sampling the oscillatory PWM signal of the pixel over a temporal window, an N-tap averaging filter is realised where N is defined as:

$$N = \text{floor}\left(\frac{T_{\text{window}}}{T_{\text{PWM}}}\right) \quad (5.1)$$

Where T_{window} represents the temporal length of the window and T_{PWM} the period of the PWM signal generated by the pixel. As thermal noise is uncorrelated and can be removed by averaging, this averaging filter has the potential to lower the LoD of the ISFET pixel by eliminating high-frequency chemical noise contributions. Furthermore, the programmability available on this pixel architecture allows the modification of T_{PWM} by tuning the biasing current I_{Bias} , enabling two degrees of freedom on this resolution enhancement.

5.4.1 Experimental Setup & Results

The validation of our assumption requires consistent testing conditions independent of noise contributions from other non-idealities, such as drift. Furthermore, variations on electrical sensitivity due to changes on I_{Bias} should be accounted for by normalising the results back to the reference electrode, while pH sensitivities are assumed to be independent of I_{Bias} . Lastly, variations in electrical noise due to biasing current I_{Bias} changes should be considered as well. Hence, a 2-step experimental procedure is proposed:

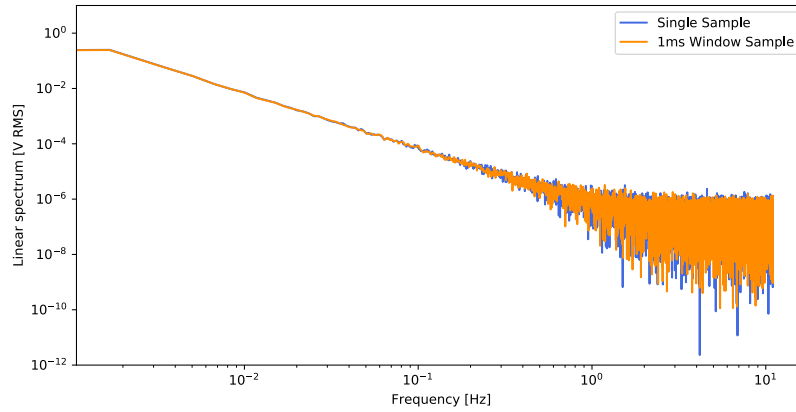
- **Calibration curves for each biasing point:** Calibration curves are obtained for each biasing point under test, calculating the electrical sensitivity under each biasing condition.
- **Simultaneous sampling of noise contributions:** To distinguish the effect of the averaging filter and decouple it from improvements due to electrical noise contributions, a hybrid sampling mechanism is implemented, retrieving a single-period sample and a window-based sample simultaneously. This way, two comparable samples are obtained under identical conditions, and any difference in their Limit-of-detection (LoD) can be attributed to the averaging filter. The exact algorithm is explained in detailed in Appendix B, Figure B.2, illustrating the simultaneous sampling scheme implementation.

As an initial verification, two biasing points were explored at a fixed sampling window of 1ms. Table 5.1 summarises the electrical characteristics of these biasing conditions.

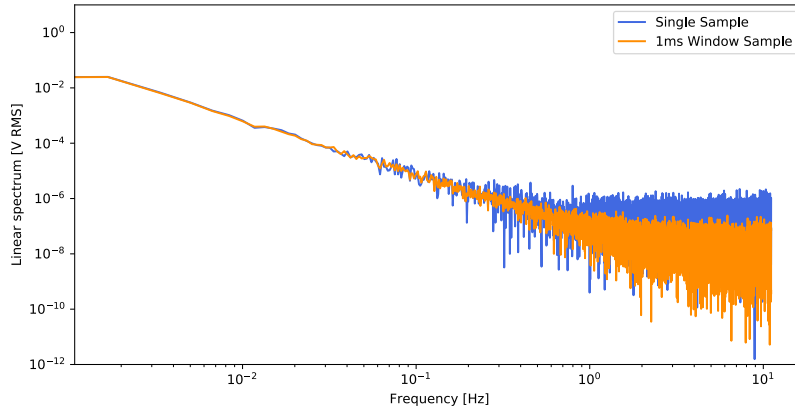
Table 5.1: Electrical characteristics for various biasing conditions

Bias	Elect. Sensitivity	T_{PWM}	Filter Size (N)
0.22 V	-317.5595 %/V	76.384 μs	13
0.31 V	-287.9536 %/V	5.6873 μs	175

The LoD for different biasing conditions was obtained by sampling one single pixel's output over 10 minutes using the simultaneous sampling strategy. Based on the methodology described in Section 3.3, PSD figures for both single sample and window sample were obtained as presented in figures 5.8a & 5.8b. This PSD was integrated from 8 mHz and 10 Hz to obtain the LoD for each sampling strategy.



(a) PSD Figure for a bias of 0.22 V



(b) PSD Figure for a bias of 0.31 V

Figure 5.8: PSD Analysis for different biasing conditions. Blue PSD represents the noise figure calculated from the single sample dataset, and orange PSD represents the 1ms window dataset.

The LoD improvement was evaluated both on absolute value and in percentage to the single-sample LoD baseline, and Table 5.2 summarises these results.

The LoD improvement achieved was 0.02pH, a positive result that falls short of overcoming

Table 5.2: Limit of Detection Results

Bias	Abs. LoD Improvement	Rel. LoD Improvement
0.22 V	0.005850 pH	0.8149 %
0.31 V	0.021868 pH	8.7068 %

the resolution bottleneck. A closer analysis of both PSD graphs and LoD results provides insights into the reasons behind the lack of significant resolution enhancement. The thermal noise achieved on 0.31V biasing - which provides a 175 tap filter - is considerably lower than the single sample one, while the 0.22V biasing thermal noise almost matches its single sample, following the theoretical behaviour. However, the LoD is mainly determined by the flicker noise contribution, which cannot be reduced through an averaging filter. Hence, the attention needs to shift towards techniques that reduce flicker noise to achieve significant improvements on ISFET's LoD, such as the real-time compensation proposed in Section 5.5.

Due to this limitation, this technique was not explored any further.

5.5 Real-time drift compensation for ISFET-based long-term monitoring

The monotonic change present at the ISFET output commonly referred to as drift is one of the most challenging non-idealities introduced during CMOS fabrication. This constant variation pushes the chemical signal outside the ADC input range after a short time (approximately 30 minutes), limiting the use of these arrays for long-term monitoring. Furthermore, this drift is usually indistinguishable from slow ion concentration changes, leading to a poor LoD.

Several solutions have been proposed to address drift limitations. As the reference electrode is an accessible and programmable terminal, it has been previously used on a feedback controller to mitigate drift [15]. However, this mechanism is unsuitable for array configurations where only one reference electrode potential is available and shared by all pixels. Furthermore, the influence of the reference electrode potential over the drift trend should be considered, as any variation on this biasing voltage would modify the drift slope. This influence was postulated by Jamasb et al. [16], who proposed an initial analytical model for this monotonic drift, fitting the trend as an exponential decay function. Using this analytical model, the same authors demonstrated a numerical method to compensate drift based on small sampling windows [17]. However, this method assumes that the concentration change rate is considerably superior to the drift rate, a condition that limits the applicability for long-term monitoring of slow changes. At a device level, Hu et al. presented a reset gate technique that eliminates the accumulated drift and homogenises the response across the array [18, 19], at the expense of leakage. Alternatively, the drift can be reset through calibration, such as the mechanism presented in Moser et al. [9].

However, the slow calibration process and the need for reconstruction mechanisms have limited the applicability of this mechanism.

Hence, for a system to be capable of performing real-time compensation of drift, the compensation mechanism should be designed to fulfil the following criteria:

1. Performs rapid correction, ideally between two consecutive frames
2. Applicable to each pixel individually, as drift can differ significantly from pixel to pixel
3. Avoid reference electrode potential modification, which could potentially modify both the polarity and the rate of the drift
4. Minimise delays on processing and calculation of drift values, along with communications overhead

This section describes the principle of operation of a novel real-time drift compensation technique that fulfils this criterion, along with the obtained results and the potential applications that this technique would enable.

5.5.1 Principle of operation

The real-time drift compensation system utilises the programmability provided by oscillator-based ISFET architectures to encode the chemical information in the input values of the compensating DAC. This compensation is achieved by mirroring the sensing information from the output to the feedback loop of the controller, shifting the ADC requirements from the output to the internal compensating DAC. The drift compensation system is composed of two subsystems that enable its operation. Each subsystem is now described in detail.

Programmable ISFET Array

The dual-sensing array presented in Section 3.3 was designed with several degrees of programmability to enhance the system's adaptation capabilities. This flexibility can be leveraged to implement a real-time drift compensation scheme.

As previously discussed, each pixel in this array is addressed using a set of commands transmitted through an SPI interface. The external controller loads simultaneously the pixel address and the DAC value required for compensation through this interface, enabling pixel-wise operation point programmability. This mechanism was previously used for trapped charge compensation, described in Section 5.3, implementing a Proportional controller that tunes the input voltage

coming from DAC to establish an equilibrium on the input OTA. This controller serves as the basis for real-time drift compensation.

Closed Loop Controller

The compensation algorithm used for mitigating trapped charge effect (Sect. 5.2, Step 2 & Appendix B, Figure B.1b) can run continuously to maintain the output duty cycle at 50 %. This way, any change in the output Duty Cycle reflects in the DAC calibration values at the next frame. Figure 5.9 illustrates this controller.

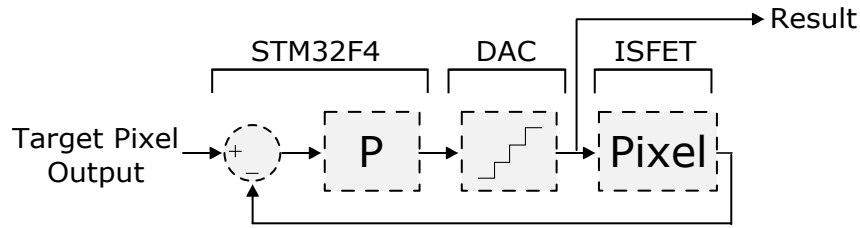


Figure 5.9: Real-Time Drift Compensation Controller Architecture

Using this real-time compensation method, the chemical signal is modulated onto the DAC calibration values instead of onto the PWM signal. Two benefits are obtained from this approach:

- The chemical dynamic range is expanded without the need to complex and power/area-hungry large-input ADC and without introducing modulation at the floating gate. The ADC values are no longer tied to the limited dynamic range of the linear OTA - 0.2025 V as per Sect. 3.3 - but to the entire operation range of the input NMOS - approximately 1.4V in TSMC 0.18 μm .
- Cross-sensitivity from chemical information to the thermal information is minimised, as the PWM output is maintained constant around 50 %. This phenomenon enables simultaneous chemical and thermal acquisition.

5.5.2 Experimental Results

The proposed drift compensation mechanism was tested under various conditions to validate these long-term monitoring claims while preserving pH sensitivity.

Electrical Sensitivity Analysis

The ISFET electrical sensitivity using our real-time compensation mechanism was evaluated by immersing the dual-sensing ISFET array described in Section 3.3 in pH 7, creating potential

steps with the Ag/AgCl Reference Electrode. Figure 5.10 presents the results of this experiment, showing the evolution of each pixel output along with the average response highlighted in black.

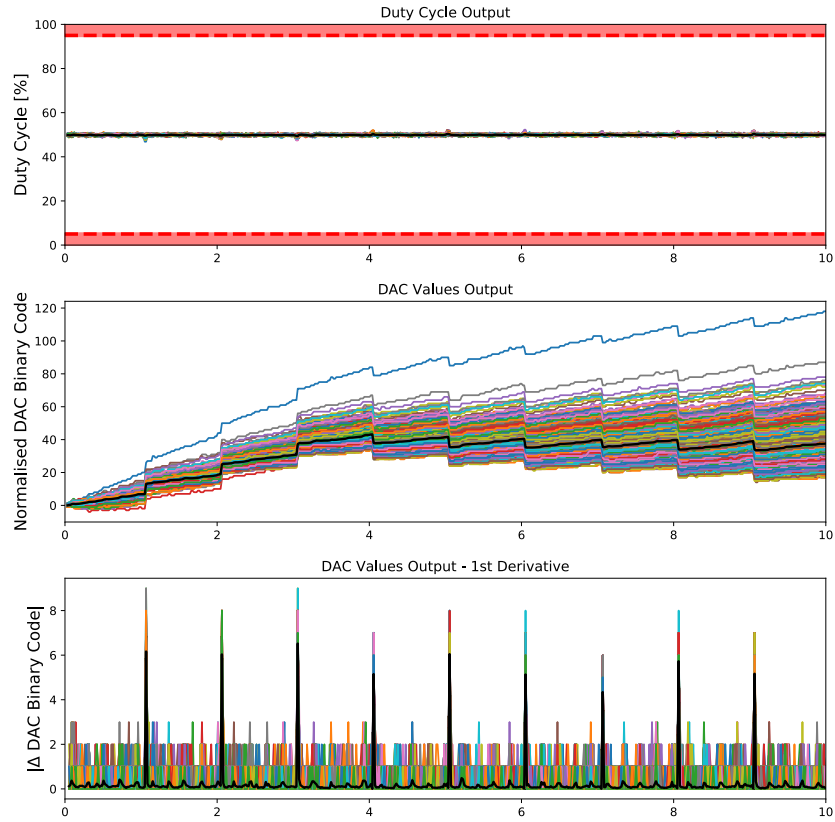


Figure 5.10: Electrical Sensitivity using Real-Time Drift Compensation

The DAC value changes due to the Reference Electrode could be distinguished by inspection, yielding an electrical sensitivity of 474 DAC counts/V and a capacitive attenuation of 0.42, a result in line with the ones presented in Section 3.3.5 and reported in [13].

pH Sensitivity Analysis

After confirming that the architecture remains electrically sensitive, its chemical sensitivity was evaluated. For this purpose, the chip surface was exposed to deionised water (pH 5.375), and drops of 10 μl of NaOH were added to the solution, changing the pH. Figure 5.11 presents the resulting curve, showing the evolution of each pixel output along with the average response highlighted in black. This analysis yielded a pH sensitivity of 13.66 mV/pH, which follows the results reported in [13], and confirms that pH reactions can be monitored using real-time drift compensation.

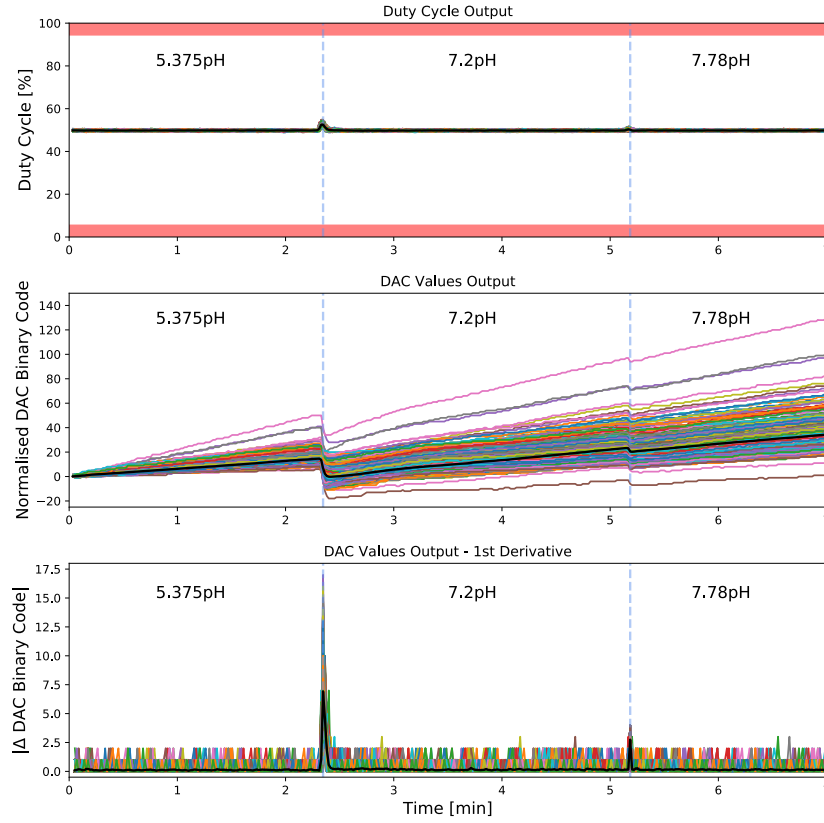


Figure 5.11: Chemical Sensitivity using Real-Time Drift Compensation

Long-term Monitoring - 36 hours

One of the main benefits of this real-time compensation is the relaxation of the dynamic range requirements, shifting the burden away from the output ADC. To quantify this phenomenon, both uncompensated and compensated configurations were assessed by exposing the ISFET array to deionised water for long periods of time, quantifying the number of pixels in range. Before starting this experiment, the ISFET array was calibrated to ensure all pixels were operating at the optimal biasing conditions. Figures 5.12 and 5.13 present the results from these two experiments, showing 1 hour using no drift compensation and 36 hours compensating drift in real-time. Table 5.3 analyses the active pixels with both experiments upon completion, validating the suitability of real-time drift compensation for long-term monitoring.

Table 5.3: Long-term Monitoring Results

Experiments	# of Active Pixels	% of Active Pixels
1 hour without real-time compensation	80	7.8125 %
36 hours with real-time compensation	1017	99.3164 %

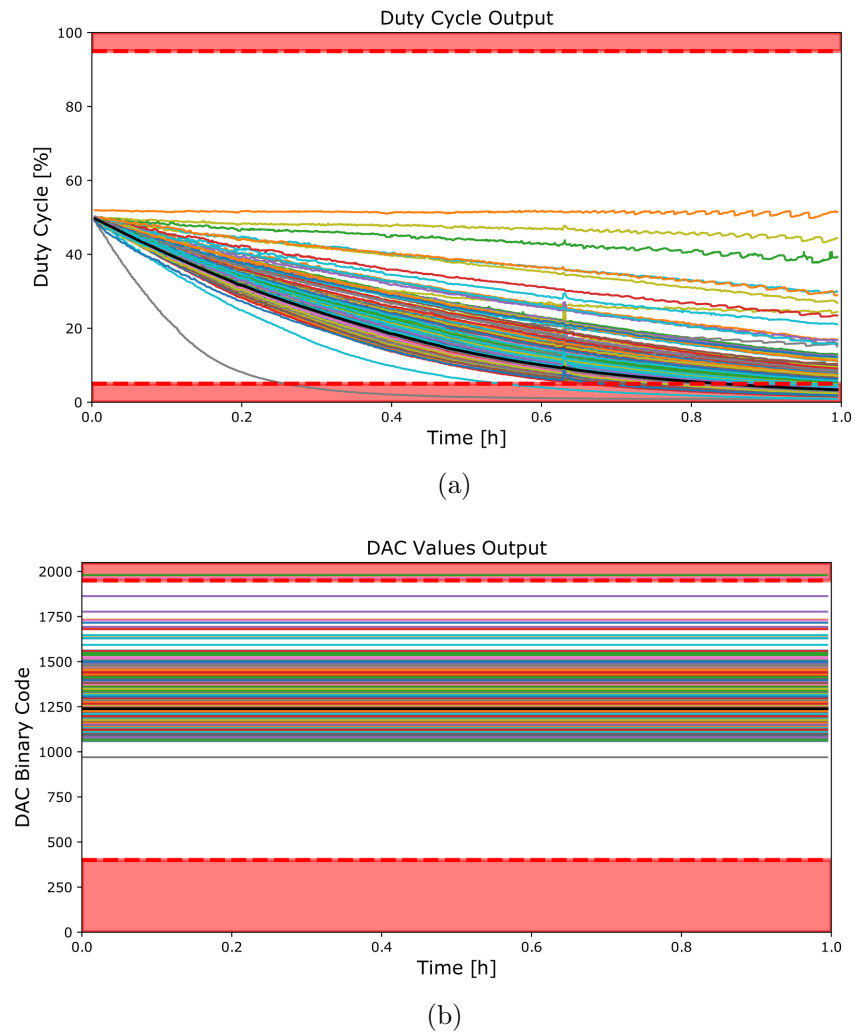


Figure 5.12: Long-Term Monitoring Analysis without Real-Time Compensation. Figure (a) presents the Duty Cycle results, while Figure (b) presents the DAC values used throughout 1 hour

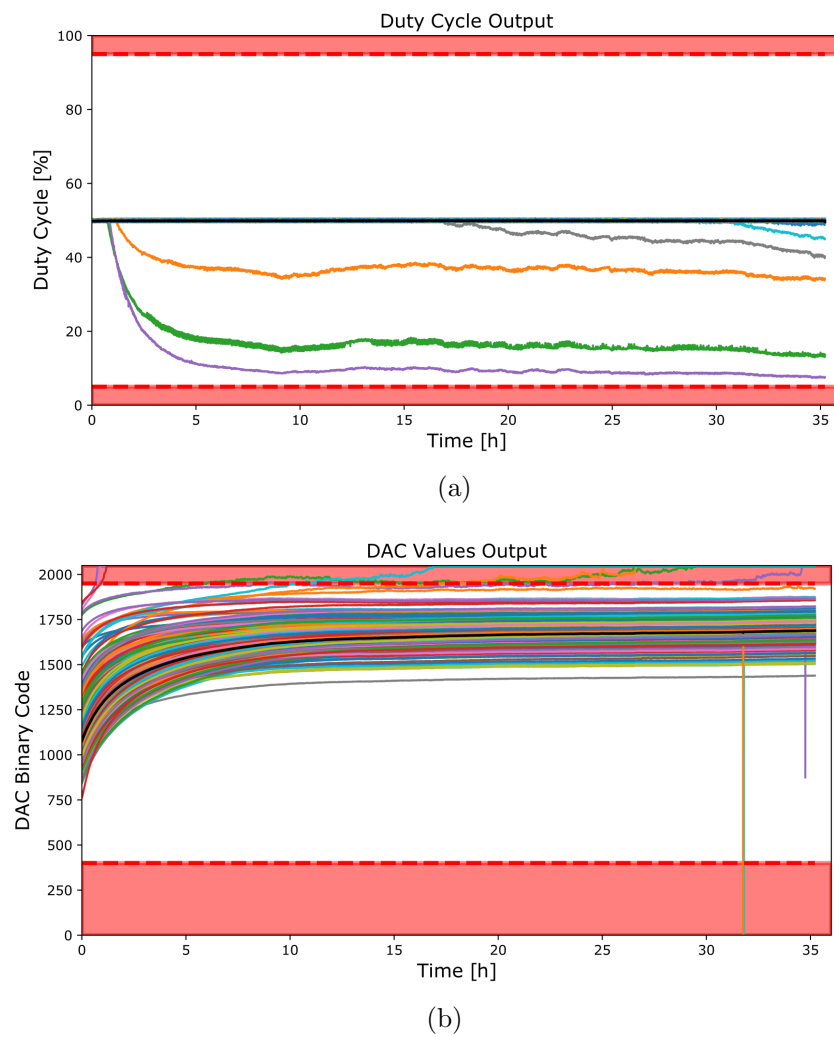


Figure 5.13: Long-Term Monitoring Analysis with Real-Time Compensation. Figure (a) presents the Duty Cycle results, while Figure (b) presents the DAC values used throughout 36 hour

Drift Modelling and Forecasting

Beyond the highlighted sensing benefits, this long-term monitoring provides large datasets that can unveil further insights on drift evolution, opening the doors for predictive models that forecast drift trends. This section presents an initial validation for such models, using the 36 hours monitoring dataset.

Following the physical model proposed by Jamasb et al. [16], monotonic drift with a constant reference electrode potential would follow an exponential trend, as per Eq. 5.2

$$\Delta V_G(t) = -(Q_D + Q_I + Q_{inv}) \left(\frac{\varepsilon_{ins} - \varepsilon_{SL}}{\varepsilon_{ins} \cdot \varepsilon_{SL}} \right) \cdot x_{SL}(\infty) \cdot (1 - \exp[-(t/\tau)^\beta]) \quad (5.2)$$

where Q_D and Q_{inv} represents the charge stored in the depletion layer and the inversion charge, and Q_I models the effective charge induced in the ISFET sensitive layer per unit area. Furthermore, ε_{SL} and ε_{ins} represent the dielectric constant of both the chemically-modified surface after solution exposure and the native pH-sensitive insulator (Si_3N_4 in our case), $x_{SL}(\infty)$ is the final thickness modified by the solution and τ , and β are fitting-specific parameters derived from Fick's first law of diffusion [16].

Using this equation and the initial parameters proposed by Jamash et al. [16, 20], the dataset obtained during our 36 hours experiment can serve as a training set to forecast the drift's trend. This process was performed in two steps: firstly, the model's validity was assessed using the full 36 hours dataset to fit the model, followed by a 24-hours/12-hours data split for training/validation with a forecast of 160 hours. Figures 5.14 and 5.15 provide these results, illustrating the fitting on three independent pixels. The following conclusions can be drawn from these preliminary results:

1. **Validated drift exponential model beyond initial scope [16]:** The initial model was evaluated on standalone ISFET sensors fabricated through a custom fabrication process. The results presented in this thesis validate the model for ISFET implemented on standard CMOS technology while expanding its validity beyond 12 hours.
2. **Potential for drift forecasting:** The proposed curve-fitting approach has the potential to enable real-time drift forecast. For seizing this opportunity, large datasets sensing long-term drift evolution should be acquired. The real-time compensation mechanism catalyses this opportunity.
3. **Light influence on drift trend:** The light's influence on the drift model is reflected on the fitting, especially significant on the last few hours of the sample that matched the sunrise. This might be due to a modification on the sensing surface sensitivity due to

photon interaction, enabled in this case by sunlight. However, this dataset provides only anecdotal evidence, and further experimentation would be required to establish a clear correlation.

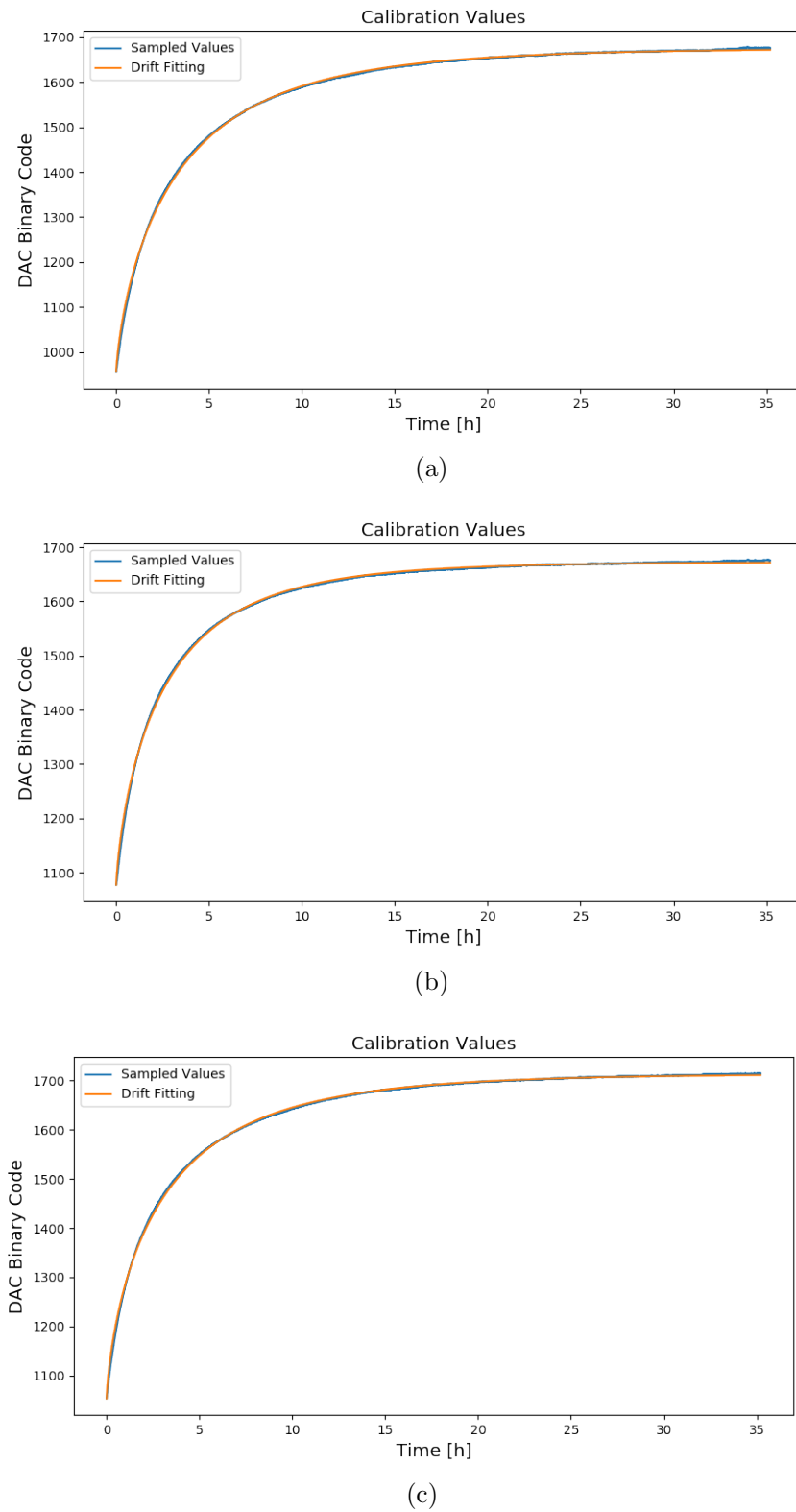
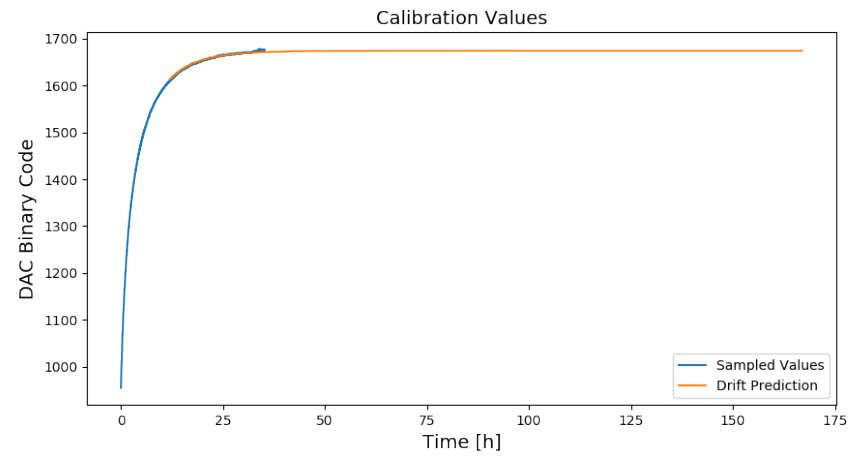
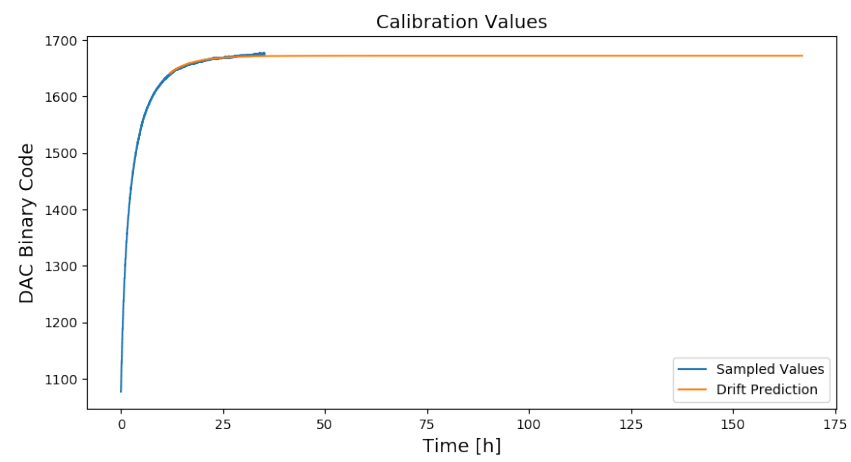


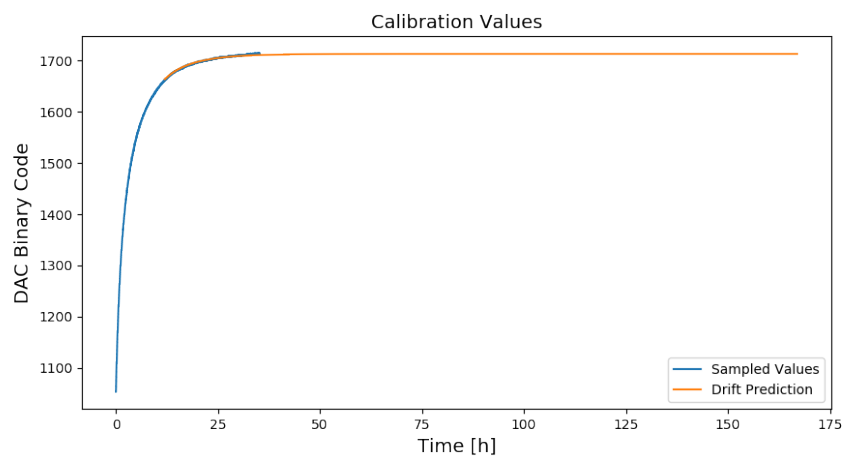
Figure 5.14: 36-Hour Exponential Fitting using model presented in [16]. Each curve represents the fitting of one pixel



(a)



(b)



(c)

Figure 5.15: 160-Hour Exponential Fitting using model presented in [16], predicting the drift forecast for 160 hours. Each curve represents the fitting of one pixel

These results open new horizons on our understanding of drift, moving from a reactive approach focused on post-processing drift removal to a proactive strategy that forecasts and predicts drift slope based on long-term datasets. Furthermore, the influence of external conditions on drift evolution highlights the need for multi-sensing platforms that provide the sensing capabilities to decouple the various phenomena affecting the sensing environment. However, I would like to highlight that these sensing elements and compensation mechanisms target only the mitigation of non-ideal effects created at the sensing surface, adding complexity to avoid surface modification. Ideal solutions would tackle the problem at its root - the electrochemical interaction with the sensing surface.

The acquisition of long-term datasets and the study of the light influence remains future work for this thesis due to shortages in the number of dual-sensing ISFET arrays after the 36-hours test.

5.6 Summary

This chapter addressed the need for software methods that enable compensation or mitigation of ISFET non-idealities. To catalyse the development of these methodologies and the acquisition of reproducible results at the Point-of-Care, this chapter presented “instantDNA”, a novel portable platform that couples a custom PCB for ISFET sensing acquisition with a Raspberry Pi that provides computational capabilities and intuitive user experience through a touchscreen. This prototype was presented at the Biomedical Circuits and Systems Conference 2019 (BioCAS 2019) on the demonstration session, achieving the Best Demo Award BioCAS 2019.

Leveraging on the versatility of this platform and the programmability by the dual-sensing ISFET array (Sect. 3.3), I presented three computational methods that aim to overcome the main limitations of ISFET arrays: trapped charge and noise, usually associated with monotonic drift. Firstly, a fast and accurate trapped charge compensation mechanism was proposed, yielding rapid full-array compensation through an optimisation algorithm that combines optimal reference electrode biasing and internal compensation through on-chip DAC.

Secondly, the dual-sensing programmability and intrinsic oscillatory behaviour were exploited to explore noise performance improvement through a window-based filter, reducing the thermal noise. Unfortunately, its flicker noise remained ISFET’s LoD bottleneck, highly influenced by the monotonic drift, making this method unsuitable for LoD enhancement.

Based on these results, the attention turned to drift compensation in an attempt to overcome flicker noise. For this purpose, I presented a real-time compensation mechanism that enabled long-term monitoring by shifting the dynamic range requirements away from the ADC. This software method remained sensitive to electrical potentials and ions variations and achieved

continuous monitoring of at least 36 hours with over 99% pixel in range. This analysis also validated drift models beyond their initial scope and opened the doors for large datasets acquisition that enable predictive drift analysis.

In the next section, Data-driven algorithms and Information-based approaches are explored, both on ISFET sensing and beyond, demonstrating its potential to revolutionise PoC diagnosis.

5.7 Publications

Several publications arose from the content of this chapter.

- [12] M. Cacho-Soblechero et al. “Live Demonstration: A Portable ISFET Platform for PoC Diagnosis Powered by Solar Energy”. In: *BioCAS 2019 - Biomedical Circuits and Systems Conference, Proceedings* 2018.99 (2019), p. 1 - **Best Demo Award BioCAS 2019**
- [13] M. Cacho-Soblechero et al. “A Dual-Sensing Thermo-Chemical ISFET Array for DNA-Based Diagnostics”. In: *IEEE Transactions on Biomedical Circuits and Systems* 14.3 (2020), pp. 477–489.
- [21] S. Karolcik, M. Cacho-Soblechero et al. “A high-performance raspberry Pi-based interface for ion imaging using ISFET arrays”. In: *IEEE Sensors Journal* 20.21 (2020), pp. 12837-12847.

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- [1] N. Moser et al. “Live Demonstration : A CMOS-Based ISFET Array for Rapid Diagnosis of the Zika Virus”. In: *2017 IEEE International Symposium on Circuits and Systems (ISCAS)* June 2016 (2017).
- [2] A. Au et al. “Live Demonstration: A Mobile Diagnostic System for Rapid Detection and Tracking of Infectious Diseases”. In: *Proceedings - IEEE International Symposium on Circuits and Systems* 2018-May.99 (2018), p. 1.
- [3] S. Karolcik, N. Miscourides, and P. Georgiou. “Live demonstration: A portable high-speed ion-imaging platform using a raspberry Pi”. In: *Proceedings - IEEE International Symposium on Circuits and Systems* 2016 (2019), p. 2830.
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- [12] M. Cacho-Soblechero et al. “Live Demonstration: A Portable ISFET Platform for PoC Diagnosis Powered by Solar Energy”. In: *BioCAS 2019 - Biomedical Circuits and Systems Conference, Proceedings* 2018.99 (2019), p. 1.
- [13] M. Cacho-Soblechero et al. “A Dual-Sensing Thermo-Chemical ISFET Array for DNA-Based Diagnostics”. In: *IEEE Transactions on Biomedical Circuits and Systems* 14.3 (2020), pp. 477–489.
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Chapter 6

Software Opportunities for ISFET Sensing and beyond

6.1 Algorithmic methods on e-Health Solutions

PoCT devices require minimally trained personnel to achieve a reliable diagnosis, favouring solutions that provide automated results without the need for the clinician’s interpretation. In this context, smart data-driven algorithmic methods applied to PoC sensing have flourished in the literature over the past few years, enhancing sensing capabilities and enabling accurate pathogen detection, quantification and multiplexing. These methods have leverage the availability of bench-top instrumentation datasets [1, 2] to enhance multiplexing capabilities using a data-driven approach. Furthermore, these methods are incorporated in paper-based portable PoCT, inferring analyte concentration on multiplexed sensing channels using data-driven models [3]; or on wearable platforms, enabling real-time muscle-fatigue forecasting using surface electromyography (sEMG) [4]; to name a few.

Simultaneously, the exponential increase of data generated by IoT devices is making increasingly urgent a shift from cloud processing to edge processing [5–7]. In this context, the proposed “Diagnosis-on-a-Chip” represents a timely solution for ISFET PoCT platforms, enabling the deployment of AI models close to the sensing source.

This chapter explores various synergies between Data-Driven algorithmic methods and Biomedical Electronics with the potential to be deployed at the Point-of-Care, both on ISFET diagnostic platforms and wearable technologies. These synergies investigated target two key areas:

- **Data Transmission and Storage:** The need for large datasets for AI training on e-Health is driving the development of ubiquitous sensors, whose data need to be trans-

mitted and stored. ISFET technology has recently experienced a similar trend, with the design of ultra-high frame rate ion imagers [8–10]. These imagers require high-bandwidth interfaces and large drive storage to enable the real-time analysis of chemical images. This chapter explores data compression opportunities using commonly used image compression algorithms, optimising its parameters to enhance performance based on ISFET images distinct features.

- **From Data-harvesting to Information-sensing:** Differences in frequency response between raw data and features extracted for predictive models have the potential to enable relaxation of sampling requirements by achieving analogue feature extraction, improving power efficiency while enabling further parallelism. One of the most relevant examples of this is sEMG wearable platforms, where channel scalability is capped by Nyquist frequency. Hence, this chapter presents a 4-channel sEMG system with on-chip feature extraction to enable a validation analysis of the Information-focused paradigm.

This section analyses these two solutions in detail.

6.2 JPEG Deployment and Optimisation for Chemical Image Compression ¹

A wide range of ultra-high frame rate architectures have been developed [9–12] since high-resolution, high frame rate ISFET arrays were initially envisioned by Zeng et al. in 2018 [8]. These platforms target the acquisition of novel insights on ion dynamics, relying on FPGA-based platforms with high-bandwidth transmission protocols such as PCI-Express or USB 3.0 to transfer the large datasets generated. Based on bulky components with high power consumption, this architecture is limiting its applicability at the Point-of-Care. Moreover, the architectures targeting higher frame rates, peaking now at over 6000 frames/s [13], require significant storage to enable real-time ion diffusion analysis - one minute of data requires over 45 Gb. These strict storage requirements further challenge its portability. This section proposes and implements a customised compression for ISFET imagers to overcome these limitations.

6.2.1 Introduction to Image Compression

In 1972, the computer scientist Nasir Ahmed published a landmark paper with the title “Discrete Cosine Transform” [14, 15] which set the basis for modern image compression algorithms.

¹The proposed solution was achieved in collaboration with Junming Zeng and Lei Kuang, fellow PhD students at Imperial College London

Based on this Discrete Cosine Transform (DCT), in 1992, the Joint Photographic Experts Group (JPEG) proposed one of the most popular lossy compression algorithms, JPEG, which catalysed the proliferation of digital images over the past few decades [16].

Image compression aims to eliminate redundant and superfluous information from the original picture [17]. Image compression algorithms are classified based on the integrity of the compressed data:

- **Lossless Compression Methods:** These compression methods apply mathematical transformations to the image while preserving its integrity. The image recovered after decompression is identical to the pre-compressed one. Examples of lossless algorithms are Run-Length Encoding, Lossless Predictive Coding or Multi-resolution Coding, which are applied to lossless formats such as BMP [18], PNG [19] or TIFF. Usually, these algorithms tend to achieve smaller compression ratios than lossy compression methods.
- **Lossy Compression Methods:** These compression methods exploit redundancies in the data to reduce the required information to store and reconstruct it. These redundancies are usually unveiled by transforming the data onto a different domain, applying transformations such as the DCT [14]. Lossy compression algorithms trade image quality with compression ratio. Examples of these algorithms are the already mentioned JPEG [16] and its more recent update, JPEG-2000 [20].

Large ISFET imagers generate images comparable to low-resolution photon-generated images, becoming suitable candidates for size reduction using image compression algorithms while optimising its specific features. This section explores the validity of this assumption, applying one of the most popular and widely supported compression algorithms: JPEG.

6.2.2 JPEG Architecture

JPEG compression format is a lossy compression method that leverages the coefficient distribution of the image DCT transformation. The image information is usually concentrated on the low-frequency coefficients, while high-frequency coefficients remain less significant for image reconstruction. Hence, these high-frequency coefficients can be discarded to reduce the bit-rate while minimally impacting the image quality. The steps to perform JPEG compression, illustrated in Figure 6.1, are the following:

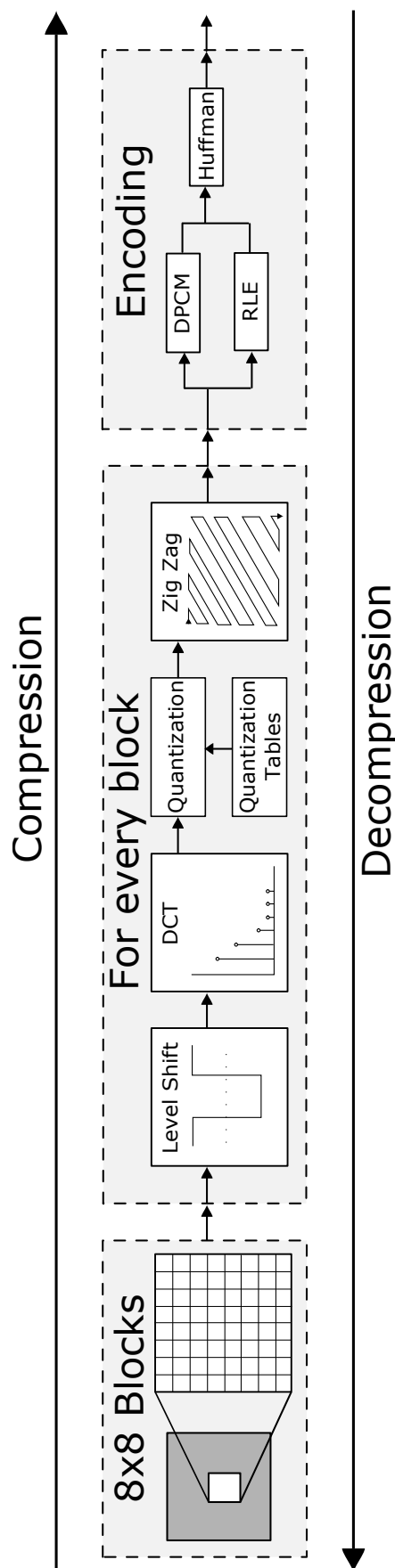


Figure 6.1: JPEG Compression and Decompression Architecture

1. **Extract Minimum Coded Unit:** Divide the target image in blocks of 8x8 pixels. For each block, perform actions 2 to 5.
2. **Level Shift:** Center the pixel values around zero, ranging now from -128 to 127
3. **Perform the Discrete Cosine Transform:** Obtain the DCT coefficients by performing the 8x8 DCT transform to the target block.
4. **Quantization:** Multiply the DCT coefficients by a pre-defined quantization table, rounding the result. This table sets the image quality, establishing the trade-off between Compression Ratio (CS) and Peak-Signal-to-Noise Ratio (PSNR)
5. **Zig-Zag Encoding:** Re-position the coefficients to optimise subsequent encoding.
6. **Lossless Encoding:** Further encode each block's coefficients using lossless techniques
 - **DPCM Encoding:** Encode DC Components using Differential Pulse-Code Modulation (DPCM)
 - **RLE:** Encode AC Components using Run-Length Modulation Encoding
7. **Huffman Encoding:** Further encode the resulting bitstream using an Entropy encoding, such as Huffman encoding [21].

JPEG files decompression follows the same steps in reverse order: Reverse encoding, unquantize based on quantisation tables, perform the Inverse DCT and unshift the data, and finally retrieve the compressed version of the original image.

The JPEG algorithm “quality level” or “compression level” is determined by the input image and the selected quantisation tables. JPEG specifications provide a set of quantisation tables that are used as the benchmark for balanced compression, targeting generic images. However, these tables can potentially be adjusted to the input images' specific characteristics. The methodology proposed and implemented in this thesis leverages this flexibility to tailor quantisation tables to ISFET arrays, optimising the compression parameters for ion imagers. These chemical imagers generate sparse frames, with fast variations due to noise that could be potentially eliminated and slow variations across the array where reactions are occurring. Hence, quantisation tables can be created to leverage these peculiarities and further increase the compression ratio without degrading image quality. To achieve this, the optimisation uses the data generated from our state-of-the-art ultra-high frame rate Lab-on-Chip platform, described in the next section.

6.2.3 Real-Time Lab-on-Chip Platform

The data used for the JPEG encoder optimisation was obtained through a Real-Time Lab-on-Chip platform for ultra-high frame rate ISFET arrays, developed at the Centre for Bio-Inspired Technology by my fellow PhD candidates Junming Zeng and Lei Kuang. The platform, illustrated in Figure 6.2 is composed by:

- **Ultra-High Frame Rate ISFET Array:** Chemical information is acquired through a current mode 128x128 ISFET array, with a peak frame rate of over 6000 frames/s thanks to its column-parallel ADC strategy.
- **Custom PCB:** The ISFET array is inserted into a custom PCB that provides biasing signals and LVDS connectivity.
- **FPGA Dev Board:** A Xilinx VCU118 FPGA Development board is used for data processing and transmission
- **USB 3.0 Dev Board:** An FTDI FT601 Development board is connected to the FPGA to provide connectivity to a PC, where the data is displayed and stored.

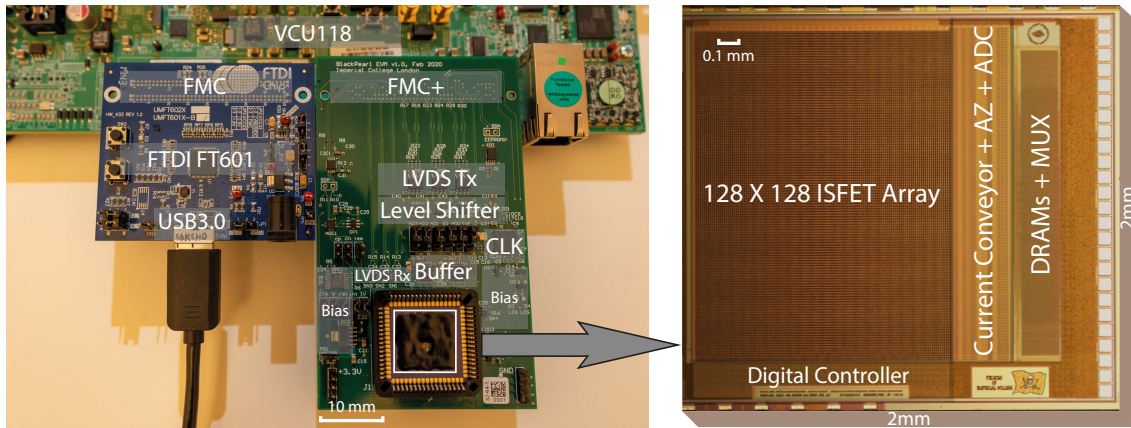


Figure 6.2: Real-Time Lab-on-Chip Platform, as presented in [13] (© 2021 IEEE)

A high-speed ion diffusion reaction was acquired using this platform to develop an optimal JPEG encoder for ISFET arrays.

6.2.4 A Bio-Inspired JPEG Compression Optimization

Standard JPEG quantisation tables were designed for photon-mediated digital images and empirically determined based on human perception, leading to a sub-optimal performance on

chemical images. The chemical images' distinct characteristics open the opportunity for tailored quantisation tables, allowing the compression optimisation based on a set of ISFET frames to boost its bit-rate performance with minimal quality loss.

Problem Definition

The problem of quantization tables optimisation can be mathematically formulated as follows [22]. Given a quantization table:

$$Q = \{Q_k : k = 0, 1, \dots, 63\} \quad (6.1)$$

both bit rate (R) and distortion (D) can be defined as the corresponding rate-distortion ratio on each block:

$$D = \sum_{n=1}^{NumBlocks} \sum_{k=0}^{63} D_{n,k}(Q_k) \quad (6.2)$$

$$R = \sum_{n=1}^{NumBlocks} R_n(Q) \quad (6.3)$$

being *NumBlocks* the number of results 8x8 blocks of the target image, $D_{n,k}$ the distortion on block n of index k, and R_n the bit-rate at the block n with the quantisation Q.

The JPEG quantization tables optimisation problem can be then defined as a constrained optimisation problem as follows:

$$\begin{aligned} \min\{D(Q), R(Q)\} \quad & \text{subject to} \\ D(Q) & \leq D(Q_{JPEG50}) \\ R(Q) & \leq R(Q_{JPEG50}) \end{aligned} \quad (6.4)$$

Hence, this optimisation problem targets the minimisation of both distortion and bit-rate based on an optimised quantisation table Q, subject that the rate-distortion ratio remains balanced - this is, without sacrificing neither distortion nor rate.

Peak-Signal-to-Noise Ratio (PSNR) measures this distortion, and the resulting Compression Ratio (CR) quantifies the bit-rate generated. Based on these two metrics, a single-output

score function enforces PSNR and CR improvement while providing a quantifiable performance metric for optimisation algorithms, as illustrated in Figure 6.3.

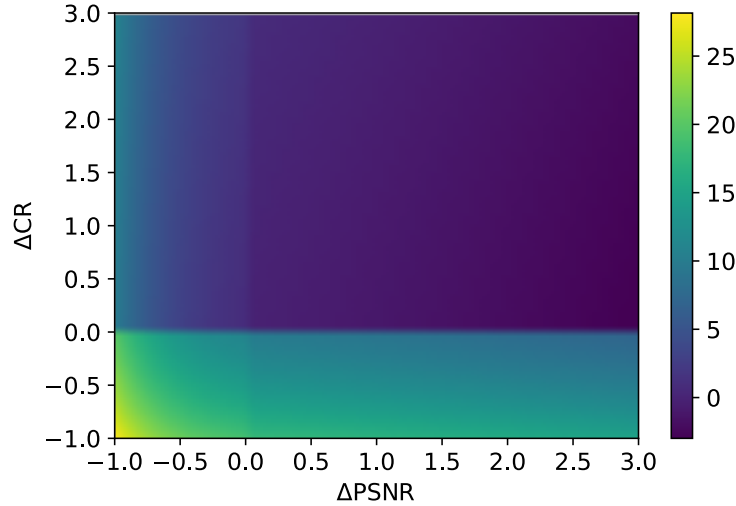


Figure 6.3: Optimisation function results on a ΔPSNR and ΔCR space

Optimisation Algorithm

The defined optimisation problem has many sub-optimal solutions at the rate-distortion space, limiting the applicability of Gradient-Descent algorithms as it would likely settle on local minima.

In this context, Evolutionary Algorithms have been adopted as a promising solution due to their bio-inspired population-based metaheuristic approach that enables global optimisation on a solution space with multiple local minima. These algorithms, inspired in stochastic phenomena present in nature, have been previously used for JPEG optimisation on standard images: Cultural Algorithms (CA) [23], Genetic Algorithms (GA) [24], and Particle Swarm Optimisation (PSO) [25] have shown promising results. This work implements PSO for quantisation table optimisation.

Particle Swarm Optimisation [26] is inspired by particle dynamics to solve the target minimisation problem. Each possible solution, represented as a particle on the search-space, is influenced by its initial state, its best local solution and the global best solution found by any particle. The position, direction, and velocity of these particles are recalculated on each iteration, leading to the optimal global solution.

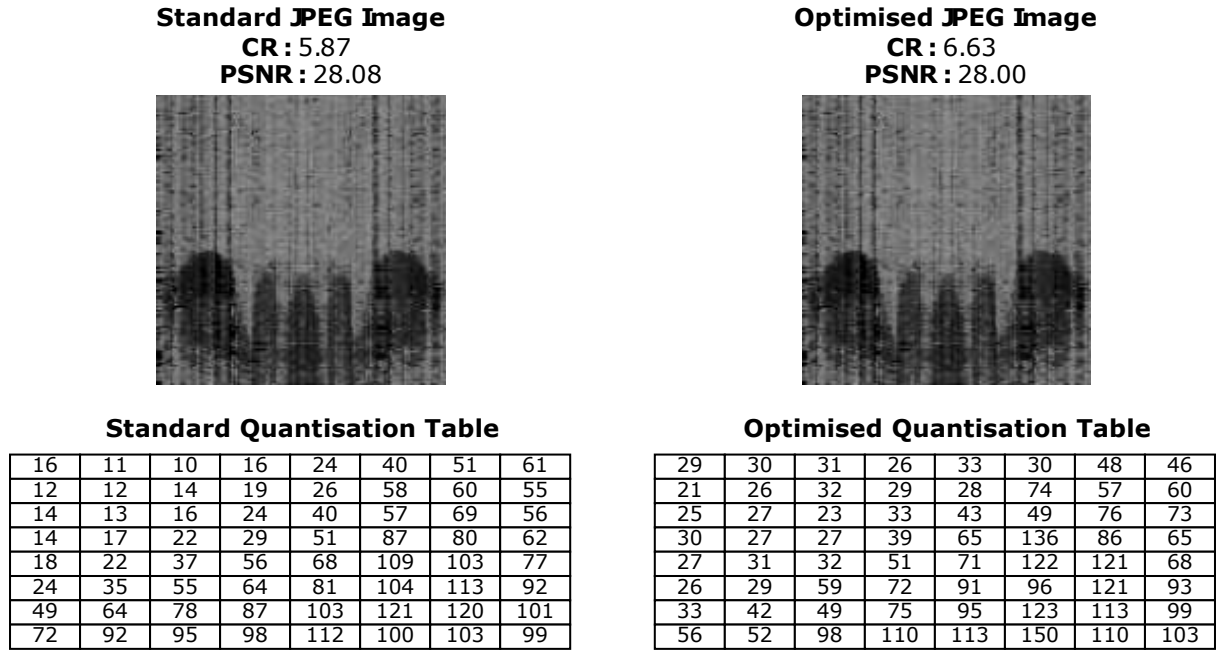


Figure 6.4: Particle Swarm Optimisation Results, showing a comparison between an image compressed on standard JPEG and optimised JPEG. Both quantization tables Q_{50} and Q_{Opt} are provided [13] (© 2021 IEEE)

Table 6.1: Optimisation Result Summary [13] (© 2021 IEEE)

	Compression Ratio			PSNR		
	Average	Variation ($\Delta\%$)	Std. Deviation	Average	Variation (Δ dB)	Std. Deviation
Standard JPEG Q_{50}	5.88	-	0.32	28.08 dB	-	0.37 dB
Optimised JPEG Q_{Opt}	6.63	+ 13.03%	0.39	28.00 dB	-0.08 dB	0.33 dB

6.2.5 Results

From the dataset provided for this optimisation, four frames were randomly selected to ensure that the generated score can be generalised across images. On each iteration, the scores of each image were calculated and averaged.

Assuming the standard JPEG quantisation table (Q_{50}) as the closest available solution to the global minima, the particles were randomly initialised on the surrounding search space. Two hundred particles were generated, simulating its dynamics for 150 iterations and preserving the best-known solution. The stochastic influence was controlled by balancing the acceleration coefficients, usually referred to as nostalgia ($c1 = 0.5$) and envy ($c2 = 0.3$). Quantisation table ranges added an additional constrain to the solution, as their ranges must remain between 1 and 255.

Figure 6.4 presents the comparison between standard (Q_{50}) and optimised (Q_{Opt}) JPEG quantisation tables results, showing an example image along with the average performance obtained.

Table 6.1 summarises this performance, showing an improvement on Compression Ratio of 13.03% compared with standard JPEG compression, with minimal quality loss (-0.08 dB). This performance was consistent across frames, illustrated by a standard deviation in line with the standard JPEG one.

The optimisation of the JPEG compression algorithm partially alleviates the transmission bottleneck, which is especially remarkable when scaling to large and dense arrays. This optimisation decreases the storage and the communication requirements for ultra-high frame rate ion imagers by reducing the bit rate without any additional hardware overhead or extra compression protocol and minimally decreasing the image quality. To the best of our knowledge, this represents the first optimisation of standard compression algorithms targeting ISFET-generated chemical images, demonstrating the improvement potential of current compression algorithms on chemical imagers.

Despite these compression's positive results, the CR improvement achieved is insufficient to trigger a change in the transmission interface required to transmit ultra-high frame rate ISFET images, still relying on high-speed interfaces. Hence, as future work, the distortion value could be modified to better represent the content of the image: instead of the PSNR used in this work, the distortion could be measured as the detection accuracy of an ML algorithm in charge of detecting the chemical reaction. This methodology would pave the way for next-gen customised compression protocols that benefit from the unique features of ISFET ion imaging to achieve significant gain in bit-rate. Furthermore, leveraging the small frame-to-frame variations achieved through ultra-high frame-rate, protocols aiming with spatio-temporal compression can be implemented on-chip to achieve further compression, such as MPEG [27]. Such compression algorithms, in order to operate in real time, will require system-level integration with dedicated video compression blocks, following a similar trend than the one observed in CMOS system [28–30].

6.3 4-Channels sEMG Architecture with On-Chip Feature Extraction

The emerging demand for highly parallel interfaces with multiple channels operating simultaneously for Point-of-Care diagnosis has revived the interest in Analog-to-Information converters capable of performing feature extraction at the edge [31, 32]. These architectures aim to alleviate the sampling bottleneck by extracting information before digitisation. In synergy with the accelerated integration of data-driven predictive algorithms on biomedical applications, this trend represents an exciting opportunity for developing alternative front-end strategies based on the detection of target-specific events. In this section, I explore the real-time monitoring

of Low Back Pain at the Point-of-Care using Surface Electromyography as a use case of this opportunity.

Low Back Pain (LBP) is one of the most common musculoskeletal conditions, affecting over 500 million patients across the globe [33, 34]. Truck muscles fatigue levels have been previously linked with the development of LBP [35], opening the possibility of early detection of LBP progression through the continuous monitoring of early symptoms. However, LBP real-time monitoring in a wearable manner has been constrained by the physiological structure of low back muscles, requiring simultaneous monitoring of multiple spatial points to assess the muscle status.

In this context, Surface Electromyography (sEMG) has risen as a promising technique to achieve real-time fatigue analysis at the PoC.

6.3.1 From Data-Harvesting to Information-Focused: a novel approach for sEMG architectures ²

Surface Electromyography (sEMG) is an electrophysiological technique that measures the biopotentials generated during muscle contraction [36]. This technique has raised significant clinical interest, with applications ranging from muscle fatigue monitoring [37–39] and forecasting [4], to motor disability rehabilitation [40] or sEMG-based pattern recognition and gait analysis [41]. These applications rely on a multi-channel acquisition, obtaining sEMG signals from various spatial points to reconstruct muscle activity, requiring large arrays of electrodes and parallel front-end strategies to process them simultaneously.

Over the last decade, sEMG has been coupled with CMOS technology to achieve instrumentation miniaturisation, channel parallelism and minimal power consumption, enabling its integration on portable and wearable platforms to provide real-time data in a wireless fashion [38, 42, 43]. These platforms can enhance patient compliance and technology adoption, generating larger datasets that can provide further clinical insights.

The requirement of large datasets generated by the sEMG acquisition platforms, gathering data from many muscle fibres simultaneously, challenges the limits of sEMG front-end scalability. The expansion in the number of channels has been previously solved by increasing the number of parallel ADCs, which leads to a larger silicon area and higher power consumption, limiting its portability and wearability. ADC-sharing sensing schemes have been previously proposed [44] to alleviate this problem, but the number of channels shared by a single ADC is bounded by Nyquist frequency, which for sEMG signals is 1 kHz.

²The circuit and simulations presented in this section were designed and performed by Wei Tu under the direct supervision of Dan-Emanuel Terracina Barcas and Miguel Cacho Soblechero.

Recent data-driven predictive algorithms generated based on sEMG signals have proposed specific features used to analyse and forecast muscle fatigue evolution [41]. These features, such as Root Mean Square (RMS) and Zero Crossing (ZC), can be mathematically represented as shown in Eq. 6.5 and 6.6.

$$RMS = \sqrt{\frac{1}{N} \sum_{n=1}^N y_n^2} \quad (6.5)$$

$$ZC = \sum_{n=1}^N |sign(y_n) - sign(y_{n-1})| \quad (6.6)$$

The temporal evolution of these features correlates with muscle fatigue, whose variations occur within minutes [45]. Hence, there is an opportunity for extracting these features on-chip before digitalisation, potentially relaxing the sEMG signal sampling requirements and enhancing this way channel parallelism. This solution would effectively reduce the need for data sampling, focusing only on extracting the underlying information provided by the sEMG.

This section presents a 4-channels sEMG Front-End with in-built feature extraction, enabling the simultaneous acquisition of raw sEMG data and two fatigue features, sEMG envelope for RMS and Zero Crossing. This platform would serve as the initial evaluation platform for the proposed change in paradigm, transitioning from a data-harvesting approach to an information-focused strategy. The following subsections present the architecture of the system and the preliminary results obtained from system simulation.

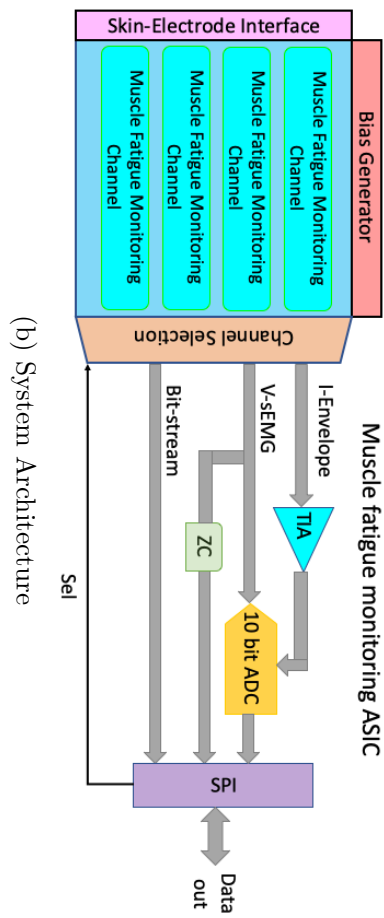
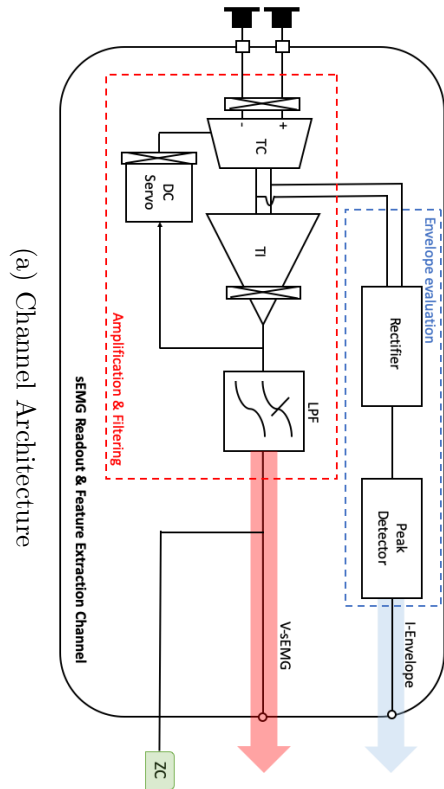


Figure 6.5: High Level Architecture of the proposed sEMG sensing system, as presented in [46] (© 2021 IEEE)

6.3.2 sEMG Channel Architecture

Inspired by the architecture proposed in Yazicioglu et al. [47], the proposed sEMG channel architecture, illustrated in Figure 6.5a, is composed of 3 main blocks: a Transconductance-Transimpedance (TC-TI) input stage, a Gm-C Filtering Stage and an Envelope Stage for in-channel feature extraction. This section describes each block in detail.

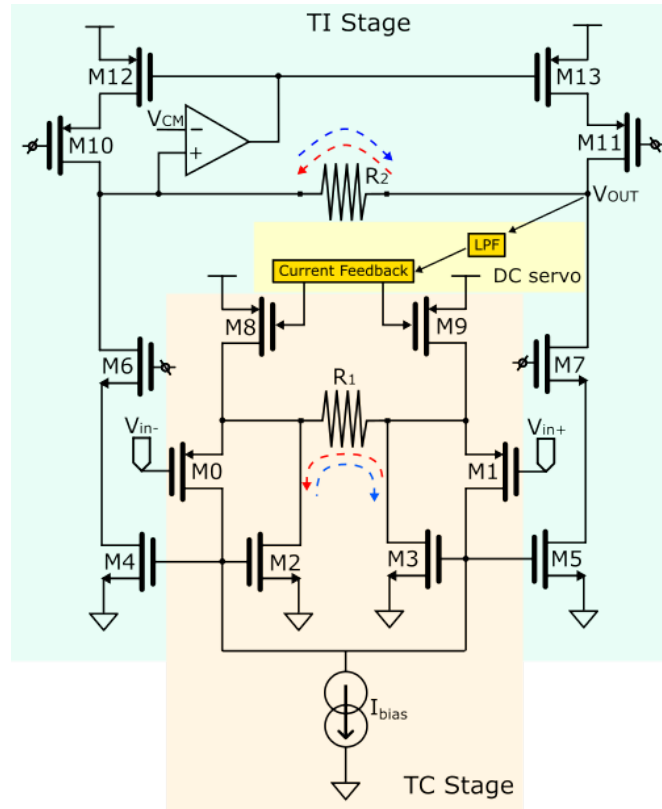
TC-TI Amplification Stage

A chopped TC-TI architecture is proposed as the channel input stage, providing large input resistance, high CMRR, low noise and low power consumption. Furthermore, this architecture can be integrated on a multi-channel approach using only a single input stage by replicating the differential current from the TC output, limiting the area and power consumption of the system. This amplifier architecture provides a voltage gain defined by two internal resistances, R_1 and R_2 , as presented in Equation 6.7:

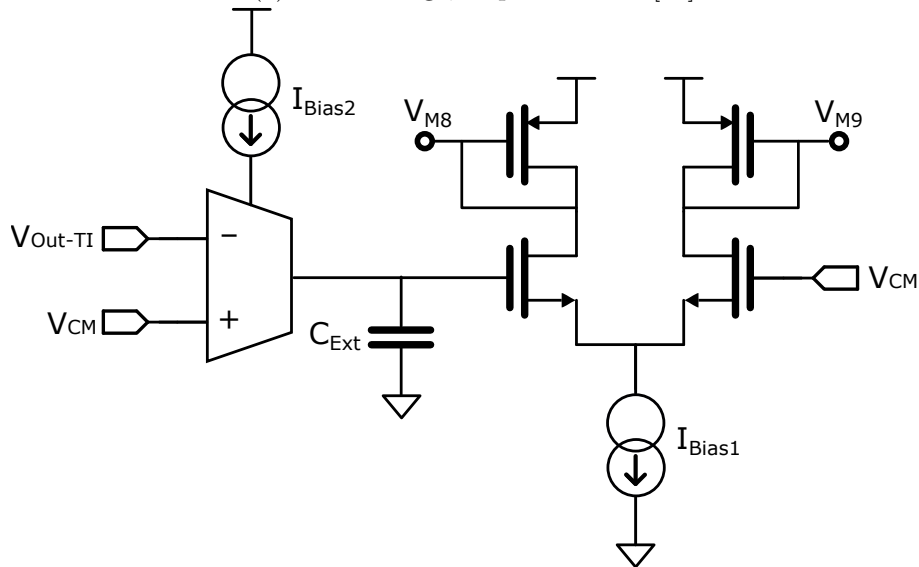
$$Gain_{IA} = TC \times TI = \frac{R_2}{R_1} \quad (6.7)$$

These resistors are sized to yield the maximum possible gain without compromising the dynamic range, achieving a gain of 36 dB. Figure 6.6a illustrates the transistor level schematic of this stage.

A DC servo loop performs common-mode stabilisation, achieving high CMRR while rejecting DC offsets - effectively acting as a High Pass Filter (HPF). The exact HPF time constant is established by an off-chip capacitor of $3\mu F$, setting the 3dB cut-off frequency to 10 Hz. Figure 6.6b shows the architecture of this DC servo stage.



(a) TC-TI Stage, as presented in [46]



(b) DC Servo Architecture

Figure 6.6: Input Stage Architecture, formed by (a) TC-TI Amplification Stage, (b) DC Servo, acting as HPF by rejecting DC components; as presented in [46] (© 2021 IEEE)

Gm-C Filtering Stage

An in-channel 2nd order LPF is implemented through a Gm-C filter, realised as shown in Figure 6.7. The size of this capacitor is minimised by operating the transconductance amplifier in weak inversion, which enables low power operation, large linearity and precise control of g_m by the biasing current:

$$g_m = I_{ds}/n \cdot U_t \quad (6.8)$$

The corner frequency of this structure is programmable and defined by:

$$\omega_0 = \frac{g_m}{\sqrt{C_1 C_2}} \quad (6.9)$$

where C_1 and C_2 represents 1pF in-channel capacitors. The frequency response of this filter, after the initial amplification and filtering provided by the TC-TI stage, is presented in Figure 6.8.

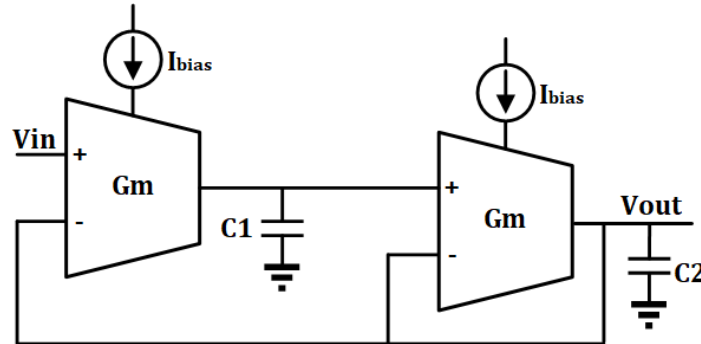


Figure 6.7: Second Order Gm-C Low Pass Filter using $C_1 = C_2 = 1\text{pF}$, as presented in [46] (© 2021 IEEE)

Envelope Generator

As discussed in Section 6.3.1, one of the main features correlated with fatigue that can be extracted from sEMG signals is the RMS evolution. The signal's envelope is extracted on-chip using two current rectifiers and a peak detector.

The differential currents generated at the TC stage are mirrored to the Envelope stage for current-mode processing. This block is formed by two half-wave current rectifiers that constitute a full-wave current rectifier, inspired by the architecture proposed by Zhak et al. [48]. This operation is achieved by rectifying the TC's fully differential currents and mirroring them to

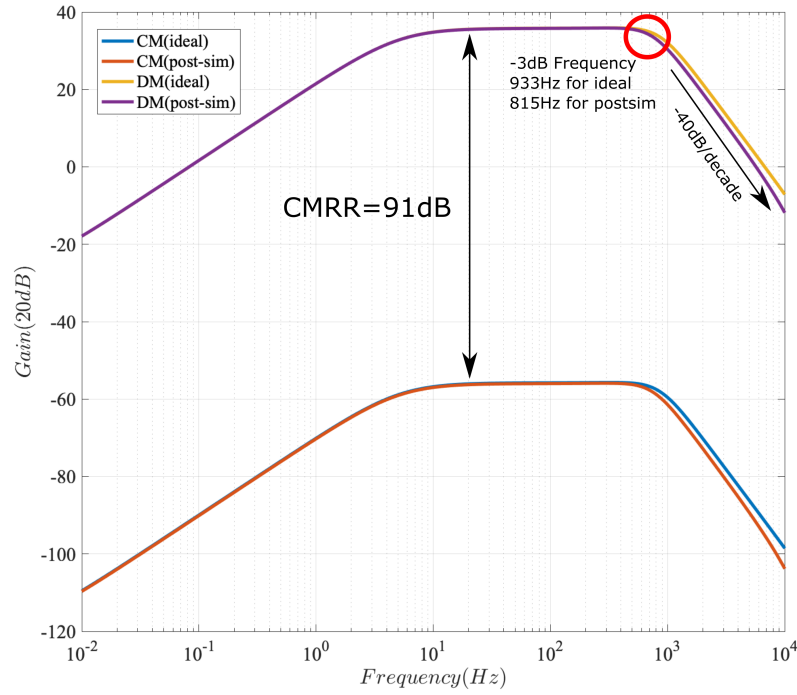


Figure 6.8: Raw sEMG Frequency Response after conditioning stages

a peak detector. The peak detector performs the signal envelope, with an attack and release time programmable through the external capacitors C_{rise} and C_{fall} , which ultimately control the corner frequency. Figure 6.9 presents the envelope architecture.

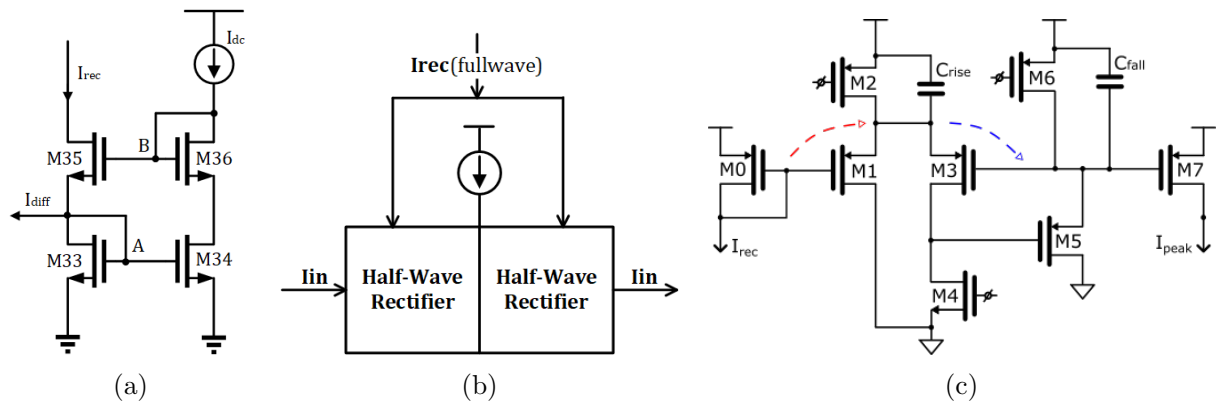


Figure 6.9: Envelop Detector, formed by (a) Half wave rectifier, (b) Full wave rectifier, composed by two half wave rectifiers, (c) Peak detector circuit, generating an output signal I_{peak} , as presented in [46] ((© 2021 IEEE))

6.3.3 System Architecture

The channel described in the previous section was integrated as part of an SoC, as illustrated in Figure 6.5b, composed of six main blocks:

- **4 sEMG channels:** The proposed channels were stacked, forming a block with four sEMG channels. Each channel layout was planned so no additional connection was required, enabling the inclusion of additional channels with minimal overhead. All sEMG channels operate in parallel and extract both raw sEMG signal and sEMG envelope simultaneously.
- **Bias Generator:** Weak inversion operation at the Gm-C requires fine control of biasing current to ensure robust cut-off frequency due to its exponential function to V_{gs} . A chip-level biasing block was implemented to enable precise biasing control while remaining scalable to multi-channel architectures. This biasing block is formed by cascoded current mirrors that generate all biasing conditions. All four channels share these signals, and more channels could be stacked and share these signals if required.
- **Channel Selection & Digital Control:** This digital control unit enables channel selection for digitisation, choosing from either raw sEMG signal or envelope. The selected channel signal is also redirected to the Zero Crossing Rate Converter. This block also provides an SPI interface for off-chip communication, enabling both data acquisition and system programmability
- **Zero Crossing Rate Converter:** The Zero Crossing Rate Converter transforms the sEMG signal into a PWM signal representing the common-mode crossing transitions. This ZC feature is obtained through a comparator connected to the common-mode potential and the output of one sEMG pipeline. The output represents the comparison states, where V_{DD} is obtained when the sEMG value is above the common-mode reference voltage, and ground where the sEMG signal is below this reference.
- **Transimpedance Amplifier (TIA):** The current generated from the sEMG envelope is converted to voltage through a TIA for further digitisation by the ADC.
- **Analogue to Digital Converter (ADC):** A 10-bit, single-slope ADC converts the provided signals (raw sEMG or TIA-generated voltage) into digital codes that can be transferred off-chip through the SPI interface.

This System-on-Chip serves as an experimentation platform to validate our assumption on Information-Focused sampling. The prototype was sent for fabrication, and the preliminary results obtained from its simulation are presented in the following section.

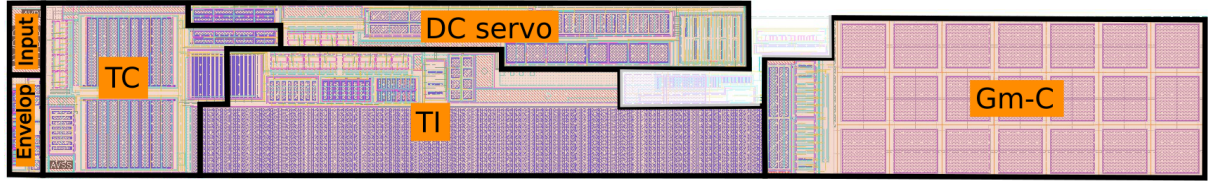


Figure 6.10: sEMG Channel Layout [46] (© 2021 IEEE)

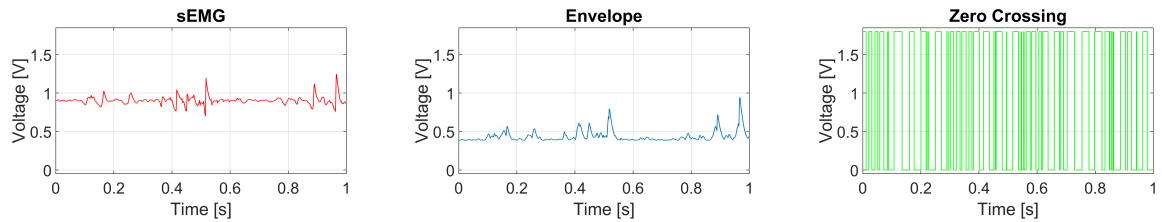
6.3.4 Simulation Results

The proposed sEMG Information-Focused system was designed on standard CMOS TSMC 180nm technology and sent for fabrication. Figure 6.10 provides the sEMG channel layout, highlighting each block forming the pipeline. Figure 6.12 shows these channels integrated as part of an SoC.

Figure 6.11 presents a sample simulation using prerecorded sEMG signals, confirming the functional behaviour of the feature extraction architecture. Table 6.3 highlights the measured performance for both the sEMG channel and the overall SoC, and the comparison with state-of-the-art systems is provided in Table 6.2.

Table 6.2: Comparison between sEMG wearable platforms [46] (© 2021 IEEE)

Parameters	This work	[49]	[50]	[51]	[38]	[52]
Environment	Lab and Outdoors	Lab	Lab and Outdoors	Lab and Outdoors	Lab and Outdoors	Lab and Outdoors
Components	ASIC	Custom	Myoware EMG and Arduino MEGA	RHD2132 Intan chip and CC3200 microcontroller	ASIC	HM121 STMicroelectronics
sEMG extraction	✓	✓	✓	✓	✓	✓
Wearable	✓	✓	✓	✓	✓	✓
On-chip Feature Extraction						
Muscle Fatigue - ZC	✓	✗	✗	✗	✓	✗
Muscle Activity - RMS	✓	✓	✗	✗	✓	✓
Multichannel	✓	✓	✗	✓	✗	✗
Power consumption	4.24 mW	Not specified	Not specified	119 mA	628 μ A	26 mW
Supply voltage	1.8 V	-	3.1-5V Myoware 7-12V Arduino Mega	3.3 V	3.3 V	Not Specified



(a) Raw sEMG signal, sampled at the channel output after amplification and filtering (b) Envelope of sEMG signal, a feature of muscle activation levels (c) Zero crossing of sEMG signal around the common mode potential

Figure 6.11: Simulation Results from sEMG channel, as presented in [46] (© 2021 IEEE)

Table 6.3: Simulated System Performance [46] (© 2021 IEEE)

sEMG Channel	
Signal Assumptions	
<i>Assumption</i>	<i>Value</i>
Input dynamic range	$\pm 10\text{mV}$
Maximum Input offset	20mV
Simulated Performance	
<i>Performance parameter</i>	<i>Value</i>
Channel Size	$90 \times 630 \mu\text{m}^2$
Sensing domain	Voltage
Power consumption	
Total	$42.61 \mu\text{W}$
TC stage	$5.616 \mu\text{W}$
TI stage	$5.688 \mu\text{W}$
DC servo	$8.568 \mu\text{W}$
Gm-C LPF	$0.0297 \mu\text{W}$
Envelope	$22.72 \mu\text{W}$
Total gain	36dB
CMRR	91dB
Signal spectrum	$10\text{-}450\text{Hz}$
Noise floor	$30\text{-}60 \text{ nV}/\sqrt{Hz}$
Integrated noise	$0.78\text{uV}_{\text{rms}}$
Input impedance	$2.08\text{G}\Omega @200\text{Hz}$
System - Simulated Performance	
System Size	$500 \times 900 \mu\text{m}^2$
Total power consumption	4.24 mW
10-bits ADC	2.23 mW
TIA	$383 \mu\text{W}$
Zero Crossing	$313 \mu\text{W}$
Digital Control	$649 \mu\text{W}$
4-Channel sEMG	$170 \mu\text{W}$
Channel Biasing	$492 \mu\text{W}$
ADC Resolution	$10\text{-bits} / 15.6 \mu\text{V}$
Fatigue features	sEMG Envelope Zero crossing

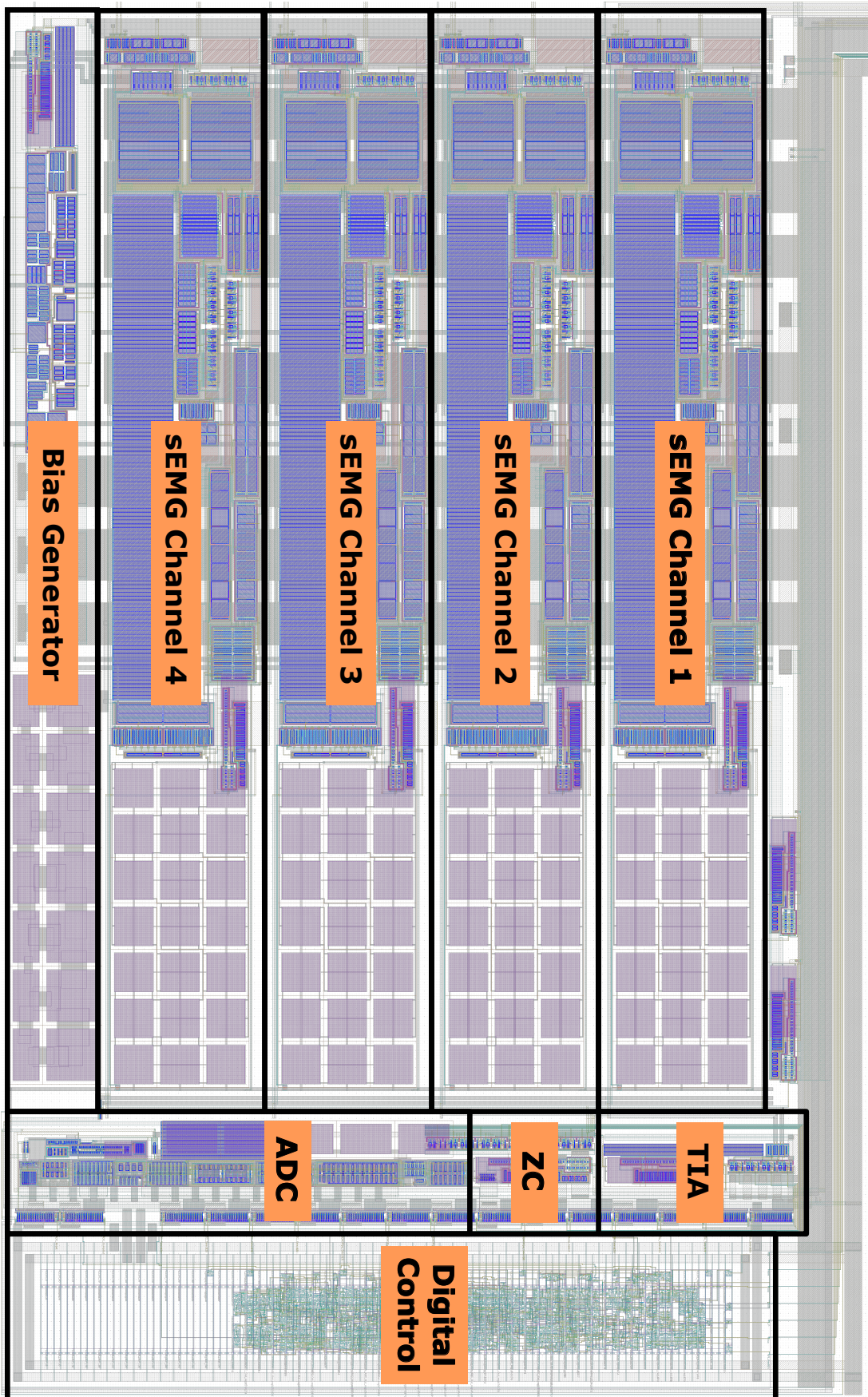


Figure 6.12: sEMG System Layout

Upon arrival from the fabrication of the proposed prototype, this system will be integrated as part of a wearable sEMG platform, enabling its functional and clinical validation. Our assumption on Information-driven sampling will then be tested, validating whether this feature extraction on-chip can reduce the sampling rate without harming the fatigue forecasting accuracy using the predictive model proposed by Moniri et al. [33]. The results obtained during this trial can change the current state-of-the-art sEMG sensing landscape, moving from a generalist approach of sEMG front-end development to a targeted, application-driven approach that leverage insights provided by algorithmic models to optimise hardware architectures.

6.4 Summary

The incorporation of algorithmic methods on sensing systems has the potential to enhance performance by optimising and tailoring the information required for each application. In this chapter, two examples were analysed to showcase the potential of this data-driven optimisation.

The initial example tackled the transmission and storage bottleneck present on ultra-high frame rate ISFET arrays. These platforms generate large datasets with high throughput, requiring bulky transmission interfaces (such as PCI-Express) and bench-top PCs for storage. In this context, I leveraged the widely-used JPEG image compression algorithm to compress the ISFET-generated chemical images, reducing the image size significantly with minor image distortion. This compression was further optimised by modifying the JPEG quantisation tables. Initially designed for natural images, these tables can be tailored to chemical images through a bio-inspired approach, using Evolutionary Algorithms to solve this optimisation problem. Using this approach, the Compression Ratio was enhanced by 13.03% with minor PSNR degradation (-0.08 dB), yielding a novel ISFET-targeted JPEG algorithm with enhanced performance.

The second section of this chapter explored the transition from Data-Harvesting to Information-Focused sensing in the context of sEMG signals. The need for large electrode arrays and high parallelism for the analysis of LBP at the PoC is currently limited by these systems' power consumption, which prevents its long-term deployment as a wearable solution. The proposed system aimed to leverage recently discovered LBP fatigue features to lower the Nyquist frequency of the system, enhancing its scalability with minor overhead. This architecture aimed to achieve this by extracting these features on-chip on the analogue domain, potentially reducing the ADC frequency per channel by sampling only fatigue information rather than harvesting raw sEMG signal. By relaxing the sampling requirements, these systems could become more scalable, reducing the power consumption per channel and enhancing its suitability for wearable platforms, ultimately helping patients and doctors better tackle musculoskeletal diseases.

These developments represent promising examples of the opportunities lying in the interface

between sensing and software. With state-of-the-art PoC sensing systems constrained by portability, power, and data storage limitations, a transition towards information-focused sensing leveraging the insights unveiled by algorithmic methods is key to overcoming current sensing bottlenecks. Furthermore, the accelerated growth of Machine Learning and Artificial Intelligence solutions represents an unparalleled opportunity for unraveling new data patterns undiscovered by classical software methods, enabling further integration at the sensor level and yielding gains in power and area. Information-focused sensing is an exciting and emerging research field, and I envision fruitful developments over the next decade.

6.5 Publications

Several publications arose from the content of this chapter.

- [13] J. Zeng, M. Cacho-Soblechero et al. "An Ultra-High Frame Rate Ion Imaging Platform Using ISFET Arrays with Real-Time Compression". In: *IEEE Transactions on Biomedical Circuits and Systems* (Under Review)
- [46] W. Tu, M. Cacho-Soblechero et al. "A 4-Channel sEMG ASIC with Real-Time Muscle Fatigue Feature Extraction". In: *2021 IEEE International Symposium on Circuits and Systems (ISCAS)* (2021), pp. 1–4.

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Chapter 7

Conclusion

7.1 Overview

This thesis leverages Voltage Controlled Oscillators' sensing and programmable capabilities to implement the next generation of ISFET-based platforms for infectious diseases detection at the Point-of-Care. This synergy between ISFET imaging and VCOs is motivated by the need for accurate temperature control on DNA amplification protocols and pixel-level programmability to compensate CMOS ISFET non-idealities and adapt to changing sensing conditions. For this purpose, two initial VCO-based architectures were fabricated and compared, demonstrating their programmability characteristics and their suitability for chemical imaging. Based on this analysis, an optimised VCO architecture was presented, using a linear OTA coupled with a 2-stage Sawtooth Oscillator to achieve adaptability and dual-sensing capabilities. This dual-sensing capability enabled chemical and thermal sensing from the same spatial point without additional circuitry while achieving fast compensation of trapped charge and potential drift mitigation. This pixel was integrated as part of a 32 x 32 array, and its suitability for DNA detection was confirmed.

The need for amplification-based diagnosis at the Point-of-Care in a deliverable form factor motivated the proposal of a new architectural paradigm on ISFET-based platforms, branded as a "Diagnosis-on-a-Chip". This concept advocates for integrating sensing elements and computational capabilities on the same substrate, blending elements from both domains to optimise platform footprint. For this purpose, a novel Digital ISFET Sensor architecture was implemented, combining sensing elements, an ADC and memory at the pixel level. This architecture enabled highly parallel operation, achieving full-frame acquisition on a single ADC cycle. Furthermore, sensing output was stored in-pixel, enabling its integration with computational elements without bulky memories. Using this architecture, I proposed an example system formed by a Digital ISFET Sensor array integrated with an ARM Cortex M3, paving the way for the

next generation of “Diagnosis-on-a-Chip” ISFET systems.

The computational capabilities integrated on the “Diagnosis-on-a-Chip” require software methods that enable accurate reaction detection. In this context, a portable platform was fabricated, “instantDNA”, rich in processing capabilities to fast-track the development of computational methods targeting the mitigation of ISFET non-idealities. Leveraging the oscillatory behaviour of VCO-based architectures, a chemical noise reduction technique was proposed, showing minor improvement by averaging thermal chemical noise. Using the adaptability mechanisms enabled by VCO-based architecture, real-time chemical drift compensation was proposed to extend dynamic range without strict requirements on the ADC stage, opening new opportunities for long-term drift forecast by blending large datasets with Machine Learning algorithms. Additional opportunities surging from the application of data-driven software methods were explored in the last section of this thesis, presenting two examples of sensing systems whose performance could be improved by leveraging data insights.

7.2 Contributions

Looking back at the structure proposed in Chapter 1, the work presented in this thesis contributes to answering the posed research questions as follows.

7.2.1 How can we develop ISFET-based PoC platforms more adaptable to both non-idealities and external conditions?

This question was initially addressed in Chapter 3, looking at the hardware challenges using Oscillator-based ISFET architectures and their application at the PoC.

- I proposed and compared two novel VCO-based ISFET architectures, CCRO and Sawtooth Oscillator, identifying their benefits in terms of adaptability and scalability, as well as the potential for ultra-low power consumption.
- I optimised one of the proposed architectures, achieving a compact, adaptable and dual-sensing pixel architecture based on a Sawtooth Oscillator. This architecture, integrated as part of a large array, achieved for the first time thermal and chemical sensing on a single spatial point without additional instrumentation, eliminating the need for off-chip sensors.
- I envisioned and simulated two additional architectures, exploiting the presented benefits of Oscillator-based architectures. Leveraging on the CCRO front-end, a scalable

and ultra-low-power ISFET architecture was designed, minimising the power supply required for operation and trading power performance with sampling rate. This approach yielded the lowest reported power consumption for an ISFET architecture. Furthermore, the multi-sensing capabilities were expanded to four modalities, ions, temperature, light and fluid detection, modulating all results on a single waveform. These results, while promising, would still require *in silico* verification.

Based on the adaptability mechanisms provided in Chapter 3, Chapter 5 contributed by presenting software methods to address ISFET non-idealities based on this programmability capabilities.

- I presented a fast and accurate 2-step trapped charge compensation controller, achieving over 99% of pixels in optimal operation point across a 32 x 32 array. This controller used both reference electrode potential and the internal DAC to compensate trapped charge, creating the basis for the subsequent drift compensation.
- I enhanced ISFET dynamic range by creating a real-time drift compensation controller, mirroring the sensed output to the compensation input. Using this drift compensation mechanism, 99.3% of array pixels remained active after 36 hours of continuous monitoring.
- Using the data obtained during the long-term monitoring trial, I validated the drift model proposed by Jamasb et al. [1] for 36 hours, opening opportunities for drift forecasting based on large datasets coupled with ML.
- I proposed a resolution enhancement mechanism by temporally averaging the pixel signal, leveraging on the oscillatory nature of VCO output. This experiment demonstrates the need for flicker noise reduction techniques, as further filtering of thermal noise would not improve pH resolution.

These contributions aimed to realise the vision of a Sense-Aware ISFET PoC Platform: a platform capable of sensing both internal and external events, forecast its trend and adapt to its influence, achieving a robust, resilient and precise diagnosis.

7.2.2 How can we reduce ISFET-based platforms footprint at a system level to enhance their deliverability to the PoC?

The PoC devices' requirements have shifted over the last year due to the COVID-19 pandemic, requiring a deliverable diagnosis that could potentially be sent through postal mail nationwide to the patient's home at a minimal cost. Chapter 4 explored this shift in requirements and provided the following contributions.

- I postulated the need for a “Diagnosis-on-a-Chip”, a new design paradigm that urges further integration of computational capabilities and sensing elements to reduce the device’s footprint.
- To achieve this “Diagnosis-on-a-Chip”, I proposed a novel ISFET architecture, named Digital ISFET Pixel, that merged both an ISFET sensor, an ADC and a memory bank at the pixel level. This architecture was highly scalable to larger arrays, requiring a single ADC cycle to acquire an entire frame. Furthermore, it eliminated the need for on-chip memories while improving capacitive attenuation performance by increasing the sensing area. Finally, this architecture could be integrated with computational capabilities without overhead, as shown in the example system.

Although these results are still subject to verification *in silico*, I expect the proposed vision to be essential to achieve a compact, inexpensive and deliverable PoC diagnosis that helps the fight against any future pandemic crisis.

7.2.3 How can novel data-driven methods help enhance the PoC sensors’ sensing capabilities?

Chapter 6 widened the thesis perspective beyond the proposed circuit-based approach to sensing challenges, proposing data-driven algorithmic methodologies to unravel hidden sensing patterns and overcome current bottlenecks, with major implications to biomedical diagnosis. This chapter encompassed two main contributions:

- I leveraged on chemical images’ distinct characteristics to optimise JPEG compression algorithm for ISFET images, reducing the data required to recover the chemical information while preserving the image quality. This algorithm was validated on chemical images acquired from an ultra-high frame rate ISFET array, addressing the need for optimised data transmission for high throughput systems.
- I proposed an alternative data acquisition approach for sEMG sensing, focusing on the underlying information enclosed on the raw data. By extracting on-chip fatigue-related information, there is an opportunity to lower the sampling frequency while obtaining improvements on power and parallelism, with subsequent gains on wearability and clinical relevance. This concept is still to be verified *in silico*.

The results of this chapter represent the first step towards fully answering this research question, proposing a set of concepts that can become promising research lines to continue in future work, with high potential for overcoming current sensing bottlenecks and enhancing sensing capabilities.

7.3 Recommendations for Future Work

Based on the work presented in this thesis, several promising opportunities have been identified for future research, as detailed below:

7.3.1 Sense-Aware ISFET Array

The development of multi-sensing arrays using the proposed oscillator-based architectures opens exciting opportunities for further enhancing the sensing capabilities while improving its resilience to changes in external conditions.

ISFET sensors are responsive to changes in their external conditions, modifying their sensitivity and the evolution of their non-idealities. Incorporating additional sensors, such as photodiodes, would enable a comprehensive analysis of the effect of these external conditions, potentially facilitating the development of an analytical model that forecasts the evolution of these effects *a priori*. A model like this, coupled with the proposed adaptability in-pixel, could improve the current Limit of Detection.

Furthermore, light sensing coupled with ion imaging could enable pathogen multiplexing on a single reaction. By leveraging state-of-the-art data-driven approaches [2, 3], both sensing modalities could serve as additional degrees of freedom for primer differentiation, expanding the maximum number of multiplexed assays on a single well. This multiplexing would be key for achieving comprehensive screening through PoC diagnosis.

These Sense-Aware ISFET systems, capable of acquiring multi-modal data, adapt in real-time and enhance sensing possibilities, represent a promising research alternative to overcome current ISFET limitations.

7.3.2 Deployment of Diagnosis-on-a-Chip

The integration of sensing and processing capabilities on the same silicon chip, realising the presented “Diagnosis-on-a-Chip”, is one of the most exciting future research for ISFET-based PoC devices. Transitioning from a portable device, which would require a processing station for thermal control, data acquisition and post-processing, to a deliverable “Diagnosis-on-a-Chip” has the potential to shift the current diagnosis paradigm. This new paradigm would bring the precision of nucleic acid methods such as PCR and LAMP to the patient’s home, widening the applicability and impact of ISFET-based PoC platforms.

7.3.3 Detection of slow ion variation during long-term monitoring

One of the main limiting factors for the applicability of ISFET-based platforms beyond amplification-based sensing is the precision and accuracy during slow ion reactions over long periods of time. The concentration of ions on fluids such as sweat and ISF varies between minutes and hours, overlapping with chemical drift and preventing event identification and quantification. The development of analytical drift models and the availability of large datasets using long-term monitoring could mitigate the effect of low-frequency noise, enabling the identification of ionic reactions through anomaly detection. Ultimately, the identification of such reactions would enhance the suitability of ISFET sensors for their integration into wearable platforms, enabling its use for continuous, real-time electrolyte monitoring.

7.3.4 Information-Based Compression of chemical videos

The high transmission bandwidth required for ultra-high frame rate ISFET platforms prevents the miniaturisation of these devices and their applicability at the PoC. The JPEG-based compression optimisation of ISFET images proposed in this thesis represented the first step towards overcoming this challenge, and it could be further improved by using a two-fold approach: Firstly, incorporating information-based metrics tailored to the required application rather than the generic PSNR. By focusing on accuracy metrics to identify specific events, the compression ratio can be further optimised without compromising the underlying chemical information. Secondly, the small frame-to-frame variations makes this type of images ideal for compression algorithms focused on spatial and temporal redundancy removal, such as MPEG [4] or learning-based video compression algorithms [5, 6].

7.4 Thesis Discussion and Outlook

At the beginning of this thesis, array-based ISFET architectures were transitioning from an academic use as bench-top instruments to the deployment at the Point-of-Care. This shift was achieved by integrating sensing elements and instrumentation on the same substrate, reducing its form factor to make it suitable for portable diagnostic platforms. ISFET integration on these PoC platforms introduced additional challenges related to the sensing environment and a set of opportunities that will shape the field for the coming years. I would like to finish this thesis by briefly reviewing the future trends that will shape the field in the years to come.

Firstly, academic research has extensively focused on ISFETs implemented on CMOS native passivation for developing such platforms, looking at compensation mechanisms to tackle its

non-ideal effects. However, commercial applications have opted for surface passivation modification, trading additional manufacturing costs for robustness and reproducibility. This reproducibility represents an essential factor in safety-critical devices such as PoC diagnosis. Hence, I envision that successful ISFET-based platforms will explore additional passivation opportunities in an attempt to maximise accuracy over the next decade.

Secondly, the challenging sensing environment requires a novel approach at a system level. As the external conditions might significantly affect the sensing outcome, the platform would require a controlled and easy-to-use encapsulation and the sensing means to analyse the surrounding environment. In this context, I foresee further integration of sensing capabilities on a single die, as shown throughout this thesis, which not only provides awareness of both internal and external conditions but also enable sensing enhancements such as multi-modality multiplexing - using both chemical and light probes to determine the exact pathogen on a sample.

Thirdly, this sensing environment and the compensation of its non-idealities and cross-sensitivities requires physical models that represent analytically the effect of different phenomena on the electrochemical recognition element. Only mechanistically understanding the electrochemical behaviour of the sensing surface, researchers will be able to design and develop robust and resilient sensors. Hence, with the increase of the commercial application, I foresee a significant increase of the research devoted to unravelling the underlying effects during the sensing process.

Fourthly, the rise of data-driven and learning algorithms has the potential to unravel hidden patterns on the sensing data, enabling novel sensing modalities and improving state-of-the-art performance. One example use case could be the application of Neural Network Autoencoders as anomaly detection, enabling early detection of surface degradation, one of the most urgent challenges on biosensing. Hence, I expect an increase in the number of applications that leverage on data-driven models to enhance capabilities and overcome bottlenecks.

Moreover, the race for better sensors at the Point-of-Care sometimes shadows the need for sample acquisition strategies for a End-to-End diagnosis with minimal human intervention. In the sample acquisition field, the recent development of microfluidics as part of PoC solutions is enabling the automation of sample acquisition and preparation steps, and I foresee further integration between microfluidics and sensing elements in the coming years, achieving truly monolithic and autonomous devices. An example of this trend is the recent announcement from XFAB [7], which will start offering silicon-based microfluidics integrated with custom CMOS circuits. This announcement, along the current trend towards incorporating additional solid-state electrodes such as multi-electrode arrays on CMOS [8, 9], might open synergies of different sensing modalities beyond ISFET-only arrays.

Finally, the COVID-19 pandemic exposed vulnerabilities on current PoC approaches. In a sit-

uation of complete lockdown where minimal population movement is vital for pathogen spread control, PoC devices that require no fixed infrastructure to operate, rapid time to deployment and can be delivered by post could significantly impact disease transmission, providing a rapid and systematic assessment of pandemic spread across the population. This assessment would potentially enable health policymakers to establish evidence-based and targeted strategies. For ISFET PoC platforms to seize this opportunity, I foresee that the components that currently form these portable platforms will be integrated on a single die, bringing together biasing, sensing, computation, and connectivity to reduce costs and minimise footprint. These “Diagnosis-on-a-Chip” systems have the potential to shape future pandemic responses, delivering affordable, timely and accessible healthcare for all.

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Appendix A

Chip Gallery

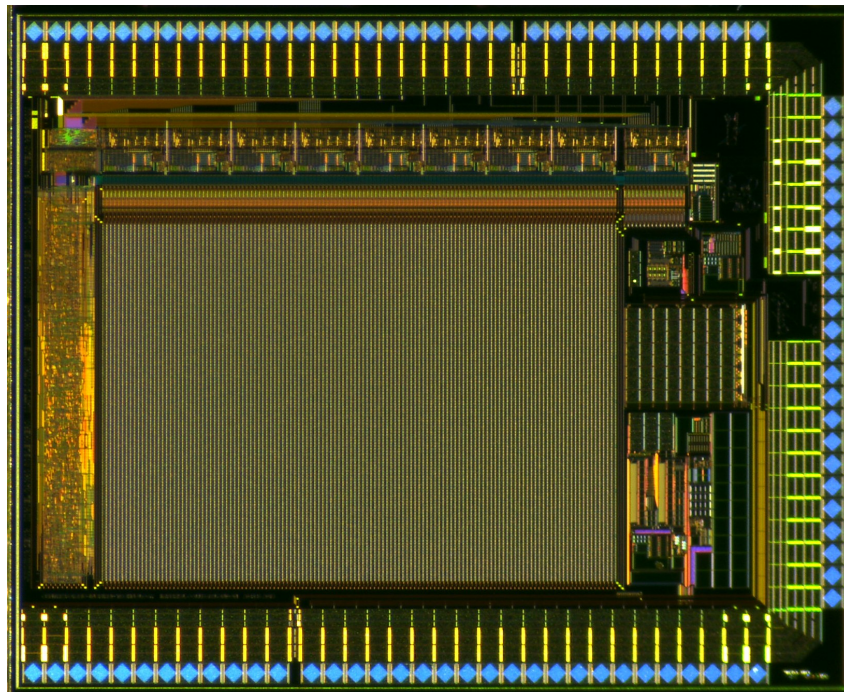


Figure A.1: LEGOLAS Chip - Winter 2018: Two test structures for exploring ISFET-based Oscillator Architectures

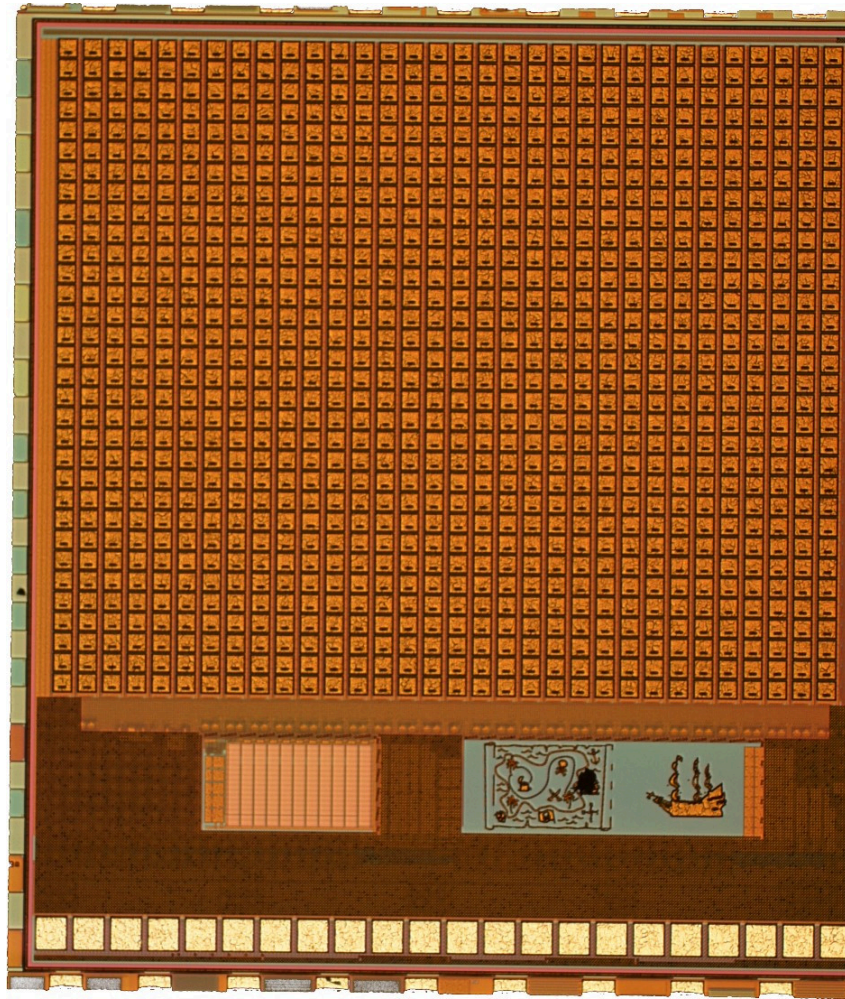


Figure A.2: BLACKPEARL Chip - Summer 2018: A 32 x 32 ISFET array with dual-sensing pixels, an on-chip compensation DAC and a Digital Control Unit

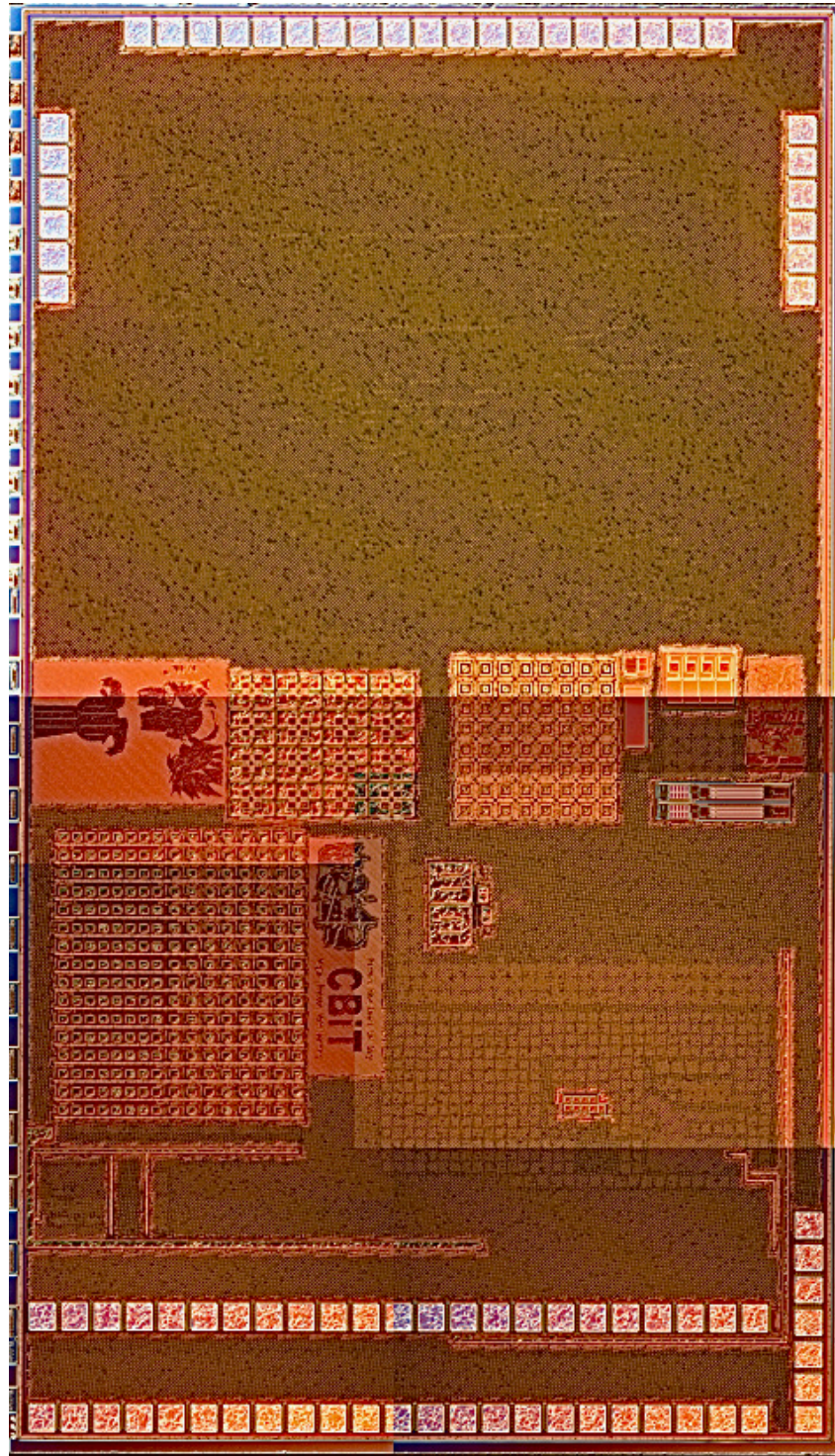


Figure A.3: Goku Chip - Winter 2021: A 16 x 16 Digital ISFET Sensor (DIS) array with In-Pixel ADCs

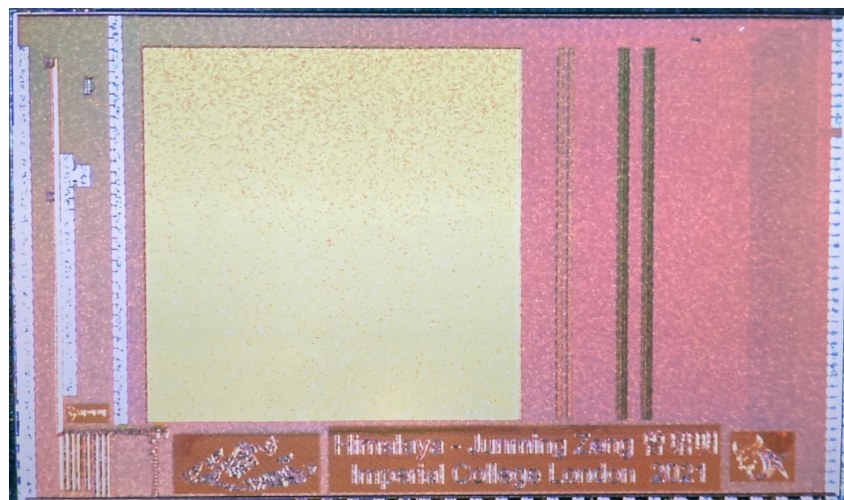


Figure A.4: Himalaya Chip - Winter 2021: A 4 channels sEMG front-end with in-built feature extraction

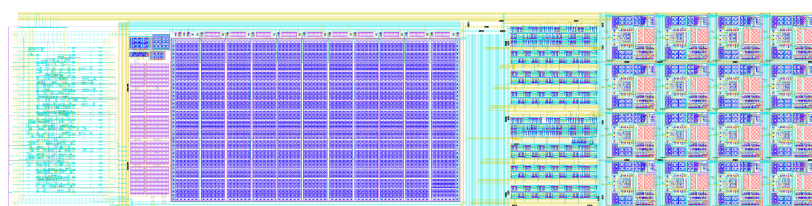
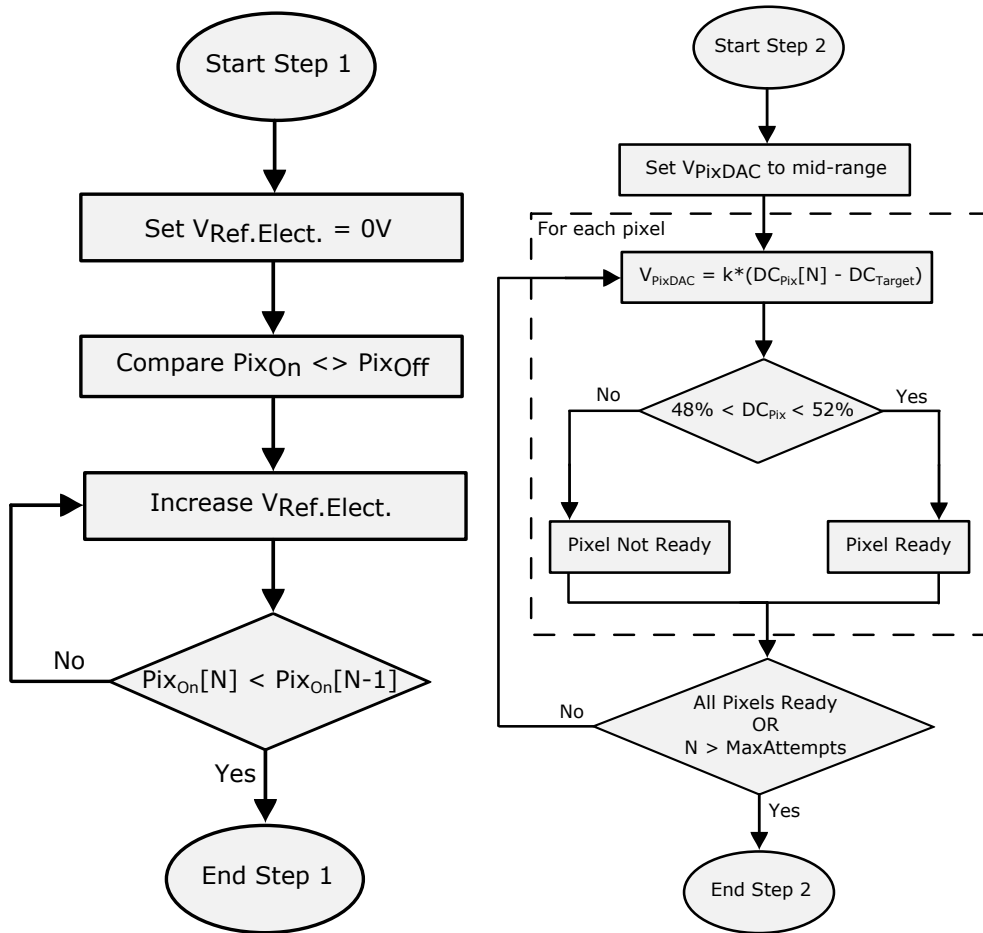


Figure A.5: Multisensing Array - Pending of Fabrication: A 16 x 16 Multisensing Array, sensing 4 modalities (ion, temperature, light and fluid detection) from a single spatial point

Appendix B

Algorithmic Methods Flowcharts



(a) Trapped Charge Compensation - Step 1 - Set the reference electrode potential to the optimal voltage

(b) Trapped Charge Compensation - Step 2 - Calibrate the pixel operation point to 50% duty cycle

Figure B.1: Trapped Charge Compensation Flowchart

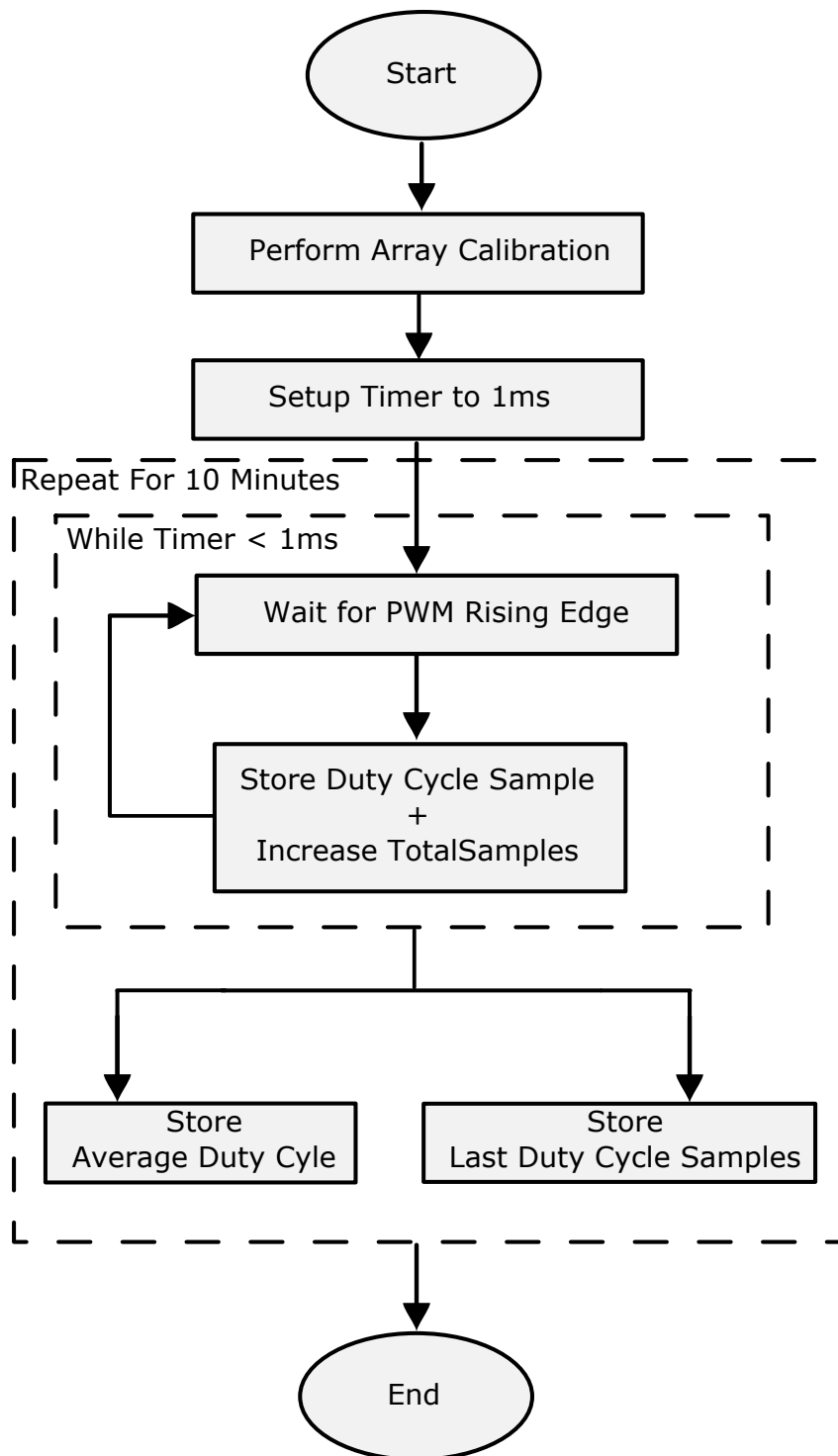


Figure B.2: Resolution Analysis Flowchart - Acquire samples from sensor during 10 minutes, using both a 1ms averaging window and a single sample

Appendix C

Full list of Publications

The full list of publications emerging from the content of this thesis is now included, classified by chapter and sorted by date of publication.

C.1 Chapter 3

- M. Cacho-soblechero, T. S. Lande, and P. Georgiou. “A fully-digital ISFET front-end with In-Pixel Sigma-Delta Modulation”. In: *2018 IEEE Biomedical Circuits and Systems Conference (BioCAS)* (2018), pp. 2–5.
- M. Cacho-Soblechero and P. Georgiou. “A Programmable, Highly Linear and PVT-Insensitive ISFET Array for PoC Diagnosis”. In: *2019 IEEE International Symposium on Circuits and Systems (ISCAS)* (2019), pp. 1–5
- M. Cacho-Soblechero et al. “Programmable ion-sensing using oscillator-based ISFET architectures”. In: *IEEE Sensors Journal* 19.19 (2019), pp. 8563–8575.
- M. Cacho-Soblechero et al. “A Dual-Sensing Thermo-Chemical ISFET Array for DNA-Based Diagnostics”. In: *IEEE Transactions on Biomedical Circuits and Systems* 14.3 (2020), pp. 477–489.
- M. Cacho-Soblechero et al. “An Ion-to-Frequency ISFET Architecture for Ultra-Low Power Applications” In: *2020 IEEE International Symposium on Circuits and Systems (ISCAS)* (2020), pp. 1–5
- Q. Hua, M. Cacho-Soblechero et al. “A Multi-sensing ISFET Array for Simultaneous In-pixel Detection of Light, Temperature, Moisture and Ions” In: *2021 IEEE International Symposium on Circuits and Systems (ISCAS)* (2021), pp. 1–5

C.2 Chapter 4

- J. Han, M. Cacho-Soblechero et al. “A Digital ISFET Sensor with In-Pixel ADC”. In: *2021 IEEE International Symposium on Circuits and Systems (ISCAS)* (2021), pp. 1–4.

C.3 Chapter 5

- M. Cacho-Soblechero et al. “Live Demonstration: A Portable ISFET Platform for PoC Diagnosis Powered by Solar Energy”. In: *BioCAS 2019 - Biomedical Circuits and Systems Conference, Proceedings* 2018.99 (2019), p. 1 - **Best Demo Award BioCAS 2019**
- M. Cacho-Soblechero et al. “A Dual-Sensing Thermo-Chemical ISFET Array for DNA-Based Diagnostics”. In: *IEEE Transactions on Biomedical Circuits and Systems* 14.3 (2020), pp. 477–489.
- S. Karolcik, N. Miscourides, M. Cacho-Soblechero, P. Georgiou. “A high-performance raspberry Pi-based interface for ion imaging using ISFET arrays”. In: *IEEE Sensors Journal* 20.21 (2020), pp. 12837-12847.

C.4 Chapter 6

- W. Tu, M. Cacho-Soblechero et al. “A 4-Channel sEMG ASIC with Real-Time Muscle Fatigue Feature Extraction”. In: *2021 IEEE International Symposium on Circuits and Systems (ISCAS)* (2021), pp. 1–4.
- J. Zeng, M. Cacho-Soblechero et al. “An Ultra-High Frame Rate Ion Imaging Platform Using ISFET Arrays with Real-Time Compression”. In: *IEEE Transactions on Biomedical Circuits and Systems* (Under Review)

C.5 Additional Publications

- A. Moniri, L. Miglietta, K. Malpartida-Cardenas, I. Pennisi, M. Cacho-Soblechero, N. Moser, A. Holmes, P. Georgiou, J. Rodriguez-Manzano. “Amplification Curve Analysis: Data-Driven Multiplexing Using Real-Time Digital PCR”. In: *Analytical Chemistry* (2020), pp. 13134-13143