DEVICE LEVEL CHARACTERIZATION OF OUTPHASING AMPLIFIERS

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In candidature for the degree of
Doctor of Philosophy

By

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ABSTRACT

The outphasing technique proposed by Chireix in 1935 is one of the classical methods of addressing power amplifier (PA) efficiency degradation caused by operating in output back-off (OBO) conditions, where PA efficiency is typically low. Essentially, the envelope from the input signal is eliminated, and two CW signals are constructed; these have constant amplitude, while their relative phase offset holds the original information contained by amplitude modulation. Consequently, efficiency improvements are achieved by amplifying signals with constant amplitude using PAs operating in saturation, where efficiency typically peaks. The envelope is restored at the output by means of a vector summation of both signals, using a non-isolating combiner at the output stage

The main focus of the work described in this thesis was placed on extending bandwidth of the inherently narrowband technique of outphasing and then adopting this method to modern telecommunication standards. Two prototype PAs were designed to investigate whether bandwidth improvements can be achieved by adopting a broadband balun as a combining structure in the outphasing PA. Two baluns were designed and fabricated to be used in the demonstrator circuits; one using a section of semirigid coaxial cable and the other, a planar balun realized on 10 mil thick Alumina substrate. A novel method of fabrication was proposed for the former structure, which achieved more than double octave bandwidth, from 1.25 GHz to 4.7 GHz with losses lower than 1dB, an amplitude imbalance (trace separation) below 0.75 dB and phase imbalance within ±5 degrees. The measured CW performance of the prototype circuits produced results comparable with the state-of-the-art solutions available in literature. Moreover, this work demonstrated that a balun with sufficient bandwidth allows load modulation to be prescribed at fundamental and second harmonic frequencies, opening the possibility of waveform engineering to

implement continuous PA modes such as class J in outphasing PAs. The desired harmonic load termination was achieved without any specialized matching networks, and solely by means of load modulation provided through active device interaction.

The thesis concludes with the formulation, analysis and description of the novel concept derived from Chireix outphasing. Several outdated assumptions still prevalent in outphasing analysis included in literature today are challenged and reformulated for modern semiconductor devices such as GaN HEMTs. Through this process, a new concept of Current Mode Outphasing (CMOP), is proposed and described in detail. One of the significant advantages of the proposed approach is it allows the elimination of the combiner structure, which typically dominates the size of the final outphasing circuit, due to the presence of λ/4 transmission lines. Consequently, the demonstrator MMIC circuit, containing DC bias, stability elements and pre-matched to 50 Ω on input and output, has been deployed on an area of 2.3 mm x 2.8 mm. The CMOP circuit was fabricated using 0.25 µm GaN technology and achieved a bandwidth of 1.6 GHz centered at 3.35 GHz, whereas the maximum CW output power remains within 43 dBm ± 0.5 dB. A total gain of more than 12 dB is reported from 2.95 to 3.95 GHz, while a maximum Power Added Efficiency was measured as 68.5% at 3.25 GHz and remains greater than 60% from 2.85 to 3.8 GHz, and above 50% for almost the entire frequency range. The output back-off (OBO) efficiency peaks at 3.25 GHz with 53.5% and 45.6% for 6 dB and 8 dB back-off, respectively, and remains above 30% and 23.7% for the entire frequency range. To the best of the authors' knowledge, this is the largest fractional bandwidth achieved in an outphasing PA, that has been reported in literature.

KEY CONTRIBUTIONS

Broadband planar balun - A novel approach to realizing and fabricating a planar balun structure has been demonstrated, where conventional bond wires are replaced by conductor bridges supported on polyimide blocks. Three different prototype structures were fabricated on 10 mil thick alumina substrate ($\varepsilon_r = 9.8$, $\tan\delta = 0.0001$) using thin film fabrication technology. More than double octave bandwidth is reported, from 1.25 GHz to 4.7 GHz with losses lower than 1 dB, an amplitude imbalance (trace separation) below 0.75 dB and phase imbalance within ±5 degrees. Measurements show good agreement with simplified 2D EM simulations. The performance of the balun is assessed for suitability in applications where amplitude and phase balance are of critical importance, such as push-pull or outphasing amplifier topologies. The balun is then employed in the subsequent outphasing circuit described in Chapter 4.

Outphasing PA #1 – A circuit is designed and fabricated using packaged GaN HEMTs from Wolfspeed and a broad-band balun as a power combiner in a Chireix outphasing system. The co-axial balun operates over an extended octave bandwidth, which allows load modulation to be proscribed at fundamental and second harmonic frequencies, allowing continuous modes such as Class B-J to be implemented. The desired harmonic load termination is achieved without any specialized matching networks and solely by means of load modulation provided by the active device interaction. Simulation results are verified and demonstrated; drain efficiencies of more than 65% and 50% are maintained over 6 dB and 9 dB output power ranges, respectively, with signals operating at 1.95 GHz, while reaching a maximum combined power of 44.8 dBm. This work is described in Chapter 4

Hybrid Outphasing PA prototype – A circuit is designed and fabricated that demonstrates the application of a broadband planar balun as a power combiner. This circuit uses the previously designed planar balun, described in Chapter 4, combined with two TGF2023-01-2 12W GaN HEMT devices from Qorvo, operates at centre frequency of 1.9 GHz and demonstrates a 15% bandwidth, where the maximum output power is maintained within 0.5 dB deviation from 41.2 dBm. A PAE above 55% and 44% when operating at its peak and 6 dB output back-off (OBO) output power,

respectively, is achieved over the same bandwidth. This work is described in Chapter 4

CMOP – A power amplifier architecture based on outphasing which represents the main novelty reported in this thesis. Two active devices are operated as current sources loaded by a single-ended load, and a combination of phase and amplitude control allowing a constant output voltage and therefore high-efficiency to be maintained for both devices. Output series compensation reactances are used to reduce the imaginary part of the modulated load and improve the efficiency. An integrated circuit prototype, fabricated on 0.25 µm GaN technology, is used as a demonstrator. Physical size is 2.3 mm x 2.8 mm, with an achieved bandwidth of 1.6 GHz centered at 3.35 GHz. The maximum CW output power remains within 43 dBm ± 0.5 dB. A gain of more than 12 dB is reported from 2.95 to 3.95 GHz, while a maximum Power Added Efficiency was measured as 68.5% at 3.25 GHz and remains greater than 60% from 2.85 to 3.8 GHz, and above 50% for almost the entire frequency range. The OBO efficiency peaks at 3.25 GHz with 53.5% and 45.6% for 6 dB and 8 dB back-off, respectively, and remains above 30% and 23.7% for the entire frequency range. This work is described in Chapter 5.

Measurement system dedicated to dual input RF PAs – phase-coherent measurement system was developed to characterise outphasing circuits presented in this work. The system is described in Chapter 6.

ACKNOWLEDGEMENTS

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LIST OF ABBREVIATIONS

Term	Description
ACLR	Adjacent Channel Leakage Ratio
ADS	Advanced Design System
AM	Amplitude Modulation
BBG	Baseband Generator
BW	Bandwidth
CHFE	Centre for High Frequency Engineering
CMOP	Current Mode Outphasing
CSP	Control Signal Power
DPD	Digital Predistortion
DSO	Digital Sampling Oscilloscope
DSP	Digital Signal Processing
DUT	Device Under Test
ET	Envelope Tracking
FET	Field Effect Transistor
GaAs	Gallium Arsenide
GaN	Gallium Nitride
HB	Harmonic Balance
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
LAN	Local Area Network
LDMOS	Laterally Diffused Metal-Oxide Silicon
LMBA	Load Modulated Balanced Amplifier
LO	Local Oscillator
LPF	Low Pass filter
LTE	Long Term Evolution
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuit
OBO	Output Back-Off
OFDM	Orthogonal Frequency Division Multiplexing
OMN	Output Matching Network
OTL	Offset Transmission Line
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratio
PBO	Power Back-Off
PCB	Printed Circuit Board
PDK	Process Design Kit
PM	Phase Modulation
RFIC	RF Integrated Circuit
RFPA	RF Power Amplifier

SCS	Signal Component Separator
SMD	Surface Mount Device
SMT	Surface Mount Technology
TL	Transmission Line
VNA	Vector Network Analyser
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiplexing Access

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TABLE OF CONTENT

CHAPTER 1

INTRODUCTION

1.1 Research Motivation

1.1.1 Growth of mobile telecommunication infrastructure

The last few decades have seen a remarkable and steady proliferation of mobile telecommunication services. As of June 2020, the mobile networks around the world carry almost 300 hundred times more data than a decade ago, with a total of 8.1 bn mobile subscriptions. It is estimated that the latter will grow further by 0.8 bn by 2026, with 4.4 bn subscribed clients on the recently introduced 5G standard [1].

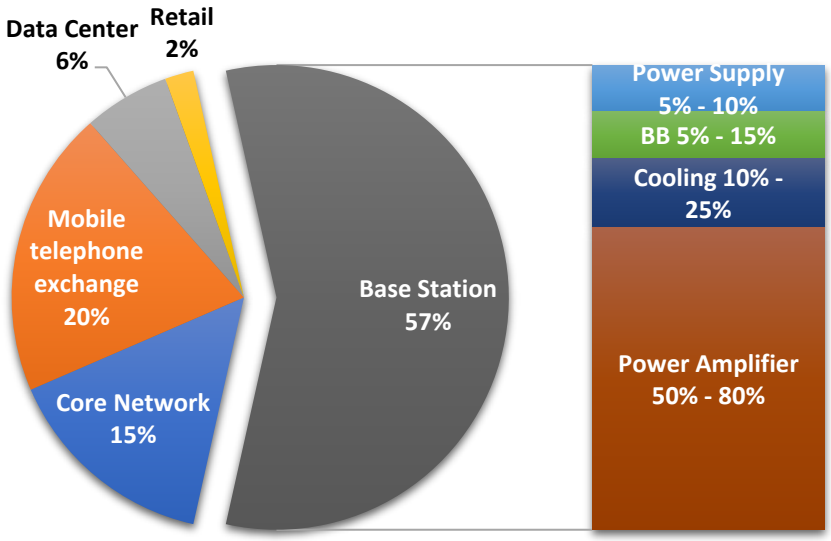

Figure 1.1 - Power distribution in mobile telecommunication network (left) and mobile base station (right) [2].

The mobile networks sector has become a substantial contributor to greenhouse gases. According to [1], the amount of carbon dioxide emitted by the mobile sector will reach 179 MtCO2 by 2020 and account for 51% of the total carbon footprint of the information and communication technologies sector.

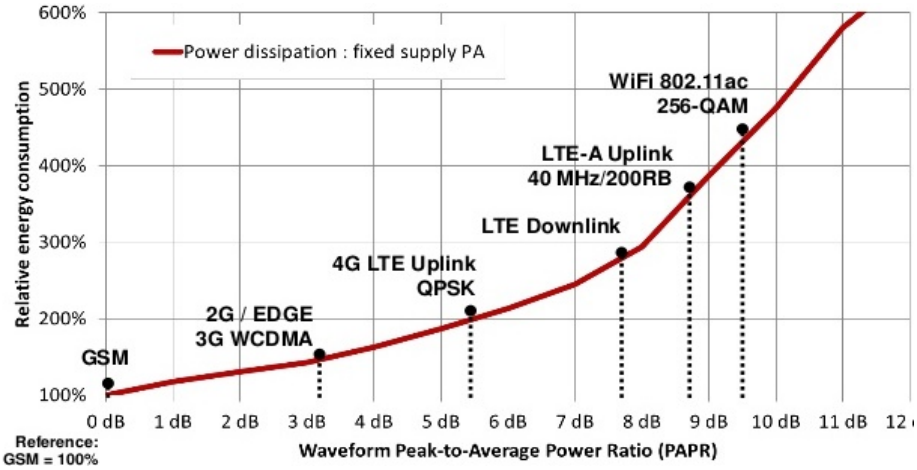

Figure 1.2 - Evolution of telecommunication systems and growing PAPR (reproduced from [3]).

The demand for mobile data transmission is predominantly driven by video streaming and smartphone devices [1]. It is expected to grow by a factor of four in the next five years. The data rates and throughput mandate spectrally efficient modulation schemes such as Orthogonal Frequency Division Multiplexing (OFDM). One of the main drawbacks of such modulation techniques are signals exhibiting a high peak-to-average power ratio (PAPR) as shown in Figure 1.2. These signals generally require the PA to operate in a backed-off condition, with a detrimental effect on its average efficiency, as illustrated in Figure 1.3 showing a probability density function of two, the OFDM as mentioned earlier and WCDMA. The blue trace on that figure represents the theoretical efficiency of PA operating in a Class – B mode. The average efficiency of such PA would be well below its theoretical maximum. Historically, several solutions have been proposed to address the efficiency drop caused by input signal

back-off [4]. One such technique is Chireix outphasing, the main subject of research presented in this thesis.

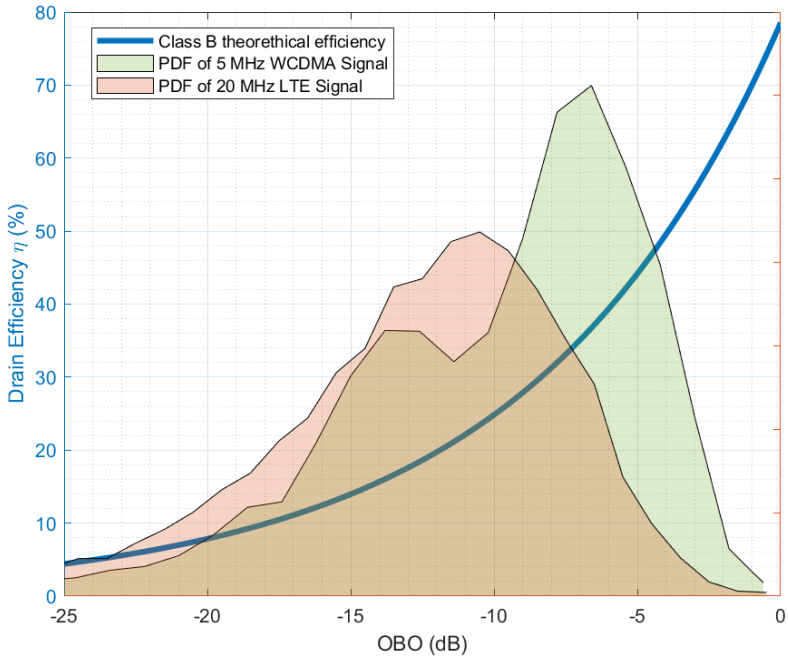

Figure 1.3 - Probability Density Function (PDF) of a typical LTE and WCDMA signals. Solid line represents the theoretical efficiency of a PA operating in a class-B mode.

1.1.2 GaN technology and its advantages

The vast majority of the power consumption in a typical mobile base station is attributed to the power amplifier section. The PA alone can utilise 50% - 80% of the total power consumption[5]. Consequently, high-efficiency PAs result in lower operational costs and contribute less to the CO2 emission.

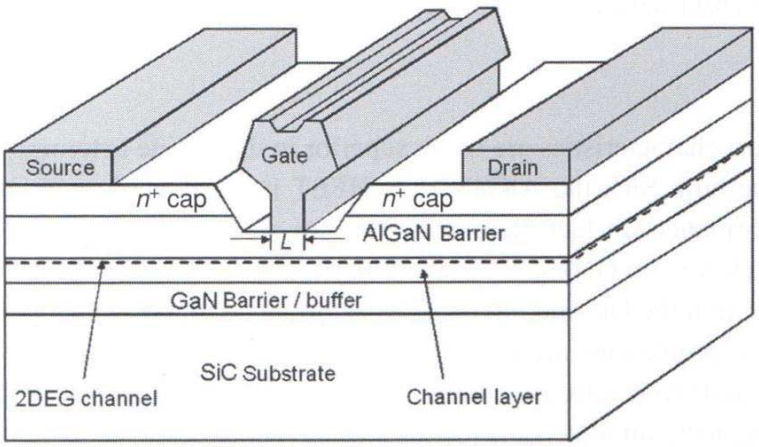

Figure 1.4 - The cross-section of a typical AlGaN/GaN HEMT device [6].

Over the past years, the base station was dominated by PAs using LDMOS active devices. These transistors offered high power density but were limited in the frequency they operated at – typically below 3.5 GHz due to the significant parasitic output capacitance arising from the lateral structure of the active device. With the GaN technology becoming mature in recent years, this technology can offer a power density comparable with that of an LDMOS, but with several advantages. The electron mobility ($v_s \approx 2 \times 10^7$ cm/s). Furthermore, the wide bandgap offered by GaN HEMT devices makes them perfect candidates for RF devices and certainly for successors of LDMOS devices in the mobile telecommunication segment. The wide bandgap property of GaN is particularly desirable for this project. The wide bandgap offered by GaN allows higher breakdown voltage. Thus the active device can withstand higher VSWR than LDMOS when terminated with a mismatched load. Later in chapter 3, it will be shown that the active devices in an outphasing system are presented with an active load that can take any values from purely resistive to purely reactive, almost open-circuit conditions.

1.2 Research Objectives

The subject of outphasing has been heavily researched over recent decades, leading to a wide range of available research publications. However, there are very few commercially available outphasing systems, and those existing on the market are usually mixed with other efficiency enhancement techniques such as Envelope Tracking (ET) rather than standalone systems. It should be emphasised that Chireix PAs are notoriously cumbersome for the HB (Harmonic Balance) solvers when it comes to non-linear simulations using the models of commercially available active devices. Convergence problems are not uncommon when higher-order harmonics are considered in simulations where two or more saturated or overdriven active

devices interact with each other. It is one of the examples where somewhat straightforward trigonometric equations look trivial on paper but can cause problems for systematic computer algorithms such as HB solvers. Moreover, the frequency dependence of several key components and their sensitivity for variation makes the first-pass design of outphasing PAs particularly difficult to achieve and depends on the fabrication technology. Tuning options are usually minimal for the fabricated PAs. The research objectives are based on the limitations of Outphasing PAs, which were discussed in detail in Chapter 3, and where the existing research is either limited, absent or inconclusive.

Successful implementation of outphasing PA, suitable for operation with signals employed in the modern telecommunication systems, requires extending the bandwidth of this inherently narrowband technique. Therefore, the main focus of this thesis is to eliminate or improve the key elements contributing to the narrowband operation.

The first objective is to investigate whether a broadband balun used as a power combiner in an outphasing system can lead to improvements in its frequency response. Single-ended termination in outphasing systems is typically realised using λ/4 Transmission Lines (TL), intrinsically narrowband structures, and this is the most prevalent solution reported in the literature. Surprisingly, given the differential nature of load termination in outphasing, there are very few documented attempts of using balun as a power combiner in such systems. A significant part of this task is allocated to the design, fabrication and characterisation of the suitable balun. Further improvements are expected by using bare die GaN HEMTs rather than packaged devices, thus eliminating parasitic elements associated with the former.

Characterisation and verification of outphasing require a measurement setup capable of generating two phase-coherent RF signals. Instrument synchronisation

and frequency locking using a 10 MHz signal was deemed unsuitable for this purpose. Therefore, deployment, commissioning and evaluation of the dedicated measurement system formed the second part of the objectives.

1.3 Thesis Organisation

The first three chapters contain introductory material. The essential background information was provided in **Chapter 2**, where the concept of load modulation is introduced along with the most common applications in PA design. The chapter is concluded with the description of Class J PA as an example of a continuous mode PA family. The entire **Chapter 3** was dedicated to Chireix outphasing. The chapter starts with brief history of this technique, and is followed by theoretical and analytical explanation of the classic approach to outphasing. The comprehensive literature review with the most recent state-of-the-art PAs concludes that section.

The experimental work was described in Chapters 4 – 7**. Chapter 4** was split into two main parts, each dedicated to the outphasing PA circuit designed during this research. Each part starts the design process, simulation and characterisation of the balun, which is then used as a power combiner. Each part of Chapter 4 was concluded with characterisation and measurement results for each PA.

Chapter 5 was entirely dedicated to the concept of CMOP – the main novelty described in this work. The first part of the chapter contains the description of the COMP concept using ideal device models, followed by a discussion on input drive strategies, outlining the relative advantages and disadvantages of each strategy. Description of PA circuit design process was provided in the middle section, which is then followed by characterisation process and experimental results.

The measurement system tailored for the characterisation of dual input PA was described in more detail as it was built as part of this research and formed an integral part of it. Two measurement systems used during this research were described in Chapter 6. The information contained in the section on the active load-pull was intended to support work described in Chapter 7.

Chapter 7 contains additional research related to the thesis. In both cases, it involves numerical modelling of GaN HEMT devices, supported with experimental verification.

Chapter 8 concludes and summarises the work described in this document. The outcomes of this research and review and possible future directions for this project are explored.

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CHAPTER 2

BACKGROUND

2.1 Reduced Conduction Angle PAs

RF Power amplifiers have conventionally used the “reduced conduction angle” approach in order to improve the efficiency over a basic Class A design. For over a century, these modes have been assigned letters of the alphabet, A, AB, B, C, to indicate decreasing conduction angle, giving increasing efficiency but decreasing power gain. This approach is well known and widely covered in several generations of textbooks and courses, and the details will not be duplicated in this thesis. A seminal book that covers the subject thoroughly is given in [1]–[4].

One aspect of reduced conduction angle modes that is not so well covered in older texts and references is the treatment of the harmonic components, which become increasingly significant as the current waveforms become more pulse-like. Conventionally, these harmonics were short-circuited, so that the output waveform was sinusoidal. This process was relatively straightforward in the days of vacuum tubes, which displayed a high output fundamental impedance which was matched using high Q resonators which morphed into radial or coaxial cavities at GHz frequencies. At lower frequencies, even harmonics could alternatively be shorted using a push-pull configuration.

More recently, the use of solid state (transistor) devices has led to some important variations on the shorted harmonic approach. Class F, which retains some third harmonic component, and yet more recently, Class J, which utilises residual

second harmonic, respectively in the output voltage waveform, not only give improved performance but can be easier to implement when the fundamental output impedances are very low in comparison to the historical vacuum tube applications. Most recently, an entirely new set of modes has been described, and termed “Continuous Modes”, which make extensive use of harmonic components in the device voltage waveforms. These modes are of very recent origin and will form an important component in work reported in this thesis. As such, a more detailed description forms a part of this Chapter.

2.1.1 Continuous PA modes

A recent and important discovery in PA design has been continuous modes [2], which have enabled the combination of harmonic tuning and broadband operation. Originally introduced as an extension of class B for purely reactive second harmonic terminations, the approach has now been applied to many different PA classes and cases [5]–[7]. This section describes the continuum of class B operation, which is referred hereafter to as class J.

The Class J is the example of successful application of waveform engineering to shape a drain voltage and current responses by providing a proper set of fundamental and second harmonic termination.

Starting with the assumption of class B mode of operation, consideration is only given to fundamental and second harmonic frequencies. Higher order harmonics are assumed to be negligible for the purpose of this analysis. When half rectified sine wave operation is adopted, the drain current can be defined as

$$i_d(\theta) = I_{\max}\left(\frac{1}{\pi} + \frac{1}{2}\sin(\theta) - \frac{2}{3\pi}\cos(2\theta)\right) \tag{2.1}$$

The basic assumption made in the construction of continuous modes is the zero-grazing condition for the voltage waveform, that limits the clipping of the current waveform and leads to the definition of the continuum itself. The drain voltage waveform described in (2.2) meets this condition, and can be rearranged to be expressed using the operator $(1 - \alpha\sin(\theta))$ as shown in (2.3).

$$v_d(\theta) = V_{\mathrm{K}} - (V_{\mathrm{DC}} - V_K)\left(\cos(\theta) - \sin(\theta) + \frac{\sin(2\theta)}{2}\right) \tag{2.2}$$

$$v_d(\theta) = V_K + (V_{\mathrm{DC}} - V_K)(1 - \cos(\theta))(1 + \alpha \sin(\theta)) \tag{2.3}$$

The harmonics in the voltage waveform are generated by the drain current $i_d(\theta)$ flowing through the parasitic capacitor C_{DS}.at the generator plane. Assuming zero knee voltage V_K, the derivations from (2.1) and (2.3) were plotted in for $-1 < \alpha < 1$, with the special case $\alpha = 0$ representing typical waveforms of a class B mode of operation. In each case, the newly derived set of waveforms provides the same performance as predicted by class B operation.

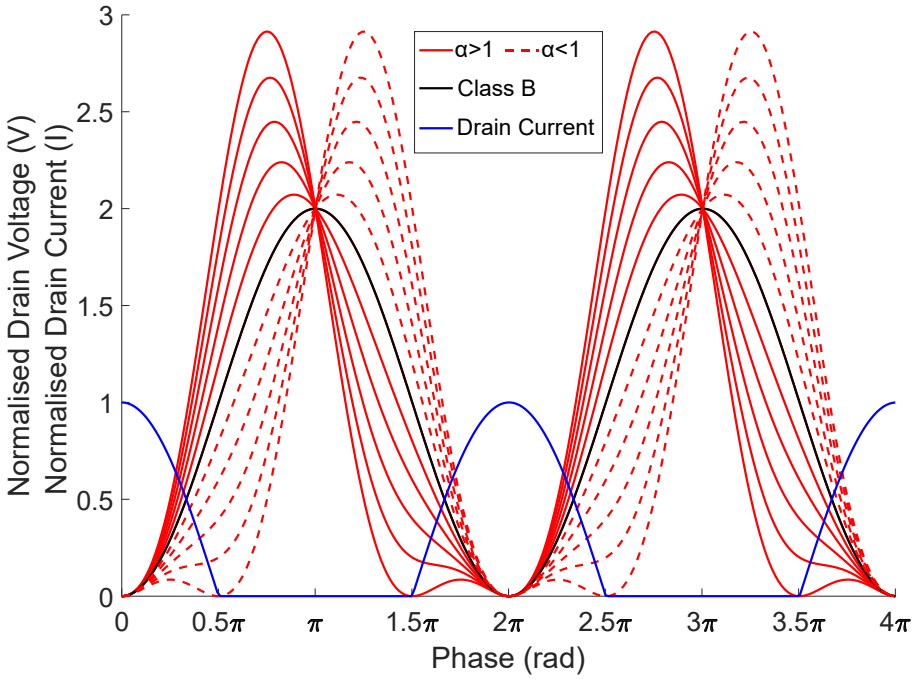

Figure 2.1 - Voltage and current waveforms produced by a PA operating in the class J. Voltage variation for different parameter a is shown and compared to class B operation.

The impedances Z_1 and Z_2 corresponding to the fundamental and second harmonic load terminations required to create such set of waveforms can be obtained from (2.1) and (2.3) with a further definition of the optimum intrinsic load impedance R_{opt} given in (2.6).

$$R_{\text{opt}} = \frac{2(V_{\text{DC}} - V_K)}{I_{\max}} \tag{2.4}$$

$$Z_1 = \frac{(V_{\text{DC}} - V_K)(1 + j\alpha)}{\frac{I_{\max}}{2}} = R_{\text{opt}}(1 + j\alpha) \tag{2.5}$$

$$Z_2 = \frac{-(V_{\text{DC}} - V_K)(j\alpha)}{\frac{4I_{\max}}{3\pi}} = -j\alpha\frac{3\pi}{8}R_{\text{opt}} \tag{2.6}$$

All fundamental and second-harmonic impedances plotted on Smith chart in Figure 2.2 result in the same output power, gain, and efficiency. This continuum of impedances provides the flexibility of choosing the design space and has been shown to extend bandwidth exploited in many research papers [8], [9].

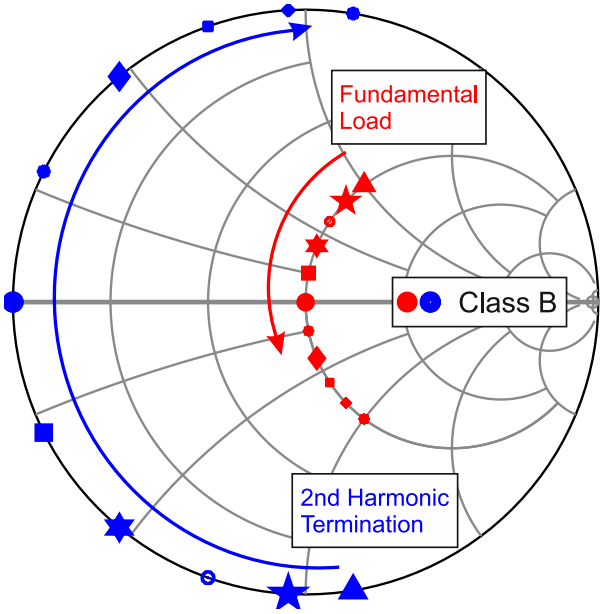

Figure 2.2 - Load termination at fundamental and 2nd harmonic frequencies for Class B Continuum.

The trajectories shown in Figure 2.2 present an interesting opportunity in a load modulated environments described later in this section. With a careful consideration during the design process, it was shown in Chapter 4 that the load

modulation in outphasing PA can be maintained at harmonic frequencies as long as the combining structure have sufficient bandwidth. It should be noted that the analysis presented here, assumes no influence from the presence of the 3rd and higher order harmonics.

One of the fundamental assumptions in the outphasing theory presented in Chapter 3, is the operation in a saturated region of given active device. Therefore, application of Class-J in outphasing branch PAs could be questionable due to the “zero-grazing” assumption. Later in Chapter 7, the “zero-grazing” condition was challenged and a Class J operation was demonstrated for saturated GaN HEMT devices.

2.2 Load Modulation Techniques

This section describes a technique where two or more sources, which model active devices in a simplified form, are terminated into a common load in a non-isolated manner. This way, the impedance presented to each device depends on the physical termination as well as the output from each source. The load modulation effect is the underlying principle of the Load Modulated Balanced Amplifier (LMBA), Chireix and Doherty PAs – all described in the next sections of this Chapter.

The term *Load Modulation* is typically used to describe a process where an apparent impedance of a fixed load is dynamically changed. This is usually achieved when two or more active devices are connected to the common load, as shown in Figure 2.3. In this scenario, the impedance presented to one device, depends on the fixed load as well as the output from the other device. Often named as load-pulling, the device #2 pulls the load seen by device #1. It is assumed that the name load-pull in this thesis is used exclusively to refer to measurement system and technique, which were further described in Chapter 6.

The ability to alter the impedance presented to the PA is used to improve the back-off efficiency of the given PA. In fact, since maximum efficiency of the device is achieved when the output voltage is grazing zero, only a loading impedance that varies with the amplitude of the current can guarantee zero grazing at levels of output power, in presence of a fixed drain bias voltage.

2.2.1 Principle of Operation

Figure 2.3 shows a simplified diagram of load modulation taking place between two active devices, represented by current sources. The fixed single-ended load R_L is connected to the output node from the generators. The equations (2.7) – (2.9) govern voltages and currents in this circuit.

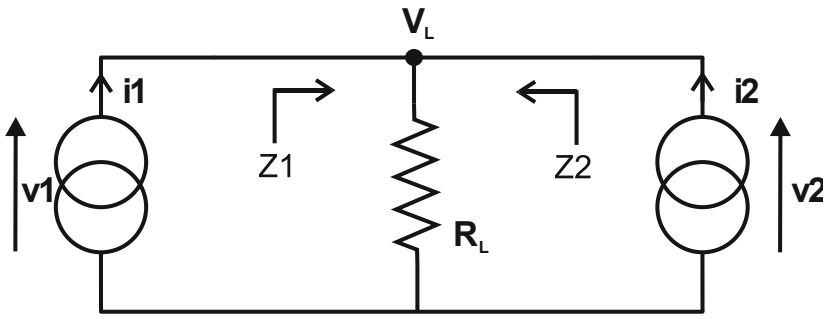

Figure 2.3 - Simplified schematic illustrating ac active Load-Pull concept.

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} R_L & R_L \\ R_L & R_L \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{2.7}$$

After expanding the matrix, it can be shown that the impedance seen by each branch, denoted as Z_1 and Z_2 is a function of the fixed load resistance and currents from both generators. Therefore, a change in output from one device will result in a change of operating conditions for the second device and vice versa.

$$Z_1 = R_L(1 + i_2/i_1) \tag{2.8}$$

$$Z_2 = R_L(1 + i_1/i_2) \tag{2.9}$$

2.2.2 The Doherty PA

After careful examination of the load modulation circuit from the previous section, it becomes apparent that the output voltages from both generators are identical and increase proportionally to the increase in output current. Achieving a constant voltage swing at the output during back-off operation is therefore not possible in such configuration. The classical solution to de-coupling both devices was proposed by Doherty in 1936 [10]. He proposed to use two active devices that will remain on until a certain back-off level is achieved, 6 dB in the case of the original paper. The two PAs are often referred to as *main* and *auxiliary.* The auxiliary typically reaches its maximum efficiency at the designated OBO level, while the former remains off until this level is reached. For power levels greater than the chosen OBO

point, power from both PAs is combined in the manner that will be shown later in this section.

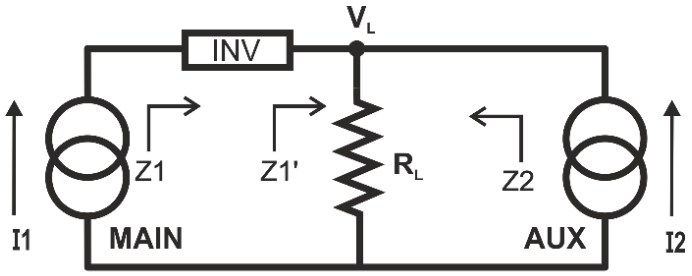

Figure 2.4 - DPA schematic.

The essential component of a DPA is an impedance inverter, as shown in the diagram in Figure 2.4, which is used to invert the impedance Z1 into Z1' proportional to 1/Z1. This ensures that the increase in output current I1 results in decrease in impedance presented to the device, thus allowing for a constant voltage swing. The inverter, which is typically realised using a quarter-wave transformer in form of TL, introduces an undesired phase shift into the circuit that needs to be compensated / offset at the input stage using either another quarter-wave transformer, as in Figure 2.5 or a hybrid splitter [11].

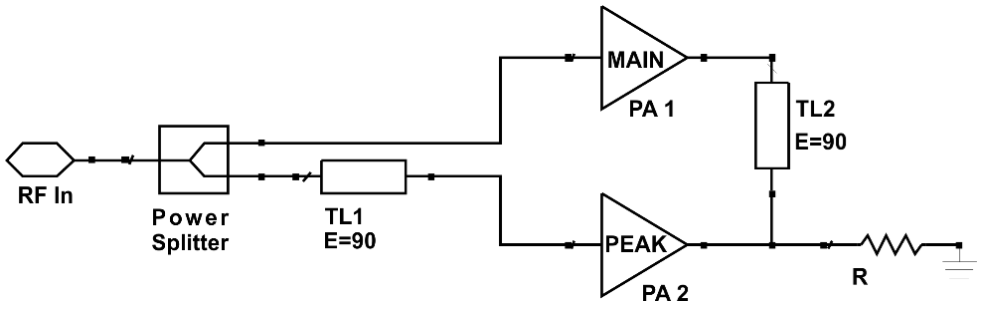

Figure 2.5 - Schematic of a typical Doherty PA.

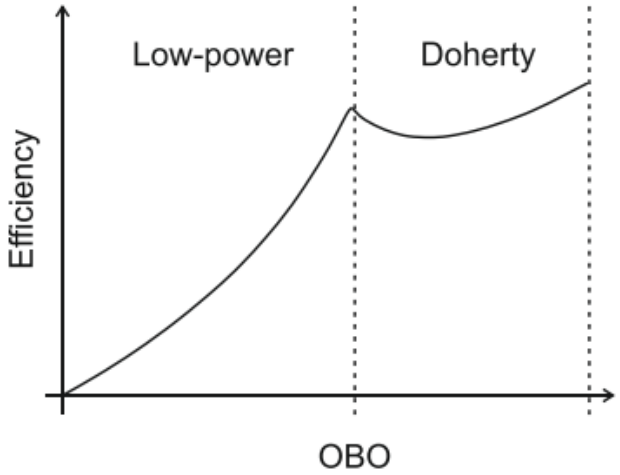

Figure 2.6 - Efficiency plot for DPA, as in classical arrangement OBO is 6 dB (reproduced from [9])

The typical efficiency achieved by DPA is shown in Figure 2.6, where two operating regions can be distinguished. Up to the OBO power level only the main PA is contributing to the total output power, where its load impedance is $2R_{OPT}$. Power levels greater than OBO are realised using both PAs. In the classical implementation of DPA, the common load R_L is chosen as $R_{OPT}/2$, where R_{OPT} is the optimum load termination for class AB PA. To ensure that the Aux device remains switched off during low-power mode, a Class C PA is adopted with a properly selected bias point.

Despite many advantages, this topology has limitations too. The mismatch in gain profile introduced by using a class C as the peaking amplifier creates an imbalance in output currents as PA biased this class typically supplies less output current than class AB equivalent at the same input drive. The most common solution for this issue is an implementation using devices of different size and maximum power output levels, typically referred to as *Asymmetrical* DPA. Furthermore, highly non-linear operation in Class C introduces signal distortion and offers low gain, when compared to class B or AB. Bandwidth limitations arise from using frequency-dependent components in the design and reliance on matching networks to ensure that load modulation follows designated values. The latter is often impeded by non-

linear parasitic elements of an active devices, which vary with frequency and operating conditions.[9]

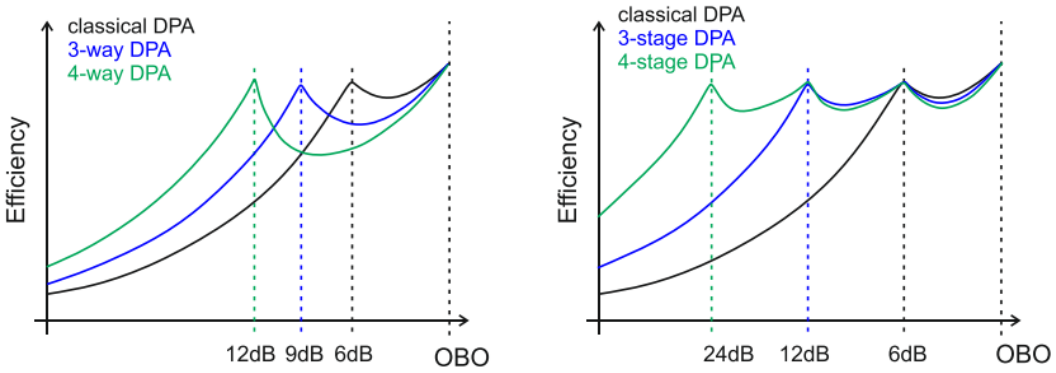

Figure 2.7 - Efficiency plot of multi-way and multi-stage realisation of DPA (reproduced from [9])

The literature offers many expansions of DPA into cascaded multi-way and multi-stage topologies, with the corresponding efficiency plots as shown in Figure 2.7. The difference between each approach comes from either using a single Main device with a number of Aux PAs, designed to turn on at a given power levels or in the case of multi-stage solution, using cascaded pairs of Aux/Main devices [13].

2.2.3 The Chireix PA

Outphasing is another efficiency enhancement technique introduced in the 1930s, based on the load modulation technique. Chapter 3 is entirely dedicated to this subject, and it is only being mentioned here for quick comparison with other load modulation topologies presented in this Chapter.

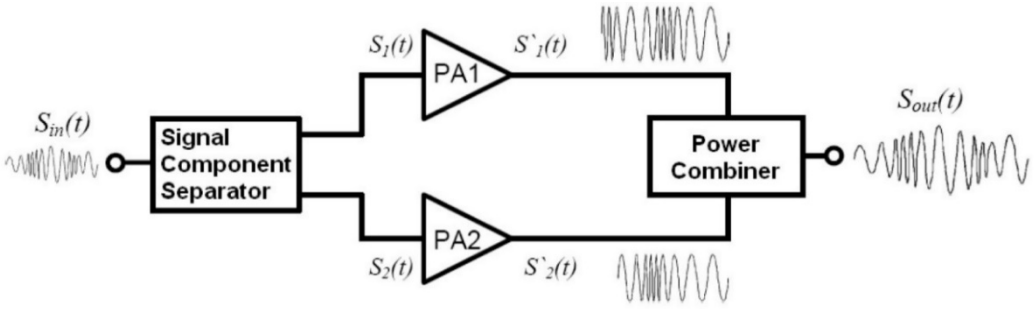

Figure 2.8 - Chireix Outphasing diagram.

In Outphasing, the efficiency is preserved by amplifying signals of constant amplitude at the peak efficiency for a given PA. The signal containing Amplitude Modulation (AM), is decomposed into two signals of a constant amplitude, where the AM information is preserved in the form of a relative phase between new signals. The amplified signals are recombined by the means of vector summation at the output as shown in Figure 2.8. Upon a close inspection, Chireix outphasing is more of a modulator rather than PA. In the classical implementation of this topology two active devices operate at a constant power level, where efficiency typically peaks.

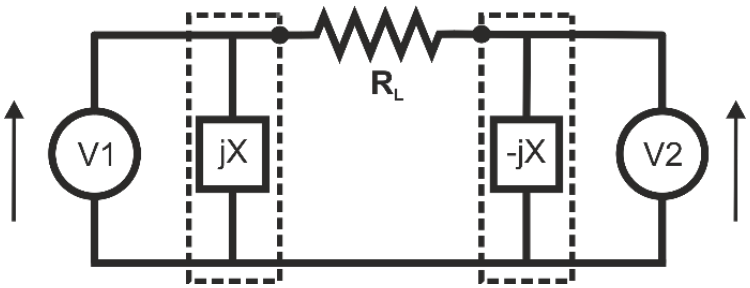

Figure 2.9 - Outphasing circuits, shwoing inclusion of compensation elements (right).

Looking at the circuit in Figure 2.9, the first notable difference with Doherty PAs is the load R, which is connected differentially across the outputs from each generator. Moreover, the Load modulation in outphasing takes place as a result of varying phase between signals (unlike in DPA, where the magnitude of the output current was varied). Finally, devices are treated as voltage sources as a strong approximation of their behaviour when pushed into saturation.

2.2.4 Load Modulated Balanced Amplifier (LMBA)

A more recent advancement in load modulated amplifiers is a variation of the balanced power amplifier structure [14]. The LMBA alone deserves much more scrutiny and description than it is required for the purpose of this thesis, so this section briefly introduces the concept, while further information can be obtained from [15].

Unlike in two previous examples, this concept uses an external control signal to regulate load modulation and the impedance presented to each active device. The control signal is referred to as CSP, as in the original concept presented in [14]. Still, the CSP can be derived from a single RF generator by means of a power splitter or coupler.

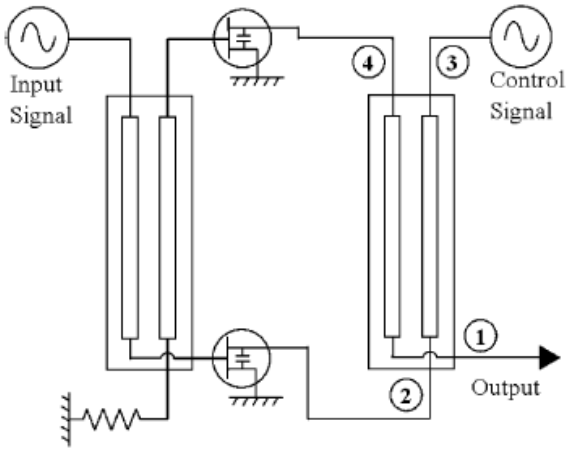

Figure 2.10 – Schematic of LMBA (reproduced from [12])

The CSP is introduced through an isolated port in the output hybrid coupler, as shown in Figure 2.10. In the classic implementation of a balanced topology, that port is typically terminated with a 50 Ω load. The signal with current amplitude and phase given as $I_c e^{j\varphi}$ transforms the impedance for each active device in the same manner and is given by

$$Z_A = Z_0 \left(1 - \sqrt{2}\, \frac{I_c e^{j\phi}}{I_b}\right) \tag{2.10}$$

$$Z_B = Z_0\left(1 - \sqrt{2}\,\frac{I_c e^{j\phi}}{I_b}\right) \tag{2.11}$$

Where I_b is the current of each PA and is assumed to have equal magnitude and quadrature-phase offset typical for balanced amplifier topology, and Z_0 refers to the characteristic impedance of the coupler.

The modulation of impedances Z_A and Z_B is achieved by adjusting the power delivered by CSP and described as a ratio to the output power from each branch PA, denoted as α. Authors of [14] state α = 1/4 as the condition to modulate the impedance presented to each active device by a factor of 2, so the CSP is 6 dB lower than that being delivered by a single PA, or 9 dB down from the total output. The very important feature of LMBA is a full recovery of power injected from CSP, which contributes to the overall output power.

The concept was further refined in [16] and evaluated as an efficiency enhancement technique. Authors report 800 MHz bandwidth centred at 2.1 GHz and PAE of 48%, 43% and 39% for saturation, 6 dB and 8 dB OBO. Characterisation using LTE modulated signal returned PAE of over 40% and the average power of 10 W after linearisation using DPD.

2.3 Baluns and their Application in Power Amplifier Design

This section introduces the concept of the balun and briefly describes its typical role in PA design. Baluns are widely used in RF/microwave designs, and their desired parameters can vary across the applications. For the PA design space, the transformation property of the balun is typically exploited for splitting and combing power, with the latter particularly investigated for outphasing circuits in Chapter 4. Following a brief introduction of the structure, some applications will be described with a discussion on the various solutions available in the literature, considering their potential usefulness in outphasing circuits.

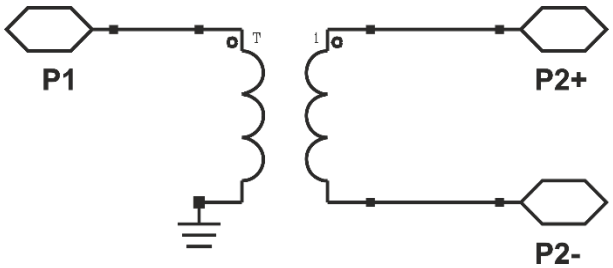

Figure 2.11 - Simplified schematic of a typical balun.

Figure 2.11 shows a simplified schematic model of a typical balun (combination of words balance-unbalance). The structure allows a single-ended, unbalanced ground-referenced signal to be transformed into a balanced, differential signal by means of magnetic coupling. This property makes the balun an indispensable component in many RF and microwave architectures, including filters, mixers, antennas, and power amplifiers (PAs). However, while realising baluns at sub-GHz frequencies is somewhat straightforward and well documented, the design for higher GHz bands often results in trade-offs between the different figures of merit, thus reaching an octave bandwidth while maintaining amplitude, phase balance and acceptable losses can be challenging [17].

One of the main objectives of this thesis is the investigation of bandwidth improvements by using a broadband balun as a power combiner in outphasing PA. The term broadband in this case refers to a bandwidth covering fundamental and harmonic frequencies, which consequently would allow a load modulation at these frequencies. It is shown in Chapter 4 that class J-alike termination was achieved by means of load modulation alone, which was possible because of the inclusion of the second harmonic frequency in the balun's bandwidth. Any insertion losses introduced by the balun will have a detrimental effect on the overall efficiency of the PA. Finally, trace separation defined as a difference in power split from Port 1 between Ports 2 and 3, which can be observed as a difference in S12 and S13. The significant difference would lead to unequal loading of each branch PA, which could lead to the physical damage of active devices or result in operation different from outphasing. The operating frequency was chosen to be around 2 GHz, which is common to many telecommunication standards. Another desirable feature offered by the balun is the characteristic impedance presented at the balanced ports when operating in the odd mode. This impedance is typically half of the single-ended Z_0, which usually is 50 Ω. Thus, the odd impedance presented for the balanced output between ports 2 and 3, can be exploited in the choice of the active device for the outphasing PA. Ideally, the Z_{odd} in such case would have a value close to the optimum load at intrinsic plane of the chosen active device.

The subject of baluns, both coaxial and planar, was the subject of research on several occasions within the CHFE (Centre for High Frequency Engineering), with some interesting observations leading to improvements in performance. In each case, the coupling of the structure to the *main* ground was identified as the major factor contributing to performance degradation. Multi-octave bandwidth was achieved in [18] by a balun made from a section of semi-rigid coaxial cable and suspended over a cut-out slot made in the carrier PCB. The increased distance to the ground was shown to

improve the performance of the balun, with further improvements achieved using a ferrite bead mounted on the outer conductor. The application of ferrite in balun design is a widely documented method of suppressing higher-order resonances and has been successfully applied to structures fabricated using both coaxial semi-rigid cable [19] and planar structures [20]. This approach, however, often leads to extra-losses making this method less desirable if efficiency is the main design target.

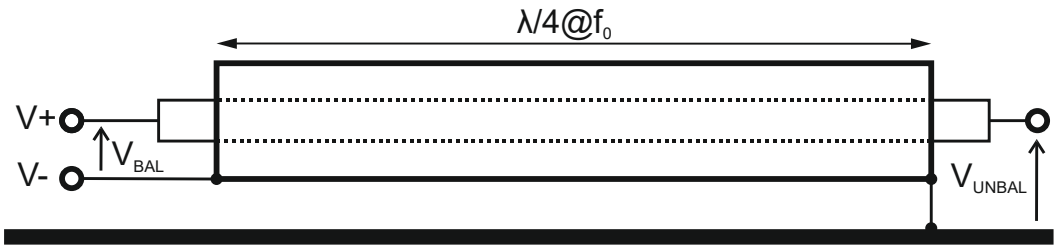

Figure 2.12 – Representation of a balun realised using a λ/4 section of coaxial cable.

The parasitic ground coupling was investigated in planar baluns, such as the Marchand structure, and described in [21]. The authors show that the trace separation in balun structure realised using a co-planar TLs, can be attributed to the unwanted, additional TL formed between the inner conductor and ground as depicted in Figures 2.12 and 2.13. The observations and derivations from that work, were subsequently employed in the design of the balun used in this work and described in Chapter 4.

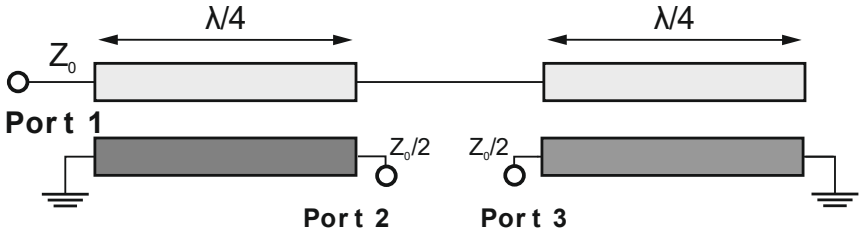

Figure 2.13 - Planar balun realised using transmission lines. Single-ended input at Port 1 is transformed into balanced output between Ports 2 and 3.

Baluns with considerably larger bandwidths can be achieved using multilayer structures, for example, GaAs MMIC as shown in [22]. However, such solutions were excluded from this project due to the complexity, losses, and cost involved in fabrication.

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CHAPTER 3

OVERVIEW OF THE CHIRIEX OUTHPASING TECHNIQUE

This thesis, and all of the work reported herein, is entirely focused on the Outphasing PA technique, first described by Chireix in a seminal 1936 paper. As such, a more detailed description of the technique itself will be given, and its evolution over the subsequent time summarized. Despite much work that has been published at the research level, it is fair to say that outphasing has not shown the same level of commercial implementation in wireless communications systems that has occurred for other techniques described in Chapter 2, such as the Doherty PA and Envelope Tracking (ET). Some reasons for this will be described in this chapter, as they form in part the motivation for the work described in later chapters; most notably, limited bandwidth and the dependency of the Chireix analysis on active devices behaving as voltage sources.

The first part provides a brief historical background, followed by the theory of operation and analysis of outphasing PAs. The key components of a typical outphasing system are described and discussed. The effects of load modulation are investigated in detail, and the analysis is extended to include effects of compensation elements. The analysis is concluded with mathematical description of outphasing PAs, which is also intended to serve as comparison for equations derived for the CMOP approach introduced in Chapter 5. The second part of this chapter provides an overview of modern implementations of outphasing PAs, that are available and presented in literature. A review of existing publications dedicated to this subject is

provided with assessing achieved performance, which is used as a reference for the prototype amplifiers presented in Chapters 4 and 5. Limitations and conclusions of the outphasing approach are discussed in the final section.

3.1 Introduction

The outphasing technique, proposed by Chireix in 1935 [1], is one of the classical methods of addressing efficiency degradation caused by operating a power amplifier (PA) in output back-off (OBO), where efficiency is typically low. Essentially, the envelope from the input signal is eliminated, and two CW signals are constructed; these have a constant amplitude, while their relative phase holds the information originally contained in the amplitude modulation. Consequently, efficiency improvements are achieved by amplifying signals with constant amplitude using PAs operating in saturation, where efficiency typically peaks. The envelope is restored at the output by means of a vector summation of both signals, using a non-isolating combiner at the output stage [1].

Chireix sold his patent to McClatchy Broadcasting, who is credited with the first documented outphasing transmitter deployed in 1948 [2], with commercial outphasing transmitters being introduced in the early 1950s by RCA under the name *Ampliphase*. These were manufactured and supported throughout the 1960s until the early 1970s. These commercial units were capable of generating signals up to 100 kW AM for broadcast. To the authors knowledge, there is just one operational unit left, a 50 kW model BTA-50H, which is maintained as an auxiliary transmitter at the KFBK radio station in California, USA [3]. Authors in [2] refer to a document indicating a great deal of interest in Ampliphase by the BBC at that time, with their own trials with outphasing taking place in the 1940s in collaboration with Marconi.

The commercial outphasing Ampliphase attracted its customers by having lower initial costs, as, unlike the non-outphasing solutions, Ampliphase transmitters did not require modulation transformers. The savings were apparently offset by higher maintenance costs due to the reported reliability issues [2].

Despite its promising benefits of improving efficiency, the outphasing systems suffer from a number of shortcomings. Some of these shortcomings were observed in the early commercial deployment of Chireix concept and include PM/AM distortion present on the recombined output signal. In fact, the total signal cancellation using phase manipulation is purely theoretical and very difficult to implement, if not impossible. As a result, the residual amplitude is always present on the output signal, which cannot reach 0 V. This was further shown during calibrations of the measurement system described in Chapter 6. Ampliphase addressed the issue of linearity with a rather elegant solution for reducing input drive. A resistor was added between/across grids of driving amplifiers. Considering input signals that were in phase, there would be no current flowing through the resistor. However, this would not be the case for input signals out of phase, as there would be a significant power dissipated in the resistor, enough to sufficiently back-off the input signal [2].

The refinements to the outphasing technique proposed by Chireix were originally designed for high-power broadcast stations used to transmit TV and radio signals. These transmitters were based on vacuum electron devices or vacuum tubes. It would take a good few decades before semiconductor devices would replace the vacuum tubes in high-power PAs. This, perhaps obvious detail, is crucial in the context of Chireix's work. The derivations and analysis in the first part of this chapter closely follow that proposed by Chireix in his original work. At first sight, the concept of active devices operating as voltage generators and the floating load termination, although appropriate in the context of using vacuum electron devices, is perhaps not well-suited to the application of modern semiconductor devices, as the assumptions pose difficulties when implementing outphasing PAs using semiconductor technology at microwave frequencies.

3.2 Theory of Operation

The term outphasing or Chireix outphasing describes the concept proposed by Henri Chireix in 1935 as an effective method to address efficiency drop in RF power amplifiers caused by operating in OBO conditions, where the efficiency of a PA is typically low. It was shown in Chapter 2 that the efficiency of a PA, terminated with its optimum load impedance $R_{L,}$ quickly degrades as the output power is reduced. The reduction of output power requires the reduction of either drain current (I_D) or DC supply voltage (V_{DD}). The latter is exploited in envelope tracking systems and is not discussed here. A full available voltage swing at the output with a reduced drain current I_D, requires a load with higher than optimum impedance since $R_{OPT} = 2V_{DD}/I_{OBO}$, where $I_{OBO} < I_{MAX}$ For a PA operating in class-B, the drain efficiency is reduced by 3 dB if output power is backed-off by factor of 6 dB.

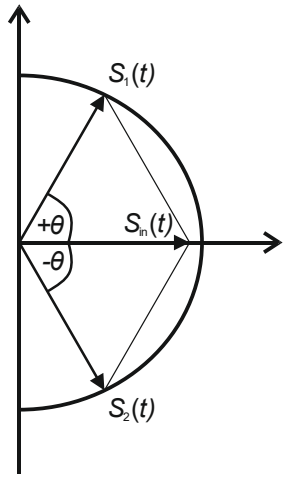


Figure 3.1 - Vector representation of signal composition in the outphasing concept (reproduced from [4]). The driving signals S_1(t) and S_2(t) are created with an equal amplitude and phase difference corresponding to the amplitude of S_{in}(t).

$$S_{\text{in}}(t) = A(t)\ \cos(\omega t) \tag{3.1}$$

$$S_1(t) = \cos(\omega t + \theta) \tag{3.2}$$

$$S_2(t) = \cos(\omega t - \theta) \tag{3.3}$$

$$\theta = \cos^{-1}\left(\frac{A(t)}{\max(A)}\right) \tag{3.4}$$

$$S_{\text{out}}(t) = S_1(t) + S_2(t) \tag{3.5}$$

In the outphasing concept, efficiency is preserved by amplifying signals of constant amplitude at the peak efficiency for a given PA. The original signal containing Amplitude Modulation (AM) given as (3.1), is decomposed into two signals of constant amplitude (3.2)-(3.3), as shown in Figure 3.1, where the AM information is preserved in the form of the relative phase between new signals, described in (3.4). The amplified signals are recombined by means of vector summation at the PA output (3.5) [5].

A typical outphasing system was shown in Figure 3.2, where the three key elements are identified; firstly, a signal conditioning module, referred to as a Signal Component Separator (SCS), two or more similar PAs and finally, a power combiner. The role of SCS is to, using the input signal, create two new constant amplitude signals with the required phase offset as described earlier. Given the prevalence of modern DSP capabilities, this element is assumed to be easily realised within a digital software environment such as Matlab, and will not be discussed further in this Thesis. However it should be noted that SCS capability can be extended beyond its original purpose. Additional signal conditioning at this stage can, for example, incorporate DPD (Digital Pre-Distortion) or can be used to realise the *Mixed-Mode* operation, that was described later in this chapter.

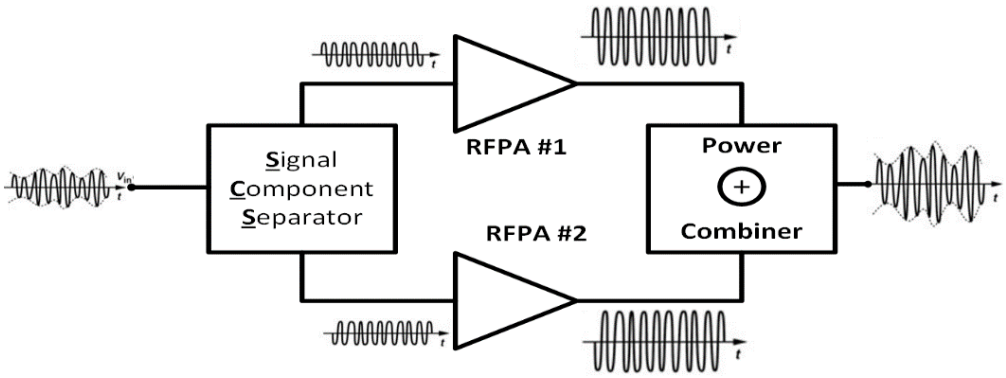


Figure 3.2 - Typical Chireix Outphasing, showing key system components.

To preserve Chireix's derivations from his original work, designed for thermionic valves, which are typically modelled as voltage sources, the branch PAs are assumed to be operating in a deep saturation, where they usually achieve peak efficiency. This assumption will be challenged in Chapter 5, and in Chapter 4, it will be shown that although saturated devices can act as constant voltage sources, they are limited by the finite current they can deliver. In other words, the transistors within the branch PAs, when approximated as voltage sources, will not be able to deliver the constant voltage for certain load impedances, thus defying the approximation.

Another crucial observation when operating branch PAs at constant output power and in deep saturation, is the fact that the DC component at the output of each device remains constant at all times, while the overall PA output power varies with the outphasing angle. This is reflected in poor gain and PAE figures, with the latter often significantly deviating from drain efficiency figures for outphasing PAs. The issue of poor gain performance becomes more evident when signals employed in the modern telecommunication systems such as OFDM are considered, where PAPR figures can be close to gain offered by the active devices.

The obvious choice here is to realise OBO through a combination of AM and PM, i.e., control of both the amplitude and phase of input signals. In fact, the necessity to back-off the input signal in order to avoid compromising gain and hence preserve

PAE, was acknowledged and implemented in a number of previous works dedicated to outphasing [3,4,5,6]. The term "Mixed-Mode" outphasing is often used in literature to describe the technique where signals driving an outphasing structure are constructed using both amplitude and phase control. The Mixed-Mode approach is presented in [7], with only a short explanation provided to describe the theory driving the design process. Authors of work in [6] determine experimentally the phase threshold where outphasing is no longer utilised, and their PA operates in class B. Another approach to control output voltage in outphasing amplifiers was shown in [8], where authors use a discrete modulation of drain voltage supply in a similar fashion to envelope tracking.

Interestingly, none of the aforementioned published research has attempted to refine the classic outphasing theory based on voltage source approximation, which is no longer valid if the amplitude of driving signals is backed-off. A simple investigation of the circuits in Figure 3.7, reveals that the analysis of these circuits changes fundamentally if voltage generators are substituted by current generators, which are typically and more commonly used for modelling of active semiconductor devices. This observation will be expanded in Chapter 6 with further, novel refinements to “mixed-mode” outphasing, introduced through the concept of Current Mode Outphasing (CMOP).

In his work, Chireix proposed a non-isolating power combiner to enable load modulation to work properly. While the theory assumes a floating load connected differentially across output of each PA, which is valid and appropriate when considering vacuum electron devices, the practical solutions for semiconductor devices will be described later in this section. Chireix’s work was intended for PAs based on vacuum electron devices, which in fact are typically modelled as voltage sources. The relatively high voltages seen at the output, often described in multiples of 10s of kV for high power TV or radio broadcasting transmitters, required radically

different approach to load connection. The load was typically an antenna with a balanced feed, and occasionally, the output from such PAs was coupled to a low impedance load using transformer or a resonant cavity, where the load would indeed be “floating”.

3.3 Analysis of Outphasing Circuits

The basic Chireix configuration is shown in Figure 3.3. Two voltage sources, whose relative phase can be adjusted, are series connected into a “floating” load. The key aspect of this circuit is that the two device outputs are not combined in a conventional manner but interact with each other. So as the phase is varied, the load presented to each device varies substantially and can be tailored to maintain good efficiency as the overall combined power is reduced.

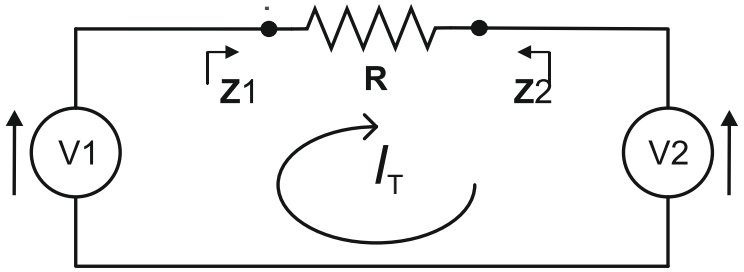


Figure 3.3 - Equivalent circuit describing Outphasing PA without compensation.

Both voltage sources have equal magnitude *V* and phase offset *θ,* here also refered to as the outphasing angle.

$$V_{1,2} = V \cdot e^{\pm i\theta} \tag{3.6}$$

Total current in the circuit I_T is given by

$$I_T = \frac{V_1 - V_2}{R} = \frac{V}{R} \cdot 2j \sin\theta \tag{3.7}$$

The impedance Z_1 and Z_2 represent the load impedance seen by each of the voltage source and it is given as

$$\boldsymbol{Z_{1,2}} = \frac{V_{1,2}}{I_T} = \frac{R}{2}(1 \mp j \cot\theta) = \frac{1}{\boldsymbol{Y_{1,2}}} \tag{3.8}$$

The derived impedances from this analyisi are plotted on Smith chart in Figure 3.4, with the real and reactive parts plotted seperately in Figure 3.6. From these plots, it can be observed that as the reative phase between input signals varies, the load impedance presented to each PA changes from R/2 for $\theta = 90°$ to open circuit conditions for $\theta = 0°$. The latter represents a case where the PA operates in push-pull configuration. It is clear from (3.8) that the real component of the load impedance is constant and is not affected by the outphasing.The reactive part however varies with phase and output power reduction is realised by combining both output signals in a destructive way.

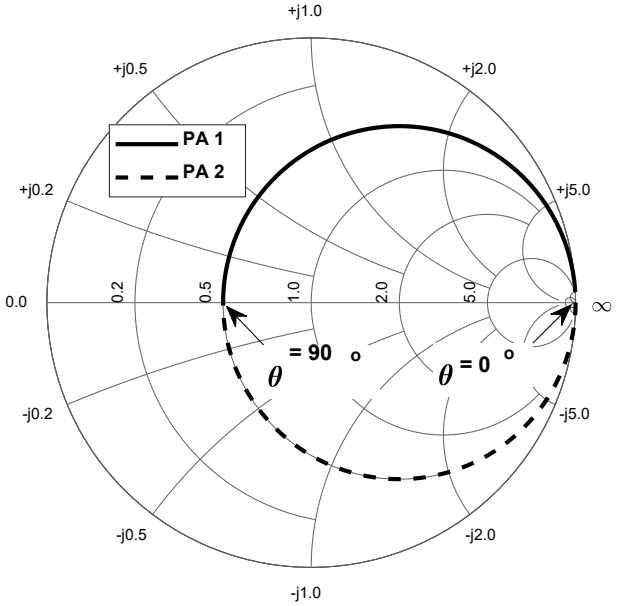


Figure 3.4 - Load impedance presented to each branch PA as the outphasing angle θ varies from 0° to 90°.

Analysis of the circuit using admitances rather than impedances gives equation 3.9, as shown in Figure 3.5, and provides a corresponding conductance G and suceptance B, which are then plotted in Figure 3.6.

$$\boldsymbol{Y_{1,2}} = \frac{2\sin\theta^2 + j\sin 2\theta}{R} = G_{1,2} \pm jB_{1,2} \tag{3.9}$$

$$\boldsymbol{Y_1} = G_{1,2} + jB_{1,2} = \boldsymbol{Y_2^*} \tag{3.10}$$

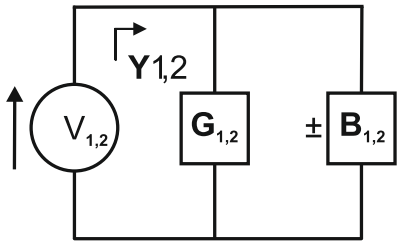
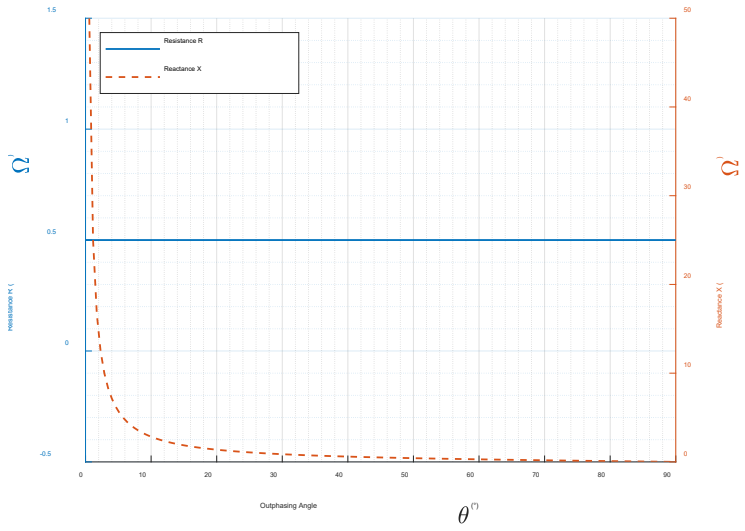
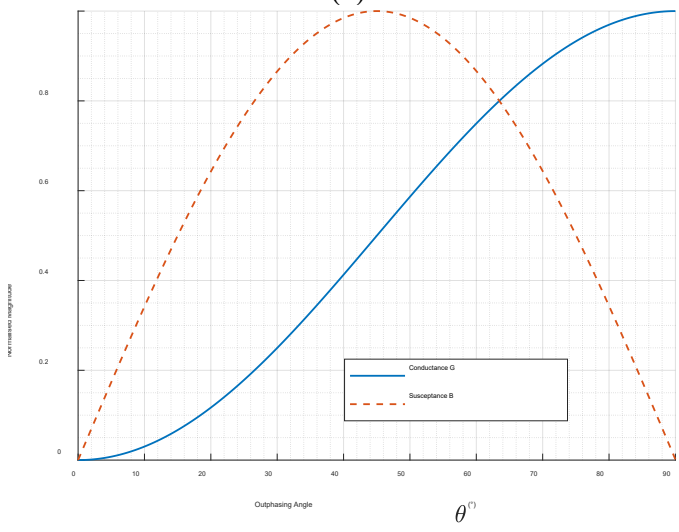


Figure 3.5 - Y equivalent circuit.



(a)



(b)

Figure 3.6 - Output impedance (a) and admittance (b) as a function of outphasing angle θ.

3.3.1 Outphasing with compensation elements

In his concept of outphasing, Chireix proposed an inclusion of additional shunt reactive components, often refered to as compensation elements.

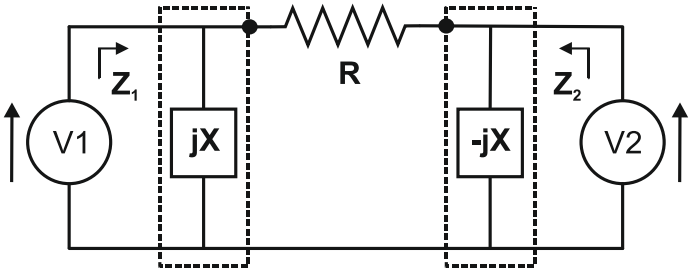


Figure 3.7 – The concept of compensation elements.

The role of these elements is to “resonate-out” the unwanted reactive part of the load impedance, at a specific phase angle θ_{COMP}. Eliminating the reactive part of load impedance at this angle ensures that the PA is operating at its peak efficiency, and this effect was shown in Figure 3.10, where the second peak in the efficiency can be observed. These components have a suceptance, B_{COMP}, described as:

$$B_{\mathrm{COMP}} = \frac{\sin(2\,\theta_{\mathrm{COMP}})}{R} \tag{3.11}$$

$$\boldsymbol{Y_{1,2}} = G_{1,2} \pm jB_{1,2} \mp jB_{\mathrm{COMP}} \tag{3.12}$$

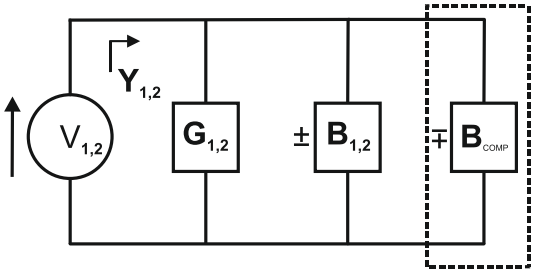


Figure 3.8 - Equivalent circuit describing an outphasing PA with the reactive compensation elements enclosed by a dashed line.

The load impedance trajectories presented to each of the branch PAs, for compensation phase θ_{COMP} = 15°,20° and 45° are plotted on Smith chart in Figure

3.9. The DE corresponding to each of aforementioned θ_{COMP} is plotted in Figure 3.10 as function of the outphasing angle. Finally, in Figure 3.11, the same DE is plotted as function of the output power back-off.

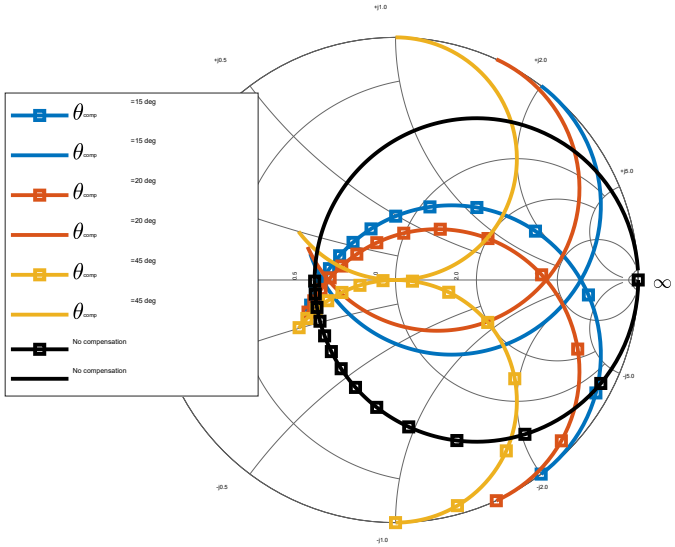


Figure 3.9 - Variation of the load impedance presented to each PA as a function of phase offset between input signals.

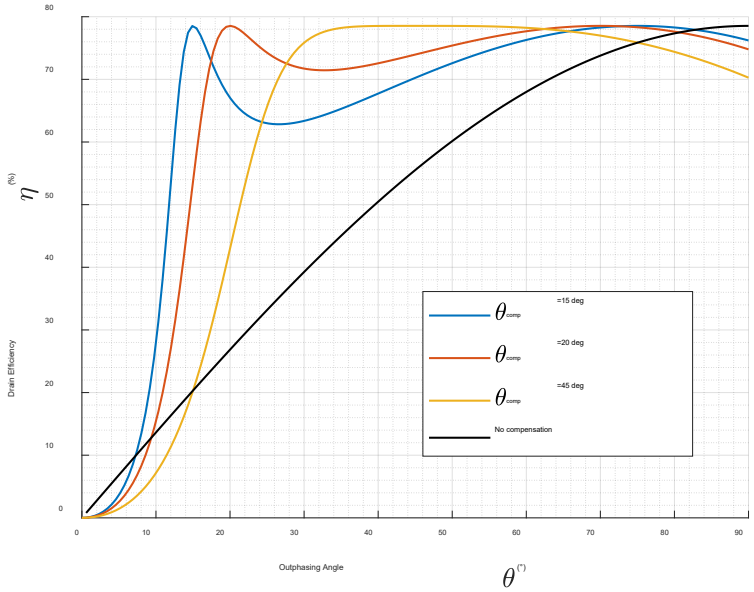


Figure 3.10 - Drain efficiency as a function of outphasing angle θ plotted for for θ_{COMP} = 15°, 20° and 45°. Efficiency of circuit without compensation elements shown by solid black line for comparison.

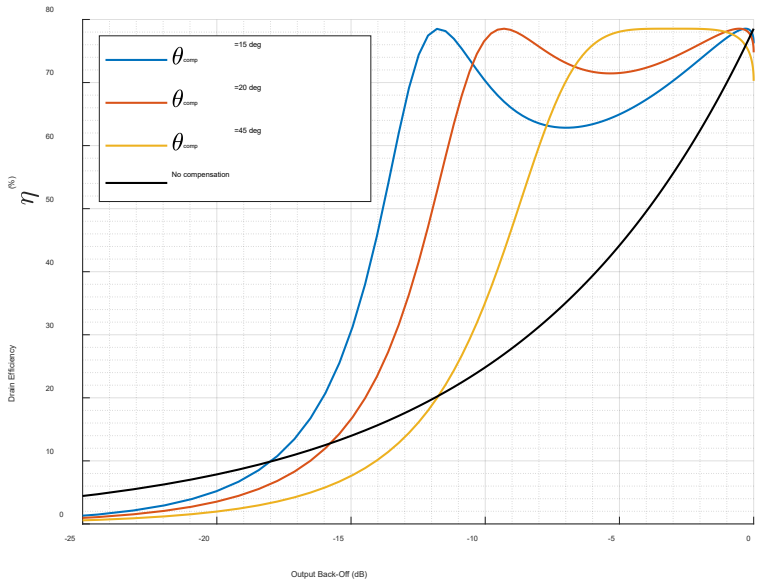


Figure 3.11 - Drain efficiency as a function of output power back-off for θ_{COMP} = 15°, 20°and 45°. Efficiency of circuit without compensation elements shown by solid black line for comparison.

3.4 Implementation of Chireix Outphasing in Modern PA Design

The theory of outphasing presented in the previous sections, assumes a load connected differentially across output of each PA. This is both impractical and difficult to implement at microwave and higher frequencies. Baluns are structures widely used in push-pull PAs and were described in Chapter 2. These structures can transform single-ended loads to differential equivalents when power combining. Therefore, a power combiner realised using a balun seems a natural choice to address the problem of realising a floating load in outphasing circuits. However, at the time this research commenced, there were very few examples of such circuits described in the literature, despite the subject of Chireix outphasing being very well researched. Another, method of addressing the floating load problem, and perhaps more common in the literature, is inclusion of the quarter wave transformers as shown in Figure 3.12a. The idea originates from the paper published by Raab in 80s'[6], which reviews and modifies outphasing theory for PAs using semiconductor active devices. The proposed quarter wave transmission line acts as impedance inverter, transforming previously assumed output voltage source into a current source, which then can be combined into single-ended load.

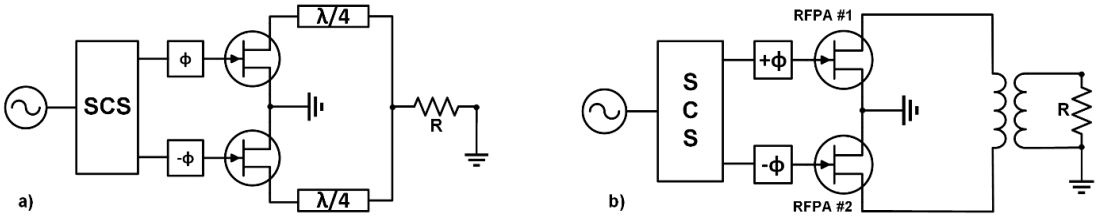


Figure 3.12 - Outphasing PA where combiner was realised using with a) λ/4 TL and b) balun.

3.4.1 Literature review

Given the vast number of papers published in the subject of Chireix outphasing and available literature, this section focuses on the most recent advancements in this area. Consideration is given for the state-of-the-art solutions,

as well as to the research that can be directly compared to the work presented in Chapter 4 and Chapter 5. The more comprehensive cross-section of the research has been a theme featured several times in IEEE magazines, such publications can be found here in [10] and [11].

Resonator elements typical for switched mode PAs, make this class particularly attractive for outphasing. In fact a great deal of research in this subject, employs class E mode of operation, where the Chireix compensation network is exploited as a part of resonating circuitry. Some examples are provided in [10], [11]. In the former, the combiner was deployed using a planar balun with an LC network realised on the single-ended part of the balun.

The interesting work was described in [12], and extended in [13] where authors employ a balun as a power combiner for two GaN HEMTs operating in class E mode. The reported bandwidth of 350 MHz was centred around 1925 MHz. It is one of very few documented implementations of outphasing using GaN HEMTs and aiming at IC level integration. Moreover, that work includes a balun as a power combiner, however it is deployed outside the IC, as expected due to its size closely related to λ/4. These two merits are important for comparing the CMOP circuit that does not require such combining structure, that work was described in Chapter 5. Authors quoted area as 18 mm x 14 mm excluding the combiner and compensation elements, as those were implemented off-chip and required further 11 mm x 2.6 mm. Both publications do not provide details regarding the balun or its performance, however, broadband operation is stated. Only drain efficiency is quoted in both papers, in fact PAE figures are rarely reported in the literature for the reasons that was discussed in later in this section. Successful integration of an integrated outphasing PAs, utilizing class D branch PAs, fabricated using CMOS technology, were reported in [14]–[17], however this technology does not provide the power levels offered by active devices fabricated in GaN technology. Transmission Lines whose

size is λ/4 are the most typical implementation of the combiner in the literature of outphasing, such as in [18]. However, at sub-6 GHz frequencies the dimensions of the combiner can dominate the final size of a circuit. For this reason, the power combiner is often deployed off-chip as seen in previously quoted work. The impact of the inherently narrowband nature of the quarter-wave transformers, on the bandwidth in outphasing PA was the subject of study in [19], where authors conclude and pinpoint influence of parasitic elements in a packaged GaN to detrimental effects on the bandwidth. Reported PA, based on packaged GaN HEMT, operates of over a 600 MHz BW centred at 3.4 GHz, achieves 50% and 41% DE and PAE, respectively, whilst operating at 7 dB OBO. The TL combiner implementation was further refined in [20] and [21] where authors cascade the outphasing PAs in in a binary manner, which allows to significantly reduce the reactive loading of the combiner when compared to the typical dual branch implementation. The *multi-way* combining concept was demonstrated using the system with branch PA operating in class F^{-1}, at 2.15 GHz. The peak CW drain efficiency was reported as 68.9% whilst delivering 42 dBm. Conversely, the same concept was applied in work presented in [22] where the reversed, *multi-way* combiner was used as SCS.

Work presented in [23] was dedicated to through overview and analysis of the branch PAs operating in modes where the harmonic termination is crucial. Several PA classes are described, most notably, class B-J, class F and F^{-1}. The theoretical derivation of the trajectories for is supported by circuit based on two PAs configured in a class B-J and operating at 900 MHz. Authors report PAE of over 60% for 7 dB OBO, however the performance is achieved at that frequency only and it is shown to deteriorate rapidly over the measured frequency range of 800 MHz to 940 MHz.

3.4.2 Inclusion of amplitude control in the Outphasing PA

When amplifying signals commonly employed in modern telecommunication systems, such as those used in Orthogonal Frequency Division Multiplexing (OFDM), any achieved Power Added Efficiency (PAE) improvements start to be eroded when the peak-to-average ratio (PAPR) starts to increase significantly, for example, exceeding 10 dB, and is therefore close to the typical gain of an active device. The need to back-off the input signal, in order to avoid compromising gain and hence preserve PAE, was acknowledged and implemented in a number of previous works dedicated to outphasing [8], [24]–[26]. The term “Mixed-Mode” outphasing is often used to describe the technique where signals driving an outphasing structure are constructed using both amplitude and phase control. The Mixed-Mode approach is presented in [27], with only a short explanation provided to describe the theory driving the design process. Authors of [26] determine experimentally the phase threshold where outphasing is no longer utilized and their PA operate in class B. The input control strategy is explained more thoroughly in [28], where authors also analyze outphasing circuit using current sources. The final circuit that was presented, however, still required a power combiner and authors did not claim any improvements over typical outphasing circuits described in literature, nor provided sufficient details for comparison. Another, and slightly different, approach to control output voltage in outphasing amplifiers was shown in [29], [30], where authors use a discrete modulation of drain voltage supply in a similar fashion to how it is done in envelope tracking systems. The work described in Chapter 5 proposes and discuses in detail the input driving strategy, which manipulates both phase and amplitude of the input signals, allowing measured PAE to remain very close to DE figures.

3.4.3 Chireix – Doherty PA topologies

Several publications were dedicated to PA topologies falling somewhere between Doherty and Chireix implementations. Given the similarities between these two techniques, authors in [31] propose a solution where two PAs operate in a classical Doherty configuration for low power output and as Chireix outphasing for higher output power. The described PA reaches 52.4 dB peak output power at 2.17 GHz and achieves average efficiency of 50% when operating with 3.84 MHz W-CDMA signals exhibiting 6.6 dB PAPR. Another example of PA operating in Chireix-Doherty space was presented in [32]. Authors reported a significant bandwidth of 1.1 GHz to 3.7 GHz achieved by their PA, which reaches 44 dBm peak output power and achieves 45% efficiency at 6 dB OBO. In both cases described above, the PA topology involves a series transmission lines used as power combiner. For Doherty operation the lines have 0º and 90º electrical length. Similarly, for Chireix operation, these lines have 90º electrical length. In both publications, authors show that the electrical length of the transmission lines can be further optimized leading to the Doherty-Chireix topology. The idea was further expanded in [33] as a general approach to dual-input PA. Comprehensive analysis of the combining structure parameters was demonstrated by PA operating at 2 GHz with 20 MHz LTE signals exhibiting 9.5 dB PAPR. Authors report an average drain efficiency of 60% a peak output power of 43 dBm.

All publications referenced in this section exploited the dual-input nature of Doherty and Chireix topologies. The ability to construct signals with an arbitrary relative phase offset, allows for a fine tuning of the signals driving each of the branch PAs which goes beyond the textbook definitions, thus falling into Doherty-Chireix framework.

3.4.4 Performance comparison of the most relevant outphasing PAs reported in the literature

Ref.	Tech.	Freq (GHz)	Peak Output Power (dBm)	BW (MHz)	PAPR / OBO (dB)	DCRF (%) peak/obo	PAE (%) peak/obo	notes
[34]	GaN	1.9	36	10	10	-/42	-/-	Avg. efficiency
[35]	GaN	3.5	42	20	6.5	-/22.7	-/-	
[13]	GaN	2.3	48.5	350	8	70/50	69/49	Extr. from plots
[32]	GaN	2.4	44	2600	6	-/50	-/45	
[33]	GaN	2	43	-	9	-/61	-/-	CW
[33]	GaN	2	43	20	9.6	-/60	-/-	Doherty-Chireix
[31]	LDMOS	2.17	52.4	3.84	6.6	-/50		Doherty-Chireix
[20]	GaN	2.14	42 avg.	-	3.47	68.9/57	-/-	four-way combiner
[36]	GaN	10.1	34.3	-	-	-	70/-	with supply modulation
[37]	GaN	9.7	37	10	11.3	-/25.6	-/15.6	PA DCRF / Total System efficiency
[19]	GaN	3.4	42.9	600	7	51/24	42/21	CW only
[38]	CMOS 45 nm	29	22.7	-	6	42.6/30	41.3/29.6	Current Mode Chireix
[39]	GaN	2.14	50	<5	6.5	77/61	-/-	four-stage Doherty

3.5 Conclusions

In summary, the Chireix, or outphasing PA technique has had an interesting history. Having been proposed and implemented in the early era of commercial radio broadcasting, it fell into disuse for several decades. The explosive growth of mobile communications in the 1990s triggered an extensive and worldwide effort to improve the efficiency performance of PAs excited by signals having advanced digital zero-crossing modulation scheme. Despite a wide variety of recent literature on the subject, certain issues remain either lightly, or under-researched. These issues formed the starting point of this work and were outlined in Chapter 1.

3.6 References

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CHAPTER 4

DESIGN AND IMPLEMENTATION OF AN OUTPHASING RF POWER AMPLIFIER WITH BALUN COMBINER

This chapter describes two RFPA circuits designed and built to investigate and demonstrate an application of baluns in outphasing amplifiers. Two circuits were made using different technologies: the first used packaged devices, in particular Cree CGH40010F discrete GaN HEMTs, and a balun which was implemented using a coaxial cable, mounted over a slot in the ground plane. Whereas, in the second RFPA, a planar balun implemented on alumina substrate was employed in a “chip & wire”, hybrid fabrication technology. This design was based on GaN HEMT die devices from Qorvo, the TGF2023-01-1. Each subsection in this chapter is organized that the preliminary design, simulations, and measurements of the relevant balun are followed by simulation and implementation of the RFPA. Measurements and brief discussion is provided at the end of each subsection.

4.1 Demonstrator 1: Cree CGH40010F 10W

The following section describes the design process and characterization of an outphasing circuit, based on a commercially available packaged GaN HEMT device from Cree. Two of these devices were paired with a balun, implemented using a section of a suspended co-axial semirigid cable. The circuit described in this section was used to demonstrate suitability of a broadband balun as a power combiner structure in an outphasing architecture. The bandwidth and the impact of parasitic elements of an active device on the performance of an outphasing amplifier were investigated.

The balun designed for this work operates over an extended octave bandwidth, which allows load modulation to be prescribed at fundamental and second harmonic frequencies, allowing continuous modes such as Class J to be implemented. The desired harmonic load termination is achieved without any specialized matching networks, and solely by means of load modulation provided by the active device interaction. In this work, we show that the efficiency characterized by class J-like waveforms can be achieved solely by means of load modulation (without the need of matching networks) that provides appropriate termination to harmonic impedances, hence significantly reducing the complexity of the design and offering potentially broader bandwidth operation.

This design exploits an alternative way of realising the load compensation network, which has the advantage of not requiring additional discrete components to provide the susceptance described in Chapter 3. Instead, the same effect is achieved using simple transmission lines, here named offset transmission lines (OTLs), placed in series with the output of each PA. A similar principle was introduced in [1] and analysed in [2] as the solution to negating the effects of output parasitic elements of the active device and matching elements in Doherty power amplifiers.

However, in this work, the OTLs not only account for the unwanted effects of the device parasitic elements, but are also adjusted to provide the required Chireix compensation effect for high back-off efficiency. Work utilising a similar concept was presented in [3], but the concept was limited to system level analysis, at the combiner reference plane. The important difference in this work is the focus on the effects of OTLs on the intrinsic level behaviour of the active device, together with an explanation of the mode of operation, which to our knowledge has not been previously shown or demonstrated in Chireix outphasing PAs.

4.1.1 Balun design and characterization

The balun required for this work was implemented using a 26 mm long section of suspended RG405 semi-rigid coaxial cable. The passive structure was characterized in a dedicated fixture and the measured data obtained was subsequently employed in simulations of the outphasing system, presented later in this section.

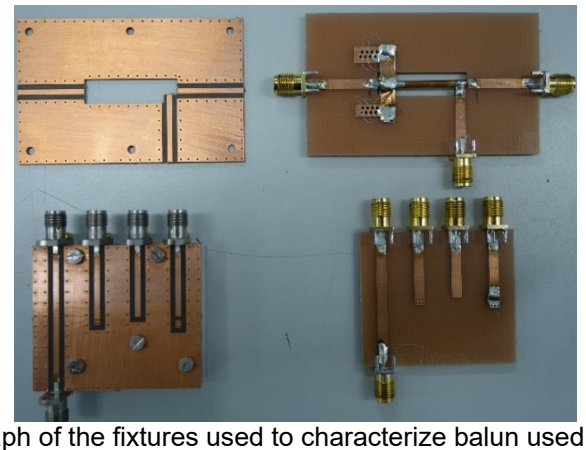

Figure 4.1 - Photograph of the fixtures used to characterize balun used in this work.

Measurements revealed that the structure's single-ended reference impedance Z0 = 50 Ω, was transformed to 24.9 Ω and 19.7 Ω at each of the balanced terminals for f = 2.0 GHz, and 34.5 Ω and 26.7 Ω for f = 4 GHz. Previous research, discussed in Chapter 2 shows that one of the major factors limiting the bandwidth of a balun realized using coaxial cable is attributed to the coupling between the outer

conductor (shield) of the cable and global ground. In the work presented here, the balun was sus-pended 6 mm above a deep slot to limit this coupling effect and to ensure that losses at the second harmonic are sufficiently low for load modulation at that frequency, which is confirmed by the plot shown in Figure 4.2.

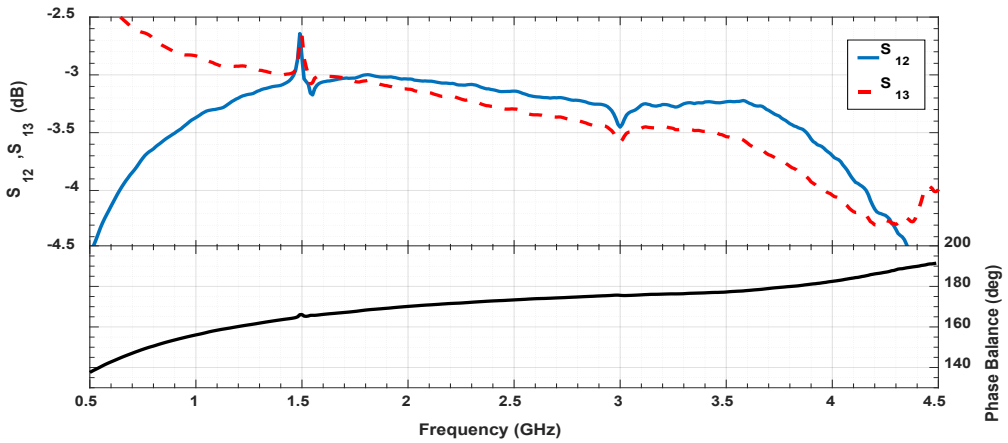

Figure 4.2 - Measured S parameters of the coaxial Balun terminated to 50Ω on the single ended side and 25Ω on the balanced side. Transmission coefficients (top) and phase balance between differential terminals (bottom).

4.1.2 Design strategy and implementation

Initially, the design strategy for this demonstrator assumed that a discrete SMT components would be used for realization of the load compensation network. Using two inductors L_1 and L_2 as shown in Figure 4.3, the parasitic output capacitance C_{DS} could be incorporated into the design of load compensation network, where this capacitance would be partially or fully absorbed by the aforementioned inductors in the manner shown in Figure 4.4.

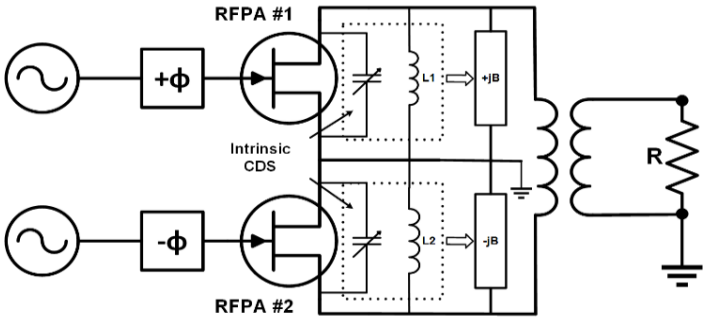

Figure 4.3 - Concept of incorporating the parasitic capacitance CDS into the design of load compensation network realized using inductors L1 and L2.

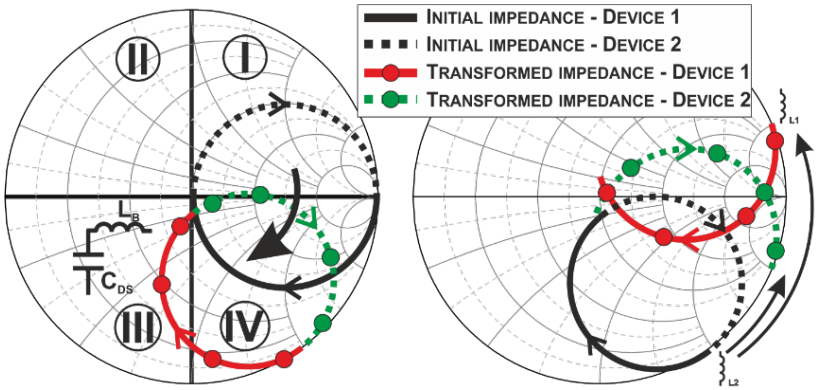

Figure 4.4 - Effects of parasitic elements associated with the active device and its package, on intrinsic load impedance trajectories (left). Effects of inductors L_1 and L_2 from Figure 4.3 (right).

This strategy however proved impossible to be implemented, because the modulated load impedance, initially dominated by parasitic elements of the active device as shown using black traces on Smith chart in Figure 4.4, undergoes further shift introduced by the output bias network and package of the active device. This shift in a real implementation cannot have zero physical length. Assuming, that the DC bias networks are optimised to have a negligible effect on the RF signal, the dominating effect comes from transmission lines formed by mounting pads and traces that comprise the essential part of the output DC bias block. The effects of phase shift provided by the output bias network would move the outphasing impedance trajectories further towards quadrants IV and III on the Smith Chart, as confirmed by simulations and shown in Figure 4.5. At that stage of the design process, achieving the shunt reactance required for the load compensation, without introducing

additional transmission lines, would prove either impractical or impossible, depending on the frequency, and components' size and the technology used for circuit fabrication. The additional transmission line would require an electrical length that, when combined with the existing phase shift, would need to be a multiple of 180° to align the phase to the intrinsic plane. In other words, the Γ_1 reference plane needs to be rotated, using the OTLs to match the Γ_1' reference plane, similarly to what is done in Doherty PAs with offset lines [2].

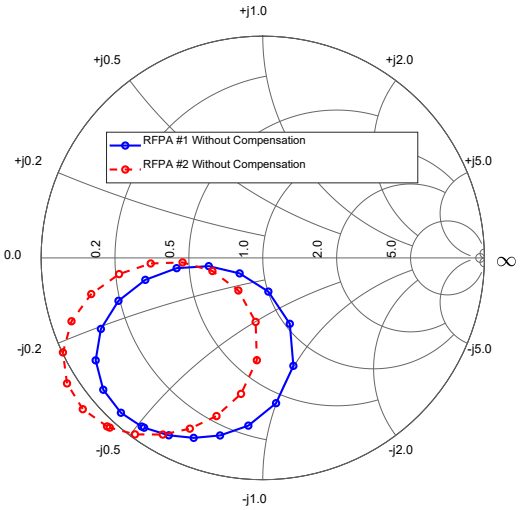

Figure 4.5 – Simulated effects of DC bias and device output parasitic elements on the load impedance trajectories at the intrinsic plane.

It was shown in Chapter 3 that the impedance presented to each device, denoted as Z_1 and Z_2 on Figure 4.6, in an outphasing system without a load compensation, is a function of the load resistance R and phase offset φ between two input signals:

$$Z_1(R,\varphi) = \frac{R}{2}(1 - j\cot\varphi) = Z_2^*(R,\varphi) \tag{4.1}$$

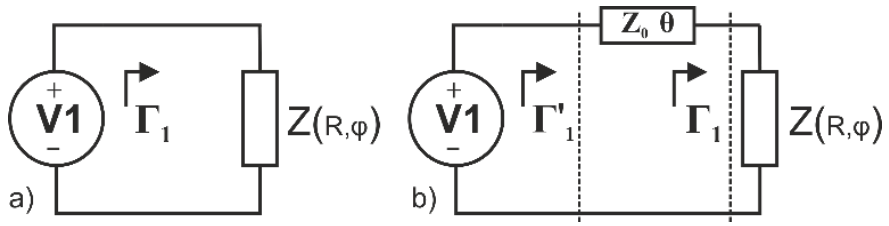

Figure 4.6 - Impedance transformation using a transmission line.

This load modulated impedance can be represented generally as Z(R, φ). If this load is connected to a voltage source, as shown in Figure 4.6, the expected outphasing load modulation will be observed. If, however, a transmission line of impedance Z_0 and length θ is placed between Z(R, φ) and the voltage source, then the voltage source will be presented with a transformed load impedance, that is easily defined in terms of reflection coefficient normalized to Z_0:

$$\Gamma'_1 = \Gamma_1 {}^{-2j\theta} \tag{4.2}$$

The transformation in (4.2) represents a phase change in the complex number and is a rotation of constant radius [4]. Therefore, the point represented by Γ_1' in Figure 4.6 can be found by a rotating Γ_1 around a circle with a constant-radius, defined by the value of Z0 of the transmission line. In this work this parameter was chosen to be *R*/2 to match a real part of (4.1). This is true in general, and also applies if we place two transmission lines, one at the output of each device between the load resistor and each voltage generator in the outphasing circuit shown for example in Figure 4.7.

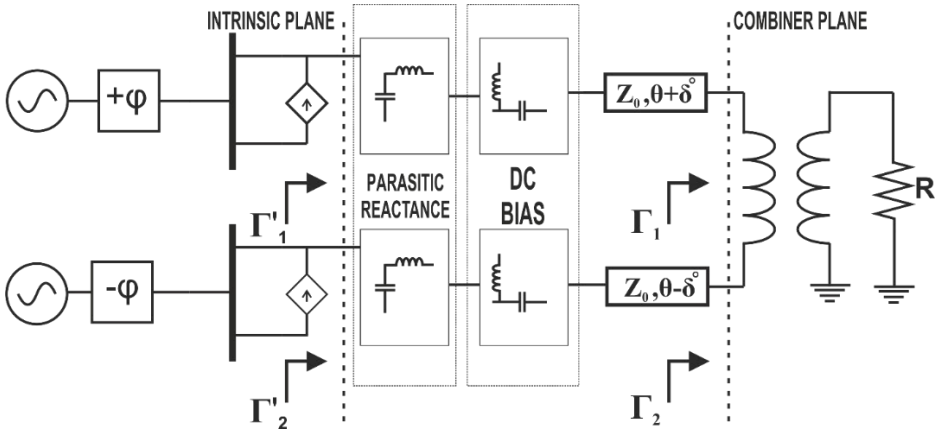

Figure 4.7 - Outphasing system with load compensation network realized using Offset Transmission Lines.

However, this analysis is limited because the voltage sources can supply any current demanded by the load. The modulated load impedance described by (4.1) would now also depend on the length of the transmission lines, and would not be related to Z(R, φ) as defined in (4.2), i.e. it would be represented by trajectories completely different from those of a classical outphasing circuit. Conversely, a real active device, although approximated as a voltage source in classical outphasing analysis, can only supply finite current. This boundary on the maximum current makes the result of the analysis that assumes the rotation on constant radius circles reasonably accurate independently of the length of OTL. This can be observed from the simulated impedance trajectories, which are a result of load modulation acting on the output of each active device, shown in Figure 4.8 for OTLs with various electrical lengths θ. The foundry large signal model of the device is used for these simulations.

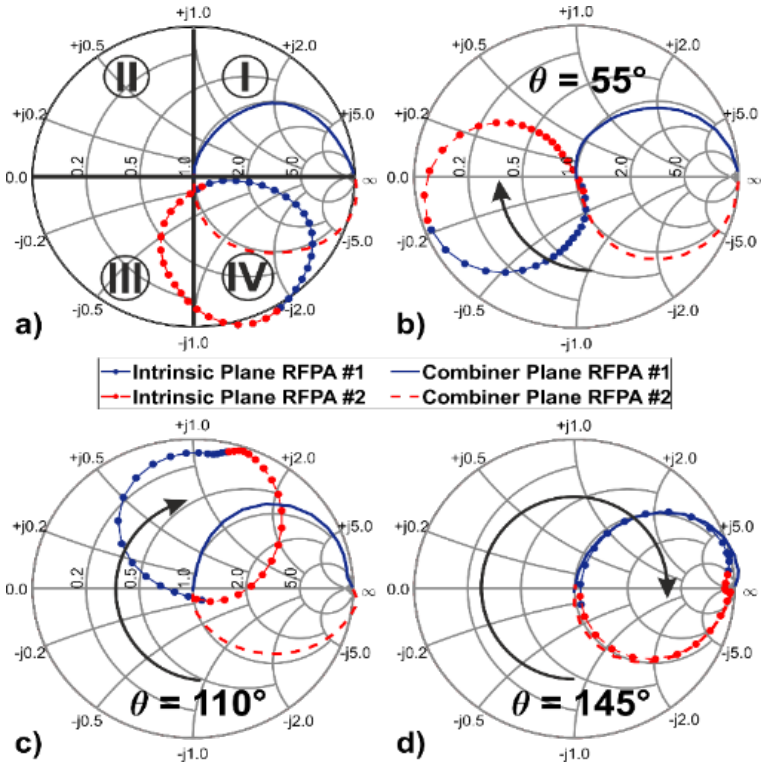

Figure 4.8 - Simulated effects of the offset transmission lines, with electrical length θ, on load modulation at intrinsic generator and combiner planes: a) $\theta = 0^{\circ}$ b) $\theta = 55^{\circ}$ c) $\theta = 110^{\circ}$ d) $\theta = 145^{\circ}$

The desired transformation from (4.2) is achieved at the intrinsic plane of each device, while the impedance at the combiner plane remains almost unaffected by the presence of the OTLs. Furthermore, it is shown that the load modulation at intrinsic plane is preserved while that reference plane is rotated using OTLs, thus (4.2) can be applied to load modulation function from (4.1). For the specific case analysed in Figure 4.8, the value $\theta = 145^{\circ}$ provides the compensation required similarly to when using classical compensation susceptance $\pm B_{comp}$.

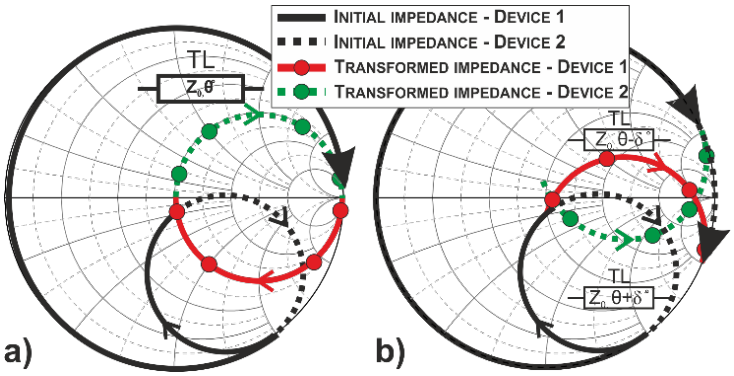

Figure 4.9 - Concept of the offset transmission lines, with: a) equal length to null the effect of output parasitics, b) with different lengths to provide the load compensation effects.

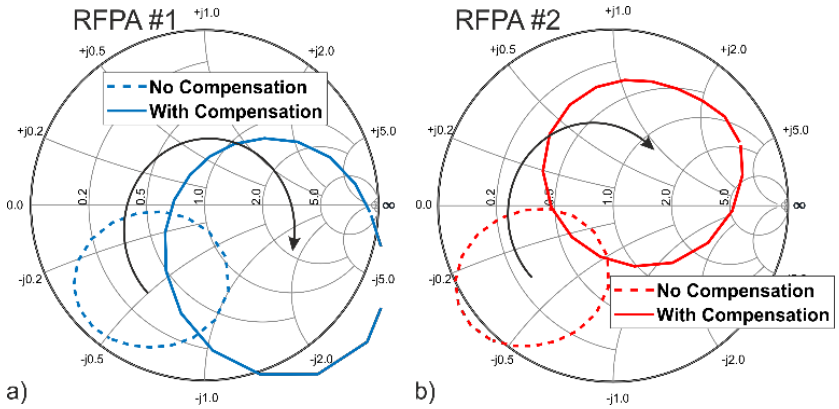

Figure 4.10 - Simulated Impedance trajectories rotated using offset transmission lines, presented at the intrinsic plane of: a) device 1 (upper branch), b) device 2 (lower branch).

In this work, the theory is advanced by proposing the use of two transmission lines with an electrical length offset δ from the initial θ value to provide a load compensation effect similar to the ideal shunt reactance method as shown in Figure 4.9 where the concept is demonstrated. Simulated effects of OTLs consisting of two transmission lines with Z0 = 25 Ω and electrical lengths of 115º (θ - δ) and 135º (θ + δ) was shown in Figure 4.10. This approach would provide load compensation effect allowing the outphasing system to reach a total drain efficiency in excess of 60% over 10 dB output power back-off.

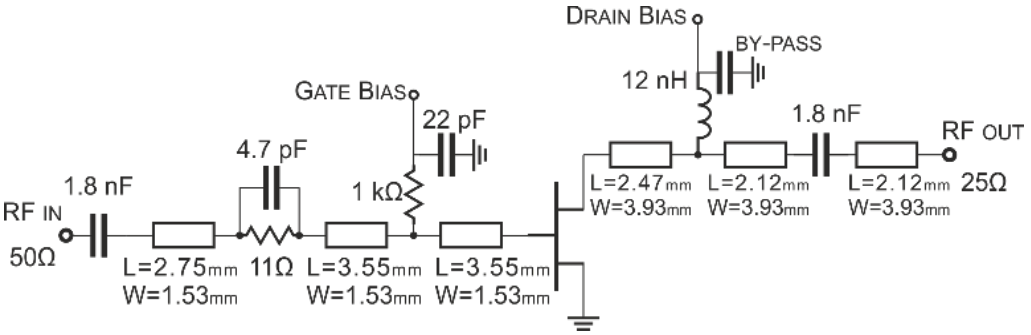

Figure 4.11 - Schematic of the individual branch PA.

In order to avoid using an output matching network (OMN), a device was required that would reach its peak efficiency and power output when presented with an impedance close to previously measured odd impedance (Z_{ODD}) of the balun.

The CGH40010F, 10 W GaN HEMT from Wolfspeed met the required specifications, since its optimum intrinsic load is around 25 Ω. Two devices operating with a 28 V DC drain supply were biased in a deep class-AB mode (I_{DQ} = 40 mA). The input matching network was omitted for the scope of this work and the device fed via a 50 Ω transmission line, while stability was attained using a parallel of capacitor and resistor of 4.7 pF and 11 Ω, respectively, in series to the gate as shown in Figure 4.11. DC bias was introduced using a 1 kΩ resistor at the gate and a 12 nH inductor at the drain stage.

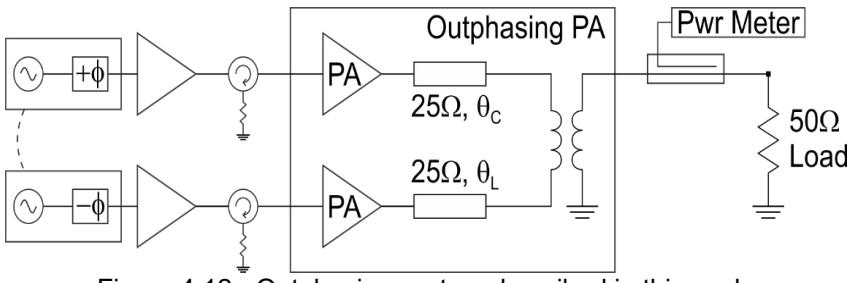

Figure 4.12 - Outphasing system described in this work.

The modulation of the load presented to each device is achieved by sweeping relative phase offset between input signals of each RFPA, as shown in Figure 4.13 in

a form of impedance trajectories. It can be noticed that the second harmonic impedance trajectories are also subject to load modulation, rotated by the insertion of the compensation network

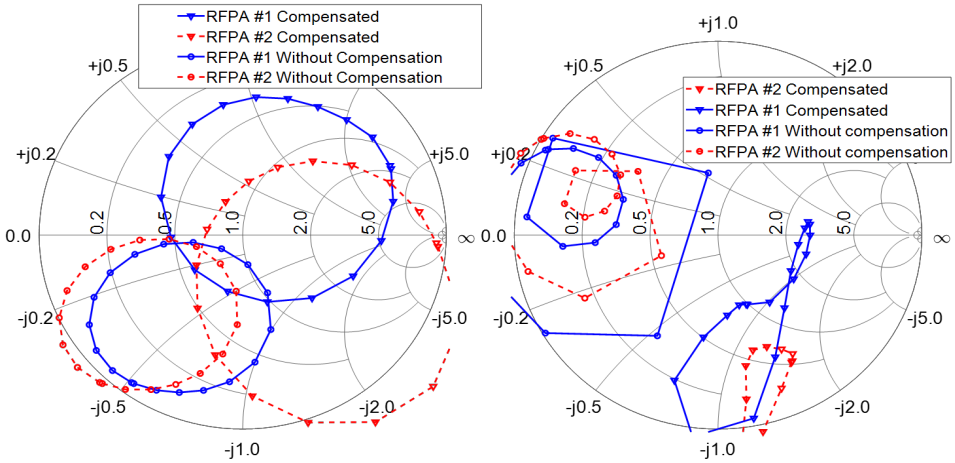

Figure 4.13 - Impedance trajectories presented to each device at its intrinsic generator plane at fundamental (left) and second harmonic (right) frequencies.

The simulated performance of the proposed system is shown in Figure 4.14. The peak power is achieved for a phase offset around 100 deg (Figure 4.14a) while efficiency of both RFPAs is above 50% up to 200 deg (Figure 4.14b), that reflects in an overall efficiency higher than 50% on 9 dB back-off range. Investigation of the output waveforms (Figure 4.14d) revealed the phase shift in current and voltage waveforms, which minimizes the overlap and hence dissipated power. The phase shift was achieved by means of natural harmonic injection by the second device, resulting in negative second harmonic impedance seen at the intrinsic generator plane, (-1.6-j58) Ω.

The circuit was built on 0.51 mm thick RT Duroid 5880 substrate (εr = 2.2, tanδ = 0.0009 at 10 GHz), photo shown in Figure 4.15.

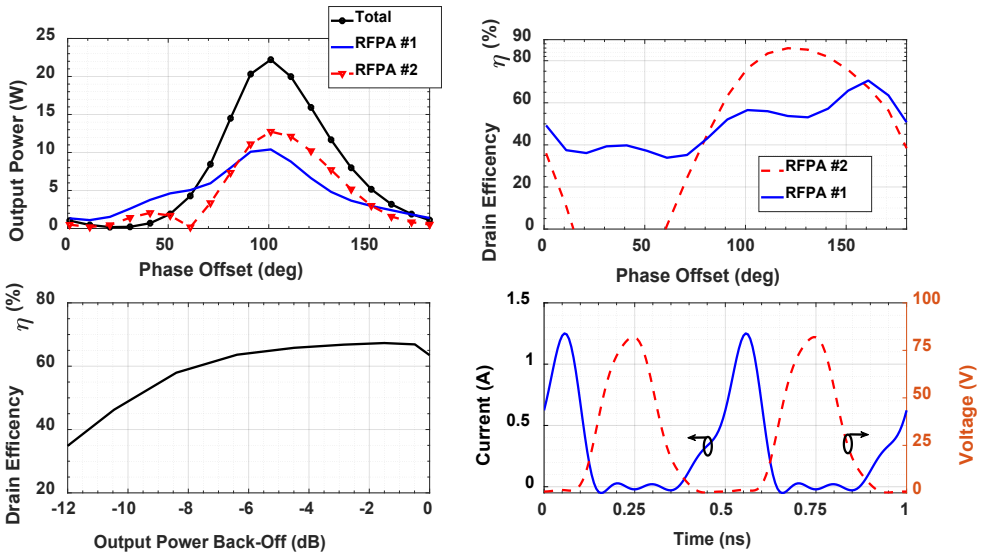

Figure 4.14 - Simulated performance of the outphasing system showing: a) output power, b) drain efficiency of individual RFPA, c) drain efficiency of the outphasing system, d) output waveforms of the more efficient device at 120° phase offset.

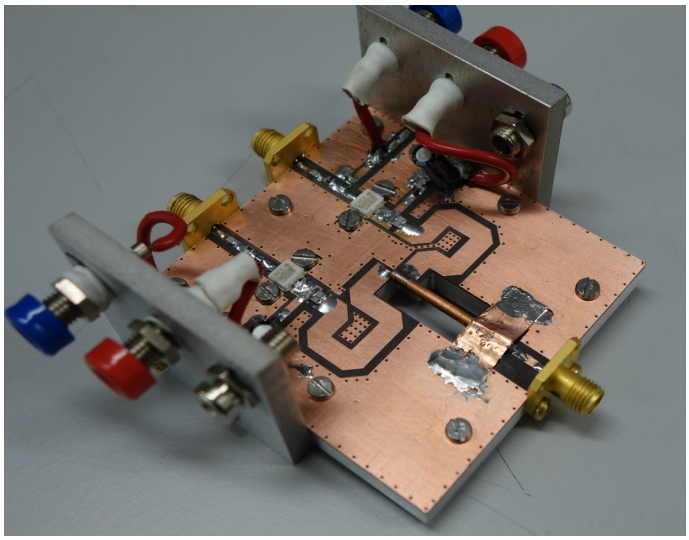

Figure 4.15 - Designed outphasing circuit (board size: 67 mm x 63 mm x 6 mm).

4.1.3 Experimental verification (Measurements)

A minor carrier frequency adjustment to 1.95 GHz was required to compensate for the shorter electrical length of the fabricated OTLs. These were revealed to have a consistent difference in actual electrical length and appeared approximately 5º shorter when compared to simulated results. The circuit was then re-simulated taking into the account the offset introduced by fabrication process.

Figure 4.16 shows the resulting good comparison between measured and re-simulated efficiency vs. output power back-off, for an available input power of 31.3 dBm, when sweeping the phase between the two inputs. The efficiency stays above 65% and 50% over a 6 dB and 9 dB output power range, respectively. The achieved maximum output power is 44.8 dBm, and very good agreement is achieved between simulations vs. measurements, as shown in Figure 4.17.

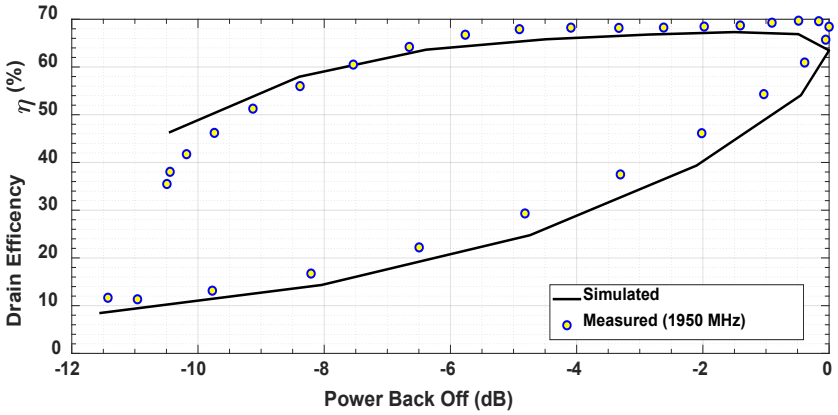

Figure 4.16 - Simulated and measured PBO performance of the described outphasing system.

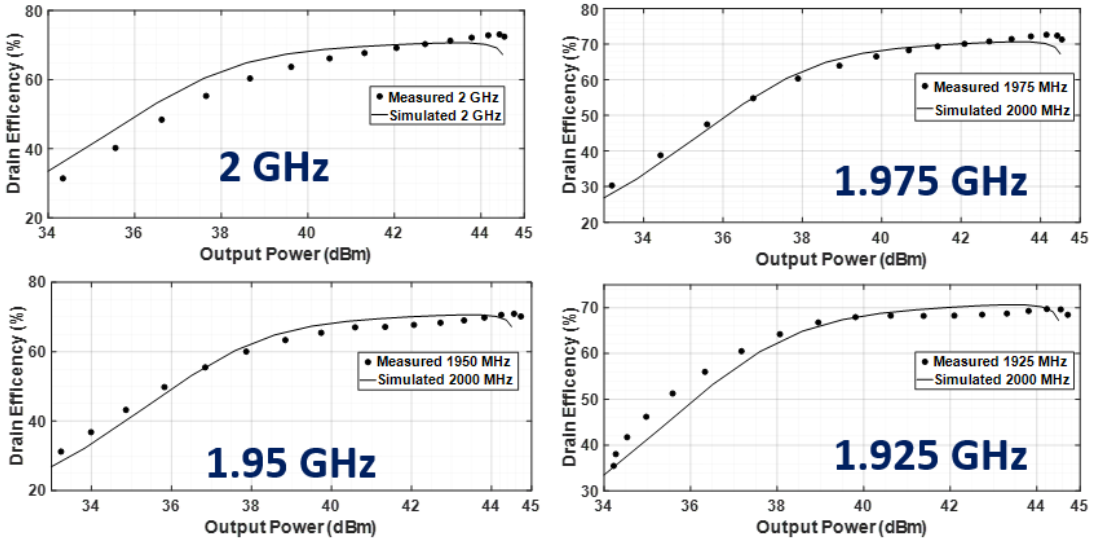

Figure 4.17 - Simulated and measured performance of the outphasing demonstrator

4.1.4 Conclusions

An alternative solution for load compensation in Chireix outphasing amplifiers has been presented and demonstrated, where the load modulated impedance trajectories presented to each device can be transformed within the unity Smith Chart region, by means of offset transmission lines. This has proven very useful in the presented case, where achieving load compensation would otherwise not be possible without introducing additional transmission lines. This paper demonstrates that with the correct choice of transmission line parameters the shunt reactive components usually associated with outphasing structures are redundant and not necessary to achieve the load compensation effect similar to the one proposed by Chireix.

4.2 Demonstrator 2: Qorvo TGF 12W

This section presents a novel approach to realizing and fabricating a planar balun structure,

This Section presents an outphasing power amplifier using a planar balun as power combiner. The balun with bandwidth extending to and over octave was fabricated using thin film technology on alumina substrate where conventional bond wires are replaced by conductor bridges supported on polyimide blocks. Three different prototype structures were fabricated on 10 mil thick alumina substrate (εr = 9.8, $\tan\delta$= 0.0001) using thin film fabrication technology. More than double-octave bandwidth is reported, from 1.25 GHz to 4.7 GHz with losses lower than 1dB, an amplitude imbalance (trace separation) below 0.75 dB and phase imbalance within ±5 degrees. Measurements show good agreement with simplified 2D EM simulations. The performance of the balun is assessed for suitability in applications where amplitude and phase balance are of critical importance, such as push-pull or outphasing amplifier topologies.

The outphasing PA design adopts a hybrid approach, utilising a pair of bare die devices with bond-wire connections to the alumina passive networks, to minimise the extra parasitic effects introduced by packaging. The characterised prototype, that uses the TGF2023-01-2 12 W GaN HEMT from Qorvo, operates at centre frequency of 1.9 GHz and demonstrates a 15% bandwidth, where the maximum output power is maintained within 0.5 dB deviation from 41.2 dBm. On the same bandwidth, the PAE is above 55% and 44% when operating at its peak and 6 dB output back-off (OBO) output power, respectively. The power back-off is realised by both amplitude and relative phase modulation.

4.2.1 Balun design and characterization

The balun used in this work was derived from a broadband structure presented in [5], where the authors extended the bandwidth and minimise a trace separation by means of maintaining a specific ratio, given by (4.3) and (4.4), between the characteristic impedance of transmission lines that form the structure as shown in Figure 4.18.

$$\frac{Z_0}{Z_{inner}} = \frac{Z_{stub}}{Z_{stub,inner}} \tag{4.3}$$

$$Z_{stub} = \frac{Z_0^2}{2Z_{outer,stub}} \tag{4.4}$$

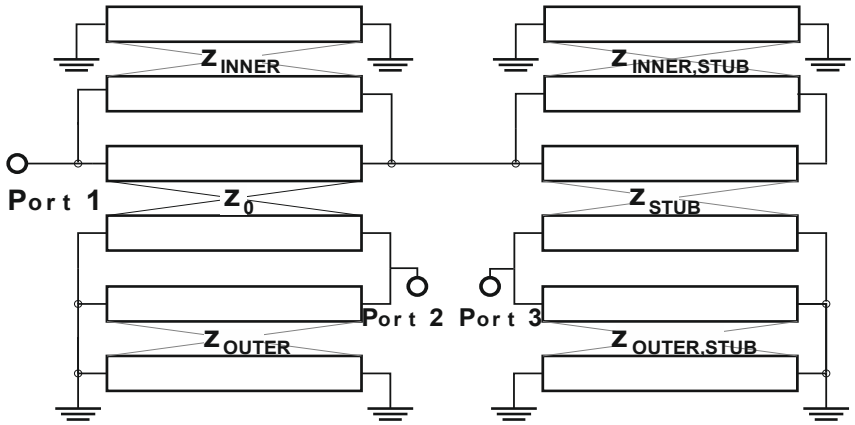

Figure 4.18 - Simplified Transmission Line based model of the proposed balun structure

Satisfying the equations in (4.3) and (4.4) leads to an improvement in performance of the balun topology that was originally proposed by Marchand [6]. The structure presented in [5] satisfied the above equations by halving the characteristic impedance of the inner conductor in the stub section. This was achieved by creating two transmission lines connected in parallel, as shown in Figure 4.19 (TLs denoted W5 and W7).

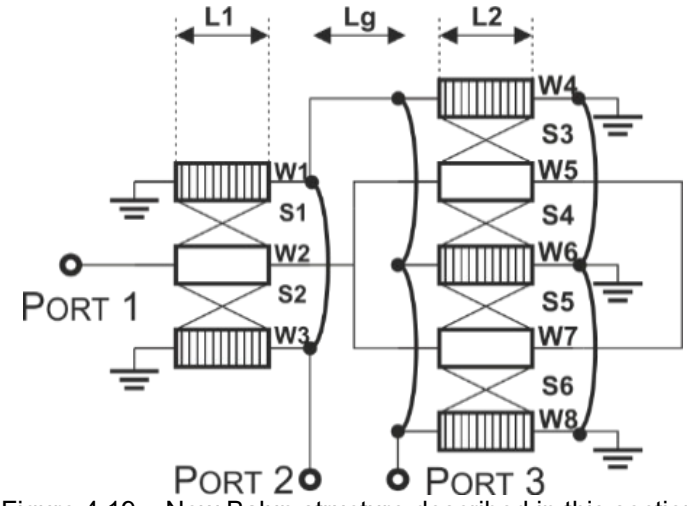

Figure 4.19 – New Balun structure described in this section.

The structure for this work was modified to work at the frequencies around 2 GHz telecommunication bands and was further refined by adopting a different manufacturing technology and eliminating the requirement for bond wires on the balun structure. The overall dimensions of the balun (with ground via-holes) are 22.25 mm x 1.16 mm. All passive circuits were fabricated using thin film technology on an alumina substrate (ε_r = 9.8, tanδ = 0.0001).

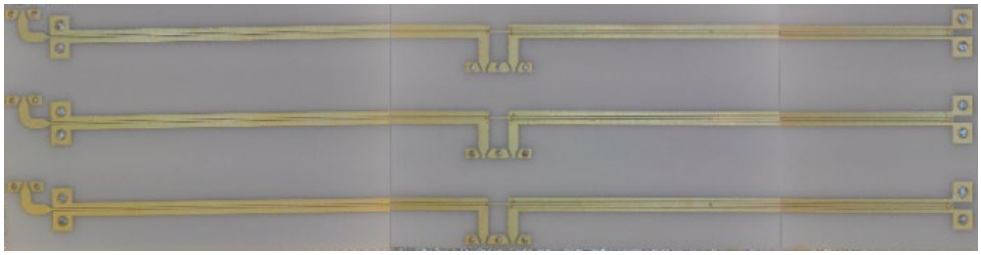
Figure 4.20 - Photograph of the fabricated balun structures.

The fabricated baluns, shown in Figure 4.20, with corresponding dimensions provided in Table 1, satisfy (4.3)and (4.4), where the bond wires used in [5] have been replaced by metal bridges suspended on polyimide support blocks. The polyimide has a permittivity of 3.3 and typical thickness between 3 to 6 μm. Example of such bridge

is shown in Figure 4.21b and compared to the solution realised using bond-wires (Figure 4.21a). The layout of the air-bridge structure benefits from less discontinuities, which were previously introduced by pads required for reliable bond wiring process. Moreover, the new structure is lower profile, more robust and less susceptible to mechanical damage.

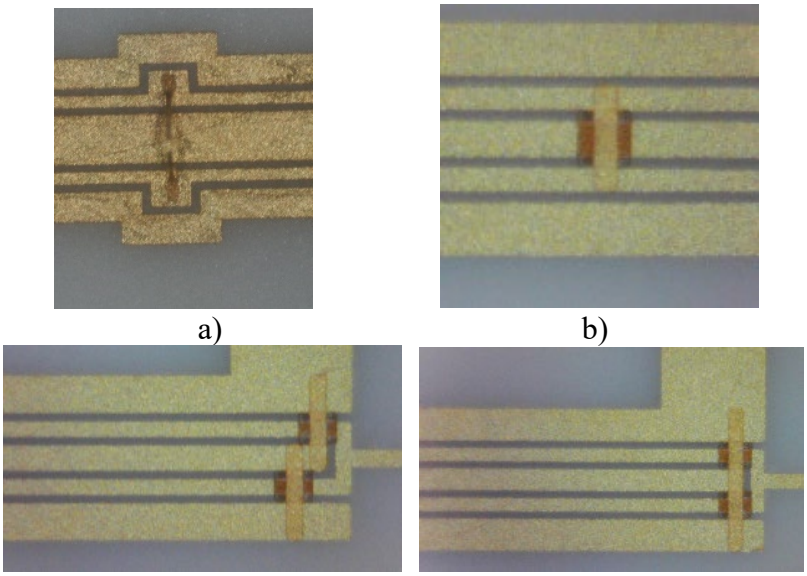

Figure 4.21 – Photograph of the brides realised using: a) bond wires, b) polyimide, c) offset polyimide, d) in-line polyimide.

Measurements were performed using a 3-port Vector Network Analyser and probe station. The calibration plane was extended to the probe tips using a vendor specific calibration kit. The effects of probe footprint and feed lines were removed by a de-embedding process, using on-board calibration standards. The S-Parameters were acquired in a three port, single-ended configuration, with port designations following the numbering shown in Figure 4.19.

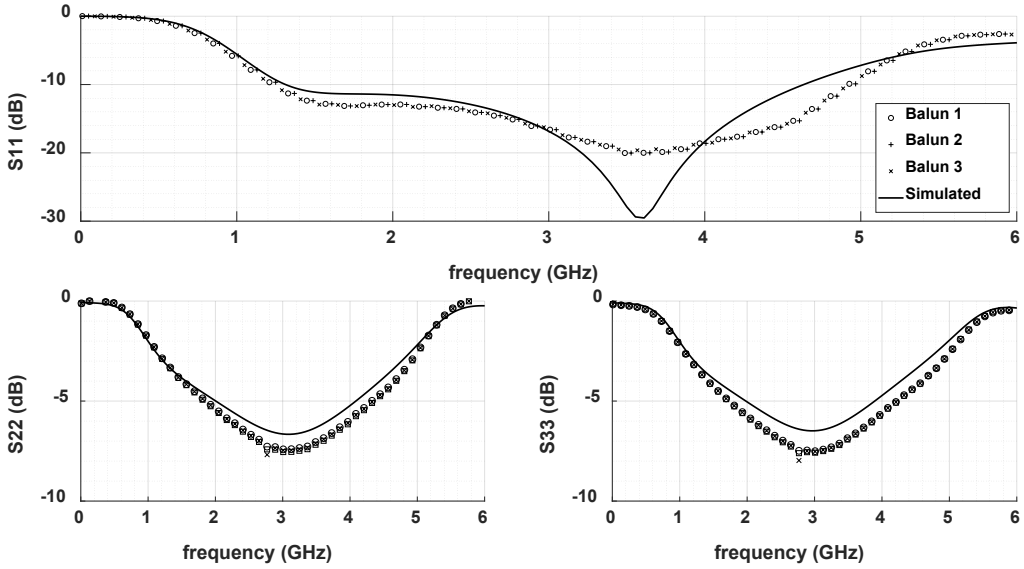

Figure 4.22 - Measured and simulated input return loss of the balun structures.

Figure 4.22 shows the simulated and measured (using 3 samples) input return loss at each port, measured with a single-ended 50 Ω termination. The measurements show very good agreement with simulations; the main difference is a deeper resonance of S_{11} at approximately 3.5 GHz observed in simulation that does not affect the practical use of the balun. The phase balance, shown Figure 4.23 (top) remains within +/-5° of 175 degrees for frequencies between 0.1 GHz to 5.9 GHz, where a strong resonance was observed. The trace separation, shown in Figure 4.23 (bottom) and derived from plots shown in Figure 4.24, was measured to be less than 1 dB for the same frequency band and is in good agreement with simulations, with maximum deviation of less than 0.25 dB. The odd impedance of the balun was measured to be 37 Ω for ports 2 and 3, while the even mode impedance for port 1 was measured to be 68 Ω. For the S-Parameter measurement environment, these values ideally should be 25 Ω and 50 Ω respectively. Therefore, further improvements in the performance of this balun structure should be possible by implementing an impedance matching network. No difference was observed in performance between the in-line and staggered bridges solutions.

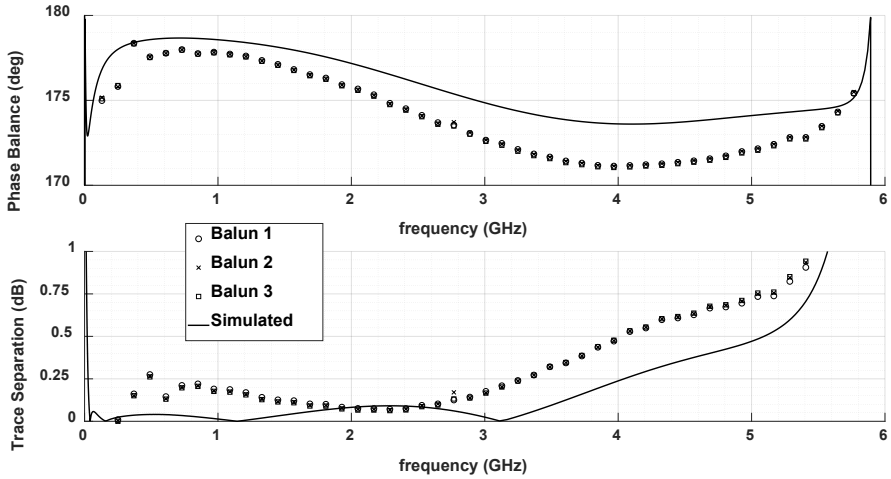

Figure 4.23 - Measured and simulated phase balance (top) and trace sepaation (bottom) of the balun structures.

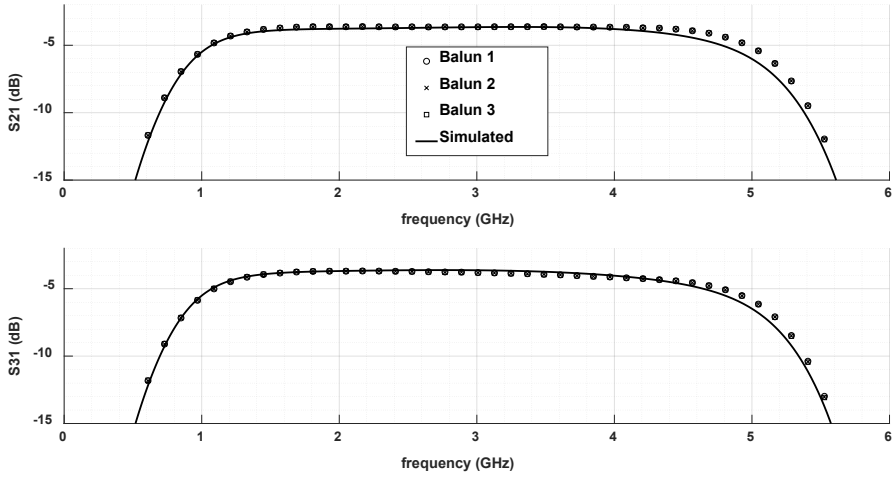

Figure 4.24 - Measured and simulated transmission parameters of the balun structures.

4.2.2 Design strategy and implementation

The circuit shown in Figure 4.25 was used to characterize the output conditions presented to each active device during outphasing operation. The measured data was compared to simulations and used in the subsequent outphasing simulations. The simulated and measured trace separation of the output structure was less than 0.07 dB and 0.15 dB respectively, over the frequency range from 1.75 GHz to 2.05 GHz and were shown in Figure 4.26. The simulated and measured phase balance were within 177º ± 0.3º and 176º ± 0.5º, respectively, for the same frequency range.

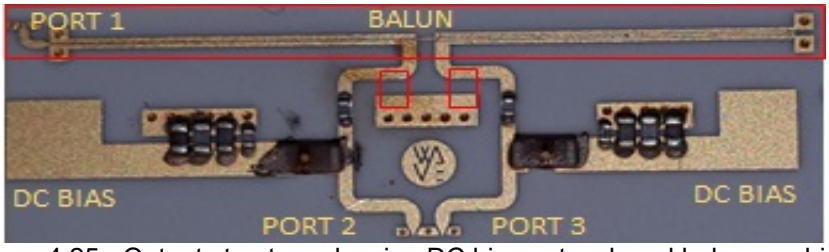

Figure 4.25 - Output structure showing DC bias network and balun combiner

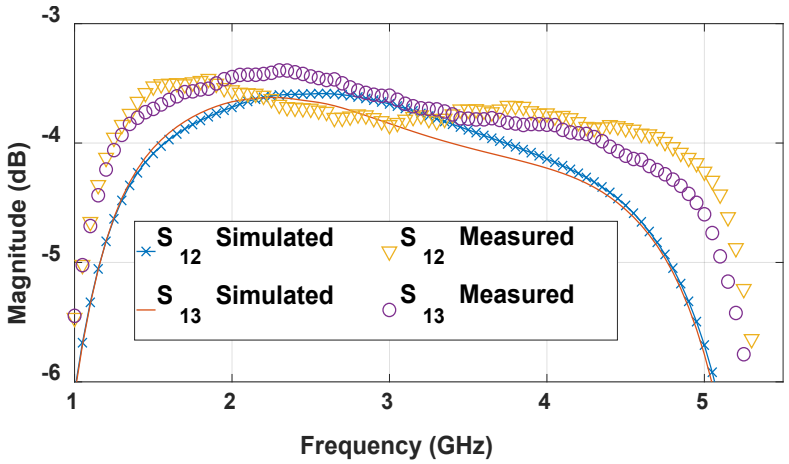

Figure 4.26 - Simulated and measured S12 and S13 parameters of the power combining structure.

The measured total insertion loss associated with single ended measurements of S12 and S13 was in range of -3.45 dB to -3.56 dB for the aforementioned frequencies. These losses would translate to approximately 0.5 dB losses in output power when the structure is used as power combiner in the outphasing PA described in this paper. The input return loss (S11), presented in Figure 4.27, shows good matching to 50 Ω for frequencies in range of 1.2 GHz to 5.15 GHz where magnitude of S11 is lower than -10 dB. For the 1.75 GHz to 2.05 GHz band, the measured S11 resulted lower than -15 dB.

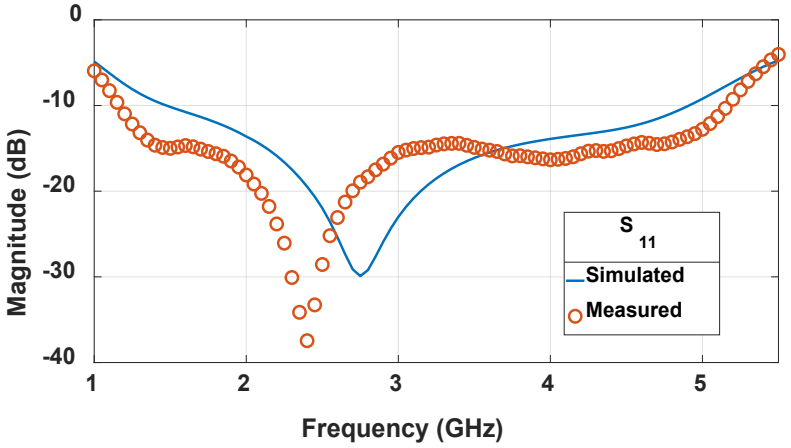

Figure 4.27 - Input Return Loss measured at the output terminal (Port 1).

This outphasing circuit was based on two TGF2023-01-2 12 W HEMT GaN bare die devices from Qorvo, operating at 28 V DC drain supply. The transistors were biased in deep class AB with I_{DQ} = 40 mA. Stability was attained using a parallel combination of R/C network with values of 10 Ω and 4 pF, respectively, as shown in Figure 4.28. Drain DC supply was introduced using a 12 nH inductor, and a 12 pF capacitor was used as DC block on the output, see Figure 4.28. No input matching was included in the design, and the devices were biased at the gates using an external bias-T. On the output terminals, both active devices are presented with impedances around 50 Ω, which is twice the optimum intrinsic load for this particular device, and should result in lower output power, but higher efficiency [7].

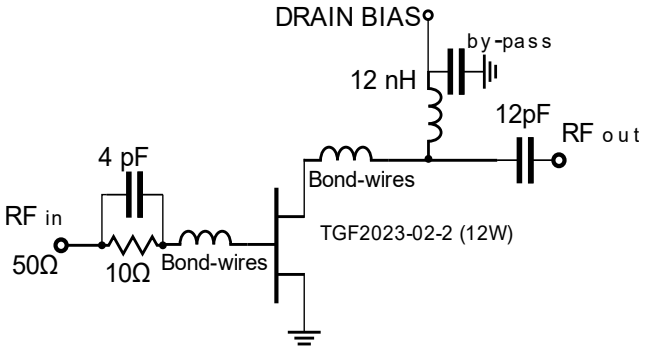

Figure 4.28 - Schematic of the individual PA branch.

The fabricated PA is shown in Figure 4.29. The Chireix compensation elements denoted as inductors L1 and L2 were determined and fitted during initial

measurements by trial and error. Inductors with values 3.6 nH and 2.2 nH for L1 and L2, respectively, were finally chosen to provide the best bandwidth performance.

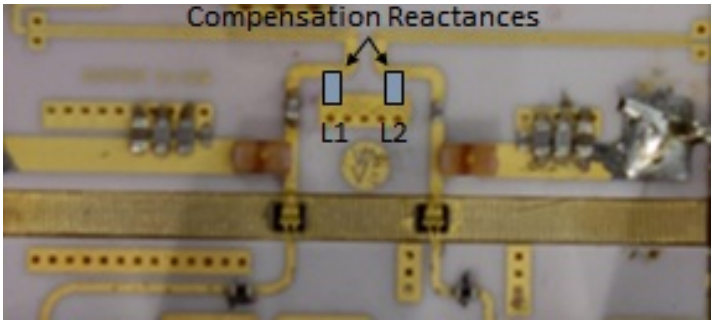

Figure 4.29 - Photograph of the proposed outphasing system (26 mm x 19 mm).

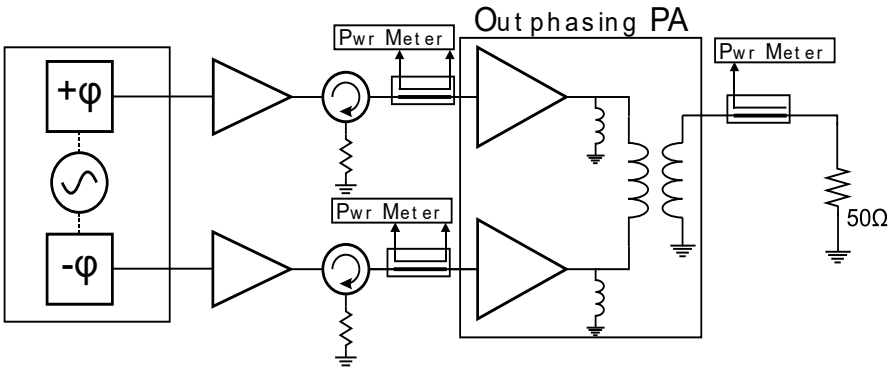

Figure 4.30 - Outphasing circuit.

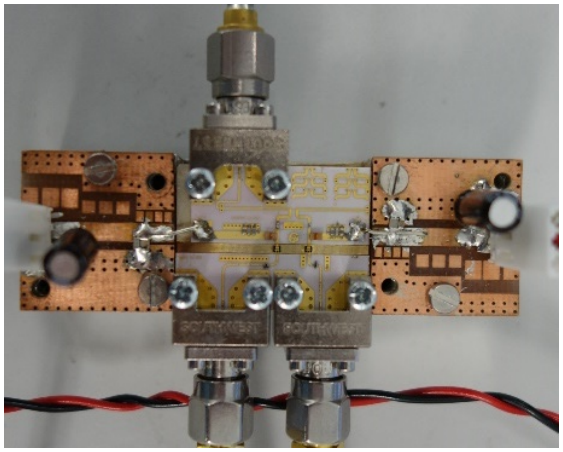

Figure 4.31 - Outphasing PA on its launcher fixture.

4.2.3 Experimental verification (Measurements)

The characterisation has been carried out using the measurements system described in Chapter 6. During the characterisation at each given frequency, the PA

was fed using signals of equal amplitude with full phase sweep, while the input/output power, and DC power consumption were measured and recorded. This cycle was repeated, while the amplitude of input signals was backed off in steps of 1 dB

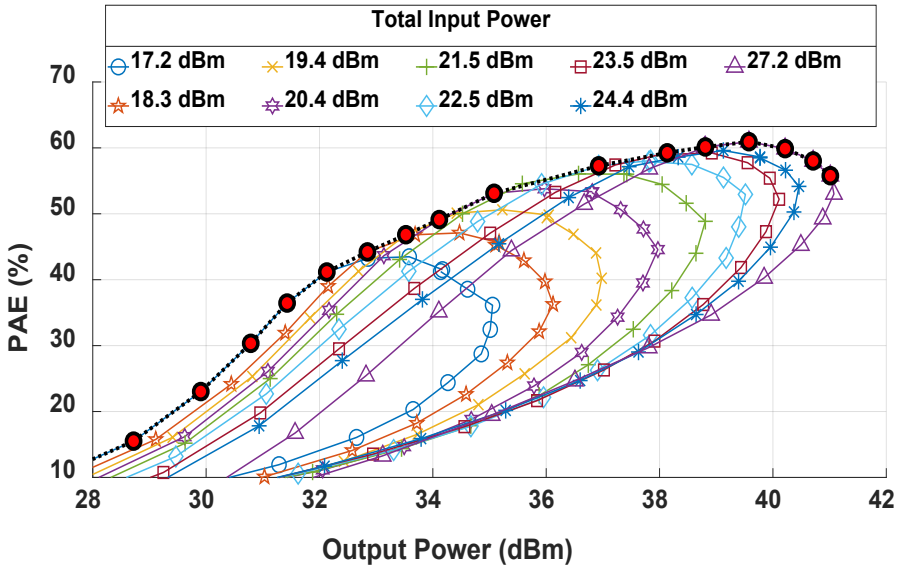

Figure 4.32 - CW Characterisation of the proposed outphasing system, measured at 1850 MHz Output power back-off is realised by means of controlling both the phase and the amplitude of input signal. The achievable system PAE is marked by dotted line.

A first set of measurements was completed collecting data over a wide range of frequencies. However, since no input matching was used, for a meaningful calculation of the PAE, the input mismatch needed to be measured. Therefore, two directional couplers were added to the system for a second round of measurements, and the input reflection coefficient $|\mathbf{\Gamma}_{IN}|$ for each active device was calculated using the measured forward and reflected power in (4.5). Then, PAE could be calculated using (4.6).

$$|\mathbf{\Gamma}_{IN}|^2 = \frac{P_{REF}}{P_{FWD}} \tag{4.5}$$

$$\mathrm{PAE} = \frac{P_{\mathrm{out}} - P_{\mathrm{IN1}}(1 - |\Gamma_{\mathrm{IN1}}|^2) - P_{\mathrm{IN2}}(1 - |\Gamma_{\mathrm{IN2}}|^2)}{P_{\mathrm{DC}}} \tag{4.6}$$

Unfortunately, the PA was damaged during the second set of measurements, and only one frequency (1850 MHz) was fully characterised to obtain $|\Gamma_{IN}|$. The performance at this frequency was calculated using (4.6) and is shown in Figure 4.32. The PA reached a maximum output power of 41.1 dBm, where its PAE was 58%, 55% and 44% at saturation, 6 dB and 8 dB OBO, respectively. A maximum PAE of 61% was reached at 1.5 dB OBO. The PAE for the other frequencies, as shown in Figure 4.33, was estimated using the reflection coefficient obtained at 1850 MHz.

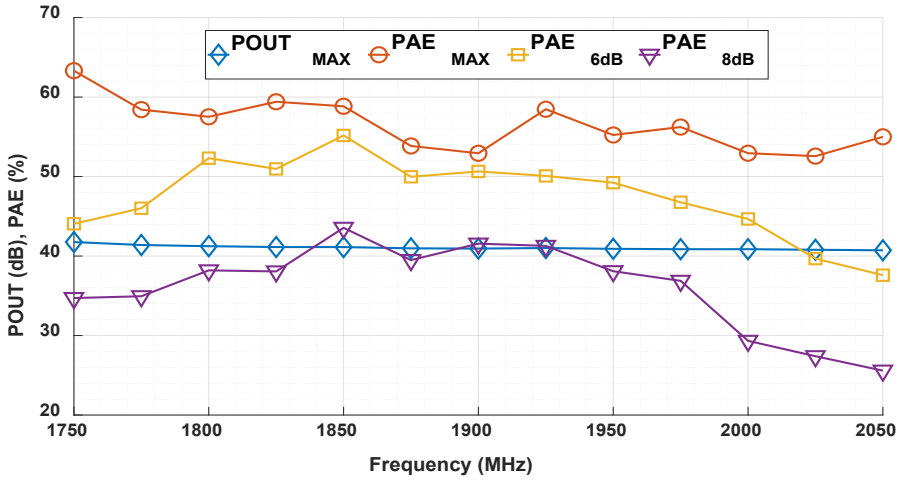

Figure 4.33 - Performance of the proposed outphasing system vs. CW frequency. PAE is estimated using the reflection coefficient measured at 1850 MHz.

Figure 4.33 shows the performance of the described outphasing PA across 300 MHz of bandwidth, spanning from 1.75 GHz to 2.05 GHz. The maximum output power is maintained within 0.5 dB of 41.2 dBm. Efficiency at the peak output power is around 60% with the highest figure at 1.75 GHz and lowest at 1.9 GHz. Efficiency at 6 dB OBO was around 45% with the highest value of 55% measured at 1.85 GHz and the lowest, 38%, estimated at 2.05 GHz. Possible improvements are expected after further reduction of drive power at frequencies above 1.975 GHz, a case not tested in the first run of measurements.

4.2.4 Conclusions

This work produced a 1.25 - 4.7 GHz balun with low trace separation, making it particularly suitable for PA applications in balanced or outphasing amplifier topologies. A novel method of interconnection, using metal bridges supported by polyimide pillars, is adopted as an alternative to bond wires. The top structure profile was lowered to less than 10 microns which eliminated the discontinuities created by the pads required for bond-wires. The repeatability of the bridging structure was verified across three measured balun samples.

The outphasing PA, working at the centre frequency of 1.9 GHz, demonstrates a 15% bandwidth with stable peak power output within 0.5 dB of 41.2 dBm. Input reflection coefficients was measured during PA characterisation using signals operating at 1.85 GHz and were subsequently applied to estimate the power added efficiency from previously measured data, where such coefficient was not recorded. Since the best performance is observed during this measurement, it is possible that efficiency figures are underestimated and therefore could be improved by repeating measurements, where input reflection coefficient is measured for each given frequency. The efficiency was further hindered by losses introduced by the output structure. Full bandwidth of the output structure, although broadband, could not be fully utilised in this work.

4.3 References

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CHAPTER 5

CURRENT MODE OUTPHASING (CMOP)

This chapter introduces and describes the concept of Current Mode Outphasing (CMOP) where the active devices operate in principle as current sources rather than voltage sources. The Output power Back-Off (OBO) is realized using relative amplitude and phase control of the input signals, with the difference that maintaining device operation in a non-saturated mode ensures that active devices operate as current sources and therefore can be combined through a convenient single-ended load, rather than a differential load as in the traditional Chireix outphasing or a combining structure as proposed by Raab [1]. Using this design approach, an amplifier is realized with a fractional bandwidth of 45%, which is, to the authors' knowledge, the widest reported bandwidth for an outphasing power amplifier. The advantage of not needing a specialist combiner, often implemented using balun or λ/4 transmission line (TL), allows for straightforward circuit integration and fabrication using MMIC technology, leading to footprint reduction. In this work, the stabilized circuit, pre-matched to 50 Ω, delivered 20 W output power for signals operating in the range of 2.55 to 4.05 GHz and was fully integrated on a 2.3 mm x 2.8 mm die.

A novel PA architecture is presented based on the outphasing solution proposed by Chireix. The principle of operation and design process is described for a fully integrated MMIC prototype fabricated in WIN Semiconductor GaN-on-SiC 0.25 µm technology process. In Chireix's original outphasing paper and most

presented work on this subject, active devices operate in saturation mode and are assumed to behave as voltage sources. In this work, however, active devices are modelled as current sources, which are typical for most semiconductor devices when operating in their linear or non-saturated mode, and the non-isolating power combiner, typical for Chireix outphasing circuits, is no longer required with a simple series compensation reactance used instead of traditional shunt elements. The demonstrator circuit, entirely contained within 2.3 mm x 2.8 mm die, is characterized using CW signals, achieving a bandwidth of 1.5 GHz centred at 3.3 GHz where maximum output power remains within 43 dBm ± 0.5 dB. Output power back-off (OBO) is controlled by both phase and amplitude of the input signals.

5.1 Introduction and motivation

Much work dedicated to outphasing still follows the original Chireix analytical derivations, improved by Raab in the '80s [1], as discussed in Chapter 4, where the active devices operating in saturation are approximated as voltage sources. Work presented in this chapter introduces a fundamentally distinct approach to outphasing; the Current Mode Outphasing (CMOP). Not only is the assumption that active devices operate in saturation as voltage sources discarded, but the circuit is analyzed using linear controlled current sources. Furthermore, the mode of the operation itself is based on the control of the current (phase and amplitude) of the two devices. This significant and distinct difference allows for improvements over the traditional outphasing approach. Also, in this work, OBO is realized using amplitude and phase control of the input signals; these are used to maintain, at any given time, constant and full output voltage swing of the active devices without driving them into deep compression. This leads to good efficiency and gain, which translates into PAE figures closer to maximum DCRF efficiency.

Another crucial difference in this work, compared to Chireix outphasing, is the use of a grounded, common-mode load, as distinct from the differential load which is mandated in the classical configuration. Thus, the use of a power combiner that incorporates inverting sections can be avoided; in Chireix outphasing, this element is often realized using structures such as baluns (see Chapter 4) or transmission lines [2], [3] whose physical size is closely associated with $\lambda/4$, which at sub-6 GHz frequencies can dominate the final size of a circuit. For this reason, in work describing integrated RFIC outphasing circuits, the power combiner is often deployed off-chip. Such work can be found in [4], where the package integrated outphasing circuit achieves 350MHz bandwidth and output power similar to the present work. Despite the package having dimensions 13 mm x 14 mm, the effective area of the final circuit was quoted as 470 mm^2 as the matching network and combiner were deployed off-

chip. These combiner implementations, along with the intrusion of device parasitics, restrict the operation of the Chireix outphasing technique in practice to moderate or narrow bandwidths [5]. For example, outphasing circuits operating in the sub-6 GHz, do not usually offer bandwidths of more than a few hundred MHz [6], [7]. It should also be noted that the frequency response of an outphasing PA has at times been quoted in terms of -3 dB bandwidth [8]; a figure which is more commonly used in filter design rather than a PA performance metric

In this work, an MMIC demonstrator is designed and fabricated, with a size of 2.3 mm x 2.8 mm, that delivers continuous 20 W output power in the 2.55 – 4.05 GHz range. To the best of the authors' knowledge, this is the largest fractional bandwidth achieved in an outphasing PA, as reported in the literature. Given its size, power output, and frequency, this novel PA architecture constitutes the state-of-the-art outphasing design.

The chapter is organized as follows: Section 6.2 describes the CMOP concept using ideal device models. Section 6.3 compares different ways of driving the ideal devices with relative advantages and disadvantages. Section 6.4 shows the design procedure by using the demonstrator circuit as a guide. Section 6.5 reports the measurement results, while Section 6.6 considers key conclusions.

5.2 Theory of operation

Figure 5.1a shows a typical circuit model used to describe a Chireix outphasing PA. Power is delivered to the load R_L, connected differentially across the outputs of branch PAs, operating in saturated mode and therefore approximated as voltage sources. The output power is varied by adjusting the outphasing angle between the two sources. Such operation creates a load modulation effect, and therefore the impedance seen by each PA varies and depends upon the outphasing angle, load R_L, and reactance X. Further analysis has already been described in Chapter 3 and was omitted in this section.

The proposed CMOP architecture is depicted in Figure 5.1b, where the voltage drop V_L across load resistor R_L is given by:

$$V_L = R_L(I_1 + I_2) \tag{5.1}$$

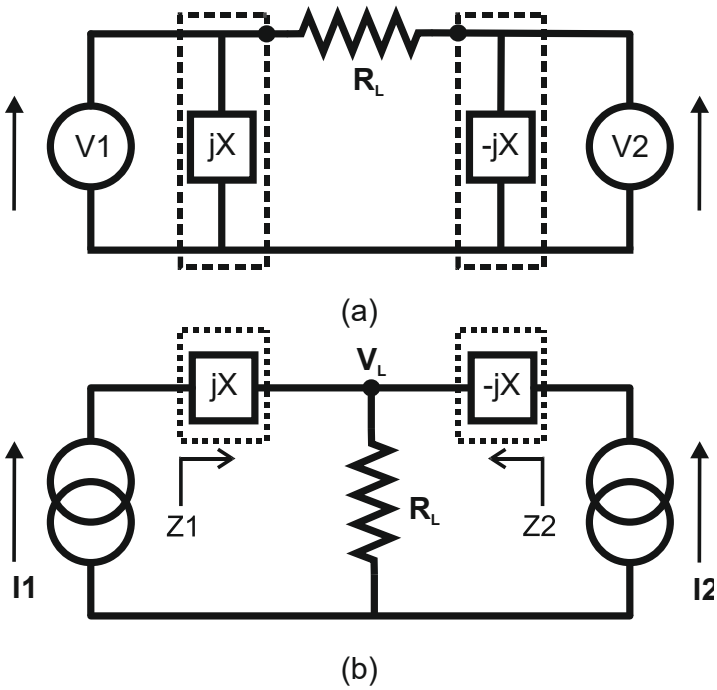

Figure 5.1 - Circuit model describing an outphasing PA: a) typical Chireix implementation, b) current mode operation proposed in this work.

With reference to Figure 5.1b, if currents $\boldsymbol{I}_1$ and $\boldsymbol{I}_2$ have equal magnitude I_M and a phase offset φ, so that $I_1 = I_M$ and $I_2 = I_M e^{j\varphi}$, the impedances Z_1 and Z_2 presented to each device can be described as:

$$Z_1 = R_L\left(1 + \frac{I_2}{I_1}\right) + jX = R_L(1 + e^{j\varphi}) + jX \tag{5.2}$$

$$Z_2 = R_L(1 + e^{-j\varphi}) - jX \tag{5.3}$$

These impedance trajectories, as φ varies, are shown on Smith charts in Figure 5.2, where the load modulation action, due to varying phase difference between outputs of each generator, is captured in the form of trajectories.

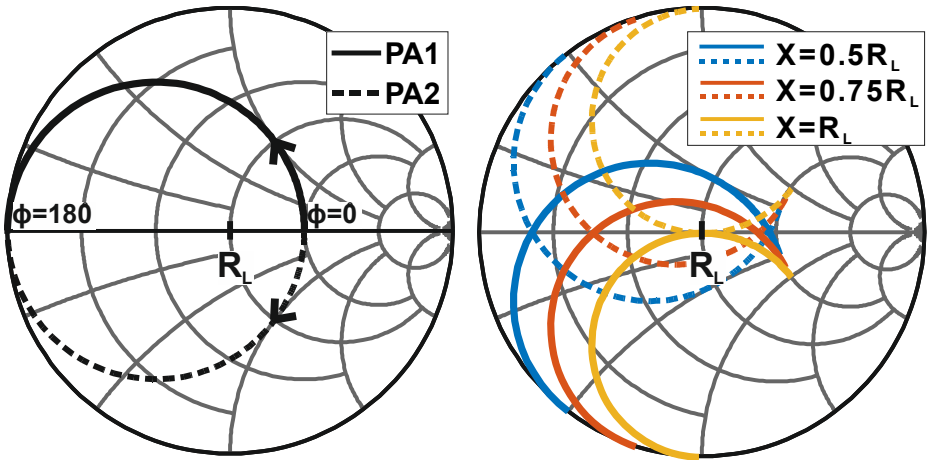

Figure 5.2 – Load modulated impedance presented to each branch PA as the relative phase between signals φ is varied from 0° to 180°: a) without compensation, b) with compensation X/R_L = 0.5, 0.75 and 1.

Where no compensation is introduced, the impedance trajectories follow a constant conductance circle, resulting in short circuit condition when φ = 180° and real impedance 2 R_L when φ = 0°. Adding a series compensation reactance ±jX, offsets the circular trajectories by "resonating-out" unwanted reactance at the chosen

phase angle φ_{comp}, in a very similar fashion as proposed by Chireix, thus improving efficiency.

A constant output voltage swing (targeted to be equal to V_{DC} in an ideal case) is maintained by means of control of the magnitude given the relative phase between output currents $\boldsymbol{I}_1$ and $\boldsymbol{I}_2$. Therefore, a relationship describing the requirement for the output current is given by:

$$I_M = \frac{V_{\mathrm{DC}}}{|Z_1|} = \frac{V_{\mathrm{DC}}}{|Z_2|} \tag{5.4}$$

Where I_{M} depends on the relative phase between input signals φ and can be calculated as:

$$I_M(\varphi) = \frac{V_{DC}}{R_L}\left[1 + 2\cos(\varphi) + 2\frac{X}{R_L}sin(\varphi) + \left(\frac{X}{R_L}\right)^2\right]^{-\frac{1}{2}} \tag{5.5}$$

Assuming class B operation, the output power and DC power absorbed can be calculated as a function of φ:

$$P_{DC} = \frac{4}{\pi} I_{\mathrm{M}} V_{\mathrm{DC}} \tag{5.6}$$

$$P_{RF} = \frac{R_L \cdot |\, I_1 + \, I_2|^2}{2} = R_L {I_{\mathrm{M}}}^2 \left(\frac{1}{2} + \cos\varphi\right) \tag{5.7}$$

Which allows the curves shown in Figure 5.3 to be plotted, where the efficiency vs normalized output power is shown for different compensation reactance values.

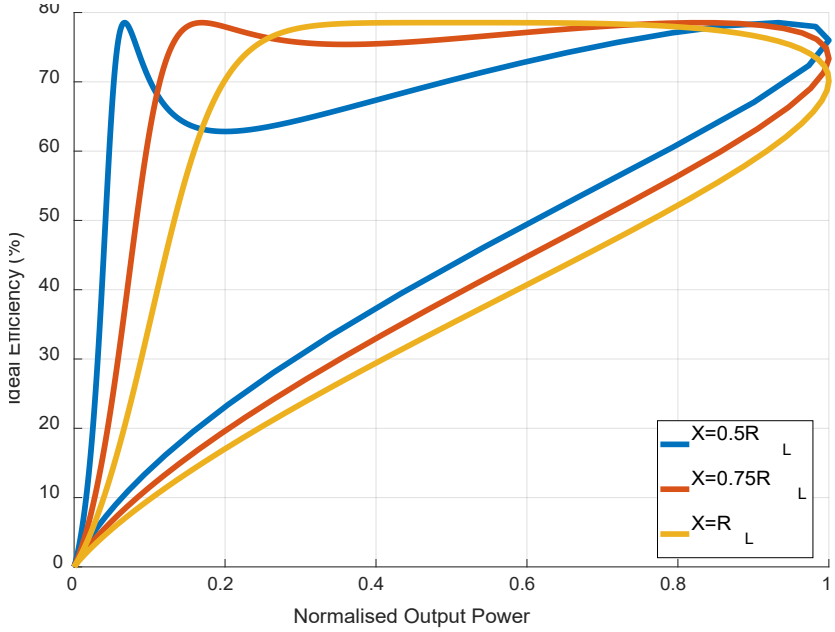

Figure 5.3 - Theoretical efficiency vs normalized output power for CMOP utilizing ideal class B PAs with X/RL ratios of 0.5, 0.75 and 1.

At this point, the analysis assumes that the PBO is implemented by varying the phase alone; in this respect, it is similar to the Chireix approach, except that the devices are current sources rather than assumed to operate as voltage sources. The next section will show that in a CMOP the PBO can alternatively be implemented by backing off the drive to the devices, thus reducing compression and preserving PAE.

5.3 Input Drive Strategy

The hysteresis of the efficiency vs power curves can be better understood by observing the two quantities plotted separately, each vs the outphasing angle, see Figure 5.4.

It can be noted that pushing the outphasing angle φ beyond a value φ_{MAX} will not benefit either output power or efficiency. φ_{MAX} corresponds to the point of maximum output power and can be calculated by setting the first derivative of the output power as a function of φ to zero:

$$\varphi_{\mathrm{MAX}} = 180 - \tan^{-1}\left(\frac{\frac{4X}{R}}{4 - \left(\frac{X}{R}\right)^2}\right) \tag{5.8}$$

Conversely, φ = -180° can be considered as the other limit of the outphasing angle, which is where no output power is generated.

However, by observing the $I_M(\varphi)$ vs φ (plot shown in Figure 5.5) it can be seen that there is a value of φ, indicated as φ_{MIN}, where the slope of $I_M(\varphi)$ changes sign, meaning that a higher input drive is required to decrease the output power. Apart from affecting the gain and PAE, such an arrangement is difficult to implement in a real scenario due to the change of slope that would appear in an output power vs input power function.

This point is found by investigating and solving the derivative of (5.6) in order to obtain function minima:

$$\varphi_{\mathrm{MIN}} = -\tan^{-1}\left(\frac{X}{R}\right) \tag{5.9}$$

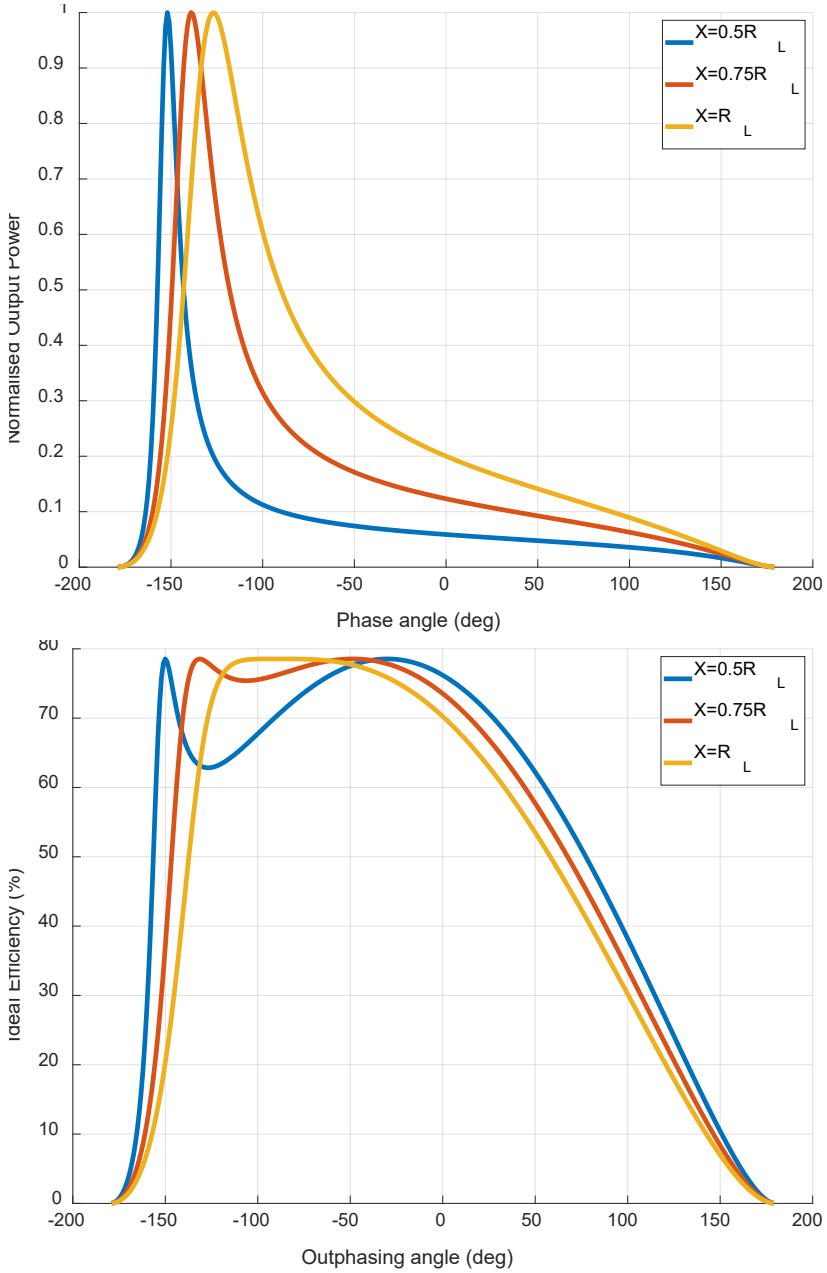

Figure 5.4 - Normalized output power (top) and theoretical efficiency (bottom) vs outphasing angle for CMOP utilizing ideal class B Pas for X/RL ratios of 0.5, 0.75 and 1.

An alternative input drive approach therefore is to stop relying on outphasing at φ_{MIN} and achieve further OBO is by reducing the input drive, and consequently the output current while maintaining a fixed phase φ_{MIN}between currents $\boldsymbol{I}_1$ and $\boldsymbol{I}_2$.

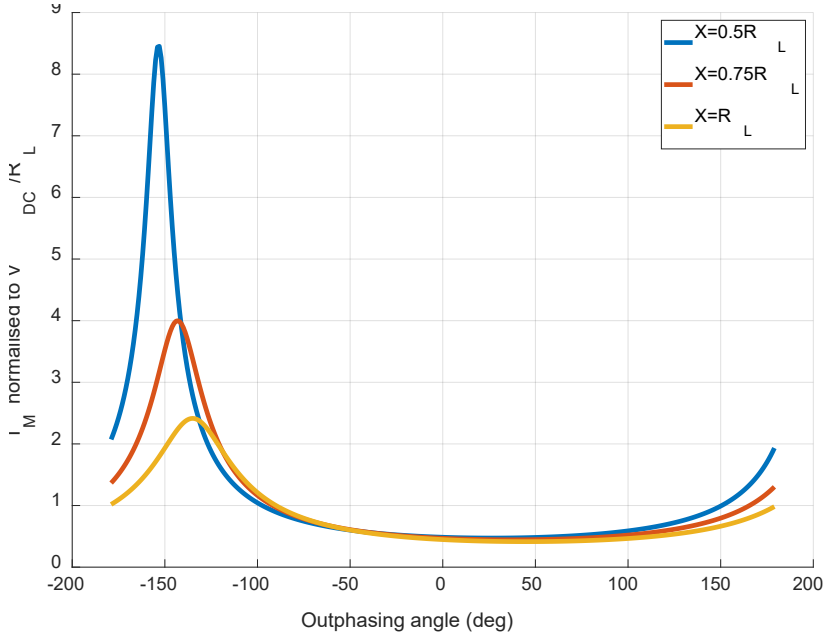

Figure 5.5 - Normalized current vs outphasing angle for CMOP utilizing ideal class B PAs X/RL ratios of 0.5, 0.75 and 1.

The theoretical DC to RF efficiencies of the CMOP circuit in Figure 5.1b, employing *X*/*R* ratios of 0.5, 0.75 and 1, are plotted in Figure 5.6. The solid line on that plot represents efficiency for OBO realized by means of varying the relative phase and magnitudes of output currents $\boldsymbol{I}_1$ and $\boldsymbol{I}_2$, while the dotted line shows OBO region where the power reduction was achieved solely by control of magnitude for each output current, whilst the relative phase stays fixed as given by (5.8).

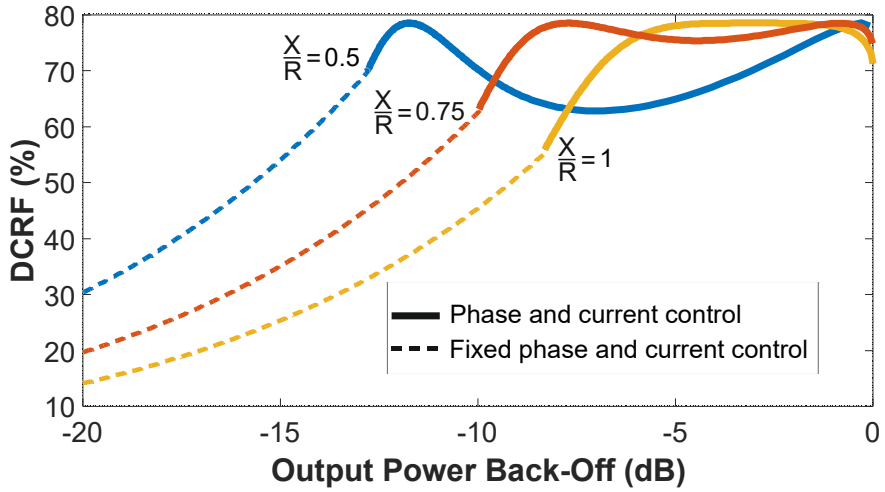

Figure 5.6 - Theoretical OBO and DC to RF efficiency for CMOP utilizing branch PAs biased in class B or deep class AB for X/R ratios of 0.5, 0.75 and 1.

5.4 Design Strategy and Implementation

The circuit to demonstrate the CMOP concept was designed using Advanced Design System (ADS) software by Keysight and the dedicated PDK for the GaN 0.25 µm HEMT technology process provided by Win Semiconductor. The centre frequency was chosen as 3.25 GHz. The design was simplified by assuming load termination as R_L = 50 Ω, and therefore no provisions for output matching networks were necessary. Following (5.2) and (5.3), such termination would allow load modulation up to around 100 Ω. Active devices, 12 x 200 µm, with the estimated optimum intrinsic load R_{OPT} = 25 Ω and parasitic output capacitance C_{DS} = 1.5 pF were chosen for the design of each of the branch PAs. The output capacitance is absorbed by the on-chip bias inductor, as shown in Figure 5.7, in order to minimize the impact and interaction of C_{DS} with load compensation reactances. It was shown earlier, in Figure 5.6, that choosing X/R_L = 1 should allow just over 8 dB OBO to be realized by controlling the relative phase and magnitude of the output currents. Consequently, X = 50 Ω was realized using inductor L_{COMP} = 2.6 nH and C_{COMP} = 1 pF for each branch PA, as shown in Figure 5.7.

Each branch PA was biased in deep class AB with I_{DQ} = 40 mA and operating from a DC supply rail of V_{DC} = 28 V. The input was matched to 50 Ω using an on-chip low pass filter, consisting of a series inductor and shunt capacitor with values 1.15 nH and 0.8 pF, respectively. Gate bias voltage is supplied using a 5 Ω resistor in series with a 0.7 nH inductor, and the former is also a part of the stability network. Further stability was attained using a parallel R/C network, as depicted in Figure 5.7

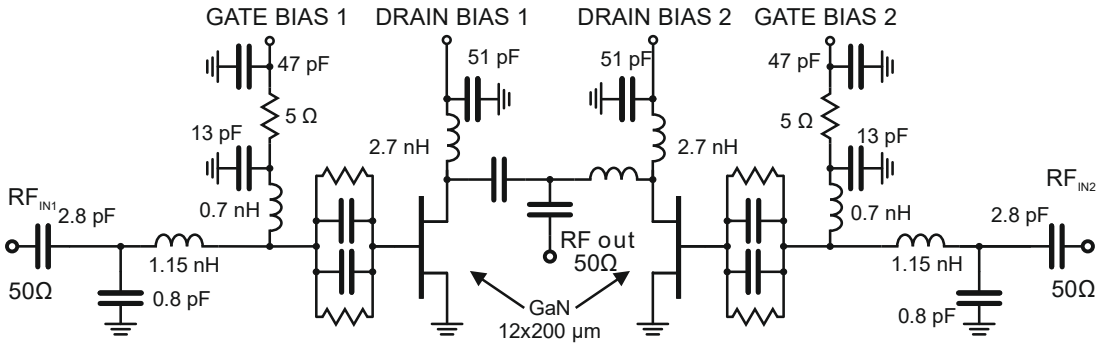

Figure 5.7 - Full schematic of the proposed CMOP demonstrator circuit.

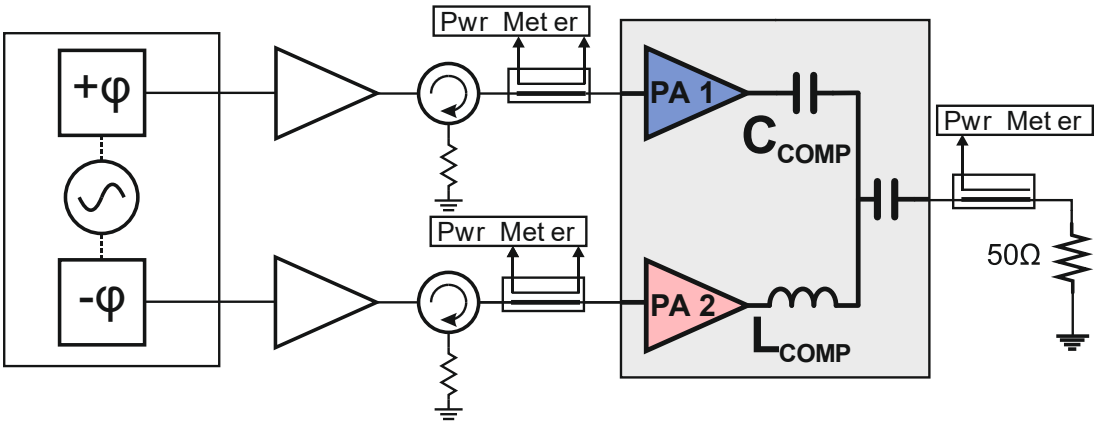

Figure 5.8 - Diagram of the measurement setup used for CW characterization of the CMOP circuit, here enclosed by shaded rectangle, showing two branch PAs and compensation/combination reactance LCOMP and CCOMP.

Simulated DC-RF efficiency for the circuit operating at 3.25 GHz is shown in Figure 5.9. The simulation was set up for each branch PA to be excited using an input power P_{in} ranging from 16 to 24 dBm in steps of 0.5 dB and 25 to 30 dBm in steps of 1 dB. The 1 dB and 2 dB compression points were established at P_{in} = 26 dBm and 28 dBm, respectively, where the simulated output power reached 42.4 dBm and 43.2 dBm. The corresponding system gain was calculated to be 13 dB and 12 dB, respectively. Figure 5.9 shows that outphasing *combined* with output current control is used to reduce output power by around 5 dB from the maximum to 38.5 dBm, further power reduction is achieved using the linear scaling of the output current by reducing the drive power P_{in} and corresponds to the predicted action shown in Figure 5.6 for the case of $\frac{X}{R} = 1$.

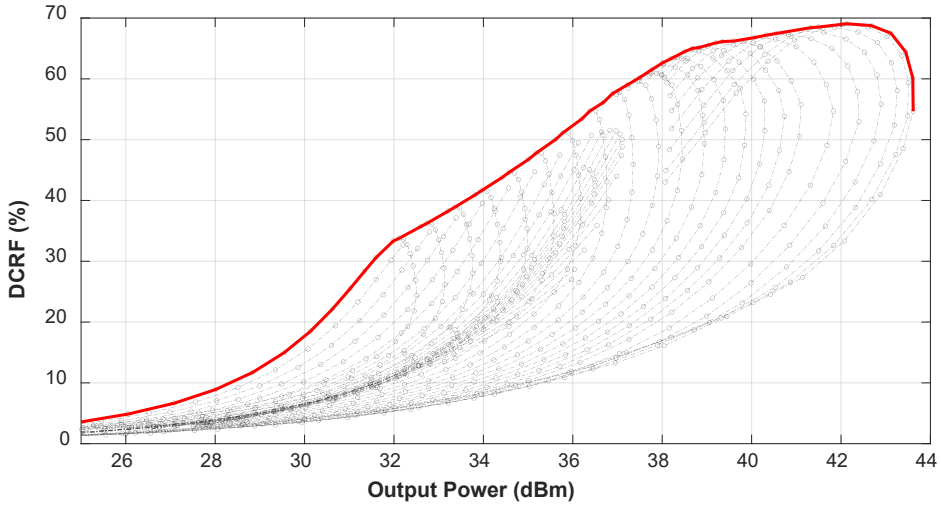

Figure 5.9 - Simulated performance of the demonstrator circuit. Grey traces represent the response of the circuit during full, 180° relative phase sweep when the circuit is excited with input power varied from 30 dBm to 24 dBm in 1 dB steps and from 24 dBm to 16 dB.

The fabricated MMIC is presented in Figure 5.10. The actual CMOP circuit occupies an area of 2.3 mm x 2.8 mm, and the remaining space was dedicated to test structures used for individual characterization of the key components of this design. Bond wires were required to provide connectivity between on-chip bias inductors and by-pass capacitors.

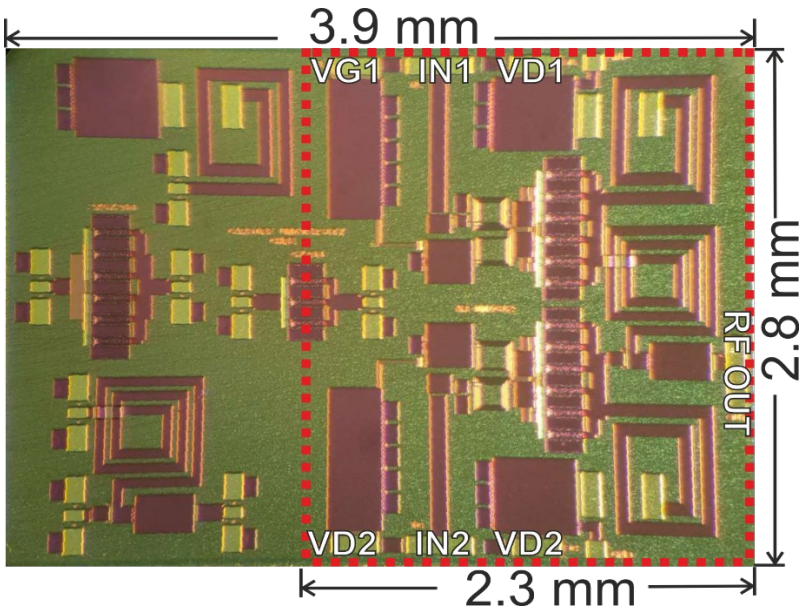

Figure 5.10 - Photograph of the fabricated MMIC chip, containing test structures and the CMOP circuit, which is enclosed with a dashed line.

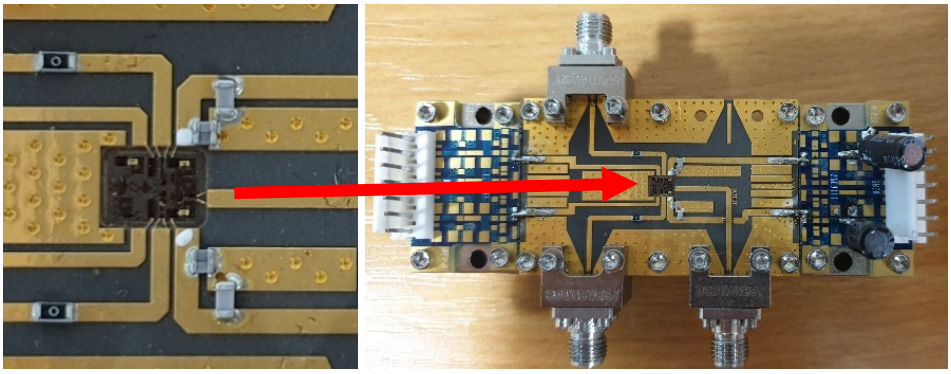

Figure 5.11 - The fixture used to deploy and interface with the MMIC chip with CMOP demonstrator.

A dedicated PCB fixture, fabricated on 0.2 mm thick, metal-backed Rogers Duroid 5880 substrate with $\varepsilon_r = 2.2$, was used to launch and to interface with the fabricated MMIC chip. Additional SMD by-pass capacitors were assembled off-chip on the PCB traces supplying DC to the MMIC nodes VD1 and VD2, as shown in Figure 5.11.

5.5 Experimental Verification

The characterization of the CMOP circuit was carried out using the measurement system described in detail in Chapter 6 and shown again in Figure 5.8. The input signals were generated using an Anritsu MG3710A dual output signal generator. A vector containing *I* and *Q* samples was uploaded to the instrument using a Matlab script via LAN connection. An internally shared Local Oscillator (LO) and synchronized baseband generators ensured the phase coherency and time alignment between the two generated signals.

During the characterization at each given frequency, the circuit was excited using signals of equal amplitude over a full relative phase sweep, while the input/output power and DC power consumption were measured and recorded. The forward and reflected powers were measured using input couplers to calculate input power supplied to each branch PA. This cycle was repeated while the amplitudes of input signals were gradually backed off. The effect of the full, 360° sweep of the relative phase between input signals was captured in the form of "loops" plotted in Figure 5.12, this was explained in the previous section and is attributed to the fact that 180° sweep is required to achieve the relevant OBO and maintaining high efficiency. The further 180° sweep also results in output power reduction. However, as previously discussed, the efficiency is lower during this part of that sweep.

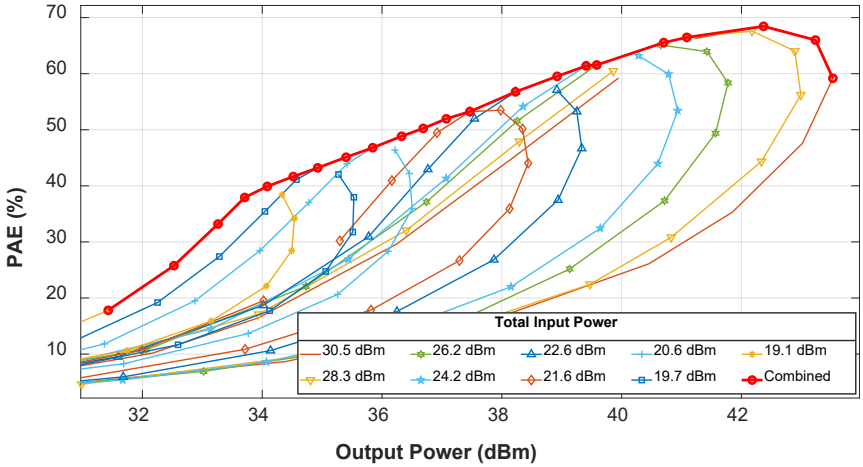

Figure 5.12 - Measured performance of the proposed CMOP circuit.

The characterization process illustrated in Figure 5.12 was repeated for frequencies of 2.55 to 4.15 GHz, and the collated performance characteristics are shown in Figure 5.13. The output power remains within 43 dBm ±0.5 dB while the peak of maximum PAE of 68.5% is achieved at 3.25 GHz and remains > 60% for frequencies 2.85 to 3.8 GHz and above 50% for almost the entire frequency range. The OBO efficiency also reaches its peak at 3.25 GHz with 53.5% and 45.6% for 6 dB and 8 dB OBO, respectively, and remains above 30% and 23.7% for the entire frequency range. The gain, recorded at the maximum output power, was measured to be 13.1 dB at 3.25 GHz and remains above 10 dB for almost the entire frequency range, i.e., all frequencies except the 2.55 GHz, where it was measured to be 9.8 dB. A gain over 12 dB was measured for frequencies in 2.95 to 3.95 GHz.

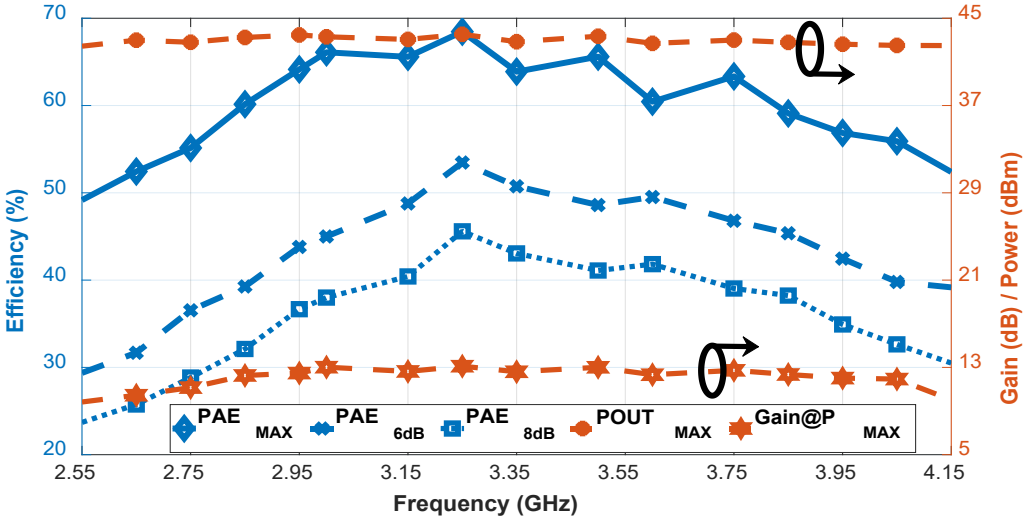

Figure 5.13 – Measured broadband performance of the CMOP circuit.

5.6 Conclusions

This chapter presents a novel PA concept derived from the Chireix outphasing topology. Theory and modelling are in good agreement with the simulated and measured data. The drawbacks and limitations associated with Chireix outphasing are addressed by operating the active devices as current sources. This allows full utilization of the gain offered by these devices, which in turn translates onto PAE figures close to maximum DC-RF efficiency. Another benefit of current mode operation, and the distinct feature of this design, is lack of a complex power combining structure, leading to significant circuit size reduction and improved bandwidth, here reported to be more than 45%. Unlike the Chireix solution, where the active devices need to be driven into saturation in order to maintain a constant voltage at the output, the solution presented in this paper maintains the constant output voltage by means of controlling the magnitude and the relative phase of output current from each device. The numerical solution governing this control was derived and demonstrated using an MMIC circuit deployed on 2.3 mm x 2.8 mm chip area.

The concept can benefit from further investigation, particularly in the transition points where OBO is realized initially using control of phase and then magnitude of the output currents. Consequently, the design may benefit from further efficiency improvements through such optimization.

At the time of completion of this thesis document, it was noticed that the concept very similar to CMOP had been described in a conference paper [9], and therefore it was omitted from the initial literature review. Although the authors refer to their work as Current Mode Outphasing and indeed, the outphasing analysis was provided using current sources, the authors do not claim any benefits over a typical implementation of outphasing PA. Moreover, in their work, authors still required a power combiner realized using lengthy transmission lines. Another work describing

an outphasing PA operating in the current mode was presented in [10]. The concept, referred to as inverse outphasing, was demonstrated by PA realised using a 45 nm CMOS technology operating at mm-wave frequencies. The authors targeted high-fidelity 10 Gb/s signals and wide modulation bandwidth at much lower power than power levels offered by GaN technology used in this work. The reported bandwidth of 4 GHz, centred at 29 GHz, translates to a fractional bandwidth of 13.8%, which is significantly lower than the figure reported in this work, 45%.

5.7 References

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CHAPTER 6

MEASUREMENT SYSTEMS

This chapter describes two measurement systems used to investigate key aspects described in this thesis. The first section describes an active Load-Pull system, developed initially at Cardiff University and later commercialised under the spin-off Mesuro, now part of Focus Microwave.

The second section describes a new system that was developed as part of this research project to facilitate characterisation and measurements of PAs driven with two independent input signals, with outphasing being an example of such PA topology. In the classic realisation of outphasing systems, the Signal Component Separator (SCS) section would establish and construct the input signal to drive for each branch PAs, based on the original input signal. The process was described in detail in Chapter 6. These signals would require having an equal amplitude and the relative phase offset. Since the design of the SCS section was outside the scope of this project, the input signals had to be generated independently, outside the PA; the generation section of the new measurement system is principally aimed at performing the SCS operation. This chapter details how the measurement system can generate phase-coherent drive profiles for dual input PA architectures. Although built having outphasing PAs in mind, the system is not limited to those and was successfully used to characterise other PA topologies such as Doherty PA (DPA) or Load Modulated Balanced Amplifier (LMBA). Several solutions were explored during the course of building the system, the most significant being reported in this chapter while outlining their disadvantages and thus the reasoning behind abandoning their concept. The

chapter is concluded with the measurements showing the verification procedure for CW and modulated signals.

6.1 Active Load and Source Pull

The load modulation effect, as described in Chapter 2, is intrinsically typical of Load Pull measurement systems. In principle, the performance of a DUT is investigated by presenting the desired reflection coefficient at its ports, on the output side for Load-Pull or the input side for Source-Pull. Typical measurements often involve evaluating performance (gain, PAE, efficiency, etc.) at reflection coefficient points on a region of the Smith chart and are represented by contours of a constant level [1]. This way, the performance of a DUT can be assessed without the necessity of building designated fixtures and auxiliary circuit elements, such as impedance matching networks.

Figure 6.1 - Load Pull measurement system deployed at Cardiff University based on PNA-X.

The bandpass multiplexers are used to inject signals independently between fundamental and harmonic frequencies. The system used for this work, shown in Figure 1.1, was an active source/load pull system based on a Keysight's PNA-X as receiver configured as shown in Figure 1.2. That instrument allows access to the

internal coupler arm path, which in turn enables usage of external couplers, located much closer to DUT improving flexibility and stability of calibration.

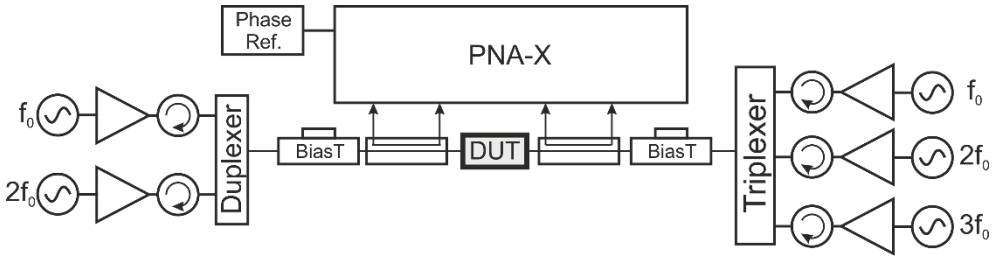

Figure 6.2 - Schematic of Load Pull system used in this research work.

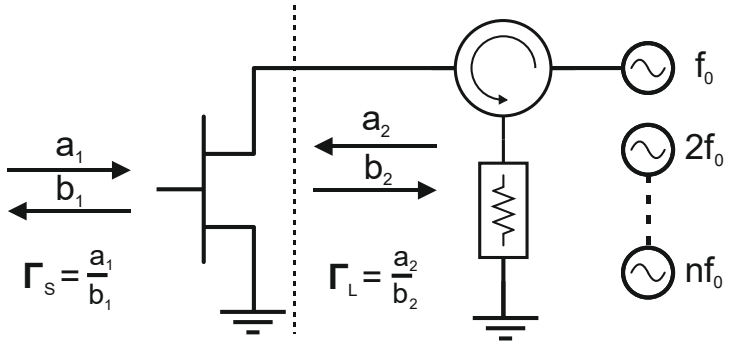

Figure 6.3 - a and b waves

Three signal sources on the output side of DUT were used to control load impedances at fundamental, second and third harmonic frequencies. The control of a second harmonic impedance on the input side was configured to present a short circuit condition. This was shown to improve and speed up the process of establishing the desired second harmonic impedance at the output since it decreases dramatically the impact of the second harmonic generated at the non-linear gate-to-source capacitance of the device. The desired reflection coefficient is achieved by injecting signals through circulators, as depicted in Figure 6.3. Circulators ensure that the reflected signals are attenuated and terminated with a 50 Ω load, thus isolating the signal booster amplifiers used.

The inclusion of a phase reference unit, here realised using a comb generator in a similar fashion as described in [2], allows the reconstruction of voltage and current time-domain waveforms at the DUT ports at each measured gamma point. This feature was particularly useful to plot a dynamic load-line and create fan diagrams in Chapter 7.

The limitations of this load pull system are imposed by several factors. The frequency limit of PNA-X, 26.5 GHz, encompasses fundamental and harmonic frequencies. Therefore, for measurements, maximum fundamental frequency is around 8 GHz if control of 2^{nd} and 3^{rd} harmonics is also required. The system is currently set up to work with CW only. The relevant PNA-X options for pulsed operation are present, however. The power handling is currently limited by components on a direct RF path, mainly RF probes and bias-T elements, typically does not exceed 20 W at 2 GHz. Since the PNA-X measures *a* and *b* waves through an external coupler, the excess power can be attenuated as needed to protect the instrument and couplers can be tailored for the specific requirements. Although active load-pull allows presenting any Γ, even outside the unity Smith chart, it should be noted that measurement accuracy degrades for $|\Gamma| > 0.85$ due to a typically lower calibration accuracy at that part of Smith chart.

6.2 Phase Coherent Characterization System dedicated for dual input PAs

The characterisation of outphasing PAs required generating signal profiles with known phase offset. The phase stability, accuracy, and repeatability were cordial to the accurate characterisation of the outphasing PAs described in this document.

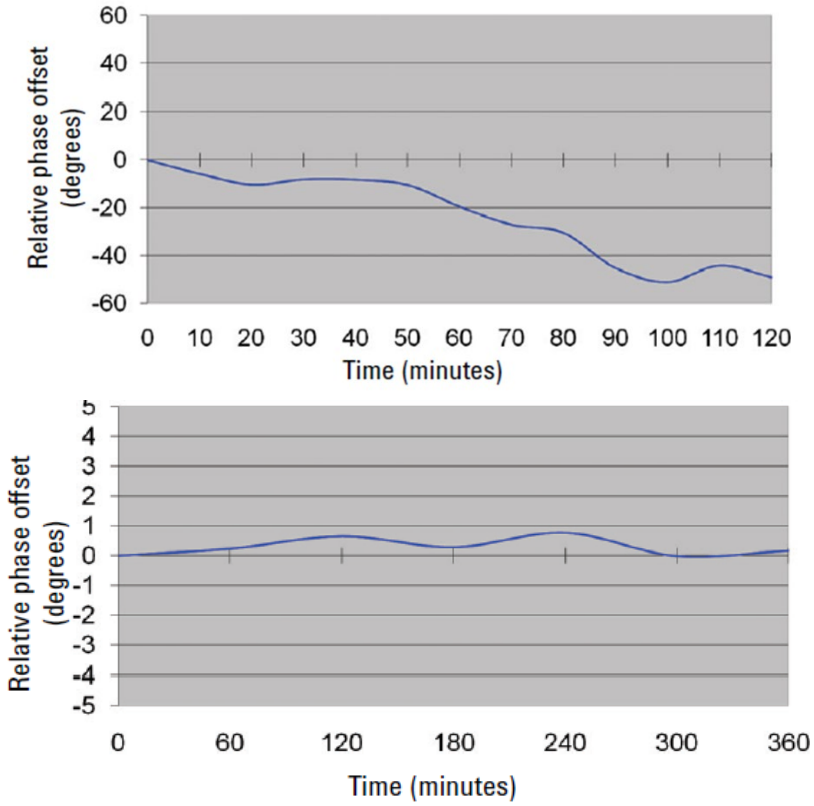

Figure 6.4 - Comparison of the phase stability of two signal generators achieved using 10 MHz reference signal (top) and by sharing LO (plots reproduced from [3]).

Initially, the measurement system was deployed using Keysight's PSG E8267D and/or ESG E4421B, available at CHFE. The most common and often sufficient method of synchronising the units is using a 10 MHz reference signal but unfortunately would not provide acceptable phase stability [4], as shown in Figure 6.4. Although both units would be frequency-locked, and some level of phase stability would be achieved, the resulting phase coherence was deemed unacceptable for the purpose of this work for two main reasons. Firstly, let's imagine a measurement where the relative phase setting is swept over 360 degrees. When including all the swept parameters, such measurement might last several minutes, meaning that the relative phase between RF inputs of the DUT will not be the same for 0 and 360 degrees, making it impossible to have confidence in the actual phase shift range covered. Secondly, once an "optimum" phase delay is found to achieve a certain performance target, there might be an interest to use that phase delay in more advanced

measurements, at a distance of hours or even days. This clearly would not be possible with such a significant drift.

Fortunately, these signal generators have the extra option (HCC) that allows access to the LO path in each unit. The main source of phase drift over time can be attributed to the fact that each unit is using the respective internal LO. Therefore, a much greater degree of phase coherence was possible when the Master instrument's LO was split and shared with another unit (Slave) as shown in Figure 6.5. The LO signal generated by the Master device was split using a resistive 6 dB splitter and fed to both Master and Slave Signal generators. The application note from Keysight provides full guidelines on operating instruments in such configuration. Notably, the length of RF cables used to distribute LO signal was critical [1].

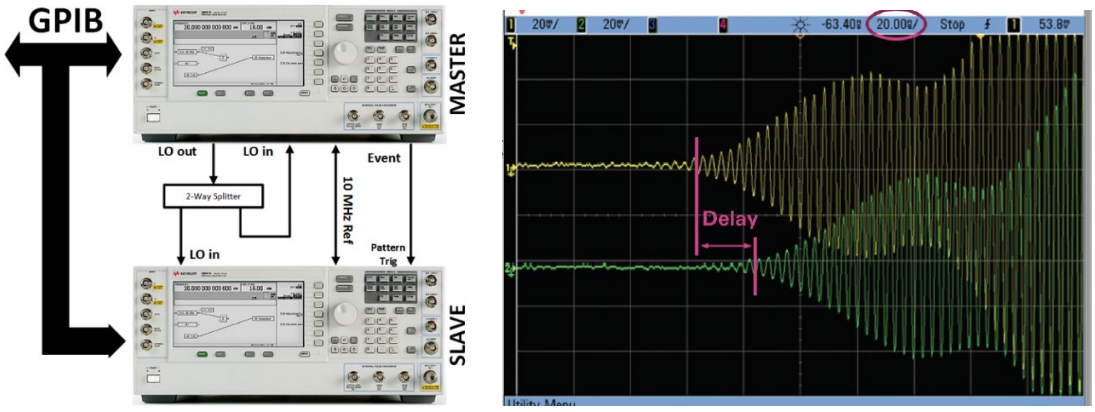

Figure 6.5 – Two PSG/ESG signal generators operating with a shared LO (left), and the BBG synchronisation issue (right).

The distinct drawback of such configurations became apparent during the verification measurements. The procedure is described in the next section. The trigger delay between baseband generators (BBGs) in each instrument required further post-processing in Matlab software to re-align demodulated I and Q samples, as illustrated in Figure 6.5. Although CW signals could be recovered that way, the

same was not possible for modulated signals. This is a known limitation of ESG/PSG instruments operating with shared LO and was addressed in MXG signal generators from Keysight, where the instruments have a built-in software option that synchronises BBG in each MXG instrument. At this stage, the individual signal generators were replaced with the recently procured MG3710A, dual output signal generator from Anritsu, and the remainder of this chapter focuses on the system based instrument, shown in Figure 6.6

6.2.1 System description

The software controlling the measurement system was developed in Matlab® environment, taking advantage of the available instrument control toolbox. The next subsections briefly describe the operation when taking measurements using CW and modulated signals.

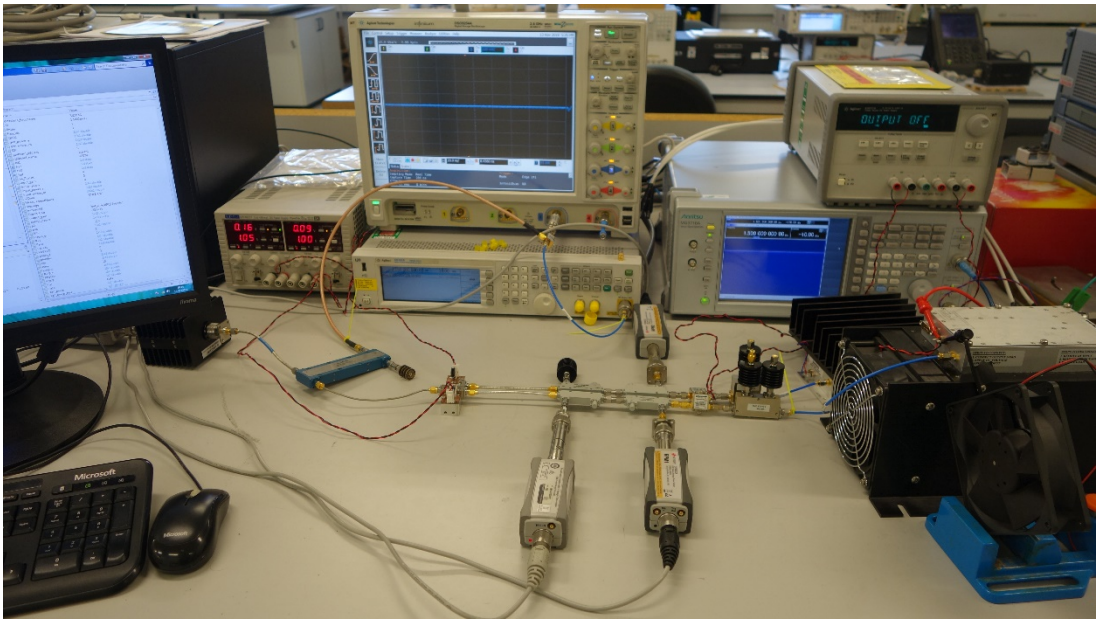

Figure 6.6 - Photograph of the measurement system described in this chapter.

The MG3710A is a 100 kHz to 6 GHz dual output RF signal generator. It can be configured to operate with the LO shared between each channel similarly as described in the previous section [5]. Each of the RF channels can operate independently, with the respective LO and BBG. The main advantage of this device

is a built-in programmable delay between BBG for each channel. This function was further described later in the section containing the verification procedures.

6.2.2 Principle of operation

The vector-matrix containing baseband I and Q samples is processed using Matlab. The amplitude and phase of the test signal is calculated using (6.1) - (6.3). For dual output operation, the first channel of the signal generator, denoted as SG1, is kept with a fixed phase ∅ and described by (6.4). At the same time, the signal for the second channel (SG2) has an additional phase offset δ introduced as described in (6.5).

$$A = I + j\,Q \tag{6.1}$$

$$|A| = \sqrt{I^2 + Q^2} \tag{6.2}$$

$$\phi = \tan^{-1}\left(\frac{I}{Q}\right) \tag{6.3}$$

$$A_{\mathrm{SG1}} = |A|(\cos(\phi) + j\ \sin(\phi)) \tag{6.4}$$

$$A_{\mathrm{SG1}} = |A|(\cos(\phi + \delta) + j\ \sin(\phi + \delta)) \tag{6.5}$$

The measurement takes the form of a parameter sweep loop, with the possibility of nested loops for one or more parameters such as amplitude, phase, and frequency. For a loop operation, signals are pre-computed in pairs for each iteration and uploaded to the instrument via LAN connection. The optional data acquisition from power supplies allows calculating DCRF and PAE using the recorded voltage and current values. A power meter is sufficient to measure the output power levels during CW characterisation, while the modulated signals are extracted from the carrier frequency using a mixer and low-pass filter to an intermediate frequency and acquired using a DSO, as shown in Figure 6.7.

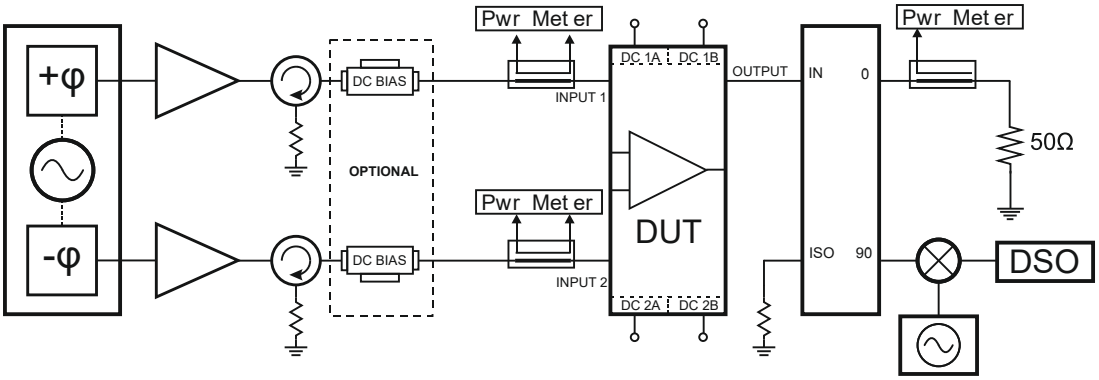

Figure 6.7 – Block diagram of the measurement system/

The system can operate with a coupler attached to each of the inputs. The power measured through these couplers provides the necessary information to calculate a magnitude reflection coefficient Γ_{IN}, given by (6.6), at each DUT input. With the presence of input couplers, the PAE can be adjusted using the operational gain as in (6.7)

$$|\Gamma_{\mathrm{IN}}|^2 = \frac{P_{\mathrm{ref}}}{P_{\mathrm{fwd}}} \tag{6.6}$$

$$\mathrm{PAE} = \frac{P_{\mathrm{out}} - P_{\mathrm{IN1}}(1 - |\Gamma_{\mathrm{IN1}}|^2) - P_{\mathrm{IN2}}(1 - |\Gamma_{\mathrm{IN2}}|^2)}{P_{\mathrm{DC}}} \tag{6.7}$$

6.2.3 Calibration and Verification Process

Before the measurements can be done, the system requires several "pre-characterisation" or calibration steps. The optional couplers on the input stage (with inclusion of attenuators if necessary) are characterised separately using a VNA and the corresponding touchstone file containing the scattering parameters is employed in MATLAB to adjust the power readings. A "thru" measurement is taken for each carrier frequency, bypassing the DUT to determine and offset losses in the signal path.

The DUT was replaced with a 6 dB resistive splitter/combiner to verify that the dual-RF setup was valid. The verification was done using a test signal generated by the LTE Matlab toolbox. Initially, a full 360º phase sweep was performed at CW with the 2 GHz carrier frequency, which allowed to find the point where signals were in-phase, i.e. with no relative phase offset present between each signal at the DUT plane. From this point, the modulated signal was introduced, and further measurements were done with the phase fixed at the previously determined value. Once acquired, the output signal was decomposed into a matrix vector containing *I* and *Q* samples and subsequently compared to the original input to determine the distortion, quantified by a Normalised Mean Square Error these samples and given in (6.8). The post-processing done in Matlab allows quantifying AM-AM, AM-PM and ACLR distortion, as shown in Figure 6.8.

$$\mathrm{NMSE} = \frac{\Sigma|x-y|^2}{\Sigma|x|^2} \tag{6.8}$$

The BBG synchronisation was achieved by determining a delay value that produced the least distortion during measurement. The delay of 37 ns between each BBG produced the most acceptable results and was used throughout all the characterisation measurements.

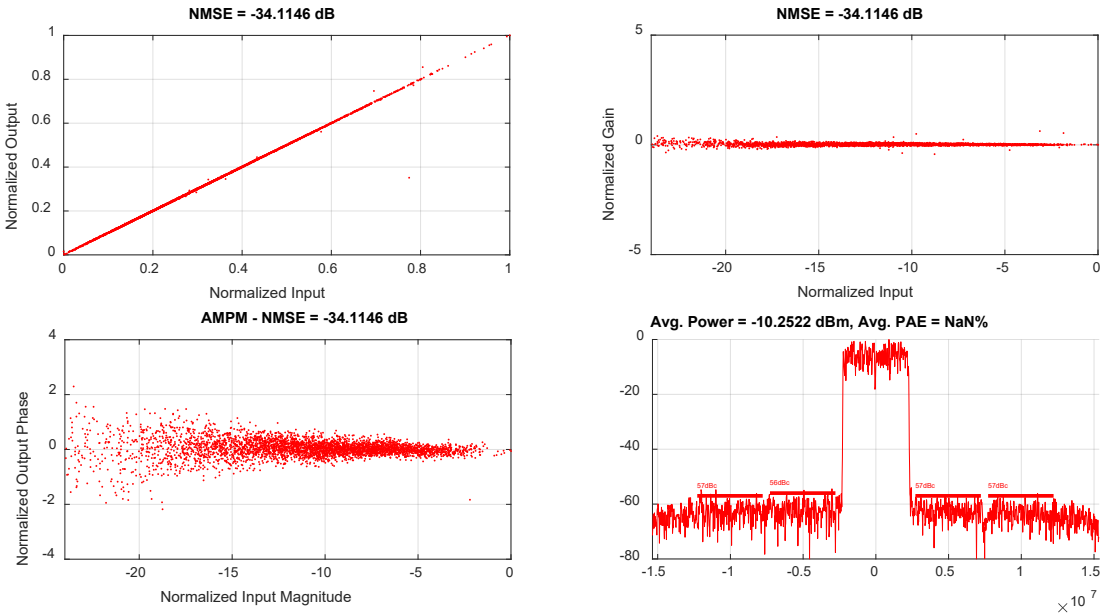

Figure 6.8 - Figure 14: Linearity (top left), phase coherence (bottom left), gain (top right) and spectrum (bottom right) of two signals generated using MG3710A and combined in-phase using 6 dB resistive power splitter. Local oscillators are shared between each channel.

6.2.4 Conclusions

This chapter summarised the development of the measurement system designed for the purpose of characterising dual input PA architectures, such as Outphasing. The verification process confirmed that the phase remained within ±2º of the originally supplied signal and would remain stable over a prolonged period, at least several days. No significant AM-AM distortion was introduced by the system either. The measured ACLR of -56 dB confirmed that the measurement system introduced no spectral regrowth. The value is well above the requirements set out for PAs designed for LTE and 5G base stations. In such cases, the maximum allowed ACLRs currently defined as -45 dB [6].

6.3 References

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CHAPTER 7

POWER AND EFFICIENCY CONTOURS IN CONTINUOUS MODES IN GAN HEMT DEVICES

This section of the thesis is dedicated to key investigations closely related to the outphasing technique and begins with a definition of a simple numerical model used to describe the non-linear behaviour of an active device, referred to as “N-model”. The numerical validation of two experiments featured in this chapter is conducted using this numerical model.

The first experiment was dedicated to investigating continuous modes when using saturated GaN HEMT devices. The original derivation of class J in [1] assumed an output voltage “grazing” zero condition, which limits the clipping of the current waveform. However, as described in Chapter 4, one of the fundamental assumptions for outphasing PAs is that each branch of the PA is operating in its saturated region, where the PA typically exhibits heavy non-linear behaviour, thus the “zero-grazing” condition is no longer valid. This experiment confirmed the continuum of class B in the saturated PA, thus it was shown that continuous PA modes, such as class B-J, are suitable for implementation in outphasing circuits.

The last section of this chapter presents a novel method of predicting power and efficiency contours for GaN HEMT devices operating in back-off conditions, using the N - model. It was shown that the efficiency contours follow a constant Q line on a Smith chart, as the input power is reduced. Observations and modelling presented in

that section can be applied during the design of an outphasing PA, to refine the choice for the necessray compensation reactance.

7.1 A Simplified Model of an Active Device – the "N - Model"

The simplified knee-model, described in [5], was shown to accurately predict the optimum power and efficiency contours for the saturated GaN devices. Work presented in this chapter utilises the same numerical model to describe the knee behaviour of an active device. The model is used to explore the power and efficiency contours for GaN devices operating in saturated and backed-off conditions. In both cases, the modelled data show good agreement with experimental data.

$$i_D(t) = a(t) \cdot \left[1 - \left(1 - v_{DS}(t)\right)^{\mathrm{N}}\right] \tag{7.1}$$

The equation governing the model was given in (7.1), it shows the function of time varying drain current i_D *as* the function of V_{DS}, baseline current *a*(t) and the parameter *N*. This parameter defines a profile of the knee for the given active device, with the values of $N = 4$ and $N = 6$ being typical for GaN HEMT devices.

Two active devices fabricated using 250 nm GaN HEMT technology, 6x80 µm and 6x130 µm, were used to verify the modelling work presented in this chapter. Figure 7.1 shows a set of waveforms, referred to as a "fan diagram" [2], representing a measured load-line when the active device was presented with a real load in the range of 10 Ω to 400 Ω while the device was driven into saturation, with corresponding saturation output power P_{SAT}. The captured waveforms were de-embedded to account for the output parasitic capacitance C_{DS}. The static value of 0.25 pF for smaller 6x80 µm device, was determined from the initial load-pull measurements, and was used in the de-embedding process for the subsequent measurements. This figure also contains plots of the modelled knee response from (7.1) for values of N =4,6 and 8. The value of maximum drain current I_{MAX} = 0.41 was extracted from fan diagram on this plot, and th value of $N = 8$ provided the best fit for this device. The process was repeated for the larger, 6x130 µm GaN HEMT from Qorvo. The

measured fan diagram (de-embedded using C_{DS} = 0.4 pF) was shown in Figure 7.2 along with the plot showing a modelled knee response from equation (7.1) for the maximum drain current I_{MAX} = 0.7 mA with N = 4 and 6, the former provided the best fit with the measured data.

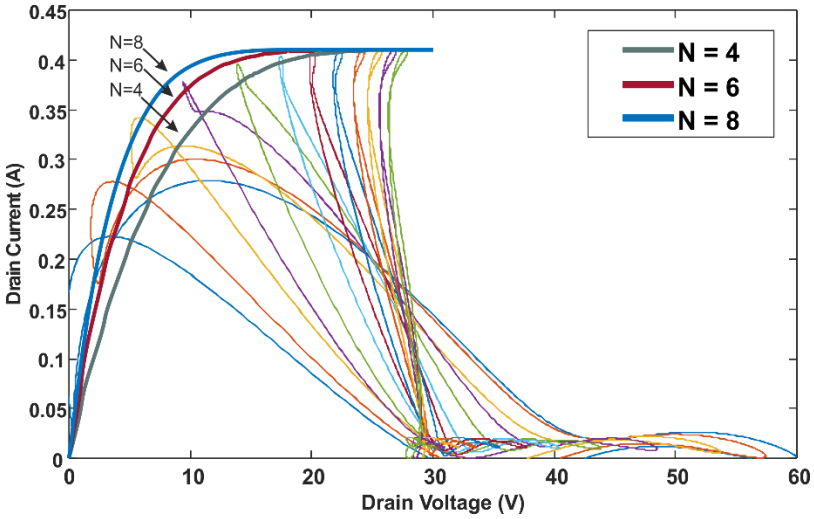

Figure 7.1 – Fan diag 6x80 µm

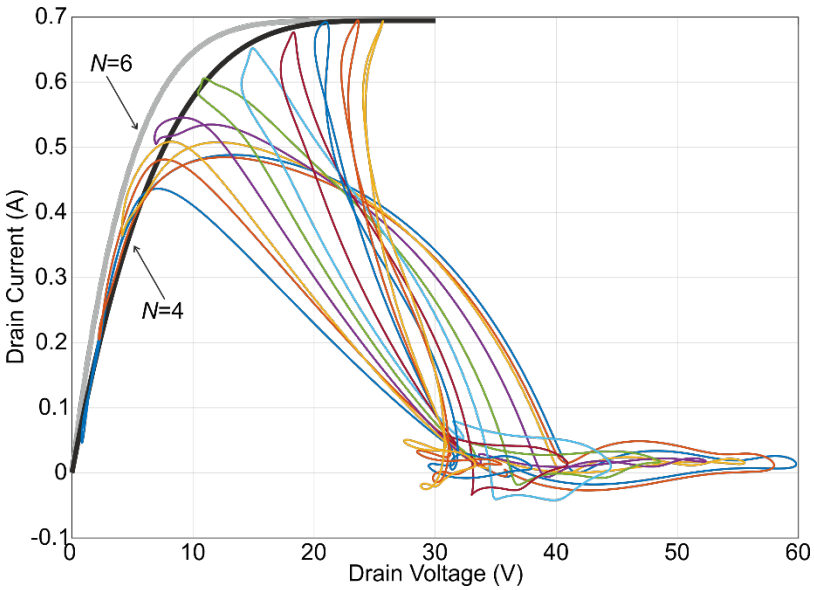

Figure 7.2 - Fan diagram of 6x130 µm

Both experiments described in this chapter assume an active device operating in a class-B mode, at 900 MHz, with 28 V DC drain supply. Therefore, the knee shaping function $a(t)$ from (7.1) was defined as shown in (7.2), to resemble a

truncated sinewave characteristic to this PA class, where the conduction angle θ = π. This is a general equation that applies to both experiments described in this chapter, however, the reduced drain current I_α is only used in section 7.3, while it is initially assumed as $I_\alpha = I_{MAX}$ for experiment in section 7.2.

$$a(t) = \begin{cases} \frac{I_\alpha}{I_{MAX}} \sin\theta & 0 < \theta < \pi \\ 0 & \pi \leq \theta \leq 2\pi \end{cases} \tag{7.2}$$

7.2 Power and efficiency continuous modes in saturated GaN HEMT devices

One of the fundamental assumptions in outphasing circuit is that active devices operate in saturated mode. To exploit benefits of continuous modes such as continuum of class B (class J) in outphasing PA, it was necessary to validate such PA mode when the active device is operating in saturation. The original derivation of class B-J presented in [1] assumes active device operating in its linear region with the "zero-grazing" condition where the swing of an output voltage can be approximated to 0 V at its minimum. This assumption limits a clipping of the current waveform and defines the continuum itself. However, when driving the device deeper into compression, some assumptions on the ideal device can no longer be sustained and require further ad-hoc modelling [3]. For example, in devices with a smooth knee behaviour, such as GaN devices, the optimum loads for maximum power and efficiency are quite far apart, with the optimum for efficiency around twice the optimum for power [4], [5]. Moreover, while for linear operation it is enough to substitute the "zero-grazing" condition with a knee-grazing condition, in saturation this approximation does not make sense anymore, since the knee can be explored down to 0 V, or lower [5] .

In this section it is shown that a continuous behaviour can also be observed in saturated devices without imposing any limitation on clipping. Simulations using a described earlier simplified N-model for the device and source-load pull experimental characterisation are critically analysed and compared to describe the discovered continuum.

7.2.1 Theory and numerical modelling

For an ideal device with drain bias voltage V_{DD} and maximum current I_{MAX}, biased in class B with shorted harmonic terminations, the optimum load is $R_{OPT} = 2V_{DD}/I_{MAX}$ for both maximum power and efficiency. This result assumes a half

sinusoidal current waveform and no knee effect, and leads to an output power of P_{MAX} = 0:25$V_{DD}I_{MAX}$ and efficiency η_{MAX} = π/4 [6]. For the same drain current waveforms, the continuous modes are defined as the voltage waveforms whose minimums graze zero and that lead to the same P_{MAX} and η_{MAX} . Having defined a constant current waveform and a continuum of voltage waveforms, it is possible to derive the harmonic impedance continuum by dividing the voltage Fourier components by the current components. This leads to the well-known definition of the class B- class J continuum in terms of fundamental and second harmonic loads Z_1 and Z_2:

$$\begin{cases} Z_1 = R_{\mathrm{OPT}}\,(1 - j\beta) \\ Z_2 = R_{\mathrm{OPT}}\,j\,\dfrac{3}{8}\,\pi\,\beta \end{cases} \tag{7.3}$$

where β is a real free parameter with limitation |β| ≤ 1. This result has been widely adopted and can enable high-efficiency broadband design in linear power amplifiers.

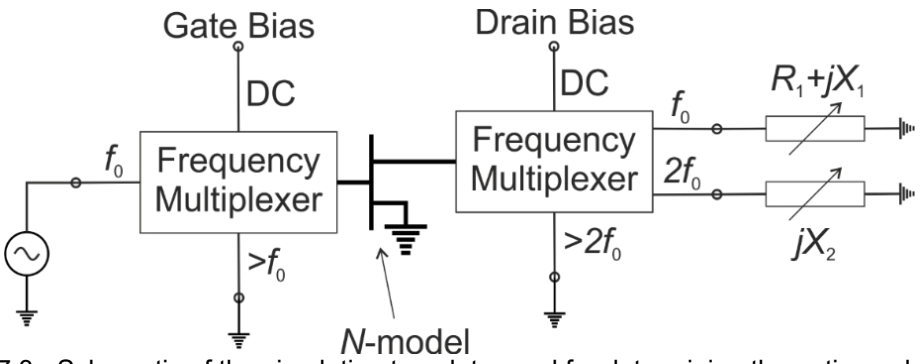

Figure 7.3 - Schematic of the simulation template used for determining the optimum loads for maximum power and efficiency with the *N* model.

Setting the second harmonic to an arbitrary reactance makes the analysis very complicated, so in this work, the model is implemented in a simulator to study the continuum. A symbolically defined device component is used in the Advanced Design System (ADS) to implement (7.1) and simulate the simplified device in a load-pull

template. In particular, the fundamental load is swept on a grid inside the Smith Chart, while the second harmonic load is swept on the border of the Smith Chart. Source harmonic terminations are all short-circuited. Schematic of the simulation setup was shown in Figure 7.3 shows, while the position of the simulated optimum fundamental impedance for maximum power and efficiency (Z_{1P}, Z_{1E}) at different second harmonic loads Z_2 for $N = 4$, $N = 6$, and $N = 8$ were shown on a Smitch chart presented in in Figure 7.4. The Smith Chart is normalised at R_{OPT}, ie. the optimum intrinsic load for each device.

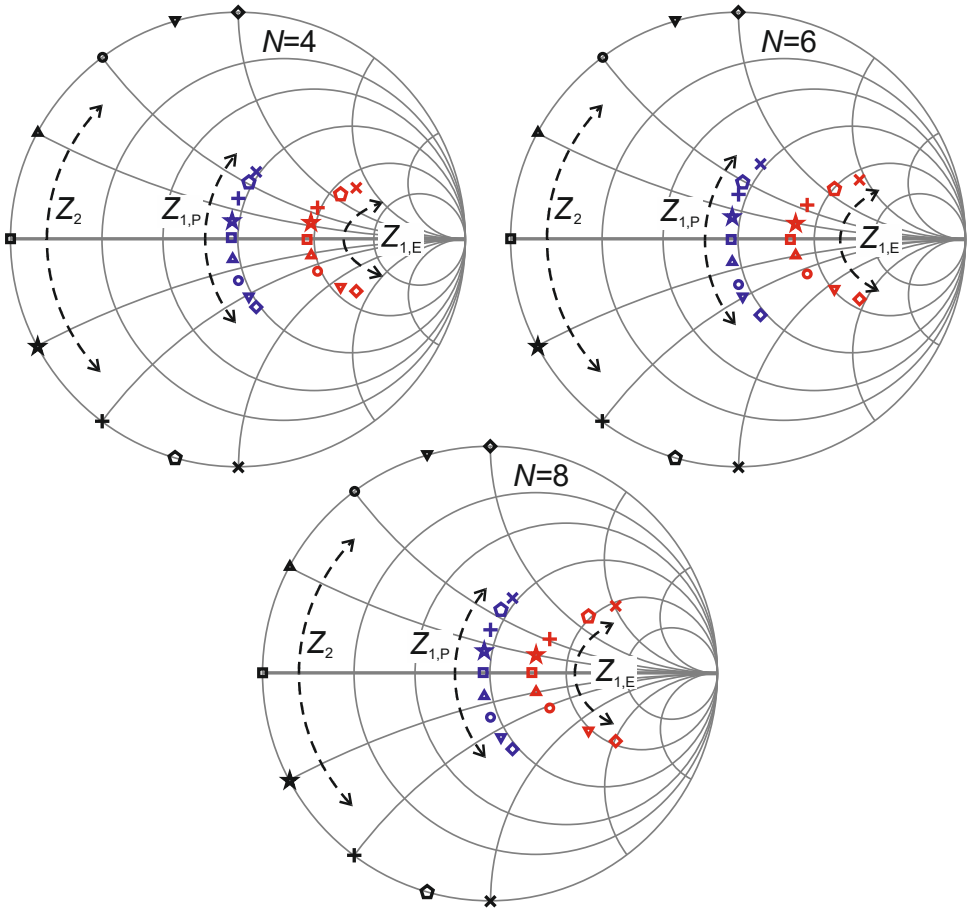

Figure 7.4 - Simulated optimum fundamental and second harmonic loads for N = 4, 6 and 8.

The first important result is that a continuum can be observed and that it has a similar trend compared to the original continuous modes. In fact, for increasing second harmonic reactance, the optimum fundamental loads have an increasing

reactance with opposite sign [6]. The optimum for output power maintains a relatively constant real part, while the optimum for efficiency has a larger distortion and tends to increase for larger $|Z_2|$. The second important thing to notice is that N has quite a visible impact on the position of the optimum impedance, especially for efficiency. For this emulation, it means that the knee profile is key to shaping the optimum efficiency.

7.2.2 Experimental Verification

To verify that the continuum can be observed experimentally, source/load pull characterisation is adopted to recreate the environment shown Figure 7.3. The description and details about this measurement system were provided in Chapter 6.2.

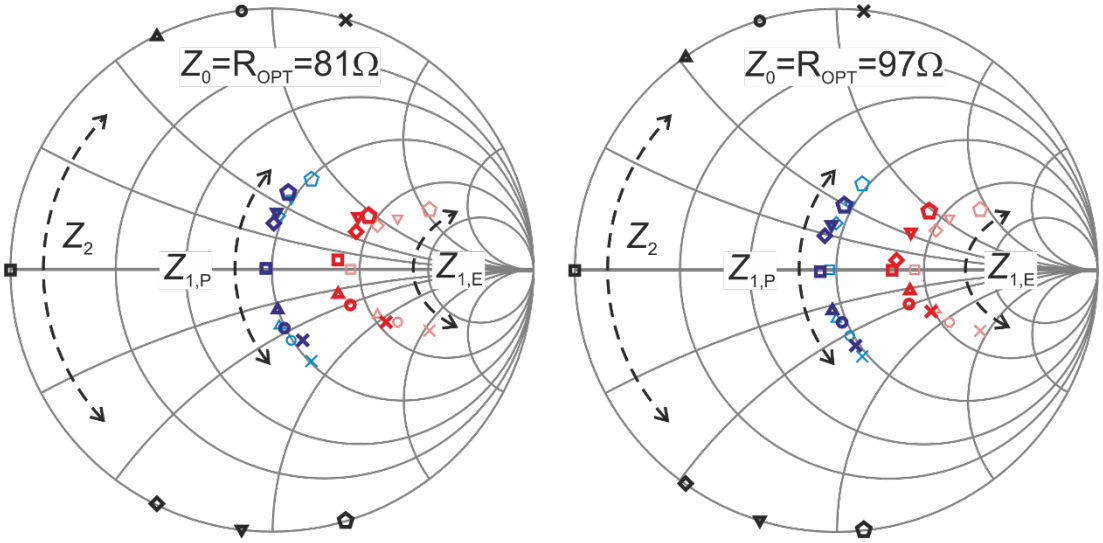

Figure 7.5 - Before realignment.

A first set of measurements was used to identify the optimum load for output power and efficiency with shorted harmonics, with a drive power level that saturates the device. The optimum loads are also chosen to estimate the output capacitance in order to de-embed the reference plane – placing it at the intrinsic current generator – for an easier comparison with the N-model results. The search for optimum fundamental loads was then repeated at different Z_2 values. Figure 7.5 shows the resulting optimum loads on both the devices. The Smith Charts refer to the intrinsic

generator plane and are normalised to $R_{OPT} = 2V_{DD}/I_{MAX}$, with the I_{MAX} determined from the fan-diagrams described in the previous section. On initial inspection, the optimum power impedance continuum is clearly present, and agrees well with the predictions for both devices. The main difference with the simulations is the extension of the imaginary components of the impedance continuum. An explanation for this can be found in the device drain current baseline that is not an ideal truncated sinewave. In fact, the ratio between second and fundamental Fourier components of drain current for negligible knee interaction is approximately ≈ 0.31, while it is ≈ 0.42 in the ideal case. This means that the imaginary part of the second harmonic voltage in the real device is, at the same second harmonic impedance, lower than expected, leading to a lower fundamental imaginary part needed to compensate.

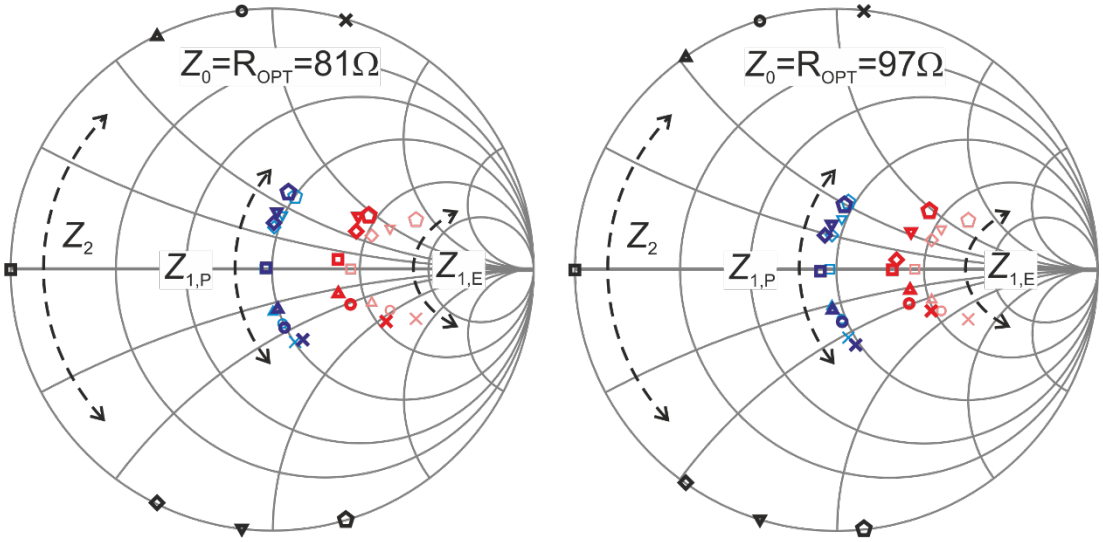

Figure 7.6 - After realignment.

Figure 7.6 shows the same measured optimum loads, but this time compared with the simulated ones whose imaginary part of the impedance has been scaled by a factor 0.31/0.42. This is a very rough approximation, since the scaling of the second harmonic current in the baseline function does not guarantee the same scaling in the total current once it has seen through the non-linear knee-function. Nevertheless, it has yielded a rather accurate adjustment of the simulated optimum impedances for

output power. Conversely, the optimum efficiency impedances are predicted less accurately, however, a continuum can still be clearly observed. This is also true when applying scaling to the imaginary impedance components. This can be attributed to a stronger interaction with the knee in this higher impedance region that decreases the accuracy of the linear scaling applied.

7.2.3 Conclusions

The continuum of maximum power and maximum efficiency fundamental loads for a saturated GaN device has been predicted, using a simplified knee-model, and verified through measurements for the first time. The proposed model shows good accuracy when predicting the optimum power loads, with the accuracy further improved by a linear scaling deducible from the drain current Fourier components. The trend of the optimum efficiency loads is also indicated by simulations, while the prediction of the exact loads is less accurate and requires further analysis.

7.3 Prediction and Experimental Characterisation of Efficiency Contours for GaN HEMTs in Power Back-Off Conditions

Research on modelling active devices focuses primarily on devices working in or close to its saturation mode. Work showing efficiency for devices operating in OBO conditions is somewhat less available in the literature. An example of such work can be found in [4], where authors estimate power and efficiency contours using their active device model and verify their work using an LDMOS device (a 250 W input and output pre-matched Si LDMOS from Freescale Semiconductor). This work presents the method to determine constant efficiency contours using a more accurate, although still very simple, device approximation. Verification is done using GaN active device but can be expanded for other technologies such as GaAs or LDMOS.

Experimental characterisation using a source-/load-pull setup, described in Chapter 6, is used to extract the limited number of parameters needed for the simplified model and to verify the predicted contours. The modelled data shows good agreement with experimental data. This method can help designers in selecting the appropriate load modulation trajectories and the corresponding drive levels of the transistors to optimise the design of load modulated power amplifiers.

The simplified knee model described earlier in 7.1 was shown to accurately predict the optimum power and efficiency contours for the saturated GaN devices [5]. This work utilises the same numerical model to describe the knee behaviour of the active device. The model is used to explore efficiency contours for GaN devices operating in a backed-off condition. The modelled data shows good agreement with experimental data. Constant efficiency contours are observed to move along the real axis on a smith chart as expected, as the value optimum intrinsic load impedance increases when the power output is reduced. It is also observed and shown in this paper, that these contours follow a constant Q line on a smith chart. This is a very

important (a crucial) observation as it simplifies prediction of contours at each output power level, while the optimum load impedance can be deducted from the load line.

Expressing the fundamental voltage and current in the phasor form (7.4) as it was shown in [5] allows simulation of arbitrary loads presented to the active device, by sweeping variables (V,ϕ) and evaluating key parameters from (7.5)-(7.7). The numerical operations used to derive power and efficiency contours were performed in MATLAB software.

$$V_{\mathrm{DS}} = V\big(-cos(\phi) + jsin(\phi)\big),\cdot I_{DS} = I_{1R} + jI_{1Q} \tag{7.4}$$

$$P_{\mathrm{OUT}}(\mathrm{V},\phi) = 0.5 \cdot \Re(V_{\mathrm{DS}} \cdot I_{\mathrm{DS}}^{*}). \tag{7.5}$$

$$Z_1(\mathrm{V},\phi) = \frac{V_{\mathrm{DS}}}{I_{\mathrm{DS}}} \tag{7.6}$$

$$\eta(\mathrm{V},\phi) = \frac{P_{\mathrm{OUT}}}{I_{\mathrm{DC}}} \times 100. \tag{7.7}$$

7.3.1 Theory and numerical verification

Generic 6x80 μm GaN HEMT die transistor from Qorvo, biased in a deep class AB, with 28 V drain supply and operating at 900 MHz, was used for experimental verification. The Source/Load-Pull, described in Chapter 6, was used for characterising and measuring the power and efficiency of the active device. The third harmonic was presented with an open circuit at the output, while the second harmonic was presented with short circuit to ensure that the impedance for maximum efficiency contours was centred on the real axis of a Smith chart. The relevance of a phase of second harmonic and its relation to the efficiency of a PA was shown in [1]. Source pull of the second harmonic was employed to present the second harmonic with a short circuit at the input.

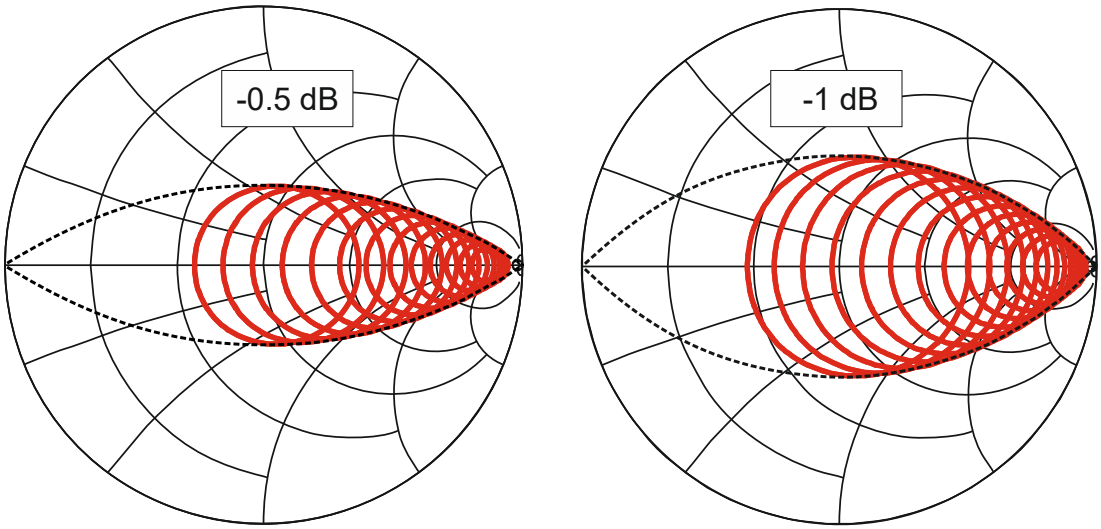

Figure 7.7 - Modelled efficiency contours for output power levels decreasing from saturation to -20 dB, in 2 dB steps for device with a knee profile characterised by N = 6. Smith chart is normalised to intrinsic load which provides the maximum efficiency when device is operating in saturated mode.

The maximum drain current I_{MAX} was measured and determined as 0.41 A, hence the optimum intrinsic load R_{OPT} = 137 Ω. This value was also verified in a load-pull measurement and shown on a Smith chart presented in Figure 7.8. With known maximum current I_{MAX} (7.1) could be solved for various N values, with N = 8 providing the best fit to describe the knee profile characteristic to this device.

After the output power saturation point was established, the maximum drain current was noted, and the input drive power was gradually reduced. Each iteration involved performing a load-pull sweep to determine efficiency, which was followed by capturing a fan diagram. The later was required to determine the output drain current and its ratio to $I_{MAX,}$ so the OBO level could be calculated in a similar fashion as in the previous section of this section.

While the authors of work in [5] shown that their model predicts the power and efficiency for a saturated active device, this work focuses on determining efficiency for an active device operating in OBO condition. Smith charts presented in Figure 7.9 show a set of efficiency contours, in -0.5 dB step for the active device operating in saturation and in -2.36 dB OBO. In both cases, the efficiency predicted by the numerical model (7.1) is in good agreement with the measurements.

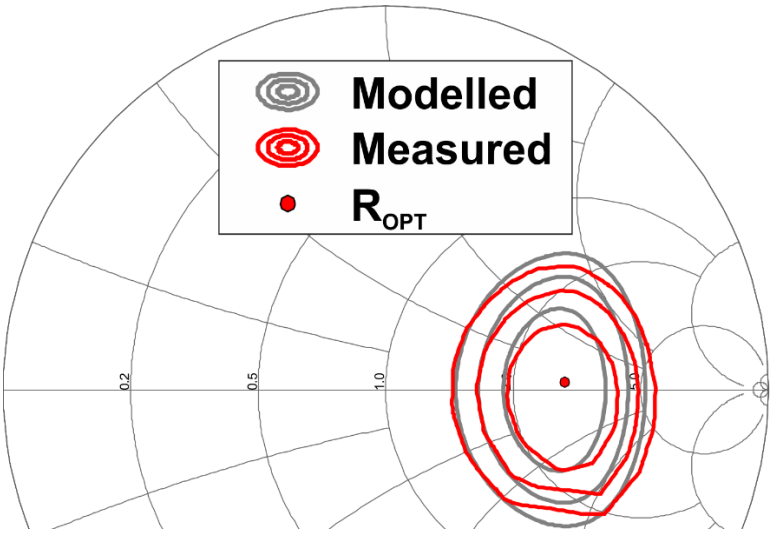

Figure 7.8 - Measured and modelled contours of constant delivered power, in steps of 0.5 dB, for the active device operating in saturation mode, thus producing output current I_{MAX}. Optimum intrinsic load for this device R_{OPT} = 137 Ω is shown and used in subsequent modelling of efficiency contours.

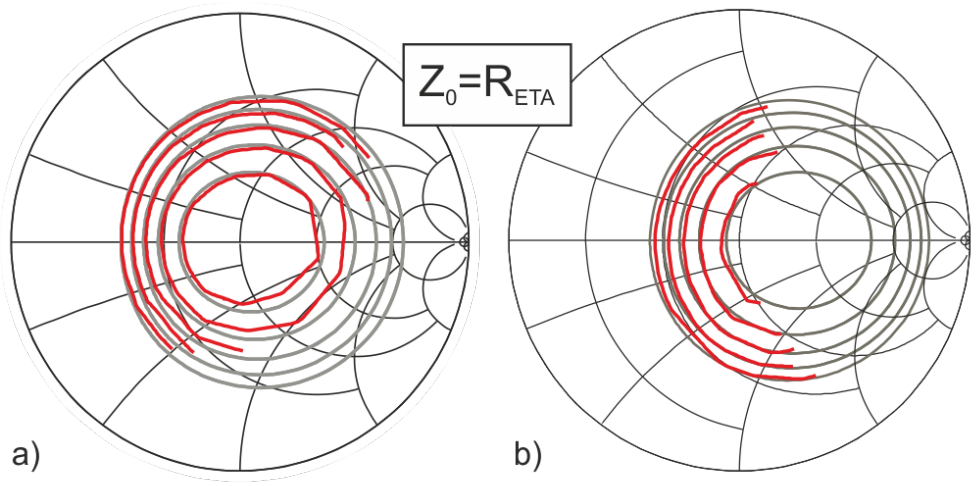

Figure 7.9 - Measured efficiency contours showing a good agreement with the model described in this chapter. Contour levels in (a) and (b) are decreasing in 0.5 dB steps, for the device operating in saturation (a) and -2.36 dB OBO (b).

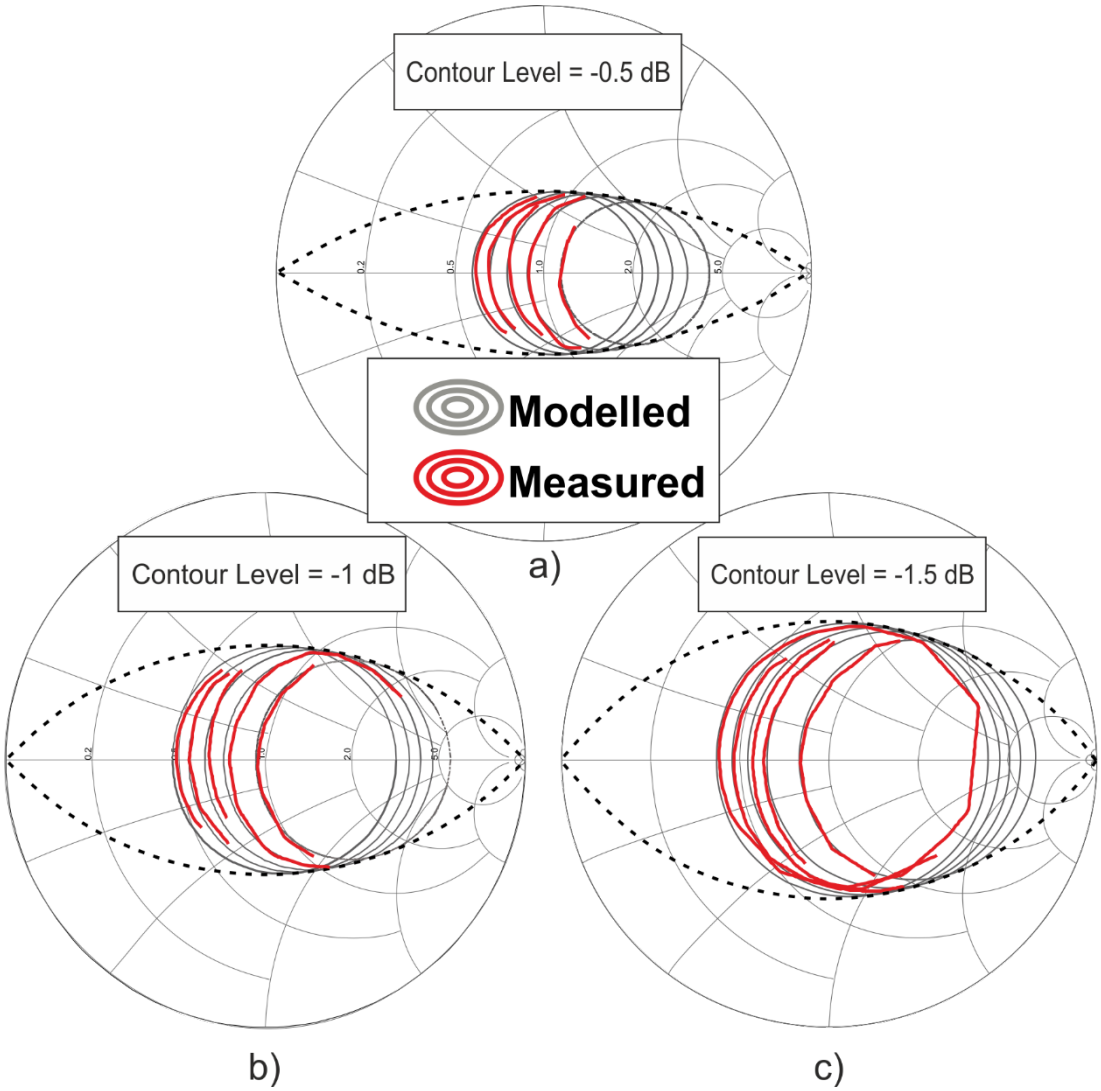

Figure 7.10 - Measured efficiency and modelled efficiency contours in (a), (b) and (c) shown for OBO levels: 0, -1.2, -2.36, -3.7 and -5.85 dB. Contour levels: (c) -0.5 dB, enclosed by Q = 0.68 (d) -1 dB, enclosed by Q = 1.05 and (e) -1.5 dB, enclosed by Q = 1.41. Smith chart was normalised to intrinsic load which provides the maximum efficiency when device is operating in saturated

7.3.2 Conclusions

For the saturated device, the optimum load impedance for efficiency was modelled and measured to be R_{ETA} = 210 Ω. All Smith charts presented in this document were normalised to this value. The measured efficiency contours of levels: -1.5, -1 and - 0.5 dB, were presented in Figure 7.10, and show good agreement with modelled results. These contours are enclosed by a constant Q line: 0.68, 1.05 and 1.41 for each plot respectively. Five OBO levels were measured and modelled: 0 (saturated output), -1.2, -2.36, -3.7 and -5.86 dB.

This section presented a simplified method of predicting efficiency contours for GaN HEMT transistors, using a simplified numerical model to characterise knee behaviour of an active device. Predicted contours were verified experimentally using Source/Load-Pull system and show good agreement with modelled data. Moreover, it was demonstrated that the contours are enclosed by a constant Q line on a Smith Chart and can be accurately predicted from a load line. This work provides further insight and requirements for PA designs utilising a load modulation technique, such as Chireix Outphasing. This method can be used to further refine the load impedance values required to be presented to an active device to achieve high efficiency figures for large OBO levels. The work can be extended to show that the same numerical model can be used to model output power contours for OBO conditions.

Constant efficiency contours are observed to move along the real axis on a smith chart as expected, as the value optimum intrinsic load impedance increases when the power output is reduced. It is also observed and shown in this paper, that these contours follow a constant Q line on a smith chart. This is a very important observation as it simplifies prediction of contours at each output power level, while the optimum load impedance can be deducted from the load line.

7.4 References

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CHAPTER 8

CONCLUSIONS

8.1 Summary of work done and achievements

The work presented in this thesis has focused on exploring and adapting the original outphasing concept, originally proposed by Chireix in 1935, to the needs of modern telecommunication standards and systems. The primary objective was to extend the bandwidth of the inherently narrowband concept, and this was achieved by employing a broadband planar balun as the power combiner element. The balun itself constitutes a state-of-the-art and was fabricated using a novel solution, not reported elsewhere in the literature.

Several key assumptions in the analysis of the outphasing concept were challenged and addressed, specifically the fact that the active devices need to be approximated as voltage sources when operated in saturation. This somewhat intuitive assumption, which greatly simplifies numerical analysis of the outphasing circuit, was shown to be invalid in the case of active devices, which are typically modelled as current sources. In this work, it was demonstrated that although a saturated device will exhibit properties of a voltage source, the limited nature of output current it can supply invalidates the assumption. Analysis of the outphasing theory, where the active devices are correctly modelled as current sources, led to the formulation of the CMOP concept. The main objective identified in Chapter 1, improving the bandwidth of outphasing circuits, has been accomplished and demonstrated. In fact, the demonstrator PA achieved the largest fractional bandwidth achieved in an outphasing PA that has been reported in literature. Chapter 5 has been

dedicated to explaining this vital concept, concluding with the demonstration of this novel solution using an MMIC PA fabricated in 0.25 μm GaN technology. The areas of improvement and possible further research opportunities are outlined in the next section.

All the power amplifiers that have been designed, fabricated, and reported in this thesis have been characterized and measured using the system that was conceived and assembled as a part of this research. The phase-coherent system, for dual input PA topology, was based on MG3710A dual output RF signal generator from Anritsu. Two phase-coherent carrier signals with frequency of up to 6 GHz can be generated, with the internal baseband generator capable of handling modulated signals with bandwidths up to 160 MHz. The instrument control, signal processing and data acquisition were implemented in Matlab.

8.2 Future Directions

8.2.1 Characterization of the mm-wave CMOP MMIC

Another circuit was designed and fabricated for operation at mm-wave frequencies following the successful implementation of CMOP PA operating in sub- 6 GHz frequencies. The MMIC was fabricated in 0.15 µm GaN process, and targets nominal frequency of 28 GHz. Due to the time constraints and limitations arising from the covid lockdowns since early 2020, the characterization was not completed in time for the thesis submission. Further research is warranted by the initial circuit's remarkable performance, particularly the measured bandwidth. The gain observed in CMOP was also significantly greater than the figures reported in the state-of-the-art DPA solutions that operate over similar bandwidth.

8.2.2 Expansion of the characterisation system

The measurement system, described in Chapter 6, was developed as a part of this research and proved its characterization capabilities when operated with CW signals. Although the system was used with LTE signals and DPD for another project not related to this thesis, further work is needed to create a solution for constructing a *mixed-mode* signal for outphasing circuits. Currently, the system is limited to 6 GHz, which is the upper limit of the signal generator. As the mm-wave frequencies are becoming more available and attract significant research interest, expanding the capabilities of the characterization system to operate at these frequencies can be identified as a viable option.

8.2.3 Investigation of linearity in CMOP PA

The linearity of CMOP is another interesting subject worth investigation with scrutiny. Once the *mixed-mode* outphasing is implemented for the dual input characterization system, the drive input strategies described in Chapter 5 can be implemented and assessed with the demonstrator PA. Although outphasing has a

reputation for introducing a great deal of distortion (see Chapter 3), the CMOP operates in a linear region of its active devices and strong output voltage clipping is prevented by applying input drive schemes proposed in this work. Having the advantage of complete control over input signal at the DSP level in Matlab, opens an opportunity for signal pre-distortion tailored specifically for CMOP.