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Controlled Fault-Tolerant Power Converters for Power Quality Enhancement

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***Abstract*—Power quality depends generally on the interaction of electrical power with electrical equipments. If electrical equipments operate correctly and reliably without being damaged or stressed, a suitable level of power quality is assured. On the other hand, if the electrical equipment malfunctions, is unreliable, or is damaged during normal usage, power quality is poor and probably the economical loss could be important like the technical one.**
In the scenario of the Distributed Generation, power quality issues will be moreover important because an higher dissemination of power conditioning equipment will be requested and this obviously increases the sources of vulnerability of the electrical system.
In this paper fault tolerant power converters are considered as a viable solution of power quality problems and a suitable control algorithm of them is presented. The control proposed in the paper is based on the model of the power converter reformulated in terms of healthy leg binary variable and the paper shows how this control is able to save the aspect of power quality when the converter works in the linear range. The effectiveness of such an algorithm and of the fault tolerant power converters are finally verified by means of simulations.

Keywords-fuel cells, hybrid power systems, power system control, power supplies

I. INTRODUCTION

In today's market, electrical energy is to be granted for the most part of applications. The growing use of microprocessors in appliances, office equipment and process controls has made all the operators aware of the power quality demands over the unpredictability of its supply.

Power quality issues can be divided into short and long duration, but all of them are equally important. Equipment and machinery can be damaged or even fail when subjected to power anomalies. One or two seconds of outage or a surge can bring "business applications" down for hours or days. Spikes, surges, brownouts and other power issues are potential problems to be fully taken into account.

These problems can be compounded by starting, running and stopping large machinery and other business-critical systems[1].If electrical equipments and plants are more than 15 years old, they probably are not designed to meet the demands of today's high power equipment. The systems supporting any organization's key functions with electrical energy may overload wires causing power problems and failures that can harm valuable data and equipment. A synthesis of all these problems and issue is illustrated in the report [2].

A different solution is the conceptions of systems, devices and equipments able to continue their operation even in the case of a fault occurrence with a sufficient degree of power quality savings. The architectures able to realize this concept are called fault-tolerant.

Since a decade, in power electronics, fault tolerant architectures have been introduced and developed gaining a growing attention in the research and industry applications for their reduced costs and low enhancements in complication of their control algorithms.

The technical literature on fault-tolerant converters is to be considered rich but not exhaustive because the research fields are still up and running and open questions are waiting to find suitable answers [3-17]. Among the various aspects investigated, the most frequently discussed are issued to control problems [6,7][15,16], fault diagnosis and protection issues [3,8][10-12], topologies, reconfiguration of circuits and controls, effect of the fault tolerant operations on the main network [10] and on the loads in "mission critical" tasks with a special reference to evaluation of performance in A.C. electrical drive [3-6][9]. Several fault identification techniques were introduced in the past essentially based on the analysis of the current-vector trajectory to identify fault modes, on the determination of the fault condition from the instantaneous frequency of the current vector and finally on the comparison between the measured voltages and the estimated ones via the model of the healthy inverter [13].

This paper introduces a control strategy suitable for fault tolerant operation of static power converters used in different applications. This control is suggested from the mathematical model of the converter formulated in terms of "healthy leg binary variables". Such new variables allow, in numerical simulations, both the management of the unfaulted and faulted conditions.

The fault-tolerant converter control is also based on the assumption that the converter is able to provide a symmetrical voltage system even in fault-tolerant mode. By requiring that the inverse symmetrical component of reference voltages is null, it is possible to create new reference signals to apply for the modulation of the two healthy legs. The choice of reference voltages with a null inverse sequence allows to achieve a minimum loss in power

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quality and also limits the current distortion when the converter operates within the linear region. In the over-modulation range an increase of the current distortion, and only a limited increase in the electrical unbalance, will manifest.

The proposed control is verified through numerical simulations with the aim to confirm its effectiveness. With a slight change in the phase of the new reference voltage system the control can be applied both when the converter draws energy from the grid or when it delivers energy to a passive load.

II. FAULTS OCCURRENCE AND THEIR MANAGEMENT IN FAULT TOLERANT CONVERTERS

The reliability of the modern power converters has limited the probability of faults occurrence, even more for those localized on the single power devices. Actually the most frequent faults are represented by short circuit and permanent switching off of a single device. Among these two faults the second appears more often. On the other side, electronic power devices are protected by series connected fast fuses so that the short circuit condition quickly evolves to the open line condition [3].

Taking the intervention modes and the converter topologies into account, the fault tolerant converter may be divided into two big families:

- the redundant converters;
- the non redundant converters.

The first ones are characterized by the presence of some additional not switching devices during normal operation and used as back-up units in the case of a fault occurrence with the loss of a converter leg. The ratings of the additional devices are practically the same of the main devices because they must be able to ensure the "normal operation" of the converter with the same voltage and current values.

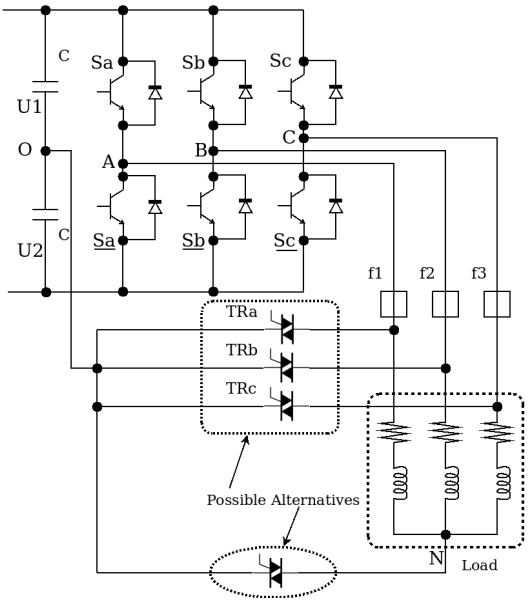

Figure 1. Topology of non redundant Fault tolerant converter.

Fig. 1 shows a non redundant fault tolerant converter on which this paper is focused. In this case the additional components are only the triacs connecting each phase of the load, after the protecting fuses, at the middle point of the DC Link. The switching of such a triac guarantees the enclosure of the current path both in the case of the fault of a silicon device and in the case of a phase interruption before the load. Note that the non redundant converter topology is similar to that of a B4 converter with DC link capacitor splitting. However the B4 converter is not intended to be a fault tolerant converter [14,17].

The fault on a single device reduces of two units the number of the possible conduction states, but in spite of this it is still possible to follow the voltage reference with a suitable precision even if the normal linear range of the converters is reduced. In the case when the voltage asymmetry margins are narrow the usage of passive symmetrizing cells must be taken into account too.

III. A SUITABLE CONTROL FOR FAULT-TOLERANT CONVERTERS

In a previous paper the authors considered the aspect of power quality in micro-grid management for faults occurrence, diagnosis and control of all the components [10]. In this paper the attention is focused on the particular aspect of fault-tolerant control specifically for the converters.

In order to introduce a suitable control for fault-tolerant converters employed in micro-grid two cases must be taken into account:

1. the converter draws energy from the network and releases it to a symmetrical passive or active load (i.e. an A.C. electrical drive). In this case the performance in load management is of primary importance (e.g. for electrical drives continuity and performance in terms of low degradation of the torque profile are mandatory);
2. the converter injects generated energy into the grid. In this case the control must take into account the problem of frequency and voltage regulation and the capital problem of output synchronization to the network.

In each case the suitable control for fault-tolerant converters examined in this paper can be suggested and better understood recalling the mathematical model of the fault-tolerant converter in a form conceived and set-up by the Authors. In this model the "healthy leg binary variable" defined as:

$$\begin{aligned} h_k &= 1 \quad \text{if } k-th \text{ phase is healthy} \\ h_k &= 0 \quad \text{otherwise} \end{aligned} \tag{1}$$

are introduced. With this definition the model consists of two set of equations, one for output voltage and one for DC link:

$$v_{kN} = U_{DC} T H_k S_k + T(I - H_k) \mathbf{I} U_2 \tag{2}$$

and

$$U_1 = \frac{1}{C}\int_0^t (i_0 - S_k^t H_k^t i_k)dt$$
$$U_2 = \frac{1}{C}\int_0^t (i_0 - [S_k^t H_k^t - \mathbf{1}^t (I - H_k)]i_k)dt \quad (3)$$

where:

$$H_k = \begin{pmatrix} h_A & 0 & 0 \\ 0 & h_B & 0 \\ 0 & 0 & h_C \end{pmatrix} \quad (4)$$

U_{DC} is the whole capacitor bank voltage;

U_1, U_2 are the partial capacitor voltage;

i_0 is the DC side input current, before the capacitor bank, of the converter

C is the value of the single capacitor;

I is the diagonal eye matrix

$\mathbf{1}$ is the vector whose elements are ones $[111]^t$

v_k is the vector of the converter output voltages;

i_k is the vector of the load currents;

S_k is the vector of the switching functions;

T is the topological matrix of the converter:

$$T = \frac{1}{3}\begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix} \quad (5)$$

With these positions, eqs (2)-(5) describe completely the behavior of a fault tolerant converter, even in the healthy condition with a double set of equations considering also the transient evolution, in particular for the phenomenon of DC link voltage imbalance during fault-tolerant mode. The advantage of the healthy leg binary variable is evident and can be further confirmed in the definition of a suitable control strategy for fault tolerant converter.

If a fault in the converter power device occurs, an entire leg of the same converter is loosen. This implies that, even if in the non redundant topology the faulted phase is reconnected to the middle point of the DC link capacitor bank, the classical sinusoidal control is not able to guarantee the symmetry in voltage and current. In particular the current of the faulted phase is reduced of a factor $\sqrt{3}$.

Such a symmetry may instead be achieved if a different set of reference voltages is synthesized and used for Pulse-Width-Modulation purpose. The different set of reference should guarantee a symmetrical system of output voltages and currents. This is important in both the cases when the converter is connected to the network and when it is connected to a load that requires a minimal degree of power quality loss. In the case of an electrical A.C. drive the maintenance of a symmetrical set of currents implies that the torque profile is not too much degraded and so that the mechanical performance of the drive can be considered fully acceptable. By the other hand if the converter is connected to the A.C. side of grid, the converter capability to maintain a set of symmetrical voltages save the aspect of power quality because only small disturbances are propagated in the mains without the need to use expensive solutions for their mitigation. The set of voltage references in the fault-tolerant mode should have, for this reasons, a minimal inverse component. The presence of a zero sequence component does not affect converter output because of its topology when the load is symmetrical. In the case of a phase fault the voltage references consist of a set of two sinusoidal signals destined to the control of the healthy legs. To fix the ideas suppose that the signals phasor are:

$$U_{ref1} = U_x e^{j0}$$
$$U_{ref2} = U_x e^{-j\varphi} \quad (6)$$

It is not important the real argument of the phasors, but the displacement angle between them.

For the three fault cases, on phases A,B, and C respectively, the inverse component of this reference system is:

$$U_{invA} = 0 + \alpha U_{ref1} + \alpha^2 U_{ref2}$$
$$U_{invB} = U_{ref1} + \alpha 0 + \alpha^2 U_{ref2} \quad (7)$$
$$U_{invC} = U_{ref1} + \alpha U_{ref2} + \alpha^2 0$$

where

$\alpha = \exp(j2\pi/3)$

Calculating the modules of the inverse components the expression:

$$|U_{inv}| = \sqrt{2}U_x\sqrt{1+\cos\left(\varphi \pm \frac{2\pi}{3}\right)} \quad (8)$$

is obtained (+ is for fault on phase A and C while - is for fault on phase B). In each case the minimum inverse factor is reached for $\varphi \pm \frac{2\pi}{3} = \pi$ i.e. for $\varphi = \frac{\pm\pi}{3}$ (always with + for phase A and C and - for phase B) and it results just $|U_{inv}| = 0$.

Hence, in a faulted converter, when the reference voltages for healthy legs consist of a couple of sinusoidal signals with a 60 degrees phase displacement, then the converter output voltages are a three phase symmetric system and the same is to be said for currents, obviously with a symmetrical load.

By superimposing reference via a closed loop control the new references given by the control system would be of the same type. The general expression of the reference voltages (u_k with $k = A,B,C$) valid for healthy and faulted conditions is:

$$u_A = u_A h_A h_B h_C + \sqrt{3}\left(\underline{h_C} u_B - \underline{h_B} u_C\right)$$
$$u_B = u_B h_A h_B h_C + \sqrt{3}\left(\underline{h_A} u_C - \underline{h_C} u_A\right) \quad (9)$$
$$u_C = u_C h_A h_B h_C + \sqrt{3}\left(\underline{h_B} u_A - \underline{h_A} u_B\right)$$

where $\underline{h_k}$ is the negation of the k_{th} healthy-leg binary variable and u_k is the set of normal symmetrical three phase reference voltages.

Equation (9) may be also written in the more synthetic form:

$$u^* = \lambda u + \sqrt{3}u \wedge \underline{h} \quad (10)$$

that develops the vector notation and where $\lambda = h_A h_B h_C = det(H_k)$.

The modified reference voltages are very simple to be implemented on micro-processor and diagnostic signals on the converters can be used to synthesize the new post fault reference voltages. In (9) the general term λu is the reference for the healthy case while the vectors cross product $\sqrt{3}u \wedge \underline{h}$ is the new reference in the faulted case. The factor $\sqrt{3}$ guarantee the identity of the voltage and current amplitude, even after the fault has occurred. Note that the cross product vector term $\sqrt{3}u \wedge h$ should be 90 degrees clockwise rotated if the converter is connected to a grid containing generators to maintain the synchronization of the converter voltages with the grid ones. In this case the reference voltages system, expressed in vector form, results:

$$u^* = \lambda u + \sqrt{3}(u \wedge h)e^{-j\frac{\pi}{2}} \quad (11)$$

IV. VALIDATION OF THE CONTROL

In order to verify the validity of the proposed control for fault-tolerant converters connected to micro-grids several numerical simulation have been carried out with the help of the MATLAB© - SIMULINK© software package.

Simulation results are illustrated in Figs. 2 to 6 showing how the fault condition is managed by the model with the modified control strategy in order to guarantee the minimal degree of power quality degradation.

Fig. 2 shows the converter phase voltage both at unfaulted (upper) and faulted leg (lower) after the faults occurred: their first harmonics continue to be a symmetrical system even after the fault. The voltage waveforms will be quite different from those with unfaulted converter condition and the faulted leg voltage exhibits the greatest difference. Fig. 3 shows converter phase currents before and after fault occurrence with the instantaneous modification of the converter references. The converter linear range during the fault is, in each case, restricted. Linear range is quite important in order to guarantee the minimal asymmetry for the current system. An over-modulation running should require a further modification of the displacement angle between the reference voltages in order to gain at least a sub optimal symmetry condition.Fig. 4 shows the power degradation manifesting as a greater distortion and unbalance in the load currents if over-modulation occurs (i.e. with an amplitude modulation index higher than 0.5, in the faulted case).

Fig. 5 shows instead the modification of the converter voltages for faulted and unfaulted legs during over-modulation and faulted mode.Fig. 6 shows the voltage imbalance on the two DC Link capacitors.

The simulation results confirm the presence of fluctuations in the capacitor voltages. However, in general, this difference does not affect significantly the entire value of the DC Link voltage and the general converter performance.

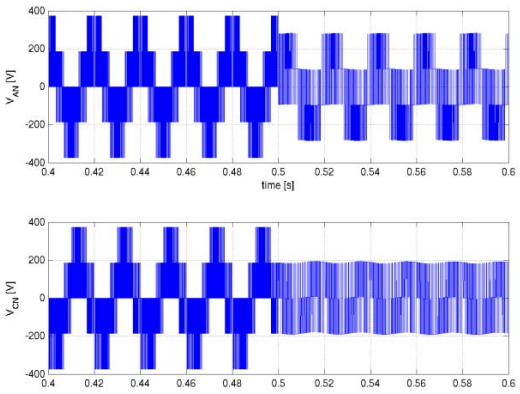

Figure 2. Phase voltages at unfaulted and faulted converter leg.

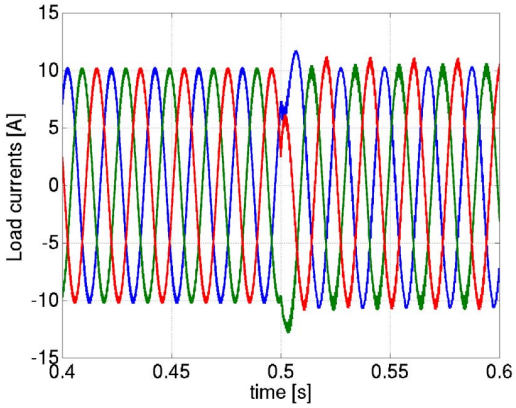

Figure 3. Load Current before and after faults.

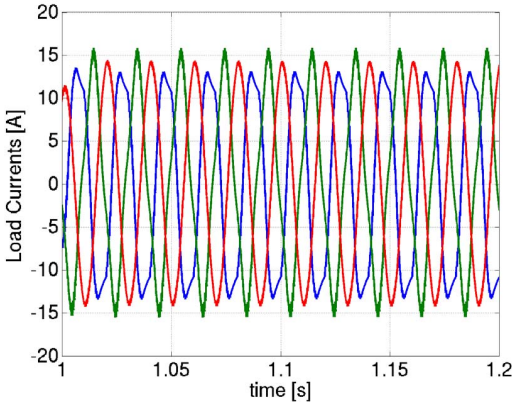

Figure 4. Distorted and unbalanced load currents with higher distortion during faulted condition in over-modulation mode.

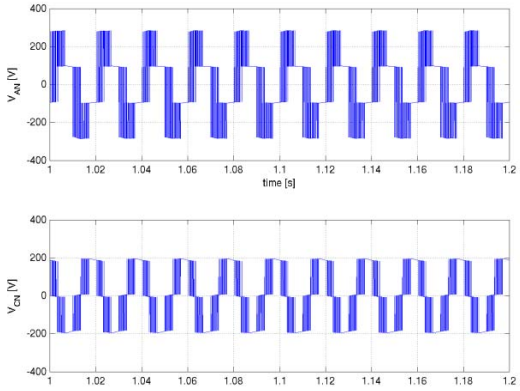

Figure 5. Converter voltages during faulted and over-modulation mode in unfaulted and faulted leg.

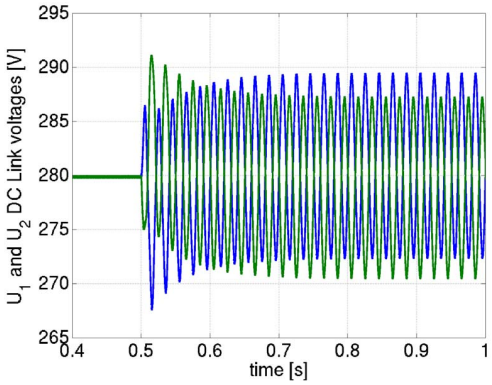

Figure 6. Voltage imbalance through DC Link Capacitors

V. CONCLUSIONS

In this paper fault-tolerant converters have been considered as an interface with grids and load for power quality improvements. Focusing the attention on the non redundant converter topology, a suitable control strategy based on the converter mathematical model was presented, discussed and finally simulated. The converter model introduces the "healthy-leg binary variables", describing the healthy or faulted state of each converter leg. The same healthy-leg binary variables enable the easy implementation of a suitable control based on the assumption that the voltage output of the converter can continue to be a symmetrical system, even after fault occurrence, by modifying the reference voltages. The new reference voltages exhibit a null inverse sequence component and a zero sequence that is directly filtered by the converters in virtue of their topology. Simulation results presented in the paper show the effectiveness of the proposed control strategy evidencing how the converter control can guarantee a minimal degree of power quality degradation.

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REFERENCES

[1] Piegari L., Rizzo R., Tricoli P. "A Comparison between Line-Start Synchronous Machines and Induction Machines in Distributed Generation"PrezgladElektrotechniczny (Electrical Review), ISSN 0033-2097, R. 88 n. 5b/2012, pp. 187-193.

[2] Cerretti A., Botton S., Sartore S. "I problemi del gestore della rete di distribuzione", AEIT Seminario didattico-Medium and small generation: interaction with network and market, Rome, Oct 22-23, 2007.

[3] SalmonJ. C., "Current overload protection features of hybrid inverter drives", Proceedings of the 1992 International Conference on Power Electronics and Motion Control, 1992.

[4] ChatzakisJ., AntonidakisE. "A Novel N+k Fault-tolerant Hot-swap DC/AC Inverter Design" Power Electronics Specialists Conference, 2008. PESC 2008. IEEE, pp. 3291 – 3294.

[5] Jun Li, Alex Q. Huang, Subhashish Bhattacharya, Guojun Tan "Three-Level Active Neutral-Point-Clamped (ANPC) Converter with Fault Tolerant Ability" APEC 2009. 24th Annual IEEE pp. 840 - 845

[6] L. Zhou, K.Smedley "A Fault Tolerant Control System for Hexagram Inverter Motor Drive" APEC, 2010 25thAnnual IEEE pp. 264 – 270.

[7] Brando G., Dannier A., Del Pizzo A., Rizzo R. "Quick identification technique of fault conditions in cascaded H-Bridge multilevel converters" Proc. Aegean Conference on Electrical Machines and Power Electronics ACEMP 2007, Bodrum, Sept. 2007, pp. 491-497.

[8] Karimi S.,Poure P.,Saadate S. "A fault tolerant three-leg shunt active filter using FPGA for fast switch failure detection" PESC 2008. IEEE pp. 3342 – 3347.

[9] Dan Sun,Yikang He "A modified direct torque control for PMSM under inverter fault" Proc. ICEMS 2005, Vol. 3, pp. 2473,2005.

[10] GendusoF., MiceliR., and RiccoGalluzzoG. "Flexible Power Converters for the Fault-Tolerant Operation of Micro Grids" XIX International Conference on Electrical Machines ICEM 2010, Rome (Italy), 6-8 Sept, 2010, pp. 1-6.

[11] Brando G.,Dannier A., Del Pizzo A., Rizzo, R. "A generalized modulation technique for multilevel converters" Intern. Conference on Power Engineering, Energy and Electrical Drives POWERENG 2007, Setubal, 12-14 April 2007.

[12] Del Pizzo A., Spina I., Schäfer U., Beti L.T. "A parameter estimation method for on-line failure detection in permanent magnet AC-brushless motors having current-dependent parameters" 8th IEEE SDEMPED 2011, Bologna Italy; 5-8 Sept. 2011.

[13] De AraujoRibeiro R.L.,Jacobina C.B., da Silva E.R.C., Lima A.M.N. "Fault detection of open-switch damage in voltage-fed PWM motor drive systems" IEEE Trans. on Power Electronics, Vol 18, Issue 2, pp. 587 – 593, March 2008.

[14] BlaabjergF., FreyssonS., HansenH., Hansen S."A New Optimized Space-Vector Modulation Strategy for a Component-Minimized Voltage Source Inverter" IEEE Trans. on Power Electronics, Vol. 12, N. 4, July 1997.

[15] Piegari L., Rizzo R. "A control technique for doubly fed induction generators to solve flicker problems in wind power generation" Proc.of Power and Energy Conference PECon 2006, Malaysia, Nov. 2006, pp. 19-23.

[16] Brando G., Rizzo R. "An optimized algorithm for torque oscillation reduction in DTC-Induction motor drives using 3-Level NPC inverter" Proc. International Symposium on Industrial Electronics ISIE 2004, Ajaccio, May 2004, pp. 1215-1220.

[17] WelchkoB. A., LipoT. A., JahnsT. M., SchulzS. E."Three-Phase AC Motor Drive Topologies: A Comparison of Features,cost and limitation", IEEE Transactions on Power Electronics, Vol. 19, No. 4, July 2004.