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Energy Efficient and Wideband Class-J Doherty Power Amplifier

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***Abstract*—This paper presents a systematic design technique for a wideband GaN HEMT Class-J Doherty amplifier based on the second harmonic tuning. Following a theoretical explore on the expanded design space for a dynamic load modulation, the output matching networks of both Carrier and Peaking amplifiers are synthesized to satisfy the Class-J load requirement. A wideband Class J DPA with a symmetrical architecture is designed as a proof-of-concept to operate over a 1.5 to 3.2 GHz band frequency and delivers 40%-47% power added efficiency.**

Keywords—Doherty Power Amplifier, Class-J PA, Broadband, 5G, High Efficiency.

I. Introduction

Doherty power amplifier (DPA) [1] is well-known to 1.5speed connectivity with high reliability. The dynamic load modulation mechanism for efficiency enhancement in DPA has been performed by an impedance inverter that provides the interaction between Carrier and Peaking PAs. However, in conventional DPA, the impedance inversion is implemented by means of quarter wavelength transmission line, which has a frequency-dependent electrical length and results in a narrowband behavior of DPA. Meanwhile, the broadband modulation bandwidth of 5G transmitters strongly imposes huge burden on RF circuit design for ultra-wideband power amplifiers. In response to this demand, a great number of bandwidth extension techniques have been proposed for DPA, including reduction of the impedance transformation ratio [2], two-section peaking network [3], network based on branch-line coupler [4], frequency response optimization [5] and parasitic compensation technique [6]. Most of these works are focused on the practical limitations of conventional DPA attributed to the imperfections of its building blocks.

In the conventional Doherty PA, the load impedance is set to $2R_{opt}$, when the peaking PA is off and, it transforms to $R_{opt}/2$ at the carrier output node through the impedance inverter consisting of two transmission lines. The impedance transformation ratio at 6dB back-off region is 4 and at the peak power level is 1, when both active devices provide the equal amount of output power. This impedance transformation ratio limits the bandwidth of DPA at back-off. In work [7], increasing the load impedance $R_{opt}/2$ to the higher value of $\sqrt{2}R_{opt}/2$, leads to a fractional bandwidth of 20%-67% by using GaN device. However, higher load impedance degrades the efficiency at saturation. Moreover, broadband operation of DPA has been achieved by compensating the output capacitances. In work [8], the parasitic capacitances are absorbed into the transmission lines of impedance inverter. That increases the characteristic impedance of T-lines and decreases the lengths of them. In that work, the DPA is implemented using LDMOS transistors and 37-47% drain efficiency across the band frequency of 650-950 MHz for LTE signal have been obtained. In other effort [9], the effect of the second harmonic component on the load modulation is eliminated by using a same reactance at back-off (OBO) and saturation demonstrating 44-55% drain efficiency across the frequency band of 3.3 to 3.75 GHz.

Recently, post matching technique has been proposed in literature to extend the DPA bandwidth. In this method, the narrowband output combiner is replaced by a low-pass network to transform the load impedance into the average optimum resistance across the bandwidth. Fractional bandwidth of 54-77% has been reported over the 0.9-2.7GHz band Frequency [10] considering only fundamental matching. In [11] short-circuited second harmonic is included into the post-matching and the implemented DPA delivers 47-54% drain efficiency at OBO over the 1.8-2.7GHz.

The main purpose of this paper is to represent the systematic approach of a Class-J DPA using the post matching network for more design space over a wide bandwidth. The design methodology includes the optimum Class-J DPA bias

conditions, source pull/load pull simulations and stability assessment. The work is organized in the following sections. Section 2 provides a brief overview on the Class-J theory of operation and optimal load impedances at the fundamental and second harmonic terminations. The design topology of a dynamic load modulation using post matching network is presented in Section 3. The wideband operation of proposed Class-J DPA is verified by ADS simulation results in Section 4. Finally, the main conclusions are discussed in Section 5.

II. Review of Class–J Operation Mode

The key difference between the Class-J PA and Class-F or F^{-1} modes of operation [12], is the requirement for a specific capacitive second harmonic termination that generates a rectified sine-wave. In this mode of operation, the combination of a reactive component at the fundamental and a low capacitance value can restore the RF power and efficiency excellent results. In such a way, the harmonic flowing into the capacitor, generates the reactive voltage component for higher fundamental component whilst, the fundamental matching network blocks the higher harmonic currents. The drain voltage and current waveforms are characterized by half-sinusoidal waves with a phase shift between them and can be expressed by a Fourier series expansions in equations (2) and (3):

$$V_{d,B}(\omega t) = V_{dc}(1 + \sin(\omega t)) \tag{1}$$

$$\begin{aligned} V_{d,J}(\omega t) &= V_{dc}(1 + \sin(\omega t))(1 + \cos(\omega t)) \\ &= V_{dc} * [1 + sin(\omega t) + cos(\omega t) \\ &\quad + 1/2\, sin(2\omega t)] \end{aligned} \tag{2}$$

$$I_{d,J}(\omega t) = I_{max}\left(\frac{1}{\pi} + \frac{1}{2}\sin(\omega t) - \frac{2}{3\pi}\cos(2\omega t)\right) \tag{3}$$

Class-J drain voltage can be achieved by a shift of the Class-B PA drain voltage, given in equation (1). It is easy to see that adding the sine and cosine functions provides a phase shift for the component at the fundamental frequency and the second harmonic voltage adds in phase to boost the fundamental component. Therefore, the voltage waveform consists of DC, fundamental and second harmonic voltage components.

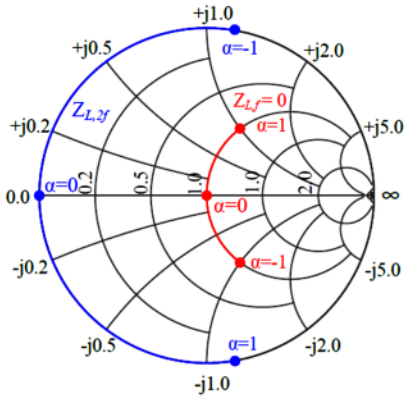


Fig. 1. Desired fundamental and harmonic load impedances of FET.

$$\begin{aligned} V_{d,J}(\omega t) &= (V_{dc} - V_k)(1 + \sin(\omega t))(1 \\ &\quad + \alpha\cos(\omega t)) \end{aligned} \tag{4}$$

$$\begin{aligned} V_{d,J}(\omega t) &= (V_{dc} - V_k)\,[1 + sin(\omega t) + \alpha cos(\omega t) \\ &\quad + 0.5\alpha\, sin(2\omega t)] \end{aligned} \tag{5}$$

By adding a factor to the front of the cosine function (α) in equation (5), which sweeps from -1 to 1, the result is a family of voltage waveforms [13]. The Class-J is the case where α is equal to 1, and class-B happens to be the case where α equals 0, and there is also the mirror image of Class-J where the α equals -1. Fig. 1 shows the fundamental and harmonic impedances at the current source by varing α. The key difference between the Class-J PA and other related PAs is the requirement for a specific capacitive second harmonic termination to generate a rectified sine-wave. In this mode of operation, the combination of a reactive component at the fundamental and a low capacitance value can restore the RF power and efficiency excellent results. In such a way, the harmonics flowing into the capacitor, generate the reactive voltage:

$$\begin{aligned} Z_{L,J@f_0} &= \frac{(V_{dc} - V_k)(1 + j)}{\frac{I_{max}}{2}} \\ &= \frac{2(V_{dc} - V_k)}{I_{max}}(1 + j) \end{aligned} \tag{6}$$

$$\begin{aligned} Z_{L,J@2f_0} &= \frac{-0.5(V_{dc} - V_k)j}{\frac{2I_{max}}{3\pi}} \\ &= -\left(\frac{3\pi}{8}\right)\frac{2(V_{dc} - V_k)}{I_{max}}j \end{aligned} \tag{7}$$

As can be seen in equation (7), the load impedance at the second harmonic leads directly to a shunt capacitance value. As a result, the Class-J scheme offers a potentially wide-band and high efficiency operation. The simulated time-domain drain voltage and current waveforms are plotted in Fig. 2 [14]. Class-J PA uses a phase shift between the voltage and current waves to provide the purely reactive second harmonic termination, however, the phase overlap between the waveforms may degrade the performance of the PA.

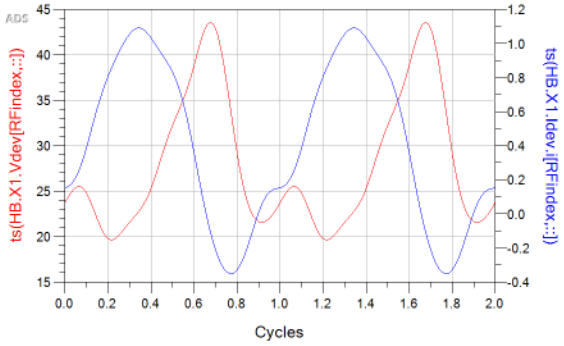


Fig. 2. Normalized current and voltage waveforms.

III. A Post-Matching Doherty PA Emploing Specific Second Harmonic Termination

Fig.3 shows the principle of post-matching structure [15], in which the load impedance of Z_0 is decreased to the Z_0'close to the transistor's optimum impedance. To design a symmetrical DPA a Gallium-Nitride (GaN) high electron-mobility transistor (HEMT) is selected due to its electrical properties of wide band gap, high power density and high thermal conductivity. The biasing condition can be defined by considering a tradeoff among desired gain, efficiency, IMD and RF output power. Theoretically, for Carrier PA a bias point close to the cut-off region can provide high-efficiency in broadband applications, while reducing the conduction angle for Peaking PA near Class-C bias point, requires a progressively higher excitation amplitude and implies a gain reduction.

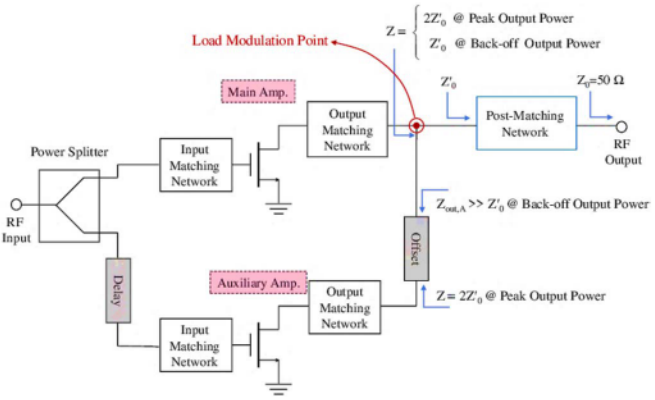
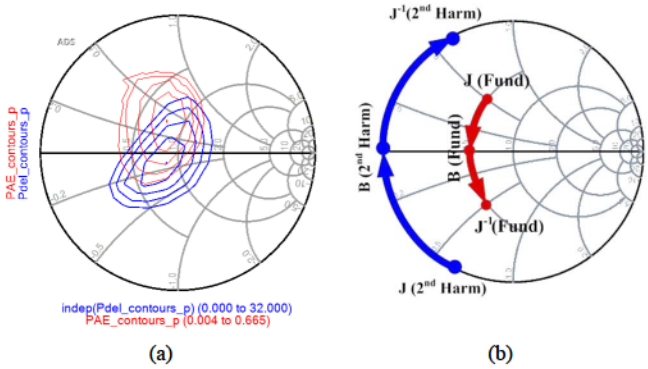


Fig. 3. Post-matching DPA technique.

In order to the control the fundamental and second harmonic terminations, the load-pull/source pull simulations are carried out to track the transistor performance by varying impedances. In this work, using the nonlinear model of the FET, Load-pulling analysis is carried out at several frequencies between 1.5 to 3.2 GHz for the efficiency and output power contours over the normalized fundamental and second harmonic reactive plane at the intrinsic device. The overlap between the efficiency contours that is bounded by at least 50% Power Added Eficiency (PAE) throughout the frequency band can provide the proper load impedance at back-off. While the optimal impedances in Doherty region can be obtained by output power contours when the input power is set to 30dBm to make the device saturated. Fig. 4(a) indicates that for Cree CGH40010F GaN HEMT device the maximum PAE and output power at center frequency are around 65% and 42dBm respectively at OBO. In the second step, the second harmonic load termination can be defined by conducting the second harmonic load-pull simulation, while the device sees the optimum fundamental load impedance and the higher harmonics are all open-circuited. Fig. 4(b) shows the distribution of second harmonic terminations across the periphery of the Smith-Chart and the output loads predicted for the Class-J design space. The Class-J amplifier is very sensitive to the second harmonic termination which is realized by device output capacitance and has a considerable effect on the DPA efficiency.

In this design, the Multisection-matching networks based on low pass transformers for both post-matching and output matching networks (OMN) of Carrier and Peaking PAs are employed. This method can suppress the harmonics significantly and provides a wide frequency bandwidth with minimum power gain ripple. Typically, for the low impedance values, the design methods of the Chebyshev multi-section transformer is based on the transforming low-pass filters (LPF) of a ladder configuration [16]. Fig. 5. illustrates the LPF that consists of series inductances with shunt capacitances, with different transformation ratios $r = R_1/R_2$. Where R_1 is the characteristic impedance of the network and R_2 is the input resistance of the LPF. The output impedance is resistive because the output device capacitive reactance is compensated by the inductance.



(a) (b)

Fig. 4. (a) Output power and PAE counters of load-pull at fundamental frequency, (b) Design space of fundamental and harmonics load impedances.

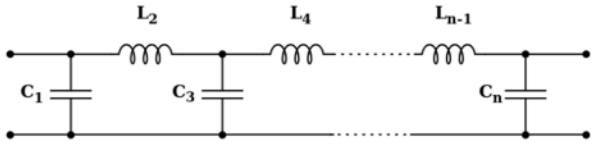


Fig. 5. Ladder topology of low-pass filter

$$C_1 = g_1/2\pi(f_2 - f_1)R_1\,, \qquad (8)$$
$$C_3 = g_3/2\pi(f_2 - f_1)R_1$$

$$L_2 = g_2R_1/2\pi(f_2 - f_1), \qquad (9)$$
$$L_4 = g_4R_1/2\pi(f_2 - f_1)$$

In order to simplify the calculations of low-pass impedance transformer for Carrier PA by considering $C_1$and L_2 in Fig. 6, the impedance Z_{opt} can be expreesed as:

$$Z_{opt} = jwL + \frac{1}{jwC + \frac{1}{R}} \qquad (10)$$

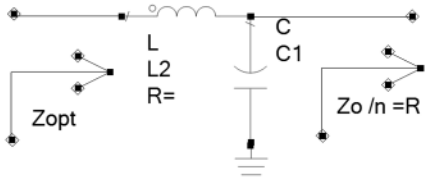


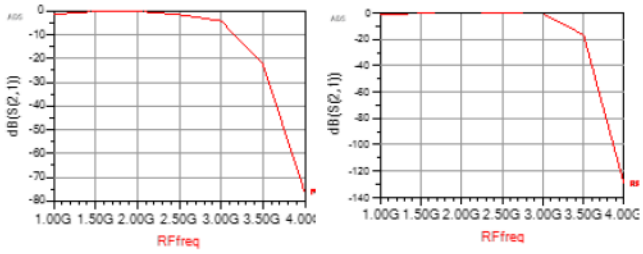
Fig. 6. Low-pass impedance transformer

Expression (10) can be expanded to real and imaginary parts while the imaginary part can be adjusted by varying the inductor value. The real part of Z_{opt}, by changing R to $2R$, can be computed as:

$$Z_{opt} = \frac{R}{1 + R^2\omega_0^2C^2} = \frac{2R}{1 + 2R^2\omega_0^2C^2} \quad (11)$$

$$\omega_0 = \sqrt{\frac{1}{2R^2C^2}} \quad (12)$$

Thus, R is determined by the low-pass impedance transformer in Fig. 6, the impedance ratio of post matching network can be obtained by $n = Z_0/R$, where, $Z_0 = 50\Omega$. The output matching network of Carrier PA at back-off region, transfers the real part of the matching impedance (Z_{opt}) to the optimum impedance that can make the device saturated with 3dB lower than saturated power level. Whilst, at Doherty region, the output matching network provides appropriate matching from $2Z_0'$ to the average optimum impedance that provides the maximum output power. In this work, from the simulated results, the optimum impedances are obtained within a range of 13-25Ω at OBO, therefore, the average impedance of 17Ω is set for Z_{opt}. Since the output impedance of the Peaking PA has an influence on the Carrier PA matching at lower power levels, an offset line is required at the peaking OMN to provide large output impedances [17,18].The series section of inductance can be realized as a short circuited transmission line and the shunt capacitance can be replaced by open circuited shunt transmission line. Values of the dc blocking capacitors are often chosen at picofarad due to their self-resonance frequency and low effective resistance at the fundamental frequency. The load modulation needs to operate on the fundamental component then, the capacitive second harmonic terminations are integrated into the OMNs. The independent design of the fundamental and harmonic matching networks allows for the suppression of the harmonic power. The input matching network is responsible to maximize the gain level over the operating band frequency. Thus, the key design feature of this matching network is to closely match the transistor at the highest bandwidth frequency, where the power gain is at the lowest level. In such a case, the power gain at the lower frequencies will be sacrificed to compensate the intrinsic transistor gain roll-off. The initial approach for selecting the average optimum source impedance is to perform source-pull simulations over the band. Fig. 7 demonstrates the frequency response of the input (a) and output (b) matching networks over the frequency band contributing in an overall flat transducer gain.



(a) (b)

Fig. 7. S-parameter of the distributed elements of the matching networks. (a) IMN, (b) OMN.

It should be noted that the distributed network synthesis for a wideband bias network is required during the design process. The drain-biasing network affects the overall efficiency due to the high voltage and current flowing through this line. An appropriate thickness of the microstrip bias line provides low inductance at low frequency for stability, and high impedance in the operating frequency range for a minimum loss. Fig. 8 indicates the network synthesis for the desired bias line including a set of decoupling capacitors, radial stub to short out the RF signal from 1.5 to 3.2 GHz and a 90° transmission line to transform the short circuited condition to open circuit at the gate of the device. The minimum bias-tee line's width, that can handle the maximum DC drain current of 0.6A is calculated as 0.516mm, which corresponds to an 80Ω characteristic impedance for Rogers4350 substrate. It is important to highlight that a circuit design solution that increases the real part of the impedance would be applicable to provide significant stability margin. Since there is a trade-off between stability and gain, a series resistor at the transistor input will push the load stability circle outside of the Smith Chart and improve the Return Loss without sacrificing the power gain at the design frequency.

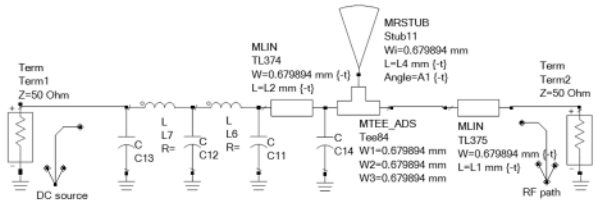


Fig. 8. Drain bias network schematic.

IV. Simulation Results

Both transistors are biased at $28V$ drain voltage, and the Carrier PA is set at -3.1V gate voltage while the Peaking PA with lower gate voltage is turned on when the output power of Carrier PA reaches 3dB back-off from the saturation. The DPA is swept over the 1.5 to 3.2GHz bandwidth, in 200MHz frequency steps, by using a single-tone continuous wave RF signal generator.

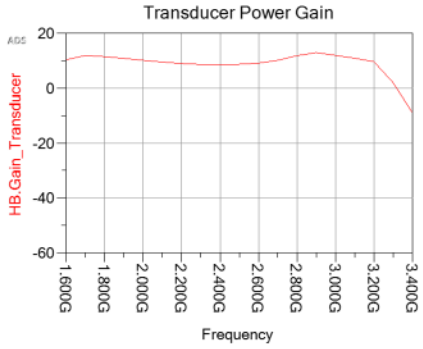


Fig. 9. Simulated gain flatness vs frequency.

Simulation result of transducer power gain versus frequency in Fig. 9 shows the gain flatness between 10 to 13dB within the entire bandwidth. Fig. 10,11 indicate that a peak drain efficiency of 58%, at center frequency with the average PAE of 47% at 6dB OBO and maximum output RF power of 42dBm have been achieved. which can be considered as a stable and satisfactory performance for the wideband DPA.

The simulated results are compared with the measured performance of recently published papers on state-of-the-art wideband DPA in Table I. It confirms that the presented wideband Class-J DPA offers aceptable performance in terms of efficiency and gain for 5G wireless communication systems combining wideband and high efficiency.

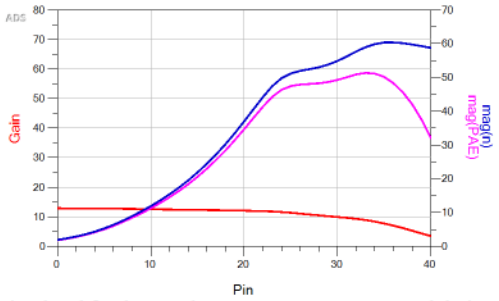


Fig. 10. Simulated fundamental RF output power, PAE and drain efficiency vs input power.

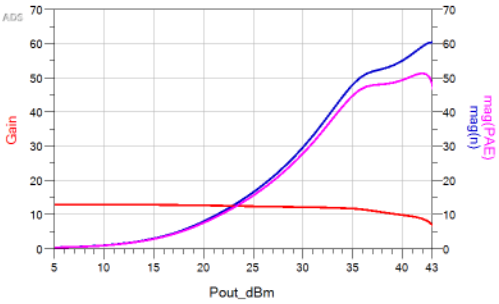


Fig. 11. Simulated fundamental RF output power, power added efficiency and drain efficiency vs output power.

TABLE I. PERFORMANCE COMPARISONS WITH RECENTLY PUBLISHED BROADBAND DPAS

Ref.	Bandwidth (GHz)	Pout(dBm)	Gain(dB)	DE peak%	DE OBO%
[19]	1.8-2.2	41.8-42.3	8.6-12.2	69-73	54-60
[20]	1.7-2.8	44-44.5	12.1-14.7	57-71	36-41
[21]	3-3.6	43-44	8-11	55-66	38-56
This work	1.5 to 3.2	40-42	10-13	50-58	40-47

V. CONCLUSION

In this paper, a broadband DPA based on Class-J PA over the frequency range of 1.5 to 3.2 GHz has been proposed and validated by a GaN HEMT transistor. A broadband impedance matching network is employed at the output of DPA to reduce the impedance transformation ratio. It is shown that the key for obtaining the maximum efficiency in Class-J PA lies in the second harmonic voltage component as a capacitive load that increases the fundamental voltage component. The bias network is shaped by the desired compromise among the isolation, current-handling and low-frequency stability. The Chebyshev matching network is selected by minimum reflection coefficient as an approximation of an ideal network. The designed broadband Class-J DPA can provide a maximum 51% PAE and 42dBm output power within 72% fractional bandwidth.

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