Iberdrola Innovation Middle East &
University of Strathclyde

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Distributed ReStart: Non-conventional Black-Start Resources

RTDS Based Network Energization from Grid Forming Converters: Part 1

GENERAL NOTES

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CONTENTS

Distributed ReStart: RTDS Based Network Energization from GFCs: Part 1

1. Introduction

Following the past two studies submitted as part of Distributed ReStart project tasks between SPEN and Iberdrola Innovation Middle East, this report summarizes preliminary results achieved as part of the third work package of the project, undertaken in experimental collaboration with the state-of-the-art smart grid laboratories at the University of Strathclyde, namely the Dynamic Power Systems Laboratory (DPSL) and the Power Networks Demonstration Center (PNDC).

The aim of this report is to shed light on the real-time modeling of grid forming converters for black-start applications, starting from a similar simplified network reported in work package 2 study for proof of concept, and then expanding into Chaplecross electrical network in Scotland to simulate the black-start energization of a smaller segment from this network as a preliminary step to extended planned tests that take into account further scenarios. Throughout this report, the GFC control used is illustrated in Figure 1, including soft energization, voltage support and grid synchronization capabilities. The modified grid-synchronization control requires access to high-precision voltage measurements from the synchronizing point.

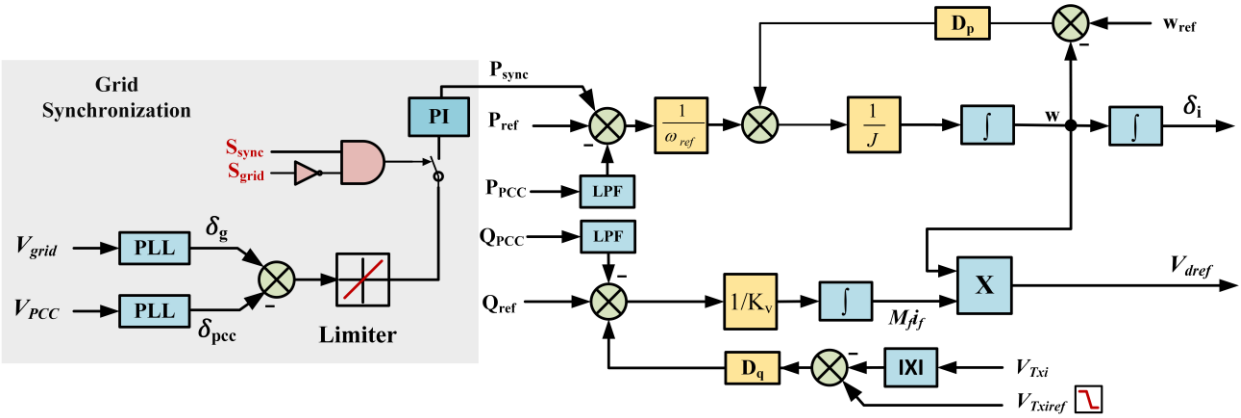

Figure 1: High-level VSM control block diagram for the GFC loop used in this study.

Power Hardware in the Loop (PHIL) is then investigated to test the integration of external hardware converter to the simulated RTDS networks in grid-forming mode. This technique aims to test hardware converter's ability to energize a modeled version of the network, through supplying the simulated RTDS network with a controlled voltage input. The hardware grid-forming converter feeds a scaled power into an interface current source converter receiving its reference from the simulated network, such that the hardware voltage-source/current-source twin mimics the simulated network behavior.

This study aims to provide practical insights on PHIL benefits for grid-forming converters testing, and whether or not that should be considered as a viable tool for GFC testing in addition to RSCAD/PSCAD pure simulations. The prospective advantages of using PHIL for GFC testing is bridging the gap further between simulation and hardware and unlocking the testing ability of hardware GFCs on expanded network modeled in real time. That being said, the application of this idea has its limitations and challenges that are highlighted in a dedicated

section with relevant recommendations. In this report, the PHIL capability is validated for the simplified black-start network, with the aim of expanding its application in the final report into Chaplecross network scenarios.

2. Simplified Network Simulation in RTDS

A similar network to that used in WP2 study report is first simulated in RSCAD software to perform preliminary analysis in real-time-digital-simulation (RTDS) platform in preparation for the PHIL tests. The network block diagram is illustrated in Figure 2.

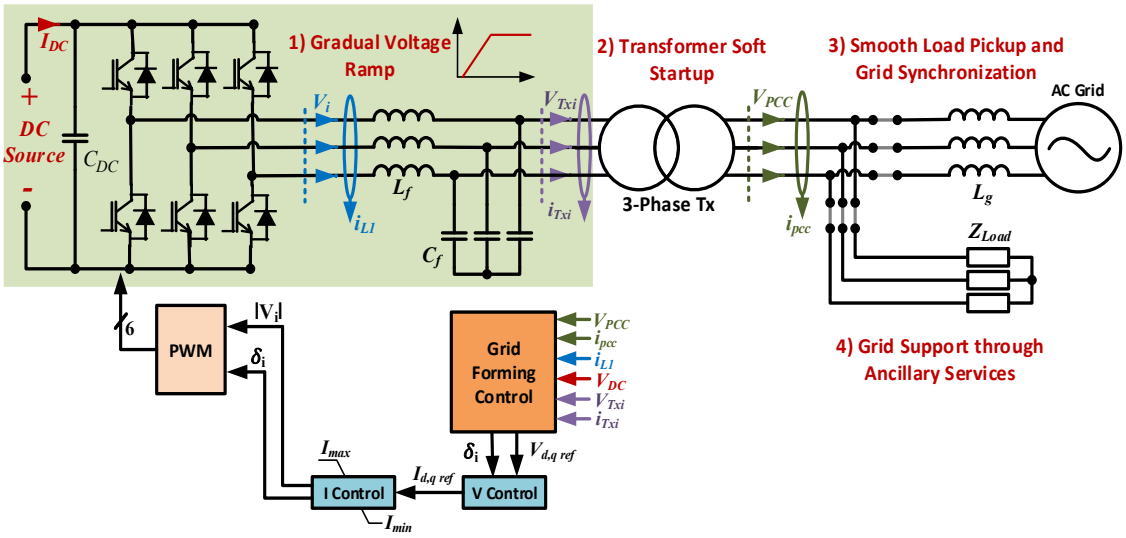

Figure 2: Simplified network used for preliminary grid-forming control validation in RTDS platform.

A Chaplecross network model has been developed by the UK National HVDC Center for transient and protection analysis. Since Chaplecross is the area of interest for this study, the transformer model used in the model to interface Steven Croft's power station to the network is embedded in the simplified RSCAD network in Figure 2 with similar saturation characteristics. Using the soft black-start sequence illustrated in Figure 2, the simulated network black-start functionality in RSCAD is confirmed.

A summary of results is illustrated in Figure 3. Soft voltage ramp of 10 seconds is applied, then a 20 MW load is connected at t = 12 s, followed by grid synchronization control activation at t = 14, and the actual synchronization tacking place just before t = 20 s. Transformer residual flux is set to arbitrary values for this test. The resulting energizing inrush current is minimal due to the soft energization, the large load pickup causes a momentary voltage disturbance that is countered by the GFC voltage control, and load synchronization is achieved smoothly with minimal impact on the frequency trace. The active power setpoint after synchronization is set to 30 MW to test the control's ability to follow a setpoint robustly, driving the frequency back to 50 Hz. Figure 3 also illustrates a zoomed view on voltage and current at the synchronization instant, illustrating the seamless voltage transition, and the smooth current adjustment to follow P and Q setpoints.

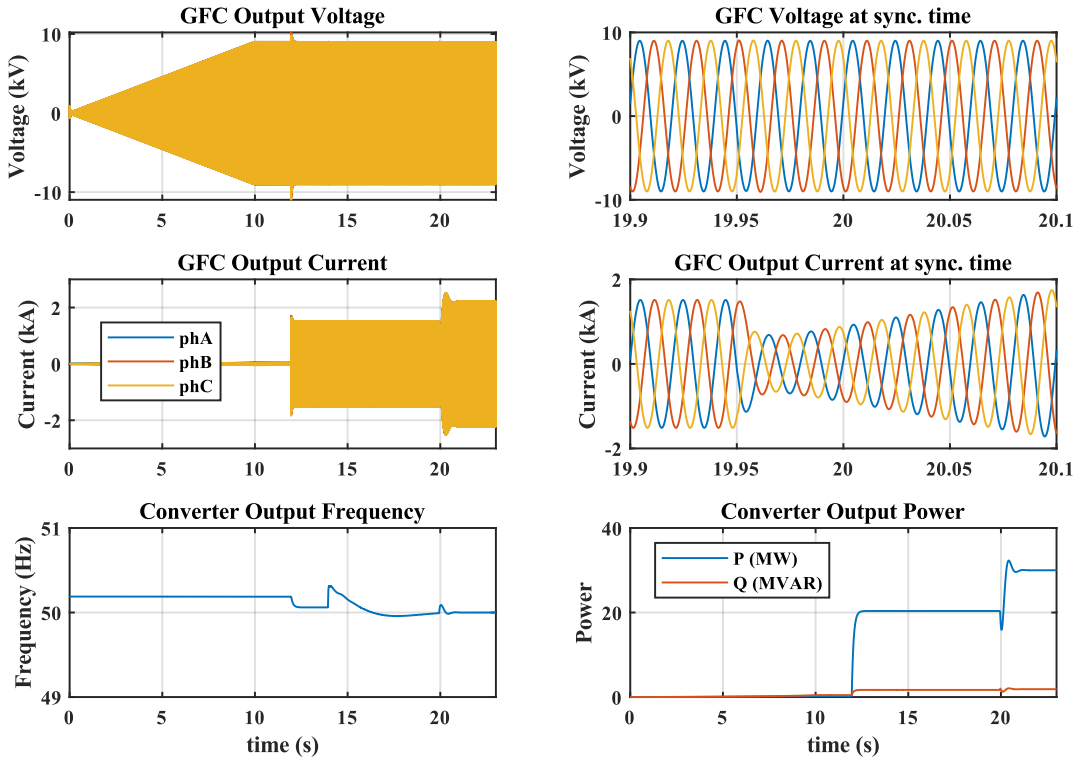

Figure 3: Simplified network RTDS simulation results.

3. Chaplecross Network Restoration Scenario

The UK National HVDC Center model for Chaplecross network is adapted in this study to investigate the capability of grid-forming converter (GFC) trials for black-start. The Steven's Croft power station is replaced by a GFC average model at the 11 kV bus to energize segments of the network in post-blackout scenarios. One scenario is presented in this report, with the aim of extending to multiple network segments in Part 2 of this study through additional scenarios. The selected scenario requires the GFC to energize the area marked in red in Figure 4, encompassing two large power transformers (53 MVA at 11/33 kV and 90 MVA at 33/132 kV), and two earthing transformers. The HVDC Center model assumes a 1% rated magnetizing current for the transformers, a knee voltage of 1.25 pu, with an air-core inductance of 0.265 pu for the 53 MVA transformer and 0.3 pu for the 90 MVA transformer. Variations to these parameters in reality can alter the studied inrush current behavior.

Two sub-scenarios are covered here. First, the GFC is required to synchronize to the 132 kV point after the 90 MVA transformer HV side. The GFC here is required to energize both 53 MVA and 90 MVA transformers and the earthing transformers. In the second scenario, the synchronization takes place at the 33 kV point before the 90 MVA transformer (with the assumption that this transformer is energized by the HV grid) to investigate the

reduced energizing requirements. The source is assumed to have sufficient capacity at the time of energization (i.e., solar irradiance in case of PV, wind speed in case of wind turbines or SoC in case of storage).

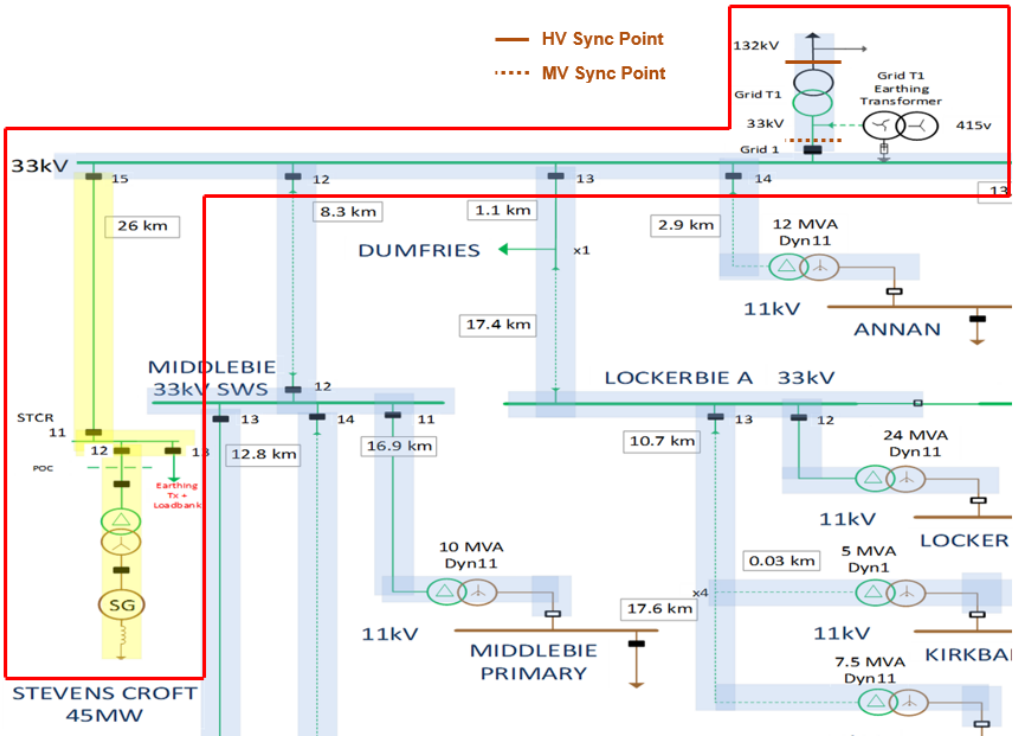

Figure 4: Chaplecross network section considered for energization in RSCAD model (with HV/MV synchronization).

The residual flux is maintained in both the 53 MVA and 90 MVA transformers at phase A: 0.8 pu, phase B: 0 and phase C: -0.8 pu throughout the tests to emulate conditions near worst-case scenarios. In steady state island mode, with the cables and transformers only connected to the converter, it is observed that GFC consumes 1.56 MW and absorbs -3.64 MVAR when both 53 MVA and 90 MVA transformers are connected. When the 90 MVA transformer is energized by the grid and only the 53 MVA is fed by the converter, the steady state requirements decrease to 0.56 MW and the converter absorbs -4.68 MVAR. These numbers are indicative based on the existing network model and the covered scenario in Figure 4, and can help sizing a converter if it mainly aims to soft energize the network and connect to a different source that can then take care of additional load supply.

3.1. Hard Energization – Chaplecross (Both Main Tx Connected)

Hard energization is first tested only with voltage control applied; the breaker is closed at -30 degrees to generate the maximum inrush in phase AB of the delta primary of interface transformer at its zero-crossing point. The converter phase currents can exceed 20 kA as observed in some simulations, and peaks around 15 kA for the case presented here as illustrated in Figure 5, demanding around 300 peak MVAR for the full network energization as in Table 1. For comparison, a 40 MVA converter is rated at 2.97 kA per phase (1 pu). Clearly, classical hard energization in this case is not advised.

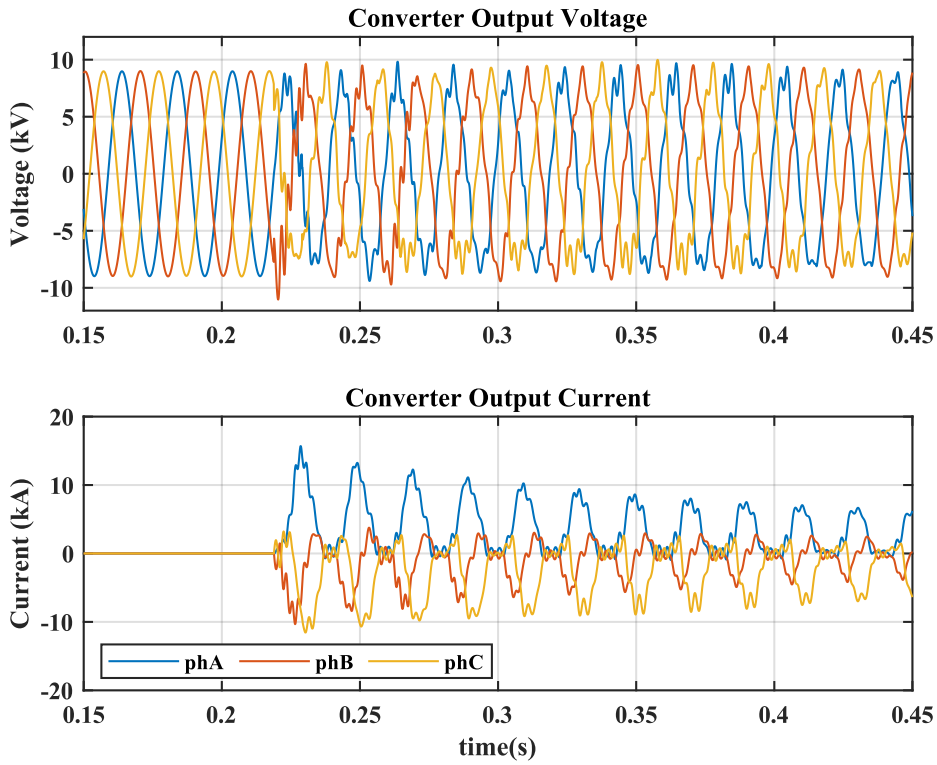

Figure 5: Hard energization results from Chaplecross scenario (Voltage Control) with both transformers connected.

Next, hard energization with inner voltage and current control loops is tested. The inner loops are implemented in synchronous dq frame using PI controllers. This implementation is observed to reduce the peak observed current to around 8 kA at around 125 MVAR requirement with similar initial energizing angle (see Figure 6). The control current reference is restricted here to 5 kA peak. Setting stricter current limits is observed to reduce the peak current further, however, resulting in higher voltage spikes at the energization instant. This could be an interesting point for further studies to balance both acts.

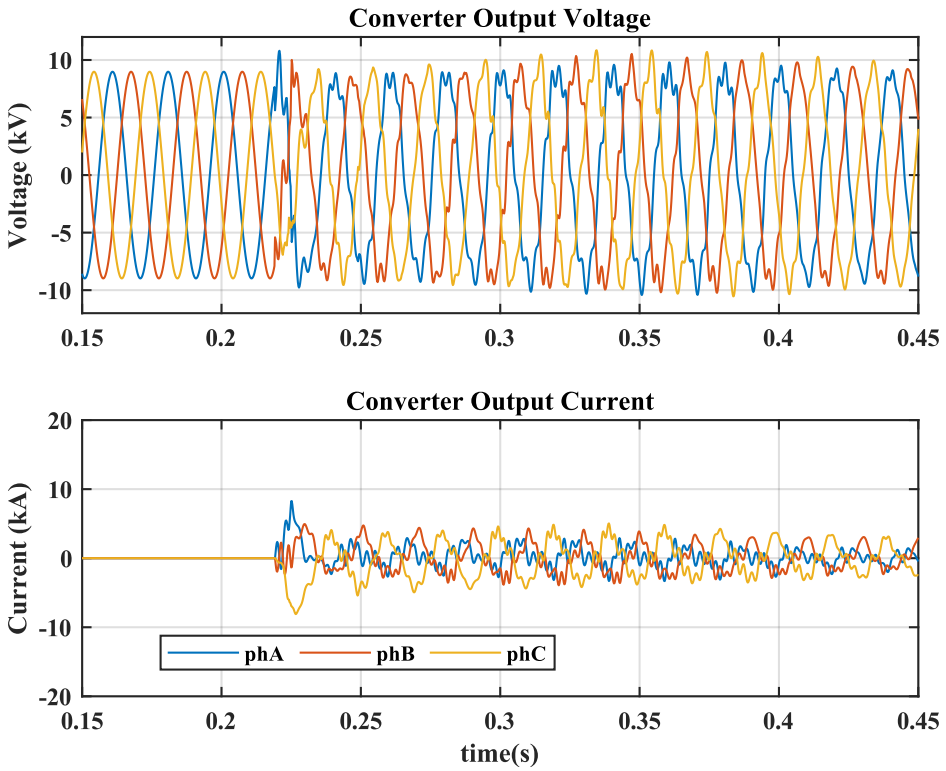

Figure 6: Hard energization results from Chaplecross scenario (Current Control) with both transformers connected.

In both previous cases (voltage and current controlled energization), the transients are stabilized in few seconds and the steady state voltages and currents are as illustrated in Figure 7. The current is non-sinusoid as it is primarily composed of the 53 MVA and 90 MVA transformers magnetizing currents with active hysteresis loops.

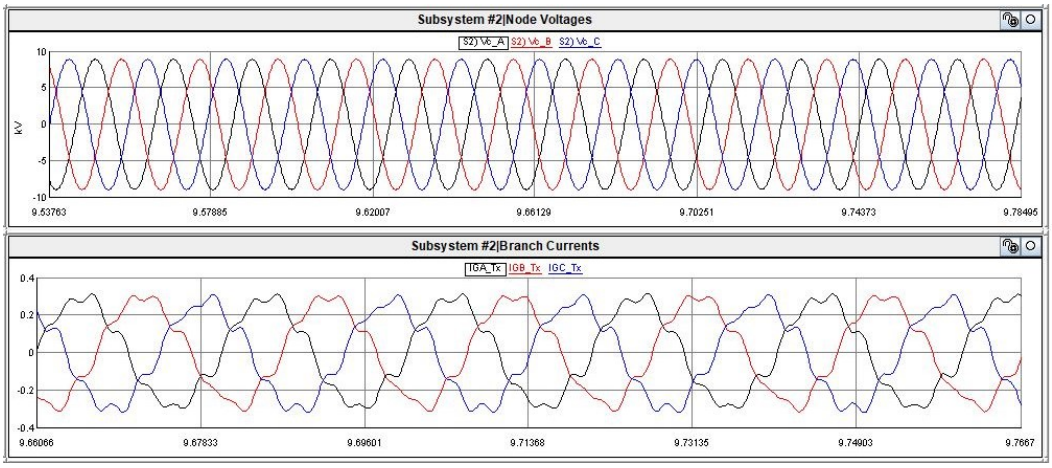

Figure 7: Steady state post-energization converter voltage and current (kA) waveforms from RSCAD.

3.2. Soft Energization with Complete Black-Start Sequence – Chaplecross

Soft network energization aims to minimize inrush current by gradual transformer core flux buildup to avoid saturation and consequent large magnitude inrush currents. Selection of appropriate ramping times is important to avoid too fast ramps that could still cause inrush, or too slow that could cause protection equipment malfunctions. In this section, the soft energization of the highlighted network in Figure 4 is carried out for both MV and HV synchronizing points, with connected inner voltage and current loops. The ramping time is selected as 10 seconds.

3.2.1. Synchronizing at 132 kV (HV) Side

All circuit breakers are initially closed (except for the synchronizing point), and the ramping is initiated for a duration of 10 seconds. The results of this scenario are illustrated in Figure 8. The inrush current buildup is significantly minimized compared to hard energization case with both transformers, peaking around 1 kA with a peak 0.8 MVAR energizing demand. Then at t = 12 s, the local load is connected (6 MW/1MVAR). The synchronizing control is then activated to gradually match the phase angle between the voltages on both sides of the synchronization point.

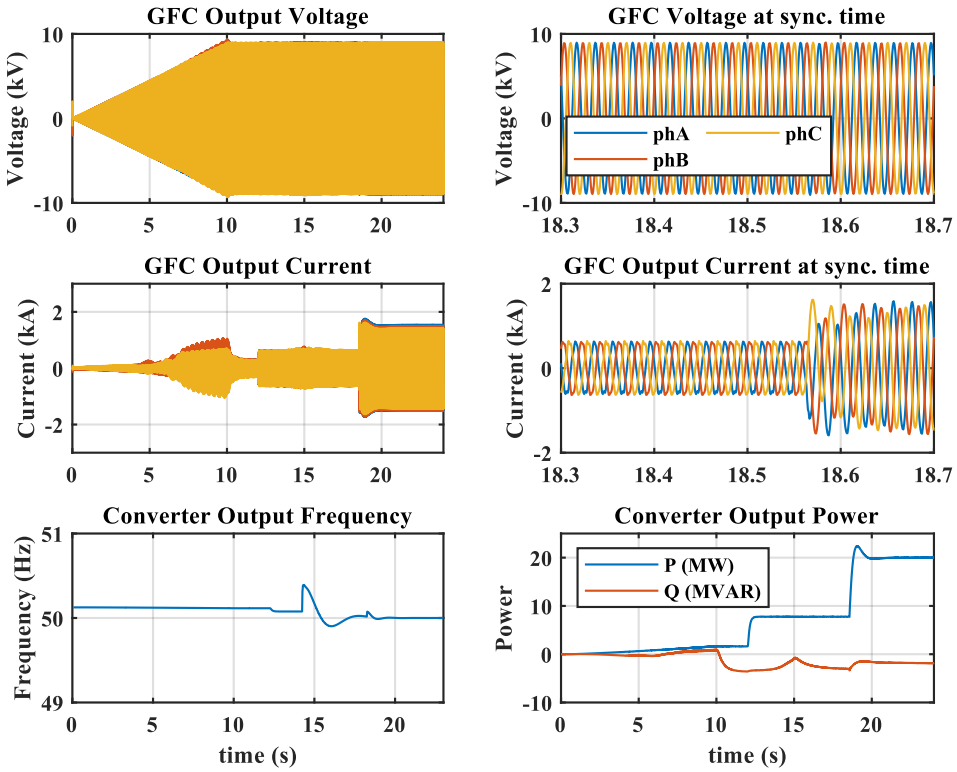

Figure 8: Chaplecross scenario soft energization results (HV Sync Point).

At t = 18, the synchronization is complete, and the HV grid is connected successfully. The VSM shifts at this point to tracking P and Q setpoints, or P and voltage support (design choice, see Figure 1). In this case, voltage tracking is selected as a priority over Q injection, and thus Q varies according to the voltage setpoint. The P

setpoint is set to 20 MW. The GFC frequency trace is within acceptable limits throughout the operation, changing mostly during synchronization because of the fast-synchronizing PI control operation (see Figure 1). This can be smoothed for longer durations in reality by choosing slower PI control gains, as these are set here to achieve fast synchronizing voltages phase matching for combined results demonstration purposes.

Finally, a summary of energization scenarios MVAR energizing requirements covered in this report with both 53 MVA and 90 MVA transformers connected is presented in Table 1 for design reference. Most of the power demand during energization is reactive (resulting from transformers and cables energization). Soft energization reduces the reactive power requirements during energization to a minimum value. Then, the post-energization steady state requirement depends on the combination of transformers magnetizing and cables current. The used source and converter filter should be sized according to the prospective scenario.

Table 1: VAR requirements for network energization using different starting techniques (for HV sync point).

Both 53 MVA and 90 MVA Tx Connected	**Max Network Energizing Power**
Hard (Voltage Controlled)	300 MVAR
Hard (Current Controlled – 5 kA current limit)	125 MVAR
Soft Energization (10 seconds)	0.8 MVAR
Steady State P and Q before synchronization*	1.5 MW, -3.64 MVAR

* Based on the default network model components and parameters in RSCAD.

3.2.2. Synchronizing at 33 kV (MV) Side

The difference in this case is that the synchronization takes place before the 90 MVA transformer (i.e., when this transformer is energized from the grid side). Thus, the energizing load on GFC is decreased in transient operation, which leads to decreased converter current during the first 10 seconds, peaking around 0.5 kA compared to 1 kA in the previous case. Similar sequence to that followed in section 3.2.1. is followed here, and successful energization is achieved as illustrated in Figure 9. The choice of energizing only the 53 MVA transformer and cable segment or both the 53 MVA and 90 MVA transformers depends on the available capacity in the energizing source, converter size and the energizing method. An adequate selection of soft energization time as in section 3.2.1. supports the case of simultaneous energization for both transformers.

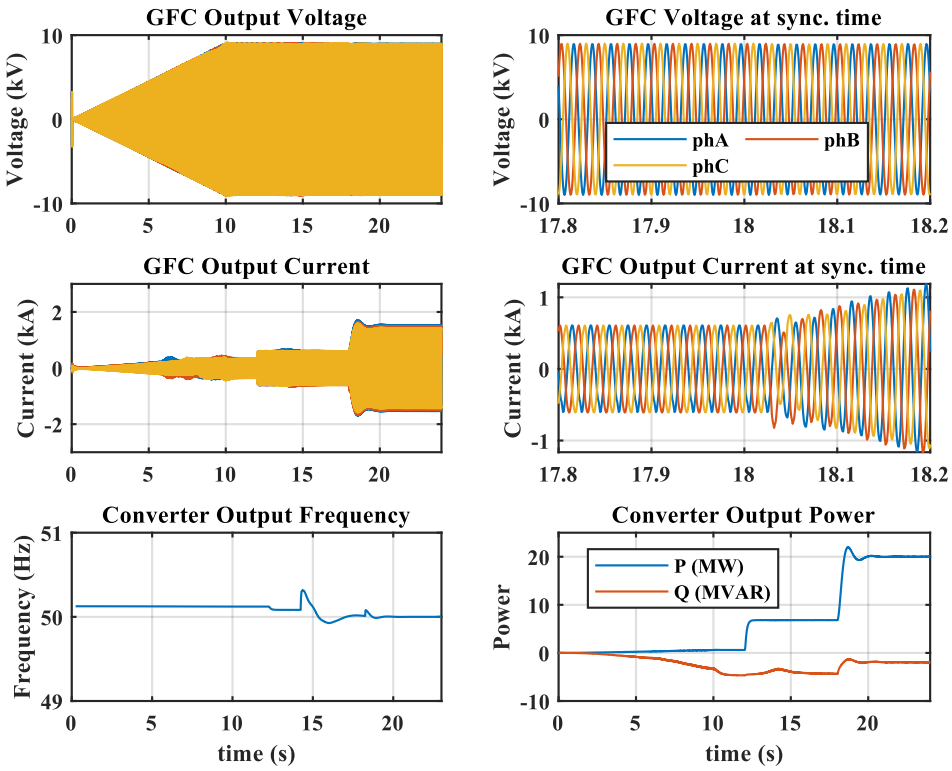

Figure 9: Chaplecross scenario soft energization results (MV Sync Point).

4. Power Hardware in the Loop (PHIL) for GFC Black-Start Application

4.1. PHIL Overview

Power Hardware in the Loop (PHIL) technique is typically utilized in power converters context to carry out investigations of physical grid-following converters that are interfaced with the real-time emulated power grid through a power amplifier, and use the voltage provided by the power amplifier to synchronize and regulate its output for grid-tied application. In this case study, as the grid-forming converter has its internal control loop to regulate voltage and frequency to energize the power network, the PHIL setup for grid-following converter testing is not applicable as the power amplifier and the grid-forming converter regulate their voltage and frequency separately and the lack of voltage synchronization may lead to stability issues. The current-type ideal transformer model (I-ITM) interface is thus employed to tackle the stability issue and incorporate the grid-forming converter in the PHIL setup.

Figure 10 illustrates the block diagram of the PHIL simulation that comprises a real-time digital simulator (RTDS), current-type ideal transformer model (I-ITM) interface, Triphase 15kVA (TP15kVA) converter operating in its current-source mode, and Triphase 90kVA (TP90kVA) converter implemented with grid-forming control schemes. As shown in Figure 11, in the I-ITM interface based PHIL setup, the output voltage V_{abc}^{*} of the GFC (i.e., TP90kVA converter) is measured and fed back to the RTDS to energize the emulated

power network via controllable voltage sources. On the other hand, the current I^*_{abc} flowing through the point of common coupling (PCC) in the simulated power network is measured and transmitted to the current-source power amplifier (i.e., TP15kVA) as a command signal to regulate its output current. TP15kVA is coupled with TP90kVA by sourcing current, thus enabling the PHIL closed-loop configuration and mimicing the relative power behaviors in the emulated power network.

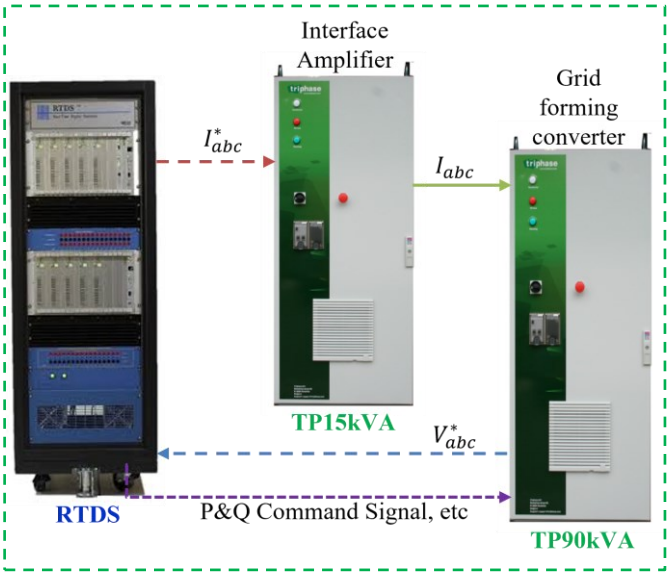

Figure 10: Block diagram of the PHIL configuration.

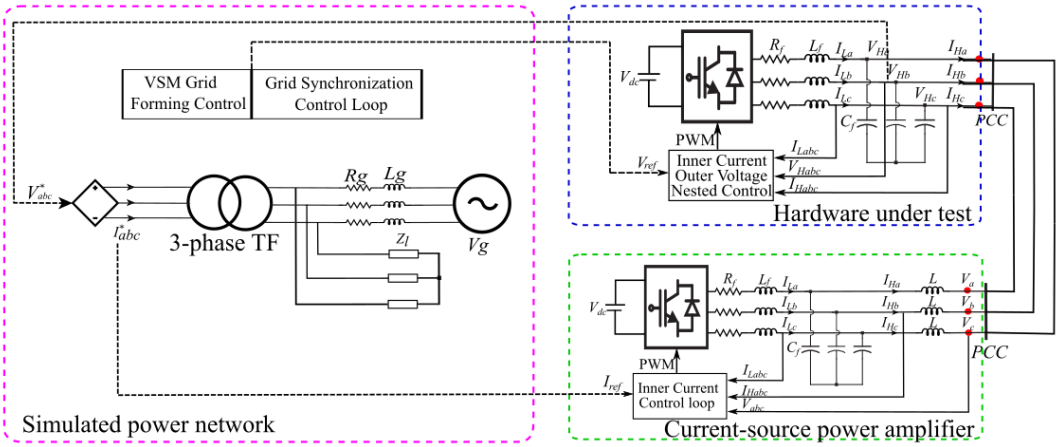

Figure 11: Circuit diagram of the emulated power network and the power converters.

Due to the limited voltage levels of the TP90kVA converter and the current constraint of the TP15kVA current-source power amplifier, scaling ratios are employed to facilitate the capability of the power converter to be tested and to scale down the command current signal within the current constraint of the TP15kVA converter. This represents the power converter that is emulated in the RTDS with higher power rating and voltage levels than that of the actual TP90kVA power converter. Voltage ratio (r_v=27.5) is implemented to scale up the TP90kVA rated output voltage (0.4kV) to a higher rated voltage (11kV) of the controllable voltage sources in

the emulated power network in RTDS. Current ratio (r_i=1/300) is designed to scale down the command signal before it is sent to TP15kVA. By doing so, the power rating of the emulated GFC at the simulation side is 8250 times that of the actual TP90kVA converter.

The time delay steaming from the signal conversion units (e.g., ADC and DAC cards, low-pass filters designed for noise mitigation), the digital control of the power amplifier, and the digital computation of RTDS, inevitably degrades the PHIL closed-loop stability margins, deteriorates the power signal synchronization and the transparency of the power transfer between the simulation side and hardware side. As the VSM control and grid synchronization control are dependent on accurate power measurement and voltage signal synchronization, time delay compensation schemes are developed to facilitate the PHIL simulation and to enable a more stable and accurate closed-loop simulation environment. The dq-frame phase-shift time delay compensation scheme and the DFT based time delay compensation scheme and are extensively utilized to compensate for the time delay in the PHIL setup.

4.2. PHIL Results

The simplified network presented in Figure 2 is used as a basis for the preliminary PHIL tests to validate the hardware GFC integration for black-start. The tests aim ultimately to achieve stable and accurate PHIL operation throughout the black-start process, and to identify potential challenges in the process. Hard energization is not tested in PHIL to avoid tripping the interface current amplifier. Instead, soft energization with t = 10 seconds is used here, followed by 40 MW load pickup in simulation at t = 13 s. The used ratio scales down in real-time the 3 kA per phase in simulation when the load is connected to 10 A in hardware.

Voltage delay compensation is implemented in RSCAD to match the measured voltage phase from hardware converter with the reference control sent from RSCAD (see Figure 11), whereas current reference time delay compensation is performed in the hardware side. Figure 12 illustrates the closed-loop PHIL results for soft transformer energization and load pickup (from RSCAD). The voltage and current panels on the right represent a zoomed version around ramping end time (t = 10 s). The frequency remains close to 50 Hz throughout the test, and the measured power in simulation quickly ramps to 40 MW at load connection instant. Voltage-mode VSM is used in this test for preliminary PHIL functionality validation.

Hardware current measurements are also recorded during the test to validate the observed trends in RSCAD and the hardware current reference tracking behaviour of the interface amplifier. As illustrated in Figure 13, the scaled down three-phase reference at ($r_i = 1/300$) is received correctly at the hardware side, and the actual measured current attempts to track the ramping trend. However, with noisy and oscillatory behaviour throughout the voltage ramp. A disturbance is also observed in the dq current amplifier reference prior to load connection with 10 A reference, which suggests a potential impact from the hardware converter phase-locked-loop (PLL)

at low and harmonic rich current values. Addressing this tracking issue and implmeneting stable current control and grid synchronization as part of the integrated control are the next steps for the project PHIL investigation.

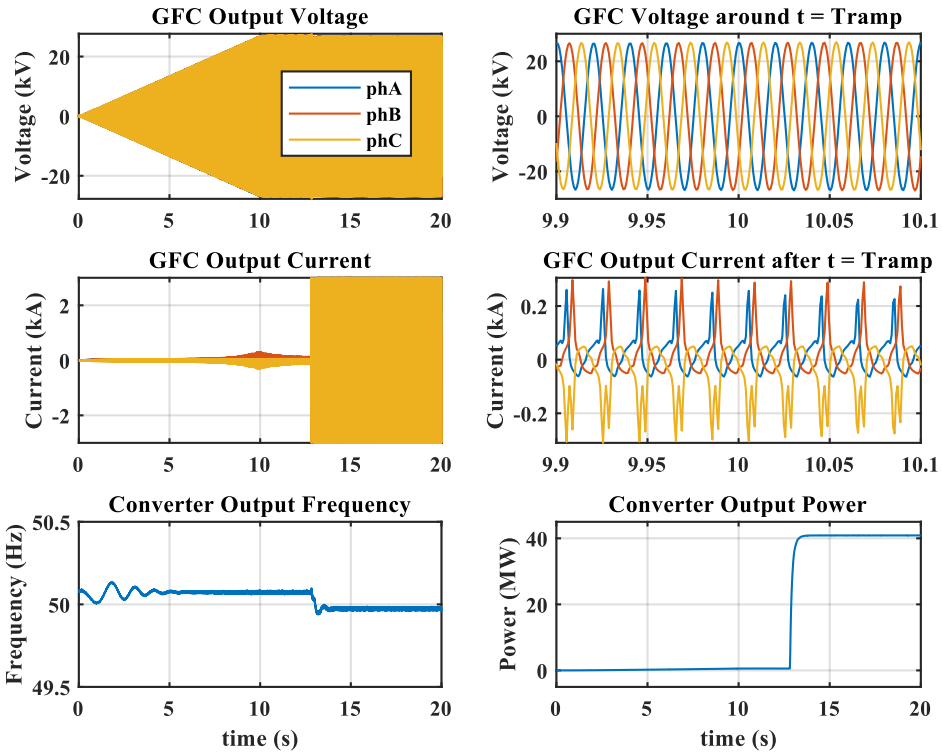

Figure 12: PHIL results (from RSCAD) for the transformer energization and load pickup (40 MW) steps.

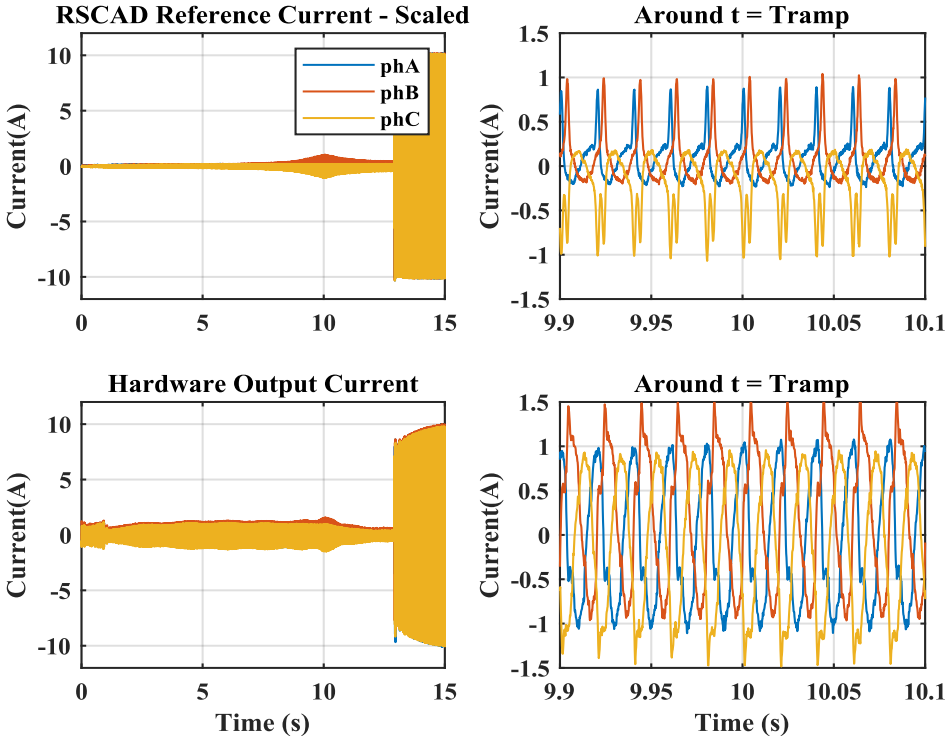

Figure 13: PHIL current reference from RSCAD vs. actual hardware output current.

5. Lessons Learned and Opportunities Identified

5.1. RTDS Network Models Exchange

Real-time digital simulator platforms utilize processor- or core-based hardware and licensing configurations. The development of models, particularly for large-scale networks, on such platforms should be paid careful attention to if the model is to be exchanged for use between multiple organizations that have different configurations and number of cores. Real-time simulators offer the capability for users to manually allocate each power system and control components to available processors or cores while reserving one or two processors or cores for network solution. However, this manual allocation makes the model exchange process difficult, as the model may not run seamlessly on the real-time simulator configuration of other organizations and would require manual modifications. It is recommended that auto-allocation of processing power is chosen – a default setting within most real-time simulators.

In this case study, multiple processors or simulator racks could be utilised to run the network simulation at the PNDC. However, this requires the use of travelling wave transmission line or cable models to split the overall model into subsystems. This process can be manually intensive and presents challenges if there are no lines already present in the model in locations that naturally split the model into equal portions from a processing requirement point of view. As an alternative, the Chaplecorss network model developed using NovaCor is fragmented into smaller segments for each scenario to run on the allocated PB5 RTDS racks at the PNDC.

5.2. PHIL Time Delay Compensation

Time delay is a critical determinant of the stability and accuracy of any PHIL experiment. The exchange of signals between multiple units in a closed loop PHIL configuration presents variability, most often compensated as an average value. This presents an opportunity for more precise time delay compensation methods to be developed that can be utilized to support testing of novel functionalities to support realization of a net-zero power and energy system.

5.3. Internal vs. External Control Implementation of PHIL-Control

The grid-forming converter control in PHIL can be implemented either directly in the external hardware (e.g., triphase) based on internal and scaled down measurements from the network and using the hardware control board, or internally in RTDS side based on the simulated network. In the latter case, the controller output is sent to the hardware converter to drive its components, and the physical output voltage is then sent back to the RTDS network. Table 2 summarizes highl-level advantages and limitations of both options as observed from this work.

Table 2: High-level PHIL Control Approaches Comparison

	Perceived Advantages	Perceived Limitations
Hardware Control	- Direct consideration of hardware filter dynamics with internal measurements. - Direct control implementation on the target hardware board.	- Requires access to higher number of scaled control measurements from the simulated network (e.g., for synchronization). - More prone to variable delays.
RTDS Control	- Direct access to all control measurements in simulated network. - Direct time delay compensation for the control.	- Indirect consideration to hardware GFC filter measurements (requires additional measurement points).

5.4. Fiber vs. Copper Wire for Signal Exchange

Most real-time simulators offer two types of I/O interfaces for the exchange of signals with the power amplifier: (i) typical copper wire for analogue signal transmission or (ii) transmission through fiber using Aurora protocol, a serial protocol dedicated to high-speed point-to-point communication. The signals transmitted through copper wire analogue transmission presents more noise than fiber-based communication as shown in Figure 14. The noise in the signal can cause issues with the implementation of control and its performance. Employing a low pass filter with a high cut-off frequency is typically adopted to mitigate the issue. In this PHIL case study, random frequency jumps were observed when using copper wire transmission, which resulted in consequent jumps in measured power. These jumps were eliminated when fiber transmission was used instead. Thus, signal exchange over fiber is preferable when possible.

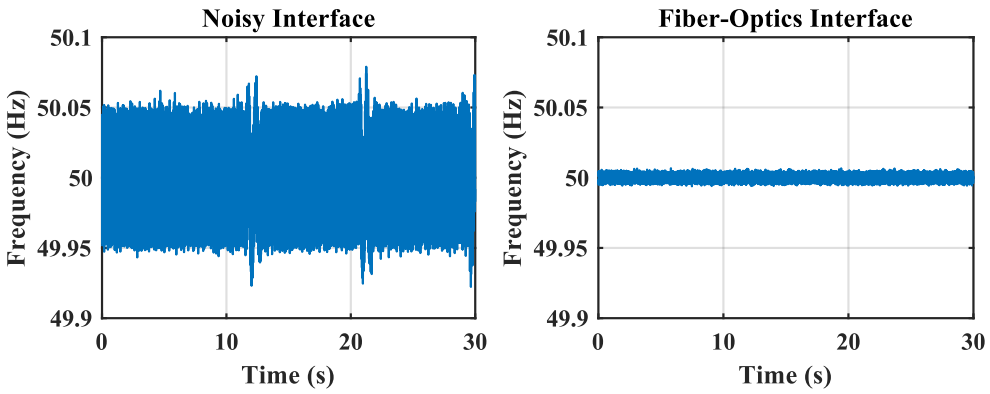

Figure 14: Frequency behaviors of the voltage signals transmitted by (a) copper wires (b) fiber link.

5.5. Impact of Numerical Models and Their Sensitivity to Signal Variations

PHIL interfaces hardware and software components to form a combined network. The simulated network model in RSCAD is discretized and numerical in nature, meaning that components are represented using a set of mathematical discrete equations and approximations.

Power transformers inrush currents are correlated to core flux values in most power system simulators, and the flux is estimated by integrating the winding voltages. Small mismatches introduced by analogue to digital

conversion can thus lead to creating an offset which can influence the flux integrator, thus overestimating the resulting inrush current.

This was observed in the present PHIL study when input transformer voltages had a non-zero variable average creating a less than 0.2% offset, which this was sufficient to produce 20 times the steady-state peak converter current (700-800 A instead of 39 A peak). On the shorter term a solution is devised based on signal processing to compensate the offset by subtracting the moving average from the received voltage, restoring the PHIL magnetizing current to its nominal range (see Figure 15). Further investigation is recommended to provide more insights on the sources and remedies of this phenomenon.

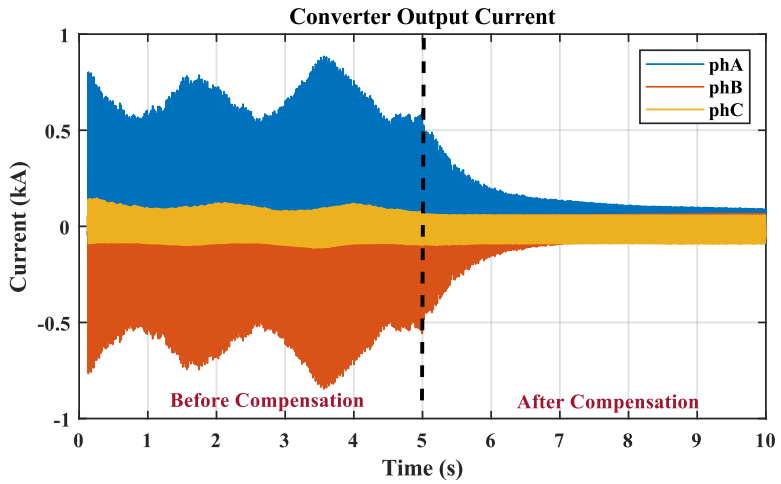

Figure 15: Comparison between magnetizing current before and after A/D impact compensation on input voltage.

6. Remarks

This report presented simulations and power hardware in the loop (PHIL) results of grid forming converters (GFC) used for black-start applications. Simulation results using RSCAD software were first used to successfully validate the model behavior for a similar network as the one implemented in MATLAB/Simulink in WP2 report. Then, an RSCAD model for Chaplecross network developed by National HVDC center was used to test black-start of a network segment, replacing Steven Crofts generator with an average model GFC. Simulation results show that using hard energization with 0.8, 0, -0.8 pu residual flux in the 11/33 kV and 33/132 kV transformers phases resulted in excessive inrush currents beyond the transformer rating under voltage and current control scenarios. Soft energization with a 10 seconds ramp, on the other hand, was observed to significantly reduce inrush currents, even when energizing both main transformers and the earthing transformers simultaneously. Grid synchronization using a modified control was also tested and successful connection to the 132 kV simulated grid was achieved under different scenarios. Notably, varying the network model assumptions could influence the reported quantified results. Though, the observed soft energization impact remains valid.

PHIL hardware-software interface technique was also tested with the aim to investigate its capabilities and understand its challenges and limitations. Current Ideal Transformer Method (I-ITM) was used for the interface at the DPSL. Stable closed-loop operation was observed when using the simplified RSCAD network model for black-start in terms of soft energizing the simulated transformer and picking up simulated load, however with tracking mismatches for the hardware current when low current references are applied. Further investigation is planned first to validate stable operation of grid synchronization in closed-loop PHIL for the simplified network and to investigate different control implementation options, in addition to transformer energization. Then, it is planned to expand the PHIL technique investigation into Chaplecross network elements at the PNDC, where work is currently ongoing by the PNDC team to validate the hardware converters and RTDS units' readiness at the facility for these tests.

The presented and planned studies are among the first trials to test GFC operation for black-start with PHIL techniques. The lessons learned so far present interesting opportunities to be explored in terms of improving the GFC-PHIL interface, and the GFC control robustness in response to practical network conditions and variations. Collectively, the outcomes of this project should contribute to answering the question of the added-benefits from using PHIL as a complementary tool to pure simulations in validating novel functionalities of power electronic devices.

7. Relevant Publications

[1] A. Alassi, K. Ahmed, A. Egea-Àlvarez, and O. Ellabban, "Innovative Energy Management System for MVDC Networks with Black-Start Capabilities," Energies, vol. 14, no. 8, 2021.

[2] Z. Feng et al., "A Scheme to Improve the Stability and Accuracy of Power Hardware-in-the-Loop Simulation," in IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society, 18-21 Oct. 2020 2020, pp. 5027-5032.

[3] A. Alassi, K. Ahmed, A. Egea-Alvarez, and C. Foote, "Soft Transformer Energization: Ramping Time Estimation Method for Inrush Current Mitigation," in 2021 56th UPEC Conference, 31 Aug.-3 Sept. 2021 2021, pp. 1-6.

[4] A. Alassi, K. Ahmed, A. Egea-Alvarez, and C. Foote, "Modified Grid-forming Converter Control for Black-Start and Grid-Synchronization Applications," in 2021 56th UPEC Conference, 31 Aug.-3 Sept. 2021 2021, pp. 1-5..

[5] M. H. Syed, E. Guillo-Sansano, S. M. Blair, A. Avras, and G. M. Burt, "Synchronous reference frame interface for geographically distributed real-time simulations," IET Generation, Transmission & Distribution, https://doi.org/10.1049/iet-gtd.2020.0441 vol. 14, no. 23, pp. 5428-5438, 2020/12/01 2020.