

Solution-Processed High-Performance ZnO Nano-FETs Fabricated with Direct-Write Electron-Beam-Lithography-Based Top-Down Route

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Zinc oxide (ZnO) has been extensively investigated for use in large-area electronics; in particular, the solution-processing routes have shown increasing promise towards low-cost fabrication. However, top-down fabrication approaches with nanoscale resolution, towards aggressively scaled device platforms, are still underexplored. This study reports a novel approach of direct-write electron-beam lithography (DW-EBL) of solution precursors as negative tone resists, followed by optimal precursor processing to fabricate micron/nano-field-effect transistors (FETs). It is demonstrated that the mobility and current density of ZnO FETs can be increased by two orders of magnitude as the precursor pattern width is decreased from 50 μm to 100 nm. These nano-FET devices exhibit field-effect mobility exceeding $\approx 30 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and on-state current densities reaching 10 A m^{-1} , the highest reported so far for direct-write precursor-patterned nanoscale ZnO FETs. Using atomic force microscopy and parametric modeling, the origin of such device performance improvement is investigated. The findings emphasize the influence of pre-decomposition nanoscale precursor patterning on the grain morphology evolution in ZnO and, consequently, open up large-scale integration, and miniaturization opportunities for solution-processed, high-performance nanoscale oxide FETs.

1. Introduction

Over the past decades, oxide semiconductors have found widespread applications in flexible and transparent large-area electronics such as active-matrix display panels.^[1,2] In order to fabricate these devices, the primary focus has transitioned from investigating vacuum-based thin film deposition techniques towards a solution-based processing approach as a cheaper alternative. Regardless of the deposition technique employed, micro-n-scale patterning of the active oxide channel layer using top-down techniques has been an inevitable step in large-scale integration of these devices, primarily to achieve device isolation^[3] as well as for suppressing gate leakage current by decreasing the overlap area between gate and source/drain electrodes.^[4,5] However, achieving nanoscale resolution in oxide patterning using wet etching techniques has proven very challenging,^[5]

on account of the difficulty in controlling the delamination during the lift-off processing. Among different oxide semiconductors being investigated for electronic device applications, zinc oxide (ZnO) is the most intensively studied. In particular, ZnO nanostructures exhibit a plethora of functional applications such as field-effect transistors (FET),^[6–20] gas sensors,^[21–24] photovoltaics,^[25,26] UV photodetectors,^[27–29] nonvolatile memories,^[6,19,30] and piezoelectric generators.^[24,26,31] While bottom-up growth is the most commonly used method for fabricating the ZnO nanowires, the devices fabricated using these bottom-up grown nanostructures lack positional control in device fabrication that limits overall large-scale integration. Hence, in order to make fabrication of devices completely compatible with complementary metal oxide semiconductor (CMOS) process flow, an increasing number of top-down approaches are being investigated in recent years.

Most conventional top-down patterning techniques depend on liftoff,^[32] wet etching,^[5,33] or reactive ion etching (RIE).^[34,35] In addition, techniques like nanoscale spacer lithography (NSL) that involve atomic layer deposition and directional reactive ion etching have also been utilized for fabricating ZnO nanowire-based FETs^[17,36,37] and gas sensors.^[38] However, etching-based techniques often lead to detrimental effects on

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device performance by damaging the oxide channel layer.^[33] In addition, resist residues left after the stripping process are expected to cause deterioration of the oxide semiconductor interface. Cho et al. have thus recently reported a modified wet-chemical-etching processes to increase the durability of the oxide channel.^[5]

In recent years, direct-write patterning of sol-gel precursors has been investigated as a cost-effective alternative to vacuum-based techniques for fabricating metal-oxide channel in FET devices. Direct-write patterning has several marked benefits over conventional processing, primarily requiring fewer steps in fabrication flow while attaining precise positional control in device placement. Furthermore, direct patterning of oxide semiconductors evades photoresist residue as well as degradation of the channel layer during etching steps. In addition, direct-write patterning is easier to implement for synthesizing nanoscale oxide structures. In this direction, thermal nanoimprint lithography (NIL)-based direct patterning of ZnO precursor layer has also been previously reported.^[39,40] Moreover, modifying ZnO precursor with photosensitizer 2-nitrobenzaldehyde^[41,42] or dispersing ZnO nanoparticles into photosensitive agents^[43] has also been studied for UV-NIL. Similarly, nanopattern templates have also been utilized for fabricating ZnO nanopatterns by vapor-phase infiltration synthesis of zinc ALD precursor into block copolymer templates^[44,45] and in electron-beam lithography (EBL) nanopatterned SU-8.^[27,45]

Direct-write patterning of sol-gel precursors for the fabrication of micro/nanoscale oxide structures is being increasingly utilized for making FETs and high-density device arrays. This includes strategies like using benzoylacetone or acetylacetone along with acids or bases as additives for fabricating metal oxide devices.^[4,46,47] Similarly precursors based on acrylate such as zinc methacrylate^[48,49] and zinc diacrylate^[50] have been exploited for synthesizing photopatterned oxide FETs. However, due to the inherent resolution limit of photolithography-based direct-write techniques, majority of nanoscale ZnO devices are

fabricated from routes utilizing EBL, soft-EBL,^[51,52] infiltration synthesis,^[27,53] and direct-write EBL.^[54-56] In addition to the conventional acrylate based precursors, other novel precursors such as zinc naphthenate (Zn(NPH)) and zinc neodecanoate (Zn(NDN)) are also explored for fabricating nanopatterns using EBL^[54,55] or direct-write extreme UV-interference lithography (EUV-IL).^[57] However, reports of ZnO nanowire FETs from these precursors are rather rare (one report by Jones et al. with Zn(NDN) precursor).^[56]

Towards this end, we have implemented an EBL-based direct-write approach to fabricate ZnO transistors with width varying from microns to nanometer scales. A detailed study is performed through extensive process optimization of bottom-gate-top-contact (BGTC) ZnO micro-FETs fabricated from Zn(NDN) and Zn(NPH) direct-write precursors. Subsequently, improvement in the device performance because of post-decomposition annealing of ZnO channel is demonstrated. Finally, upon scaling down ZnO channel width to nanoscale, a two orders of magnitude enhancement in the ZnO FET performance is reported and a comprehensive understanding of the charge transport in these nanostructured devices is developed based on structure-property correlation and parametric understanding of the trap dynamics.

2. Results and Discussion

2.1. Direct-Write Electron-Beam Lithography

The processing steps involved in the direct-write electron-beam lithography (DW-EBL)-based fabrication of ZnO micro/nanostructures is depicted in **Figure 1a**. In order to evaluate the lithographic performance of both the precursors (Zn(NDN) and Zn(NPH)) (structures shown in Figure 1b,c), an exposure dose matrix was generated as described in the Experimental Section. The extracted normalized resist pattern thickness for

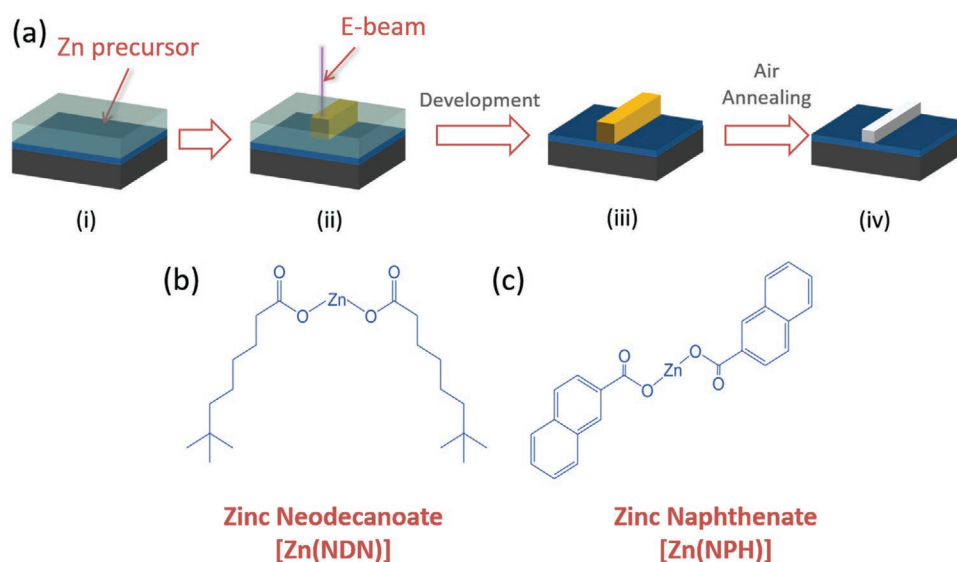


Figure 1. a) Schematic representation of direct writing of ZnO nanopatterns using EBL-based direct-write technique. Chemical structure of b) Zn(NDN) and c) Zn(NPH) molecule.

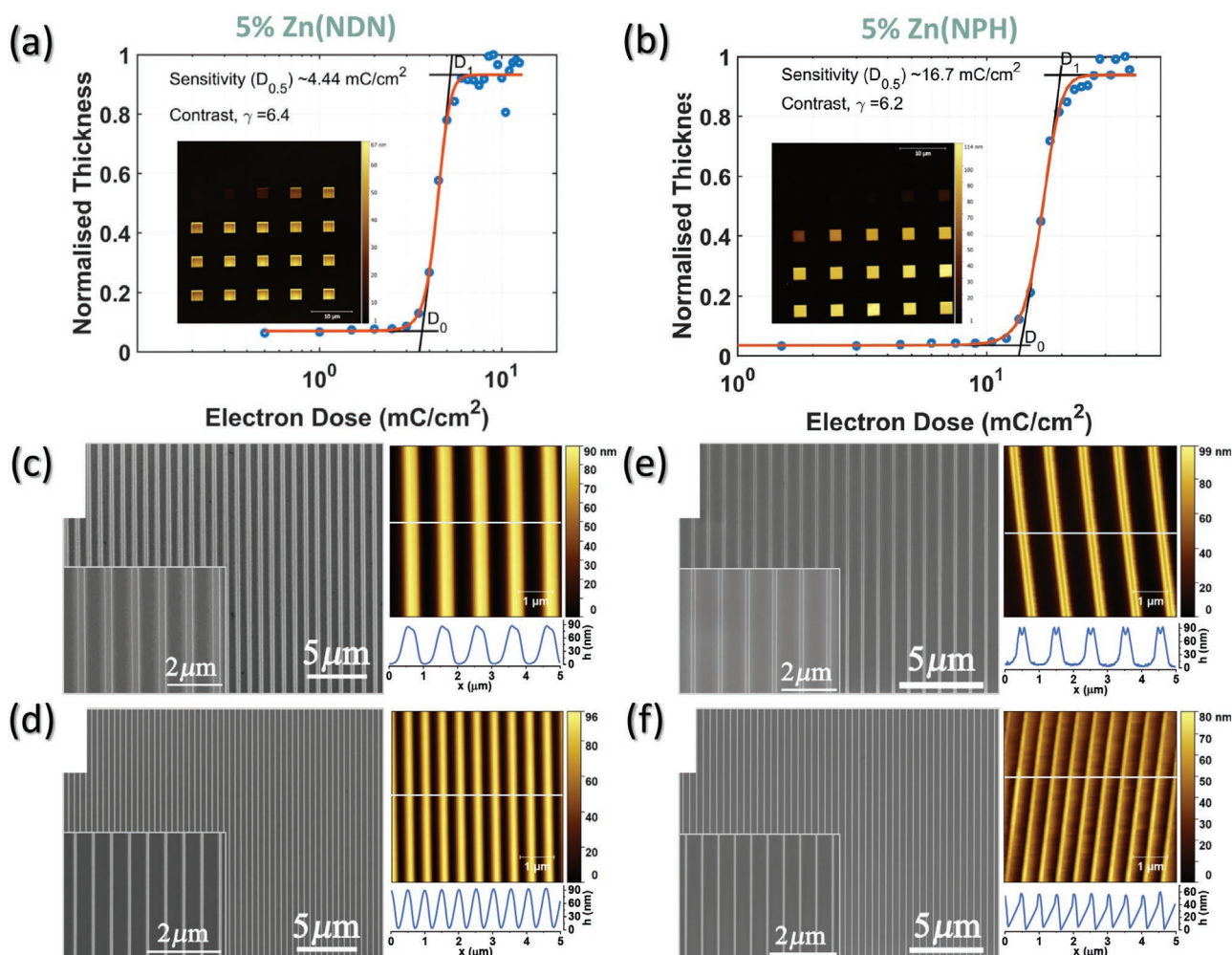


Figure 2. Electron-beam exposure dose–response curves for a) Zn(NDN) and b) Zn(NPH) based on post-development normalized resist height estimated using AFM and plotted against exposure dose. The insets show respective AFM topography images of 5×5 array of $2.5 \mu\text{m} \times 2.5 \mu\text{m}$ patterns exposed on 5% (0.136 M) precursor concentration with 1 nA current and 10 nm beam step. SEM micrographs and AFM topography images of ZnO nanoscale gratings DW-EBL patterned on 15% (0.407 M) Zn(NDN) thin film with c) 500 nm linewidth 1 μm pitch, d) 100 nm linewidth 500 nm pitch. SEM micrographs and AFM topography images of ZnO nanoscale gratings DW-EBL patterned on 25% (0.62 M) Zn(NPH) thin film with e) 500 nm linewidth and 1 μm pitch, f) 100 nm linewidth and 500 nm pitch. Gratings in (c–f) were imaged after converting into ZnO by annealing the DW-EBL patterned precursors at 500 °C for 1 h.

Zn(NDN) is plotted against the exposure dose in Figure 2a while the inset shows the acquired AFM topography profile. The resist sensitivity ($D_{0.5}$) of $\approx 4.4 \text{ mC cm}^{-2}$ and contrast (γ) of 6.4 was obtained from the sigmoidal fitting of the dose curve for thin films obtained with Zn(NDN) precursor. Similarly, the normalized resist thickness variation with exposure dose for Zn(NPH) was also modeled with sigmoidal fitting, as shown in Figure 2b. Inset depicts the AFM topography image that is used to extract the resist thickness corresponding to each exposure dose. It was found that the Zn(NPH), which contains aromatic rings in its chemical structure, exhibits slightly lower resist sensitivity ($D_{0.5}$) of $\approx 16.7 \text{ mC cm}^{-2}$ (requires higher exposure dose for crosslinking) and contrast, γ of 6.2. This difference in sensitivity between Zn(NDN) and Zn(NPH) can possibly be attributed to the inherent higher thermodynamic stability of aromatic structure in Zn(NPH) compared to the Zn(NDN) structure made up of aliphatic hydrocarbons. Thus, Zn(NDN)

requires less energy (here, electron dose) for free radical generation to initiate crosslinking (or free radical polymerization) of the monomers, thereby exhibiting better resist sensitivity. At the same time, it should be noted that both the resists exhibit comparable contrast, which solely depends on the solubility difference between the crosslinked (exposed) and un-crosslinked (unexposed) regions of the resists. In this case, we have used a mild solvent toluene as the negative tone developer that easily and selectively dissolves the un-crosslinked resist.

Grating-styled nanopatterns were then exposed using 15% (0.407 M) Zn(NDN) and 25% (0.62 M) Zn(NPH) films with 1 nA beam current and $600 \mu\text{m} \times 600 \mu\text{m}$ field size using a 10 nm beam step. This was followed by conversion to ZnO upon decomposition at 500 °C. For Zn(NDN), 50 lines of 500 nm linewidth and 25 μm length were obtained with 1 μm pitch and 100 lines of 100 nm linewidth and 25 μm length were exposed with 500 nm pitch using electron dose of 12.5 and 25 mC cm^{-2} ,

respectively. The resulting ZnO patterns after resist decomposition are shown in Figure 2c,d. Similar patterns were also fabricated on Zn(NPH) using an electron dose of 25 and 50 mC cm⁻², respectively and their images after conversion to ZnO are shown in Figure 2e,f. These grating patterns, useful for large area device and sensor arrays, illustrate the capability of obtaining high-density ZnO nanopatterning using DW-EBL from both the resist precursors.

2.2. Investigating Electronic Trap States in DW-EBL-Fabricated ZnO

Solution-processed films from both Zn(NDN) and Zn(NPH) precursors were spin coated (details in Experimental Section). Electron-beam-induced crosslinking was utilized over an area of 5 mm × 5 mm. In order to estimate the required temperature for decomposition of the precursors, thermogravimetric analysis (TGA) was performed on both Zn(NPH) and Zn(NDN) and the percentage weight loss with temperature is shown in Figure S1a,b, Supporting Information. Zn(NPH) shows complete decomposition at around ≈450 °C beyond which no mass loss was observed, which is consistent with previous reports.^[54,55] Similarly, for Zn(NDN), the decomposition completes around ≈375 °C. Accordingly, the decomposition temperature of 500 °C, well beyond the temperature at which both the precursors complete their decomposition, was chosen as

the temperature for processing the electron-beam crosslinked precursor films. Complete conversion to ZnO phase was ascertained using X-ray diffraction (XRD)-based structural analysis depicted in Figure S1c, Supporting Information.

The photoluminescence (PL) spectra acquired from the DW-EBL patterned ZnO area exhibited a sharp near band edge (NBE) peak corresponding to free exciton recombination process at ≈375–380 nm wavelength (Figure 3a), and broad peak corresponding to deep-level emission (450–750 nm) that is in agreement with the previous reports.^[58,59] Interestingly, the ratio of NBE emission to deep level emission is significantly improved (ratio ≈5.4 for Zn(NDN) and ≈3.5 for Zn(NPH) based ZnO) as compared with ZnO thin films (ratio ≈1) prepared using Zn(NDN) without electron-beam irradiation that can be correlated to the reduction of defects.^[60] Such reduction in the defects suggests higher quality of ZnO film formation after electron-beam irradiation and can be correlated with the densification of the precursor layer during crosslinking that is similar to the reported photoinduced densification in zinc methacrylate under DUV irradiation.^[49] Note that the NBE emission to deep level emission ratio is smaller for films prepared with Zn(NPH) precursor than the films prepared with Zn(NDN), despite the fact that the final DW-EBL patterned ZnO film thickness was nearly the same (≈45 nm) by using 15% (0.407 M) Zn(NDN) and 25% (0.62 M) Zn(NPH). The difference in the NBE emission, however, can be attributed to the decomposition temperature difference of the two precursors. It is highly plausible that

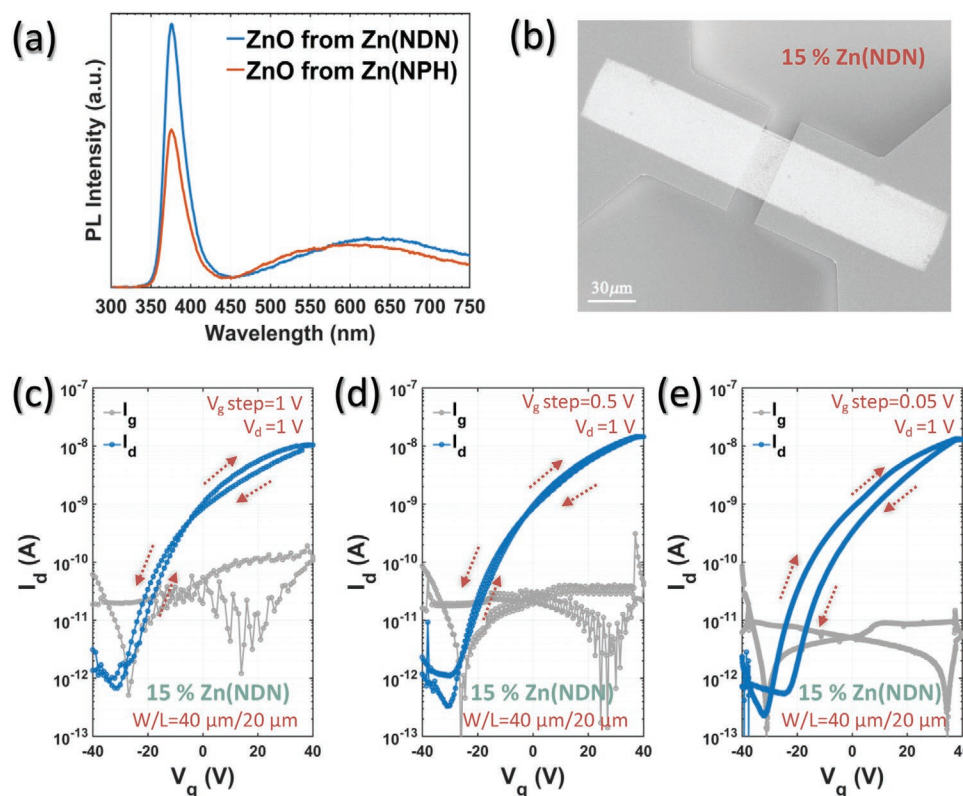


Figure 3. a) PL spectra of ZnO films prepared from EBL-patterned 15% (0.407 M) Zn(NDN) and 25% (0.62 M) Zn(NPH) after annealing at 500 °C for 1 h. b) SEM image of a micro-ZnO FET fabricated from Zn(NDN). Transfer curves measured on the same bottom gate top contact ZnO FETs ($W = 40 \mu\text{m}$, $L = 20 \mu\text{m}$) fabricated from Zn(NDN) precursor upon varying the gate voltage sweep step c) 1 V, d) 0.5 V, and e) 0.05 V under ambient condition.

the Zn(NPH) requiring higher decomposition temperature (≈ 450 °C) in comparison to Zn(NDN) (≈ 375 °C) might possess higher amount of residual carbon content when annealed at same temperature of 500 °C, thus quenching its PL. Nonetheless, based on this evidence, annealing temperature of 500 °C was regarded as suitable temperature to decompose the precursors and to obtain optimized ZnO required for further device fabrication and electrical characterization.

To investigate the electronically active traps, present within the ZnO films prepared from DW-EBL patterning, transfer characteristics on bottom gated top contact of BGTC (SEM image shown in Figure 3b) ZnO micro-FETs ($W/L = 40$ $\mu\text{m}/20$ μm) were acquired at different gate voltage sweep rate. Upon decreasing the gate voltage sweep step size from 1 to 0.05 V, the transfer characteristics under ambient conditions consistently exhibit an increase in hysteresis (Figure 3c–e). This observation points to the existence of deep level traps, which are generally activated at slower voltage sweep rates. To further obtain a molecular understanding on the origin of the deep level traps, we performed similar measurement while these ZnO micro-FETs were exposed to different ambient conditions (details in Experimental Section). Particularly, longer channel length (as shown in Figure 3b) was utilized for this set of device measurement in order to bring out the effect of the interaction between the ZnO channel and the environment. Note that the hysteresis observed for ZnO micro-FETs when the transfer characteristics are measured at a smaller step size (0.05 V) decreases significantly (Figure S2, Supporting Information) when the devices are measured under vacuum environment ($\approx 10^{-3}$ mbar). Furthermore, the $I_{\text{ON}}/I_{\text{OFF}}$ ratio of $\approx 10^4$ in ambient air decreased to $\approx 10^2$ in vacuum, due to the two orders of magnitude increase in the off current. From the above set of measurements, hysteresis in ambient air condition can be attributed to the spontaneous adsorption of oxygen and/or

water molecules on the ZnO surface that traps conduction electrons to surface states and depleting the surface mobile charge carriers.^[27] However, when ZnO devices are in vacuum environment, desorption of these species releases surface-trapped electrons charge carriers and thereby increases the off current. In the on state, however, the carriers generated due to gate action (accumulation at the gate–semiconductor interface) dominate the transport and hence similar channel current is observed for transfer characteristics measured for devices under ambient or vacuum conditions. Similar measurements performed on FETs with parylene C coated on top did not exhibit a significant variation of transfer characteristics hysteresis with the change in the gate voltage step size (Figure S3, Supporting Information). This can be attributed to the passivation of the ZnO surface minimizing adsorption of oxygen/water molecule species.

2.3. Optimization of ZnO Micro-FETs

In order to establish the optimal concentration for both the precursors, Zn(NDN) and Zn(NPH), a number of BGTC ZnO micro-FETs were prepared at different concentration. Figure 4a depicts the SEM micrograph of a typical micro-FET with Al-source and drain electrodes (on left) along with a high-magnification image showing polycrystalline nature of the ZnO micropattern. AFM measurements (Figures S4 and S5, Supporting Information) performed on DW-EBL-patterned ZnO fabricated with different precursor concentrations exhibit a marginal increase in the grain size from 20.4 nm for 5% (0.136 M) Zn(NDN) to 24.8 nm for 25% (0.678 M) Zn(NDN) and from 16.8 nm for 5% (0.124 M) Zn(NPH) to 20.2 nm for 25% (0.62 M) Zn(NPH) (Figure 4b) while the thickness of the ZnO thin films increased from 21.9 nm for 5% (0.136 M) Zn(NDN) to 77.9 nm for 25% (0.678 M) Zn(NDN), but increased

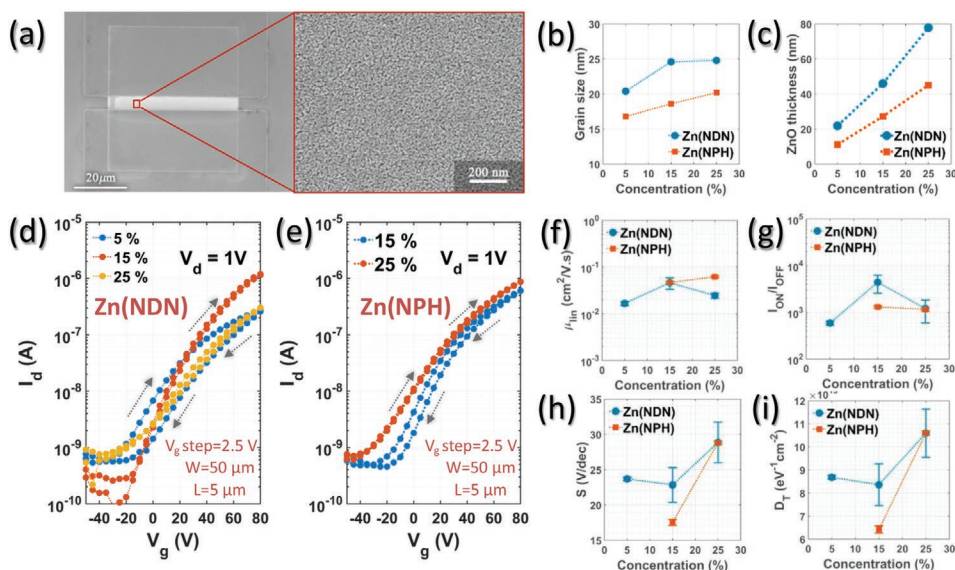


Figure 4. a) SEM micrograph of a ZnO micro-FET ($W/L = 50$ $\mu\text{m}/5$ μm) fabricated using 15% (0.407 M) Zn(NDN) (left) and high-magnification SEM micrograph of the channel region (right). ZnO grain size b) and thickness c) estimated from AFM scans on DW-EBL patterned ZnO films obtained from different concentrations of precursors. Transfer curves of ZnO micro-FETs fabricated using different precursor concentrations of d) Zn(NDN) and e) Zn(NPH). Variation in f) linear mobility, g) on/off ratio, and h) subthreshold swing. i) Interface trap density with precursor concentration.

from 11.9 nm for 5% (0.124 M) Zn(NPH) to 45 nm for 25% (0.62 M) Zn(NPH) (Figure 4c). In comparison, to the grain sizes reported in ZnO thin films prepared using acetate or nitrate precursors (grain size ≈ 40 nm),^[61–63] the morphology of our DW-EBL patterned micro-ZnO regions exhibits rather smaller grain size (≈ 17 – 25 nm), which is marginally higher than the ZnO thin films prepared using Zn(NDN) without electron-beam exposure (≈ 10 – 12 nm).^[60] This difference in grain size can be attributed to the lower metal content and higher decomposition temperatures of Zn(NDN) and Zn(NPH) compared to zinc acetate and zinc nitrate.

Typical transfer characteristics acquired from FETs fabricated with different concentrations of Zn(NDN) and Zn(NPH) is shown in Figure 4d,e. It was observed that the FETs fabricated from 5% (0.136 M) Zn(NDN) exhibited hysteresis that decreases upon increasing the concentration. Note that the device with highest ON current was observed for the FETs fabricated with 15% (0.407 M) Zn(NDN). Interestingly, when the precursor concentration was increased to 25% (0.678 M) Zn(NDN), a slight degradation in the device performance was observed, which can be attributed to the fact that, while the film thickness was increased to 779 nm, the grain size remained nearly the same (≈ 24.6 nm). Such huge difference in the thickness and grain size could point towards porosity within the film, in agreement with the AFM measurement (Figure S4c, Supporting Information). The presence of such porosity and the large surface-area-to-volume-ratio of the ZnO grains may lead to increased amount of chemisorbed oxygen, effectively depleting the charge carriers and decreasing the FET current. In contrast to Zn(NDN), no working transistors were obtained for ZnO FETs fabricated from 5% (0.124 M) Zn(NPH) precursor. This trend can be associated to the insufficient percolation in the channel region for ultrathin ZnO layers fabricated from precursors with bulkier organic groups, or in other words, lower Zn content.^[44] Nevertheless, upon increasing the Zn(NPH) precursor concentration to 15% (0.371 M), a field-effect modulation was observed in the ZnO FETs, with a further improvement in the transfer characteristics for 25% (0.62 M) Zn(NPH) (Figure 4e). This increase in the channel current and suppression of hysteresis upon increasing the precursor concentration in general can be correlated to the increase in conduction pathways that occurs due the improvement of the ZnO film quality. Consistently, the output curves for FETs fabricated with different precursor concentration exhibit an increase in channel current with concentration specifically for devices fabricated with Zn(NPH) precursors (Figure S6, Supporting Information). The output curves exhibit linear I - V characteristics at lower drain voltages, whereas a small deviation towards nonlinearity is noticed at higher drain voltage possibly due to charge crowding/saturation like behavior. In addition, output curves measured at low V_g ($V_g < 30$ V) exhibit a concave shape that is a typical characteristic of injection barrier formed at the metal–semiconductor interface despite the usage of low work-function Al as the S-D electrode in our devices. However, when gate voltage is increased ($V_g > 30$ V), sufficient charge carrier density is induced mitigating the effect of such local injection barriers.

FET characterization on a number of devices was carried out and calculated average values of the transistor performance parameters are summarized in Figure 4f–i. The

error bars indicate the standard deviation in the measured parameters performed on five devices. Devices prepared with 15% (0.407 M) Zn(NDN) and 25% (0.62 M) Zn(NPH) concentration exhibited highest value of average linear mobility (μ_{FET}). The mobility value increased from 1.67×10^{-2} to 4.86×10^{-2} $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ when Zn(NDN) precursor concentration was increased from 5% (0.136 M) to 15% (0.407 M). However, when the precursor concentration was further increased from 15% to 25%, a marginal decrease in mobility was observed. This observed variation in μ_{FET} with precursor concentration is consistent with the grain size variation (Figure 4b) and the estimated trap DOS. Our observation indicates that the best transistor performance corresponds to a sub-threshold swing of ≈ 19.8 V dec^{-1} and traps density of states $\approx 7.2 \times 10^{13}$ $\text{eV}^{-1} \text{cm}^{-2}$. Interestingly, the μ_{FET} variation with precursor concentration was less prominent than the previously reported ZnO thin film transistor devices fabricated from Zn(NDN) precursors where the fabrication process only involved spin casting followed by decomposition and no exposure to electron-beam irradiation.^[60] The densification of the precursor due to electron-beam irradiation is most probably the cause of good transistor performance even for FETs fabricated from 5% (0.136 M) Zn(NDN). Such a densification of zinc methacrylate precursor due to DUV irradiation has been previously reported by Yeh et al.^[49] In the case of Zn(NPH), devices fabricated from both 15% and 25% precursor solution exhibited $I_{\text{ON}}/I_{\text{OFF}}$ ratio of $\approx 10^3$, whereas the average μ_{FET} increased from 4.67×10^{-2} to 6.18×10^{-2} $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ as precursor concentration was increased from 15% to 25%. This mobility variation is correlated to the grain growth kinetics and decrease in the effective grain boundary region.

2.4. Effect of Post-Decomposition Annealing under Different Atmosphere

As a next step towards enhancing the device performance, we performed 15 s Ar plasma treatment carried out at 10 mbar pressure and 100 W power in an Oxford ICP-RIE system on the DW-EBL patterned ZnO, before depositing the Al S-D electrode.^[9] The purpose of using such a plasma treatment was twofold. First, this treatment removes any possible resist residue left after the development (analogous to a descum). Second, in Ar-ion plasma, energetic Ar-ion bombardment during the plasma treatment induces preferential removal of the relatively light atoms from the surfaces of II–VI or III–V group semiconductors due to momentum transfer between the ions in the plasma and the atoms on the material surface of the semiconductors.^[64] Consequently, transfer characteristics measured on ZnO FETs fabricated from Zn(NDN) precursor with Ar-plasma-treated contact electrodes exhibited an enhancement in $\mu_{\text{FET}} \approx 0.068$ $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ (Figure 5a) in comparison to the untreated contact electrode devices (0.0486 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$) discussed earlier in Figure 4d. We also performed a further step of “post-decomposition annealing” at 500 °C for 1 h under different atmospheres: 1) 100 sccm Ar flow and 2) 10 sccm flow of 5% H_2 in N_2 (forming gas) on the ZnO devices after initial decomposition of DW-EBL patterns to form ZnO channels. Representative transfer curves of FETs fabricated through

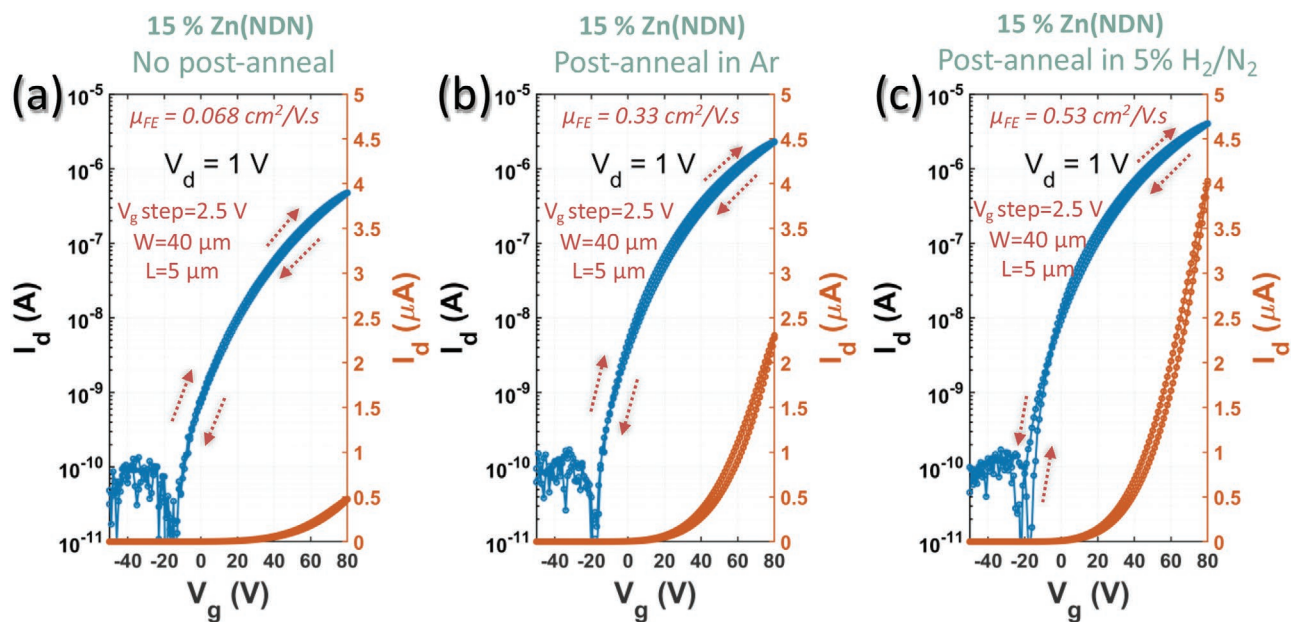


Figure 5. Transfer curves of ZnO micro-FETs ($W/L = 40 \mu\text{m}/5 \mu\text{m}$) fabricated using 15% (0.407 m) Zn(NDN) via DW-EBL patterning a) without any post-decomposition annealing; b) post-decomposition annealed at 500°C for 1 h under 100 sccm Ar and c) post-decomposition annealed at 500°C for 1 h under 10 sccm flow of 5% H_2 in N_2 (forming gas). The devices in this figure were subjected to 15 s Ar plasma treatment at 10 mbar pressure and 100 W power in an Oxford ICP-RIE system after photolithography patterning of the electrode regions and before Al metal deposition.

these post-decomposition processing are shown in Figure 5b,c. Devices post-decomposition annealed in Ar atmosphere (Figure 5b) displayed increased drain current with linear μ_{FET} reaching $0.33 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Similarly, devices post-decomposition annealed in forming gas (Figure 5c) demonstrated further increment in drain current with linear mobility rising up to $0.53 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Annealing of oxide semiconductors in Ar/forming gas atmosphere renders the surface of the ZnO slightly oxygen-deficient due to nonavailability of oxygen atmosphere, which decreases the possibility of AlO_x barrier layer formation, thereby enhancing the charge carrier injection at metal-semiconductor interface. Furthermore, annealing in different atmosphere has impact on bond rearrangement that passivates electronically active traps and vacancies or create interstitials that are effectively n-type dopants.^[65,66] The observed change in the transport properties can thus be attributed to the combination of these factors. This trend is consistent with the previous reports of enhancement in mobility of ZnO FETs when annealed in Ar or forming gas atmosphere.^[50,53,67] Nevertheless, we note that for ZnO based devices post-decomposition annealing plays a significant role in enhancing the field effect performance.

2.5. Scaling Down ZnO FETs to Nanoscale

After optimizing the micro-FETs, DW-EBL was further used to scale down the width of ZnO channels to 100 nm using the optimized processing condition obtained from micro-FET devices. To understand the evolution of device performance upon decreasing the width of the semiconducting layers, devices were fabricated from both 15% (0.407 m)

Zn(NDN) and 25% (0.62 m) Zn(NPH) precursors, which were the optimized precursor concentration obtained for the micro-FETs. Typical image of a direct write EBL scaled ZnO FET is depicted in Figure 6a,b. It was ensured that the channel length of the devices was maintained at $5 \mu\text{m}$ while the devices were scaled to the specific EBL patterned width dimensions ($40 \mu\text{m}$, 500 nm , and 100 nm). The transfer characteristics of typical bottom gated top contact ZnO devices fabricated from Zn(NDN) precursor using EBL patterning are depicted in Figure S7, Supporting Information. In order to illustrate increase in the current density with decreasing channel width, drain current was normalized by the device channel width that is presented in Figure 6c. Interestingly, we observe a clear enhancement in the device performance upon EBL scaling of the devices. ZnO FETs fabricated from Zn(NDN) with EBL width dimension of $40 \mu\text{m}$ exhibited linear μ_{FET} of $0.32 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ that increased to $3.6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ upon decreasing the device width to 500 nm . Furthermore, in the case of the 100 nm width device, another order of magnitude increment was observed in linear μ_{FET} with magnitude going up to a value of $33.7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.

A similar trend of mobility enhancement upon scaling down channel width through EBL is also observed in FETs fabricated from Zn(NPH) precursor (Figure S8, Supporting Information; Figure 6d). The estimated linear μ_{FET} increased from 0.1 to $21.4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ upon scaling the devices from $50 \mu\text{m}$ of 100 nm width. Note that we have used the gradual channel approximation for the estimating the mobility. Inherently, the edge effects due to fringing fields are neglected during this mobility calculation, which may lead to slight overestimation of the reported mobility. Majority of literature based on solution processed semiconductors have utilized

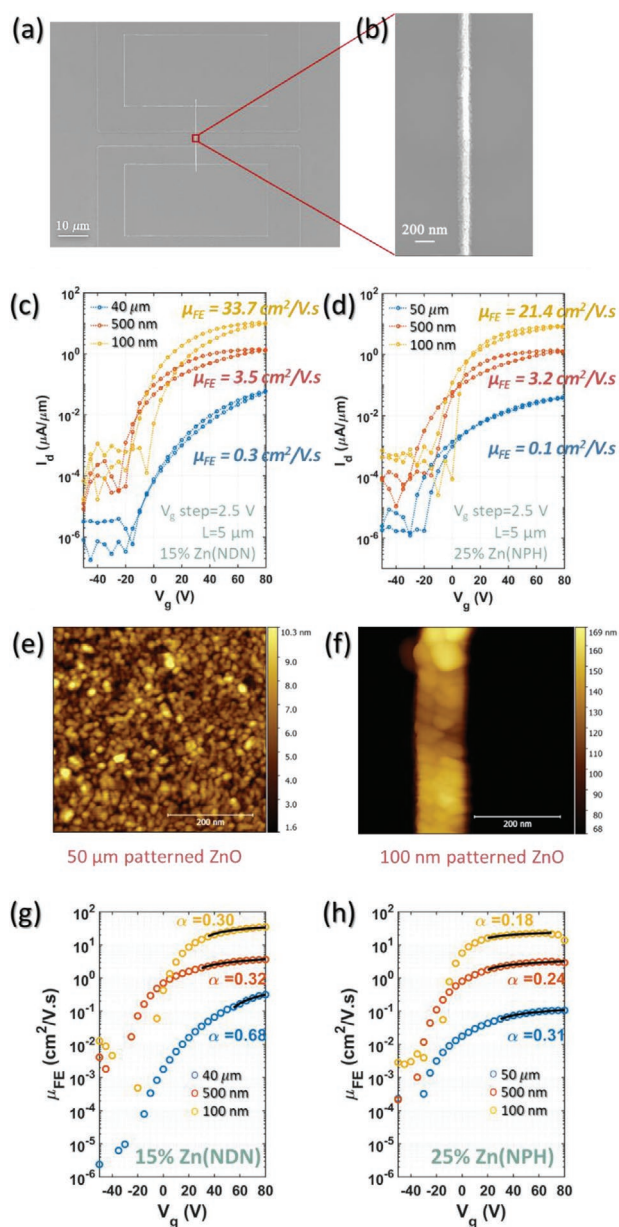


Figure 6. a) SEM micrograph depicting nano-ZnO FET fabricated from Zn(NDN) and b) high-magnification image of the corresponding ZnO nanochannel. Transfer curves (width normalized channel current) of the same ZnO FETs demonstrating enhancement in the device performance with decreasing DW-EBL patterned channel width prepared from c) Zn(NDN) and d) Zn(NPH). AFM topography images comparing the grain structure for e) 50 μm width and f) 100 nm width ZnO patterns, fabricated from Zn(NDN) at the optimized condition. Field-effect mobility versus gate voltage variation estimated from the above transfer characteristics of g) Zn(NDN) and h) Zn(NPH). The decrease in the value of α with decreasing pattern width signifies decrease in overall carrier transport deviating away from trap limited transport. All the devices in this figure were fabricated from 15% (0.407 M) Zn(NDN) and 25% (0.62 M) Zn(NPH), respectively.

the gradual channel approximation to estimate the mobility.^[46,48–50,63,68] Nevertheless, in Section S1, Supporting Information, we provide calculation of mobility upon correcting for

the fringe field that also yield similar degree of enhancement in mobility upon width scaling of the FETs. Furthermore, we have also plotted the width normalized transconductance (g_m) in Figure S9, Supporting Information, which also exhibits a trend indicating an increase in g_m by two orders of magnitude upon scaling the ZnO devices from 50 μm to 100 nm for both the precursors.

A comparison of different oxide FETs fabricated with direct-write techniques is provided in Table 1. These mobility values reported here are the best in field so far, among direct-write top-down fabricated ZnO FETs estimated through gradual channel approximation. It is also noteworthy that despite the polycrystalline morphology, our DW-EBL fabricated ZnO nanofETs exhibit performance similar to number of single crystalline unpassivated (characterized in air ambient) ZnO nanowire FETs.^[10,15,69] Despite the observed enhancement in the linear μ_{FET} , we observe an increase in the hysteresis of the transfer characteristics when the ZnO FETs were scaled from 40 μm to 100 nm (Figure 6c,d). This hysteresis can be attributed to gate induced oxygen adsorption on the ZnO surface accompanied by trapping of charge carriers at the surface states. As the width of the device is decreased, the surface area-to-volume ratio increases, leading to greater propensity for oxygen adsorption.

Next, we investigated the origin of this increase in mobility upon scaling down the devices. When broadly comparing with solution processed ZnO thin film TETs,^[60] similar to the micro-FETs discussed in the Section 2.3, the precursor densification by the electron-beam exposure very likely also aids in the case of nano-FETs. In addition, structural characterization based on the AFM analysis of the ZnO FETs with 50 μm and 100 nm width fabricated from 15% (0.407 M) Zn(NDN) is shown in Figure 6e,f. The 50 μm patterned ZnO (Figure 6e) exhibited smaller grain size ($\approx 20\text{--}24$ nm), which leads to the grain boundary scattering and limits the effective percolating-conduction pathways. In comparison, ZnO grains within 100 nm width device (Figure 6f) are not only larger (≈ 40 nm or bigger) but also much more tightly packed (interconnected grains).

An opposite trend of decreasing grain size with decreasing linewidth was reported among ZnO thin films obtained from soft-EBL-patterned zinc acetate.^[23,52,70] This may be explained by the fact that, contrary to DW-EBL method, the precursor by itself does not undergo electron-beam exposure in soft-EBL technique. Interestingly, the grain size in the ZnO nanopatterns prepared by soft-EBL-patterned zinc acetate is comparable to our DW-EBL ZnO when annealed at 900 $^\circ\text{C}$,^[52,70] but much smaller (≈ 8 nm) when annealed at 700 $^\circ\text{C}$.^[23] ZnO nanostructures fabricated by vapor phase infiltration of ZnO into nanopatterned SU-8 and rapid thermal annealing at 600 $^\circ\text{C}$ also exhibit much smaller grains ($\approx 2\text{--}4$ nm) than our DW-EBL ZnO nanostructures that indicate the efficacy of our technique and the choice of the precursor.

We have previously proposed that in case of polycrystalline ZnO thin film devices, the major source of deep level traps are the grain boundary depletion region.^[60] Due to the closely packed grains, the grain boundary region, and thus grain boundary scattering is greatly suppressed in 100 nm patterns, leading to higher electron mobility. Although the exact mechanism behind the grain evolution is not known, the difference in

Table 1. Comparison of different direct-write techniques reported and attained device performance.

Channel material	Precursor (patterning technique)	Patterned oxide linewidth (channel width)	Electron mobility [$\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$]	Channel width normalized mobility [$\text{cm} \text{V}^{-1} \text{s}^{-1}$]	ON current [μA]	Channel width normalized ON current [$\mu\text{A} \mu\text{m}^{-1}$]	Ref.
ZnO	Zinc acetate (PMMA soft-EBL)	$\approx 30 \text{ nm}$ (–)	–	–	–	–	[51,52]
InGaZnO	Zinc acetate+benzoylacetone-modified photolysis (UV lamp)	$>150 \mu\text{m}$ (1000 μm)	1.15	≈ 11.5	≈ 20	0.02	[4]
ZnSnO	Zinc acetate+benzoylacetone and acetylacetone (UV lamp 365 nm)	$\approx 5 \mu\text{m}$ (1000 μm)	0.03	≈ 0.3	≈ 10	0.01	[46]
InGaZnO	Zinc acetate+acetylacetone and NH_4OH complex (DUV 253.7 nm)	3 μm (1000 μm)	84.4	≈ 844	100	0.1	[47]
InGaZnO	Zinc methacrylate (DUV laser 193 nm)	300 nm (^a)50 \times 300 nm)	9.9	$\approx 6.6 \times 10^3$	1000	66.67	[48]
InZnO	Zinc diacrylate (DUV 254 nm)	$>40 \mu\text{m}$ (1000 μm)	0.853	8.53	50	0.05	[50]
ZnO	Zinc diacrylate (DUV 254 nm)	$>40 \mu\text{m}$ (1000 μm)	0.323	3.23	10	0.01	[50]
ZnO	Zinc methacrylate (DUV laser 193 nm)	300 nm (^a)50 \times 300 nm)	0.45	≈ 300	100	6.67	[49]
ZnO	Diethyl zinc+SU8 (EBL+infiltration synthesis)	$\approx 50 \text{ nm}$ (50 nm)	0.1	$\approx 2 \times 10^4$	0.12	2.4	[53]
ZnO	Zn(NDN)	$\approx 40 \mu\text{m}$ (40 μm)	0.3	75	2	0.05	This work
ZnO	Zn(NDN)	$\approx 500 \text{ nm}$ (500 nm)	3.5	7×10^4	0.5	1	This work
ZnO	Zn(NDN)	$\approx 100 \text{ nm}$ (100 nm)	33.7	3.37×10^6	≈ 1	≈ 10	This work
ZnO	Zn(NPH)	$\approx 100 \text{ nm}$ (100 nm)	21.4	2.14×10^6	≈ 0.9	≈ 9	This work
ZnO nanowire	CVD grown	$\approx 50\text{--}200 \text{ nm}$	$\approx 8\text{--}50^{\text{b}}$	$\approx 10^6$	≈ 1	≈ 10	[10,15,69]

^a)For the estimation, we have considered the number of nanowires to be 50, since the article did not clearly state number of nanowires per transistor device. Thus, effective channel width is considered as $50 \times 300 \text{ nm}$; ^b)While single-crystalline ZnO nanowire FETs with much higher mobility are also reported with passivation strategies, we have only included those with similar SiO_2 back-gate-based unpassivated examples.

grain structure may be attributed to a number of factors. First, higher surface-area-to-volume ratio in nanopatterns assists in efficient removal of organic components of the precursor during decomposition thereby improving the phase purity of the ZnO films. Second, the combination of factors originating from the unidirectional strain within the nanopattern and the slow ramping up/down of the temperature during the decomposition process provide driving force for lattice rearrangement leading to grain coalescence and densely packed bigger grains.^[70]

Furthermore, in order to envisage the effect of pattern widths on the carrier transport mode in these FETs, we employed an analytical power law-based model expressed as, $\mu_{\text{FE}} = K (V_g - V_{\text{th}})^\alpha$, where K and α are fitting parameters. The value of exponent α can be correlated to the underlying transport mechanism exhibited by the oxide channel. A value of α closer to 0.7 is indicative of trap limited charge (TLC) transport, whereas α value approaching 0.1 is an indication of decreased charge trapping and other transport mechanism such as percolation dominated conduction (PC) are dominant.^[60,68,71] Figure 6g,h illustrates the variation of μ_{FE} with V_g for devices fabricated

using Zn(NDN) and Zn(NPH) respectively. It can be seen that for both precursors, the value of α progressively decreases as the channel width is decreased, suggesting that the TLC transport is predominant in micro-FETs, whereas on decreasing patterned channel down to 100 nm, the effect of charge trapping on the carrier transport decreases that is reflected in higher field effect mobility.

Although, the high device performance achieved during this study has only been investigated for DW-EBL on particular precursors, it may be possible that such device performance enhancement is exhibited by rather broader set of solution precursors and oxide semiconductors. The key takeaway here is the nanoscale patterning of the solution precursors prior to decomposition into oxides. The morphological evolution similar to the one driving the performance improvement in our case has been previously shown in case of soft-EBL nanopatterned zinc acetate, wherein slow heating/cooling exhibited larger grains while rapid annealing resulted in smaller grains.^[23,70] It is incontrovertible that higher surface-area-to-volume ratio in nanopatterned precursors would facilitate

efficient removal of organic components. Furthermore, in the case of amorphous semiconductors, even if the morphological evolution similar to crystalline materials may not take place, increased performance has been shown in transistors based on amorphous semiconductors across the board, due to the densification caused by photonic curing.^[49,72] Therefore, the performance enhancement of DW-EBL processed ZnO nano-FETs reported here may spur interest in downscaling of precursor patterns to nanoscale, among solution processed oxide electronics across the board.

3. Conclusion

We have presented novel DW-EBL patterning schemes of solution precursors Zn(NDN) and Zn(NPH) for top-down synthesis of ZnO nanowires. After establishing the optimal exposure dose required to generate negative tone lithographic patterns using both the precursors, based on a sharp NBE peak and low defect emission in post-decomposition PL measurements, decomposition temperature of 500 °C was chosen for device processing. The micro-FETs fabricated with concentrations of 15% (0.407 M) Zn(NDN) and 25% (0.62 M) Zn(NPH) exhibited best performance and μ_{FET} of $\approx 0.05 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Upon shrinking the precursor pattern width down to 100 nm using both the precursors, an impeccable two orders of magnitude increment in μ_{FET} was achieved, with μ_{FET} reaching a value as high as $\approx 33.7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and on-state current densities reaching 10 A m^{-1} . AFM analysis revealed an increase in the grain size as well as improved grain packing in DW-EBL nanopatterned (100 nm) ZnO as plausible origin of the performance improvement, in coherence with decreased trap limited transport revealed through parametric modeling. Our results pave the way for nanoscale DW-EBL patterning of precursors as a CMOS process-flow-compatible strategy towards high-performance integrated oxide-based electronics.

4. Experimental Section

Precursor Preparation: Zn(NDN) (99%) ($MW \approx 407.9 \text{ g mol}^{-1}$; density $\approx 1.1 \text{ g cc}^{-1}$; chemical structure shown in Figure 1b) and Zn(NPH) ($\approx 67 \text{ wt\%}$ in mineral spirits) ($MW \approx 407.7 \text{ g mol}^{-1}$; density $\approx 1.01 \text{ g cc}^{-1}$; chemical structure shown in Figure 1c) were sourced from Alfa Aesar and diluted to the required concentration (v/v) using toluene (procured from Sigma-Aldrich) as a solvent (details of dilution are provided in Tables S1 and S2, Supporting Information, respectively). Zn(NPH) was readily dissolved by simply shaking the solution mixture, in the case of Zn(NDN), the precursor solution was subjected to ultrasonic agitation at 80 °C for 3 h to obtain a thoroughly dissolved solution. The vial was then allowed to cool down naturally. Once dissolved, the solution is stable for months.

Substrate Preparation: Boron-doped prime grade Si (100) p^{++} wafers with thermally grown SiO_2 (100 nm) were used throughout the study. Substrates sized 12 mm \times 12 mm were cleaved from 4" wafer. Substrates were cleaned in acetone and isopropyl alcohol for 10 min under ultrasonic agitation and blow dried with nitrogen gun. This was followed by submerging the substrates into a freshly made piranha solution (1:3 v/v mixture of H_2O_2 and H_2SO_4) for 15 min, followed by thorough rinse with HPLC grade deionized water and dried under nitrogen flow. Finally, 10 min oxygen plasma treatment and 200 °C hotplate baking was applied prior to precursor spin coating.

Electron-Beam Lithography: Five percent concentration solutions of each precursor was spin coated on cleaned substrates at 2000 rpm for 60 s. The electron-beam exposure was carried out using Crestec CABL-9000C system operating at 50 kV acceleration voltage. In order to characterize dose response of both DW-EBL precursors, a 5×5 array of $2.5 \mu\text{m}$ square pattern was exposed on resist film using 1 nA beam current and $600 \mu\text{m} \times 600 \mu\text{m}$ field size divided into 60000 dots (10 nm beam step). The electron exposure dose was varied from 1.5 up to 37.5 mC cm^{-2} in increments of 1.5 mC cm^{-2} for Zn(NPH), whereas dose variation from 0.5 up to 10 mC cm^{-2} in steps of 0.5 mC cm^{-2} . After 30 s development in toluene, the remaining heights of the resist patterns were characterized using AFM measurement.

The performance of both the resists was characterized by applying sigmoidal fitting model to the resist thickness variation with exposure dose plot. The resist sensitivity ($D_{0.5}$) was quantified as the exposure dose required to retain 50% resist height after development. The resist

contrast was estimated using expression, $\gamma = \frac{1}{\log_{10}\left(\frac{D_1}{D_0}\right)}$ where D_0 is

onset dose at which the resist starts to crosslink and D_1 is dose at which the entire thickness of the resist is crosslinked and rendered insoluble in developer.^[73–75]

Photoluminescence Characterization: For carrying out PL spectroscopy, $4.8 \text{ mm} \times 4.8 \text{ mm}$ area of the spin coated precursor films (obtained by using 15% (0.407 M) Zn(NDN) and 25% (0.62 M) Zn(NPH)) was subjected to electron-beam exposure (5 mC cm^{-2} for Zn(NDN) and 15 mC cm^{-2} for Zn(NPH)) using 100 nA beam current, $1200 \mu\text{m} \times 1200 \mu\text{m}$ exposure field with 60 nm step. Samples were then developed in toluene for 30 s and annealed for 1 h at 500 °C with a slow ramp rate of $10 \text{ }^\circ\text{C min}^{-1}$ to decompose the precursor and for overnight cool down. The as-fabricated thin films were excited using 266 nm laser incidence to obtain the PL.

Transistor Fabrication: Required concentration of specific precursors was spin coated on Si/SiO₂ substrates with prefabricated alignment markers. In order to fabricate micro-FETs, required regions were exposed with 20 nA beam current, $1200 \mu\text{m} \times 1200 \mu\text{m}$ exposure field with 60 nm step. An area exposure dose of 7.5 mC cm^{-2} was used for the exposure of Zn(NDN) precursor-based films, whereas 25 mC cm^{-2} exposure dose was used for Zn(NPH)-precursor-based thin films. After 30 s development in toluene and 1 h decomposition annealing at 500 °C, 100 nm Al source/drain electrodes were patterned to fabricate micro-FETs with $L = 5 \mu\text{m}$ and $W = 40 \mu\text{m}/50 \mu\text{m}$ using photolithography process as reported previously.^[60]

In order to study the evolution of device performance upon decreasing width, devices were fabricated with 15% (0.407 M) Zn(NDN) and 25% (0.62 M) Zn(NPH). The precursor patterning was carried out in two steps. First, microscale patterns, for both microdevices and charge injection pads for nanodevices, were patterned using a 20 nA current and $1200 \mu\text{m} \times 1200 \mu\text{m}$ field with 60 nm steps. The samples with Zn(NDN) were subjected to an area dose of 10 mC cm^{-2} while Zn(NPH) samples were exposed with a 15 mC cm^{-2} dose. During the second exposure step, nanoscale patterns were exposed with a 1 nA current in order to get smaller beam diameter. A field size of $600 \mu\text{m} \times 600 \mu\text{m}$ was used for exposure with 10 nm step size. The corresponding nanochannel regions were exposed to a 100 mC cm^{-2} dose for both the precursors. The samples were then subjected to optimized annealing conditions, including 1 h forming gas post-decomposition-anneal and source/drain electrode fabrication was carried out to achieve 5 μm channel length in the same manner as micro-FETs. A brief 15 s Ar plasma treatment was carried out at 10 mbar pressure and 100 W power in an Oxford ICP-RIE system after photolithography step and prior to Al metal deposition for devices specified in Sections 2.4 and 2.5).

Electrical Characterization: The electrical characterization of all the FETs was conducted using SUSS MicroTec Probe station, unless otherwise stated, and Keithley 4200 SCS under ambient air conditions at room temperature in dark. Linear mobility of the FET devices was calculated using expression: $\mu_{\text{lin}} = \frac{L}{V_d W C_0} \frac{\partial I_d}{\partial V_g}$ where L and W represent channel length and width, respectively, C_0 is an oxide capacitance per

unit area, I_d is the drain current, V_g is the gate-source voltage, and V_d is the drain-source voltage. Considering the 100 nm thick SiO₂ gate oxide and relative dielectric constant (ϵ_r) of 3.9, C_0 was estimated to be 3.5×10^{-8} F cm⁻². Subthreshold swing was calculated using the expression $S = \frac{\partial V_g}{\partial \log I_d}$. The trap concentration per unit energy (D_T) was also calculated using the following expressions: $D_T = \frac{C_0}{e^2} \left(\frac{eS}{k_b T \ln 10} - 1 \right)$ where C_0 is the capacitance per unit area, S is the subthreshold swing, k_b is the Boltzmann constant, T is the temperature of the measurement, and e is the electronic charge.^[76,77]

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Research data are not shared.

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