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ADVANCED MEMORIES TO OVERCOME THE FLASH MEMORY WEAKNESSES: A RADIATION VIEWPOINT RELIABILITY STUDY

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In memory of Mew, my beloved friend.

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Introduzione

Le memorie non volatili sono uno degli elementi chiave per quasi ogni sistema digitale moderno. Inizialmente esse erano concepite quasi esclusivamente per memorizzare il codice (firmware) che viene eseguito dall'unità centrale di processo. Tuttavia, negli ultimi 10 anni, le memorie non volatili si sono diffuse esponenzialmente anche in applicazioni che prima erano a loro precluse: la memorizzazione di grandi quantità di dati. Infatti, solo di recente le memorie non volatili hanno raggiunto densità tali da permettere un loro utilizzo anche come dispositivi di memorizzazione di massa. Si sono quindi diffusi lettori multimediali, fotocamere digitali, schede di memoria, palmari, solid state drives, ecc… cioè, dispositivi che gestiscono e richiedono sempre maggiori quantitativi di memoria.

La maggior parte delle memorie non volatili avanzate è costituita dalle memorie Flash, basate su transistor a gate flottante. Per far fronte alle crescenti richieste del mercato in termini di densità di memoria, le dimensioni della cella elementare sono state ridotte esponenzialmente. Tuttavia, recentemente ci si sta avvicinando al limite tecnologico del transistor a floating gate. Per questo motivo, varie alternative sono in fase più o meno avanzata di studio o, addirittura, di commercializzazione. Le nuove memorie vengono comunemente chiamate memorie non volatili avanzate, o emergenti. Tra esse, si distinguono due grosse famiglie:

- Le memorie basate su intrappolamento di carica in siti discreti (nanocristalli o centri trappola di un dielettrico), che rappresentano un'evoluzione del transistor a gate flottante.
- Le memorie che associano l'informazione non più alla carica elettrica, ma ad esempio allo stato microstrutturale di un materiale (come le memorie a cambiamento di fase) o alla polarizzazione residua di un ferroelettrico (le memorie ferroelettriche).

Un altro problema delle memorie a gate flottante è la loro pessima resistenza alle radiazioni ionizzanti. Questo non è solo un problema limitato a ambiti di nicchia come quello militare, medico, scientifico, aerospaziale, ecc... Infatti, con la riduzione delle dimensioni della cella elementare, sempre meno elettroni sono confinati nel floating gate. Recenti stime, infatti, indicano che meno di 100 elettroni saranno immagazzinati nel floating gate a partire dal nodo tecnologico di 32 nm. Questo implica che anche una particella alfa è in grado di corrompere il dato memorizzato. Il problema delle particelle alfa è particolarmente sentito anche in ambito commerciale, poiché è impossibile azzerare la concentrazione di contaminanti alfa-emettitori nei materiali di incapsulamento (o anche nel silicio stesso). Inoltre, anche se esiste componentistica rad-hard (radiation-hardened, più resistente alle radiazioni), la recente tendenza delle industrie/istituti operanti in settori potenzialmente radioattivi è quella di utilizzare

componenti commerciali, molto più economici, reperibili e avanzati delle controparti radiation-hardened. Questo implica che, prima di utilizzare componenti commerciali, una loro qualificazione affidabilistica (in ambito radiation) deve essere effettuata. Da questo punto di vista, pochi sono stati gli studi degli effetti di radiazioni ionizzanti su memorie non volatili avanzate, anche se in linea di principio, molte di queste memorie potrebbero presentare livelli di tolleranza alle radiazioni di gran lunga migliore di quelli delle attuali memorie flash basate su transistor a gate flottante.

L'argomento di questa tesi di dottorato è rivolto allo studio affidabilistico delle memorie non volatili avanzate, dal punto di vista degli effetti delle radiazioni ionizzanti. In particolare, saranno considerate memorie a nanocristalli (una evoluzione naturale del transistor a gate flottante), le memorie a cambiamento di fase, e le memorie ferroelettriche.

La tesi si può suddividere in 2 grosse parti. La prima parte è costituita dai primi 3 capitoli, e fornisce alcune nozioni di base sugli argomenti relativi all'attività di ricerca: le memorie e gli effetti di radiazioni ionizzanti. La seconda parte contiene i risultati sperimentali e l'attività di ricerca svolta nel corso del dottorato. Essa comprende gli ultimi 5 capitoli e le quattro appendici, nelle quale sono riportati alcuni calcoli e le descrizioni di alcune apparecchiature sviluppate e costruite (non ritenuti essenziali ai fini della comprensione del lavoro sperimentale).

In particolare:

- Il capitolo 1 presenta le memorie Flash odierne e ne illustra i concetti principali.
- Il capitolo 2 offre una breve panoramica su alcune delle memorie non volatili avanzate attualmente studiate dalla comunità internazionale di ricerca scientifica.
- Il capitolo 3 fornisce delle nozioni di base sugli effetti di radiazione ionizzante, con riferimento particolare alle memorie Flash.
- Il capitolo 4 riporta alcune caratterizzazioni effettuate su dispositivi a nanocristalli.
- Il capitolo 5 mostra gli effetti di dose totale su memorie a nanocristalli, confrontandoli con esperimenti analoghi effettuati (sempre nel corso del dottorato) su celle di memoria a transistor flottante.
- Il capitolo 6 propone un'analisi dettagliata degli effetti di evento singolo su celle di memoria a nanocristalli.
- Il capitolo 7 analizza gli effetti di dose totale su array di memoria a cambiamento di fase.
- Il capitolo 8 riporta gli effetti di dose totale su memorie ferroelettriche, considerando anche l'effetto della temperatura.

Introduction

Nonvolatile memories are one of the key points of almost any digital system. They were initially conceived as firmware storage, i.e. to store the code executed by the central processing unit. However, in the last decade the nonvolatile memories also gained another important application: the mass data storage. In fact, only in the last decade the non volatile memories reached the memory density levels required for instance to store audio, images, video clips, etc. The availability of high density memories allowed the widespread of multimedia devices such as MP3 player, video players, palm-top PCs, etc.

The largest fraction of modern nonvolatile memories is represented by Flash memories based on the floating gate MOSFET. In order to increase the memory density, in the last years the elementary cell size has been scaled down exponentially. However, floating gate is facing several scaling issues due to intrinsic limits. For this reason, several alternatives are either being evaluated or even already commercially available. Those new memories are called advanced (or emerging) nonvolatile memories. All of them can be grouped in two large families:

- The memory based on charge trapping in discrete storage sites such as nanocrystals or trap centers.
- The memories, which do not associate the information to the electric charge. Instead they may store the information under the form of the microstructural state of a material (amorphous and polycrystalline, such as in phase change memories) or the remanent polarization in a ferroelectric (ferroelectric memories).

Another big issue of the floating gate memories is their very weak tolerance to ionizing radiation. This is not only an open issue for niche applications such as military, medic, scientific, aerospace, etc., but also it could severely endanger the reliability even in future consumer products. In fact, as the cell size is scaled down, the number of stored electron in the floating gate is reduced. It is calculated that from the 32-nm technological node, the number of electrons stored in the floating gate will fall below 100. This implies that even a single alpha particle could severely compromise the stored information. Alpha emitter contaminants cannot be completely eliminated in packaging materials (or even in bare silicon), hence they are expected to be a concern for consumer products too.

Furthermore, even if radiation-hardened (rad-hard) components exist, the recent trend is to use consumer components even in those applications, which operate in radiation harsh environments. In fact, rad-hard components are much more expensive and much less available than consumer products. Still, prior to use consumer products, a

thorough radiation qualification must be performed on the devices. From this point of view, very few works addressed the effects of ionizing radiation in advanced memories.

The objective of this PhD thesis is to investigate the effects of ionizing radiations on advanced non volatile memories. In particular, nanocrystal memories, phase change memories and ferroelectric memories will be addressed.

This thesis can be divided in two parts: the first one (which comprises the first three chapters) provides the basic notions, which will be used in the next part of the thesis. The second part shows the results of the research activity, and it comprises the last five chapters and the four appendixes.

In particular:

- Chapter 1 introduces the modern Flash memories and the most important aspects.
- Chapter 2 briefly introduces some of the advanced memories currently evaluated by the international scientific research community.
- Chapter 3 gives the basic notions of ionizing radiation, in particular on Flash memories.
- Chapter 4 shows some electrical characterizations performed on nanocrystal memories.
- Chapter 5 shows the comparison between the total ionizing dose effects on nanocrystal memories and floating gate memories, manufactured with the same technology.
- Chapter 6 gives a very detailed analysis of the single event effects on nanocrystal memories.
- Chapter 7 analyzes the total ionizing dose effects on phase change memory array.
- Chapter 8 reports the combined effects of total ionizing dose and temperature on ferroelectric memories.

CHAPTER 1

Introduction to Conventional Flash Memories

Flash memories are ubiquitous in everyday life and they are, by far, the most widespread nonvolatile memory. The Flash memory is substantially a 1980s improvement of the original EPROM (Erasable Programmable Read Only Memory), which was invented in 1971 by Dov Frohman [1]. The EPROM memory can be electrically programmed, but it needs an ultraviolet (UV) exposure for its erasure. This process is very slow and in-system-programming (ISP) is not possible, because the memory chip must be disconnected and subjected to UV irradiation prior to a new programming cycle. Hence, EPROM memories require costly hardware and they render device upgrade very expensive and unpractical.

The Flash memory improves the EPROM concepts by allowing the fast electrical erasure (from which the name "Flash") of the whole memory. This allows the reprogramming of the device, without the need to remove the memory chip from the system. This feature is not only used industrially in the development phase, but also it is exploited commercially, to allow device firmware upgrade even from inexperienced users (such as computer and peripheral BIOS upgrades, cell phones, etc.). This in-turn, allow a strong reduction of the so called "time-to-market" (i.e. the devices enter the market even if they have not been subjected to a thorough testing phase. Possible firmware bugs will be discovered by the users' feedback, and the factory only needs to release the appropriate bug-fixes; finally the upgrade is performed by the end-users).

The electrically alterable memories gained also popularity in the 2000s as mass storage devices, such as memory cards, USB pendrives, cell-phones and other portable devices; this latter employment, lead to a progressive and aggressive scaling of the cell sizes, which, in turn, allowed the growth of many memory demanding-applications (in particular, multimedia), which provided a positive feedback on the memory market and development.

Nowadays, almost all Flash memory devices are based on the Floating Gate MOSFET which allows the variation of its threshold voltage, by injecting/ejecting electrical charge in an insulated electrode (the Floating Gate, FG). By now, several memory manufacturers are producing FG based Flash memory in the 45-nm node, but they are experiencing difficulties in pushing the scaling beyond the 32-nm node. In fact, the FG MOSFET suffers from several scaling limits, which are both of electrical and

reliability nature. Furthermore, there are many applications in which fast, single bit alterability is a desired feature, but Flash memories do not allow single-bit erasures, and program and erase operations are quite slow, especially if compared to most volatile memories.

At this purpose, several alternatives are been explored since the last decade as possible replacements for conventional FG based Flash memories. Further details on advanced non volatile memories will be provided chapter 2.

Another important issue (which will be dealt with in chapter 3) is the tolerance to ionizing radiation. In fact, there are many fields (scientific, medic, industrial, aerospace, military, etc.) in which electronics is potentially subjected to ionizing radiation. As it will be discussed in chapter 3, conventional Flash memory exhibit very poor ionizing radiation tolerance and they need strong countermeasures (i.e. software and/or hardware radiation hardening) to reach an adequate reliability level for radiation harsh environment, such as those encountered in aerospace or military applications. Nevertheless, as the size is scaled down, the cell become more and more susceptible to even smaller energy level, such as those released from a single alpha particle. Alpha particles can be emitted by radioactive packaging contaminants, which cannot be completely eliminated, and even their reduction would be prohibitively too much expensive from a commercial viewpoint. Hence, radiation tolerance is not only being considered a serious threat for military and avionic/space applications, but also it is becoming a concern even for consumer electronics.

In this chapter we will introduce some basic concepts on non-volatile memories, with particular reference to Flash memories.

1.1 Memory topologies and parameters

1.1.1 Non volatile memory parameters

Every kind of memory device is characterized by a relatively long list of parameters. However, the most important parameters on nonvolatile memory can be summarized to:

- Memory Density/Size: it is usually given as Mbit per chip, or Mbit/unit area.
- Retention: it is the capability of retain data when the power is switched off. The industry standard is 10-years, however the retention requirement may be very different, depending from the application. For instance a space application could require a much longer retention time, whereas a disposable device (i.e. a disposable cell-phone) has a much less stringent requirement.
- Endurance: it is the ability of sustain a certain number of program/erase cycles. As it will be discussed later, each program/erase cycle tends to degrade slightly the memory cells, up to a point the information cannot be reliably stored or recovered.

- Read/Write Speed: it is the number of bits, which can be read or written per unit time. As it will be clear later, the read and write speed depend on the way the cells are connected in the array (see paragraph 1.1.2 below)
- Random or Sequential Access: some memories are optimized for sequential accesses at the expense of an initial higher access time. Other memories can be read at any address without the bottleneck of the initial long access time.

Those parameters are strongly affected by both the kind of memory cell and to the memory cell arrangement (topologies), which will be discussed in the next section. It is important to note, however, that the relative importance of the previously mentioned memory parameters cannot be established a priori. Every application has its own priority list. For instance the embedded memory of a high speed DSP or microcontroller may require a very high read speed rather than high speed write or memory density.

1.1.2 Flash Memory topologies

Almost all the Flash memories can be grouped in two main categories, which differ in the bank topology: NOR or NAND architectures, see Fig. 1.1. In Fig. 1.1, the Floating Gate MOSFET (FGMOS) symbol have been used to indicate the memory cells, because of their widespread use on the majority of nowadays non volatile memories. However, the following considerations can be extended to other kinds of memory cells, at least for the NOR topology.

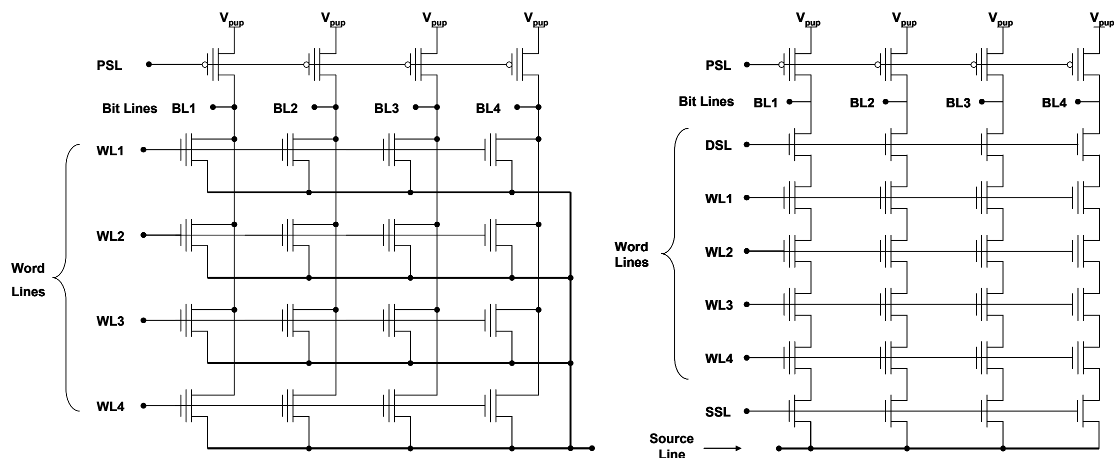

Fig. 1.1. Schematics of the two topologies. NOR (on the left) and NAND (on the right).

Both in NOR and NAND topologies, the cells are arranged in a matrix, with rows and columns. All the cells of the same rows share the selection terminal (the gate, in case of floating gate memory cells). Each row terminal is called Word Line. Each column terminal of the array is called bit line. In NOR memories, the cells have one end connected directly to a bit line, while the other end is common for all the cells of the same sector. This kind of arrangement is called “NOR”, because each column (i.e. all the cells connected to the same bit line) resembles the pull-down network of a NOR gate implemented in static complementary logic.

Conversely, in NAND memories, each column consists of a series of cells[1], resembling the pull-down network implementation of a static complementary logic NAND gate. Typically, the number of cells connected in series is limited to 16-32. In fact, as it will be discussed in paragraph 1.3.1, the read time grows with the square of the word line number.

NAND and NOR topologies have different advantages and drawbacks, hence none of the two is inherently superior to the other. The best choice is determined by the application in which the memory is going to be used.

There are mainly two differences in performances between NOR and NAND topologies. NAND topologies are somewhat smaller, hence higher densities can be achieved, using the same area. In fact, the drain and source diffusions can be shared by adjacent cells of the same column. Furthermore, there are no bit lines and source lines tracks within the arrays, further increasing the maximum memory density (see Fig. 1.2).

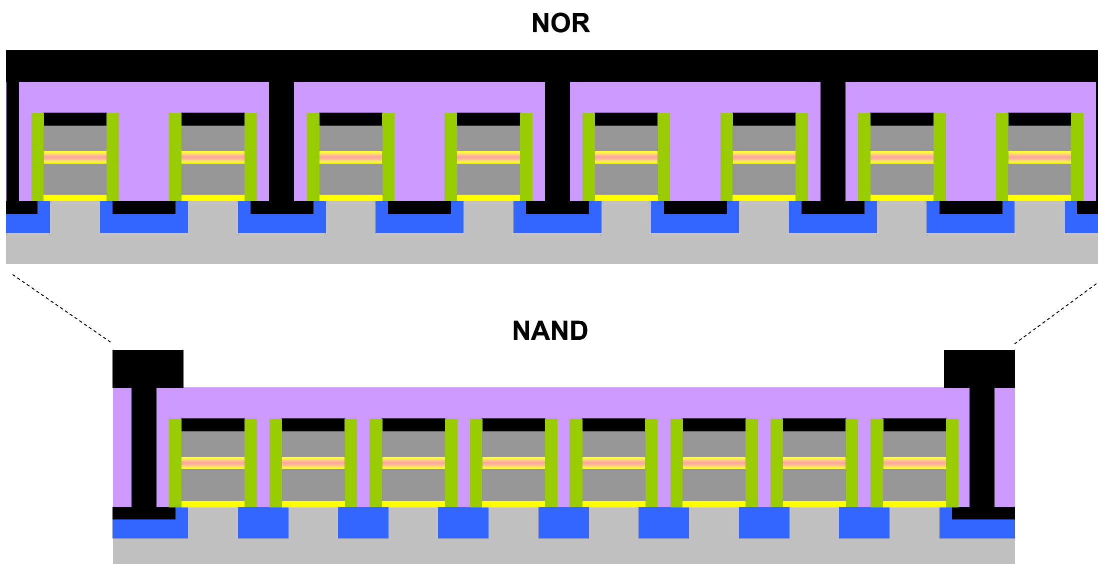

Fig. 1.2. Comparison of the schematic cross sections of 8 floating gate memory cells arranged with the NOR and NAND topologies. NAND topology allows for a consistent space saving.

Indeed, the typical single bit cell areas are ~10F^2 and ~5F^2 for NOR and NAND single level cells, respectively, where F is the minimum design rule. That is NAND memories are almost twice as dense as their NOR counterparts. However, NOR topologies are somewhat faster, at least in read operation, as it will be explained later, in paragraph 1.3.1.

NAND memories are more often used as mass storage devices, where large chunks of files are read or written sequentially. NOR memories are used to store firmware, where random read is much more frequent due to branches.

[1] Actually the term "series" is a misnomer, however it recalls that the bit line current ideally flows in all the cells of that bit line.

1.2 The Floating Gate MOSFET

The memory cell of almost all the contemporary solid state non volatile memories consists of a Floating Gate MOSFET, whose cross sections are schematically shown in Fig. 1.3.

In a FGMOS, the key element is the floating gate, which is an insulated conductive electrode (usually heavily doped polysilicon), sandwiched between the gate and the substrate of a MOSFET. The gate of the FGMOS is called "Control Gate" because it controls the channel formation and the charge injection/ejection from/to the FG. The FG is insulated by the surrounding electrodes by the tunnel dielectric and the interpoly dielectric. The interpoly dielectric owes its name because both the floating gate and the control gate are usually made of polysilicon. The dielectric between the FG and the substrate is called "tunnel" because some write operations are performed by means of tunnel effect.

Being insulated, the FG can store electrons, which modulate the cell threshold voltage. The dielectric thicknesses are chosen as tradeoff between program and erase speed and reliability (i.e. non volatility). Furthermore, the dielectric thicknesses must be chosen so that no electrons escape during standby or read operations, while allowing the charge injection or removal when the device is to be programmed or erased.

Nowadays FG MOSFETs have a typical tunnel dielectric thickness in the range 7-10nm (the higher values are adopted in the NOR topologies) and a typical control dielectric equivalent oxide thickness (EOT) within 14-20nm. The tunnel dielectric is made of high quality high temperature thermal oxide (HTO), which grants the strongest insulation. The interpoly dielectric cannot be made of HTO because the high temperature needed for this process would affect the previously growth tunnel oxide [2]. Hence, the interpoly dielectric is deposited by CVD, and it usually consists of an ONO stack (silicon Oxide, silicon Nitride, silicon Oxide). The additional silicon nitride layer is used because of its higher dielectric constant, thus allowing a much lower EOT, while keeping good insulation properties.

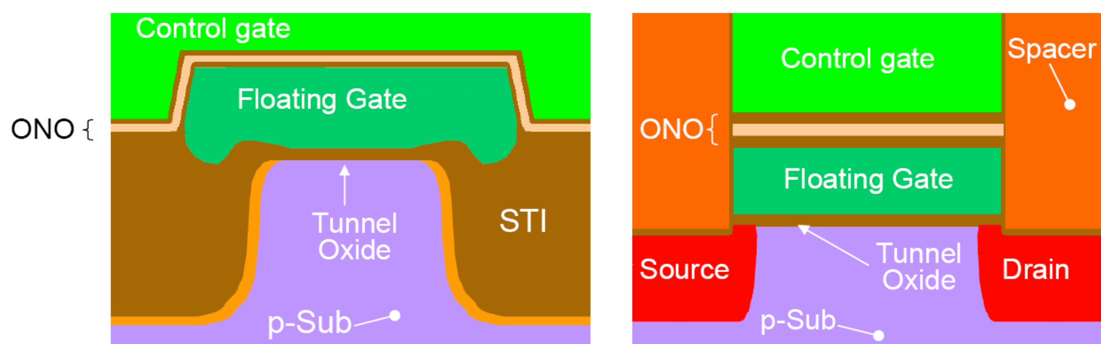

Fig. 1.3: Cross section along the word line and along the bit line of a floating gate MOSFET.

The band diagram and the transfer characteristics for the neutral (erased) and the negatively charged (programmed) floating gate are depicted in Fig. 1.4. When the cell is neutral, it features a "low" threshold voltage. Conversely, when the FG stores an excess of electrons, the cell features a "high" threshold voltage. The difference between the programmed and erased threshold voltages (ΔV_{TH} in Fig. 1.4) is commonly known as the "programming window".

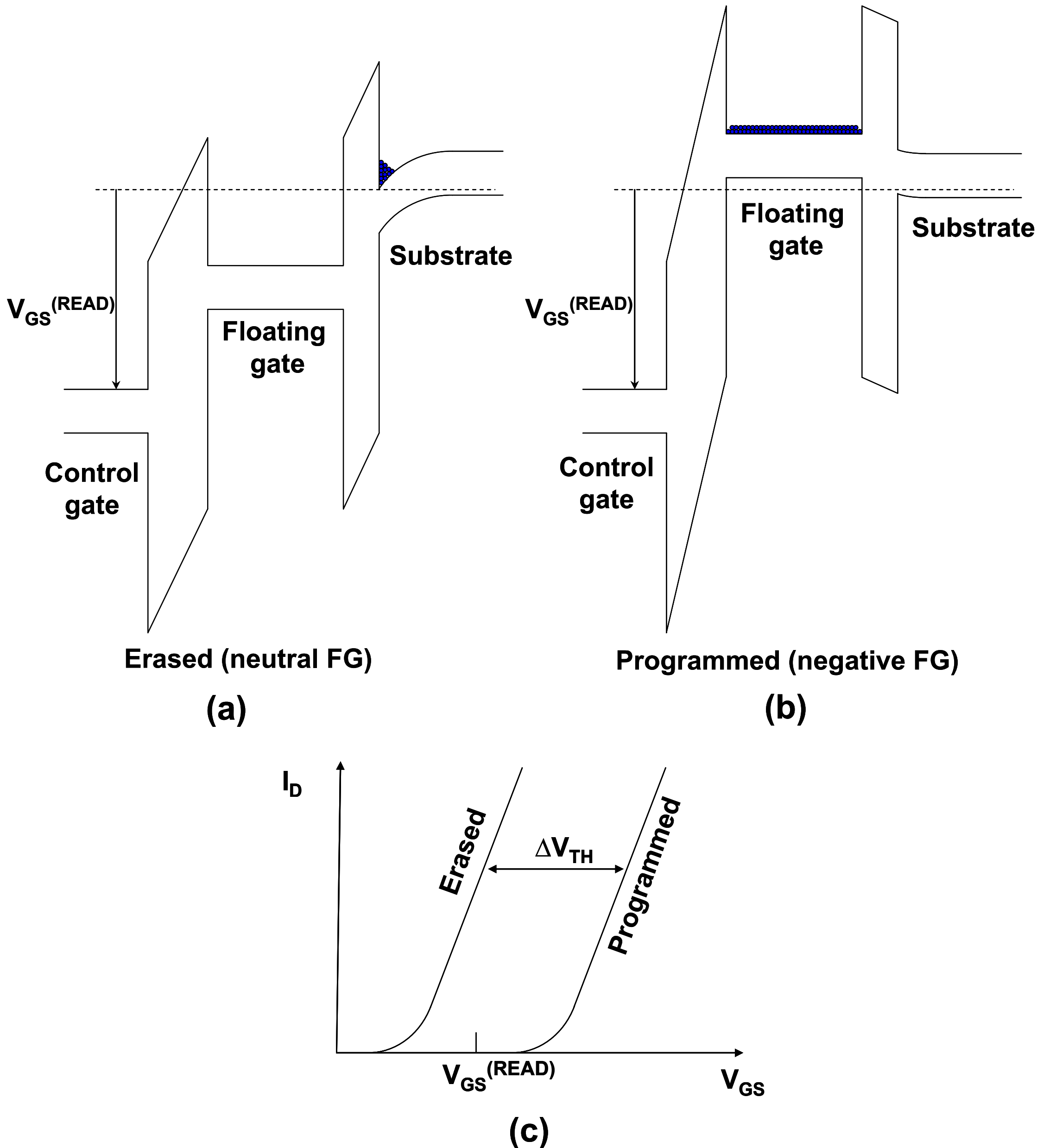

Fig. 1.4. Schematic band diagram for the erased (a) and programmed (b) cell and the corresponding transfer characteristics (c). When the floating gate is neutrally charged, inversion can occur in the substrate at the read voltage ($V_{GS}^{(READ)}$). At the same gate voltage, inversion does not occur if the floating gate stores a certain amount of negative charge.

The approximate cell equation can be found relatively straightforward considering the capacitive couplings to the FG (see Fig. 1.5) and using the Gauss's law.

$$Q_{FG} = C_{FB}\left(V_F - V_B\right) + C_{FS}\left(V_F - V_S\right) + C_{FC}\left(V_F - V_C\right) + C_{FD}\left(V_F - V_D\right) \quad (1.1)$$

Where Q_{FG} is the total charge stored in the floating gate and C_{FX} are defined in Fig. 1.5.

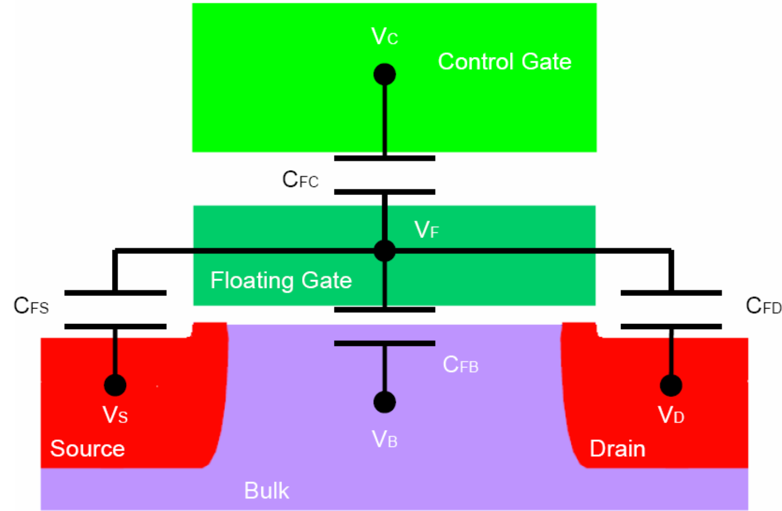

Fig. 1.5: Capacitive couplings between the various electrodes.

By defining $C_T=C_{FC}+C_{FB}+C_{FD}+C_{FS}$, the equation (1.1) can be written as:

$$V_{FG} \cdot C_T = Q_{FG} + C_{FC} \cdot V_C + C_{FS} \cdot V_S + C_{FD} \cdot V_D + C_{FB} \cdot V_B \qquad (1.2)$$

Now, by letting:

$$\alpha_i = \frac{C_{Fi}}{C_T} \qquad (1.3)$$

And solving for V_{FG}, the previous equation becomes:

$$V_{FG} = \frac{Q_{FG}}{C_T} + \alpha_C \cdot V_C + \alpha_D \cdot V_D + \alpha_B \cdot V_B + \alpha_S \cdot V_S \qquad (1.4)$$

To evaluate drain current I_D, we set V_S and V_B to zero so the last two terms in (1.4) vanish.

Adopting the classical gradual channel I_D formula for the linear region of a MOSFET, we have:

$$I_D = k' \frac{W}{L}\left[\left(V_{FG} - V_{TH}^{FG}\right)V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad (1.5)$$

By substituting (1.4) into (1.5), we obtain:

$$I_D = k'\frac{W}{L}\left[\left(\frac{Q_{FG}}{C_T} + \alpha_C \cdot V_C + \alpha_D \cdot V_D - V_{TH}^{FG}\right)V_{DS} - \frac{V_{DS}^2}{2}\right] \quad (1.6)$$

After a little algebra, the final equation (valid for the linear region) can be obtained:

$$I_D = k_{eq}'\frac{W}{L}\left[\left(V_C - V_{TH}^{CG}\right)V_{DS} - \left(\frac{1}{2\alpha_C} - f\right)V_{DS}^2\right] \quad (1.7)$$

Where:

$$k_{eq}' = k'\alpha_C$$

$$V_{TH}^{CG} = \frac{V_{TH}^{FG}}{\alpha_C} - \frac{Q}{C_T \cdot \alpha_C}$$

$$f = \frac{C_D}{C_C}$$

With additional manipulations the formula for the saturation region can be found:

$$I_D = \frac{k_{eq}'}{2}\frac{W}{L}\alpha_C\left(V_C + f \cdot V_{DS} - V_{TH}^{CG}\right)^2 \quad (1.8)$$

Fig. 1.6 shows the output characteristics evaluated using equation (1.8). Noticeably, with a high enough V_{DS}, there is a non-zero drain current. This phenomenon is called drain-induced turn-on (DTO).

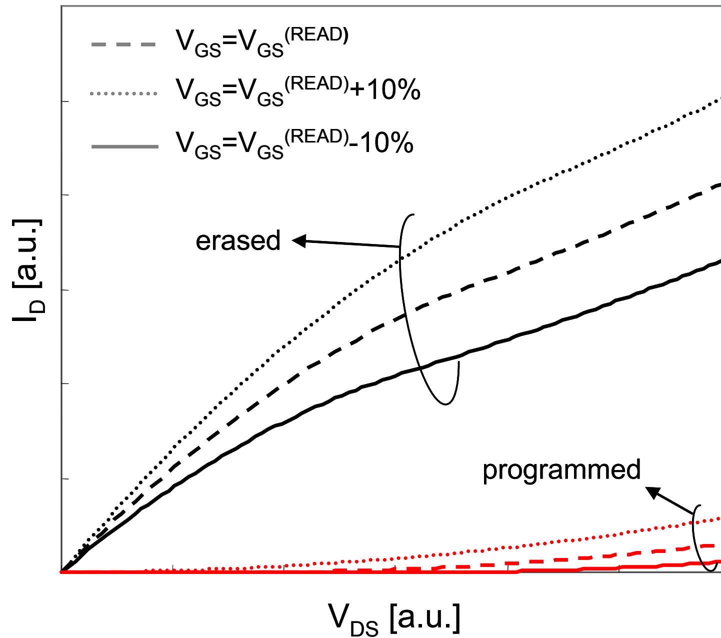

Fig. 1.6 Output characteristics of an erased (black) and programmed (red) FGMOS evaluated at different V_{GS} values.

The drain-induced turn-on is very concerning for a NOR topology. In fact, it should be noted that, even if each current is small, the overall contribution on the bit line can be quite large, because there are many MOSFET connected to each bit line. This could

result in a quite large current even if the accessed cell is programmed, therefore reducing the sensing margins.

Moreover, even if there is no read disturb, the sum of the current of each bit line would lead to great power dissipation. A possible solution is to use (as shown in Fig. 1.1) a pull up MOSFET (instead of a resistor), which can be turned off if the sector is not accessed, in order keep the quiescent current at low levels during stand by.

The drain-induced turn-on can be reduced by decreasing f, *i.e.* decreasing the C_{FD} over C_{FC}, ratio. This can be accomplished increasing L and decreasing W, since C_{FD} depends only on W whereas C_{FC} depends on the $W{\cdot}L$ product. C_{FD} mainly derives from the floating gate to drain overlap; such overlap must not be decreased in order to keep low the ON resistance of the MOSFET. Hence, the requirements on f pose a constraint on the minimum value of the channel length L.

1.3 Read and Write Operations

1.3.1 Read operations in NOR and NAND Flash Memories

In a NOR architecture, the cell information is sensed differentially, that is, the read current of the cell to be sensed is compared to the read current of a reference cell. The reference cell has the same characteristics of the cell in the memory array and same applied bias of the cell being sensed [3].

The cell selection is performed applying a positive gate voltage to the word line (WL) to be selected, and 0V to the other word lines. The drain voltage must be chosen to avoid the so called drain-turn-on. This effect is also worsened by the fact that there are several cells in parallel, hence even small current contributions could lead the incorrect data retrieval. On the other hand, higher currents usually allows faster cell readouts, which may be desirable for high speed random reads, which are very frequent in all those application in which NOR Flash are used.

In case of memory cells storing only one bit per cells (single level cell, SLC), the comparison is very simple: the cell reference cell is trimmed so that its threshold voltage is between the distributions of the programmed (charged) and erased (neutral) cells. Hence, at the same bias voltage, the reference cell has higher and lower drain current than all the programmed and erased cells, respectively.

The NAND read operation is performed differently. First, the cells may exhibit a slightly negative (neutral, erased) or a positive (negatively charged, programmed) value. The cell selection is performed applying a zero gate voltage to the cell to be selected, and a positive V_{PASS} voltage to the other cells. The cell not to be selected will act as pass transistor, while the cell selected will determine the current flowing into the cell string. Usually, the read current is very low (in the 200 nA range, compared to the tens of µA employed in NOR Flash) and the cell sensing is performed by charge integration: the parasitic capacitance of the bit line is precharged at a fixed voltage (around 1V),

then the cell string is connected to the bit line through the bit line selector. If the selected cell is programmed, a negligible current will flow and the bit line will remain charged within the read time. Conversely, if the selected cell is erased, the bit line will be discharged within the read time.

Similar read techniques are adopted for multilevel cells (MLC, i.e. cells storing two or more bits), at the expense of reduced noise margins and tighter requirements in terms of program operations, as it will be discussed in the next operation.

Simple calculations can explain the different read speeds of NAND and NOR Flash. At this purpose, some assumptions will be given, to allow many simplifications:

1. The drain capacitance of the pull up transistor (see Fig. 1.1) is negligible compared to the sum of the other capacitances of the bit line.
2. The “ON” resistance of the MOSFET grounding the source line (not shown in see Fig. 1.1) is only a small fraction of the “ON” resistance of a FGMOS (R_{FG}) and it can be neglected.
3. There are no leakage paths.

In a NOR topology the capacitance of each bit line is about $n_{WL} \cdot Cs$, where n_{WL} is the number of word lines. The propagation time taken by a bit line to go from a low level to the high level is roughly:

$$t_P^{LH} = 0.69 \cdot R_{PUP} \cdot n_{WL} \cdot C_S \qquad (1.9)$$

As can be seen, this time increases linearly as the number of word lines. Moreover the larger the C_S (i.e. the larger the FGMOS) the higher t_P^{LH} will be.

The time taken for the opposite transition of the bit line (high to low) is:

$$t_P^{HL} = 0.69 \cdot R_{FG} \cdot n_{WL} \cdot Cs \qquad (1.10)$$

This time is still dependent on the number of word lines (n_{WL}), however it is not affected by the widths of the transistors, because C_S rises as W increases whereas R_S decreases as W increases.

For a NAND topology we will also make the further assumptions (in addition to those already made for NOR topology)

1. The ON resistance of the pull up MOSFET is negligible;
2. There is no difference between the “ON” resistance of a depletion (i.e. erased) MOSFET biased with a low V_{GS} and an enhancement (i.e. programmed) MOSFET biased at high V_{GS}.

The two worst case propagation times are:

$$t_P^{HL} = 0.69 \cdot \sum_{i=1}^{n_{WL}} i \cdot R_{FG} \cdot \left(C_S + C_D\right) \cong 0.69 \cdot Cs \cdot n_{WL}^{\;2} \cdot R_{FG} \qquad (1.11)$$

$$t_P^{LH} = 0.69 \cdot R_{PUP} \cdot (Cs + Cd) \cong 1.38 \cdot Cs \cdot R_{FG} \qquad (1.12)$$

Where the approximations become valid as n_{WL} increases. As shown, the propagation times increase as the $n_{WL}{}^2$ in NAND memories. In fact, typical random read speeds are in the tens (50-100) of nanoseconds for NOR topologies, and tens of microseconds for the NAND counterparts.

1.3.2 Program and erase techniques

As already mentioned, the information is associated to the cell threshold voltage, which, in turn, can be modulated by varying the stored charge. Program operations allows to increase the excess of electrons, while erase operations allow the neutralization of the stored charge (in some cases, the FG may also store an excess of positive charges).

Basically, there are two methods to inject charge into the floating gate: the charge hot carrier injection (CHC), and the tunnel effects (typically Fowler-Nordheim tunnel, because of the triangular shape of the potential barrier). There are also optimized variants for CHC, such as the CHISEL (Channel-Initiated-Secondary-Electrons), but they all work in the same principle: the injection of the hot carriers.

In CHC (see Fig. 1.7), the electrons in the channel are accelerated by the electric longitudinal field, especially near the drain diffusion, where it is higher. Most of the accelerated electrons lose their energy due to collision with the lattice and impurities. However, some electrons can gain enough energy to overcome the potential barrier at the Silicon-oxide interface (see Fig. 1.7). Now, if there is a transversal field towards the channel, the electrons will also across the tunnel oxide and finally fall into the conduction band of the floating gate. Hot electrons will then thermalize in the thick floating gate, without stepping out from it.

Noticeably, this charge injection technique is somewhat self-limited, because, as the time elapses, the floating gate becomes more and more negative, inducing an opposite field, which eventually prevents any further electron injection.

Summarizing, to inject charges with this method, two conditions are necessary:

1) The drain to source voltage must be greater than the difference between the conduction bands of the oxide and of the silicon (about 3.15 eV).

2) A transversal field directed towards the channel must be present, in order to bring the electrons to the floating gate.

This phenomenon is very difficult to model. The “lucky electron” model is used as an approximation. In this model, a fundamental assumption is taken: the electrons never collide, hence their energy can be expressed as $q \cdot V(y)$, where V is the voltage at the point of coordinate y (assuming that the source is grounded). Consequently this model is not very accurate but it is still useful to get a qualitative scenario.

The qualitative result of the lucky electron model is:

$$I_G = CI_D \exp\left(-\frac{\phi_B}{\lambda E_m}\right) \qquad (1.13)$$

Where λ is the mean-free path, ϕ_B is the potential barrier height between the two conduction bands and E_m is the maximum longitudinal field.

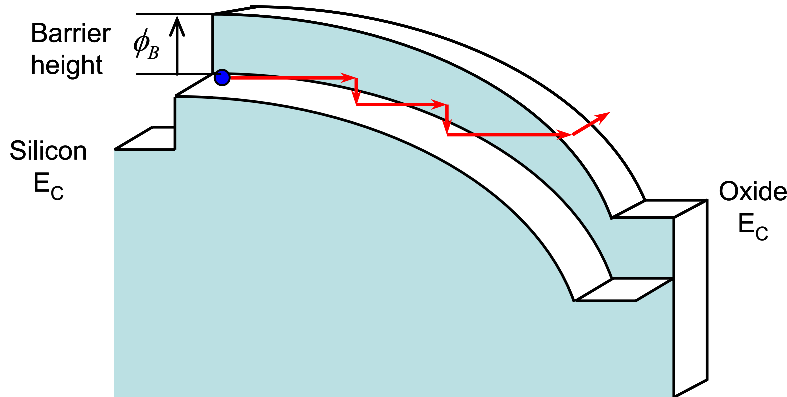

Fig. 1.7: Band diagram of the Silicon-Oxide stack during a CHC. Only the conduction bands are shown.

Another way to inject electrons into the floating gate is by tunnel effect. In this case, the electrons are not accelerated in the channel, hence they have not enough energy to overcome the silicon to silicon-oxide barrier. Still, electrons have a non zero probability to pass through the oxide. Fig. 1.8 shows two cases of tunnel effects: direct or Fowler-Nordheim (FN). With the direct tunnel, electrons across the whole oxide and "jump" directly to the anode, hence they see a trapezoidal barrier. Conversely, in with the Fowler-Nordheim tunnel, the band bending is so strong that electrons can tunnel in the oxide conduction band, before reaching the anode.

Flash memories use Fowler-Nordheim to erase (or program) the cells. In fact, the tunnel probability depends much more on the barrier width than the barrier shape, and this allows to achieve very high tunnel efficiency (by Fowler Nordheim) during write operations (applying high voltages across the tunnel oxide), and very low tunnel efficiency (direct tunnel) during read or standby, ensuring that the stored information is not compromised for a very long time (typically, at least 10 years).

By solving with the WKB model, the following formula can be obtained for the FN tunnel current density:

$$J_{FN} = A \cdot E_{OX}^{\;2} \cdot \exp\left(-\frac{B}{E_{OX}}\right) \qquad (1.14)$$

Where

$$A = \frac{q^3 m_0}{16 \cdot \pi^2 \cdot \hbar \cdot m_{OX} \cdot \phi_B}$$
$$B = \frac{4 \cdot \sqrt{2 \cdot m_{OX}} \cdot \phi_B^{3/2}}{3 \cdot \hbar \cdot q} \quad (1.15)$$

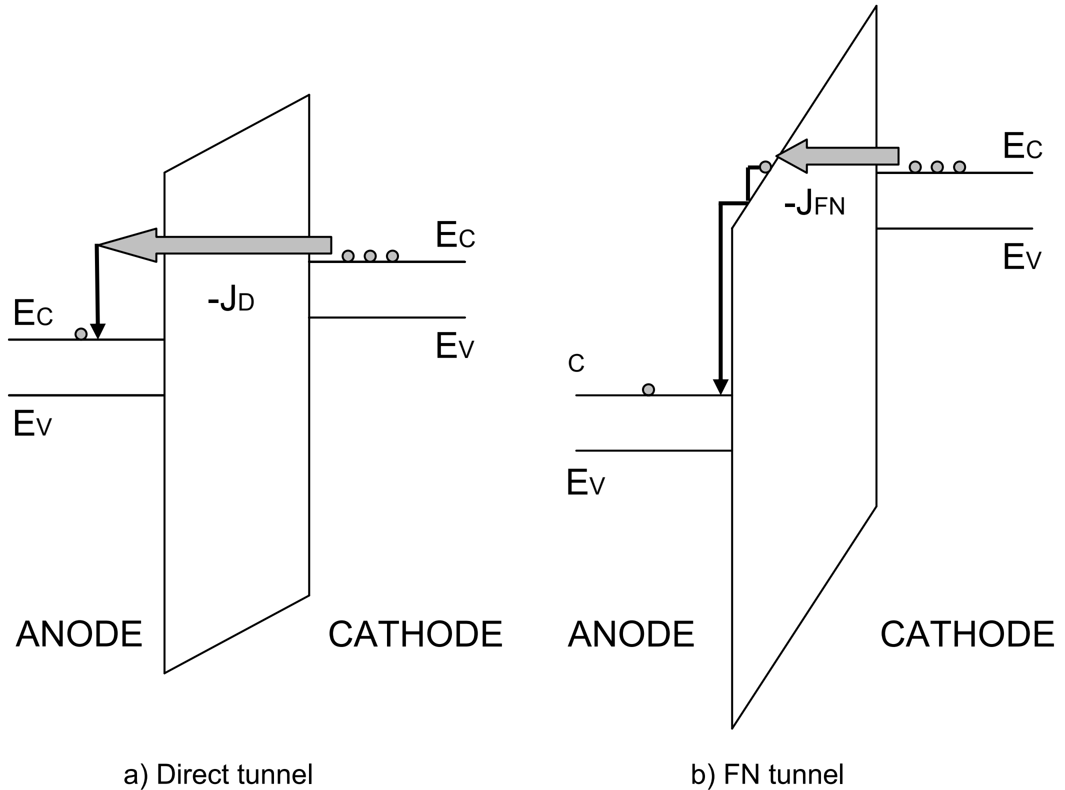

Fig. 1.8: Band diagram for direct tunnel (a) and FN tunnel (b). For simplicity the silicon band bending is not shown.

As can be seen from equation (1.14), the tunnel probability increases exponentially as the field increases. Therefore, a larger voltage drop across the oxide will lead to a stronger tunnel current; on the other hand, a smaller oxide thickness allow a greater tunnel current at a given *voltage*, because of the higher field strength. However, it should be noted that, *given the field strength*, the tunnel probability does not depends on the oxide thickness.

Because the tunneling current strongly depends on the field, the programming and erase voltages must be quite accurate and/or a smart program algorithm must be adopted.

CHC injection is fast, but very inefficient: a very large drain current is required to inject a very small current. Hence CHC requires a lot of power. On the contrary, FN tunneling is very efficient (almost all the charge reaches the Floating gate), however it requires very high voltages. Furthermore, the injected current is even smaller than that obtained with CHC, hence the FN tunneling is rather slow. FN tunnel can also be exploited to erase the devices, using the opposite voltage, while CHC only allows charge injection.

1.3.3 Program and erase operations

The programming technique used in Flash NVM is strongly correlated with the device topology. NOR Flash employs CHC to program the cells, while NAND Flash employs FN tunneling. Both NOR and NAND topologies exploit FN tunneling, which is performed per blocks, allowing a strong reduction of the erase time.

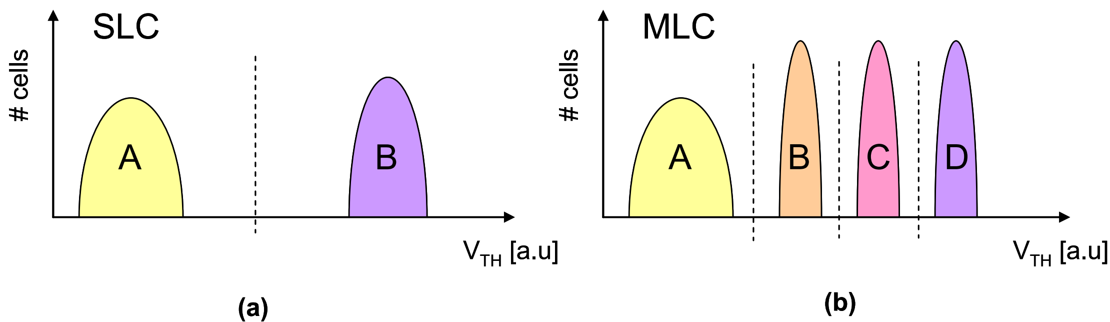

Fig. 1.9. Simplified representation of the threshold voltage distribution for a single (a) and a multi level (b) cell. As the number of bit per cell increases, the distributions must be tighter, and the sensing margins are reduced.

Program and erase operations results in a certain threshold voltage distribution, whose spread depend on the process variation, power supply variations, cell position in the array, operating conditions (temperature), etc. The threshold voltage distribution widths must be kept under certain limits, in order to be able to distinguish the programmed and the erased states. These requirements are more stringent when dealing with MLC (see Fig. 1.9). Hence, smart programming techniques are adopted to accurately place the programmed cell threshold voltage value within the desired range.

As previously mentioned, CHC program operation is fast, but it is very power consuming. Hence the faster the cell must be programmed, the higher the power consumption. Obviously, the larger the number of cells programmed in parallel, the higher the power consumption. Hence, the programming times in NOR Flash are somewhat slow (about 5-20µs per word).

Typically, CHC is performed by applying a 4.5V on the drain and 9-10V on the gate, with source grounded. The substrate may be either grounded, or kept at a negative bias, to enhance the secondary hot electron generation (CHISEL). The voltages and currents (hundreds of µA per cell) required by CHC are both rather high, hence a considerable large fraction of the chip area is needed by the high power and high voltage peripheral circuitry.

During the program operation on a NOR array, high voltages are applied to the drains or to the gates of the cells sharing the same bit line and word line, respectively (see Fig. 1.10a). This can be a quite stressing operation even for those cells not being programmed. Furthermore, the high drain voltage may reduce the FG stored charge through tunneling (drain disturb). Similarly, the erased cell sharing the same word line

of the cell being programmed may be subjected to a partial programming due to the high gate voltage.

NAND program operations are performed through FN tunneling, which requires intense electric fields to achieve high injection efficiencies. The high voltages required are very expensive in terms of peripheral circuitry, even if the programming currents are very low. Furthermore, the high fields damage the oxide by generating traps, which allow tiny leakage currents to flow through the oxide (SILC, stress induced leakage currents). Another disadvantage of FN tunneling is the time required by the program operation: some milliseconds. Nonetheless, the extremely low programming current can be exploited for the parallel programming of a large number of cells, reducing the effective programming time per word. Thanks to the parallel programming, NAND Flash feature very high write speeds with respect to their NOR counterparts, which makes them well suited for mass storage applications.

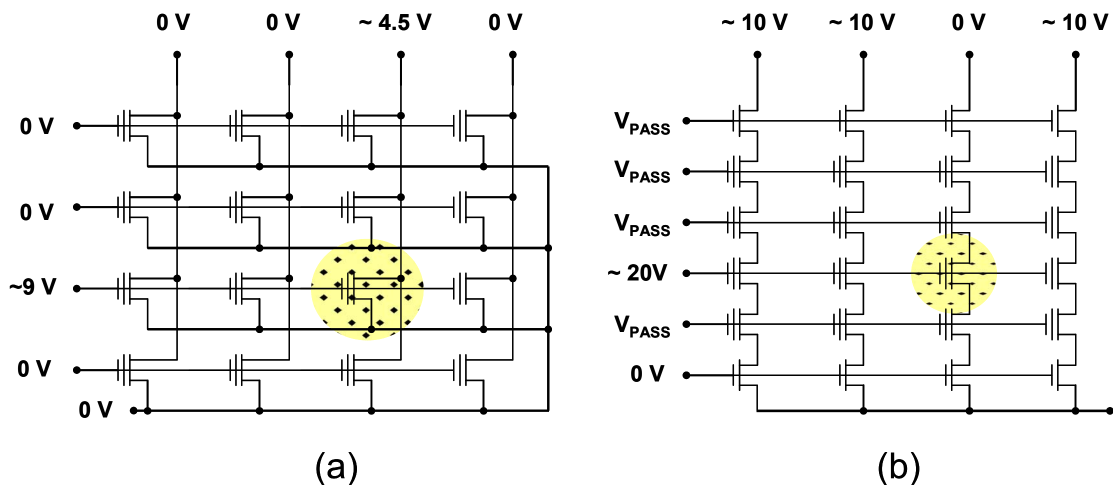

Fig. 1.10. NOR (a) and NAND (b) arrays during program operations.

To program a memory cell of the NAND array (Fig. 1.10b), the gate of the drain selector must be biased to V_{DD} and the gate of the source selector must be biased to GND. The bit lines not to be programmed are biased at relatively high voltages (8-10V), while the bit line to be programmed is kept at 0V. The gate of the word lines not to be programmed are kept at a certain voltage V_{PASS} (so that they act as pass transistor without being programmed), while the gate of the word line to be programmed is biased at 15-20 V.

Several techniques allowed to reduce in recent devices the area consumption required for the high voltage generation circuitry. These may include the self boost mechanism [4] (which exploits the capacitive coupling to build up a voltage on a dynamic substrate). Hence lower biases are needed to achieve the same gate to substrate voltage, required for the FN tunnel.

Erase operation are performed through FN tunneling, both in NOR and NAND Flash, applying a high voltage across the tunnel oxide. The memory cell is placed in an

insulated triple well to allow to bias at high voltages the insulated internal p-well. Cells of the same block are erased contemporaneously, thus reducing the erase time [2]. However, the erase times are much longer in NOR topologies than their NAND counterpart, due to the much complex erase algorithm employed in NOR.

In NOR, the erased threshold distribution must be low enough for adequate noise margin, but it cannot be too low (over erase). In fact, if a cell has a negative (or very low) threshold voltage, the cell will always drive a certain current, even if it is not addressed. This may reduce the sensing margin or, even worse, it may make impossible to distinguish the stored data on the addressed programmed cells. Hence, the erase algorithm must control that the cells drives a certain high enough current, to distinguish the erased from the programmed state. However, erase times and voltages must be chosen to avoid over erasing.

In NAND application, there is no over erase problem, and the erase distribution can be somewhat wider. In fact, during read operation, the unselected cells must act as pass transistor, hence the threshold voltage can be negative. Furthermore, the "ON" resistance of unselected cells is not significantly affected[2] by their threshold voltage during read. The erase operation is performed biasing the internal p-well with a high voltage, and grounding the word lines of the sector to be erased. The p-well is common for all the blocks, to keep low the number of structures required to bias the cell body.

1.4 Reliability: endurance and retention

The most important reliability aspects for all kinds of rewritable NVM are the endurance and the retention, which are the capability to rewrite the memory cells for a large number of times and the capability to keep the stored information for long times (which determines the nonvolatility), respectively.

Unlike volatile memories, in fact, conventional Flash memories have a non infinite number of program-erase cycles, which is typically limited to 10-100k cycles for NOR Flash and 100k-1M cycles for NAND Flash. The limited number of cycles is due to the very high fields employed during the program-erase operations. The very high fields, in fact, have two main consequences: the charge trapping in the dielectrics and the dielectric degradation by generation of traps, inducing leakage currents (SILC). A comprehensive discussion on the charge trapping mechanisms, the defect generation, and their nature is outside the scope of this thesis, and the reader may refer to [5]-[10] and the references cited therein for further details.

Fig. 1.11 shows the erased and programmed threshold voltages of a cell, as a function of the number of program-erase cycles the cell has been subjected to. Both the erased and programmed cell threshold voltage increase, indicating negative charge

[2] In fact, because of the high V_{GS}, the threshold voltage dispersion is only a small percentage of the overdrive V_{GS}-V_{TH}, hence the "ON" resistance shows a negligible variation.

trapping or even the increase of the subthreshold slope, the latter being a clear signature of the severe substrate/dielectric interface degradation.

The increase of the effective threshold voltage for the erased cell is a main concern for NAND topologies, where further erase pulses cannot be applied. Hence, a large enough sensing margin must be carefully provided for NAND memories, taking into account that this margin will decrease as the cell is cycled. On the contrary, NOR topologies allow to counteract the increased threshold voltage of the erased cell, by applying further erase pulses. This is why in commercial NOR Flash memories wide ranges of erase times are specified.

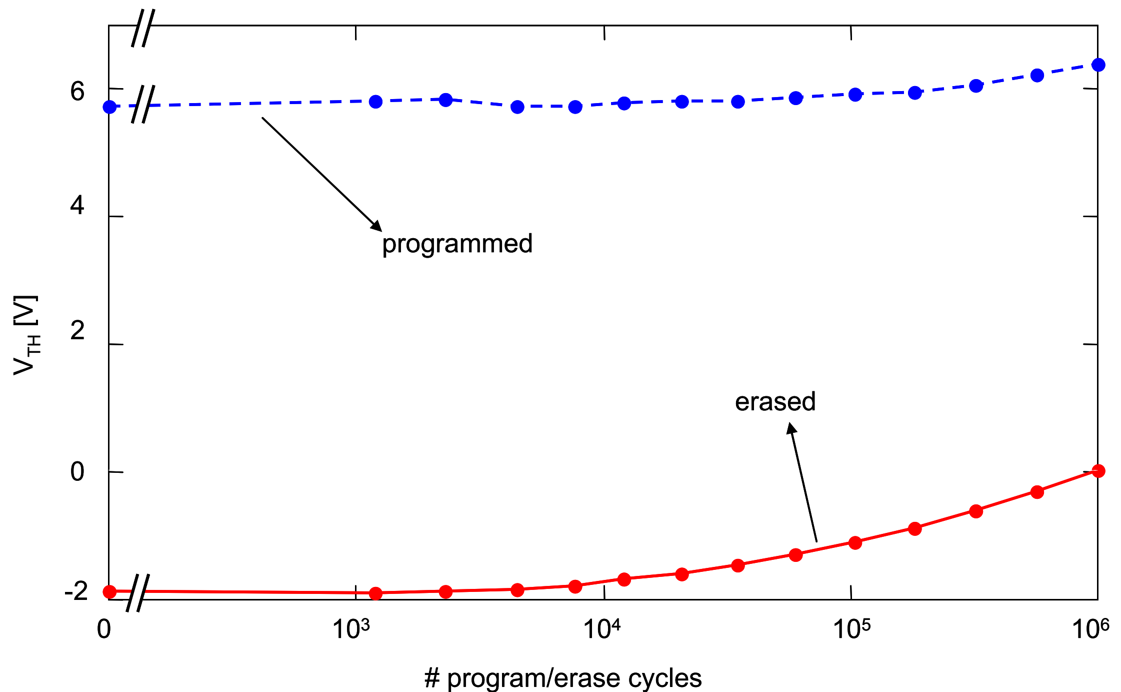

Fig. 1.11. Endurance test performed on a floating gate memory cell array. The average of the programmed and erased cell threshold voltages are plotted as a function of the number of program and erase cycles the array was subjected to.

Without smart program algorithms, the programming window can also decrease in width, due to the reduced field, during the program pulse. In fact, negative trapped charge may reduce the effective field in the tunnel oxide, allowing a smaller charge to be injected. This smaller efficiency can be counteracted by increasing the programming time.

As previously mentioned, the high fields may also create oxide defects, which allow very tiny leakage currents to flow from/to the floating gate. These currents strongly impact the retention (which must be granted even if the cell is cycled at the maximum permissible number of times). In fact, nowadays Flash memories store very few electrons (around 1000, which is estimate to drop below 100 in the sub 30-nm node [11]). To achieve the 10-year industry standard retention time, assuming a 20% sensing

margin [2], the ultrascaled cells cannot lose more than 20 electrons per year. The entity of the leakage currents is determined by the number of traps, their physical location in the oxide (they are most effective when they are located in the center), their energetic distribution and, above all, the oxide thickness. At this regard, to achieve the required reliability levels, the tunnel oxide thickness must be kept above the 7-10 nm range, while the interpoly dielectric must be kept in the range 13-15 nm [12]. It is worth to remark that a defect free 7-nm thick HTO have very little tunnel probability, at the operating read fields, and the leakage current are well below the 20 electrons/year required for the data integrity. Nonetheless, this tunnel probability is strongly enhanced if defects/traps are created, hence, the oxide thickness must also take into account the progressive increase of the leakage current as the cell is cycled.

1.5 Scaling Issues

As already mentioned, nowadays Flash memories suffer from several scaling limits. Those limits are of both electrical and reliability nature, and they are intrinsic to the floating gate MOSFET. The cell area scaling is required to achieve higher densities but, to keep the short channel effects under control the tunnel oxide thickness must be scaled too. Smaller oxide thicknesses allow also the reduction of the programming and erase voltages, with consequent benefits in terms of power consumption and smaller area required by the peripheral circuitry. However, as already discussed in the previous section, thinner oxides imply smaller robustness to stress, because of the higher SILC. Hence, to keep good reliability levels (especially in terms of retention), the tunnel oxide cannot be scaled below 7-10 nm.

Another important issue is the drain-induced turn-on already described in paragraph 1.2. This phenomenon (not to be confused with the short channel effects) is caused by the presence of the monolithic conductive floating gate. In fact, to effectively reduce the “ON” resistance of the MOSFET the gate (and the floating gate in a FGMOS) must partially overlap the source-drain diffusions, therefore there is a somewhat non negligible drain to floating gate capacitive coupling. Hence, if the potential at the drain increases, the floating gate potential is increased, effectively reducing the threshold voltage and increasing the FGMOS off current (up to a limit that the FGMOS could also be turned on for high enough drain voltages). To keep under control the DTO effect, the control gate must have a strong capacitive coupling with the floating gate, but if the cell length is scaled, the control gate to floating gate capacitive coupling is reduced, while the drain to floating gate capacitive coupling remains almost constant (drain to FG overlap does not scale with the cell length). Hence DTO poses a strong limit on both the readout voltages (thus, the speed) and the minimum cell length, in NOR Flash [12].

Another capacitive coupling-related scaling issue is present in ultradense NAND flash, whose cross section is shown in Fig. 1.12. In fact, the thick floating gates of adjacent cells may exhibit strong capacitive couplings, affecting both the read and the

write operations [13]-[18]. This is a major issue when the cell spacing needs to be scaled down.

Other FG issues are the presence of tail and fast bits [2],[19]. Tail bits form the typical tail in the distribution of erased cells and are related to intrinsic effects. Fast bits derive from cells whose threshold voltage may be several volts below the average (even past the tail). Their origin is attributed to external contaminations embedded in the tunnel oxide. Furthermore polysilicon asperities may induce higher local electric fields, thus enhancing the tunnel probability, leading either to a compromised retention or a much wider threshold voltage distribution after the program or erase operations. These effects are exacerbated when the oxide thickness is smaller.

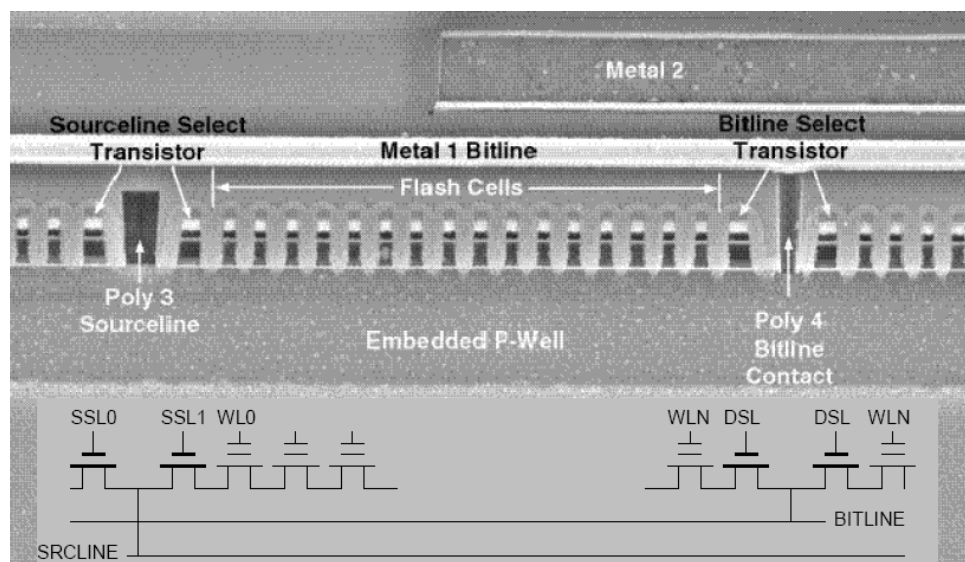

Fig. 1.12:. TEM cross section of a NAND FLASH bit line.

From the radiation tolerance viewpoint, the scaling issues are even worse, as they will be dealt more thoroughly in the chapter 3. In fact, Flash memories have several weak points, such as high voltage charge pump and peripheral circuitry, combinational and sequential blocks (for the internal state machine which handle the complex read/write operations), the NAND pagebuffer (a small RAM in which the page is downloaded for fast sequential reads) and the cell array itself. High voltage circuitry may exhibit permanent degradation after radiation exposure, while the NAND pagebuffer may show single or even multiple bit flips as in conventional SRAMs [20]-[22]. Heavy ions particles may also bring the state machine to an unpredictable state, triggering the erase or program operations in random locations. On the other hand, the floating gate cell can both lose its stored charge by several radiation induced mechanisms, and be permanently damaged by heavy ions or high radiation dose exposures. These vulnerabilities to ionizing radiation restrict the use of commercial (non rad-hard) high density Flash memories in radiation harsh environment, in all those applications that require very high reliability levels.

1.6 Conclusions

Besides memory density, which is measured in megabit per chip or per unit area, the retention time and the endurance of a nonvolatile memory are the most important factors.

Almost all nowadays Flash memories are based on the floating gate MOSFET. There are two way to arrange the memory cells in the array, NAND and NOR.

NOR topologies are optimized for high speed random read access times, but require more area and feature slow block write and erase times. Hence, NOR applications are well suited to store the firmware code or any information, which seldom requires to be updated.

NAND topologies feature slower random reads, good sequential read speed (thank to the internal pagebuffer) and good block write speeds. Furthermore, the NAND array requires much less area than its NOR counterpart. For this reason, NAND are used for mass storage devices (memory cards, USB pendrives, and solid state drives).

The floating gate MOSFET can be programmed either by channel hot carrier injection or by Fowler-Nordheim tunneling. The program operation increases the FGMOS threshold voltage by injecting electrons. On the contrary, the FGMOS is electrically erased only by Fowler-Nordheim tunneling, which allows electrons to escape from the floating gate back to the substrate. Excess of positive charge in the FG can also be achieved, but this may be a concern for NOR topologies.

Program and erase are very stressing operations, which degrade the dielectrics by generation of traps. The traps lead to leakage currents (SILC).

To limit the entity of leakage currents, the tunnel dielectric thickness must be kept over 7-10nm. However, this is in contrast to the scaling requirements, which need thinner dielectrics to keep short channel effects under control, as the cell area is scaled. Drain-induced-turn-on, which is due to the presence of the monolithic conductive floating gate also limits the cell scaling, in particular, its length. Consequently, new approaches have to be taken for the next technology nodes.

CHAPTER 2

Advanced Nonvolatile Memories: an Overview

As already discussed in the previous chapter, floating gate based Flash memories are facing several scaling issues, mainly related to the dielectric thicknesses, which cannot be reduced below a minimum value, without compromising the cell reliability. Furthermore, the floating gate capacitive couplings are becoming more and more concerning both in NOR Flash (causing the drain induced turn on) and in ultradense NAND Flash (FG to FG coupling) memories.

For these reasons, several other alternatives have been explored[3], in order to find suitable candidates to overcome the scaling issues. Among them, the new solutions can be grouped into two large and completely different approaches: the improvement of the Floating Gate MOSFET concept (discrete storage approach) and the employment of new structures and materials to associate the information to other physical properties.

With the discrete storage approach, the monolithic floating gate is replaced by a layer of discrete and insulated storage sites. Those storage sites can consist of either discrete trapping centers in a dielectric layer, or discrete nanodots. The charge is no more stored in a single monolithic electrode, but in several insulated sites. Examples of memories that implements the discrete storage approach are the nitride-based memories (SONOS, NROM™), which exploits the trapping centers of a silicon nitride layer, and the nanocrystal (either metal or silicon) memories. These memories have do not require new material and processes thus they are simple to manufacture, they are compatible with the standard CMOS process flow, and they can be inexpensively embedded in microcontrollers or DSPs. Furthermore, due to their intrinsic redundancy (the information is stored in several insulated nodes), they are more tolerant against leakage currents and single weak spots. This feature brings many advantages in terms of tunnel oxide scalability, because a defect will discharge only the neighboring storage nodes, provided that these sites are well insulated from each other. Furthermore, the process yield is increased, because a single weak spot is unable to affect the whole cell reliability. Furthermore, the absence of the monolithic conductive floating gate, drastically reduce the capacitive coupling issues (DTO and FG to FG coupling), greatly improves the cell scalability. Finally, the dual bit operation is very simple, programming the nodes either near the drain or near the source.

[3] And the research is still open, as many works are continuously published.

The other approach consists to associate the information to a particular physical property, such as the microcrystalline state (phase change memories, PCM), the magnetic state (magnetoresistive memories, MRAM) or the remanent polarization field (ferroelectric memories, FRAM). Other examples include the newly developed NRAM: the information is stored mechanically on an array of carbon nanotubes, acting as electromechanical switches. All these memories have both advantages and disadvantages. In fact, they require new materials or processes, which are difficult to integrate into standard CMOS processes. Furthermore, dual bit operation is somewhat difficult to achieve. However, these memories typically feature very high write/read speed, single bit alterability and very high endurance (in some case it is practically unlimited). This, together with their non-volatility, promotes those new approaches as universal memory.

In this chapter, we will provide a brief overview on some kind advanced nonvolatile memories, which have reached a good degree of popularity at least in the international scientific research community. For further details, the interested reader may refer to the references cited in the next sections.

2.1 Discrete storage memories

Discrete storage memories improve the floating gate memory concept by storing the charge in a layer of insulated nodes, being either trapping centers of a dielectric (typically, silicon nitride), or nanodots (nanocrystal memories). Recently, this approach is gaining gained popularity, as the conventional FG scaling issues are becoming more concerning [12]. Nowadays some semiconductor companies are already producing (or are investing many efforts in the development) these kinds of advanced memories, mainly in the form of SONOS, i.e. discrete charge trapping in a silicon nitride layer. In Fig. 2.1 the schematic cross sections of a nanocrystal and a SONOS memory cell are shown.

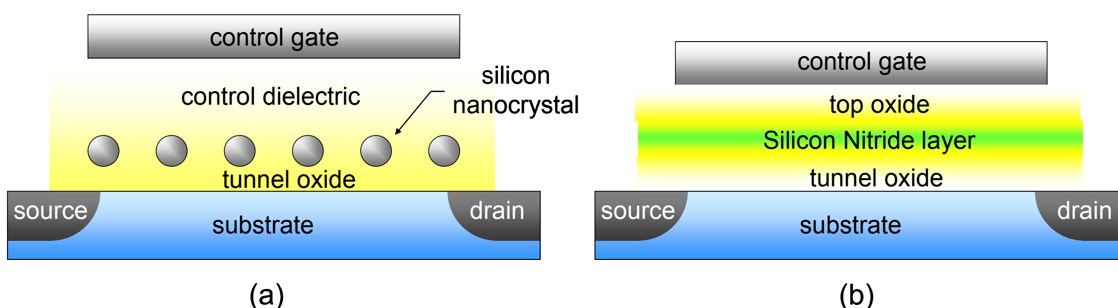

Fig. 2.1. Schematic cross-section of a nanocrystal (a) and a SONOS (b) memory cell.

The main advantage of this novel memory concept over the other alternatives is the simple fabrication processes, which is compatible with the conventional CMOS process flow, hence, those memories can be conveniently embedded in ULSI devices. Actually,

the absence of the floating gate makes in some cases nitride and nanocrystal memories more convenient than their floating gate counterpart [23].

From the scaling viewpoint, they allow the employment of much thinner dielectric layers, without compromising retention or the tolerance against SILC. Furthermore they drastically reduce the drain induced turn on and other capacitive couplings. The reduced dielectric thicknesses also allow much smaller voltages to be employed, greatly reducing the device power consumption and the space occupation by the peripheral circuitry. Furthermore, discrete storage memories allow simple dual bit per cell, being able to separately program the nodes either near the drain or the source, using CHC. The information sensing exploits the short channel effects. In fact, when the storage sites near the drain are negatively charged, the cell will show a low threshold voltage if the readout is performed at high enough drain voltages (1-2V). Conversely, if the storage nodes near the source are negatively charged, the cell will show a high threshold voltage, regardless the applied drain bias. This is because the high drain potential can screen the negatively charged storage sites near the drain, but not those near the source. In this way, the charge near the source can be sensed, regardless the charge stored near the drain. By exchanging the source and drain terminals (reverse read), and repeating the measurement at high V_{DS}, the charge near the drain can be sensed. Examples of forward and reverse I_D-V_{GS} characteristics of a nanocrystal memory cell storing two bits are shown in Fig. 2.2.

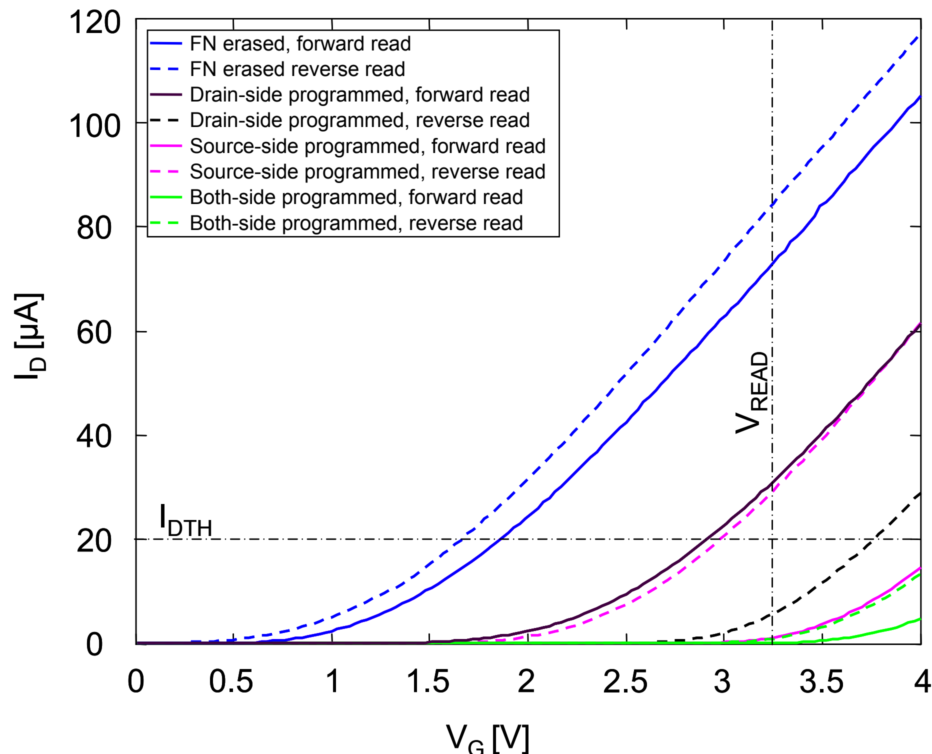

Fig. 2.2. I_D-V_G characteristics of a nanocrystal memory cells showing dual bit capability. If the cell is erased, the drain current at V_G=V_{READ} (I_D@V_{READ}) is higher than the reference value (I_{DTH}) in both forward and reverse reads. If the nanocrystals are negatively charged at both drain and source sides, the I_D@V_{READ} will be smaller in both reads. When the nanocrystals are negatively charged only at the drain/source, the reverse/forward reads give different readout values, allowing the discrimination of the stored information.

A major drawback, which has been reported on some nanocrystal and nitride based memories, is the irreversible charge trapping in the nitride layer[4] [24].

Nanocrystal memories require somewhat more complex fabrication methods with respect to nitride based memories. Furthermore, nanocrystal memories induce larger programming window dispersion due to random fluctuations in the number and spatial position of the trapping dots [25]. Nevertheless, nanocrystal memories suppress the Poole-Frenkel effect, which instead occurs on nitride traps, thus providing much better retention characteristics [25].

Nitride based memories are, at least in principle, simpler to manufacture, requiring only an oxide-nitride-oxide as gate dielectric stack. Still, the processing of the ONO layer is important, because it affects the device reliability and performance [26]. Overall dielectric thickness may vary, but they are in the range 4.5-5nm for tunnel oxide, 4-7 for the nitride layer, and 6-9 for the top oxide. [12].

Nanocrystals can be either metallic or silicon, both having advantages and disadvantages. Metal nanocrystal feature several benefits, such as higher density of states around the Fermi level, improved coupling with the channel, wide range of available work functions, and smaller energy perturbation due to carrier confinement. Furthermore, in silicon nanocrystal each electron induce a very large variation of the Fermi level, which is instead negligible in metal nanocrystal, owing to the presence of thousands of electrons in the conduction band, even when neutrally charged. On the other hand, silicon nanocrystal memories, in fact are much easier to integrate into conventional CMOS process flows.

Silicon nanocrystal can be synthesized in several ways, the most common being (see [27] and the references cited therein):

1) Ion implantation [27].
2) Aerosol deposition [27].
3) CVD [27],[28]

Of the three methods, the CVD method seems to be the most promising, because of the best control on the nanocrystal density, size, and both lateral and vertical spatial distribution.

Nanocrystal memories and nitride based memories can be programmed through CHC or FN tunneling, and, like conventional Flash, they can be erased through FN tunneling.

[4] This is not an intrinsic problem of nanocrystal memories and recent works showed that this issue has almost eliminated, either using optimized cell structures [25] or avoiding the ONO stack as control dielectric.

Assuming that the layer of discrete storage sites (nitride layer or nanocrystal layer), has thickness t_S, density n and the control dielectric has thickness t_C, the approximate relation between stored charge and threshold voltage variation is:

$$\Delta V_{TH} = \frac{qn}{\varepsilon_{Ox}}\left(t_C + \frac{1}{2}\frac{\varepsilon_{Ox}}{\varepsilon_{Si}}t_S\right)$$

For instance, if the storage site density is $5 \cdot 10^{11}$cm^{-2}, the control dielectric thickness is 12nm and the storage layer thickness is 6nm, the threshold voltage variation is 0.3V if each site contains one electron.

However, the actual threshold voltage and programming window depends on the readout current, as it will be discussed more in detail in chapter 4. On the contrary, this is not observed in conventional FGMs. This is due to the presence of the layer of discrete storage sites, which induce a non uniform potential on the channel. Furthermore, the storage sites non uniformity also plays a role on the threshold voltage and programming window dispersion.

Nonetheless, several works have shown the good potentialities of both SONOS and nanocrystal technology [23]-[31], even from the ionizing radiation viewpoint [32]-[39], due to the reduced dielectric thickness and intrinsic information redundancy. Furthermore nitride trapping memories are already commercially available from various semiconductor companies.

2.2 Phase change memories

In Phase Change Memories (PCM), the information is associated to the electric resistance of a chalcogenide material. The resistivity, in turn, depends on the microstructural state of the material: amorphous (high resistance) or crystalline (low resistance). One material, which is candidate to be employed as storage element, is $Ge_2Sb_2Te_5$ (Germanium-Antimony-Tellurium, GST).

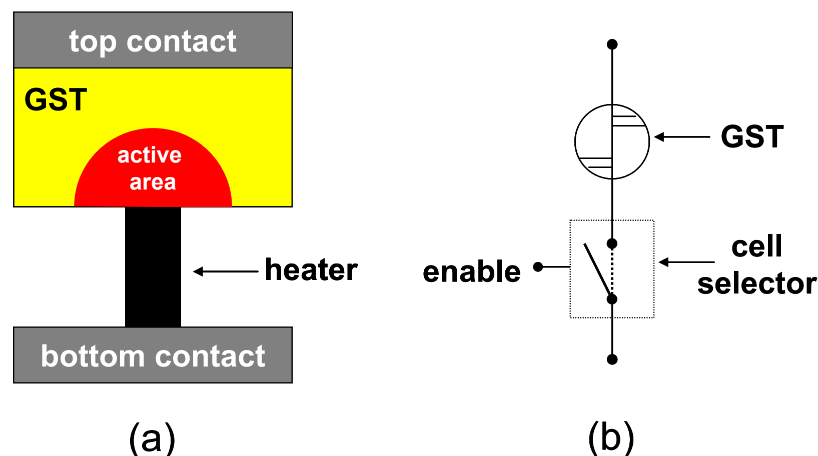

Fig. 2.3. Schematic cross section of a typical PCM memory cell (a). PCM memory cell with its cell selector (MOSFET, BJT, etc.)

The physics underlying the working principle of the chalcogenides is not fully understood, and several different models have been proposed [40]-[45].

Fig. 2.3 shows a typical PCM cell. Basically it consists of a chalcogenide material which is sandwiched between two metal elements: the top contact and the heater, which is, in turn, connected to the bottom contact. As its name suggests, the heater has the function to heat and melt the chalcogenide during the write operations. Noticeably, only a small fraction of the whole chalcogenide takes part into the write process (active area in Fig. 2.3). To be employed into the memory array, the PCM cell must be completed by a selector, being either a diode or a transistor (MOSFET or BJT).

Without going into details, the PCM working principle is very simple: when a high enough voltage is applied across the chalcogenide, being either in the amorphous or crystalline state, a large current flows through it (and through the heater), inducing a partial melting of the storage element. In this state, the active area is melt and it features no ordered structure. If the voltage is slowly removed and the temperature remains between 300°C and 500°C for a minimum "quench time", the chalcogenide tends to crystallize. Conversely, if the current (hence the heat) is quickly shut down, the chalcogenide cools down too fast to crystallize, hence it remains amorphous. Actually, the programming technique may be different. Fig. 2.4a summarizes the temperature evolution of the programming technique described above. The other programming technique depicted in Fig. 2.4b, consist of not to varying the cooling time (which would require the careful control of the voltage evolution during the cooling phase), but to use two different temperatures for the program (commonly called SET) and erase (RESET) operations. For the SET operation (i.e. low resistance, crystalline chalcogenide), the temperature reached is between 300°C and 500°C. On the contrary, for the RESET operation the temperature is brought above 600°C inducing the melting of the active area.

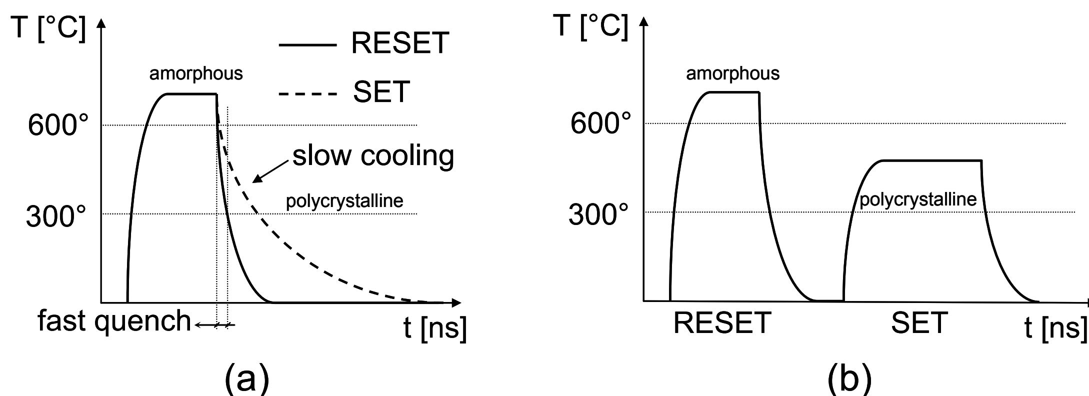

Fig. 2.4. Two methods to switch the state of a GST: time based (a), and amplitude based (b). 300°C and 600°C represent the glass-transition and the melting temperature, respectively. In the first method, the fall time of the temperature waveform determines the final state: if the fall time is rapid enough, the GST remains amorphous, conversely, if the fall time is long, the GST turns into its polycrystalline phase. In the second, the applied pulse amplitude control the temperature reached by the GST and, in turn, its final phase. In this case, only the RESET fall time is critical and must be faster than about 2ns.

It is worth remarking that thank to a physical phenomenon called electronic switching [42]-[44], the resistance is not constant as a function of the applied voltage, and it suddenly drops when high enough voltages (around 1.5V) are applied to the memory element. This allows to reach the high temperatures required for the phase change even if the current state is RESET (high resistance).

The SET and RESET operations are very fast and can be performed in times as low as 10 ns (the time required for the crystallization). However, those operations require very high currents and, despite the quite low voltages employed (up to 5V), strong charge pumps are required. Furthermore, PCM memories are programmed using high currents, hence they cannot be employed in NAND Flash memories[5]. Furthermore, the chalcogenide integration requires new processes and the cell selector must handle a rather large current. The latter reason implies that the selector is much larger than the chalcogenide cell itself, limiting the maximum integration. At this regards, a possible solution is to switch from MOSFET selectors to BJT selectors, however, the BJT integration requires additional process steps and the selector would be still much larger than the memory element [46].

Another limiting factor of this new technology is the strong requirements from the thermal viewpoint. In fact, being the SET and RESET operations thermally driven, the cell must be carefully optimized so that there is an enough thermal insulation between the cell and the adjacent elements (tracks, selector, and other cells). Insufficient insulation may lead to thermal crosstalk between adjacent cells (that is, the information stored in adjacent cells can be altered when one cell is written), or, even worse, to the contamination of the chalcogenide with the metals of the contacts, which would compromise the phase change capability .On the other hand, the heat must be quickly dissipated after a write operation, hence a careful tradeoff between insulation and dissipation must be performed. Nonetheless, the environment temperature may strongly impact the device performance or functionality. Furthermore, the strong temperature dependence may hamper the integration of this kind of memories into ULSI devices, which may reach very high temperatures. At this regard, SET and RESET voltages and current must be carefully chosen in order to grant the functionality in the whole operating temperature range: if the cell is not correctly programmed, it may feature zones with different phase states leading to a resistance, which is at intermediate values between the high and low resistance states.

Other problems derives from the so called read disturb: the cell readout voltage and current may induce the cell self heating if it is not properly controlled, possibly causing spurious electronic switching or slowly degrading the stored information. The SET and

[5] Actually, PCM array with NAND topology could be achieved by connecting the selector in parallel to the GST cell. In this way, when the cell is not selected, the cell selector shorts the GST, which then unaffected by the write operation. However, the “ON” resistance of the cell selector would pose a strong limit on “ON” resistance (hence the selector size) and/or on the number of cells in series per bit line, making NAND topology less attractive for PCM.

RESET operations, if not precisely controlled, may also lead to the permanent damage of the cells.

From the radiation viewpoint, chalcogenides memories do not suffer from charge loss as in conventional floating gate and discrete storage memories, but, in principle, radiation induced defect may still be a concerning issue, at high doses. Furthermore, heavy ions may strongly affect the state of the chalcogenides, if the heavy ion hits the active area.

Despite all those drawbacks, the fast write times, the single bit alterability, and the good endurance ([12],[46],[47]), make PCM very appealing as universal memory, especially as possible enhancement to SRAM and DRAM memories, adding the non-volatility, which also allow the device to be shut off without lose the stored information. PCM samples are also already available from some semiconductor companies.

2.3 Ferroelectric memories

Ferroelectric memories (FRAM) associate the information to the remanent polarization of a ferroelectric material. As it will be discussed later, FRAM allow single bit alterability, extremely high endurances, very high read and write speeds, low power and, of course, non volatility.

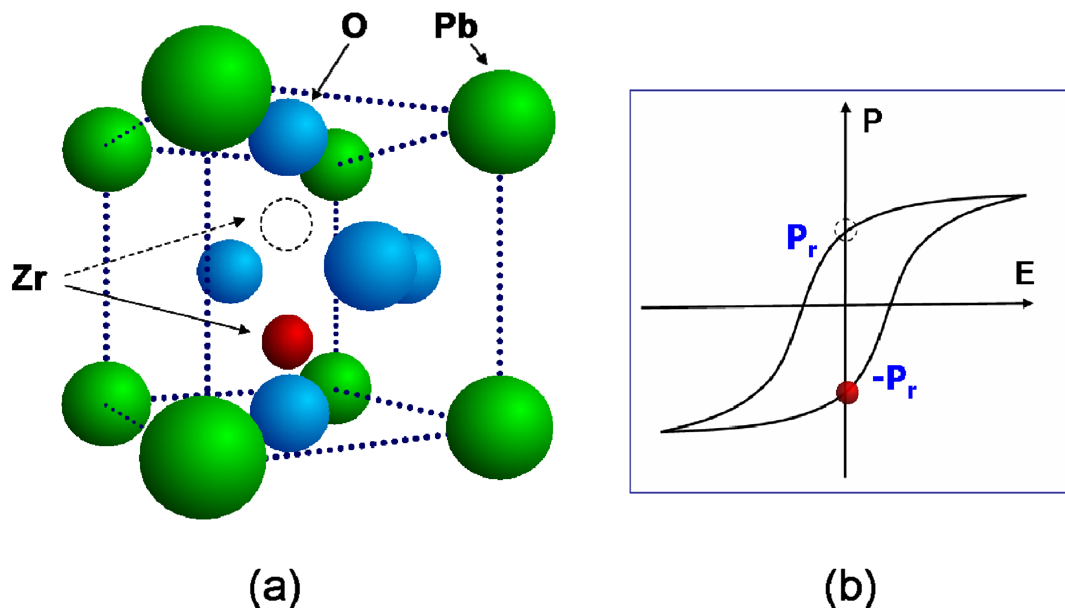

Fig. 2.5. PZT (Lead-Zirconate-Titanate) crystal structure (a), and hysteresis cycle of a ferroelectrics (b). The Zirconium atom has two possible stable states, each one characterized with its remanent polarization value (P_r or $-P_r$), which are shown with the solid red and hollow dashed circles in (a) and (b).

The ferroelectric property is a phenomenon which is observed in a class of materials commonly known as Perovskites. A typical crystal structure is depicted in Fig. 2.5a. The central atom has two equal stable low energy states, and its position can be switched by applying an external electric field, which will cause the atom to move toward the field direction. The field, in fact, switches the positions of the high energy and low energy states, hence the atom will move, following the low energy state. Each

one of the two stable states (see Fig. 2.5a) has a small remanent polarization because the crystal will act as dipole, each one having opposite polarization values (see Fig. 2.5b). The switching between the two states may be as fast as few nanoseconds, and actually the bottleneck would be the propagation delays of the peripheral circuitry, especially when driving large arrays.

In principle, there are several ways in which the remanent polarization of a ferroelectric dielectric can be sensed. The most promising and straightforward way is to embed the ferroelectric layer in a MOSFET (see Fig. 2.6). In this way, the remanent polarization would affect the effective threshold voltage of the ferroelectric MOSFET (FeFET), and the information, can be simply sensed using one of the widespread techniques adopted by other kind of memories. This technique has the obvious advantage to require only one transistor per cell (the FeFET), and this would allow to achieve very high memory densities. However, several technological issues, mainly due to the difficult integration of the ferroelectric material in the MOSFET structure[6], hamper this promising ferroelectric integration, and this technique is not currently used in commercial FRAM [48],[49].

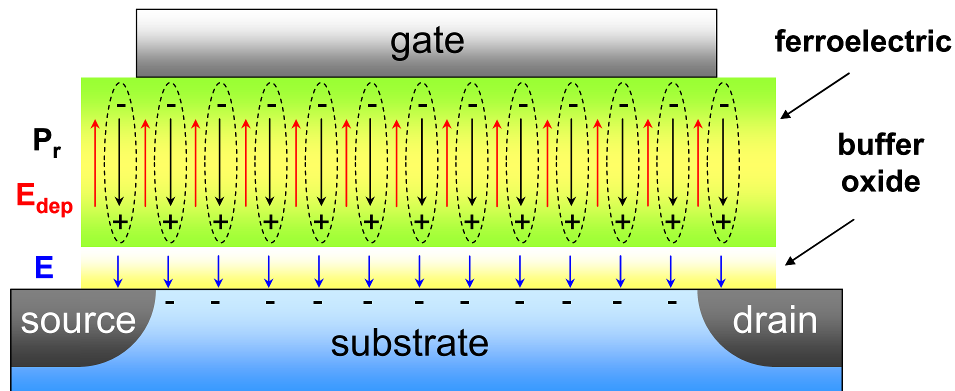

Fig. 2.6. Schematic cross section of a ferroelectric MOSFET. The P_r is the remanent polarization, while E_{dep} is the depolarizing field, which causes the reduction of the remanent polarization when the external applied field is zero.

Another way to sense the stored information is by using a capacitor, which employs the ferroelectric material as dielectric (the ferroelectric capacitor, see Fig. 2.7a). At this purpose, ferroelectrics have extremely high dielectric constants, hence very large capacitance values can be achieved even for small capacitor, facilitating the sensing circuitry, even for very thick (200nm) dielectrics. Several years ago, the memory cells required the employment of two capacitors and two selectors, strongly limiting the memory density [50]. However, in the last years, this limitation has been overcome, and nowadays ferroelectric cells employ a 1T-1C structure (see Fig. 2.7b). Ferroelectric and

[6] There are three main problems of ferroelectric transistors: the depolarizing field, the leakage currents and, in particular, the difficulty to achieve good interface between ferroelectric dielectric and silicon. In fact most ferroelectric films will easily react with silicon to form a nonferroelectric interfacial layer even at temperatures as low as 500 C [51],[52], which are easily reached during the manufacturing processes. Furthermore Pb may diffuse from the ferroelectric (PZT) into silicon, inducing several degradation mechanisms [52].

DRAM memories share the same memory array structure, as shown in Fig. 2.7c. However, FRAM require an additional plate line, required for the read/write operations.

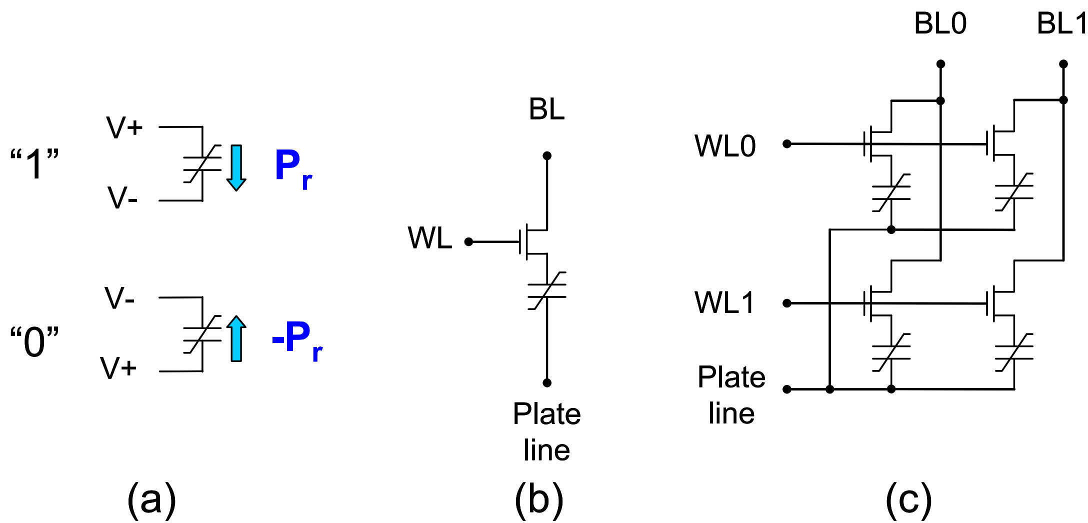

Fig. 2.7. Ferroelectric capacitor symbol and its polarization in the two logic states (a). The ferroelectric memory cell (b). Schematic of a 2x2 bit ferroelectric memory array (c).

When low voltages are applied to a ferroelectric capacitor, it behaves like a linear capacitor. However, if a high enough voltage (1-3V, [12]) is applied, the switching of the polarization induces an excess of charge (which can be seen as an increased equivalent capacitance), which can be sensed.

With reference to Fig. 2.8, when a cell is not addressed, the word line, the plate line and the bit line are held low (Fig. 2.8a). To read the memory cell, the plate line and the word line is held at V_{DD}, while the bit line was already precharged to 0V (Fig. 2.8b). Hence, a voltage of $-V_{DD}$ is applied to the capacitor, which may or may not switch, depending on the stored information (remanent polarization), "1" or "0". If the capacitor switches (polarization down, "1" in Fig. 2.8), then the induced charge Q_S will be shared with the bit line capacitance and the switched ferroelectric equivalent capacitance C_S. The resulting voltage in the bit line will be proportional to the $C_S/C_{BITLINE}$ ratio (Fig. 2.8c). If the polarization had been already up ("0" in Fig. 2.8), the capacitor would not have switched, inducing a much smaller charge, hence a much smaller bit line voltage (Fig. 2.8c). The ratio of these two voltages is greater than two, because of the equivalent capacitance of the switched capacitor is at least two times the capacitance of the unswitched capacitor (C_{US}). The information can be now sensed using a conventional sense amplifier and a reference, similar to DRAM, which drive the bit line, either high or low, for the switched and unswitched case, respectively (Fig. 2.8d). At the end of the read cycle, the information is lost, and for this reason this technique is called "destructive read"[7]. The information is restored by grounding the plate line, which forces the original polarization state if the bit line is high (Fig. 2.8e). After that, the cell

[7] Several non destructive read techniques have also been proposed in the literature, however most of them are based on the FeFET, see for instance [50].

is unselected by bringing the corresponding WL low, and the bit line is precharged to 0V, for the next read operation.

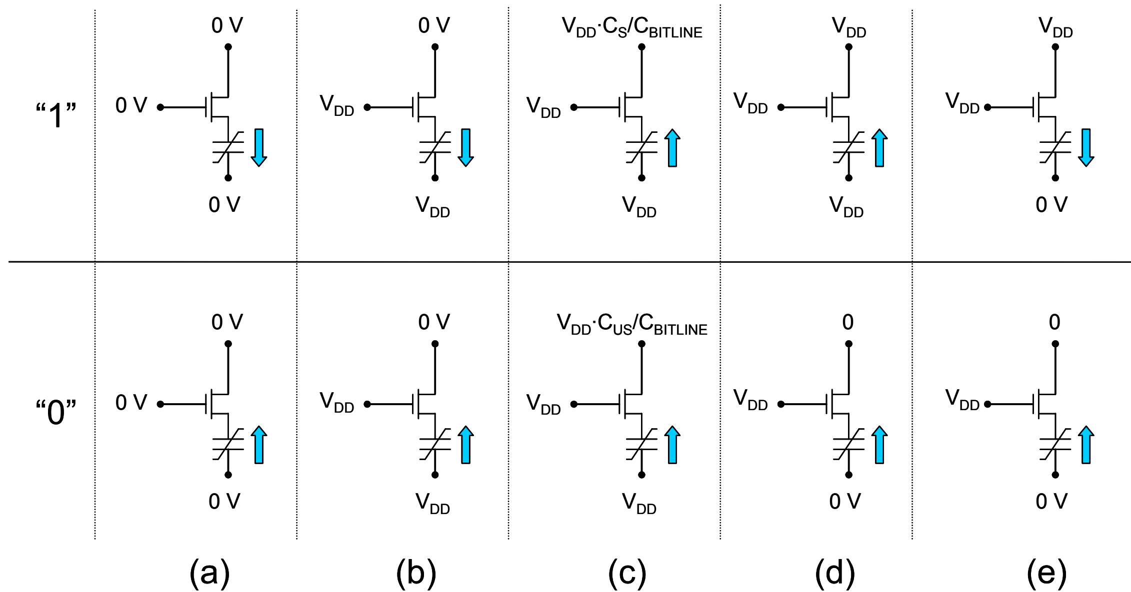

Fig. 2.8. Read operations for the "0" and "1" case. In the idle operation, the bit line, plate line and word line are forced to 0 (a). The plate line and the word line are forced to V_{DD}, and the bit line bias is removed (remaining precharged ad 0V) (b). After few nanoseconds, the bit line voltage is brought to $V_{DD} \cdot C_S/C_{BITLINE}$ or $V_{DD} \cdot C_{US}/C_{BITLINE}$, depending on the stored state ("0" or "1"). The sense amplifier restores the logic level on the bit line (d). The plate line is forced to 0V, restoring the previous polarization in the case "1", or leaving unchanged the stored information in the case "0" (e). Then, the voltages return to the case (a).

The write operation is much more straightforward and it is accomplished by simply selecting the cell and forcing the correct voltage to the ferroelectric capacitor. During both read and write operation, a small quantity of charge is switched, at the expense of the power supply. However, the energy required for these operations is much lower than any other kind of memories [12]. Furthermore, unlike SRAMs or DRAMs, the standby consumption is virtually zero, because there are neither pull ups in the array (like 4T-SRAMs) nor refresh cycles. This makes FRAM very suitable for all kinds of low power applications. Of course, when the memory cell is embedded in a complete memory device, the power consumption increases due to the external peripheral circuitry and the parasitics (the bit line capacitance, etc). Nonetheless the power consumption of FRAM is still much lower than FLASH devices. For instance to write 32kbit, 27μJ are required. This value is much lower than the typical 10.5mJ required for a conventional floating gate based EEPROM [53].

As previously mentioned, FRAM is also extremely fast and it offers practically unlimited number of write/read cycles (more than 10^{15} accesses on the earlier commercial devices), making FRAM as possible candidate as universal memory and SRAM and DRAM replacement in a wide number of applications.

However, like PCM, FRAMs uses uncommon materials, hence they require ad-hoc processes for their deposition. Furthermore, as already mentioned, FRAMs suffer from some technological scaling issues, such as the impossibility employ the ferroelectric material as gate dielectric, due to the poor ferroelectric to silicon interface [49],[51][52]. This, in turn, forces the uses of ferroelectric capacitors, which require a lot of area, especially if they are planar and not stacked or buried like in conventional nowadays DRAMs. In addition, the thickness of ferroelectric capacitors cannot be scaled down too much, because the dielectric layer lose its ferroelectric properties due to the depolarizing field when sizes are too small [54]. Depolarizing field not only reduces the ferroelectric properties, but also affect the retention [48]. Nonetheless, the very high dielectric constant of ferroelectrics may partially reduce the needs of the thickness scaling[8].

Like PCM, FRAM does not associate the information to an electric charge, hence they do not suffer from radiation induced charge loss. However, high radiation doses may still, in principle, alter the ferroelectric properties [55]-[59].

Currently, FRAM devices are already commercially available, but the integration levels are very low: to date, the maximum density is 16Mbit [60]. Nonetheless, their low power consumption and their high speed still grant them a niche market for several applications.

2.4 Magnetoresistive memories

Magnetoresistive memory (MRAM) is a nonvolatile memory, which associates the information to the ferromagnetic properties of some materials. The information is sensed by the magnetoresistive tunneling.

A MRAM cell is based on the magnetic tunnel junction (MTJ), which consists of two ferromagnetic plates separated by a thin insulating layer. One plate is a permanent magnet with a fixed field, while the field on the other plate can be switched.

The MRAM cell working principle exploits the fact that the tunnel effect preserves the electronic spin. The density of states (DOS) is spin dependent, and the two distributions (DOS_{UP} and DOS_{DOWN} for the spin up and spin down electrons, respectively) depend on the polarization of the ferromagnetic material. Referring to Fig. 2.9, in the first case, both the ferromagnetic plates are polarized in the same direction. Hence the two DOS will be much similar: lots of spin up electrons are available on the left plate, and a lot of spin up states are free at the right plate. On the contrary, if the two metal plate polarizations are opposite, they will feature almost symmetric DOS: a lot of spin up electrons are available on the left plate, but few free spin up states are available on the right plate; vice versa, few spin down electrons are available in the left plate, and

[8] Although the thickness reduction is desirable, because it would improve the cell planarity (therefore its compatibility with the CMOS process flow), the capacitor area scaling is most stringent, to achieve high densities.

lots of free spin down free states are available in the right plate. Since the electronic spin is conserved during tunneling, when a bias is applied to the two metal plates, the total current flowing can be expressed as the sum of two distinct currents, one for spin up electrons and another for spin down electrons. In the first case, (parallel polarization, see Fig. 2.9a) the I_{UP} will be large, due to the simultaneous presence of many electrons and many free states in the DOS_{UP} distribution of the left and right plate, respectively. I_{DOWN} will have a small contribution due to the small number of available electrons and free states in the DOS_{DOWN}. In the second case (antiparallel polarization, Fig. 2.9b), I_{UP} will be small due to the small number of available states in the DOS_{UP} distribution on the right plate, and I_{DOWN} will be negligible as well, because of the lack of many electrons in the DOS_{DOWN} distribution of the left plate. Hence, in the first case, the current will be high (low resistance), whereas in the second case, the current will be smaller (higher resistance).

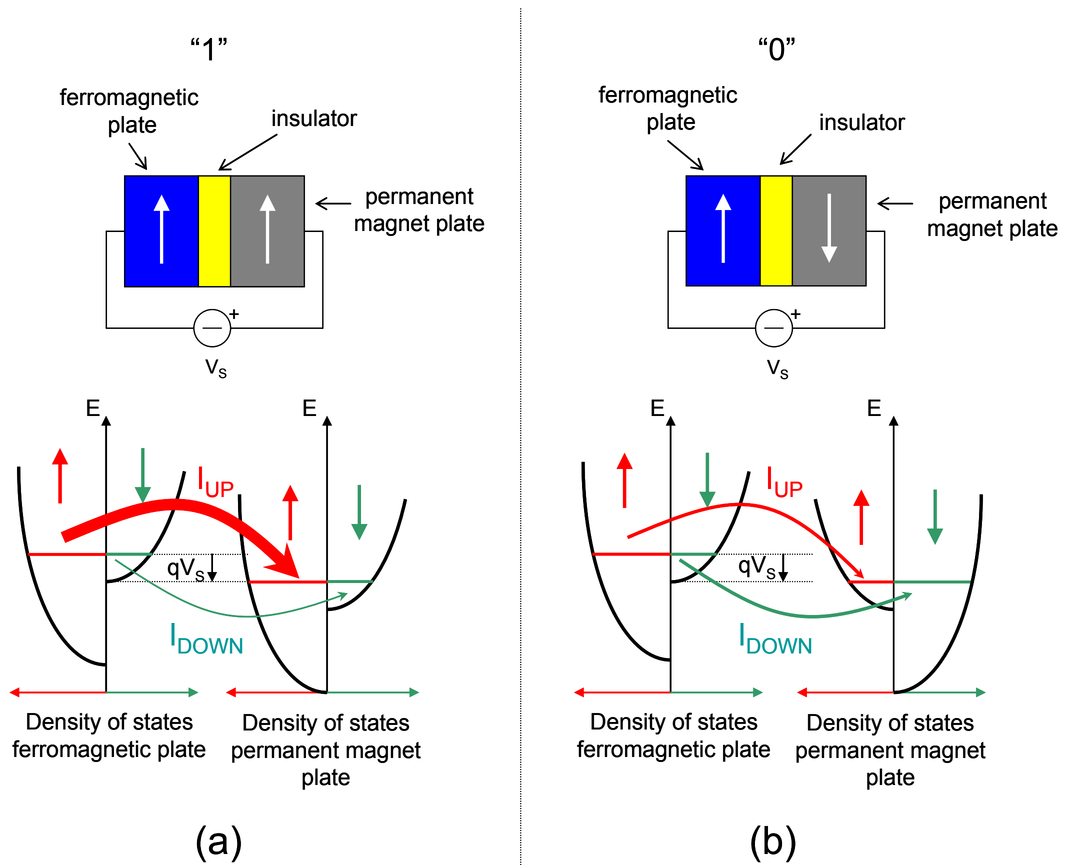

Fig. 2.9. Schematic cross section of the magnetoresistive tunnel junction and corresponding density of state for the two plates, for the "1" (a) and "0" (b) stored logic value.

There are several ways to implement a fully functional MRAM cell [61],[62]. A simple implementation is shown in Fig. 2.10. Besides the MTJ, an additional write line (arranged at right angles with respect the bit line) and the cell selector are required. The bit line is then connected to the sense amplifier. Other more sophisticated and optimized structures exist, whose treatment is beyond the scope of this thesis.

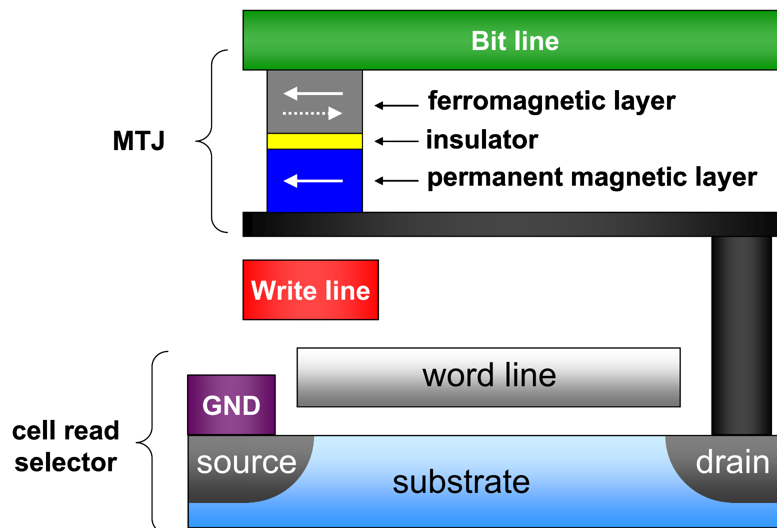

Fig. 2.10. Schematic representation of a MTJ cell with its cell selector and the write line.

The information readout is accomplished by turning on the cell selector: the sensing amplifier will detect the current flowing into the MTJ cell, hence retrieving the stored information. Data writes are performed by allowing the simultaneous current flow on the write and bit lines. Each current flowing in the bit lines and write line contributes for almost half of the total field required to store the information, hence only the cells, which are at the intersections between the "active" writes line and bit lines, s are programmed.

The program operation for this kind of memory is fast, but it requires high current levels. As a result, even if this memory does not require refresh like DRAM memories, it suffers from very high power consumption [12], especially if compared to FRAM memories (compare for instance FM22L16 available at [60] with MR2A16A available at [63]). Like FRAM and PCM, MRAM allows single word alterability, and, at least, in principle, MRAM features unlimited endurance, which allows to use MRAM also as SRAM replacement.

Besides power consumption, MRAM has several other issues. Firstly, it requires a very complex structure, even compared to FRAM or PCM, due to the presence of two write lines. Furthermore the MTJ is made of materials, which are uncommon in CMOS processes, hence it cannot be cheaply integrated in ULSI devices. The MTJ is also sensitive to heat and to external magnetic fields, hence appropriate device shielding is required. Furthermore, as the cell size is scaled down, magnetic crosstalk during write operation can lead to the corruption of the stored information in adjacent cell. New cell structures have partially solved this problem [64]-[66], at the expense of a much higher complexity from the manufacturing viewpoint, allowing to scale the cell size down to 90-65nm [67],[68].

Currently MRAM devices exist, but at small sizes (16Mbit at most). Like the FRAM market, further improvements could make this technology more compelling, especially as DRAM replacement, enhancing the DRAM speed and adding nonvolatility.

2.5 NRAM™ memories

Nano-RAM (NRAM) is an advanced nonvolatile memory developed by Nantero, whose conception is relatively recent. Unlike other kinds of memories, which are truly solid state (there are no moving parts), this kind of memory is nano-electromechanical. The NRAM memory arrays are based on a matrix of nanoscale switches, realized with carbon nanotubes.

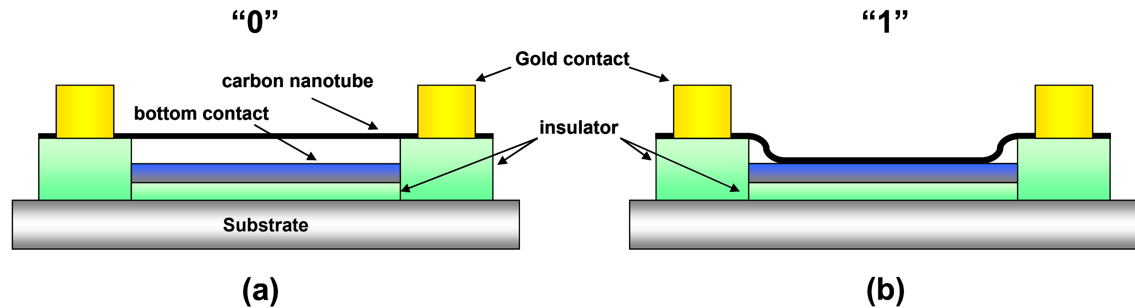

Fig. 2.11. Cross section of a NRAM memory cell, in the two opposite states, "0" (a) and "1" (b).

Fig. 2.11 shows a schematic view of the NRAM cell. The cell consists of one or more nanotubes suspended on two insulated island. The nanotubes are connected to the memory array through a gold contact. A metal electrode lies below the nanotubes. In this arrangement, nanotubes feature two stable states. In the first state, the nanotubes are physically suspended over the bottom metal electrode, making no electrical connection: when a small potential difference is applied to the two electrodes, the current is almost zero. This state is stable due to the low mechanical strain, which corresponds to a minimum of the potential energy. The other stable state is when nanotubes touch (or they are close to) the bottom metal electrode. In this position, the Van der Waals force is strong enough to overcome the mechanical strain, and the position is kept. In this case, a current flows if a small voltage is applied to the two electrodes, and it can be sensed by the external circuitry. Write operation can be performed by means of high voltage electric pulses [69],[70].

NRAMs are very promising from several viewpoints. Due to the presence of nanotubes, the memory cell can be scaled down to few nanometers in width and about 100 nanometers in length [12]. Speed is also very fast compared to Flash memories, requiring only few nanoseconds for the write operations [12]. NRAM are also low power devices, because very tiny currents are required for the program operations .These features make NRAM as possible candidate for universal memory for a broad variety of applications, such as DRAM replacement, mass storage, etc.

However, NRAM still features several drawbacks, mainly due to technological issues. First, the actual cell size is strongly limited by current lithography processes. Second, the controlled nanotube growth is still difficult and the process of selection and removal of unwanted nanotubes is commercially unpractical. Third, nanotubes are material uncommon on standard CMOS processes, hence ad-hoc facilities and manufacturing steps are required. Finally, despite the theoretical infinite endurance,

actual samples have shown only 50 millions cycles [12],[71], which is much higher than the conventional Flash, but much lower than other kind of advanced memories, such as FRAM o MRAM.

From the radiation viewpoint, NRAM are intrinsically stable, being electromechanical devices as shown in [72]. However high radiation doses or high energy recoil atoms (which can induce defects on the nanotube lattice), may still degrade the device performances, especially endurance.

2.6 Conclusions

Conventional Flash memories are facing several scaling issues, and new strategies are being evaluated to overcome these problems. Among the scaling issues, the dielectric thickness and the parasitic capacitive couplings are the most concerning. The alternatives can be grouped in two mainstreams: the discrete storage approach or the employment new memorization concepts other than charge storage, such as PCM, FRAM, MRAM or mechanical nano-memories (NRAM).

The discrete storage approach is an improvement of the conventional Floating Gate MOSFET, which consist in replacing the monolithic floating gate with a layer of discrete and insulated storage sites. In this way, the memory cell features an intrinsic redundancy and the stored information is much more robust against leakage currents than the conventional FGMOS. Furthermore, the absence of the conductive floating gate strongly reduces the parasitic capacitive coupling effects. Devices that implement the discrete storage are nanocrystal and nitride trapping based memories. These devices are easily implemented in conventional CMOS process and can also bring some improvements even in terms of endurance and programming speeds.

On the other hand, the new approaches consist in associating the information to physical properties, such as the micro structural state of a chalcogenide, the remanent polarization of a ferroelectric material, or the magnetic properties of a ferromagnetic plate. These new approaches features very high write and random read speeds, single bit (word) alterability and practically infinite endurance, which allow them to be considered as universal memories. On the other hand, these memories suffer from several specific problems and technological limitations, which are hampering their integration and widespread use. Furthermore, these memories employ uncommon materials and/or complex structures, which may be incompatible with the conventional CMOS processes and or may require additional fabrication steps with respect to conventional non volatile memories.

CHAPTER 3

Radiation Effects on Conventional Flash memories

Ionizing radiation are atomic (heavy ions), subatomic particles (protons, electrons, etc) or high energy photons (X-rays, γ-rays, etc), which release their energy to the matter through ionization, i.e. exciting and detaching the electrons from atoms or molecules. As it will be discussed later, some neutrally charged subatomic particles (neutrons) do not directly ionize the matter, but they are able to generate ionizing byproducts.

The effects of ionizing radiations on electronic systems have been object of intensive research and in the past two decades several books, works and review articles have been published [73]-[76]. The first observations of ionizing radiation induced failures on electronic systems or devices were made in the early 1960s. For instance, many concerns arose from the first satellite failures [77]-[80], which followed the detonation of high altitude a nuclear warhead during the Starfish Prime test of 1962. Interestingly, ionizing radiation was found also to be the cause of bit flips in some Intel DRAMs, in the 1970s: alpha emitter contaminants were unintentionally embedded in the packaging material. This latter event highlighted that ionizing radiation was a strong concern even for consumer applications, and many efforts were taken to avoid alpha emitter contaminations. Recently, in November 2003, the sun launched one of the largest solar flare ever recorded, which knocked down satellites and cellular communications [82],[83].

The ionizing radiation effects may vary, depending both on the radiation source (γ-rays, x-rays, electrons, protons, neutrons, heavy ions, etc.), its energy, the type of electronic devices (MOSFET, BJT, memory cell, etc.) and on the particular circuit and system they are embedded into. In the following sections, an introduction on the main radiation effects will be provided.

Beside military, there are several other fields in which electronics may operate in radiation harsh environments, such as high altitude flights and aerospace, medical, high energy physics, industrial, nuclear power, etc. applications. Furthermore, as the device sizes scale down, in principle less energy is required to trigger unwanted effects. This may be a concern even for commercial applications, even if they do not operate in radiation harsh environment: traces of alpha emitters contaminants or the small fraction of cosmic radiation which survives the interaction with the thick Earth’s atmosphere

may still be enough to induce measurable effects on electronic devices, as can be seen in Fig. 3.1 [84] and in [85]-[88].

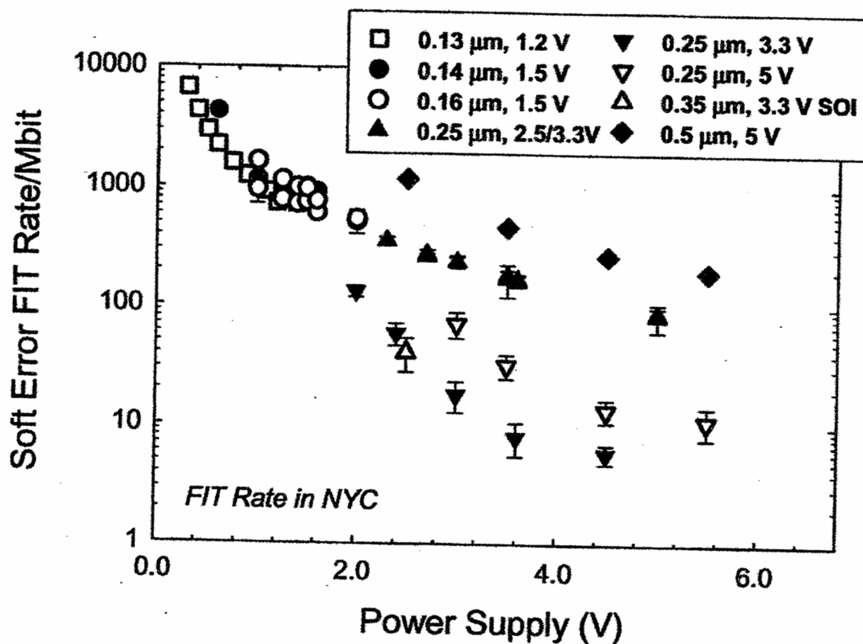

Fig. 3.1. Comparison of the soft error rates measured on SRAM devices manufactured with different technologies and with different power supply. Those value are expressed as FIT/Mbit (1 FIT = 10^9s) and they were measured at sea level [84].

3.1 Introduction to radiation sources and their interaction

There is a large variety of radiation sources, which may be produced naturally by radioactive decay, nuclear reactions (fission and fusion), solar flares etc. or artificially as in particle accelerators or x-ray tubes. For instance, the Earth is continuously struck by the so called cosmic rays, which are ionizing particles that impinge on its atmosphere. Cosmic rays have a very broad energy spectrum (see Fig. 3.2), ranging from few eV to over 10^{20} eV (several Joules per particle!) and consist in both charged and uncharged particles (e.g. neutrons, photons, etc.). Fortunately, most of the dangerous charged particles are captured by the Earth's magnetic field and trapped in the Van Allen radiation belts, and they become a concern only for those equipments operating beyond the low earth orbit. However, the interaction with the higher atmospheric layers creates a huge variety of byproducts (called air showers), which may reach the sea level. Among them, we found radioactive isotopes that are continuously created in the atmosphere (for instance by the reaction of a nitrogen atom with a neutron), protons, electrons, etc. Radioactive isotopes, in turn, may undergo in radioactive decay, releasing for instance alpha particles, electrons, γ-ray, etc. Additionally, the sun releases large quantity of high energy particles, threatening satellites. Nuclear power plants release γ-rays and neutrons, which affect the sensors used therein. Radioactive isotopes found in the terrestrial crust are also a source of ionizing radiation, and they pose a serious threat if unintentionally embedded in

packaging materials. Table 1 shows the alpha emission rate for silicon and many common packaging materials.

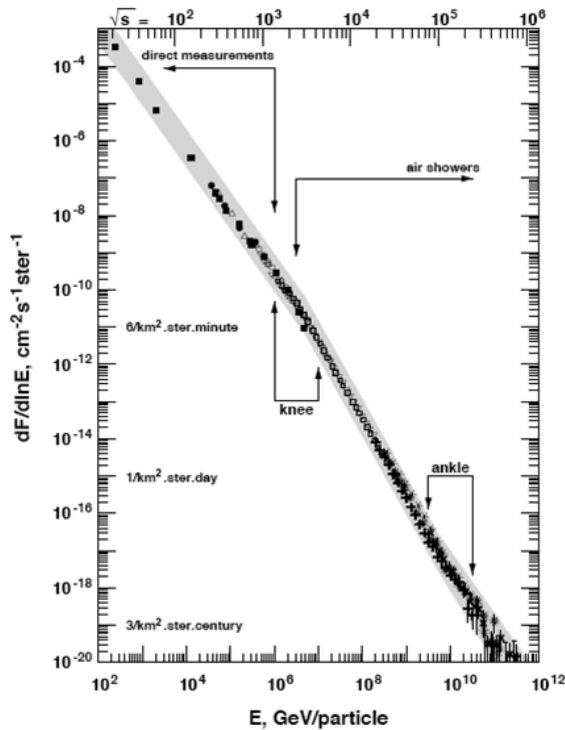

Fig. 3.2. Energy spectra of primary cosmic ray [89].

Material	Emission rate [$\alpha \cdot cm^{-2} \cdot hr^{-1}$]
Bare Si	0.00020
Plastic (epoxy)	0.00080
Ceramic lid A	0.15
Ceramic lid B	3.10
Ceramic DIP A	0.02320
Ceramic Dip B	0.03230
Ceramic Dip C	0.02610
Plastic DIP A	0.00109
Plastic DIP B	0.00124

Table 1. Emission rate of silicon and different packaging materials commonly used in electronic devices. The values are non zero even for bare silicon, indicating that the complete elimination of alpha emitter is almost impossible [90].

The most common ionizing particles are photons, protons, alpha[9] particles, ions, electrons and neutrons. These particles can be summarized to charged particles, photons and neutrons.

Charged particles interact with matters in three ways:

- By Coulomb interaction with electrons and nuclei, causing ionization and displacement damage, respectively.
- When being decelerated, causing photon emission with continuous spectra (bremsstrahlung). This is typical for electrons. The photons emitted may also induce other secondary effects, if their energy is high enough.
- By nuclear interactions (especially for high energy protons).

Photons may interact through:

- photoelectric effect
- Compton effect
- pair production

[9] Alpha particles and protons are actually ions (helium and hydrogen).

These effects, in turn, always end with the production of secondary electron/positrons.

Neutrons do not strongly interact with electrons, hence they cannot induce direct ionization. Still, neutrons can interact through elastic collisions with other charged particles (secondary charged particles), which in turn may ionize the surrounding matter. Elastic scattering of nuclei also produce displacement damage. Neutrons can induce nuclear reactions by capture or inelastic scattering, forming excited nucleus, which will eventually decay (i.e. emitting neutrons, protons, etc) or releasing nuclear fragments (fission).

Ionization in silicon typically induce transient currents, which may lead to soft errors[10], however ionization in dielectrics (or the injection in dielectric of ionized charge) may result in severe degradation of their insulating properties, up to catastrophic failures. Furthermore, some work in the literature estimate that the impinging ion may locally melt the dielectric [91]. Displacement damage increases the number of trapping/recombination centers in silicon, which decrease the carrier lifetime (this is very concerning for bipolar devices), and also affects dielectrics. Displacement damage becomes a concern also for thin metal traces [92].

3.2 Single event effects, total ionizing dose

Ionizing radiation effects may be grouped into two very different categories: single event effects (SEE), and total ionizing dose (TID) effects[11].

3.2.1 Single event effects

A single event effect is an unpredictable event caused when a single ion[12] impacts on sensitive areas of a microelectronic device. Along the ion track, hole-electron pairs are generated (see Fig. 3.3a), whose density depends on the particle properties, and in particular the linear energy transfer, which is the energy released to the matter per unit of length:

$$LET = \left(\frac{dE}{dx}\right)_{ioniz}$$

Sometimes, however, a different definition is given, and the linear energy transfer is given also by density unit.

$$LET = \frac{1}{\rho}\left(\frac{dE}{dx}\right)_{ioniz},$$

where ρ is the target material density.

In this thesis, we will always refer to LET as defined in the second definition. It is typically expressed in MeV·cm^2·mg^{-1}.

[10] Nonetheless, these transient currents may trigger latch-ups, which might be destructive.
[11] Actually, displacement damage is of great concern for many devices such as solar cells and BJT. However, this is a secondary effect and it is not a phenomenon due to ionization.
[12] Either the impinging ion or a secondary recoil ion.

Most of the radiation generated hole-electron pairs recombine within a fraction of (or some) picosecond [93]. The remaining fraction may diffuse, or, if an electric field is present, drift away separating electrons from holes (Fig. 3.3b).

If the generated charge collected by a sensitive node (e.g. a reverse biased p-n junction) of the device/circuit is larger than the critical charge required for triggering an anomalous behavior, a single event effect may be observed. In SiO_2, the generation and recombination follows the columnar recombination model [93],[94], which can produce clusters of defects in the dielectric, possibly creating localized permanent conductive paths or localized damaged regions.

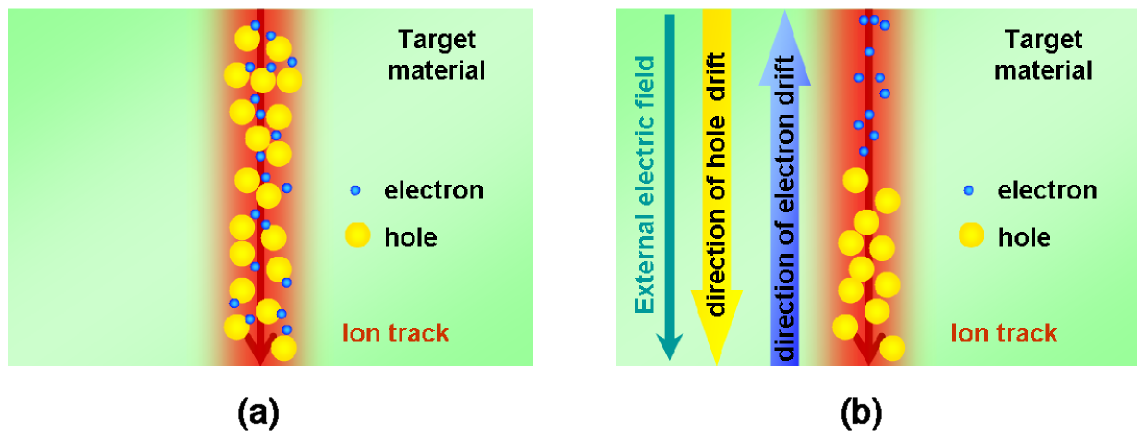

Fig. 3.3. Schematic representation of an heavy-ion strike. Along the ion path, a dense hole-electron pair track is generated (a). If an external electric filed is present during the heavy-ion strike, the electrons and holes surviving the prompt recombination drift away in opposite directions (b).

SEEs may vary, and may induce either non destructive and destructive phenomena (Soft Errors and Hard Errors, respectively).

Soft errors include (but they are not limited to): single event transients (SET), single event upset (SEU), single and multiple bit upset (SBU and MBU, a subset of SEU), Single Event Functional Interruption (SEFI) and Single Event Latch-up (SEL, when non destructive).

Single Event Upsets are the change of state or transient (single event transient, SET) induced by an energetic particle. Theses may occur in digital, analog, and optical components or may have effects in surrounding interface circuitry.

Single Bit and Multiple Bit Upset are event induced by a single energetic particle that causes single or multiple upsets (bitflip). This is typical in sequential logic or memories.

Single Event Functional Interruptions are the temporary interruption of a device or a circuit/system functionality (for instance, the temporary loss of power in a DC-DC converter).

Single Event Latch-ups are conditions, which cause loss of device functionality due to a single event induced high current state. An SEL may or may not cause permanent device damage, and (if non destructive) require the device power off to restore the normal operation.

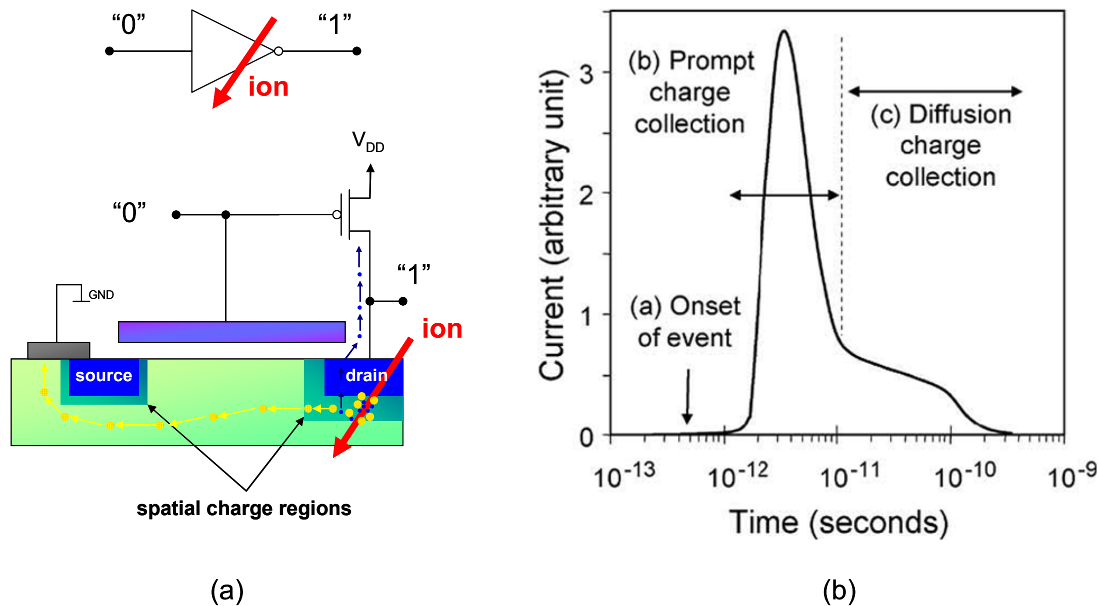

Fig. 3.4. Schematic representation of an ion strike on the drain diffusion of the NMOS of an inverter (a). A current discharges the output node capacitance generating a glitch. The current has two main contributions (b), the diffusion being the slower [95].

Soft errors typically are generated when a heavy ion strikes in a reverse biased junction such as the drain junction of a MOSFET in OFF state (Fig. 3.4a). A large amount of hole-electron pairs is generated and the carriers surviving the prompt recombination are separated by the field in the space-charge region, inducing an excess current. The ion strike also induces a local deformation of the potential, increasing the effective charge collection region. Charge may also be collected by diffusion. The diffusion current is somewhat lower, but also has a longer duration (Fig. 3.4b). It should be noted that as the feature size scales down, the number of sensitive nodes, which collect the carriers (by either drift or diffusion) increases. The excess current, discharges the output voltage node and it creates glitch. Depending on the capacitive load and on the band of the whole circuit, this glitch may propagate and be amplified (and in sequential logic, this may eventually induce a bitflip) by the following stages, or it may be attenuated. The amplification or attenuation depends on many factors and several researches [96]-[98] are still investigating this phenomenon.

Hard errors includes: single event latch-up (when destructive), single event burnout (SEB), single event gate rupture (SEGR), RILC, RSB, and stuck bits.

Single Event Burnout is a condition, which can cause device destruction due to a high current state in a power transistor.

Single Event Gate Rupture is a single ion induced condition in power MOSFETs which may result in the formation of a conducting path in the gate oxide.

RILC and RSB (radiation induced leakage current and radiation soft breakdown) appears in MOSFETs after a heavy ion strike, which induced a partial or strong degradation of the gate oxide insulating properties [99]-[102]. RILC may also appear after very high radiation dose exposures (see next subsection) [103],[104].

Stuck bits are faulty bits in memories, i.e. which cannot be programmed anymore and they are “stuck” at either “0” or “1”.

Hard errors can be generated when the ion strike hits either a junction (triggering destructive latch-up events or burnouts), or when the ion strike destructively impact on dielectrics, leading to SEGR, stuck bits, and so on.

SEE can be measured even at the sea level (see for instance [84]), but, for an accurate investigation, they would require either very long testing times or a very large number of samples, to observe a statistically relevant number of SEE (see for instance data of Fig. 3.1). Furthermore, the particle type, energy and LET cannot be selected, and the occurrence of high-LET ions decrease very rapidly with increasing LET. Hence, most of SEE radiation experiments are performed using particle accelerators, using radiation sources with known LET and energy.

Typically a very large amount of particles are accelerated toward the target. The number of impinging particles per unit area and per second is called *flux*. The integral of the flux over the time is called *fluence*, and it represents the cumulative number of impinging particles per unit area.

3.2.2 Total Ionizing Dose

Contrarily to single event effects, total ionizing dose effects include all the (long term) electrical/optical/etc characteristic modifications, induced by the cumulative ionizing radiation dose adsorbed by the device. While SEEs come from strongly localized (both in time and in space) energy adsorption, TID effects are induced by the gradual and uniform adsorption of energy, released by a somewhat continuous flux of ionizing low-LET particles. The total adsorbed dose is defined as the energy adsorbed per mass unit:

$$TID = \frac{\text{Energy to ionization}}{\text{target mass}}$$

While the SI unit is the Gray, the rad is still widely used in the literature. 1 Gy = 100 rad.

Ionizing radiation sources (typically, electrons and photons, but also protons) may be characterized by its dose rate, which is the dose which releases to the target per unit of time. Hence, assuming a constant dose rate, the total adsorbed dose is simply:

$$TID = \int doserate(t)dt = doserate \cdot T_{irradiation},$$

where, in the last step, the dose rate has been assumed constant.

If the fluence and the LET of the radiation source are known, the TID adsorbed by the device can be evaluated with:

$$TID = LET \cdot fluence$$

Several radiation sources can produce TID, e.g., x-rays, γ-rays emitted by ^{60}Co, high-energy electrons and protons. Due to the very low density of radiation-induced electron-hole pairs, immediately after their generation the two carrier tend to recombine in time as short as few picoseconds [105], accordingly with the geminative recombination model [106], i.e., each carrier recombines with its own partner. Carrier ionization and recombination can produce trapped charge, bulk defects or interface defects. The energy released by the recombination process might generate defects in the bulk oxide or at the semiconductor/dielectric interfaces [73],[76],[106],[107]. Such traps are responsible for the majority of degradation mechanisms in MOS devices, such as the Radiation Induced Leakage Current (RILC) [103],[104], which consists in a parasitic leakage current due to a tunneling process assisted by the radiation induced neutral traps in the oxide. When traps are close to the silicon/oxide interface, they might affect the subthreshold region of a MOSFET, increasing the subthreshold swing and the threshold voltage. The recombination process is influenced by the electric field, which tends to separate the pair avoiding the recombination and producing also trapped charge [73],[76], which in turn moves the MOSFET threshold voltage.

Displacement damage may also progressively increase the trapping/recombination center density, which reduce the carrier lifetime and strongly impacts in diodes (including photo-electronic devices) and BJTs. BJT also are peculiar because they feature the so called enhanced low dose rate sensitivity (ELDRS), which were discovered in the 1990s. The interested readers may refer to [108]-[110] and the references cited therein.

3.3 Radiation effects on Flash memories

3.3.1 Overview

The FG MOSFET may be susceptible of both SEE and TID effects, which interact with the dielectric layers and may corrupt the stored information. In addition to all the radiation effects observed in the conventional MOS devices, FG-based memories present some peculiar radiation effects, due to the presence of the storage medium, i.e. the floating gate. Among them, the most important issues are the prompt charge loss after irradiation and the long-term data retention degradation, which may hamper the correct functioning of a Flash cell also at low doses. At higher radiation doses, also the permanent radiation effects on the electrical characteristics become a concern, because they can produce a permanent shift of the effective cell threshold voltage[13], increased drain leakages due to junction degradation or parasitic lateral MOSFET conduction [111]-[113], similarly to the conventional MOS devices. Actually, the permanent

[13] Due to trapped charge in the dielectrics and mobility and sub-threshold slope degradation.

damage effects are much more concerning in the peripheral circuitry, because of the increased leakages, threshold voltage variations and mobility degradation, which strongly affect the charge pumps. Still, those effects are also dangerous for the correct sensing of the information stored in the cell memory array.

In the following, we will discuss the most important radiation effects on NVMs, mostly focusing on the data retention and the prompt charge loss. TID induced permanent damage on the electrical characteristics will also be briefly treated at the end of this chapter. SEE effects on the peripheral circuitry are very important, as they may trigger unwanted program/erase cycles (leading to data corruption), bring the state machine into an unpredictable state, or cause SEL or SEGR, especially on the ESD protections or in the high voltage circuitry. However, SEEs on the peripheral circuitry are outside the scope of this thesis. A detailed analysis can be found in the references cited in this chapter.

3.3.2 Prompt Charge Loss due to TID

Fig. 3.5 summarizes the effects of the charge loss due to the TID taken from results reported in the literature on irradiation of Floating gate memories with ^{60}Co γ-rays [114]. In particular, Fig. 3.5a shows the threshold voltage (V_{TH}) probability as a Weibull plot for FG arrays programmed in the “0” and “1” state before and after different γ-rays TID levels. During irradiation, the FGs are progressively losing their charges. Consequently, the threshold voltage of all FGs programmed at high V_{TH} value uniformly moves toward lower V_{TH}, due to the loss of negative charge. The low V_{TH} distribution features the opposite behavior, due to the loss of positive charges. The progressive closure of the programming windows as a function of the TID is shown for the same device in Fig. 3.5b [114]. Similar results have been reported for other TID sources, such as X-rays and protons [115],[116].

Two important mechanisms contribute for the charge loss:

1) *Neutralization of the FG stored charge due to the electron-hole pairs generated by ionizing radiation in the tunnel oxide and/or ONO stack, which are in turn injected through the oxide.* Irradiation generates electron-hole pairs in all oxides surrounding the FG [73],[76]. Part of these carriers suddenly recombines, depending on the oxide electric field [73],[76]; due to their high mobility, the electrons that survive the prompt recombination, quickly thermalize and are swept away from the oxide [117]. Instead, the holes slowly move across the oxide by drift or diffusion and may be trapped in the bulk oxide or silicon/oxide interface or may move toward the FG [116]. The fraction of holes reaching the FG recombines part of the stored charge.

2) *Photoemission*[14]. The incoming radiation can directly interact with electrons/holes stored in the floating gate transferring enough energy to the carrier,

[14] The literature distinguishes between the photoemission of the stored FG charge, and the injection of the radiation generated charge. Still, here we consider them as an unique phenomenon.

which may jump over the oxide barrier. In addition, photoemission may occur also in the substrate and in the control gate. Part of the electrons/holes generated by the ionizing radiation in the substrate or control gate can jump the barrier and reach the FG, neutralizing the stored charge. The balance between substrate photoemission, control gate photoemission, and FG photoemission depends on the applied electric field and the polarity of the charge stored in the FG [119]. Incidentally, photoemission was the physical principle for the EPROM erasure.

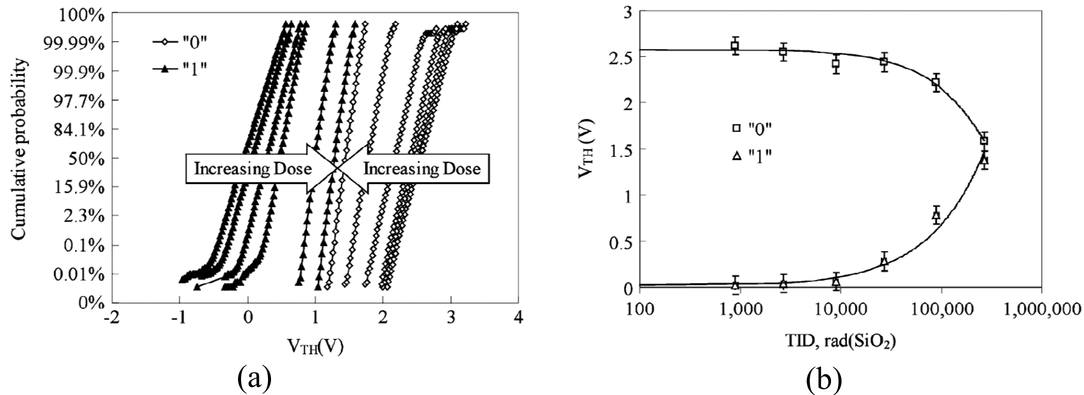

Fig. 3.5. a) Cumulative threshold voltage distributions of floating gate memories programmed at "0" (squares) and "1" (triangles), for different total ionizing doses: fresh, 9krad(SiO_2), 27krad(SiO_2), 90krad(SiO_2), 270krad(SiO_2), 900krad(SiO_2) [114]. b) Evolution of the average threshold voltage of floating gate memory cells programmed at "0" (squares) and "1" (triangles), as a function of the total ionizing dose [114].

3.3.3 Prompt Charge Loss due to SEE

SEEs are generally produced by heavy ions, which produce a dense electron-hole pair track around their hit positions. Fig. 3.6a summarizes the effect of heavy ion irradiation on the threshold voltage distribution of a FG memory (taken from [118]). The chip was irradiated with 2×10^7 iodine ions/cm^2. Before irradiation, the V_{TH} distribution has the expected Gaussian shape. After irradiation, the V_{TH} distribution exhibits a secondary peak around 6V, due to the cells that experienced a charge loss after the ion hit. The amount of charge loss depends on the program status of the cell, on the impinging ion LET, and the technology node [119]-[121]. For instance, Fig. 3.6b shows the number of errors as a function of ion fluence for different LET values (from [120]). For high-LET ion irradiation, almost the 100% of hit cells fails. As the Moore's law proceeds, the shrinking transistor sizes, featuring smaller and smaller FGs, makes them more and more sensitive to the impact of a single ion. A single ion strike may produce even multiple bit flips, as soon as the cell size and spacing become smaller than the ion track size [121].

Even though the formation of the secondary peak is not unexpected, because of the high energy released by the ion hit, its physical origin is source of some controversies. In principle, the appearance of the secondary peak in the V_{TH} distribution can be explained in a way similar to the rigid shift of the V_{TH} after TID, with the additional consideration that the heavy ion releases a huge quantity of energy in a very small volume (the so-called *microdose effect*) and only in a small percentage of cells.

Neutralization and photoemission may locally occur leading to the complete or the partially discharge of the hit FGs. Based on the columnar recombination model, several thousands of electron-hole pairs should be generated in the tunnel oxide by a single ion, depending on its LET coefficient, but only a small fraction of these pairs (in the order of some tens) survives the prompt recombination [93]. The surviving electrons are quickly swept toward the substrate, thanks to their high mobility [117], whereas holes slowly move toward the FG, where they recombine with part of the stored negative charge. The same could happen in the ONO stack. Nonetheless, this estimation is not in agreement with the number of charges, which are stored in the floating gate. In fact, assuming a floating gate capacitance[15] of 1fF, a 1-V shift of the cell threshold voltage corresponds to a charge loss of more than 6000 electrons.

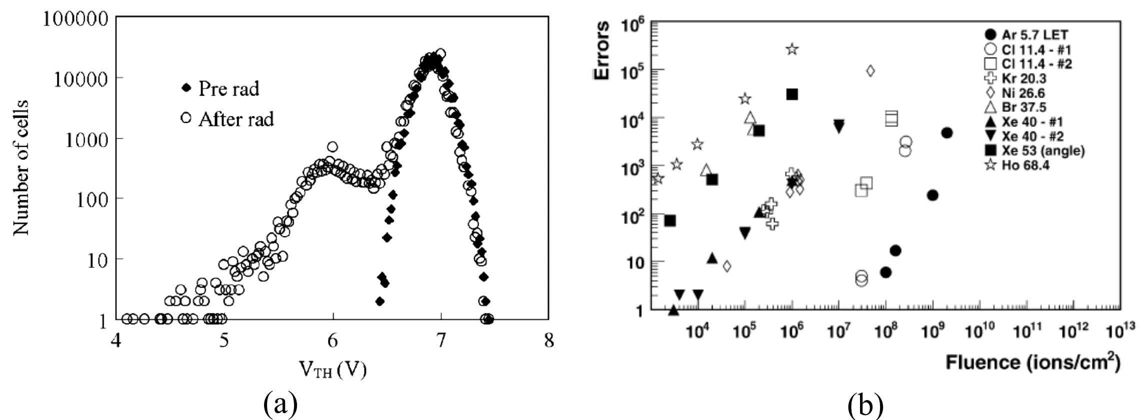

Fig. 3.6. a) Threshold voltage density distribution of floating gate memory cells before (diamonds, filled) and after $2 \cdot 10^7$ iodine ions/cm^2. Very large threshold voltage variation (as high as 3V) are observed [118]; b) number of errors as a function of the ion fluence and LET coefficient. For high-LET ions almost the 100% of hit cells fail. [120]

A pseudo model that tries to explain the much larger charge loss was presented[16] in the years 2004-2006 [122]-[124] by Cellere et al., but it lacks of consistent physical explanations of the origin of the proposed phenomena. Following this model, the dense track of electron-hole pairs should form a conductive path, which shorts the floating gate with the substrate. In those aforementioned works, it has been supposed that the resistance of such path depends on the oxide thickness, i.e., the length of the path, and on the ion LET coefficient, i.e., the amount of ionized charges. If the floating gate cell is considered as equivalent to the series of two capacitors: one between FG to substrate, source, and drain junctions and one between FG and Control Gate, the formation of a resistive path across the tunnel oxide, can discharge the floating gate. The amount of charge loss depends on the RC constant of the equivalent circuit and the time needed to shutdown the ion-strike-induced conductive path. Such time has been estimated based on considerations on the times needed for carrier recombination and on electron mobility in about 10fs, in agreement with several published works on related topics [91],[93],[125],[126]. Even though this phenomenological model can fit the experimental data, recent works questioned about the validity of the transient

[15] This value is very high for nowadays memories, which feature values below 0.1fF.
[16] With several contradictions.

conductive path [39] and the lack of physical details of the mechanisms governing the path resistance and oxide barrier lowering [119]. Furthermore, the transient conductive path, which should have a strong effect only within few nanometers from the ion track, cannot explain why severe charge losses occurred even in neighboring cells, as reported by the same proposing author [121],[127]. In fact, the cells analyzed in the aforementioned works had sizes larger than 65-90nm (in particular the distance between adjacent floating gates is larger than 100nm, as can be seen for instance in Fig. 1 of ref [121]). These values are much larger than the expected transient conductive path width. Still, the charge loss of those cells, which were not directly hit, could not be quantitatively explained by the recombination of the charge generated in the oxide with the FG stored charge. It may be argued that the transient conductive path is much wider than originally thought (i.e. in the 100nm range versus 10nm). Nevertheless, this is inconsistent with experiments performed on nanocrystal memories and with other works, as it will be discussed in chapter 6.

A more consistent and compelling model points to photoemission of ion-induced hot electron-hole pairs from the substrate and the polysilicon control gate, which are in turn injected across the tunnel oxide and IPD though the FG, neutralizing a fraction of the FG charge. The results of this model agree with recent simulation results by Dodd [128], which reported that the ion track size in silicon are much larger than in the oxide and is in the order of several tens of nanometers. This model also agrees with the experimental results of Cellere et al. (proposing author of the transient conductive path) and with both the experimental and simulation results on nanocrystal memories [37],[39].

3.3.4 The long-term retention capability

One of the most important aspects of a non-volatile memory is its retention capability, which is typically at least 10 years [12]. Ionizing radiation can severely compromise the retention of FG memories. The irradiation effects may vary, depending on the type of irradiation: heavy ion or TID.

Several works in the literature [38],[129]-[131] reported retention experiments carried out on FG memories irradiated with heavy ions. In all these works, it has been highlighted a very poor retention on those cells hit by at least one ion, while the retention of non-hit cells was unchanged. For instance, Fig. 3.7a show a typical V_{TH} distribution as a Weibull plot of an irradiated Flash memory array (from [130]), reprogrammed after irradiation and measured immediately after program, after 1.5 hours, 48 hours, and 164 hours. Even though immediately after program the whole cell distribution resembles that of fresh (not irradiated) device, just after 1.5 hours a large tail appears, indicating a slow charge loss only from the hit cells. Such tail is a signature of the formation of permanent leakage path across the dielectrics. Further characterizations, performed at longer times after the reprogramming, showed a

broadening of the tail, indicating that there were other FG cells, which had smaller leakage currents.

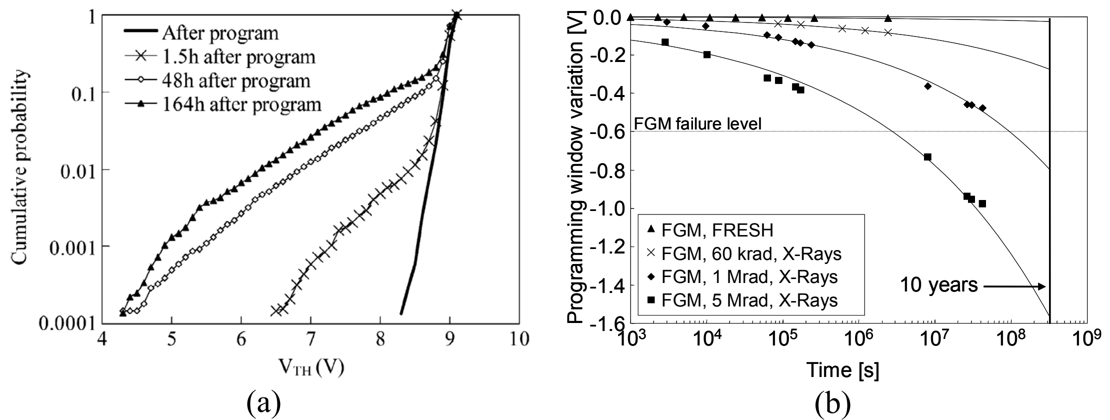

Fig. 3.7. a) Retention test performed on floating gate cells, which were identified as hit by a single iodine ion. Large threshold voltage variations as high as 5V indicate that the retention can be severely compromised by heavy ion hits. [115] b) Retention test performed on floating gate memory arrays irradiated at different doses with X-rays (data taken from [38]). The failure level is taken as the 20% of charge loss closure [2]. The evolutions show that even after only 60krad(SiO_2) the retention is strongly modified. The device is expected to fail before the 10-years if subjected to 1Mrad(SiO_2). The retention fails after 4 months (about 10^7 seconds), if the device is irradiated with 5Mrad(SiO_2).

Few works in the literature [38],[116] showed also the TID effects on FG cell arrays. Some results are shown in Fig. 3.7b (data taken from [38]). The retention of a irradiated FG cell arrays is appreciably modified with respect to the non-irradiated devices, even after only a 60-krad(SiO_2), while variation as large as 1V are expected after 10 years if it is irradiated with 1-Mrad(SiO_2). From the application point of view, TID effects on the retention appears somewhat less concerning, at least at irradiation doses below 100krad(SiO_2). In fact, at levels in the 100-krad(SiO_2) range, the Flash memory chip starts failing due to excessive peripheral circuitry degradation, which has been identified as the weak point of a commercial device [132]-[134]. Still, employing radiation hardening techniques on the peripheral circuitry can bring this failure level to higher values and data retention might become a more concerning issues even after TID.

The progressive cell threshold voltage variation on irradiated devices derives from the formation of oxide neutral traps (after TID) or cluster of defects (after heavy ion irradiation) in the tunnel oxide. Such neutral traps are responsible of the onset of the well known radiation-induced leakage currents [103],[104] and the Radiation Soft Breakdown [99]-[102], which slowly discharge the FGs. It is worth to note that even very small RILC value (below the aA range) should be enough to discharge the FG in approximately 1 hour. The physical nature of the oxide traps that lead to the RILC was investigated in several works, and it resulted similar to the traps responsible for the well known stress induced leakage current (SILC) affecting the thin gate oxide after

electrical stress. The interested reader may refer to the numerous studies in literature for more details (see for instance [135]-[138]and the references cited therein).

3.3.5 Permanent degradation effects on the FG MOSFET and on the peripheral circuitry

As already mentioned, ionizing radiation can also produce permanent or quasi-permanent[17] modifications of the electrical characteristics:

1) Oxide trapped charge in the gate oxide varies the flatband and hence the threshold voltage. Typically, positive charge is trapped within the oxides, and the threshold voltage decreases. This may also partially increase the off-state leakage.

2) Positive charge trapped in the lateral oxide may also induce small, always-on conductive paths between source and drain at the edge of the channel, increasing the drain leakage [111]-[113].

3) Radiation generated interface traps increase the subthreshold slope. The increased subthreshold slope reduces the I_{ON}/I_{OFF} ratio, it increases the effective threshold voltage, and it enhances the off-state leakage. Furthermore, the interface traps affect carrier mobility, reducing the maximum drain current.

4) Drain junction degradation at very high dose levels increase the drain leakage.

In principle both TID and heavy ion (due to microdose effects) induce permanent damage. However, heavy ion effects are limited to a much localized area. In the following, we only discuss the TID effects and the whole memory device is assumed to be irradiated.

Those effects may involve both the memory array and the MOSFETs of the peripheral circuitry.

Considering the cell array, all those effects, which affect the effective cell threshold voltage, may reduce the memory reliability because they reduce the sensing margin. Furthermore, a typical phenomenon in nMOSFET is the “rebound effect”: at low doses, the main effect is the positive charge trapping, and the cell threshold voltage decreases. At higher dose levels, the increased subthreshold slope induces an increase of the effective threshold voltage. Hence, the threshold voltage variation is not monotonic, further complicating the sensing margin requirements. Annealing also induce partial recovery of the threshold variation, inducing strong fluctuation as the time elapses. Leakages also affect the sensing margin, both in NAND and in NOR topology. In NOR applications, several cells are connected to the same bit line, therefore the leakage in the

[17] Some radiation effects may anneal. The time required for annealing may be as short as few minutes, but it may last for months or even years.

bit line is multiplied by the number of the word lines[18]. Hence, even small leakages may induce large read disturbs, which must be accounted. Conversely, in NAND applications, cells are connected in series, hence there is only one leakage contribution per bit line. However, as mentioned in chapter 1, the current levels in NAND applications are much lower (200nA versus several tens of μA).

The peripheral circuitry of commercial Flash devices has been proved to be the bottleneck from the radiation tolerance viewpoint. In fact, several devices have been reported to fail for doses as low as 10 krad(SiO_2) [132]-[134], which is fairly low level for satellite or other space applications [92]. High voltage charge pumps and peripheral circuitry are the most affected because of their thicker oxides, which render them more vulnerable to charge trapping [73], inducing threshold voltage variation. Leakages also are concerning especially for NAND applications, where the programming current (performed through FN tunnel) are very low, hence they are not manufactured to sustain very high loads, which may be represented to leaky pass transistors or other devices. Furthermore, the reduction of the mobility (or the strong subthreshold slope degradation) may negatively impact on the charge pumps. Sensing circuitry may also be affected by threshold voltage variations. Finally, all those timed operations may be compromised by the increased effective ON resistance of the MOSFETs, which is determined by the threshold voltage and the mobility.

Noticeably, the effects of the interface trap generation are more pronounced if the oxide thickness is large. In fact, subthreshold slope depends on the interface trap density and on the C_{Si}/C_{OX} ratio.

All those considerations show that, at least in principle, if a memory requires low voltages for the read/write operations, it may feature improved radiation tolerance from the permanent damage viewpoint. In fact, when lower voltages are required, thinner oxides are required, in which less charge can be trapped. Charge is also quickly neutralized by tunneling of electrons in very thin oxides [139]. Thinner oxides also reduce the effects of the interface traps. Furthermore, if extremely low voltages are required (like in FRAM), there is no need of charge pumps, which are one of the most radiation-sensitive parts [133].

3.4 Conclusions

Ionizing radiation are energetic particles and high energy photons, which can ionize matter. Ionization can occur by the direct interaction with the electrons, or by secondary effects, such as the ionization induced by the recoil of a charged particle, originated by an elastic interaction with neutrons.

Ionizing radiation is present not only in military and space environments (in particular in the Van Allen belts), but also at the sea level. Packaging materials almost

[18] Assuming an uniform degradation in all the cells.

always have a non zero alpha emission rate, affecting the reliability also on commercial/consumer applications.

There are two main groups of effects: single event effects, which are unpredictable events caused by a single (often heavy) particle strike, and total ionizing dose effects, which include all the permanent and temporary effects induced by the cumulative adsorbed radiation dose.

The floating gate cell array is strongly affected by both heavy ion and total ionizing dose effects. The main TID effects are: prompt charge loss at low doses, and permanent threshold voltage variation (due to charge trapping and subthreshold degradation), increased leakage, and compromised retention (due to oxide traps) ad high doses. The main heavy ion irradiation effects are prompt charge loss and the compromised retention.

The peripheral circuitry is even more sensitive to all kind of radiation effects: heavy ions may trigger unpredictable events, leading to both data corruption, SEFI or device failure. TID effects compromise the program and erase functionality. Device featuring lower write voltages may show an increased robustness against TID, due to the smaller oxide thickness.

CHAPTER 4

Electrical characteristics Nanocrystal memory cells

Silicon nanocrystal memories represent one of the most suitable candidates in replacing the conventional floating gate based Flash. The nanocrystal memory cell features several improvements over its floating gate counterpart: its strong tolerance against SILC allows for a much better tunnel oxide scalability; the reduced tunnel oxide thickness, in turn, allows to employ lower programming voltages, and to scale down the cell width and length; lower voltages means also lower power consumption and smaller area requirements for the charge pumps; the absence of the monolithic floating gate drastically reduces the drain-induced-turn-on and the cell-to-cell coupling; the insulated nature of the storage nodes allows simple 2-bits per cell implementation; the elimination of the floating gate allows for a much more planar structure, making them very suitable as embedded memories.

Nanocrystal memories, unlike other approach, are fully CMOS compatible and they do not require uncommon materials. Some works [25] reported very high scalability, especially if the FinFET structure is adopted.

From the radiation tolerance viewpoint, nanocrystal memories are very promising, as it will be discussed in details in the following two chapters.

This chapter is focused on some particular electrical characteristics and behavior of the analyzed samples. In fact the analyzed nanocrystal memory cells show a number of peculiar characteristics, which are either intrinsic to the presence of the layer of discrete stored charge, or derives from the presence of other elements, which are not necessarily needed for the nanocrystal memory, such as the ONO stack. Hence, to distinguish these effects from other radiation-induced degradation mechanisms, some investigations have been performed.

In particular, nanocrystal memory shows a programming window that depends on the drain readout current. As it will be explained later, this phenomenon derives by the presence of the layer of discrete stored charge. FGM do not exhibit this phenomenon, because the charge is uniformly distributed, inducing an almost uniform potential on the substrate.

On the contrary, the presence of the ONO stack in nanocrystal memory cells induces some variations on the threshold voltage as the time elapses. These variations depend on

the bias and temperature. In principle, ONO stack is not required in nanocrystal memory cell, hence this phenomenon can be avoided using ad-hoc processes.

4.1 Devices analyzed

Throughout this chapter, we will analyze nanocrystal and floating gate memory cells and arrays. Both NCM and FGM were provided by STMicroelectronics M6 (Catania, Italy), and they are realized with the same 150nm technology. Table 2 lists the cell widths and lengths of the cells analyzed. Fig. 4.1 shows the typical cross section for NCM and FGM cells.

W \ L	240 nm	260 nm	280 nm	300 nm	320 nm	340 nm
160 nm		X		X		X
200 nm	X	X	X	X	X	X
240 nm		X		X		X

Table 2. Widths (W) and lengths (L) of the cells measured throughout this chapter. The "x" indicates that cells with that W and L were measured.

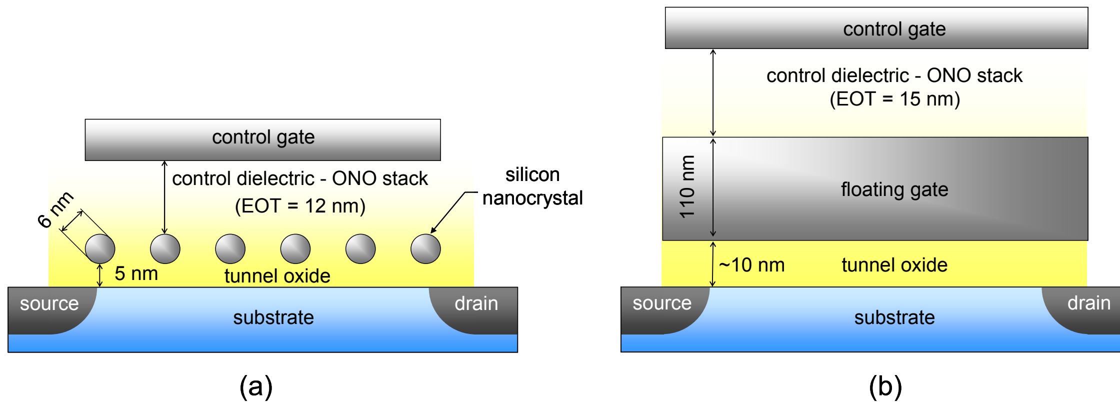

Fig. 4.1. Schematic cross-section of a nanocrystal memory cell (a) and a floating gate memory cell (b) analyzed in this thesis.

In NCM, the tunnel oxide is 5 nm thick and the control gate oxide consists of an ONO stack with an equivalent oxide thickness (EOT) of 12 nm. In detail, the physical thickness of the bottom oxide in the ONO stack is 4.5 nm; the nitride layer is 6 nm; and the top oxide is 5 nm. Each of these three layers was produced by chemical vapor deposition (CVD). The silicon nanocrystal layer was deposited by low pressure CVD (LPCVD) in the Si nucleation regime using SiH_4 as a precursor [140], using standard semiconductor equipment. A post deposition annealing was carried out in order to crystallize the Si islands. A nanocrystal density of $5{\cdot}10^{11}cm^{-2}$ was determined by TEM measurements, with an average nanocrystal diameter of 6 nm. Each cell contains about 300 nanocrystals. The average spacing between neighboring nanocrystal is 12.5-15nm, and the nanocrystal coverage area (that is, the channel area effectively covered by the nanocrystal) is about 15%. Noticeably, a threshold voltage shift of ±1V (with respect

the neutral cell), reflects a net charge density of $\pm 2.9\cdot 10^{-7}$ C/cm^2 = $1.8\cdot 10^{12}$ charges/cm^2 in the nanocrystal layer, i.e. to 10^3 electrons (holes) per cell or about 3.5 electrons (holes) per nanocrystal.

FGM cells have a tunnel oxide thickness ~10 nm and a control oxide of 15 nm, and the floating gate thickness is 110 nm.

FGM and NCM cells were also evaluated in particular array structures such as Cell Array Stress Test (CAST) [141], which are 256k cells connected in parallel, that is, with common drain, source, gate and body terminal, see Fig. 4.2. Through the CAST structure, we can measure the average cell behavior, and we are also able to detect the presence of a few defective tail cells. In particular, with this structure we can recognize the presence of few cells with a threshold voltage lower than the average CAST threshold voltage, because in this case we would see a bump in the I_D-V_{GS} CAST characteristic, due to the anticipated turn-on of these anomalous cells. However, we are not able to detect the presence of few cells with a threshold voltage higher than the average CAST threshold voltage; in fact, when most of the cells in the array are conducting, the drain current of the CAST saturates and we cannot see the variation due to few cells featuring high threshold voltages.

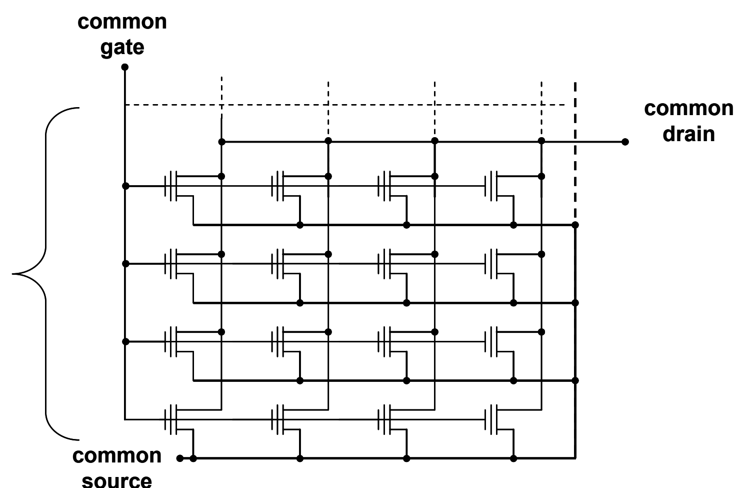

Fig. 4.2. Schematic representation of a CAST. Each transistor is either a floating gate or a nanocrystal memory cell.

Single cells can be programmed either by FN tunnel or CHC injection. Erasure is performed through FN tunnel. CAST structures can be programmed or erased only by FN tunnel. In fact, the relatively high parasitic series resistance (as high as several Ohm), which derives from the track resistance and pad-to-microtip contact resistance, saturates the maximum drain current to 2-4 mA. Furthermore, the drain current, during CHC is several hundreds of µA per cell: a CAST would need a CHC drain current as high as several tens of Amperes! Program and erased operations were timed, that is, a gate pulse with a fixed width was applied. In other words, there is not a smart program algorithm. With this program/erase method, programmed cells/CASTs store a net

negative charge, and erased cell store a net positive charge, as it will be explained in chapter 5.

4.2 The nanocrystal memory programming window and its dependence on the readout drain current

As seen in chapter 1, the programming window can be defined as the shift between the programmed and the erased I_D-V_{GS}. This is true when the programmed and the erased I_D-V_{GS} are parallel to each other, i.e., when the different stored charge polarity only induces a rigid shift. Nanocrystal memories behaves a little differently, hence a more precise operative definitions must be given. We define the threshold voltage of a cell (V_{TH}) as the gate voltage required by the cell to drive a certain, arbitrarily chosen, drain readout current (I_{DTH}), at a given drain to source voltage V_{DS}. It is obvious that the higher the I_{DTH} is chosen, the higher the V_{TH} will be. We define the programming window V_{win} as the difference between the programmed and the erased threshold voltages (evaluated, of course, at the same I_{DTH}). It is clear that, if the I_{DS}-V_{GS} are parallel to each other, the V_{win} will be constant function of I_{DTH}.

To analyze the programming window dependence on the drain readout current, we performed several experiments using about 350 single cells, featuring all the aspect ratio shown in Table 2. Program and erase operations were performed by FN tunnel.

First, we show the programming window dependence on the drain readout current and we give some definitions, which will be used in the following part of this section. Then, we present the experimental results, focusing on the dependence of the programming window evolution on several operating conditions: the amount of the nanocrystal charge, the operating temperature, the interface trap density, and the nanocrystal charge polarity.

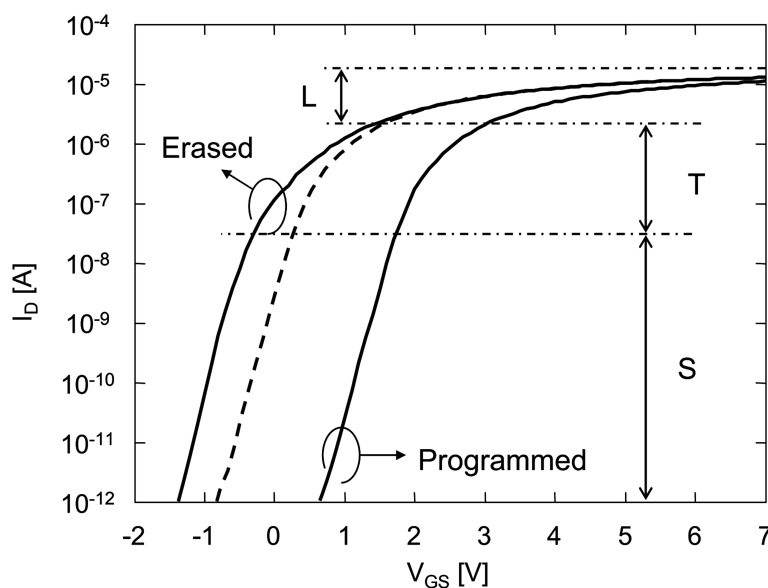

Fig. 4.3. Drain current – gate voltage characteristics of a programmed and erased NCM. V_{DS} was set to 50 mV. The dashed line is the programmed curve shifted by -1.47V. L, T, and S represent the linear, the transition and the subthreshold region, respectively

In Fig. 4.3, we show the drain current-gate voltage characteristics of a programmed and an erased cell using a +15V and -15V gate voltage pulse, respectively. We define the programming window difference (ΔV_{win}) as the difference of the V_{win} evaluated at a maximum current I_{max} in the linear region and at the minimum current I_{min} in the subthreshold region. We arbitrarily chose I_{max} and I_{min} to comply with our measurement setup. We set I_{min}=100pA, which is the minimum current value permitting a good extrapolation of the threshold voltage in subthreshold region, still being larger than the experimental resolution. We choose I_{max}=10μA because it is large enough to keep the MOSFET in deep linear region, and it is close to the largest value that can be driven by all device we analyzed, with the highest V_{GS} value (8V) and with V_{DS}=50mV.

The dashed line in Fig. 4.3 is the programmed curve shifted by -1.47 V so that it overlaps to the erased curve in the linear region. However, the programmed and the erased I_D-V_{GS} do not overlap in the subthreshold region, indicating that the programmed and the erased curves are not parallel. The erased curve in the subthreshold region lies on the left of the programmed curve, highlighting that V_{win} is larger in the subthreshold region. This phenomenon is better appreciated Fig. 4.4a, which shows the V_{win} evolution as a function of the drain readout current for the same cell. The V_{win} monotonically decreases with increasing drain current. Fig. 4.4b shows the same plot of Fig. 4.4a, with a linear I_D scale, and it highlights that the V_{win} is almost constant at high drain readout currents.

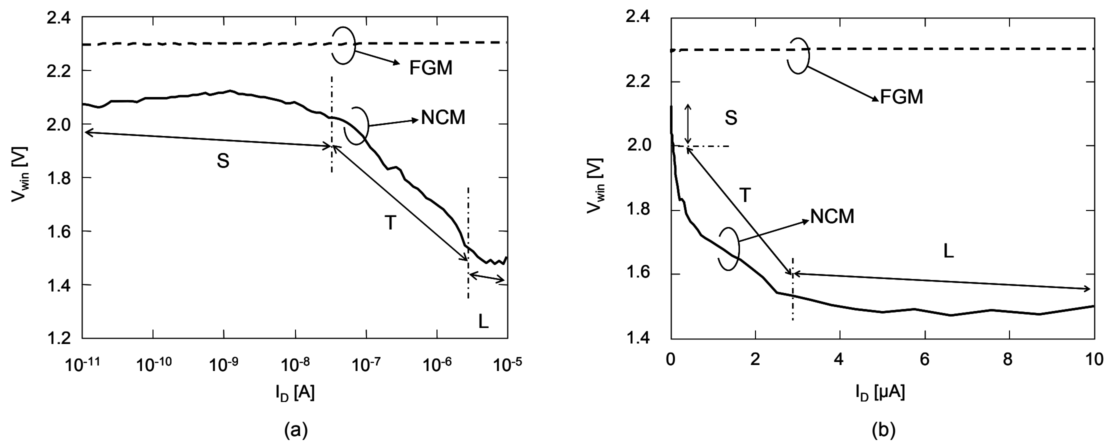

Fig. 4.4. Programming window as a function of the drain readout current: logarithmic I_D scale (a) and linear I_D scale (b). The programming window is almost constant in the L region.

In Fig. 4.3 and Fig. 4.4, we can identify three regions: the subthreshold (S) region, where V_{win} is almost constant; the linear (L) region, where V_{win} reaches its minimum value; the transition (T) between S and R regions, where V_{win} strongly depends on the I_D. Since the NC arrangement is not uniform (NCs are grown without any regular pattern) and since the number of nanocrystal may slightly change between different samples, ΔV_{win} may change between different cells (by a value as high as 300 mV), but the shape of its evolution is the same for all the devices.

Not surprisingly, I_D-V_{GS} of Fig. 4.3 and the V_{win} plot of Fig. 4.4 are very noisy. This is due to the presence of process-induced oxide border traps, which can be charged or discharged, inducing a random telegraph noise. This translates into a noisy I_D-V_{GS} curve, as previously observed in [142] on SONOS cells. This phenomenon is typically observed in stressed devices and it may be sometimes observed in fresh devices due to the process-induced traps. This random telegraph noise strongly affects the drain current especially in the subthreshold region, i.e. when the DC current is so small that it is sensitive to the trapping/detrapping of a single defect.

These results have been observed in all the NCMs cells, regardless the channel aspect ratio (which only affects, with a multiplicative factor, the drain current value). On the contrary, the FGM programming window remains always constant (see Fig. 4.4) regardless the readout current.

In the following subsections, we will show the ΔV_{win} dependence on the amount of stored charge, the temperature, the nanocrystal charge polarity, and the interface trap density. For clarity, the results are discussed in a separate subparagraph.

4.2.1 Amount of nanocrystal charge

To establish if there is any dependence of ΔV_{win} on the amount of stored charge, we programmed (and erased) the cells with different gate voltages, in order to achieve different programming windows. For simplicity, we used program and erase voltages with the same absolute value, i.e., $V_{G,erase} = -V_{G,program}$. The left axis of Fig. 4.5a shows that ΔV_{win} increases with increasing the absolute value of the program and erase voltages. In the right axis of Fig. 4.5a we show also V_{win} measured in the S region, with I_D = 100 pA.

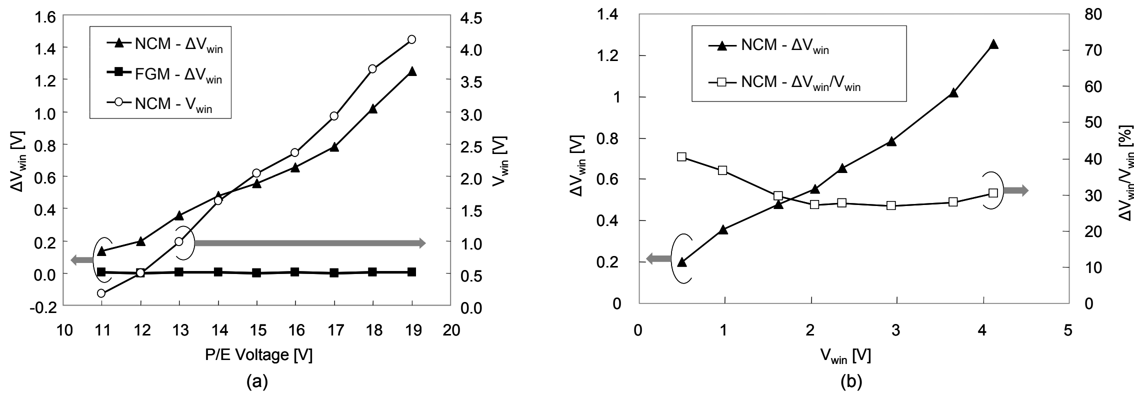

Fig. 4.5. (a) ΔV_{win} and V_{win}(@I_D=100pA) as a function of the program/erase voltage ($V_{G,program}$ =-$V_{G,erase}$). (b) ΔV_{win} and $\Delta V_{win}/V_{win}$ as a function of V_{win}.

ΔV_{win} increases with the stored charge from which the programming window linearly depends. The proportionality between ΔV_{win} and V_{win} (and thus, the proportionality to the stored charge) is better appreciated in Fig. 4.5b where we plot ΔV_{win} as a function of V_{win}. In the right axis of the same figure, we also plotted ΔV_{win} as a percentage of V_{win} (i.e., the ratio $\Delta V_{win}/V_{win}$). ΔV_{win} is approximately one third of V_{win}.

In Fig. 4.4 and Fig. 4.5, we plotted also the ΔV_{win} for FGM cells manufactured with the same technology (see dashed lines). In FGMs $\Delta V_{win}=0$ regardless the operating conditions, confirming that the I_D dependence of the programming window is related to the presence of the discrete NC layer.

4.2.2 Temperature

Studying the effect of the temperature on ΔV_{win} is an important investigation tool to have a more comprehensive picture of this phenomenon. In fact, from reliability viewpoint it is important to assess the impact of high temperature close to the operating conditions. On the other hand, the ΔV_{win} temperature dependence gives us important insights on the physical nature of this phenomenon.

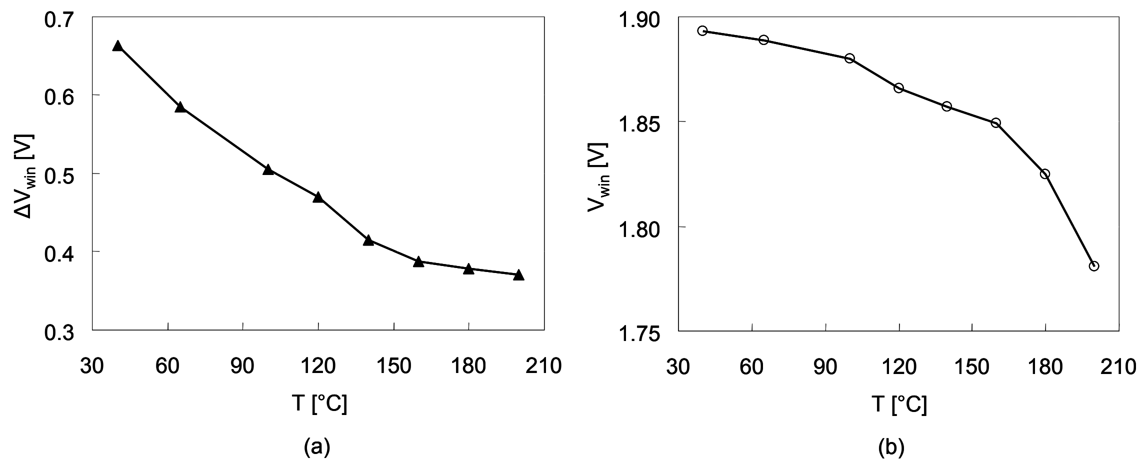

Fig. 4.6. ΔV_{win} (a) and V_{win}(@I_D=100pA) (b) as a function of the operating temperature ($V_{G,program}$ =-$V_{G,erase}$=15V).

At this purpose, we adopted the following experimental procedure. Initially, we programmed the cells at 40°C, injecting negative charge into the NC. Then, we measured the I_D-V_{GS} curves at different temperatures, from 40°C to 200°C. We let the cells to cool down to 40°C, and we repeated the I_D-V_{GS} measurements (at 40°C) to verify that no charge has been lost during the high temperature experiment. Later, we erased the same cells and we repeated the same experimental procedure. The results are summarized in Fig. 4.6: ΔV_{win} is strongly correlated with the operating temperature. For instance, ΔV_{win} decreases by 295 mV (44% of the initial value), when the temperature increases from 40°C to 200°C. In Fig. 4.6b, we plotted also V_{win} in the S region, in order to assess if the ΔV_{win} variation as a function of the temperature is due to a possible V_{win} reduction. V_{win} actually reduces, but its variation is as small as 110mV (6% of the initial value). Hence, the ΔV_{win} reduction only marginally correlates with the small V_{win} variation. In fact, by Fig. 4.5b we calculate that this small V_{win} variation could be responsible for a ΔV_{win} variation of only 29mV, which is less than 4.4% of the initial value, much smaller than the observed 44% reduction.

4.2.3 Interface traps

In order to assess if any correlation exists between the ΔV_{win} evolution and the interface trap density, we performed ionizing radiation experiments in NCM and FGM cells, evaluating and comparing the programming windows on NCMs and FGMs. Many works in literature reported that ionizing radiation generates oxide traps, positive charge trapping and interface traps in a way similar to the electrical stress, but without producing the oxide breakdown (see for instance [135],[143],[144] and references cited therein). In Fig. 4.7, we show the comparison between the I_D-V_{GS} curves of a fresh programmed cell and the same device reprogrammed after X-Rays irradiation. The major degradation phenomena observed in MOS devices are the positive charge trapping in the dielectrics and the generation of interface traps at the oxide/substrate interface [36]. The large variation of the subthreshold swing is a clear signature of the amount of the interface trap generation at the tunnel-oxide/substrate interface. In this case, the positive charge trapping has a smaller impact instead, due to the thin tunnel oxide.

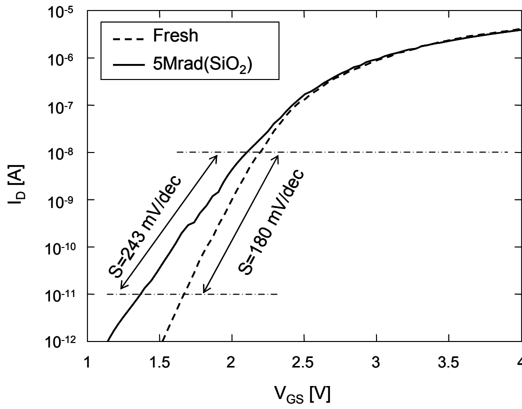

Fig. 4.7. I_D-V_{GS} plots of a fresh programmed cell and the same cell reprogrammed after 5-Mrad(SiO_2) X-Ray irradiation. . The two curves highlight the increased subthreshold swing in the irradiated device.

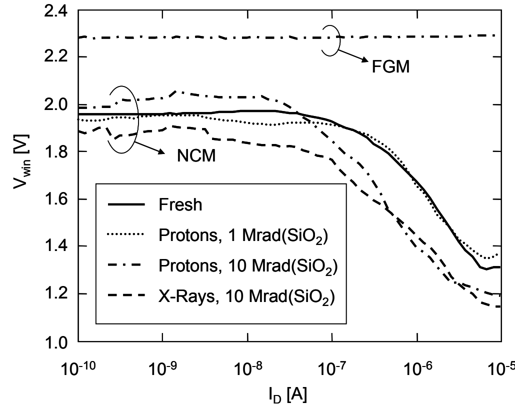

Fig. 4.8. V_{win} for fresh and irradiated (protons and X-Rays) cells.

In Fig. 4.8, we show the V_{win} of NCM cells irradiated with different doses up to 10Mrad(SiO_2). There are no clear radiation effects on the NCM V_{win} evolution. The difference among the various curves is within the cell-to-cell characteristic dispersion. For comparison, in Fig. 4.8, we show also the programming window of an irradiated FGM device, which does not depend on the drain readout current.

4.2.4 Nanocrystal charge polarity

So far, we considered the nanocrystals either negatively charged (programmed cell) or positively charged (erased cell). Now we aim to investigate the behavior of a cell with neutrally charged nanocrystals and compare it with the programmed/erased cell. In the following, we will refer as “neutral” (N) to a cell with neutrally charged nanocrystals.

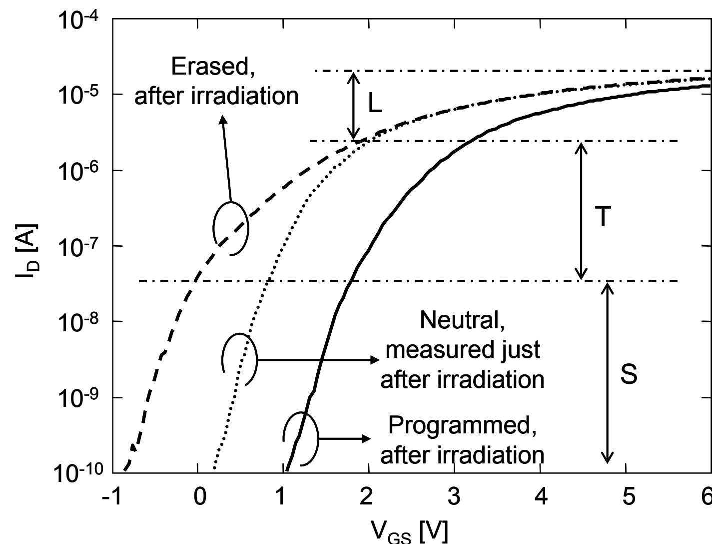

Fig. 4.9. Drain current – gate voltage characteristics of an irradiated NCM cell at 10Mrad(SiO_2) with 5-MeV protons.

In our experiments, the program/erase operations are time based. Therefore, an almost neutral cell is impossible to achieve by means of only electrical programming. On the other hand, UV-exposure is ineffective in our samples. In fact, the gate silicide masks the UV radiation and only the lateral nanocrystals can be discharged (because the nanocrystals are electrically insulated from each other). To overcome this problem, we used X-Ray and proton irradiations to neutralize the stored charge. In fact, as we will show in the sections dedicated to the total ionizing dose effects, the ionizing radiation can completely neutralize the NC charge, without inducing an appreciable permanent modification of the cell V_{win}, as it can be inferred from Fig. 4.8. In this way, we can evaluate the V_{win} between a neutral and a programmed cell or between a neutral and an erased cell.

In Fig. 4.9, we plot the I_D-V_{GS} curves of an irradiated cell, measured immediately after irradiation and after the program and erase operations. The neutral I_D-V_{GS} lies approximately in the middle of the P and E curves.

In Fig. 4.10, we plot the programming window as a function of the drain readout current measured between:

1) the programmed and the neutral cell (P-N-V_{win}, dotted);

2) the programmed and the erased cell (P-E-V_{win}, solid);

3) the neutral and the erased cell (N-E-V_{win}, dashed).

The P-E-V_{win} evolution is very similar to the one of the non-irradiated cell; the N-E-V_{win} features the same decreasing evolution. On the contrary, the P-N-V_{win} is slightly increasing.

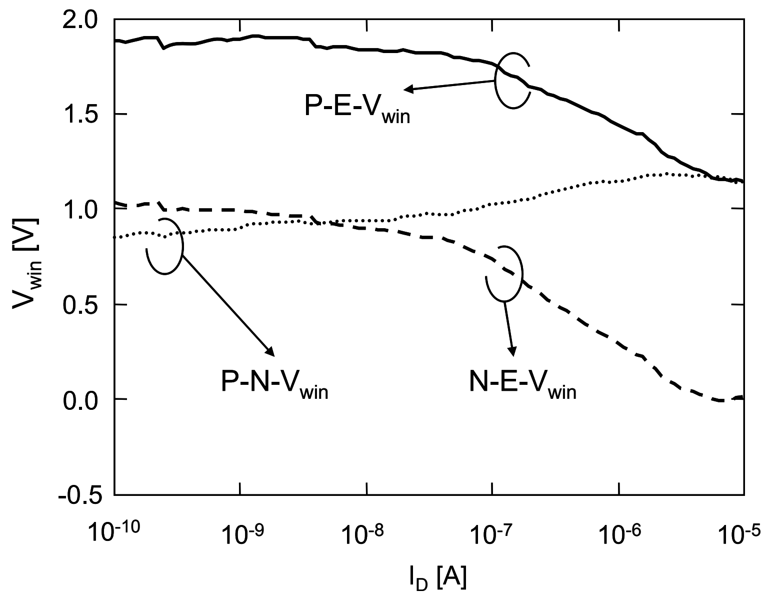

Fig. 4.10. P-E-V_{win}, P-N-V_{win}, and N-E-V_{win} as a function of I_D after 10-Mrad(SiO_2) X-Ray irradiation.

4.2.5 Discussions

All our findings can be explained considering the Debye length (L_D), i.e., the free carrier screening distance. L_D locally depends on the carrier density and it can differently affect the channel formation in the programmed and the erased cell, due to the different nanocrystal stored charge polarity. At low V_{GS} the device operates in the S region and the carrier density is below the doping level. For instance, for carrier concentration between 10^{14} and 10^{16} cm^{-3}, the L_D ranges from 400 to 40 nm. These values are larger than the average nanocrystal mutual distance (12.5 to 15 nm in our devices). Consequently, when the device is operating in the S region the free carriers uniformly spread over the whole channel area. Moreover, if V_{GS} increases in the S region, the free carrier density uniformly increases. In other words, the gate has a uniform control on the charge density all over the channel, similarly to a conventional floating gate device

However, when L_D becomes comparable or smaller than the average nanocrystal spacing, the device enters the T region (e.g., at T=300K, L_D=13nm when the carrier density reaches $10^{17}cm^{-3}$), and the cell turn on begins. Consequently, the carrier density is no longer uniform and it is higher in those zones featuring a lower local V_{TH}. In particular, as depicted in Fig. 4.11a-b, in an erased cell the channel free charge starts accumulating mostly under the positively charged nanocrystals (which cover about 15% of the channel area), whereas, in a programmed cell the free charge density is higher in those regions far from the negatively charged nanocrystals (i.e., the remaining 85% of the channel area), as shown in Fig. 4.11c-d. With increasing V_{GS} within the T region, the local free charge concentration increases, but L_D decreases, reducing the size of the spots where the carrier inversion starts. In other words, the gate does not uniformly control the channel carrier density anymore and this phenomenon can be figured as a

sort of modulation (a reduction) of the effective W/L as V_{GS} increases, leading to a smaller I_D than expected. In the erased cell, as V_{GS} increases, the L_D reduction has a strong effect, because the channel starts forming only in 15% of the device area. This translates into a considerable delayed turn-on in the erased cell (i.e., the erased cell enters the linear region at a V_{GS} higher than expected), and a higher V_{TH} in linear region.

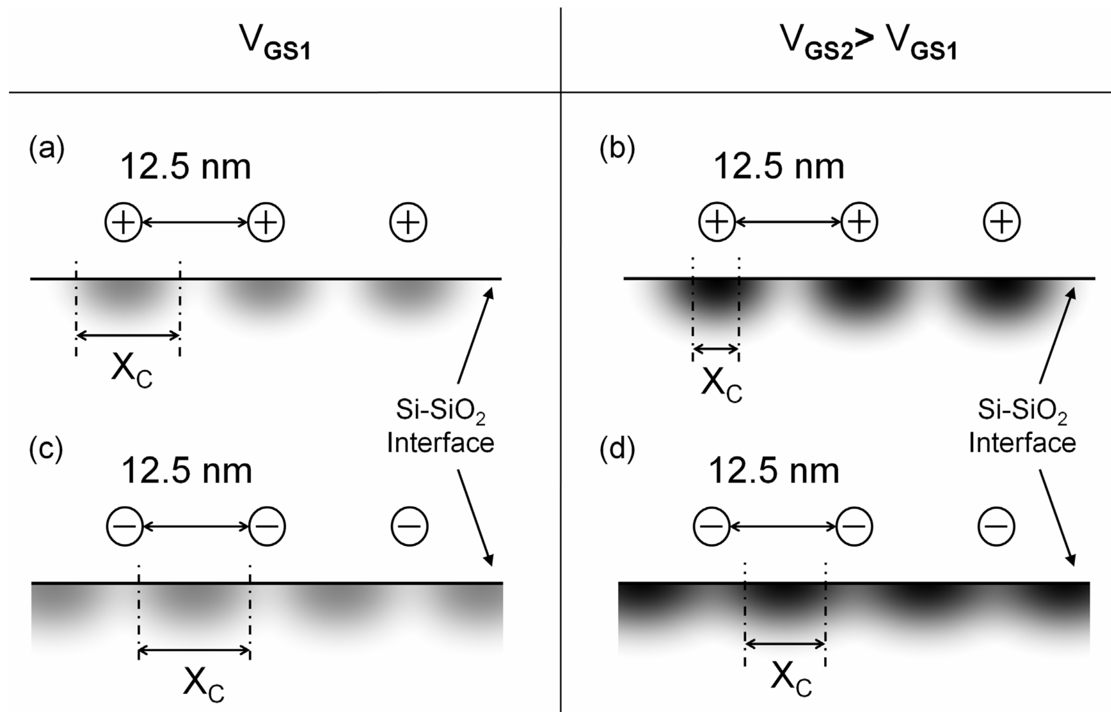

Fig. 4.11. Sketch of the free carrier distributions for a NCM in four operating conditions. The dark regions represent the free carriers. a) Erased cell at low V_{GS}. b) Erased cell at a higher V_{GS}. c) Programmed cell at low V_{GS}. d) Programmed cell at a higher V_{GS}. X_C is the free carrier distribution spread, i.e. the area in which most of the free carriers are concentrated.

However, the L_D reduction has a smaller impact in a programmed cell with respect to an erased cell, because the channel starts forming in 85% of the device area (while in an erased cell the channel starts forming only on the 15% of the device area). As a result, the programmed cell features a turn-on that is less delayed with respect to the erased cell. The delayed turn on of the erased cell, with respect to the programmed one, results in a V_{win}, which is smaller in the L-region than in the S region.

When the nanocrystals are neutrally charged, the local channel conductance spatial modulation is negligible, because the neutral NCs induce a very weak perturbation on the channel potential and the channel starts forming in the whole device area. As a result, the neutral cell turns on faster than both erased and programmed cell. As discussed above, in the programmed cell the carrier inversion starts over the 85% of the channel area, which is very similar to the neutral cells, where the carrier inversion starts over the whole channel. In fact, the programmed and neutral curves of Fig. 4.9 have a very similar shape and the P-N-V_{win} increases only by 0.25V from I_D = 100pA to I_D = 10µA (see Fig. 4.10). Conversely, the difference between the erased and neutral cell is

much more pronounced: the N-E-V_{win} decreases by 1V from 100pA to 10μA (see Fig. 4.10). This is expected, because the carrier inversion starts only on the 15% of the channel in the erased cell.

In FGMs the potential induced by the floating gate on the channel is uniform, regardless the stored charge polarity, resulting in a constant V_{win}. This confirms the idea that, the programming window dependence on the readout drain current is related to the presence of a layer of discrete nanodots.

Accordingly with this interpretation, the irradiation experiments of Fig. 4.8 show that this phenomenon has little or no correlation with the number of interface traps and oxide traps. In fact, even though irradiated NCMs cell feature a large increase of the subthreshold swing due to the generation of a large amount of interface traps, the behavior of the programming window is the same than in fresh devices. In Fig. 4.8, there is no correlation between the V_{win} evolution and the ionizing radiation dose (i.e., the interface trap density). Incidentally, FGMs and NCMs are manufactured with the same fabrication process, and the interface quality is expected to be the same in the two devices. This is a further confirmation that the peculiar V_{win} evolution on the NCMs does not depend on the interface trap density, but it is caused by the presence of the layer of discrete nanodots.

Remarkably, the mechanism described above for NCMs is quite similar to the phenomenon of charge lateral non-uniformities (LNU), which stretch out the I_D-V_{GS} curves, regardless the interface traps density [145]-[147].

It is well known that irradiation can generate fixed trapped-hole charge with lateral non-uniformity in its spatial distribution. If LNUs affected differently the programmed and erased curves, we would have observed a programming window variation even on irradiated FGMs, because we expect that LNUs impact in the same way on FGMs and NCMs (our FGM and NCM samples are fabricated with the same technology). However, Fig. 4.8 shows that the irradiated FGMs feature a constant programming window, which is the signature that the programmed and erased I_D-V_{GS} curves of the FGM cell remain parallel even after irradiation. Hence, LNUs cannot be held responsible of the programming window variation, which is observed only on NCMs. On the contrary, the different NC charge polarity of the programmed, erased and neutral cell is the dominant factor for the programming window dependence on the drain readout current.

Finally, as the operating temperature increases, the programming window dependence on the readout drain current is somewhat reduced as shown in Fig. 4.6. This is explained by the increased carrier screening length with the increasing temperature. In fact, the local free charge density is proportional to $exp(q\phi/kT)$, where ϕ is the local channel potential and T the temperature. Therefore, when T increases, the channel carrier density variation induced by the ϕ non-uniformity is mitigated and L_D increases.

For instance, with a carrier concentration of 10^{17} carriers/cm^3, L_D increases from 13.3nm to 16.3nm if the temperature is increased from 40°C to 200°C.

The programming window dependence on the operating region (subthreshold and linear) can be successfully exploited to optimize the cell functionality in a circuit perspective. For instance, if the threshold voltage sensing circuitry employs high drain readout current values, the most convenient approach is to employ negatively programmed cells for one binary state, and almost neutral cells to store the complementary state. In fact, in this case the programming window is higher in the linear region. This is the case of the NOR Flash, as briefly explained in Chapter 1, where drain readout currents of about tens of μA are employed.

Conversely, in sight of a very low power application or in NAND Flash, where the readout currents are around 200nA as mentioned in chapter 1, the programming/erase technique can be adjusted to achieve a positively charged erased cell, instead of a neutral cell, in order to exploit the larger programming window in the subthreshold region.

4.3 The effects of the ONO stack interface traps

In this section we show the effects of the Oxide-Nitride-Oxide interpoly dielectric stack interface traps. In principle, this stack is not required for the nanocrystal memory operation, but the particular process used for our samples required the deposition of the interpoly (control) dielectric by CVD. The presence of the ONO stack one major drawback: it tends to trap negative charges [148]. These charges are generally fixed, but they can also move within the ONO stack, depending on the applied bias. This results in an intrinsic (but limited) instability of the threshold voltage of the analyzed samples, which should not be confused with the retention characteristics. In our samples, the ONO stack consists of (from the control gate, toward the nanocrystals): 5nm layer of SiO_2, 6nm layer of Si_3N_4 and 4.5nm of SiO_2.

The retention-like experiments were performed on CASTs. The threshold voltages are extrapolated at I_D = 10 μA. The I_D-V_{GS} curves were taken with few points in order to reduce the effects of measurements on the experiments. The retentions experiments were performed both with zero bias, and with different gate voltages. Drain and source terminals were grounded during the retention experiment.

Fig. 4.12a shows the CAST threshold voltage variations measured in the first 1000 seconds following a program operation. The threshold voltage slightly decreases at zero gate bias; surprisingly, the threshold voltage decreases faster if a positive gate voltage is applied, while it increases if a moderate negative gate bias (-3V and -5V) is applied. Still, if a high enough negative gate voltage is applied (see curve at V_G=-8V in Fig. 4.12a), the threshold voltage features a decreasing behavior, due to electron tunneling from the nanocrystals to substrate. Fig. 4.12b shows the results of the same experiment performed on an erased CAST: the threshold voltage increases if a negative gate bias (-

3V, -5V, -8V) is applied; conversely, the threshold voltage decreases under moderate positive gate bias (3V and 5V) and increases if a gate bias as high as 8V is applied.

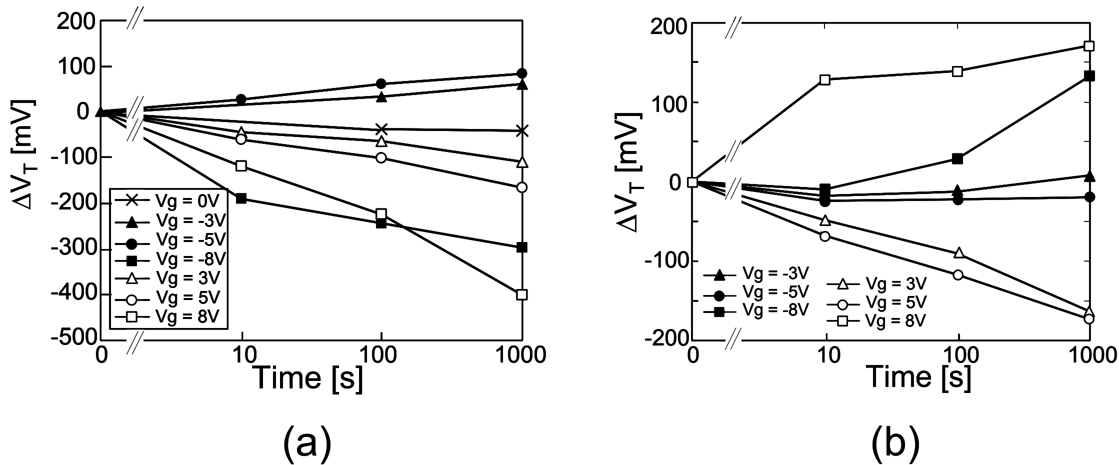

Fig. 4.12. ΔV_t evolution as a function of time for different constant gate bias applied immediately after programming at +15V (a) and erasing at -15V (b).

When a cell is in the programmed state, the nanocrystals store electrons. In principle, a negative gate bias would enhance the electron tunneling across the tunnel oxide from nanocrystal to substrate, with a consequent decrease of the threshold voltage. Conversely, under moderate positive bias the electric field across tunnel oxide is reversed, hence electrons could not escape from nanocrystals toward substrate. Thus, a larger threshold voltage decrease would have expected at negative gate bias than that measured at zero gate bias. In fact, accelerated retention test are often carried out applying a negative gate bias, as reported for instance in [149]. Symmetrically, when a positive gate bias is applied to an erased CAST (i.e. when nanocrystals stores holes), the threshold voltage should increase. These considerations are in contrast with the experimental results of Fig. 4.12. Hence the observed threshold voltage evolution under constant gate bias is not only due to discharging nanocrystals, but due also other phenomena may come into play.

Fig. 4.13 shows the threshold voltage variation (ΔV_T) of a programmed and an erased CAST, measured 100 seconds just after the program/erase operations, as a function of the gate voltage applied during the retention experiments. In the range between -5V and +5V, both the programmed and the erased CASTs show a similar behavior (their threshold voltages increase with negative gate bias and decrease with positive gate bias). For $|V_G| > 5V$, the programmed and erased CASTs behave differently. In fact, in a programmed CAST a high negative gate bias tends to erase the CAST itself, decreasing its threshold voltage value. Instead, under a high positive bias (still smaller than the programming voltage), the oxide field across the control dielectric is larger than that across the tunnel oxide. The enhanced tunnel probability across the ONO stack produces a partial discharge of the nanocrystal, resulting in a decrease of the threshold voltage. The opposite occurs for the erased CAST.

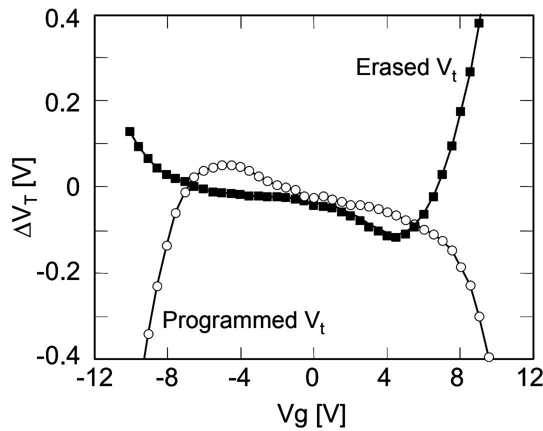

Fig. 4.13. Threshold voltage shift taken 100s after program (+15V) or erase (-15V) pulse as a function of the applied bias Vg.

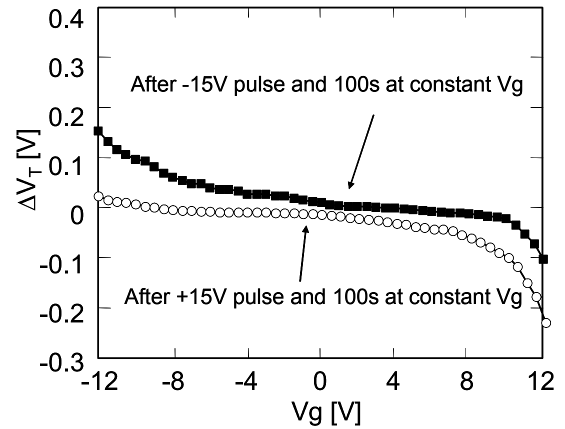

Fig. 4.14. Threshold voltage shift taken 100s after program (+15V) or erase (-15V) pulse as a function of the applied bias Vg on a CAST without the NCs.

In Fig. 4.14, the results of the same experiment of Fig. 4.13 performed on a CAST without the nanocrystal layer are shown. Noticeably, in Fig. 4.13 and Fig. 4.14, the threshold voltage shows similar evolution for $|V_G|<5V$, indicating that this threshold voltage variation cannot be related only to a charge variation in the nanocrystal layer. Incidentally, samples used in [149] did not employ ONO as control dielectric and did not show such anomalous threshold voltage behavior.

The results of Fig. 4.12-Fig. 4.14 can be explained with negative charge motion from one oxide/nitride (O/N) interface to the other one. In fact, negative charge can be trapped in these interfaces during program and erase operations [148]. With negative gate biases, the negative charge is subjected to the electric field across the ONO stack and it moves toward the bottom O/N interface, leading to an increased threshold voltage. On the contrary, with positive gate biases, the charge moves toward the top O/N interface, decreasing the threshold voltage, in agreement with the experimental results. A 100-mV threshold voltage variation could derive from $5 \cdot 10^{11}$-10^{12} electrons/cm^2 moving from one O/N interface to the other one.

Fig. 4.15 shows the results of longer retention experiments on programmed CASTs with nanocrystals. With V_G=-6.5V and -5.75V, the threshold voltage initially increases, but after a time (which depends on the V_G value), it exhibits a turn-over and it starts to decrease. This turn-over derives from the limited charge trapped amount at the O/N interfaces. When a gate bias is applied, the electric field across the ONO stack modulates the position of the trapped charge, in a time scale which depends on the applied bias. After a longer time, most of the trapped charge has been moved and the threshold voltage shift only depends on the contribution of electron tunneling from nanocrystals toward substrate, which results in the long-term reduction of the threshold voltage.

The retention experiments were also performed at high temperature (200°C). Fig. 4.16 shows the threshold voltage variation of a programmed CAST as a function of time for V_G=-5.75V and V_G=-6.5V, measured at room temperature and at 200°C. It is clear

that, for all the V_G values of Fig. 4.16, the threshold voltage initially increases and then it features a turn-over. Noticeably, when measurements are performed at 200°C, this turn-over happens at times shorter than those observed at room-temperature. This confirms the idea that the motion of the negative charge trapped within the ONO layer is responsible for the threshold voltage variation over the short time retention experiments. In fact, the negative charge motion within the nitride layer is reported to be dependent on the temperature, moving faster at high temperature, as described by the Poole-Frenkel model [148],[150].

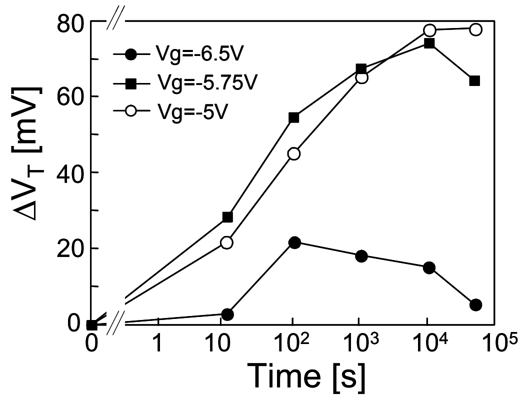

Fig. 4.15. Evolution of the threshold voltage variation as a function of time for different constant gate bias after programming at +15V

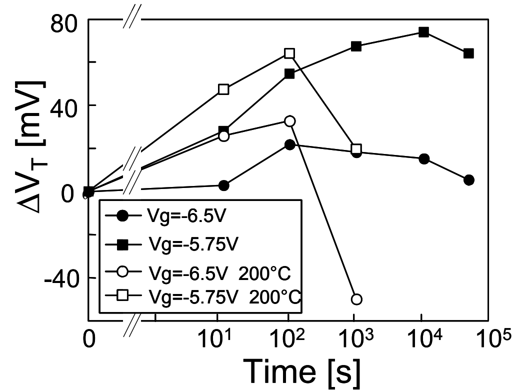

Fig. 4.16. Evolution of the threshold voltage variation as a function of time for different constant gate bias after programming at +15V. Measurements have been done at room temperature and at 200°C.

4.4 Conclusions

In this chapter we presented some electrical characterizations performed on nanocrystal memories. These results are either intrinsic to the discrete storage approach or related to the particular manufacturing process/cell structure. In particular, the programming window dependence on the drain readout current is related to the presence of the layer of positive/negative discrete charge, which differently affects the channel formation. This phenomenon can be controlled with the nanocrystal size and density. However, nanocrystal size and density control also some other properties (programming window width, lateral tunneling, retention, etc), hence a tradeoff is mandatory. The intrinsic threshold voltage drift, on the other hand, is due to negative charge trapping in the ONO dielectric stack. This particular dielectric is not intrinsic to the nanocrystal memory cells, hence, at least in principle, better dielectrics could be employed, avoiding this small threshold voltage drift.

CHAPTER 5

Total Ionizing Dose effects on nanocrystals memories

Nanocrystal memories not only bring advantages in terms of better scalability and reduced power consumption, but also, the intrinsic redundancy of the stored information may also helps in enhancing the radiation robustness.

Previous works [33] analyzed the effects of both heavy ions and total dose effects on nanocrystal memories. However, these studies were performed on nanocrystal memories manufactured by silicon ion implantation, which is definitely not one of the best methods.

In this chapter, a detailed analysis of total dose will be performed. Furthermore, the effects of total ionizing dose on NCM were never compared with the effects on Floating Gate memories, until our work [38]. A detailed comparison will be given in this chapter, using NCM and FGM manufactured with the same 150nm technology, as described in the previous chapter. Furthermore, a comparison of the effects of two different ionizing sources, 10-keV X-rays and 5-MeV protons, will be performed. The most important aspects that will be addressed are:

1) The charge loss
2) The permanent damage
3) The effects on the retention

5.1 Experimental setup

The devices used to assess the impact of TID are the same analyzed in the previous chapter, and they will not be discussed here again. For more details, refer to chapter 4.

All the program and erase operations were performed through Fowler-Nordheim injection, applying a 2-ms gate voltage pulse, with the other terminals grounded. We define the threshold voltage V_{TH} as the gate-to-source voltage required by the CAST and cell for driving a given drain current I_{DTH} = 25 µA and 100 pA, respectively, with V_{DS} = 50mV. In the following we refer to the programming window as the difference between the V_{TH} of a programmed (P) and an erased (E) device. Table 3shows the program/erase voltages and the corresponding programming windows.

All irradiations were performed at the INFN-LNL Laboratori Nazionali di Legnaro, Italy. We irradiated the devices at wafer level with 10-keV X-rays and a 5-MeV protons (LET = 0.063 MeV·mg^{-1}·cm^{2}). The terminals were floating during irradiation, which is a good approximation of the typical operating conditions. In fact, each memory cell is kept at a high impedance state for the majority of its lifetime and it is sporadically read or written. For each dose, we irradiated 20 NCM CASTs and 20 FGM CASTs, 100 NCM single cells and 100 FGM single cells: one half were programmed and one half were erased before irradiation.

Device	Program V_{GS} [V]	Erase V_{GS} [V]	Nominal Programming Window [V]
NCM	15	-15	2
FGM	15	-16	3
FGM	16.5	-17	5

Table 3. Program and erase voltages used for NCMs and FGMs

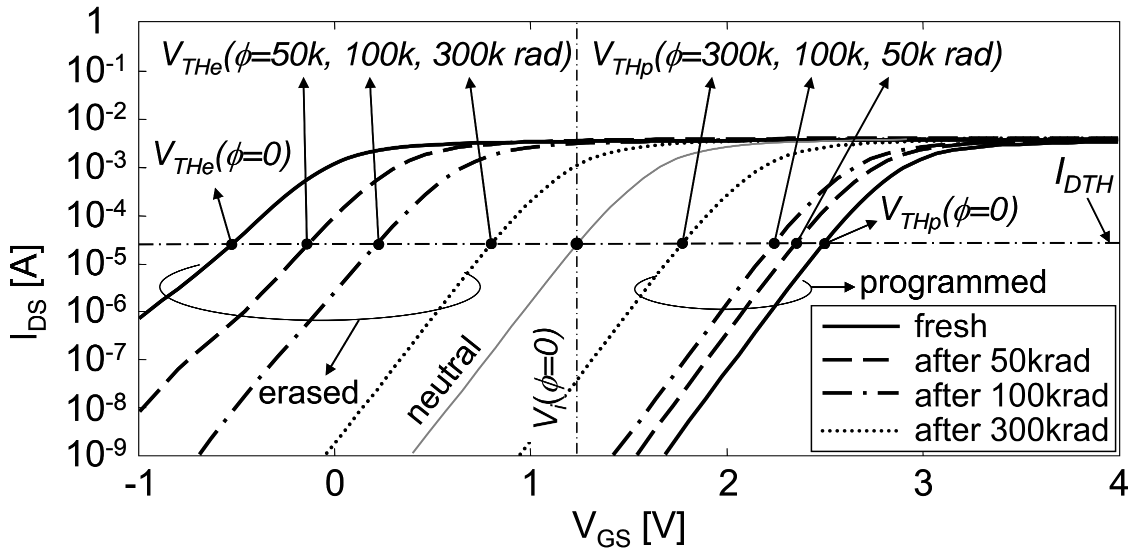

Fig. 5.1. I_{DS}-V_{GS} plots of one programmed and one erased FGM CAST measured immediately after program or erasure (fresh) and immediately after proton irradiation with different doses (ϕ = 50krad, 100krad, 300krad).

5.2 Low irradiation dose effects: charge loss

Fig. 5.1 shows the I_D-V_{GS} curves of two FGM CASTs irradiated with protons. One CAST was programmed and the other was erased before irradiation. We measured the I_D-V_{GS} at different doses ϕ. We define V_{THp} and V_{THe} the threshold voltage of a programmed and erased device, respectively. V_{THp} decreases and V_{The} increases, leading to a progressive programming window closure with increasing radiation dose. The manner in which the charge loss modifies the V_{THp} and V_{THe} is a signature that the programmed cell stores a net negative charge, while the erased cell stores a net positive charge. In fact, as it will be shown later, at such low irradiation doses the charge trapping is negligible and V_{THp} and V_{THe} approach the intrinsic value V_i, i.e., the

threshold voltage of a device with neutrally charged nanocrystals or floating gate. The value of V_i in a fresh FGM device (i.e. for ϕ=0) is shown in Fig. 5.1. The charge loss results of both NCMs and FGMs are summarized in Fig. 5.2-Fig. 5.4. Fig. 5.2 and Fig. 5.3 show the differences $V_{THp} - V_i(\phi = 0)$ and $V_{THe} - V_i(\phi = 0)$ as a function of the irradiation dose for NCMs and FGMs, respectively. For clarity, we plotted $V_{THp} - V_i(\phi = 0)$ and $V_{THe} - V_i(\phi = 0)$ instead of V_{THp} and V_{THe} because V_i has different values between NCMs and FGMs, due to the different tunnel and control dielectric thicknesses. The corresponding programming windows are plotted in Fig. 5.4, highlighting a much larger charge loss in FGMs than NCMs.

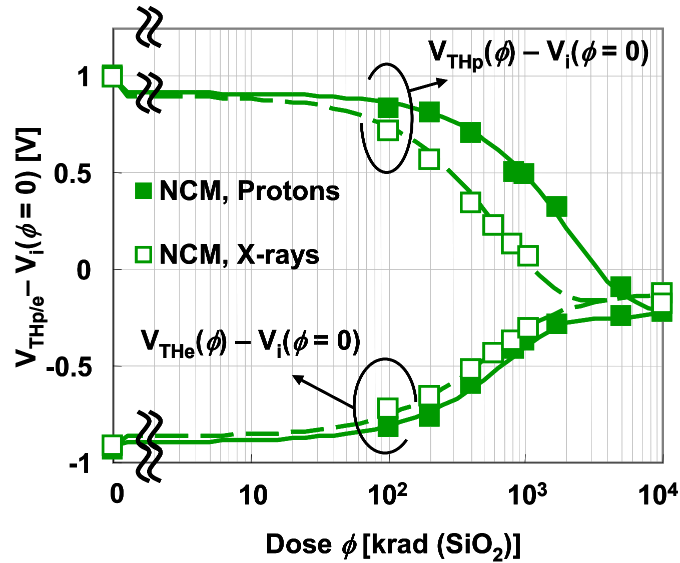

Fig. 5.2. Threshold voltages of NCMs irradiated with protons and X-rays at different doses. Solid lines are the theoretical model described in section 5.5. Each experimental point is calculated as the average between 10 samples.

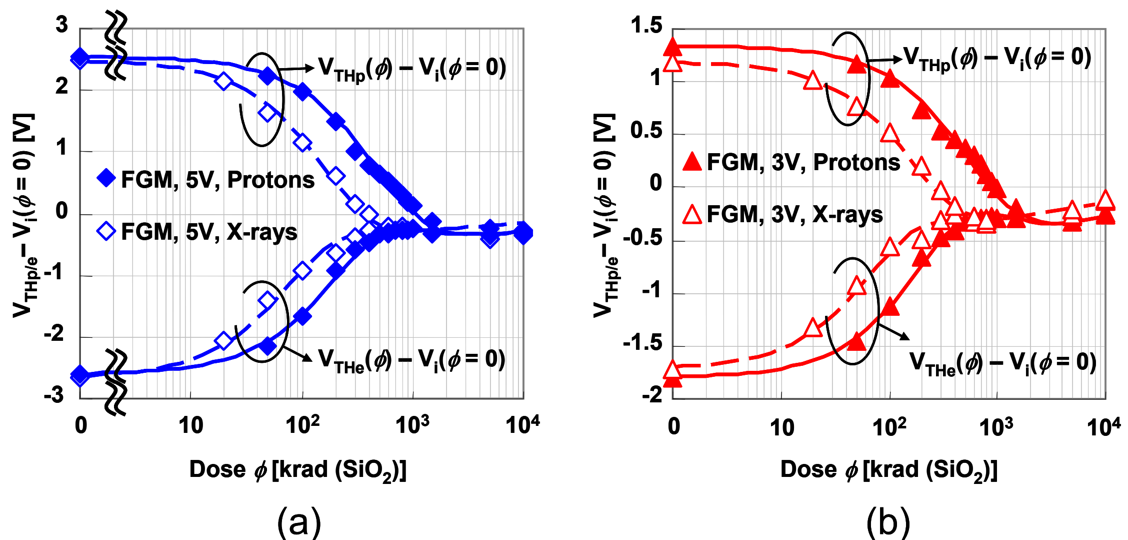

Fig. 5.3. Threshold voltages of FGMs irradiated with X-rays and protons at different doses. We used two different values of programming windows before irradiation: 3V (a) and 5V (b). Solid and dashed lines are the theoretical model described in section 5.5. Each experimental point is calculated as the average between 10 samples.

Remarkably, X-rays are much more effective than protons in charge removal. For instance, after 1-Mrad(SiO_2) X-ray irradiation on NCM, the charge is almost completely neutralized and the programming window is less than 0.5V. Instead, after 1-Mrad(SiO_2) proton irradiation on NCM, the programming window is still 0.9V, indicating that approximately only half of the stored charge has been lost.

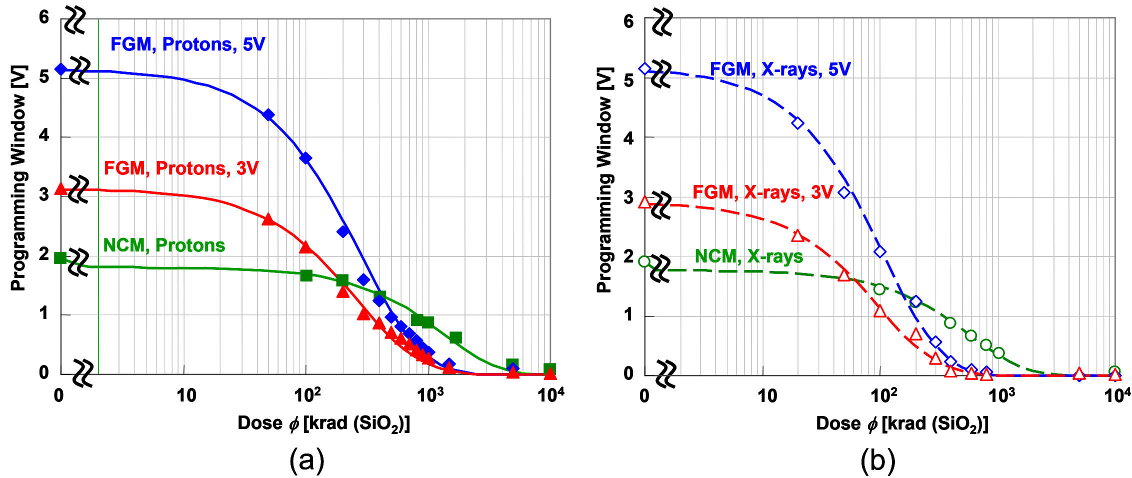

Fig. 5.4. Comparison between NCMs and FGMs after proton (a) and X-ray (b) irradiations. The lines are the theoretical model described in section 5.5. Each experimental point is calculated as the average between 10 samples.

Finally, the experiments on the single cells reported the same results achieved with the CASTs.

5.3 High irradiation dose effects: positive oxide trapped charge and interface traps

Apart the charge loss, X-ray and proton irradiations produce also some permanent effects on the electrical characteristics of nonvolatile memories. For instance, in Fig. 5.5, we plot the I_D-V_{GS} curves taken on a FGM CAST before irradiation, and on the same FGM CAST reprogrammed after a 10Mrad(SiO_2) X-ray irradiation. If the devices are reprogrammed, the programming window can be restored even after irradiation up to 10 Mrad(SiO_2). However, the programmed and erased I_D-V_{GS} curves appear shifted leftward and feature an increased subthreshold swing. This behavior has been observed in both FGMs and NCMs, independent of the radiation source (protons or X-rays). However, the modifications of electrical characteristics are less pronounced in NCMs than in FGMs.

For brevity, in the following we will refer to the permanent threshold voltage shift as ΔV_{TH}. The ΔV_{TH} (evaluated at the same constant current I_{DTH} as mentioned in the experimental setup section) of the programmed devices is shown in Fig. 5.6 as a function of the irradiation dose. The solid curves are the fits with the model which is presented in the modeling section. The four curves of Fig. 5.6 feature the same qualitative evolution, with a turnover: firstly ΔV_{TH} decreases, and then it begins to rise.

Noticeably, for a given radiation source, NCM's ΔV_{TH} evolutions have the same trend than FGM's, but they are delayed. Furthermore, proton-irradiated NCM and FGM evolutions are shifted rightward with respect to the X-ray irradiated devices.

In Fig. 5.7, we plotted the variation of the subthreshold swing (S) referred to its initial value (S_0) for the irradiated samples. The subthreshold swing increases with the dose after both X-ray and proton irradiations. Noticeably, proton irradiation produces a smaller increase of the subthreshold swing than X-ray irradiation. The solid lines of Fig. 5.7 are the theoretical fits with the model described in the section dedicated to the modeling.

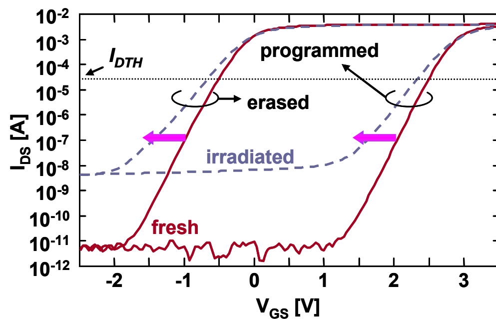

Fig. 5.5. Plot of the programmed and erased I_{DS}-V_{GS} curves of a fresh and an irradiated FGM device, after reprogramming. The device was irradiated at 10Mrad(SiO_2) with X-Rays.

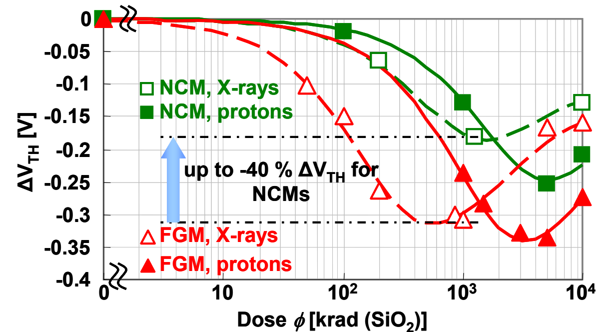

Fig. 5.6. Variation of the threshold voltages of NCMs and FGMs. Lines are the theoretical model described in section 5.5. Each experimental point is calculated as the average between 10 samples.

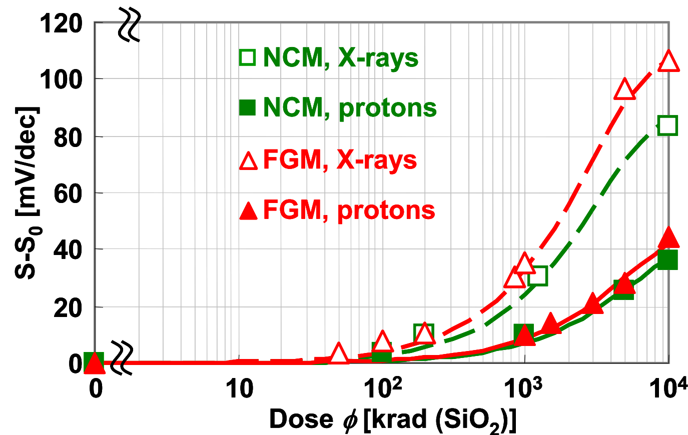

Fig. 5.7. Subthreshold swing variation of NCMs and FGMs after proton and X-ray irradiations. Lines are the theoretical model described in section 5.5. Each experimental point is calculated as the average between 10 samples.

5.4 Retention properties

Long-term data retention experiments on fresh and irradiated NCM and FGM samples were performed. The most important results of NCMs and FGMs are summarized in Fig. 5.8. The two horizontal lines identify the two failure levels, arbitrarily set to the 20% of the initial programming window as in [2]. The lines are empirical fits with a power law as in [36].

Nanocrystal memories show a very good radiation tolerance. In fact, after the 10-Mrad(SiO_2) proton irradiation, the retention curve overlaps to the fresh device. Nonetheless, large charge loss is observed after X-ray irradiations.

Despite the thinner oxides employed, NCMs features a much stronger radiation tolerance compared to FGMs. For instance, the retention properties o f NCMs after 10Mrad(SiO_2) proton irradiation is remarkably better than FGMs irradiated at only 1Mrad(SiO_2) with the same radiation source.

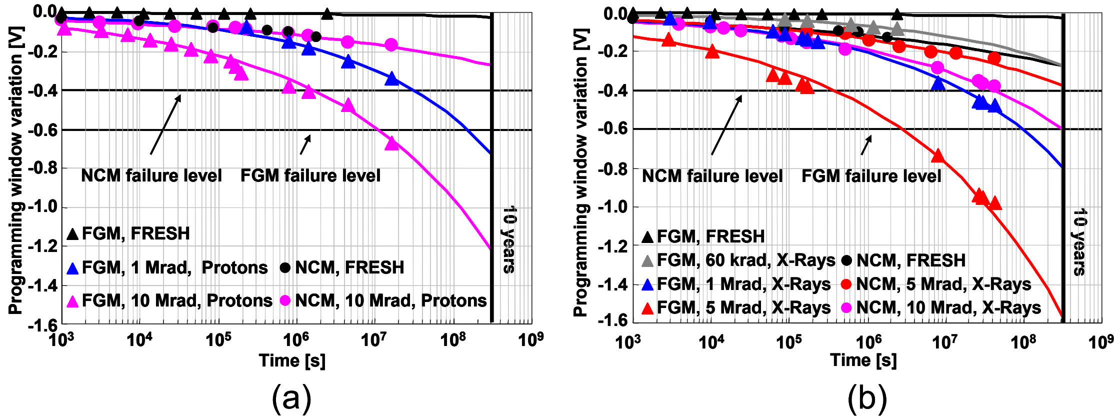

Fig. 5.8. Comparison between the retention characteristics of fresh and irradiated NCMs and FGMs with protons (a) and X-rays (b). The initial programming windows were 3V in FGMs and 2V in NCMs. Each experimental point is calculated as the average between 10 samples.

5.5 Modeling

The threshold voltage variation measured immediately after irradiation at a given radiation dose ϕ (Fig. 5.2 and Fig. 5.3), is due to two contributions: 1) the permanent threshold voltage variation, ΔV_{TH}, discussed in paragraph 5.5.1; 2) the charge loss $\Delta V_p(\phi)$, and $\Delta V_e(\phi)$ discussed in paragraph 5.5.2:

$$\begin{aligned} V_{THp}(\phi) &= V_{THp}(0) + \Delta V_{TH}(\phi) + \Delta V_p(\phi) \\ V_{THe}(\phi) &= V_{THe}(0) + \Delta V_{TH}(\phi) + \Delta V_e(\phi) \end{aligned} \quad (5.1)$$

Hereafter, the subscripts p and e refer to the programmed and erased cell, respectively.

We present our model in two steps: 1) we consider the permanent degradation effects (see Fig. 5.6), which impact on $V_{TH,p}$, $V_{TH,e}$, and V_i in the same manner; 2) we model the charge loss.

5.5.1 Permanent threshold voltage shift modeling

The complex evolution of ΔV_{TH} plotted in Fig. 5.6 is due to the concurrent actions of interface trap formation and charge trapping, which evolve with different kinetics. Therefore, we need two models to quantitatively describe ΔV_{TH}: 1) the interface trap generation model; 2) the charge trapping model.

Let us start with the interface state model. We suppose that the number N of interface traps depends on the radiation-damaged area, i.e. $N = K_1 \cdot a_D$, where a_D is the percentage of damaged area and K_1 is a proportionality constant. After the dose increment $d\phi$, the number of interface traps is increased by an amount dN proportional only to $d\phi$ and to the percentage of undamaged area, $a_{UD} = (1 - a_D)$:

$$dN = K_2 \cdot d\phi \cdot a_{UD} = K_2 \cdot d\phi \cdot \left(1 - N \cdot K_1^{-1}\right)$$

Solving for N we obtain:

$$N = N_0 + \Delta N_{\max} \left(1 - e^{-\phi K_2 / K_1}\right). \qquad (5.2)$$

N_0 is the initial interface state number, and $\Delta N_{\max}$ is the maximum number of interface traps that can be generated.

This is a good approximation only up to 10Mrad(SiO_2), which is the maximum dose used here. In fact, our model predicts the saturation of N, which is in contrast to [36], where it is shown that the subthreshold swing increases up to 1Grad(SiO_2). Nonetheless, in [36] we found that in the low dose range (<10Mrad(SiO_2)) the N growth kinetics is much faster than in the range above 10 Mrad(SiO_2), likely because the ionizing radiation is much less effective in generating interface traps in those regions already damaged. Incidentally, in [76] the interface trap growth rate was empirically fitted by a $\phi^{2/3}$ power law that increases less than linearly. Noticeably, in our model we are neglecting the generation of new interface traps in those regions already damaged by irradiation, as schematically depicted in Fig. 5.9.

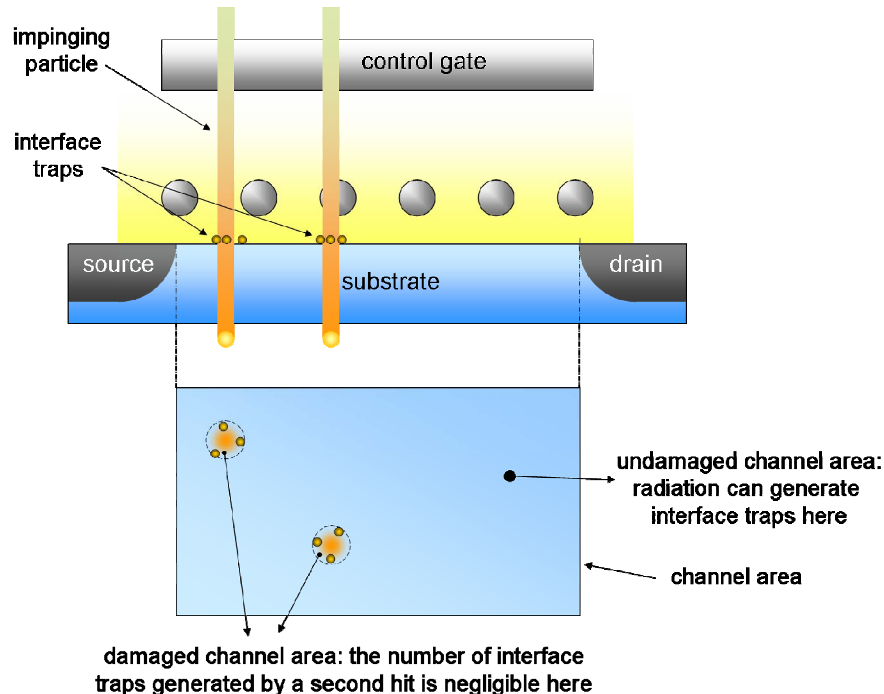

Fig. 5.9. Schematic representation of the trap generation model. An impinging particle can generate interface traps only in the undamaged channel area.

Because the subthreshold swing variation (S–S_0) linearly depends on the interface trap number variation (N–N_0), the evolution of S as a function of ϕ is:

$$S(\phi)-S_0=\Delta S_{\max}\left(1-\mathrm{e}^{-\phi/A}\right). \qquad (5.3)$$

We achieved a very good fit of the results in Fig. 5.7 (solid lines) with the values of ΔS_{max} and A listed in Table 4.

To model the positive charge trapping, we assumed:

A1) The interface traps are donor-like below the midgap, and acceptor-like above the midgap. Hence, the oxide trapped charge can be calculated from the midgap voltage (V_{mg}), i.e. the gate voltage at which the Fermi level at the Si/SiO_2 interface reaches the intrinsic Fermi level in silicon. In fact, under this condition, V_{mg} does not depend on the interface traps, but only on the net oxide trapped charge and on the FG- (NC-) stored charge. Nonetheless, due to the increased leakage of the irradiated samples, we cannot directly evaluate the midgap voltage variation. We calculated the midgap voltage variation (ΔV_{mg}) with the method described in the Appendix A.

A2) The trapped charge is uniformly distributed in the entire dielectric. Hence, ΔV_{mg} is proportional to the trapped charge density, which in turn depends on the number h of trapped holes. This is only a first order approximation, since the trapped charge density is all but constant along the tunnel and control dielectrics; in fact, near the gate and the substrate the trapped charge is easily neutralized [139]. Furthermore, in the nitride layer, positive charge generation and trapping is less likely to occur since the yield is negligible [151],[152].

A3) The radiation-generated holes are trapped in precursor sites, which may be either process-induced defects (e.g. E' centers) or radiation-induced defects. Each precursor defect can capture at most one hole.

A4) The number n_p of precursors correlates to the equivalent oxide damaged volume, like the interface trap model. Hence, n_p follows a saturating evolution similar to (5.2):

$$n_p=n_{p_0}+\Delta n_{p,\max}\left(1-e^{-\phi K_3}\right).$$

A5) Immediately after programming, the FG/NCs of an irradiated FGM/NCM store the same amount of charge than the programmed fresh device. Hence, the variation of V_{mg} depends only on the oxide trapped charge.

The dose increment $d\phi$ generates an increment of the trapped holes dh that is proportional to $d\phi\cdot n_{p,empty}$, where $n_{p,empty}$ is the number of empty precursors. From A3, $n_{p,empty}$ is the difference between the total number of precursors and the number of trapped holes h ($n_{p,empty}=n_p-h$).

DEVICE	ΔS_{max} [mV/dec]	*A* [krad]	*B* [mV]	*C* [krad]	*D* [mV]	*E* [krad]
NCM – X-rays	90	3200	460	3000	230	500
NCM – Protons	45	5800	320	2600	143	1500
FGM – X-rays	110	2800	490	2800	360	150
FGM – Protons	50	5420	200	2200	330	920

Table 4. Fitting parameter values used in the permanent threshold voltage shift model.

From A2, A3 and A4 we write:

$$dh = K_4 \cdot d\phi \cdot n_{p,empty} = K_4 \cdot d\phi \cdot \left(n_p - h\right) = K_4 \cdot d\phi \cdot \left[n_{p_0} + \Delta n_{p,\max}\left(1 - e^{-\phi K_3}\right) - h\right].$$

Taking into account that h is proportional to $-\Delta V_{mg}$ (from A1 and A2) and imposing $\Delta V_{mg}\left(\phi = 0\right) = 0$ we find:

$$\Delta V_{mg} = -B\left(1 - e^{-\phi/C}\right) - D\left(1 - e^{-\phi/E}\right) \qquad (5.4)$$

The good agreement between model and experimental data is shown by the solid lines of Fig. 5.10 (the fitting parameter values *B, C, D,* and *E* are listed in Table 4).

Finally, ΔV_{TH} is calculated by combining the S and ΔV_{mg} models of (5.3) - (5.4), with the method shown in the Appendix A:

$$\Delta V_{TH} = \Delta V_{mg} + V_{mg,FRESH} - \frac{S_{IRR}}{S_{FRESH}} \cdot \left(V_{mg,FRESH} - V_{TH,FRESH}\right) - V_{TH,FRESH} \qquad (5.5)$$

The solid lines of Fig. 5.6 show the comparison between the experimental data and the model.

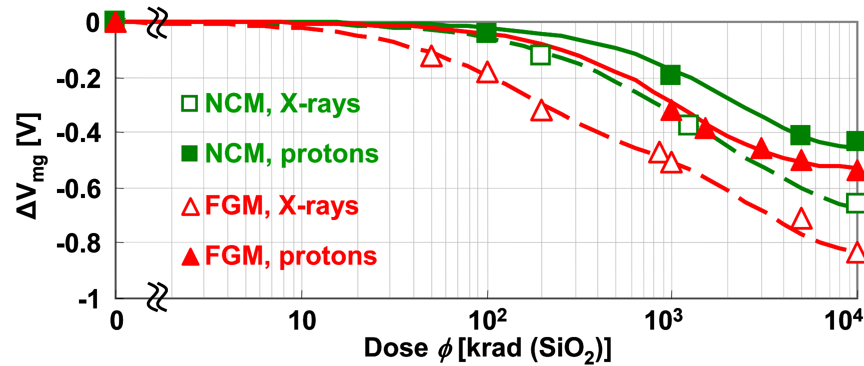

Fig. 5.10. Variation of the calculated midgap voltages in NCMs and FGMs after proton and X-ray irradiations. Solid curves are the theoretical model. Each experimental point is calculated as the average between 10 samples.

5.5.2 Prompt charge loss modeling

We define $Q_p\left(\phi\right)$ and $Q_e\left(\phi\right)$ as the stored charge in the programmed and erased FG/NCs, respectively. We assumed that the charge losses $-dQ_p$ and $-dQ_e$ are proportional both to the dose increment $d\phi$ and to the stored charge $Q_p\left(\phi\right)$ and $Q_e\left(\phi\right)$, respectively:

$$\begin{aligned} -dQ_p &= C_p \cdot Q_p(\phi) \cdot d\phi \\ -dQ_e &= C_e \cdot Q_e(\phi) \cdot d\phi \end{aligned} \quad (5.6)$$

C_p and C_e are the charge loss rate constants for electrons and holes, respectively. Solving (6) for $Q_p(\phi)$ and $Q_e(\phi)$, one obtains:

$$\begin{aligned} Q_p(\phi) - Q_p(0) &= Q_p(0)\left[1 - \exp\left(-C_p \cdot \phi\right)\right] \\ Q_e(\phi) - Q_e(0) &= Q_e(0)\left[1 - \exp\left(-C_e \cdot \phi\right)\right] \end{aligned} \quad (5.7)$$

In (5.7), $Q_p(\phi) - Q_p(0)$ and $Q_e(\phi) - Q_e(0)$ are proportional to $-\Delta V_p(\phi)$ and $-\Delta V_e(\phi)$, respectively, while $Q_p(0)$ and $Q_e(0)$ are proportional to $V_{THp}(0) - V_i(0)$ and $V_{THe}(0) - V_i(0)$, respectively; hence we can write:

$$\begin{aligned} \Delta V_p(\phi) &= -\left[V_{THp}(0) - V_i(0)\right]\left[1 - K_p \exp\left(-C_p \cdot \phi\right)\right] \\ \Delta V_e(\phi) &= -\left[V_{THe}(0) - V_i(0)\right]\left[1 - K_e \exp\left(-C_e \cdot \phi\right)\right] \end{aligned} \quad (5.8)$$

The constants K_p and K_e are used to take into account the small voltage drop that is always observable in fresh NCM devices within some hours, due to the slow motion of the negative trapped charge in the ONO stack even at zero gate bias, as previously shown in paragraph 4.3. A more complex equation with a different theoretical background has been proposed on [153],[154]. However such model requires more fitting parameters and it converges to (5.6) for low-LET particles.

By combining (5.5) and (5.8) into (5.1), we obtain a perfect fit of the charge loss data of Fig. 5.2-Fig. 5.4 (solid and dashed lines), with the parameter values listed in Table 5.

DEVICE	**C_p [Mrad^{-1}]**	**C_e [Mrad^{-1}]**	**K_p [%]**	**K_e [%]**	**[V_{THp}-Vi] @ (ϕ=0) [mV]**	**[V_{THe}-Vi] @ (ϕ=0) [mV]**
NCM – X	1.40	1.90	0.91	0.95	993	-910
NCM – P	0.40	1.18	0.91	0.95	983	-965
FGM – X (5V)	5.88	12.50	1.00	1.00	2492	-2661
FGM – X (3V)	5.71	13.33	1.00	1.00	1190	-1718
FGM – P (5V)	2.22	4.89	1.00	1.00	2544	-2604
FGM – P (3V)	2.08	4.96	1.00	1.00	1340	-1796

Table 5. Fitting parameter values used in the charge loss model. X stands for X-ray irradiation, and P stands for proton irradiation.

5.6 Discussions

5.6.1 Charge loss and data retention

By comparing the NCM's and FGM's behavior, we see that *NCMs feature a much stronger radiation tolerance over FGMs from all points of view*, even though the FGMs were programmed with a wider window and they have a much thicker tunnel oxide (~10 nm vs 5 nm).

This improvement is clear just considering the prompt charge loss. For instance, Fig. 5.4 shows that the FGM programming window decreases from 5V to 1.24V after 200 krad X-ray irradiation. For comparison, the programming window of NCMs after the same irradiation is 1.23V even though the initial value was 2V. The superiority of the NCM radiation tolerance becomes even more evident when considering the FGMs with an initial window of 3V: after 100 krad X-rays the FGMs' programming window is 1.08 V, i.e., 400mV smaller than NCMs' with the same irradiation conditions. The same considerations apply to the proton irradiated devices.

The data retention experiments of Fig. 5.8 confirm the good robustness of NCM approach against irradiation and stress again its superiority over FGM. Incidentally, NCMs feature a better retention capability despite their thinner tunnel oxide.

The improved tolerance against X-ray and proton irradiations of NCMs with respect to FGMs derives from several contributions. First, the nanocrystal technology allows a much better retention thanks to the discrete nature of the storage sites. In fact, on FGMs very tiny leakage currents may discharge the entire floating gate, while on NCMs a leakage path affects only the neighboring NCs.

Second, the smaller coverage area of the nanocrystals (15% of the total gate area in our devices) compared with the floating gate coverage area (100%) positively impacts on both the charge loss and the retention properties. In fact, only a fraction of protons (those impinging very close to the discrete NCs) are effective in the prompt charge loss. Similarly, only a fraction of the energy deposited by the X-ray irradiation takes part in the photoemission process from the NCs. Moreover, due to the small NC coverage area, there is a smaller probability that a defect will be created below a storage node. Hence, only a few of the defects are really effective in discharging the storage medium. In contrast, in a FGM all leakage paths contribute to the progressive FG discharge.

Third, the tunnel oxide thickness plays an important key-role. In fact, in the thin NCM tunnel oxide, a smaller amount of charge can be generated by the radiation and then collected by the storage nodes.

The different charge removal rates between protons and X-rays shown in Fig. 5.2-Fig. 5.4 suggest that the photoemission plays a key-role on the charge loss. In fact, protons deposit almost the same dose in Si and SiO_2; instead, for a given photon fluence, X-rays deposit almost twice the dose in Si compared to SiO_2. Hence, for the

same SiO_2 dose, X-ray irradiation deposits much more energy in the silicon storage sites (NCs or FG) with respect to proton irradiation, leading to an enhanced photoemission. Furthermore, 10-keV X-rays may also feature dose enhancement effects due to the presence of high-Z metals used in silicides, and to the photoelectric adsorption especially at the Si/SiO_2 interfaces [76], which further enhances the charge loss from NCs/FG.

Remarkably, X-ray irradiation of NCM and FGM devices feature the same dose enhancement with respect to protons by a factor in the range of 2-3, according to [155].

Incidentally, by comparing the charge loss rates for electrons and holes (see C_p and C_e in Table 5), FG/NCs are neutralized more easily if they are positively charged rather than negatively charged. This is due to the enhanced electron mobility in the oxide. In fact, the electrons that survived the prompt recombination can move toward the positively charged NCs or FG quickly. On the contrary, due to their lower mobility, the photogenerated holes are likely recombined or trapped before they reach the negatively charged NCs/FG.

5.6.2 Permanent radiation damage

The reduced tunnel and control dielectric thicknesses give some benefits even in terms of permanent damage of the cell electrical characteristics. Our achievements show that, even though the cells are reprogrammed, a permanent threshold voltage variation appears after 1Mrad(SiO_2) for NCMs and 100krad(SiO_2) for FGMs. At low doses, the positive charge trapping is the dominant phenomena, producing the initial decrease of the threshold voltage. This variation is more pronounced in FGMs than in NCMs, owing to the thicker tunnel and control dielectrics of FGMs with respect to NCMs. In fact, thicker dielectrics are much more prone to positive charge trapping than thin oxides [73]. At higher irradiation doses the increase in the subthreshold slope partially compensates the effect of positive charge trapping in the dielectrics, producing the turnover of ΔV_{TH} in Fig. 5.6.

Our model permits us to distinguish and separately quantify the contributions of interface states and positive charge trapping on the threshold voltage variation, which have different strength on NCMs and FGMs. In Table 4, the model parameters describing the degradation kinetics are mainly radiation-source dependent. The subthreshold swing is larger in FGMs than NCMs due to the thicker overall dielectrics. However, from the ratio of the gate dielectric thicknesses we expect S in FGM to be larger than in NCM by a factor 1.47. Nonetheless, experimental data show that such factor is only 1.2-1.3. This is not surprising, since we must take into account for the larger control-gate-to-FG coupling area, with respect to FG-to-substrate coupling area. In fact, the control gate completely surrounds the FG, while in NCMs the control gate is parallel to the NC layer (see Fig. 4.16).

The same considerations hold true for the positive charge build-up, which is larger in FGM. Incidentally we obtain the same factor 1.2-1.3 between the ΔV_{mg} of FGMs and NCMs, for the same irradiation conditions.

Finally, some considerations are worthy about the radiation source dependence of the permanent damage. The interface state generation is higher during X-ray irradiation, owing to the larger energy deposited in the Si/SiO_2 interface [76]. Nonetheless, paradoxically proton irradiation might be a bigger concern from the circuit viewpoint. For instance, a 10-Mrad(SiO_2) proton irradiation causes a larger V_{TH} decrease compared with X-ray irradiation at the same dose. In fact, even though X-ray irradiation produces a larger positive trapped charge within the dielectrics, the V_{TH} reduction is partially mitigated by the interface state generation, which tends to increase V_{TH}. Proton irradiation generates much less interface states, thus the V_{TH} shift is dominated by the positive charge trapping contribution, at least up to 10Mrad(SiO_2).

5.7 NCM vs. FGM Radiation Reliability

When considering the ionizing radiation effects on nonvolatile memories, the most important issues are the prompt charge loss after irradiation and the long term data retention characteristics. At higher doses, also the permanent radiation effects on the electrical characteristics become a concern, because they can produce the permanent cell threshold voltage shift.

The nanocrystal approach brings a significant improvement in all fields. The most impressive improvement is the immunity to leakage currents up to 10Mrad(SiO_2) proton irradiation shown in Fig. 5.8. In fact, after 10Mrad(SiO_2) proton irradiation, NCMs show the same evolution than fresh NCM featuring a 14% programming window decrease in a 10-year projection. A worse condition is represented by the X-ray irradiations due to dose enhancement effects, where the programming window is estimated to reduce in 10-year by 19% and 30% after 5Mrad(SiO_2) and 10Mrad(SiO_2) irradiations, respectively. In Fig. 5.8, we showed also that the retention characteristics of NCM irradiated with protons at 10Mrad(SiO_2) is even better than the FGM irradiated at only 1Mrad(SiO_2), *indicating that the improvement factor of NCM vs. FGM is greater than 10*, despite the NCM tunnel oxide thickness is half than in FGM. If we take as failure criteria the 20% reduction of the programming window [2], nanocrystal memories largely remain within this specification after 10Mrad(SiO_2) proton and 5Mrad(SiO_2) X-ray irradiations, while FGMs are widely out of the specifications for doses as low as 1Mrad(SiO_2), even for proton irradiation.

Another very significant improvement is the charge loss. In fact, by considering the percentage of the window closure, we can quantify that the nanocrystal technology increases the charge loss robustness by a factor ~3 and 4.5 for proton and X-ray irradiations, respectively (see Fig. 5.4). For instance, after 200krad(SiO_2) X-ray irradiation, NCMs keep the 63% of the initial programming window. In contrast, the

FGM programming window reduces to the 58% of its initial value after only 50krad(SiO_2), independent of the initial programming window values.

A further important projection is also the even larger robustness against TID if the nanocrystal samples were manufactured without the ONO stack. At this purpose, in Fig. 5.11, we show the percentage of programming window closure, due to prompt charge loss, calculated using (5.8) and the fitting parameters of Table 5, with unitary K_P and K_E values (i.e. not considering the effects of the ONO stack). The improvements in terms of radiation robustness are constant for each dose and it is greater than 3 and 5, for proton and x-ray irradiation, respectively. Noticeably, this improvement is independent of the initial programming window: in fact, in Fig. 5.11, the calculated curves of the FGM programmed at 5V and 3V almost overlap each other.

This large improvement of NCM charge loss moves the reliability issues to the peripheral circuitry. In fact, [132]-[134] showed that the most sensitive part of the Flash memory chip is the peripheral circuitry, which may fail at doses as low as 10krad. This is more than one decade below the dose required to reach the 20% charge loss in NCMs. However, the thinner oxides of NCMs permit the reduction of the programming voltages with respect to FGMs. Hence, charge pumps and the peripheral circuitry MOSFETs might be designed with thinner oxides, potentially increasing the immunity against trapped charge, which can sensibly change the threshold voltage.

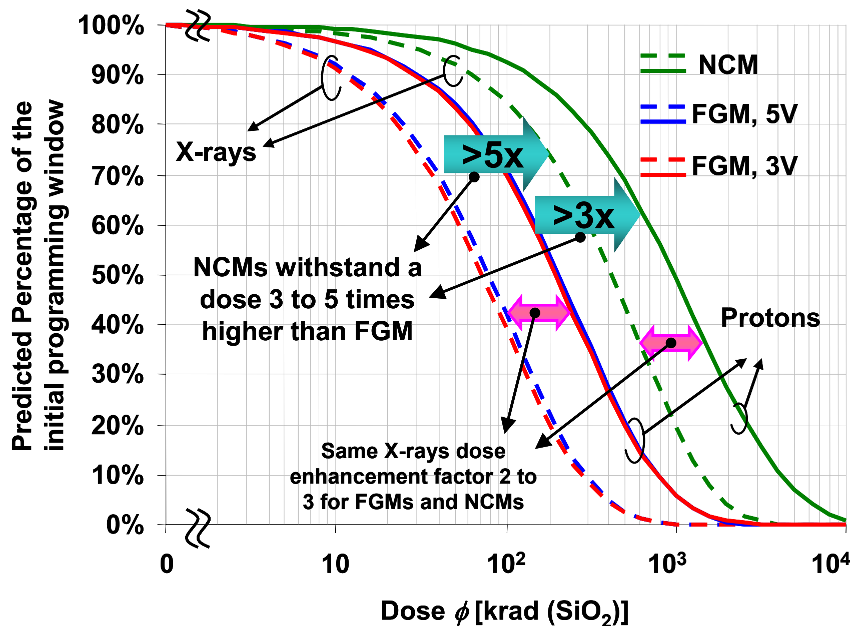

Fig. 5.11. Comparison between the percentage of charge loss of NCM and FGM, calculated using (5.8) and the fitting parameters of Table 5, with unitary K_P and K_E values. The improvement for NCM is almost independent of the initial FGM programming window (3 or 5V).

5.8 Nanocrystal memory and SONOS TID response comparison

In this section we will perform a comparison between the NCM and SONOS total ionizing dose response, using data found in the literature.

Very few works addressed the radiation response of trap-based memories like SONOS and NROM, mainly due to the relatively novelty of this new kind of memory approach and to the lack of the cell-level access of commercial devices. A quite recent work [156] investigated some of the most important aspects concerning the total ionizing dose effects on SONOS memories. In particular, in [156], the authors focused on the prompt charge loss, the dual-bit capability, and on the retention properties.

SONOS memories might, in principle, exhibit very good radiation tolerance levels as NCMs. In fact, the charge is not stored in a monolithic floating gate and the presence of discrete storage sites acts as a form of intrinsic redundancy, which increases the cell reliability.

Unfortunately, the technology used in 1 is very different from that used in our experiments. In fact, beside the very small difference in the cell gate length (350nm vs 300nm of our samples), the technology examined in [156] is SOI (silicon on insulator). The silicon on insulator technology has the advantage of being more immune to SEE (in particular SEL and SET), because of the smaller charge collection [157]. In fact, the silicon dioxide has a much wider energy gap than silicon, hence, less charge can be generated by the impinging ion and then collected by sensitive nodes. However, SOI might show some drawbacks due to its thick buried oxide. In fact, the radiation-induced trapped charge in the buried oxide might impact on the MOSFET/cell threshold voltage [157], leading to a compromised functionality of the peripheral circuitry or to the inability of retrieve or even store the correct information (see Chapter 1).

In [156], the authors used 10-keV X-rays as radiation source. Even if we cannot perform a conclusive comparison between the SONOS and the NCM approach, the same radiation source allows us at least to draw some consideration about the particular NCM and SONOS technology used in this thesis (NCM) and in [156] (SONOS). In Fig. 5.12, we show the schematic cross-section of the devices analyzed in [156].

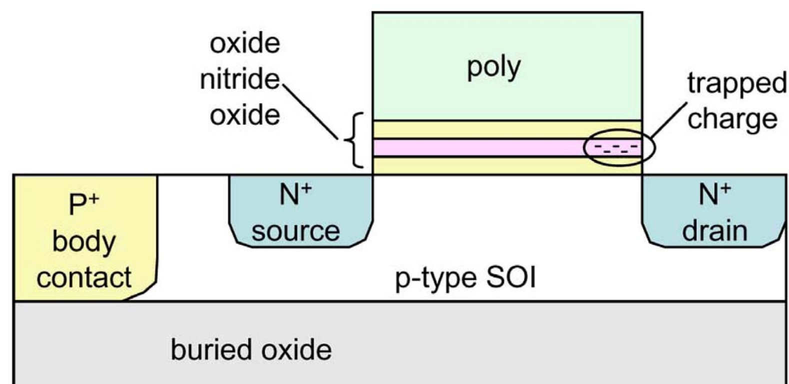

Fig. 5.12. Cross section of the SONOS memory cell analyzed in [156].

In Fig. 5.13, we report the I_D-V_{GS} characteristics measured on a NROM memory cell. Noticeably, the programming window increases with increasing currents. This is in agreement with the results found in Chapter 4 (see Section 4.2). In fact, the erased NROM cell analyzed in [156] is almost neutrally charged, while the programmed cell is negatively charged leading, to a programming window, which increases with increasing readout drain currents.

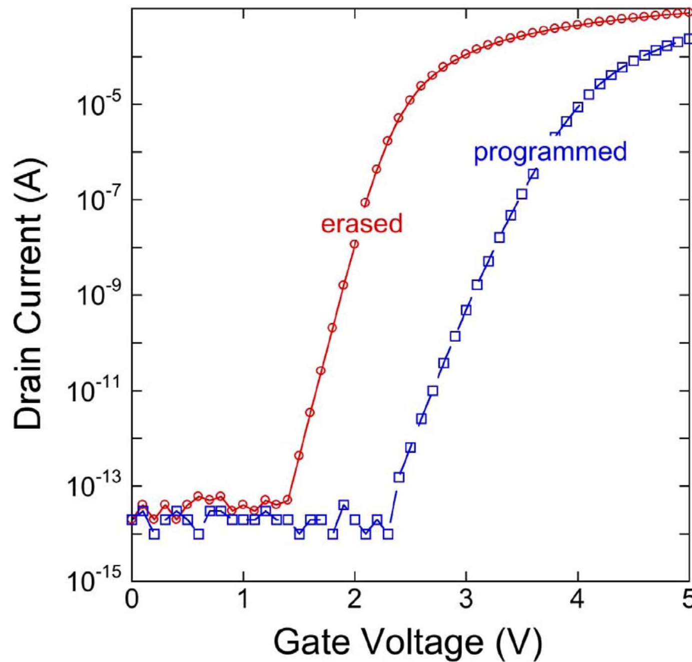

Fig. 5.13. I_D-V_{GS} characteristics of unirradiated SONOS memory cells, after program and erase operations [156].

In Fig. 5.14, we report the I_D-V_{GS} of a programmed (Fig. 5.14a) and erased (Fig. 5.14b) measured after different irradiation doses. Noticeably, both the programmed and the erased cells exhibit a leftward I_D-V_{GS} shift. The threshold voltages (extrapolated at I_D=300nA) are shown in Fig. 5.15.

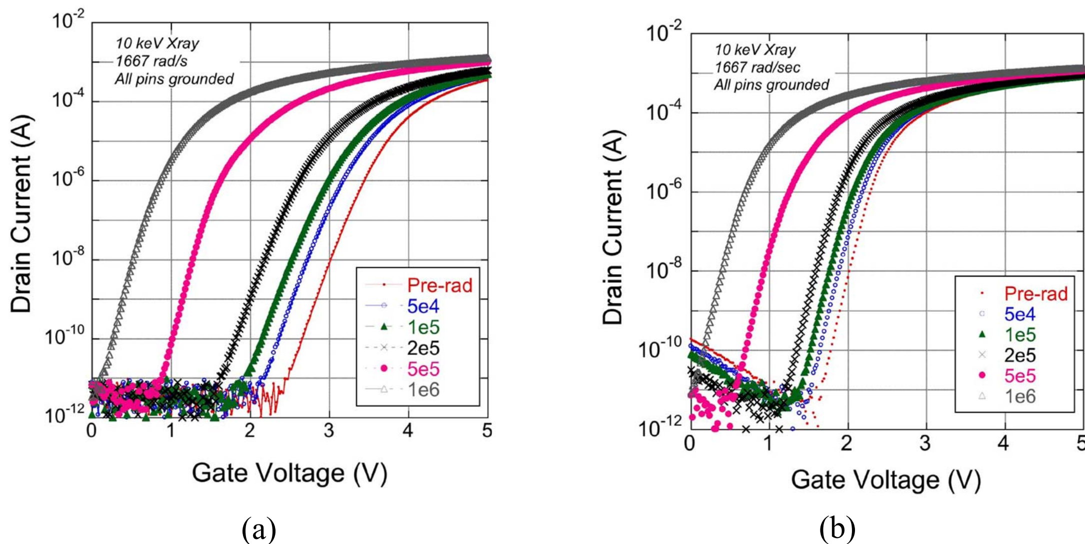

Fig. 5.14. I_D-V_{GS} characteristics of programmed (a) and erased (b) SONOS memory cell after various irradiation doses [156].

Unlike NCMs (see Fig. 5.2), both the programmed and the erased cell threshold voltage decrease with increasing radiation dose. The decreasing threshold voltage of the erased cell is not due to the neutralization of the stored charge, but it is due to positive charge trapping in the thick buried oxide. In particular, the threshold voltage of the erased cell drops from about 2.25V to 0.5V. This means that the charge trapping in the buried oxide induces more than 1.75-V permanent voltage drop. This drop might seriously compromise both the cell information sensing, and the information storage especially if used in the 1.8V systems. In particular, in NOR topologies, the induced threshold voltage variation would turn on all the cells of the same bitline, compromising the whole sector functionality. Nonetheless, by looking at the data of Fig. 5.15, we argue that, if a reference cell (which is uniformly degraded as the other cells of the sector) is employed, the information could be sensed even after a 200-400krad(SiO_2) X-ray irradiation.

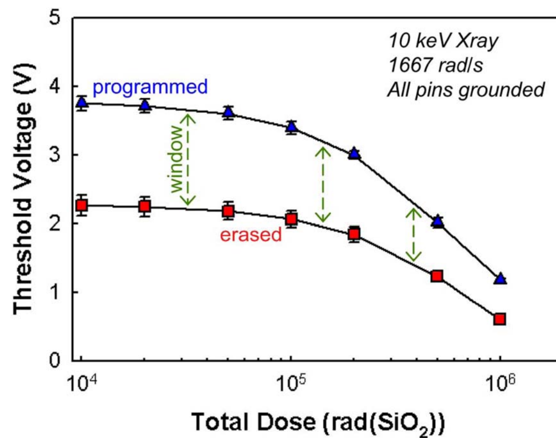

Fig. 5.15. Threshold voltages extrapolated from Fig. 5.14, as a function of the irradiation dose [156].

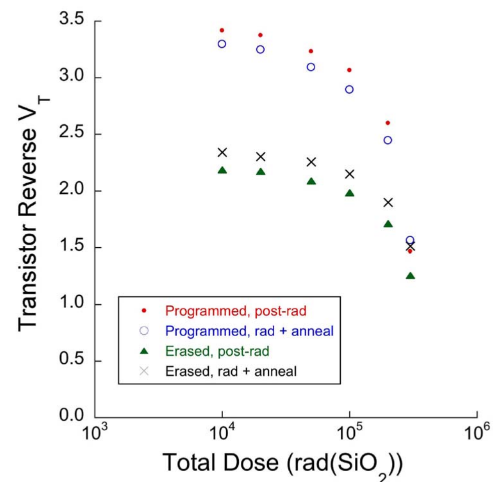

Fig. 5.16. High temperature 20-hr retention experiment performed on SONOS memory cell, after various irradiation doses [156].

Still, if we assume that the large negative threshold voltage shift is due only to the presence of the thick buried oxide, we argue that the SONOS cell might exhibit a much more limited permanent threshold voltage variation (as found in NCM), if implemented in bulk CMOS technology. From this point of view, in fact, the cell still feature a 0.8-V programming window after 500krad(SiO_2), which is comparable to the 0.74-V estimated NCM programming window after a 500krad(SiO_2) X-ray irradiation (see Fig. 5.4). If we consider only the percentage of the prompt charge loss, the SONOS cells of [156] are somewhat more robust than our analyzed NCM samples. In fact, the remaining 0.8-V programming window after 500krad(SiO_2) corresponds to about the 53% of the initial 1.5-V initial programming window value. This percentage must be compared to the remaining 0.74-V out of an initial 1.8-V value (i.e. 41%), observed in NCM memories (see Fig. 5.4 and Fig. 5.11) after the same irradiation dose. This might arise from the presence of much deeper traps in the nitride layer, which require more energy to release their electrons. Incidentally, the presence of deep traps in the nitride layer or the nitride/dioxide interface is also a drawback, which severely limits the

endurance of these kinds of devices. In fact, during the programming operations, negative charge is permanently trapped in the nitride layer, causing a progressive permanent increase of the cell threshold voltage [148].

The comparison with FGMs indicates that the SONOS approach brings a much stronger radiation tolerance. In fact, by looking at Fig. 5.11, FGMs feature a programming window, which is halved at only 70krad(SiO_2), i.e. at a dose, which is about 7 times lower than that required to reduce the SONOS programming window to the 53% of its initial value, due to charge loss. The increased radiation robustness with respect to FGMs derives from the absence of the monolithic floating gate, the absence of low-energy-gap conductive storage media (in which charge can be photogenerated), the charge storage in deep traps, and to the thinner dielectrics.

The retention characteristics of the irradiated devices are shown in Fig. 5.16. Even no long term room-temperature retention was performed, in [156], the authors stated that the 20-h 200-°C anneal time is a good indicator of the 10-year retention capability, as also confirmed by [158]. Data highlight good retention characteristics at doses larger than 200krad(SiO_2), but a failure after 300krad(SiO_2). This is comparable to the conventional FGMs. From this point of view, SONOS exhibit a much less tolerance to ionizing radiation with respect to NCMs (which can withstand at least a 5-Mrad(SiO_2) X-ray irradiation, in terms of long-term data retention). This is due to the different nature of the storage sites. As already mentioned, from the retention viewpoint NCMs show much better retention (even the unirradiated samples) because they suppress the Poole-Frenkel effect, which instead occurs on nitride traps [25].

5.9 Conclusions

For the first time we directly compared the radiation tolerance of nanocrystal and floating gate cells, employing two different radiation sources: X-rays and protons. Compared to FGMs, NCMs show a much better robustness against X-ray and proton irradiations. In fact, NCMs can withstand a radiation dose 3 and 10 times larger than floating gate cells in terms of charge loss and data retention, respectively. We also found that X-rays produce dose enhancement effects with respect to protons, accordingly with the data previously reported in the literature for semiconductor devices.

We have also developed a first order model in order to evaluate both the charge loss and the permanent threshold voltage variation. Despite its simplicity, it excellently fits both FGM and NCM data, highlighting that the physical mechanism responsible for the window closure is the same for both devices, but with reduced strength in NCMs.

Several factors contribute to improve the NCM radiation tolerance: the presence of discrete storage sites, the smaller nanocrystal coverage area, and the thinner dielectrics.

The results achieved on NCMs are in good agreements also with data reported in literature on nitride-trap-based memory cells, which exploit the discrete charge storage

approach as well. If we consider only the prompt charge loss, NCMs were slightly less tolerant than SONOS (but still much stronger than conventional FGMs). On the other hand, if we consider also the permanent threshold voltage variation induced by radiation, our NCM samples were much more radiation tolerant than SOI-SONOS, without the need of complex sensing circuitry. Still, this issue is mostly related to the presence of the thick buried oxide (which is not present on bulk planar technology), rather than being intrinsic to the SONOS concept. However, the NCM approach exhibited a much stronger radiation tolerance in terms of retention than SONOS (by a factor greater than 25). This latter consideration is not dependent on the SOI technology, but it is intrinsic to the way the charge is trapped on the storage sites: from this viewpoint, NCMs could be very well suited to embedded applications requiring long term data retention and radiation robustness.

These results open new issues, such as: the effects of radiation induced peripheral circuitry degradation on the chip reliability; the impact of the cell scaling on the radiation tolerance of NCMs. At this regard, we expect a reduced immunity when the number of nanocrystals will drop, as the cell is scaled. Nevertheless, the thinner tunnel dielectric may still be an advantage over the FGM approach, because less charge can be collected by the storage sites.

CHAPTER 6

Heavy Ion irradiation effects on nanocrystal memories

As already discussed, nanocrystal memory are very promising from the radiation tolerance viewpoint. In fact, in the previous chapter we showed a very large improvement with respect to Floating Gate memories, at least as far as TID effects are concerned. In this section a detailed analysis of the heavy ion effects on nanocrystal memories will be performed. Heavy ion effects are somewhat different from TID and they deserve a separate analysis.

Firstly, we will show the heavy ion effects on nanocrystal memory CASTs, focusing on the effects of different ion LET and fluence. The effects on the retention, the threshold voltage shift and stress kinetics will be analyzed. Secondly we will employ addressable arrays to perform a much more detailed analysis, in particular on the charge loss and on the retention. Finally, a model will be provided, which allows to estimate the charge loss as a function of several factors, such as nanocrystal density, charge, ion LET, etc. Furthermore, the model also allows to estimate the size of the area affected by the ion-strike.

6.1 Devices used in heavy ion irradiations

To evaluate the effects of heavy ion irradiation, we used CAST and addressable arrays manufactured by StMicroelectronics M6 (Catania, Italy). CAST structures do not allow to determine the effects on the single cells, still they are very useful to determine the average effect of heavy ion irradiation and to assess if any latent damage, induced by radiation, is depassivated by stress. In particular, if one wants to perform accelerated stress, the CAST is very useful [141], being able to stress a large amount of cell, at the same time. If breakdown occurs, it can be easily detected. On the contrary, the addressable arrays are useful to determine the specific cell behavior, allowing a large number of cells to be analyzed in detail.

Each addressable array contains 16 M cells, organized in 32 blocks of 512 kbits, in NOR configuration. Each block is divided in 8 sectors of 64 kbits. The on-chip test structures allow to determine the threshold voltage of each cell, and to measure the cell transcharacteristics. Cells are programmed by CHISEL and erased through FN tunnel.

As it has been already noticed in the previous chapters, CAST structures are programmed using timed operations: neither smart algorithms nor threshold voltage checking are adopted during the program/erase operations. On the contrary, the addressable arrays have the built in programming circuitry, which allows smart program and erase algorithm. This, in turn allows for a much tighter control on the cell threshold voltage. Programmed cells are negatively charged, while erased cells are almost neutral. Further details on addressable arrays will be given in section 6.3.

6.2 Radiation effects on CAST

6.2.1 Experimental setups

The irradiations on CAST structures were performed at the SIRAD facility of the Tandem Van Der Graaf accelerator at the INFN Legnaro National Laboratories, Italy [159]. The samples were irradiated with I ions (301 MeV, LET = 64 $MeV{\cdot}cm^2{\cdot}mg^{-1}$) and Ni ions (182 MeV, LET = 31.3 $MeV{\cdot}cm^2{\cdot}mg^{-1}$) at wafer level. For each ion we used three fluences: $0.83{\cdot}10^8$ ions/cm^2, $1.7{\cdot}10^8$ ions/cm^2, and $3.3{\cdot}10^8$ ions/cm^2, corresponding to hit cells percentage (assuming a single ion hit on a cell) of 5%, 10% and 20%, respectively, in the CAST. We irradiated 12 CASTs for each ion type and fluence value. The maximum ion fluence has been chosen in order to keep small enough the percentage of double hits on the same cell. We calculated (see Appendix B) that the double hit probability is 0.12%, 0.45%, 1.6% for an ion fluence of $0.83{\cdot}10^8$ ions/cm^2, $1.7{\cdot}10^8$ ions/cm^2, and $3.3{\cdot}10^8$ ions/cm^2, respectively. It should also be noted, that the probability of a triple hit is well above zero. The numbers of cells, which may have been statistically hit by 3 ions are: 5, 39, 286, for the 3 fluences (details are shown in the Appendix B). Additionally, for the higher fluence, 14 cells could have been statistically hit by 4 ions.

Program and erase operations were performed through FN tunnel, applying a 2-ms +15 and -15V gate pulse, respectively. As in chapter 5, the threshold voltage V_{TH} has been defined as the V_{GS} value required by the CAST to drive a drain current I_{DTH}=25μA, with V_{DS}=50mV.

6.2.2 Permanent degradation: subthreshold slope and gate leakage

In this section we will briefly show the permanent radiation effects on the electrical characteristics.

Despite the large gate dielectric thickness, after irradiation we measured an increased oxide leakage current, as shown in Fig. 6.1 for two CAST arrays irradiated with $3.3{\cdot}10^8$ I ions/cm^2 and $3.3{\cdot}10^8$ Ni ions/cm^2, respectively. At V_{GS} = 4V the gate current increases from 1 pA (fresh) to 100 pA and 30 pA after I and Ni ion irradiation, respectively. As expected, the gate current increase is larger after I ions irradiation, due to the larger LET coefficient. The large gate current enhancement derives from the formation of one or more permanent conductive paths across the gate dielectric, due to

the ion hit. Moreover, we observed the large leakage current increase only in some irradiated CASTs. In particular, we measured this current increase in 25% of irradiated samples with the highest fluence (50000 ion hits), while only 5% of the CAST irradiated at lower fluence (25000 and 12500 ion hits) exhibited an appreciable gate current increase. This indicates that this conduction does not uniformly affect the whole gate area, but rather is localized in one or few leaky spots that have a limited probability of being activated by the impinging ions. Still, those leakage may also arise from a very high ion hit number occurred on the same cell(s). In fact, 4 ion hits are statistically unavoidable at the higher ion fluence, and a cell in about one CAST out of two could even experienced five ion hits.

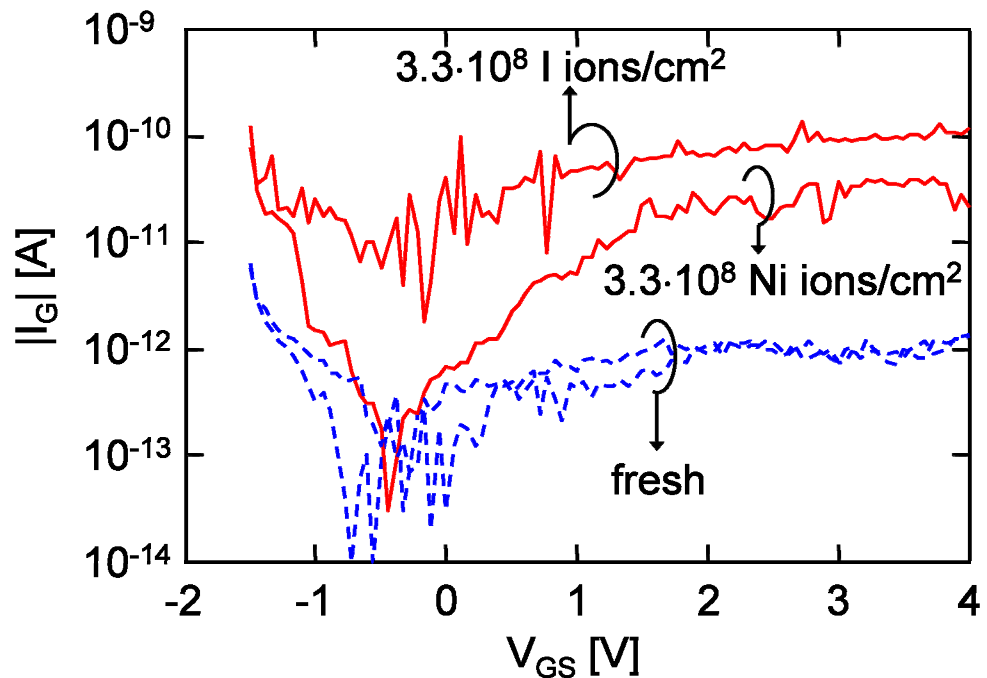

Fig. 6.1. Gate leakage current measured before and after I and Ni irradiation with an ion fluence of $3.3 \cdot 10^8$ ions/cm^2 in two CASTs.

But, what is the physical nature of the 100-pA steady state leakage current after I ion irradiation (see Fig. 6.1)? Due the large thickness of the overall insulator between the control gate and the Si substrate (12 nm + 5 nm thick = 17 nm), this conduction can not be attributed to mechanisms, such as single trap assisted tunneling producing RILC [160] or multi-trap driven RSB, which are observed in much thinner oxides (<5-6nm) [99]. Yet, previous studies [161] highlighted that radiation effects on 10-nm oxides reveal similarities with the behavior of thinner oxides, such as a measurable DC leakage current. The origin of this leakage current is related to a multi-trap-assisted conduction through a defect cluster generated along the ion track. In our NCM devices, this conduction mechanism is seldom observed; it could be promoted, or even activated, when the ion hits the gate oxide in close proximity to a nanocrystal, interacting with the ion-generated defects to enhance the path conductance. The generation probability of such paths is very low, around 10^{-5} – 10^{-6} spot/ion, in agreement with previous studies on thin gate oxide submitted to heavy ion irradiation [101],[162]-[165]. Remarkably,

the weak spots responsible for the large gate current increase could be associated to the defects generated along overlapping ion tracks. In fact, we remind that at the highest fluence, several cells might have experienced 4 hits, and there is still 50% of probability that a single cell per CAST has experienced even 5 hits.

Finally, the drain current in subthreshold region is shown in Fig. 6.2 for both the programmed and the erased states before and immediately after irradiation. Noticeably, irradiation induces negligible changes in the CAST drain current, without affecting the subthreshold slope as well. This is in agreement with previous measurements on FG memory cells [166] that showed no degradation of the cell transistor electrical characteristics after a single heavy ion hit.

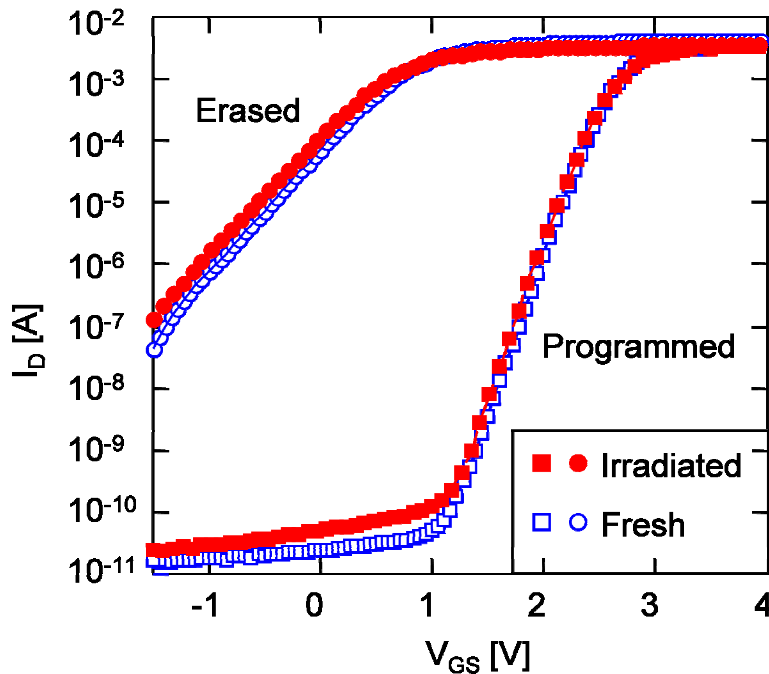

Fig. 6.2. I_D-V_{GS} curves measured before and just after irradiation with $3.3{\cdot}10^8$ I ions/cm^2.

6.2.3 Electrical Stresses and Irradiation

In order to assess if any radiation induced latent damage is present in the tunnel or control oxide, we submitted both fresh and irradiated arrays different stresses:

a) Constant Voltage Stress (CVS) with $|V_G|$ = 15V to 18V.

b) Bipolar Pulsed Voltage Stress (BPVS) by applying square pulses to the gate between $-V_G$ and $+V_G$ (V_G=15V or 16V) and pulse frequency from 10 Hz to 100 kHz.

All stresses were carried out with grounded source, drain and substrate. Fig. 6.3 and Fig. 6.4 summarize the effects of electrical stresses on some fresh and irradiated devices by using the two stress methods listed above. We measured also the CAST gate current during the program (I_g = 30nA) and erasure operation (I_g = -2nA). Both currents derive from Fowler-Nordheim tunneling injection. Any leakage current due to irradiation and/or electrical stress cannot be detected at this voltage level, being overwhelmed by the FN tunneling current. The gate current during electrical stress is plotted in Fig. 6.3,

showing the accelerated breakdown of irradiated oxide, at least when CVS is applied. The programmed and erased threshold voltage evolution is shown in Fig. 6.4a for CVS and in Fig. 6.4b during CVS and BPVS. In both figures irradiated and fresh devices are shown. Comparing Fig. 6.4a and Fig. 6.4b we observe no or negligible threshold voltage variation during negative CVS (as low as 200mV), while for both fresh and irradiated devices we observe a positive shift, as high as 1.6V, of the threshold voltages during positive CVS. No programming window closure is observed. In addition, BPVS produces also the progressive thinning of the programming window. In fact, the programmed threshold voltage shifts by 1.6V, as after positive CVS, whereas the erased threshold voltage increases by 2.8V, thus shrinking the programming window from 2.3V to 1.1V at the end of the PVS. No substantial difference appears between fresh and irradiated devices, regardless the ion type and fluences.

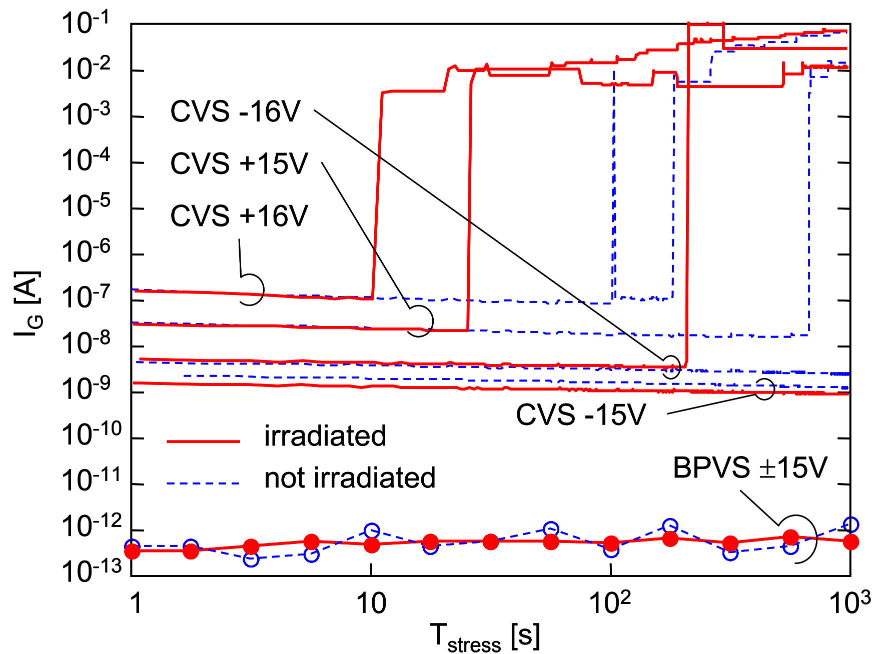

Fig. 6.3. Gate current during electrical stresses performed on irradiated and not irradiated devices. Different V_G polarities and modes (CVS and BPVS) are compared. For BPVS we show the I_G value read from I_G-V_G curves at V_G=4V.

Hence, from the viewpoint of reliability and endurance to electrical stress, heavy ion irradiation does not produce any measurable variation of the degradation kinetics of cell characteristics, before breakdown. The positive shift of the programming windows observed in Fig. 6.4a for both irradiated and fresh devices derives from the charge trapping in the ONO layer and interface trap generation in the tunnel oxide [23], as in conventional Flash cells. Differences between positive and negative CVS in Fig. 6.4a may be ascribed to the different electron energies during injection. If the negatively charged defects were generated in the ONO layer [23], then more defects should be generated with positive CVS, i.e., electron injection toward the gate. In this case electrons can gain much more energy than during negative CVS, when electrons are injected from the top oxide layer. Similarly, holes/hydrogen ions injected from the gate

during positive CVS may generate interface traps. It is worth to remark that negligible changes are observed between the irradiated and not irradiated arrays. Still, the injection currents must also be taken into account. In fact, during the negative CVS, the injection current is at least one decade smaller that during the positive CVS. Therefore, charge trapping, degradation and eventually breakdown are reasonably expected earlier.

At the beginning of each program and erase pulse, the nanocrystals store a net positive and negative charge, respectively. This means that, in the first instants of the pulse, the gate voltage mainly drops across the tunnel oxide, while, at the end of the charging process, the voltage drops across the ONO layer. Hence, we can argue that the thinning of the threshold window, observed after BPVS, is ascribed to the enhanced degradation of the tunnel oxide, which, in turn, quickly discharge many of the nanocrystals.

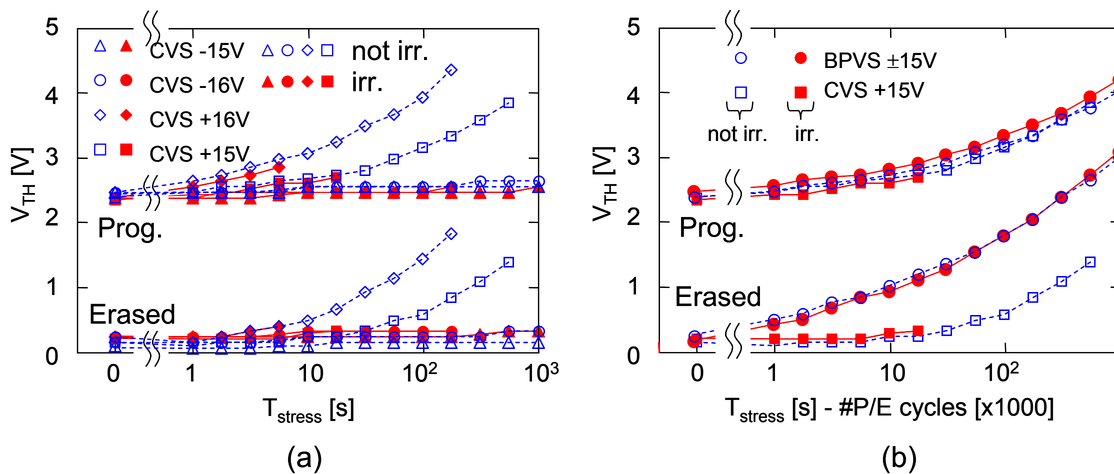

Fig. 6.4. Programmed and erased threshold voltage evolutions during positive and negative CVS as a function of the stress time, performed on one fresh and one irradiated CAST with $3.3\cdot10^8$ I ions/cm^2 (a). Comparison of the effects of CVS and bipolar stress in fresh and irradiated devices (b).

Remarkably, the irradiated devices usually breakdown earlier than non-irradiated samples. This means that irradiation produces weak spots in the gate oxide, which can act as seeds of further degradation, as previously reported [162]-[165],[167]. Nonetheless, these weak regions do not affect the degradation kinetics of the CAST programming window and no fast erasing or erratic bit is detected either after irradiation or during the following electrical stress.

Several works showed that a dense hole-electron pair cloud is created along the track, even in the dielectrics (see chapter 3). The instantaneous temperature may be so high to locally melt the silicon dioxide [91] and additionally, the recombination between holes and electrons may leave several neutral traps. Even though immediately after heavy ion irradiation no appreciable modification of the threshold voltage appears, the acceleration of TTDB (Time To Dielectric Breakdown) indicates the presence of some defective regions, corresponding to the ion hits. These regions have negligible effects on NC-MOSFET characteristics, but they may act as seeds of further degradation, when applying the high field electrical stress.

As a last remark, irradiated devices lifetime reduction is seen after CVS, i.e., when ONO is subjected to the higher oxide field. On the contrary irradiation is unable to produce accelerated breakdown during BPVS, at least in time intervals as long as those we used here. This peculiar behavior seems to confirm the idea that the major effects of heavy ion irradiation are in the ONO layers rather than in the tunnel oxide and, therefore, the accelerated breakdown observed after heavy ion irradiation should start from the ONO layer and later propagate toward tunnel oxide.

6.2.4 Prompt charge loss

Fig. 6.2 shows a very negligible variation on the I_D-V_{GS} characteristics, measured just after irradiation, both for those CASTs left in the programmed and those ones left in the erased state before irradiation. This is not unexpected, due to the discreteness nature of the stored charge: only those nanocrystals close to the ion track can be effectively discharged.

At this point, one may wonder how much is the threshold voltage shift induced by the heavy ion irradiation in a single cell. One or few programmed cells losing a critical charge would have produced an early turn-on of the anomalous cell(s). Unfortunately, the CAST structure does not allow to precisely establish the charge loss induced by heavy ions. However, they are still useful to draw some considerations and to depict some upper and lower bounds. It is worth also to remark that it is not easy finding a relation between the charge loss and the threshold voltage of a nanocrystal memory cell. In fact, whereas in a conventional Flash cell the charge in the floating gate is always uniformly distributed, in case of a nanocrystal cell, the charges are stored in discrete locations. When some nanocrystals have lost part of the stored electrons, the remaining stored charges do not rearrange themselves. This gives rise to a local variation of the charge density over the nanocrystal layer, consequently producing a local variation of the potential at the silicon/oxide interface. Hence the channel starts forming earlier in those regions where the nanocrystals have lost some of their electrons. This means that the effective threshold voltage shift of a nanocrystal cell is not only a function of the total charge lost, but it is also function of the position of the defective nanocrystals, i.e., those ones that have lost their charges. A model, which for the first time can numerically quantify the impact of the heavy ion irradiation is presented in section 6.4.

We can consider two opposite cases:

1) The small threshold voltage variation is due one cell featuring a very large threshold voltage shift (i.e. the cell(s), which experienced 4 or 5 hits)

2) The threshold voltage variation is due to each hit cell.

For sake of simplicity, we show the simulations results, considering only of the actual threshold voltage shift of the cell and not considering either the actual position or the charge lost by the defective nanocrystal. In Fig. 6.5a, we show the relation between the CAST threshold voltage shift and the damaged cell threshold voltage shift. The

different curves refer to different numbers of cells having lost charge. For instance, the 50-mV shift of Fig. 6.2 might be produced either by a 120-mV shift of 50000 cells, or by a 630-mV shift of 100 cells, or a 980-mV shift of a single cell. If the shift were produced by a single defective cell we should observe a kink in the CAST subthreshold current of Fig. 6.2, like that highlighted in the inset of Fig. 6.5b. For converse, we experimentally observed that the CAST drain current features a rigid leftward shift, which is a signature of a small charge loss in almost all the cells hit by an ion, producing a threshold voltage shift as large as 0.18V per cell.

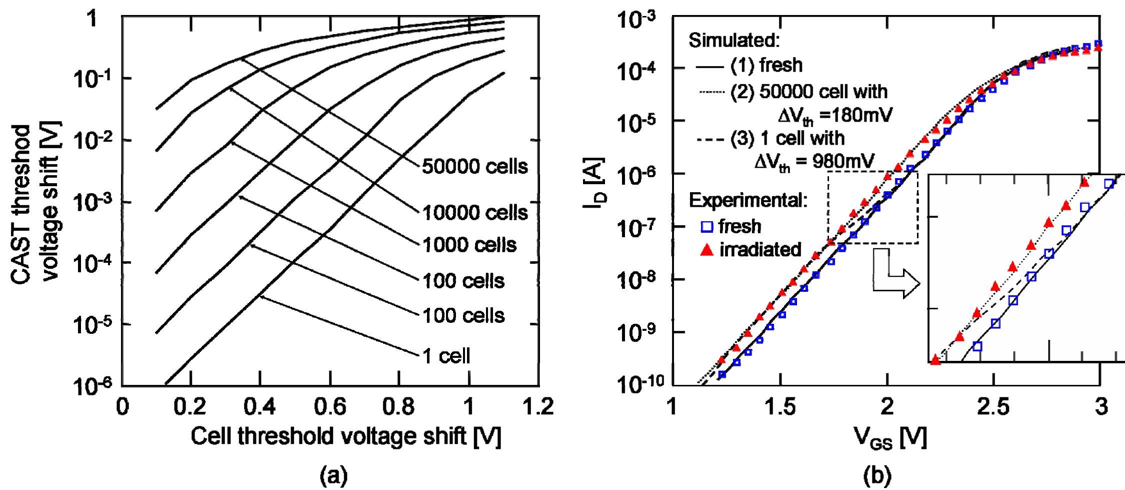

Fig. 6.5. a) Simulated relation between the CAST threshold voltage shift and cell threshold voltage shift. Different curves refer to different number of shifting cell. b) Comparison between simulated and experimental I_{ds}-V_{gs} curves in subthreshold region in the programmed CAST of Fig. 4. Three simulated curves are plotted: (1) the fresh devices immediately after the program operation; (2) effect of 50000-cell shift by 180mV; (3) effect of 1 cell shift by 980mV.

6.2.5 Data retention

We showed that the heavy ion should induce very small threshold voltage variations in nanocrystal memories, and no cell should have lost a critical amount of charge.

To assess the impact of the measured gate leakage currents shown previously, we performed retention experiments on programmed CASTs. After programming, all the irradiated and fresh devices were stored with all terminals floating and the I_D-V_{GS} curves were periodically measured over a 20 days period. The corresponding threshold voltage values are plotted in Fig. 6.6. The data in Fig. 6.6 correspond to the average of four CASTs. The threshold voltages decrease monotonically, with an average –25mV/time decade on fresh devices and –40mV/time decade on irradiated ones. The dependence on ion source and fluence is very small.

Fig. 6.7 shows the I_D-V_{GS} curves of irradiated CAST taken immediately, 9 days and 20 days after programming. The subthreshold slope does not change during this charge retention experiment. This means that no cell in the array has lost a critical amount of

stored charge, large enough to produce a threshold voltage shift in the cell, much larger than the average shift of the whole CAST, which is in the 100-mV range.

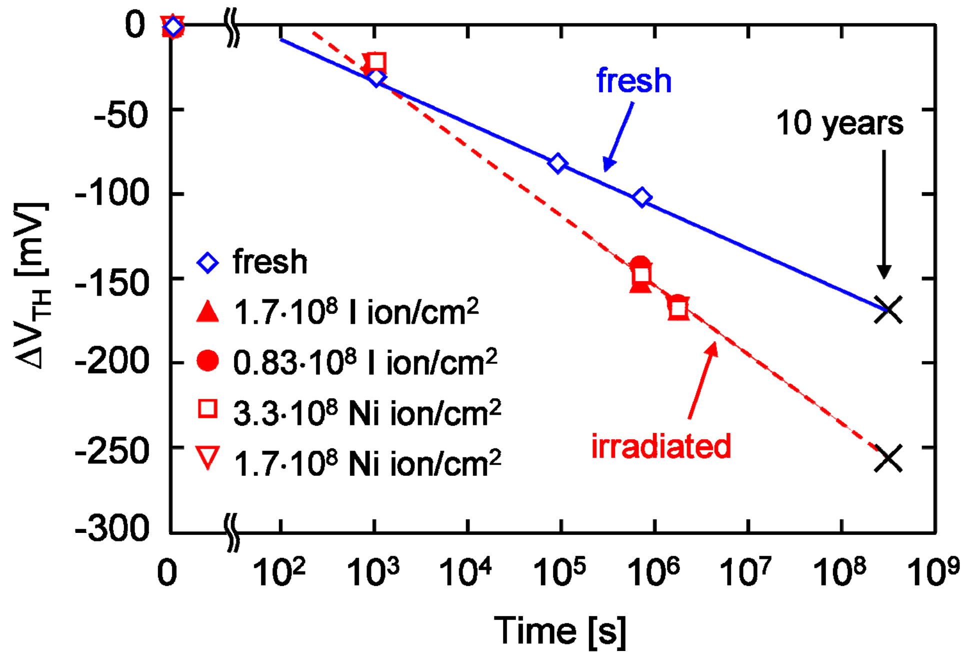

Fig. 6.6. Retention characteristics of fresh and irradiated nanocrystal memories in the programmed state.

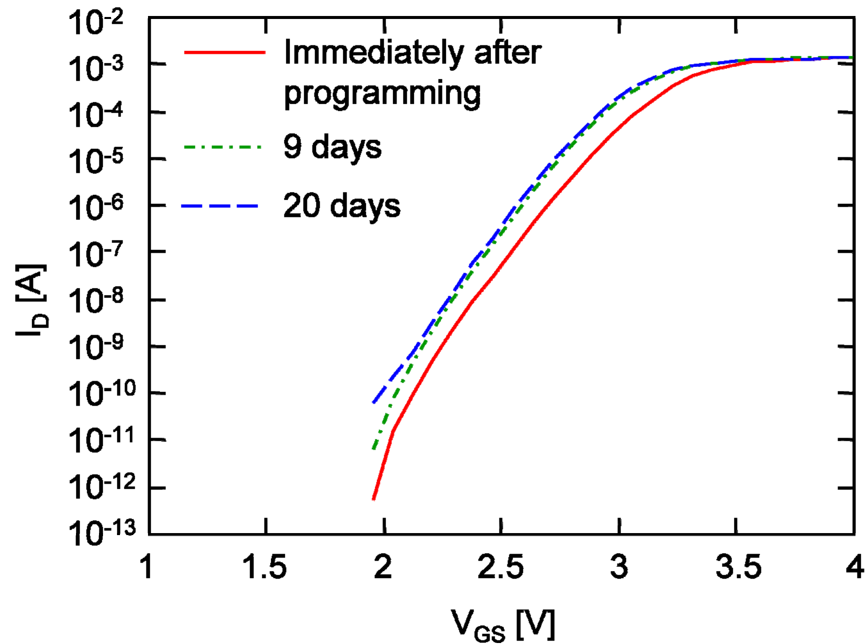

Fig. 6.7. I_D-V_{GS} curves in subthreshold region measured immediately after programming, 9 days after programming and 20 days after programming in a CAST irradiated with $3.3{\cdot}10^8$ ions/cm^2

The threshold voltage shift in this region is due to the charge lost from nanocrystals, due to the tunneling current and/or the gate excess current due to the weak spots generated by irradiation (see Fig. 6.1). In a fresh device the threshold voltage decreases by -25mV/time decade, starting from the value read at 1000s. This means that in time as long as 10 years ($3{\cdot}10^8$s) the threshold voltage should shift by –140mV (corresponding

to 0.5 electrons lost for each nanocrystal on average). Irradiated devices lose charge from nanocrystals at a faster rate (–40 mV/dec); comparing irradiated devices to each other we cannot identify any clear trend as a function of the ion type or ion fluence, likely due to the sensitivity limits imposed by CAST structure. Again, we must take into account that the threshold voltage has been evaluated from the shift of the drain current measured in subthreshold region, at a fixed current, and in the programmed state, the threshold voltage shift is dominated by the first cells turning-on. This means that in an irradiated CAST the weaker cells are the most responsible for the threshold voltage shift. We can argue that these cells might be the most damaged, e.g., those ones receiving a multiple ion hit or those cells which experience the largest increase of the gate leakage (see Fig. 6.1). Random fluctuations on threshold voltage occurring even between two consecutive measurements of the same CAST or of the same single cell add to the small variation observed, making more difficult to extrapolate the actual trend. Nonetheless, it is worth to remark again that the I_D-V_{GS} curves of Fig. 6.7, taken immediately, after 9 days, and 20 days after programming, keep parallel to each other in the subthreshold region, showing only a rigid shift toward negative voltages, due to the discharge of some nanocrystals. Again the rigid shift of the CAST characteristics is a clear signature that the majority of the hit cells are shifting leftward. From the simulation (Fig. 6.5) we calculated that if the number of damaged cells is in the order of 50000, and the actual threshold voltage variation of each cell should be 350mV. The absence of the kink in the CAST characteristics, confirms that no cell has lost most of its charge.

Now, a question arises: why the estimated cell threshold voltage variation after the retention experiments is limited to 350mV, despite the very large gate leakage of some samples? For instance, the floating gate capacitance of a memory cell is in the range of 1fF: a 100-pA leakage current should completely discharge it in few tens of μs. For converse, in Fig. 6.2, we do observe no substantial differences between irradiated and fresh devices, and no variation occurred in the subthreshold slope in Fig. 6.7, indicating that no critical charge loss occurred in the irradiated CAST cells upon retention test. This confirms that the steady state current is much localized, hence only few nanocrystals are actually discharged, while the majority of nanocrystals retain the stored charge. In addition, this also indicates that, even though one or few nanocrystals are completely discharged, the tunneling between neighboring nanocrystals is avoided or limited due to the uniform distribution of the nanocrystals within the cell.

We may wonder now how many NCs should be discharged to produce the threshold voltage shift shown in Fig. 6.6. In principle if an ion hit affects one nanocrystal at most, we should not expect to observe any appreciable change in the retention time characteristics, against the experimental evidence. Hence, it must be present some other damage mechanism that can affect also those regions of the cell, which are not directly hit. In fact, a single ion generates a dense electron/hole track with small radius. Holes surviving recombination diffuse and eventually generate oxide defects in a much wider

region than the initial track size. In a previous work [167] the size of this Physically Damaged Region (PDR), was reported to range from 0.2 μm to 1μm, i.e., as large as (or even larger than) the single cell size. However, this value is too large, probably due to the different technology of [167] and to the limitations of the CAST structure, which does not allow the extrapolation of the single cell characteristics. The experimental results performed on addressable arrays (see section 6.3) indeed indicate that that each ion should affect an area of about 100nm, as it will be also confirmed by the charge loss modeling discussed in section 6.4.

At this point some considerations are worth about the discharge rate of the nanocrystals mediated by defects in the tunnel oxide. If one defect is generated below a nanocrystal in the middle of the tunneling oxide (namely at 2.5nm from both interfaces), we may expect a fast NC discharge (occurring in seconds or less). Instead, if a trap is generated near the NC interface or in between two NCs, it should behave as a border trap [168] being 4-5 nm far from the substrate/oxide interface. Such trap may quickly capture electrons from the nanocrystals only if they lie close to them. However, they always exchange electrons with the substrate over times as long as several hours [169]. If we were dealing with a floating gate cell, each trap generated by irradiation in the middle of the tunnel oxide should contribute to discharge the monolithic floating gate, regardless its position over the gate area. For converse, in a NCM cell, the overall nanocrystal area is only 15% of the total gate area and only a small percentage of the traps generated by the impinging ion should be close enough to a nanocrystal, to be effective in discharging its stored charge. This qualitatively explains why the discharge rate of the irradiated devices is less than twice that of the fresh cells.

Despite the experimental limits intrinsic to the CAST structure, we may argue that irradiated NCMs have the potential capability to retain the stored data after 10 years, with only 250-mV decrease of the CAST threshold voltage, deriving from a 350-mV threshold voltage variation of the hit cells and a 160-mV threshold voltage variation affecting the fresh cells.

6.3 Heavy Ion effects on addressable arrays

In the previous section, we analyzed the heavy ion effects on CASTs. Those analyses proved useful to estimate the impact of ionizing radiation from some reliability aspects. In particular, CAST structures showed an increased gate leakage, and accelerated breakdown on irradiated devices. Furthermore, CAST allowed us to give the first indirect estimations on the effects of the heavy ions on the prompt charge loss and on the retention after irradiation. However, with CAST an accurate and precise estimation cannot be performed, because the evaluation of the threshold voltage of each cell cannot be performed.

In this section, we will focus on the effects of addressable arrays. In particular, we analyze the prompt charge loss, the programmability and the retention after irradiation.

Unfortunately, addressable arrays cannot be used to evaluate any increased gate leakage, which must still be performed using CASTs or single cells.

6.3.1 Experimental setup

Unlike CASTs and single cells, the nanocrystals of an erased cell store an almost neutral charge in the addressable array as it will be clear in the following section. This is achieved by the smart algorithm adopted by the programming circuitry. On the contrary, the CAST do not feature any threshold voltage controlled program/erase operations. On the other hand, these arrays are arranged in NOR configuration, hence the threshold voltage of each cell must be strictly positive, and no negative charge should be stored.

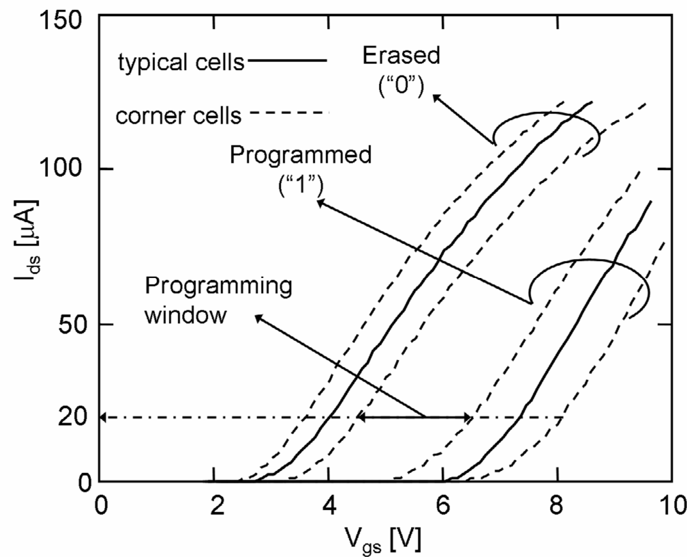

Fig. 6.8. Drain current-gate voltage (I_D-V_{GS}) characteristics for a typical and corner cells of the nanocrystal memory addressable arrays.

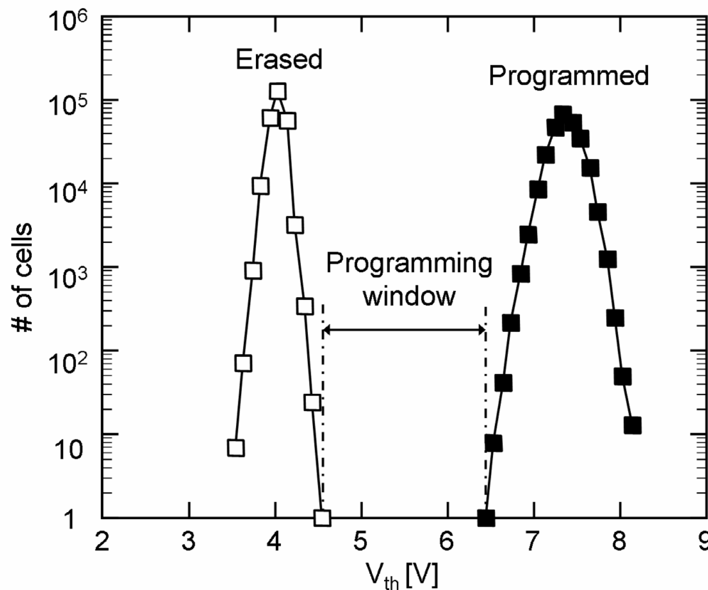

Fig. 6.9. Threshold voltage distributions of a NCM array, programmed with a checkerboard pattern.

The programming has been performed by Channel Initiated Secondary Electron (CHISEL), by applying V_{GS} = 7.5V, V_{DS} = 4.5V, and keeping the substrate at V_{BS} = -

1.2V. Erasure has been performed by Fowler-Nordheim injection from the nanocrystal layer to the substrate. Fig. 6.8, shows the I_D-V_{GS} curves (at V_{DS} = 0.8V) for both programmed and erased devices. The solid lines represent the typical cells. The dashed lines represent the corner cells, i.e., those ones corresponding to the minimum and maximum threshold voltage values. The deviation from the typical behavior mainly derives from the process parameter dispersion, the local variation of the nanocrystal density and the position of the cell within the array, which differently impacts on the cell parasitics. The cell threshold voltage has been calculated as the V_{GS} voltage required for achieve a drain current I_{ds} = 20μA (at V_{DS} = 0.8V).

Fig. 6.9 shows a typical threshold voltage distribution of a sample with one half of the cell at “1” and the other at “0”. The programmed threshold voltage ranges between 6.4V and 8.1V, the erased V_{TH} is within 3.5V and 4.6V. Hereafter, we refer to the programming window as the difference between the minimum of the programmed threshold voltage distribution and the maximum of the erased threshold voltage distribution (see Fig. 6.9). All the tested devices have characteristics similar to that shown in Fig. 6.9, with only marginal variations (less then 50mV).

Irradiation has been performed at the SIRAD facility of the Tandem Van de Graaff accelerator at the INFN – Laboratori Nazionali di Legnaro, Italy [159]. The samples were irradiated with Br ions (E = 241 MeV, LET = 38.6 $MeV \cdot cm^2 \cdot mg^{-1}$) at wafer level.

In the followings we refer as “programmed” (“1”) to a cell with high threshold voltage, i.e., when nanocrystals store negative charges, while we refer as “erased” (“0”) to a cell with low threshold voltage.

Before irradiation, each nanocrystal memory array was programmed with a checkerboard pattern, so that “0” and “1” logic values are uniformly distributed all over the array, minimizing any possible ion beam non-uniformity effect. Before and after irradiation we measured the threshold voltage distribution of the whole array, and the I_{ds}-V_{gs} curves. All the arrays were irradiated with the same ion fluence of $5 \cdot 10^8$ Br ions/cm^2. With this ion fluence, namely, 30% of the cells should be hit by one ion. Still, we expected that several cells may experience multiple hits with such high ion fluence. We theoretically estimate that only 25.92% of the cells are actually hit by at least one ion, while the remaining 74.08% of cells are not hit. In addition, the actual probabilities of single, double, and triple hits are 22.22%, 3.33%, and 0.333%, respectively. The details of the theoretical calculation of the ion hit probability are shown in the Appendix B.

Table 6 summarizes the probability of the single and multiple hits. The second column of the table reports the average number of cells hit by a given number of ions. That number is normalized to 256k cells, which is the total amount of cells storing a given logical value (“1” or “0”) in the checkerboard pattern. The corresponding percentage among the array is shown in the third column. The last column shows the

cumulative probability, i.e. the percentage of the cells that experienced at least the number of hits reported in first column.

Number of Hits	Number of cells (over 256 kbit)	Probability	Cumulative Probability
0	194200	74.08 %	100%
1	58261	22.22 %	25.92%
2	8739	3.33 %	3.69%
3	874	0.333 %	0.360%
4	65	$2.5 \cdot 10^{-2}$ %	$2.56 \cdot 10^{-2}$ %
5	4	$1.5 \cdot 10^{-3}$ %	$1.91 \cdot 10^{-3}$ %

Table 6. Percentage of cell receiving a single or multiple ion hit at a fluence of $5 \cdot 10^8$ ions/cm^2

6.3.2 Charge Loss Immediately after Irradiation

In Fig. 6.10a, we show the threshold voltage distribution of an array programmed with checkerboard pattern and irradiated with $5 \cdot 10^8$ Br ions/cm^2, after any transient charge/discharge of interface states have occurred. Fig. 6.10b shows the I_D-V_{GS} curves taken on three examples of NCM cells, which feature an appreciable threshold voltage shift of 1.03V (cell A), 1.12V (cell B), and 1.54V (cell C). The shadowed regions in the plot represent the dispersion of the I_D-V_{GS} characteristics of the fresh array, as reference. Fig. 6.11 shows the same cumulative distribution of Fig. 6.10a as a Weibull plot. Remarkably, the high-V_{TH} distribution (programmed threshold voltages) features a tail corresponding to a fraction of hit cells, which are only partially discharged by the impinging ions. In fact, this tail is small enough to avoid the complete closure of the programming window, which reduces from 1.85V to 0.85V. By calculating the cumulative distribution of the tail cells, we estimate that only 0.3% of the cells within the array feature this large threshold voltage shift.

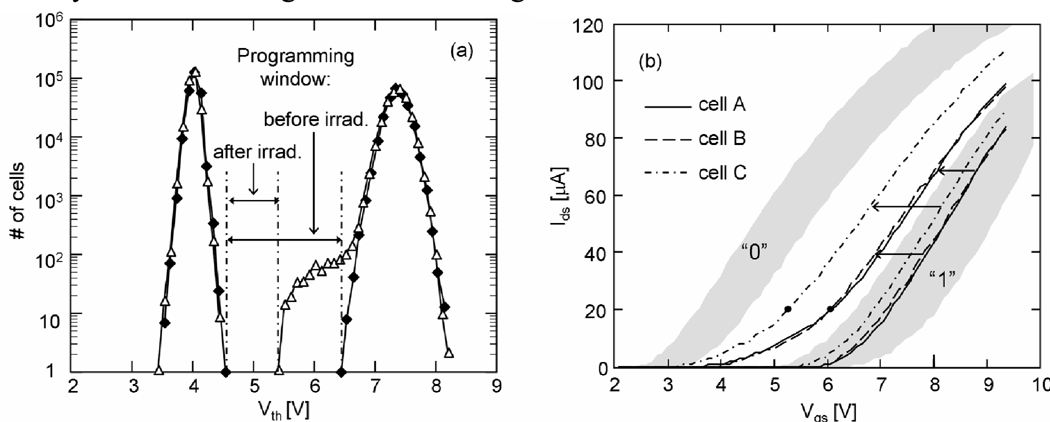

Fig. 6.10. a) Threshold voltage distributions of a NCM array, programmed with a checkerboard pattern before and after irradiation with $5 \cdot 10^8$ Br ions/cm^2. b) I_{ds}-V_{gs} curves of 3 hit cells, which feature a negative shift of the threshold voltage due to the prompt charge loss during irradiation. The gray regions represent the spread of the I_{ds}-V_{gs} curves within the fresh cell-array.

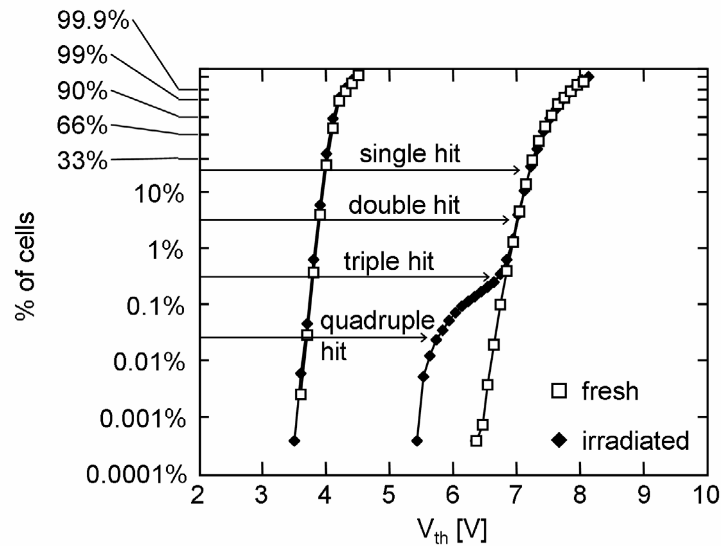

Fig. 6.11. Cumulative threshold voltage distributions of the same NCM array of Fig. 6.10 before and after irradiation with $5{\cdot}10^8$ Br ions/cm^2. In the same plot we show four markers corresponding to the probability of a single, double, triple, and quadruple hit (the probability values are taken from the last column of Table 6).

Taking into account that theoretically 25.92% of the cells are hit by at least one ion, we conclude that the majority of ions, which hit a single NCM cells, is unable to produce a noticeable threshold voltage shift. In fact, the tail of Fig. 6.11 is below 0.35%, indicating that at most 1.4% of the hit cells exhibit a large charge loss. In fact, by comparing the probability of single and multiple ion hits with the threshold voltage statistic shifts discussed above (see markers in Fig. 6.11), we can correlate the number of total cells belonging to the tail in Fig. 6.10 and 5 (0.35%) to the cells that experienced at least a triple hit (0.36%). Furthermore, we calculated that less than ten cells show a threshold voltage smaller than one half of the programming windows after irradiation. Such cells are likely correlated to the number of quadruple or quintuple hits. These data clearly show two important results. Firstly, a single ion hit is unable to affect the cell threshold voltage and at least a triple hit is needed to appreciably shift the cell threshold voltage, in contrast to that observed in floating gate memories, where almost all struck cells lose a substantial part of the FG stored charge if hit by a high LET ion [118],[122],[127],[129],[131],[166]. For instance, in case of Br ions most of the FG charge is lost. Secondly, even in a triple-hit cells, the stored charge is only partially lost.

As a last remark, we never observed any tail cells in the erased distribution. This could be explained by considering that in these samples the nanocrystals are almost neutral in the erased state, and a single ion hit is not effective in producing either interface/border traps or fixed trapped charge in these relatively thin oxides.

6.3.3 Programmability and retention properties of irradiated cells

In order to assess if any permanent damage other than the immediate charge loss remains after irradiation, we repeated the programming operation, restoring the original checkerboard-pattern of the NCM arrays. Fig. 6.12 shows the threshold voltage of a NCM array, immediately after programming, and 20 days after programming.

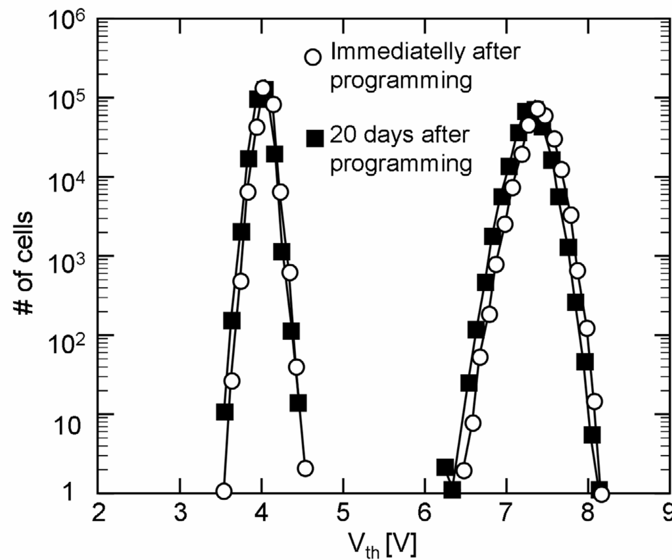

Fig. 6.12. Threshold voltage distributions of a NCM array, irradiated with $5{\cdot}10^8$ Br ions/cm^2 and reprogrammed with the checkerboard pattern (open symbols). The filled symbols are the threshold voltage distributions measured after 20-days retention experiment

The tail of cells completely disappears after reprogramming, indicating that the threshold voltage shift is actually due to a partial charge loss. After programming, we left the arrays unbiased and we again measured the threshold voltage distribution and the I_D-V_{GS} characteristics after 20 days. The tail of the hit cells does not appear anymore, indicating that any possible leakage path across the tunnel or control dielectrics produced by the ion hit is ineffective in discharging a noticeable amount of charge, as is observed in a floating gate cell after high-LET ion irradiation.

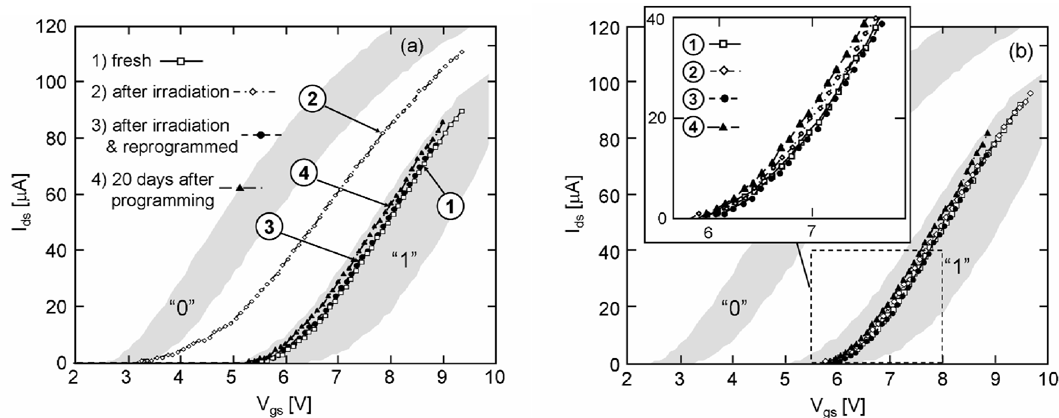

Fig. 6.13. a) Evolution of a ion multiple-hit cell before irradiation (cell C of Fig. 6.10), after irradiation, after programming and 20 days after programming. b) evolution of a cell from the same irradiated array, which does not show any threshold voltage variation after irradiation, after programming and 20 days after programming. (Curves marked with the same symbol, same line pattern and same marker refer to the same irradiation and/or programming conditions)

Furthermore, the plot of Fig. 6.13 shows the behavior of one failing cell after irradiation. We see a large threshold voltage shift after irradiation, but after reprogramming the cell the nanocrystal charge is restored. Only a small V_{TH}-shift (less than 80mV) occurs after 20 days, which is comparable with the average shift of all the other cells and within the experimental resolution of our equipment.

6.3.4 Discussions

When considering the heavy ion radiation effects on non-volatile memory, the most important issues are the prompt charge loss after irradiation and the long term data retention characteristics. The onset of oxide leakage current is strictly correlated with the second issue, since it may produce an abnormal and premature charge loss even in short time after programming. [129].

Concerning the first issue, the data shown in Fig. 6.9 and Fig. 6.11 indicate that only a moderate charge loss occurred in a small percentage of hit cells. The programming window decreases after irradiation, but the charge stored in nanocrystals is not completely neutralized even after several thousands of cells experienced a multiple hit (see Table 6 and markers in Fig. 6.11).

As already discussed in chapter 3, there are several contributions to the prompt charge loss, due to irradiation in conventional floating gate memories:

1) Transient currents flowing from/to the floating gate.

2) the recombination of the floating gate charge with the holes generated in the control and tunnel dielectrics by the ionizing radiation

3) the electron photoemission from the floating gate (nanocrystals)[19].

The first mechanism is considered [124],[119] as the most critical for the floating gate memories irradiated with heavy ions. However, there is a strong debate about its origin: a transient conductive path [124], or a transient current due to injected carriers generated in the surrounding silicon electrodes [119].

Accordingly to its proposing authors, the effects of the transient conductive path should be limited to a radius of 4nm [122]- [124]. However, if TCP really existed, it should have a very limited effect on those devices adopting a discrete storage approach, such as in NCM. In fact, only those nanocrystals within the ion track may be (partially) discharged. Because any transient conductive path is ineffective in discharging many or all the nanocrystals, the origin of the tail cannot definitely be ascribed to TCP. Hence, either contributions 2 and 3 have a strong impact, or the origins of the transient currents are different from TCP. Nonetheless, both the second and the third mechanisms are still localized within a relatively small region surrounding the ion track (i.e., where electron-hole pairs are generated), involving only a small percentage of nanocrystals. The reduction of the tunnel oxide thickness with respect to floating gate flash memories (5 nm vs. 8-10 nm in conventional flash) results also in a smaller quantity of charge produced by radiation in the oxide that can neutralize the stored charge.

[19] In the literature, the word “photoemission” is typically associated with the photoexcitation and consequent ejection of the excess stored charge of the floating gate. Indeed, photoemission could also occur from the silicon substrate or from the polysilicon control gate, which, in turn, may lead to transient currents.

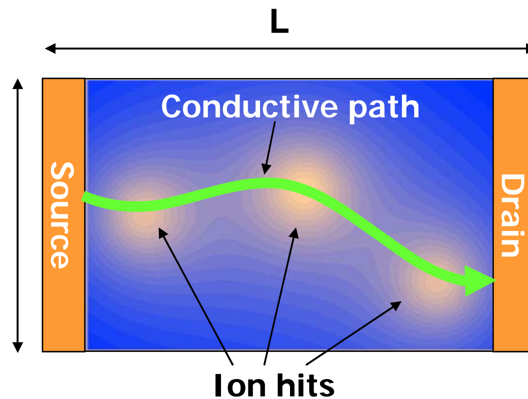

Fig. 6.14. Schematic representation of the conductive path along the channel due to a triple ion hit. The bright regions represent the ion impact area, where nanocrystals are partially discharged, permitting the channel formation at V_{gs} lower than in the remaining part of the channel.

Hence, (as it will be discussed more in detail in paragraph 6.4.5) the observed tail might be induced by transient currents of hot electrons and holes generated in the control gate or in the substrate, and then injected in the nanocrystals. In fact, in order to achieve an appreciable drain current, a conductive path must be formed along the MOSFET channel from source to drain. Therefore, to read a premature cell-turn-on a large amount of nanocrystals must lose part of their charge. We may figure out that each ion hit partially discharges the nanocrystals within its track, projecting over the channel a spot, where the threshold voltage is locally decreased. These spots of (partially) discharged nanocrystals should be distributed along the channel forming a conductive path from source to drain, as schematically depicted in Fig. 6.14. The light yellow regions represent the ion-hit area, where the nanocrystals are partially discharged, locally decreasing the threshold voltage and permitting the premature channel formation. As the channel is 300-nm long, the size of the area affected by each ion hit cannot exceed 100nm-150nm, which is comparable with the interface physically damaged region observed in MOSFETs after heavy ions irradiation [167]. This may explain why a single ion hit is unable to produce the large threshold voltage variation over many nanocrystals, required for premature turn-on the cell. Remarkably recent simulations [128] showed that in silicon (and polysilicon) a single ion hit generates a dense carrier track (>10^{18}cm^{-3}) over a size as large as 100nm, in agreement with our estimation. This suggests that the origin of the charge loss from nanocrystals is the electron-hole pairs ionized in the silicon substrate (and polysilicon gate), which may be in turn injected through the tunnel (and control) dielectric. This is also in agreements with the modeling and simulation presented by [119], which presented a very solid model from the physical viewpoint.

By comparing these data with those reported in literature on the conventional floating gate memories [154],[120]-[122],[127],[130],[131],[166], the threshold voltage shift of a floating gate MOSFET may approach 3-4V after heavy ion irradiation, often leading to the complete closure of the programming window. In addition very large bit-flip probability values have been often observed, close to several tens per cent of the hit

cells up to almost 100% of the hit cells. For comparison, in Fig. 6.15, we report the results presented on [129], which feature almost the same size of our samples. Based on the data published by the authors, we estimated the probability of single and double hits, which are shown in Fig. 6.15 (see blue arrows). The results show that, not only each ion induces a very large threshold voltage variation, but also each ion may produce some threshold voltage shifts in the neighboring cells. This happens even for nickel ions, which feature a smaller LET than bromine ions, used in our irradiations (29.3 vs 38.6 MeV·cm^2·mg^{-1}). Still, we cannot exclude that some experimental errors on the estimated fluence may come into play. Nonetheless, this must be compared with the results of Fig. 6.11, where at least a triple hit is needed to see an appreciable threshold voltage variation.

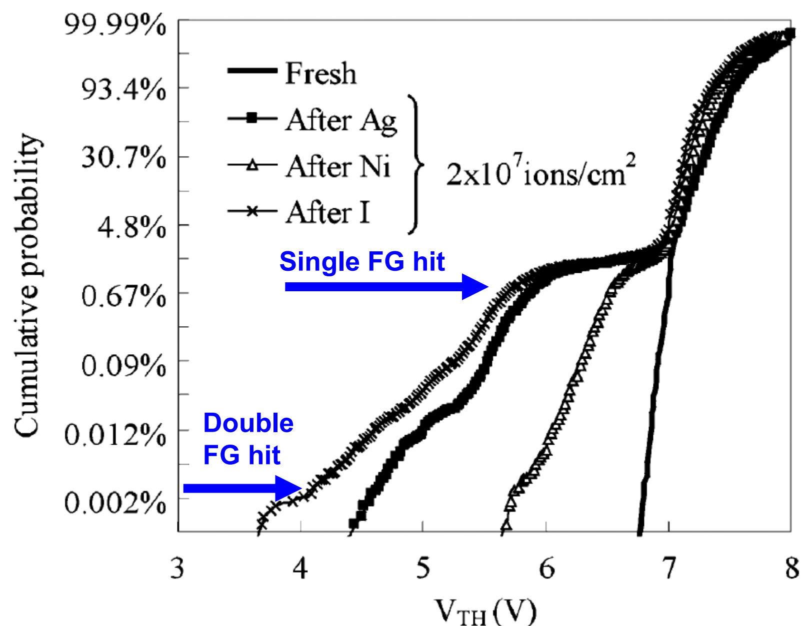

Fig. 6.15. Cumulative distributions of floating gate memory cell array before and after irradiation with Ni, Ag, and I. Fluence = 2·10^7 ions/cm^2 (corresponding to 0.8% of nominally hit FGs), LET = 29.3 MeV·cm^2·mg^{-1} (Ni); 57.3 MeV·cm^2·mg^{-1} (Ag); 64.2 MeV·cm^2·mg^{-1} (I). The two arrows have been added to indicate the probability of a single and a double ion hit, using the model presented in the Appendix B [129]. These flash memory cells have similar sizes of the nanocrystal memory cells used in this chapter.

Coming to the second problem, moving from a floating gate MOSFET typical of contemporary flash memories, with a relatively thick tunnel oxide (8-10nm), to the novel nanocrystal technology, with thinner gate oxide (4-5nm), the oxide leakage currents (both the tunnel and the control oxides) should become an even bigger issue, at least in principle. In fact, all the radiation-induced oxide leakage currents quickly increase as the oxide thickness is reduced below 6 nm [103]. These currents are either Radiation Induced Leakage Current (RILC) [104],[103], Radiation Soft Breakdown (RSB)[99],[100], accelerated breakdown or wear-out [162]-[164].

Unfortunately, the test chip used in this section does not permit direct measurement of the gate current of each cell. Nonetheless, in the previous section (see 6.2), we

studied the heavy ion irradiation effects on the same nanocrystal technology, by means of simpler structures consisting of array of cells in parallel connection (the CAST). Each cell featured the same sizes, structure, and fabrication process as those of the present section and we have reported of a 100-pA steady state leakage current after I ion irradiation, which reveals similarity with that shown by Candelori et al. in [161]. We attributed this oxide leakage to a multi-trap-assisted conduction through a defect cluster generated along overlapping ion tracks across the overall dielectric stack (12 nm + 5 nm thick = 17 nm thick). Such large leakage current can easily discharge the floating gate capacitance of a conventional flash cell in times as short as few tens of microseconds. For converse, in Fig. 6.12 and Fig. 6.13, programming the NCM array after irradiation we do not observe any tail of failing cells due to the discharging of the nanocrystal layer.

Still, 20 days after programming, the programmed threshold voltage distribution is slightly translated toward negative voltages, due to the intrinsic discharging of the interface states and nanocrystals, present even in the fresh devices, which is smaller than 80mV. The tail observed immediately after irradiation (see Fig. 6.10), does not appear anymore, indicating that no critical charge loss occurs in the irradiated cells upon retention test. This also indicates that, even though the size of the discharged nanocrystal region may be as large as 100nm, the size of the weak spot generated by the impinging ion across the oxide (if any) must be much smaller than the distance among neighbor nanocrystals, which is in the range of 10-15nm. Hence, any radiation-induced oxide conductive path may discharge very few nanocrystals, preserving the programmability and the retention properties of the NCM cell.

Clearly, the improved robustness of NCM to heavy ion irradiation derives from the discrete storage technique, limiting the transient effect of a single ion and the impact of the radiation induced steady state leakage currents expected across the thin tunnel oxide.

6.4 Modeling of Heavy Ion Induced Charge Loss Mechanisms

The previous results on CAST and addressable arrays, showed that, even after several ion hits, the nanocrystal memory cell can still be reprogrammed, without appreciable degradation on the programmability and, unlike conventional floating gate based Flash devices (compare Fig. 6.6 and Fig. 3.7a), NCMs are still capable to retain the stored data, after 20 days. The most important residual heavy ion effect is therefore the prompt charge loss, induced by the heavy ion strike. Unlike conventional FGM, the NCM store the charge in a layer of discrete and insulated nanodots; hence, when an ion impinges on the NCM, the charge do not redistributes in the storage medium. Hence, the threshold voltage is strongly correlated not only to the number of ion hits, but also to the hit positions. In order to establish the effects of the ion hit, a pseudo 3D model must be developed.

In this section we show the model of the charge loss. This model is very flexible, because it can be used with arbitrary nanocrystal distribution and non uniform

nanocrystal charge. It also provides a fine estimation of the ion track size, which well correlates with other simulations, experimental results and indirect measurements [119],[121],[127],[128], performed on other kind of devices. The model can be also adopted for other kind of localized degradation phenomena, and for all those memories implementing the discrete storage approach (SONOS, etc.). The presented data are validated with the experimental results from a microbeam heavy-ion irradiation. The microbeam irradiation allows to precisely control the position and the size of the irradiated area. In this way, the fluence levels can be increased, to evaluate the effects of multiple ion-hits, without damaging the peripheral circuitry, which is not irradiated.

6.4.1 Experimental setups

The irradiation experiments were performed at the Sandia National Laboratories (Albuquerque, NM) using a focused Cu ion beam (surface LET = 33.5 MeV·cm^2·mg^{-1}, energy = 50 MeV). The devices were irradiated unbiased.

Using the same terminology of the previous sections, we refer to “programmed cells” as those cells that have high threshold voltages, while we refer to “erased cells” as those cells that have low threshold voltages. In each array, one half of cells were programmed and one half were erased before irradiation with a checkerboard pattern. The ion beam was focused into a 1-µm^2 spot and was scanned over an area as small as 177 µm × 178 µm, which was smaller than the sector area. As schematically depicted in Fig. 6.16, the irradiation area lies completely within a single sector. Hence, only the memory cell array was irradiated, permitting us to irradiate to very high fluence levels without damaging the peripheral circuitry, which is not irradiated. The eight sectors making up the blocks were irradiated with the same fluence and irradiation area, such that 58.6% of each sector was irradiated.

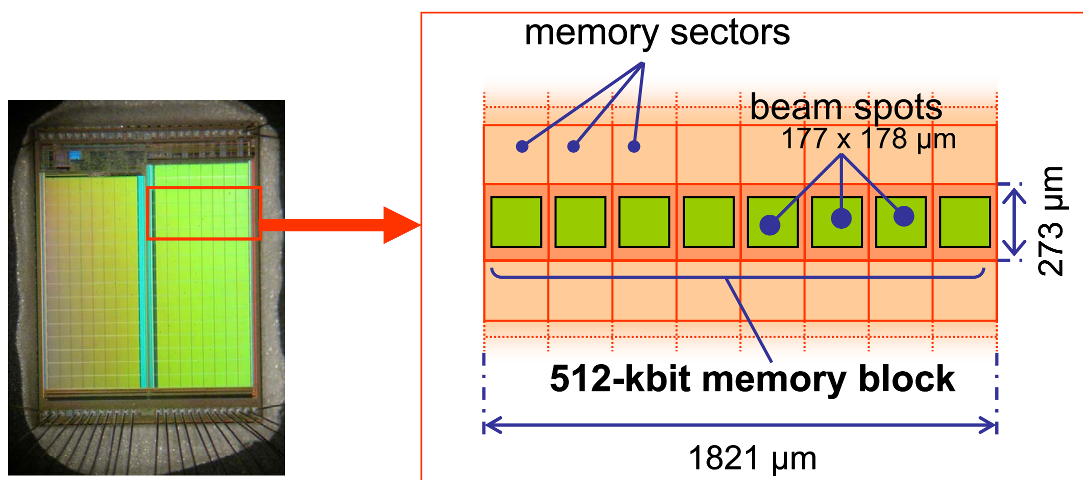

Fig. 6.16. Schematic layout representing the memory organization. The ion beam was focused only in the dark green squares, in order to irradiate only the cell array, and to avoid any radiation damage to the peripheral circuitry.

6.4.2 Experimental Results

In Fig. 6.17, we show the threshold voltage distribution before and after irradiation with $1.67 \cdot 10^9$ Cu ions/cm^2. We chose the ion fluence such that 100% of cells should have statistically received one ion hit within the irradiated area.

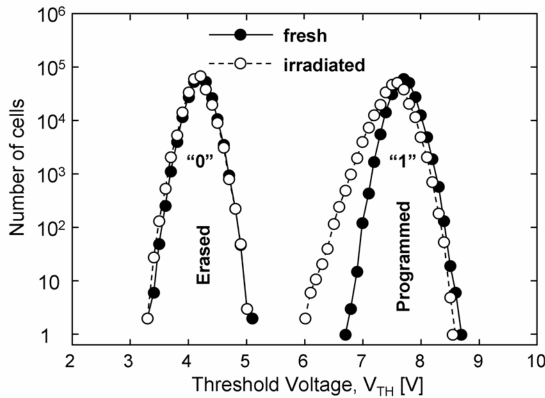

Fig. 6.17. Threshold voltage distributions of a NCM array, programmed with a checkerboard pattern before and after irradiation with $1.67 \cdot 10^9$ Cu ions/cm^2. The threshold voltage has been defined as the gate voltage required by the cell for driving a drain current I_{DS}= 20µA (at V_{DS} = 0.8V).

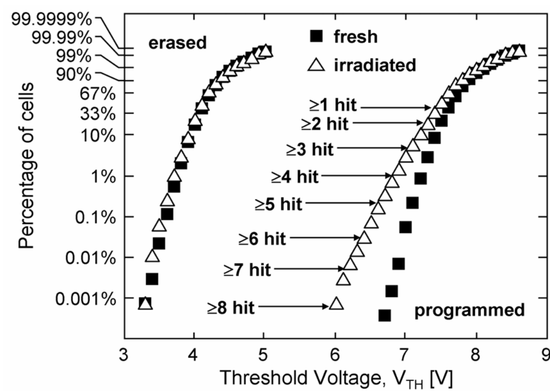

Fig. 6.18. Cumulative threshold voltage distributions of the same NCM array of Fig. 6.17 before and after irradiation with $1.67 \cdot 10^9$ Cu ions/cm^2. In the same plot, we show eight markers corresponding to the probability of a single, and multiple hits.

The heavy ion exposure has negligible effects on the erased cells, because the stored charge is almost neutral, as already discussed before. On the contrary, the programmed cell distribution features a large tail after irradiation, as can be seen in the cumulative probability distribution in Fig. 6.18. Like in Fig. 6.11, the eight arrows in Fig. 6.18 represent the cumulative probability that at least 1, 2, 3, …, 8 ions will hit a single cell. This calculation has been performed using the calculation shown in the Appendix B, and it takes into account the fact that only a fraction of the sector was effectively irradiated (58.6%). The shift between the fresh and irradiated device curves in Fig. 6.18 is 18mV for a probability of 1 hit, 0.3V for 3 hits, and increases up to 0.72V for 8 hits.

As already shown before, a single ion hit cannot produce a substantial threshold voltage variation. Even though some cells may have experienced up to 8 hits, the programmed cell distribution does not overlap the erased cell distribution. As discussed before, the origin of such a tail is the prompt charge loss due to several mechanisms: the photoemission and the recombination with the charge generated in the oxide within the ion track.

6.4.3 Modeling and Simulations

The purpose of this model is to simulate the variation of the array threshold voltage distribution after heavy ion irradiation, given the nominal ion fluence. This task is relatively simple in floating gate memory cells, because the threshold voltage shift induced by an ion strike correlates only with the amount of charge loss, independent of the hit position along the channel. In fact, the highly doped floating gate behaves like a metal plate and the remaining charge redistributes after the ion hit. Instead, in a NCM

cell each ion hit discharges only the neighboring NCs, and the stored charge does not redistribute. Consequently, the threshold voltage changes locally only around the hit position. To appreciably reduce the threshold voltage, the damage region induced by subsequent ion strikes must be contiguous along the path of the channel, and they must form a percolation path from the source to the drain.

In the following, we summarize our model in two steps. First, we consider the NCM cell electrostatics, which permits us to simulate the I_D-V_{GS} characteristics with arbitrary NC charge and spatial distributions. Second, a statistical-based simulation is used to account for the ion hit effects.

6.4.3.1 Channel electrostatics and conduction modeling

Our electrostatic model is based on the following assumptions (see Fig. 6.17 for notations):

A1) The gate and the strongly inverted channel are approximated as two infinite metallic sheets. This is a good approximation for all NCs in the center of the channel. Even though it is less accurate for the NCs on the channel edges, we verified that the edge-NCs have a minor impact on the whole channel conductance. In fact, the NC induced oxide electric field at r = 15nm (which is the average mutual distance among NCs) is less than the 10% of the oxide field at $r = 0$.

A2) Each charged NC is approximated as a point charge.

A3) The normal component of the electric field (E_{ox}) is much larger than the longitudinal component ($\boldsymbol{E_L}$).

From A1, the polysilicon gate and the strongly inverted channel act as two metal plates. Therefore, we studied a linear system of charges and conductors and we adopted the method of the superposition of the effects to evaluate the normal electric field (E_{ox}) over the channel area. Using the image charge method, we evaluated the electric field at the substrate-oxide interface induced by a single NC with a single elementary negative charge. This is calculated as a sum of infinite terms of image charges, corresponding to infinite reflections of the nanocrystal charge at the two plates. The infinite reflections produce a series of electric dipoles (+q, –q), periodically repeated along the z-axis (as shown in Fig. 6.17b). The displacement of each dipole is $2t_1$ and they are located at the coordinates:

$$z_n = 2 \cdot n \cdot (t_1 + t_2) \quad n = 0, \pm 1, \pm 2, \ldots \pm \infty$$

The normal electric field, induced by a single electron stored in a nanocrystal, is given by the summation:

$$E_{ox}^{NC}\left(r\right)=\frac{-q}{4\pi\varepsilon_{ox}}\sum_{n=-\infty}^{+\infty}\left\{\frac{\left(z_n+t_1\right)}{\left[\left(z_n+t_1\right)^2+r^2\right]^{3/2}}-\frac{\left(z_n-t_1\right)}{\left[\left(z_n-t_1\right)^2+r^2\right]^{3/2}}\right\}$$

The explanation of each symbol of the previous equation is given in Fig. 6.17.

We limited the number of terms of the sum according to the desired precision (we chose 10^{-4} %). Despite its simplicity, the results of our electrostatic model, combined with the heavy ion modeling (see subparagraph 6.4.3.2), are in excellent agreement with the experimental data. In addition, because of the assumptions, the NC-induced electric field has to be calculated only one time, shortening the simulation time. Once the position and the stored charge amount is know, the total normal electric field E_{ox} at the position $\left(x, y\right)$ can be simply calculated as the sum of all the contributions induced by the stored charges.

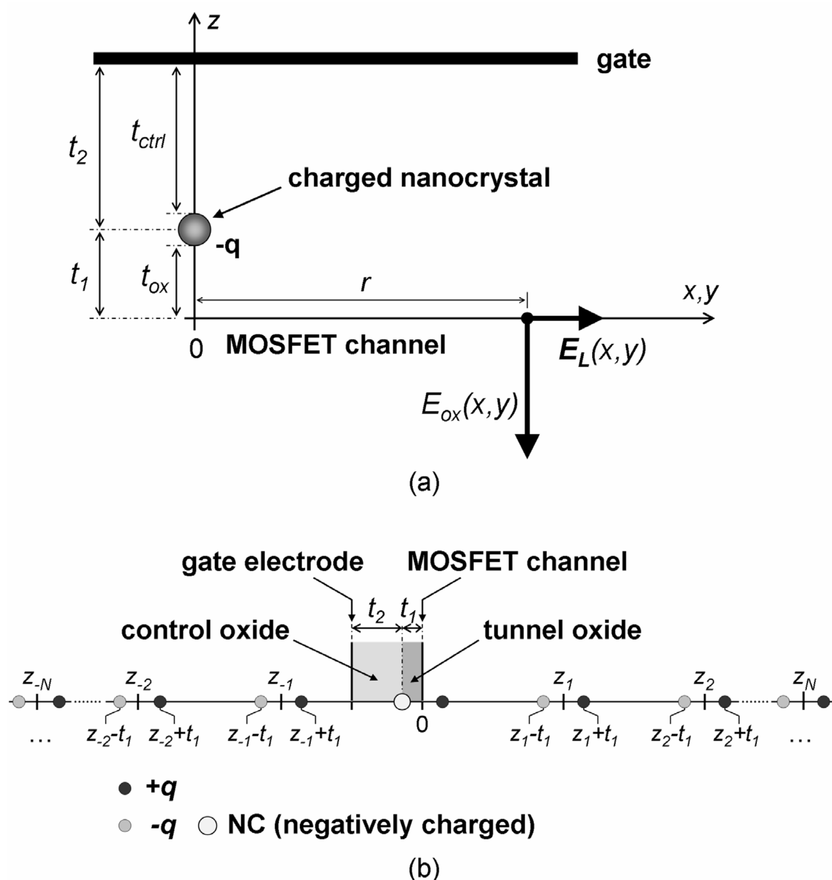

Fig. 6.19. Nanocrystal electrostatic model and notations: a) axis notation and orientation; the MOSFET channel and gate are parallel to the x-y plane. *r* is the distance of the point (x,y) from the axis origin along the channel plane. t_1 and t_2 are the NC distance from the channel and gate, respectively. The electrical field along the channel consists of the transverse (E_{ox}) and longitudinal component (E_L). b) Representation of the image charge reflections of the NC charge on the gate and channel plates along the z-axis.

After the normal electric field E_{ox} is calculated at the position (x, y) along the channel, we evaluate the local carrier density per unit of area $n_S(x, y)$ and the local channel conductance $\sigma_S(x, y)$ per unit of area:

$$\sigma_S(x,y) = \mu \cdot q \cdot n_S(x,y) = \mu \cdot \varepsilon_{ox} E_{ox}(x,y)$$

μ is the electron mobility; ε_{ox} is the oxide dielectric permittivity; and q is the elementary charge.

From A3, the longitudinal component of the channel electric field $\mathbf{E_L}$ can be calculated by Ohm's law, in the x-y plane, neglecting the effect of $\mathbf{E_L}$ on the free carrier density:

$$\mathbf{J}(x,y) = \sigma(x,y)\mathbf{E}_\mathrm{L}(x,y) = -\sigma(x,y)\,grad\left[V(x,y)\right]$$

where $V(x, y)$ is the local potential at the oxide-channel interface (z = 0).

By imposing charge conservation we obtain:

$$div(\mathbf{J}) = -div\left[\sigma grad(V)\right] = 0$$

$$\frac{\partial \sigma}{\partial x}\frac{\partial V}{\partial x} + \frac{\partial \sigma}{\partial y}\frac{\partial V}{\partial y} + \sigma\left(\frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2}\right) = 0$$

The solution of this system has been numerically calculated over a mesh grid with 1-nm width, which is a good tradeoff between simulation speed and precision.

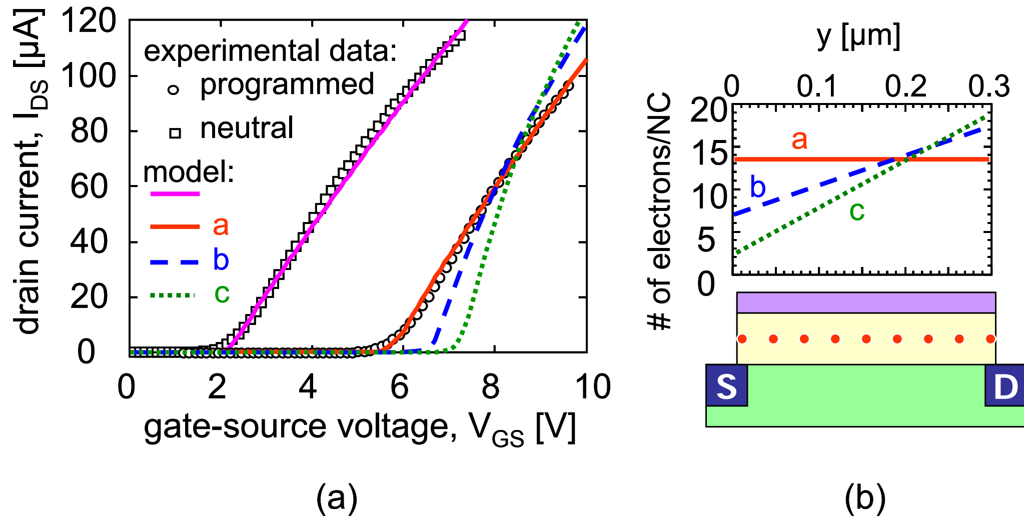

Fig. 6.20. Comparison between model (solid lines) and the experimental measurements (symbols) of a programmed and a neutral cell with different NC charge distributions. The inset shows the average number of electrons per NC as a function of the NC position along the channel.

The model has been calibrated to fit the I_D-V_{GS} characteristics of a single neutral NCM cell, i.e., a NCM cell with neutrally charged NCs. We extrapolated the product $\mu \cdot C_{ox}$,= 40.2 μA/V^2. This model can evaluate the I_D-V_{GS} characteristics for arbitrary NC

arrangement and NC charge distribution. Fig. 6.20a shows the good fit between our model and the experimental results on a neutral and a programmed cell (see solid lines). In these simulations we arbitrarily assumed that the nanocrystals are regularly spaced over a centered hexagonal lattice (see Fig. 6.21), where three nearby points form an equilateral triangle. This is an approximation of the real NC distribution, but we verified that the NC arrangement over the gate area has a negligible impact on the fresh and irradiated cell threshold voltage, as long as the total number of NCs per cell is constant and they cover the entire gate area. This is because the nanocrystal charging process tends to compensate any non uniformity in the spatial distribution of nanocrystals. In other words, the number of electrons stored within a NC decreases as the local NC density increases, due to the Coulomb repulsive force, which tends to reduce locally the oxide electric field during programming.

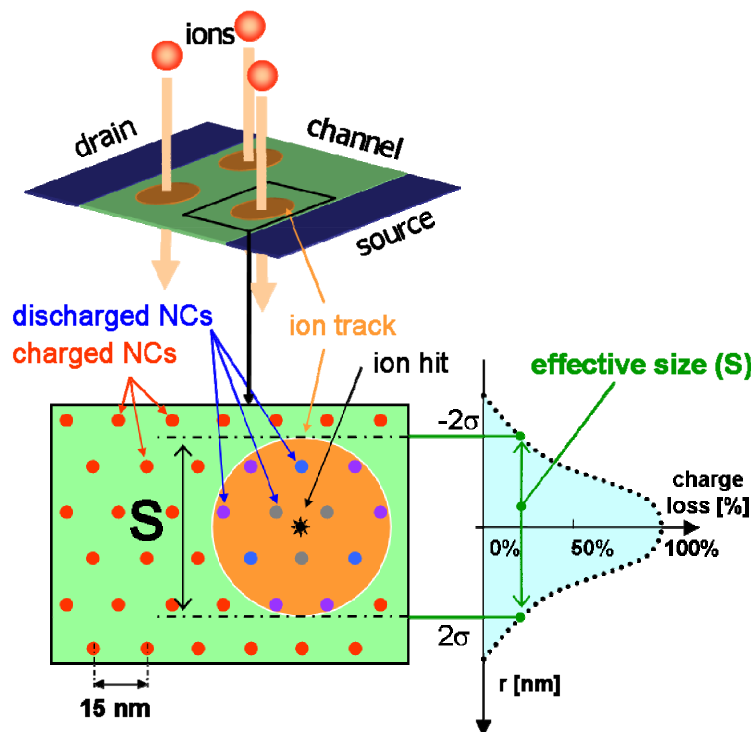

Fig. 6.21. Radiation damage model and notations: The nanocrystals are uniformly distributed with centered hexagonal pattern. The ion hit track is supposed to have a circular shape with diameter S. We approximated the amount of charge loss with Gaussian shape and we defined S = 4σ, as indicated in the qualitative plot on the right (not to scale).

Instead, the NC charge distribution is worthy of some considerations. In Fig. 6.20, we also show the simulated curves for three different NC charge distributions, marked *a*, *b*, and *c* (see Fig. 6.20b). The more the charge is concentrated toward the drain, the more the I_D-V_{GS} curves slope in the linear region. This occurs because the NCs closed to the drain (i.e., the most charged) are those most effective in limiting the drain current, while the channel conductance near the source is much higher. Hence, the MOSFET electrically behaves as if the channel length were smaller than its physical value.

The assumption that the nanocrystals are uniformly charged (as in case *a*) is a very good approximation, if the memory cell is programmed/erased with Fowler-Nordheim

injection. NOR structured flash memories usually feature more complex programming techniques, such as CHE (Channel Hot Electron) or CHISEL, which feature a stronger injection efficiency at the drain side (like curves *b* and *c*). However, we obtained the best fit with a uniform NC charge distribution. This is not unexpected. In fact, the CHISEL programming technique features good performance and larger injection efficiency with respect to the conventional CHE regime. It has also been demonstrated that CHISEL has a spatially more distributed charge injection across the tunnel oxide [170].

6.4.3.2 Radiation Damage Modeling

Once the electrostatic model of the NCM cell has been assessed, we consider the effects of the ion hits. For this, we made some additional assumptions (see Fig. 6.21):

B1) Each ion hit produces a region in a single cell where the nanocrystals are partially or completely discharged. The diameter of this region (*S* in Fig. 6.21) is strictly related the LET coefficient of the impinging ions. In the following, we will refer to the diameter S as ion track size. For sake of simplicity, we suppose *S* to be constant for all the ion hits.

B2) Anytime an ion hit occurs, it discharges the NCs within a circular area with diameter *S*, while all the charges stored outside this area are unchanged. Accordingly with the physics-based simulation reported by [128], we reasonably assume that the amount of charge loss from a NC is maximum if the NC is located very close to the ion hit position (ideally, in the center of the ion track) and it decreases with a Gaussian shape as the NC distance from the ion hit position increases. We arbitrarily defined $S = 4\sigma$ (as indicated in Fig. 6.21), i.e., the distance at which the Gaussian function fades at 13%.

B3) The ion hit number per cell (*M*) depends on the ion fluence. The probability that a cell experiences exactly *M* ion hits is calculated using the model discussed in the Appendix B and takes into account the effective irradiation area as shown in Fig. 6.16 and discussed in paragraph 6.4.1.

B4) Accordingly with the notations of Fig. 6.21, the coordinates (*x,y*) of each ion hit are described by a couple of random variables with uniform distribution within the intervals (0 – *W*) and (0 – *L*), respectively.

B5) The ion hit positions are independent of each other. Therefore, the *M* hits can be probabilistically described by *M* random variables, each of them having the same uniform distribution as in B4.

First of all, we simulated the statistical effects of exactly *M* ion hits on a NCM cell. Simulations have been implemented by using an algorithm that randomly generates the ion hit event occurrence, accordingly with the distribution probability in B4 and B5. At

each time one event is generated, the nanocrystals within a radius $S/2$ from the hit position are discharged (accordingly with B1 and B2), then a new event is generated. Once M events occurred, the E_{ox} component in linear region is updated, and the new drain-source current is simulated as described in the previous subparagraph.

Once the statistical distribution of the threshold voltage shift after M hits ($D_{V_{TH}}^{M}$) is known from the simulations, we calculated the expected threshold voltage distribution after M ion hits of the whole cell array, by convoluting $D_{V_{TH}}^{M}$ with the fresh threshold voltage distribution, $g_0\left(V_{TH}\right)$:

$$g_M\left(V_{TH}\right)=\frac{\int g_0\left(V_{TH}-\Delta V_{TH}\right)\cdot D_{V_{TH}}^{M}\left(\Delta V_{TH}\right)\cdot d\Delta V_{TH}}{\int D_{V_{TH}}^{M}\left(\Delta V_{TH}\right)\cdot d\Delta V_{TH}}$$

where $g_M\left(V_{TH}\right)$ is the theoretical V_{TH} distribution under the assumption that each cell has been hit by exactly M ions. Finally, by defining p_M as the probability that M ion hits occur in a cell (calculated accordingly with B3), the final array V_{TH} distribution is calculated as:

$$f\left(V_{TH}\right)=\sum_{M=0}^{\infty} p_M\cdot g_M\left(V_{TH}\right)$$

The main simulation variables were the ion track size (S), the ion fluence, the nanocrystal spatial distribution, and the nanocrystal charge distribution.

6.4.4 Simulation Results and Discussion

Developing a statistical description of the ion hit events producing the threshold voltage shift is the only tool for estimating some interesting parameters, such as the size of the ion hit impact region as well as the amount of charge loss per hit. In this way, it is possible to analyze the average behavior of a large number of cells under heavy ion irradiation and to extrapolate from these results the expected average behavior of a single cell. Clearly, any anomalous behavior related to some single peculiarity is neglected. The capability to trigger and locate in real time a single ion hit with nanometer resolution may be desired. However, this does not appear feasible and compatible with the instruments presently available. Hence, the model we have developed is still based on the analysis of large cell arrays, which offers undoubtedly a convenient and statistically relevant case study.

6.4.4.1 Threshold voltage shift dependence on ion track size and position

Before comparing the simulation and experimental results, in this section we analyze the impact of the ion track size S on the threshold voltage distribution after M ion hits per cell and the corresponding average threshold voltage shift, which are the most important simulation outcomes. In Fig. 6.22, we show a summary of the simulation results. Fig. 6.22a shows the average V_{TH} variation ($<\Delta V_{TH}>$) predicted by

our model as a function of the ion track size *S* and for different ion hit numbers (from 1 to 8). In these simulations, we consider for simplicity that the nanocrystals are uniformly charged and regularly spaced with the same centered hexagonal pattern of Fig. 6.21. Fig. 6.22b shows an example of the simulated Weibull plot distribution of the threshold voltage variation after 1-8 hits for an arbitrary ion track size *S* = 90 nm.

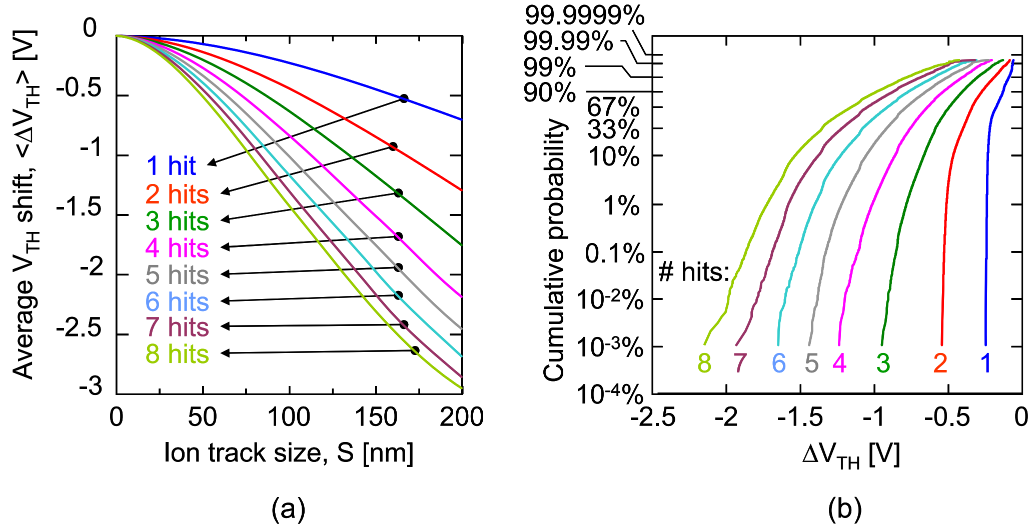

Fig. 6.22. a) Simulated average threshold voltage variation of an irradiated cell as a function of the ion track size and the number of hits. b) Simulated cumulative probability of the threshold voltage variation in an irradiated cell for different ion hit number and with *S* = 90nm.

<ΔV_{TH}> increases in absolute value, with increasing ion track size or ion hit numbers, as expected. This is primarily due to the enhanced amount of discharged nanocrystals. Noticeably, from Fig. 6.22b we observe that keeping constant *S* and increasing the ion hit number, the ΔV_{TH} distributions shift leftward, while becoming wider and wider. At this regard, some considerations are worthwhile.

First, when the ion hits are few (namely 1 or 2), the threshold voltage is not significantly impacted and it is weakly dependent on the hit position. In fact, if the ion track size (90 nm Fig. 6.22b) is much smaller than the channel length, no percolation path can exist. Consequently, the position of the ion hit is not relevant from the viewpoint of the cell threshold voltage, and the modest dispersion of the V_{TH} distribution around its mean value is mainly determined, whether the ion hit occurs in the middle or on the edges of the channel. In fact, in the last case the effective size of the discharged nanocrystal region is smaller, because it can be roughly estimated as the intersection of the circular shaped ion track and the gate active area. Hence, fewer nanocrystals are actually discharged.

Second, when the hit number increases, the manner in which the ion hits modify the cell I_D-V_{GS} is very different and it strongly depends on the ion hit positions. Let us consider, for instance, Fig. 6.23. Here we show two examples of quadruple hit patterns representing two opposite cases (see Fig. 6.23a). We assumed the track size of each ion hit *S* = 100nm. Fig. 6.23b we show the I_D-V_{GS} of a programmed device (line), and two cells that were hit by 4 ions (symbols, marked with #1 and #2, respectively). For reference, in the same plot we show also the simulation of the neutral device (line),

which is very close to the erased cell (almost neutral as discussed in paragraphs 6.3.2 and 6.4.2).

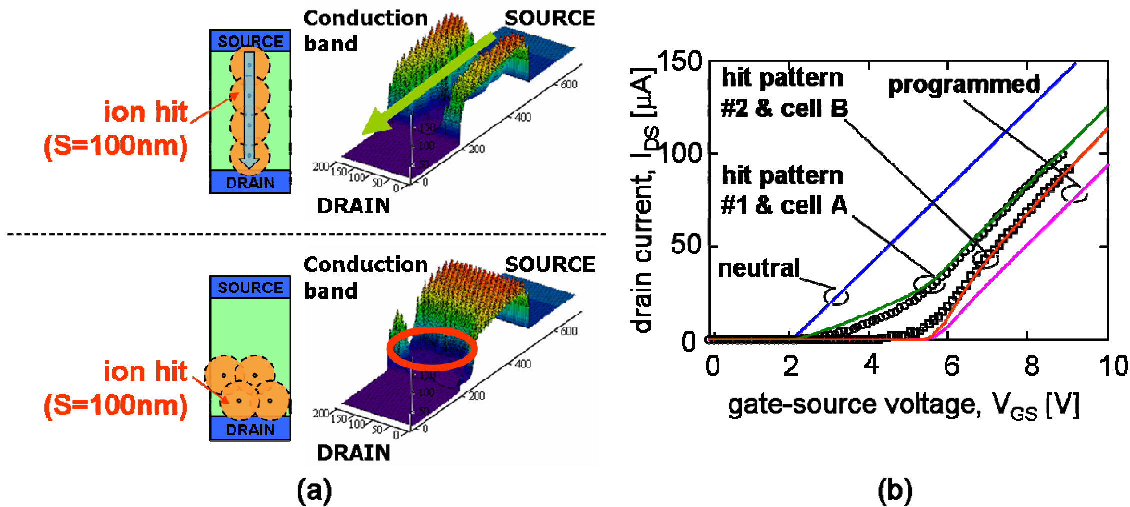

Fig. 6.23. a) Comparison between two possible quadruple hit patterns (the effective track size is supposed *S* = 100 nm. Hit pattern #1: four hits perfectly aligned along the channel and simulated channel conductance of the hit pattern. Hit pattern #2: four hits close to the source. b) Simulated I_{DS}-V_{GS} curves of the neutral, programmed and hit cells with pattern #1 and #2, respectively (lines). Two experimental examples of hit cells (A and B) are also shown, for comparison (symbols).

In the case of ion hit pattern #1, a percolation path exists between source and drain (Fig. 6.23a, up) and the cell turns on earlier than the fresh programmed cell. Instead, in case #2 the ion hit positions are very close to each other and they are not able to generate any percolation path Fig. 6.23a, down). The cell V_{TH} slightly reduces, but it is less affected than in case #1. Such difference of behavior cannot occur on conventional floating gate cells, because the V_{TH} variation mostly depends on the number of hits and not on their positions. In fact, after each ion hit the residual floating gate charge uniformly redistributes, independent of the hit positions. For comparison, in the same plot of Fig. 6.23b we show two examples of hit cells (A and B), which feature a large and a small threshold voltage shift after irradiation. Of course, we cannot exactly know how many ions hit the two cells. However, their behavior resembles the two simulation cases #1 and #2, indicating that a percolation path likely exists in the irradiated cell A, even at low V_{GS}.

Finally, in Fig. 6.24 we show the comparison between the experimental results and the simulations. We achieved the best fit of the tail cell distribution with *S* = 85nm.

6.4.4.2 Effects of the nanocrystal charge distribution

So far, we have assumed that the nanocrystals are uniformly charged and regularly spaced over the entire gate area. To take into account of such charge non-uniformity in our model, we ran simulations by using a linearly increasing nanocrystal charge density along the channel. The most important results are summarized in Fig. 6.25. Simulated effects of NC charge distribution on *VTH* variation for a 90-nm ion track size. The inset shows the average number of electron per NC as a function of the NC position along the channel.. The Weibull plot refers to the expected threshold voltage variation after 4 ion

hits with a track size S = 90nm. The main effect of the non-uniformity of the nanocrystal charge is the increased dispersion of the V_{TH} variation around its mean value. The enhanced dispersion of the threshold voltage distribution is due to the reduced sensitive area, as discussed in subparagraph 6.4.3.1. In fact, the MOSFET threshold voltage is significantly affected only by the ions hitting the cells in the drain regions, where most of the electrons are stored. This translates into a reduction of the actual sensitive gate area. In other words, this is like reducing the MOSFET channel length: fewer hits are needed to form a conductive path.

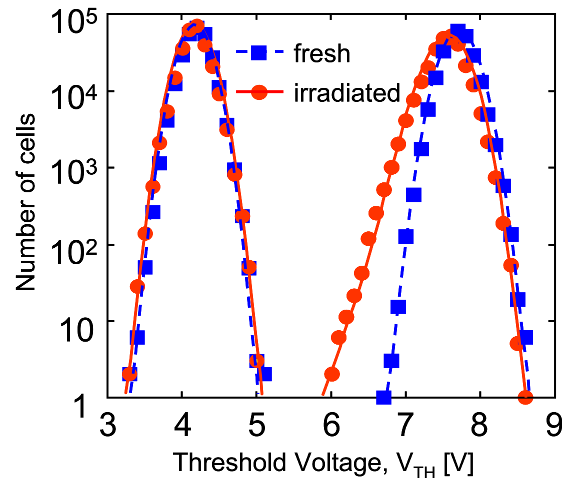

Fig. 6.24. Comparison between the simulations (lines) and experimental results (symbols) of Fig. 6.17. The symbols represent the experimental data and the lines represent the theoretical fits. The best-fit value of the ion track size is S = 85nm.

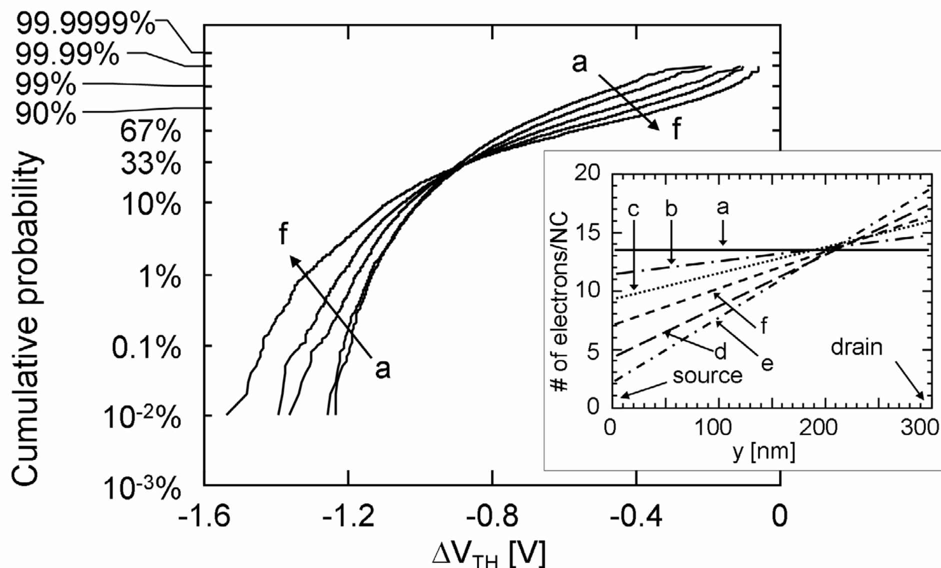

Fig. 6.25. Simulated effects of NC charge distribution on V_{TH} variation for a 90-nm ion track size. The inset shows the average number of electron per NC as a function of the NC position along the channel.

6.4.5 Charge loss mechanisms: comments on the transient conductive path

Our simulations show that in large-area NC MOSFETs, the V_{TH} decrease is modest, unless ions generate very large tracks. Incidentally, for a single hit, its position along the channel has few effects on the V_{TH} variation, as expected. Still, experimental and

simulation results confirm that 3 to 5 ions can induce a measurable threshold voltage variation.

Now some questions arise: what happens inside the ion track and what are the charge loss mechanisms?

As mentioned above, there are debates about the physical nature of the charge loss mechanisms, and the two mechanisms that can quantitatively explain the large threshold voltage variation in floating gate cells are the TCP and the transient currents of excited carriers.

Let us assume that the transient conductive path as originally conjectured by its proposing authors (i.e. a conductive cylinder of hole-electrons pairs, with 4÷5-nm radius) is the main charge loss mechanisms. Then, about one hundred of hits would be required to induce a noticeable threshold voltage variation in our devices, while we have shown that with 3-8 hits the threshold variation is small, but it is still more than noticeable[20]. The small radius hypothesized by the TCP's authors, not only does not agree with our experimental data, but also with their recent results! In fact, in [121] [127], they showed that a single ion can induce severe charge loss (as large as 2V) even in the cells adjacent to those ones, which were presumably hit directly by the ion[21]. This is surprising, as these adjacent cells may be well over 100nm far away!

Hence, to induce such large variations in such large areas, TCP cannot be as small as its authors originally conjectured: it should have a 40÷100-nm radius, rather than 4÷5 nm, that is, the ion should generate the hole-electron pairs in a cylinder with radius between 40-100nm (i.e. the impact area would be at least 100 times higher than originally hypothesized). For this reason, taking into account the ion-LET the average hole-electron density generated by the ion hit in such a large area in the silicon dioxide must be around 10^{20}cm^{-3} (and not 10^{22}cm^{-3}).

At this point, some observations are noteworthy. First, are 10^{20}pairs/cm^3 still enough to trigger a transient conductive path? In fact [124] was strongly based on the very high radiation-generated hole-electron pair density, which in turn triggered the conductive path. Besides, 10^{20}carriers/cm^3 is not a typical carrier concentration of a strong conductor. Second, some results in literature [93] state that actually, in silicon dioxide the radiation-generated hole-electron pair track have a peak density around 10^{22}pairs/cm^3 and a diameter of 4-5nm. As a result, the TCP cannot have a radius as large as 40-100nm. Hence the TCP, if occurs, is neither the responsible for the charge loss we observed in our samples, nor for the charge loss of the adjacent cells observed by Cellere et al. in [121],[127], even when the irradiation was not performed tilted [121]. As a last remark, the TCP was hypothesized because the other models in the literature could not quantitatively account for the very large charge loss. On the

[20]Even though there is not a complete closure of the programming window, i.e. the programmed and erased cell distributions do not overlap.
[21] I.e. the cells featuring the larger threshold voltage variation.

contrary, the latest model presented in [119] not only is in good agreement with all the experimental results, but also it is strongly supported by physical explanations and simulations. Hence, either the TCP is not the main responsible for the charge loss (in FG and nanocrystal cells), or it does not even exists!

Our model allows us to estimate the size of the area affected by the ion hit to be 85nm for 50-MeV Cu ions, again in agreement with the ion-track size in silicon reported by Dodd [128]. This suggests that the ionized electron-hole pairs in the polysilicon gate and in the substrate are likely responsible for the partial neutralization of the charge stored in the nanocrystals, and this is quantitatively confirmed also by the model proposed by Butt-Alam [119].

6.4.6 Effects of the cell scaling

Fig. 6.26 shows a prediction of how a single ion hit occurring exactly in the center of the NCM cell channel, i.e., in the worst case position, would affect the cell threshold voltage as a function of the cell active area. If the cell dimensions are scaled below the size of the ion track and the number of nanocrystals per cell may be as small as ten, even a single ion hit may discharge (almost) all the nanocrystals. Nevertheless, NCMs are expected to be still more robust than conventional Flash memories for several reasons. First of all, it has been shown that the floating gate may be completely discharged by a single ion hit [122],[129]. Second, multiple flips have been reported in floating gate devices with 90-nm technology nodes or smaller (i.e., when the FG area scale below $10^{-2}\mu m^2$) due to the charge collection at multiple nodes [121]. For comparison, the simulations of Fig. 6.26 predict that NCMs as small as $10^{-3}\mu m^2$ still preserve an appreciable programming window (in the range of 1V) after a single ion hit, indicating that the nanocrystals are not completely discharged yet, at least on the border region of the ion track, and that the residual NC charge is still able to sustain an appreciable electric field, which prevents the channel formation. The strong improvement is due to the discrete and insulated nature of the nanocrystals, and their reduced nanocrystal coverage area.

6.4.7 Radiation Lifetime Considerations

These achievements allow further insight and accuracy in predicting radiation lifetime under heavy ion irradiation. Nowadays several efforts are being investigated to predict how many ion hits and/or how much charge loss a flash memory cell can tolerate, before losing its bit information. In this sense, our model is a helpful tool to extrapolate the device lifetime (related to the maximum tolerable ion hits) during and after exposure to ionizing radiation.

On top of all these considerations, our results raise some questions also on the radiation sensitivity of NCMs as the size of the devices scales down. In fact, even a single ion hit may easily mark the failure of a very small-size cell.

On the other hand, extrapolating the device lifetime from this model raises the obvious question of the failure criteria definition, i.e., how large is the maximum threshold voltage shift that a flash memory cell can tolerate. This may span a wide range, depending on the technology parameters, the sensing circuitry the amount of stored charge, the sensing current, and so forth. Since, such definition is outside the scope of this study, we arbitrarily assumed that the cell fails when the programming window (i.e., the difference between the programmed and erased threshold voltage values) decreases by 20% of its initial value [2]. For instance and with reference to our results, the programming window is predicted to drop by 20% after a single hit, when the area of the cell approaches 0.006μm^2. For comparison, it has been shown that floating gate memories almost completely lose their charge even when the cell area is far above 0.1-μm^2.

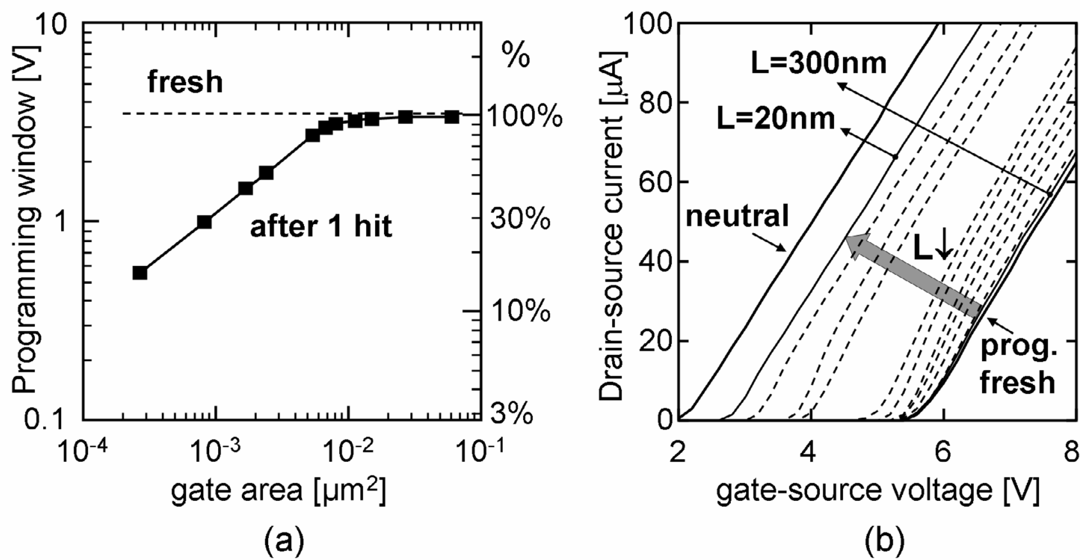

Fig. 6.26. a) Predicted threshold voltage shift after a single ion hit as a function of the cell gate area (the ion hit has been supposed in the center of the channel). b) Simulated I_{DS}-V_{GS} curves after a single hit (in the same condition of Fig. a) as a function of the gate area.

Clearly, these are only simulation results. Changes in simulation parameters (such as the ion track size or the amount of charge loss per ion hit) or technological parameters (such as the dielectrics thickness or the NC density) can produce changes in the extrapolated NCM behavior. Because the threshold voltage decrease correlates to the ion track size, the definition of proper failure criteria must face the problem of assessing the ion LET dependence of the ion track size. Moreover, it is important to note that the irradiation conditions (such as the angle of incidence, temperature, etc) might strongly influence the charge loss mechanisms. These external parameter sensitivities are essential to permit a reliable prediction of radiation hardness. More data and more extensive work are needed to clarify some important aspects, such as the trend of the window closure for very small-area cells or the charge loss dependence on LET of the radiation source. In this regard, the gate leakage current is less important for NCM technologies featuring a large number of NCs (see section 6.3). However, as the cell

sizes are scaled down and the NC number is reduced, oxide leakage currents (which were not considered here) potentially pose a threat to cell data retention.

From the viewpoint of radiation tolerance: while evaluating the device lifetime from the charge loss or the oxide leakage current may be acceptable and well justified in floating gate cell lifetime extrapolations, it may become questionable in NCM, at least as long as the cell size is larger than $0.01\mu m^2$. In these components, failure may occur on the peripheral circuitry due to the onset of SEGR or RSB, well before a critical charge loss had occurred in the cell array.

6.5 Conclusions

Heavy ion irradiation effects have been thoroughly analyzed using different devices, ion species and LET. We started from the first investigations performed on CAST, which allowed to assess the permanent damage effects on large arrays. The increased gate leakage does not affect substantially the threshold voltage. Still accelerated breakdown occurs after heavy ion irradiation. The first estimations on the ion track size were given. After that, we performed heavy ion irradiation tests on addressable arrays, which allowed us to analyze the radiation effects on each cell. This allowed us to estimate the number of ion-hits required to appreciably change the cell threshold voltage, and to confirm that, unlike FG memories, NCM still feature a good retention after irradiation: after 20 days no cell exhibited large threshold voltage variation, whereas, in FG memories, just after some hours a large tail appears.

Finally we presented for the first time a model of the heavy ion induced charge loss on nanocrystal memory cells. Our model consists of two steps: we first modeled the NCM cell electrostatics, which permitted us to simulate the I_D-V_{GS} curves. Second, a statistical-based simulation was used to account for the ion hit effects. We modeled the progressive nanocrystal charge loss as the superposition of many ion hits with a given track size, whose occurrence positions have been randomly generated with uniform distribution probability. The model has been validated with a focused microbeam test, achieving an excellent fit of the tail cells distribution. Our simulations best fit a track size of 85 nm for 50-MeV Cu ions, which correlates well to other experimental evidence and simulations previously reported (see section 6.3 and [128]). The model, together with the experimental data, give also another indirect confirmation about the inconsistency of the transient conductive path, and it is in good agreement with several other works [119],[128].

Even though in most of simulations we assumed the nanocrystals are uniformly charged and regularly arranged, this model can evaluate the I_D-V_{GS} characteristics for arbitrary NC arrangements and NC charge distributions. This permits us to extend our study to the role of the different programming techniques, which may produce non uniform charging of the nanocrystals (e.g., symmetric or asymmetric Fowler-Nordheim injection, channel hot electron, channel initiated secondary electron, and so forth).

This predictive model may also apply (with only a few modifications) to similar devices based on the discrete storage technology, such as SONOS or NROM™ or hybrid SONOS-nanocrystal devices also proposed as possible replacements for DRAMs [171] or even more advanced structures, such as FINFLASH, which integrates the advantages of nanocrystal and SONOS technologies on a FinFET, i.e., a MOSFET with vertical structure [25].

For radiation lifetime viewpoint, this model confirms the outstanding improvement of nanocrystal technology over floating gate technology, where threshold voltage shifts as large as 3-4V have been reported. It predicts that nanocrystal technology has a good potential for the discrete trap storage approach as a radiation hardened memory technology, while maintaining low fabrication costs. We also point to the role of peripheral circuitry degradation and breakdown, which can occur well before the information is lost.

CHAPTER 7

Ionizing radiation effects on Phase Change Memories

Phase change memories are considered by some companies as one of the most affordable alternatives to NOR Flash. They feature many improvements, especially in terms of enhanced endurance, high write speeds and single bit alterability. Furthermore, PCM operates at lower voltages, reducing, in principle, the area requirements for the peripheral circuitry.

PCM also store the information differently from the conventional Flash memories. The charge can be removed with much less energy than that required to melt the chalcogenides and to change its state. In addition, the energy required for a SEU is even smaller, making PCM suitable also for SRAM replacement. These considerations however cannot ensure that the PCM are radiation tolerant, and a detailed analysis will be performed here.

In this chapter we will discuss the effects of different ionizing sources on PCM arrays: protons and electrons. We will also compare the effects on arrays with different cell selectors: BJT and MOSFET. The cell programmability after irradiation and its annealing will be assessed as well.

7.1 Devices analyzed

The devices used to evaluate the radiation response of the PCM are 4-Mbit and 8-Mbit addressable arrays, built with a 0.18-μm lithography, and manufactured by STMicroelectronics (Agrate). Shallow trench isolation and 7-nm gate oxide thickness are employed. The storage element is a Germanium-Antimony-Tellurium ($Ge_2Sb_2Te_5$, GST) alloy.

The 4-Mbit arrays use MOSFET cell selectors, while the 8-Mbit arrays employ BJT selectors. BJT selectors, as mentioned in chapter 2, allow for a much denser array. Indeed, the two test chips have the same die size, despite the different memory density. However, MOSFET selectors allow to avoid the cumulative leakage arising from the reverse biased base-to-emitter junctions of all the unselected cells [47].

Fig. 7.1a shows the SEM cross section of the MOSFET array along the bit line, and Fig. 7.1b show the schematic representation of the PCM cell, without cell selector.

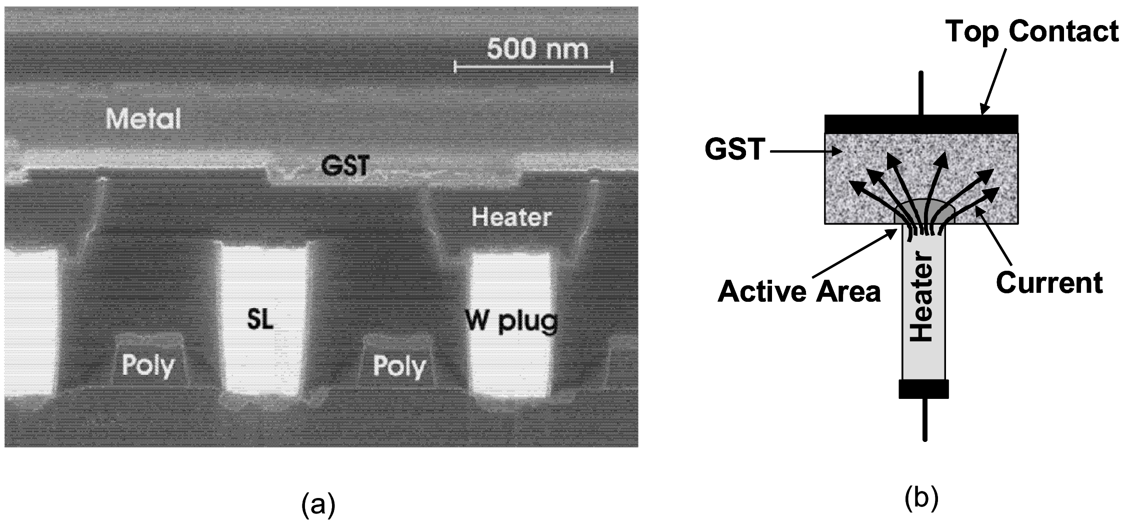

Fig. 7.1. SEM cross section of the MOSFET-based PCM array along the bit line (a). Schematic cross section of the storage element (b).

As already mentioned in chapter 2, the programming is obtained by heating the storage element using electrical pulses. Once the chalcogenides melts, it loses its polycrystalline structure and, if rapidly cooled down, it remains in the amorphous state. This operation is called RESET, and the chalcogenides feature a high resistance. To switch the storage element back to its polycrystalline state, the chalcogenides must be heated to a temperature between the glass transition state (300°C) and the melting point (600°C). During this phase, nucleation occurs and in few (tens of) nanoseconds the chalcogenide returns to its polycrystalline state. This state and the corresponding program operation are called SET, and it features a low resistance.

Fig. 7.2 shows the schematic connections between the PCM cell (GST and cell selector) and the bit line selector (M_1). Table 7 shows the voltages required for the read, SET and, RESET operations, and the corresponding currents. It is worth to remark that BJT selectors require also a non negligible steady state base current. Fig. 7.3 shows the microphotographs of the test chips used in this chapter.

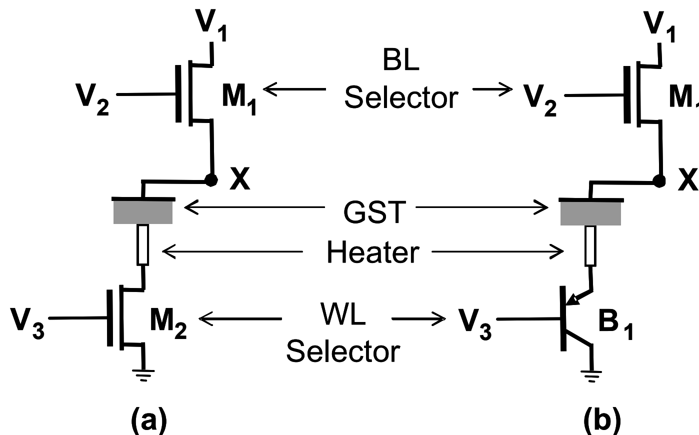

Fig. 7.2. Schematic connection of the PCM memory cell with the bit line X and its selector M_1. a) PCM with MOSFET selector (M_2). b) PCM with BJT selector (B_1).

The arrays can be fully characterized with an ad-hoc instrument, which is described in the Appendix C. It provides all the necessary voltages, pulse timings and has on-board current measurements units. Each MOSFET-based array has 2048 BL and 2048

WL, while BJT based arrays have 4 banks, each one having 1024 BL and 2048 WL. The cascode configuration allows a precise voltage control for the read and program operations, avoiding any possible read-write disturb. [47]. In fact, the voltage at the source cannot exceed the voltage applied to the gate. The stored information is sensed by applying a voltage of 1.8V to the bit line selector MOSFET (M_1 in Fig. 7.2), and enabling the cell selectors corresponding to the WL to be read (see Table 7) In this way, a 0.4V is applied to the GST resulting in a current flow, which reflects the stored data. Fig. 7.4 shows the typical distributions of the SET and RESET cell currents.

	MOSFET SELECTOR			BJT SELECTOR		
	READ	SET	RESET	READ	SET	RESET
$V(V_1)$ [V]	1.8	5.2	5.2	1.8	5.2	5.2
$I(V_1)$ [μA]	0-100	300	600	0-100	300	600
$V(V_2)$ [V]	0.9	2.7	4.6	1.2	3.1	5.0
$I(V_2)$ [μA]	0	0	0	0-40	300	300
$V(V_3)$ [V]	3-5.2	5.2	5.2	0	0	0
$I(V_3)$ [μA]	0	0	0	0-40	300	300

Table 7. Voltage and currents of Fig. 7.2 for MOSFET and BJT based PCM, during read, set and reset operations.

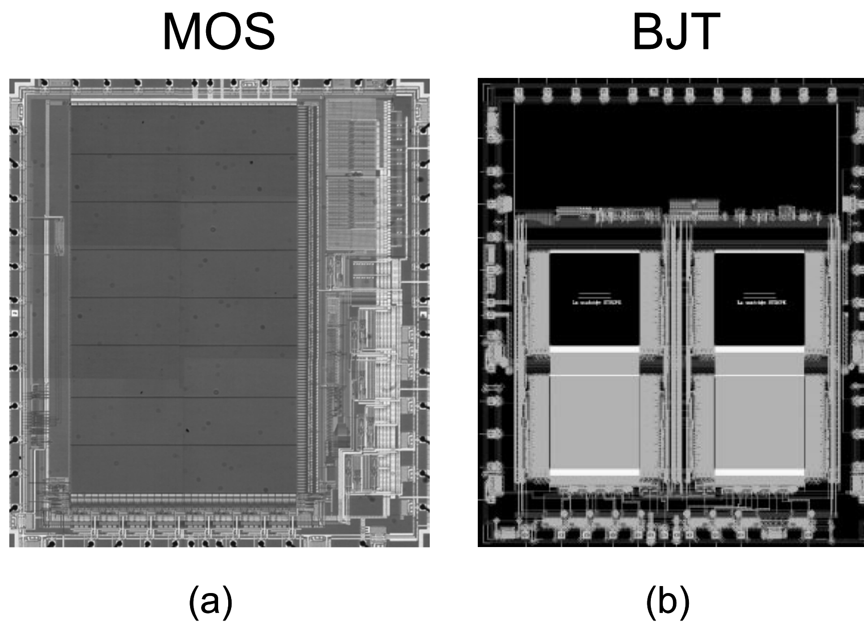

Fig. 7.3. Microphotographs of the analyzed PCM arrays: MOSFET based (a) and BJT based (b).

Noticeably, the polycrystalline state is stable and no drift is measured after 1-month retention time. On the other hand, the resistance of the amorphous state tends to increase with time [172].Thus, if a RESET operation is performed on a cell that is already in the RESET, the electrical resistance of that cell is partially reduced.

Remarkably, only a small portion of the entire GST film is actually involved in the phase change effect, while the outer layer remains polycrystalline. The GST to heater interface area is about 2000nm^2.

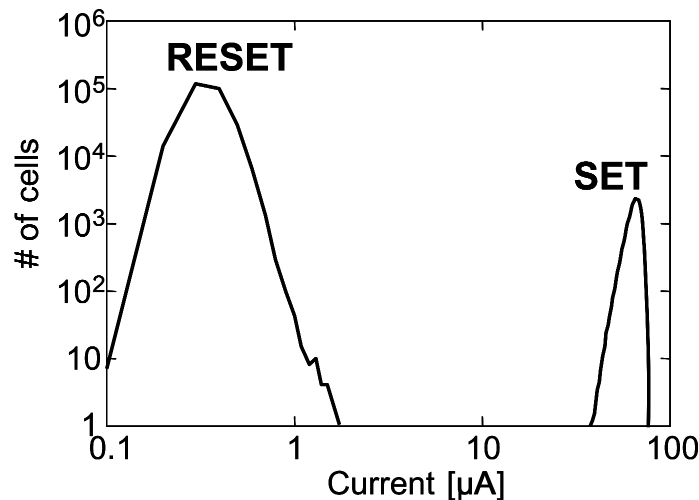

Fig. 7.4. Typical SET and RESET current distributions of a 4-Mbit PCM array.

7.2 Irradiation and experimental setup

Proton irradiation has been performed at the μ-beam facility at the INFN-LNL (Italy), using 2-MeV proton (LET=0.11 MeV·cm^2·mg^{-1}). The 8-MeV pulsed electron beam (2 μs pulse length, 25 Hz pulse repetition rate) irradiation was performed at the LINAC Irradiation Facility (ISOF-CNR, Bologna, Italy). Electron irradiation was performed using a broad beam, hence the whole chip was irradiated. On the contrary, proton irradiation can be focused on a very small area, enabling the evaluation of the radiation effects only on the memory array. Proton irradiation was thus performed in the whole chip area as well as in a small spot. We estimated that within the irradiation area, 910000 cells have been irradiated. In particular, a rectangular area comprising about 1175 WLs and 775 BLs was irradiated.

Step	Operation
1	Programming
2	1 month device storing
3	Reading
4	Irradiation step
5	1st Reading
6	Inverse programming of ½ cells
7	2nd Reading
8	Inverse programming of ½ cells
9	3rd Reading
10	To step 4

Table 8. Experimental setup employed for the electron irradiations.

The PCM arrays were programmed with a checkerboard pattern, in order to avoid any position dependent effect. In order to evaluate the effects of radiation on the cell programmability, the samples irradiated with electrons followed the experimental procedure shown in Table 8. After the cells were programmed a read and subsequent a one-month annealing were performed, in order to allow the amorphous GST to reach its equilibrium state. Without this step, the drift would have impacted on the measurement,

and it would have been incorrectly ascribed to the ionizing radiation effects. After this step, the whole arrays have been read again (step 3). Then, after the devices were irradiated (step 4) and read again (step 5), half of each array was programmed with the inverse checkerboard, i.e., the bits, which were originally in the SET state, were put in RESET, and vice versa (step 6). After the second read operation (step 7), the checkerboard pattern was restored, only programming the part of the array, which was previously modified by the inverse program operation(step 8) and a third read was performed (step 9). Then, steps 4-9 were repeated to increase the irradiation dose.

Once the effects of the ionizing radiation on the programmability were known, the whole irradiated area was only read (without reprogramming), in order to achieve better statistics (only for proton irradiation). All the devices were grounded during irradiation.

7.3 Effects of electron and proton irradiations on MOSFET-based arrays

7.3.1 Prompt irradiation effects

Fig. 7.5 shows the SET and RESET distributions measured just after electron irradiation (step 5). These distributions account only for the part of the array, which was not reprogrammed after each irradiation step. A much clearer trend can be observed considering the average of the measured SET and RESET currents, which are plotted in Fig. 7.6 as a function of the irradiation dose. Remarkably we observe very different trends on the SET and RESET distribution. In fact, the RESET current distribution monotonically increases with increasing dose, while the SET distribution features a turnover at highest dose levels.

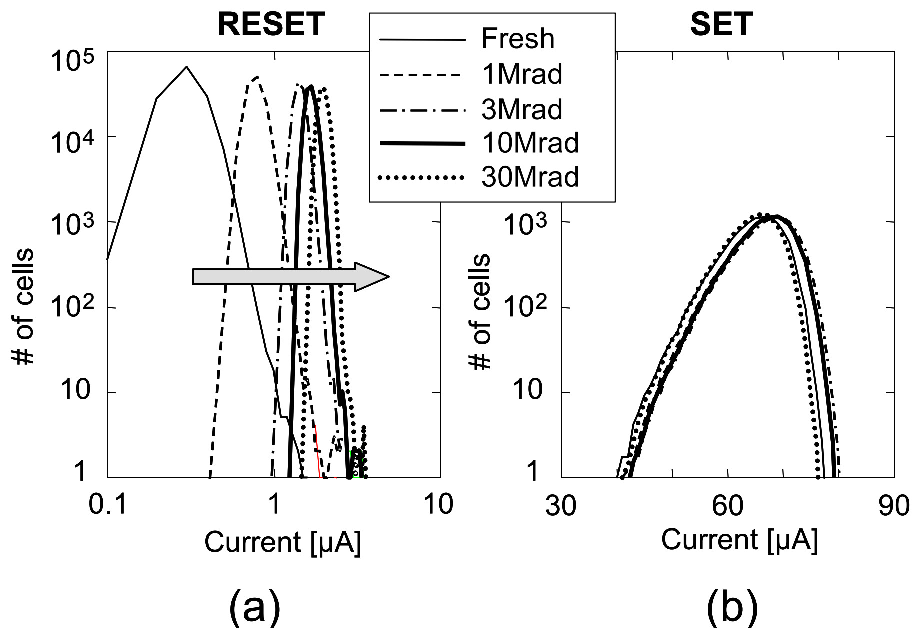

Fig. 7.5. RESET (a) and SET (b) distributions after different irradiation doses measured on arrays with MOSFET selectors. The devices were irradiated with 8-MeV electrons.

Furthermore, by considering the RESET distribution of Fig. 7.5a, there is a small "tail" of anomalous cells, which increases with increasing doses. On the contrary, no tail appears in the SET cells.

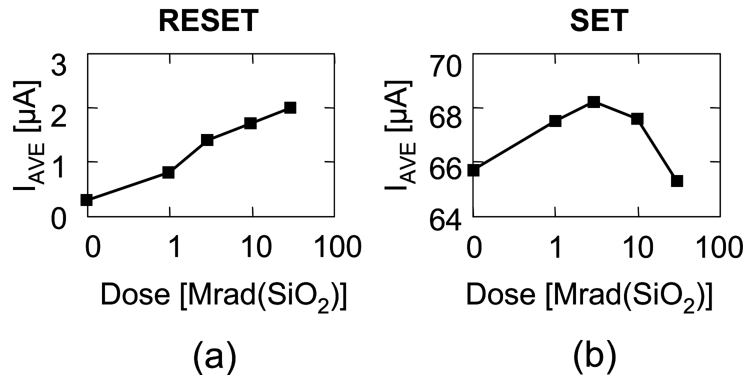

Fig. 7.6. Evolution of the average currents of Fig. 7.5 as a function of the irradiation dose. The average current of the RESET (a) distribution increases monotonically, while the cells in the SET (b) state feature a turn-over.

Proton irradiation, performed on the whole chip area, induces a much stronger effect, as can be seen in Fig. 7.7, inducing a positive almost rigid shift in SET and RESET distributions. When the proton irradiation is performed only on a fraction of the array, a secondary peak appears in the RESET distribution, while the SET distribution becomes wider (see Fig. 7.8). Noticeably, we found that the number of cells, which experienced a current variation greater than 1µA, is much higher than the cells within the irradiation spot (1.5M vs 910k cells) as it will be discussed later.

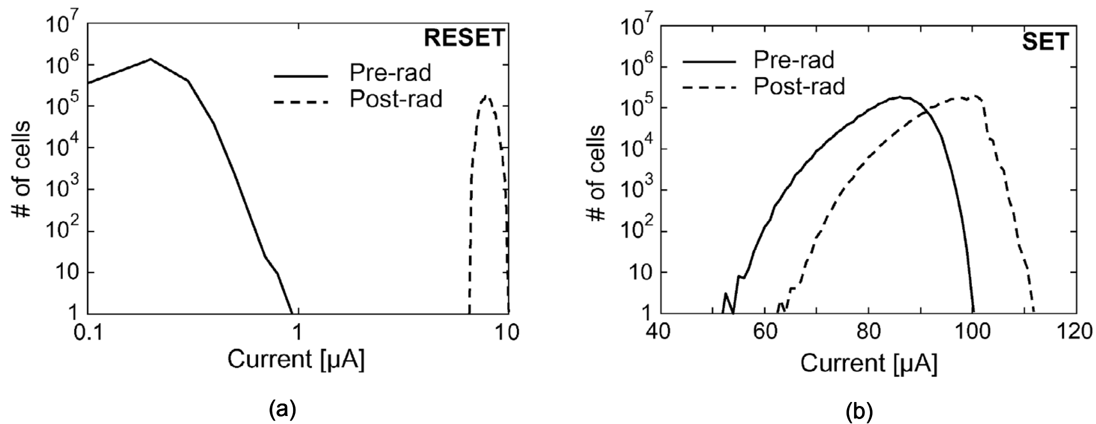

Fig. 7.7. Current distributions for RESET (a) and SET (b) cells before and after 10-Mrad(SiO_2) proton irradiation. The whole die was irradiated.

The increased currents measured in Fig. 7.5-Fig. 7.8 are all due to positive trapped charge in the oxides. In fact, there are various reports in the literature that 7-nm oxides can still trap a considerable amount of charge, which may last for days. In fact, the MOSFET M_2, which operates as a source follower, determines (through its threshold voltage and the gate applied bias) the voltage applied to the GST.

The relationship between the voltage at the gate and the voltage at the source is:

$$I_D = \frac{W}{2L}\mu_n C_{ox}\left(V_{GS} - V_{TH}\right)^2$$

$$I_D = \frac{V_X}{R} = \frac{W}{2L}\mu_n C_{ox}\left(V_{GS} - V_{TH}\right)^2 = k_n\left(V_{GS} - V_{TH}\right)^2 = k_n\left(V_2 - V_X - V_{TH}\right)^2$$

$$V_X = V_2 - V_{TH} + \frac{1}{2\cdot k_n \cdot R} - \sqrt{\frac{\left(V_2 - V_{TH}\right)}{k_n \cdot R} + \left(\frac{1}{4\cdot k_n \cdot R}\right)^2}$$

In the previous equations, the long-channel approximation has been considered. Furthermore, it has been assumed that the cell selector M_1 has a much smaller resistance than the GST. This is a good approximation as the gate to source voltage of M_1 is very high compared to its threshold voltage i.e., M_1 has a very strong overdrive. The body effect is accounted in V_{TH}.

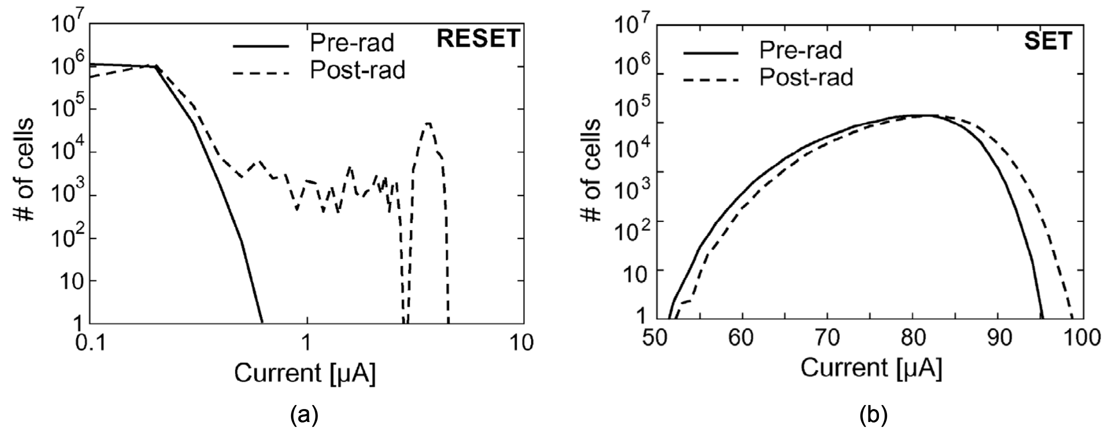

Fig. 7.8. Current distributions for RESET (a) and SET (b) cells before and after 30-Mrad(SiO_2) proton irradiation. Only part of the memory array was irradiated.

From the equation above, if the load resistance (the GST) is high enough, and if the body effect can be neglected, the voltage at node X depends (sub) linearly on $V_2 - V_{TH}$. Hence, if the threshold voltage is decreased by $-\Delta V_{TH}$ (corresponding to an increase of $V_2 - V_{TH}$), the voltage at the node X increases almost of the same amount ΔV_{TH}. Thanks to our experimental setup, we can precisely evaluate on a fresh device the effects of the increasing $V_2 - V_{TH}$. Fig. 7.9a shows the set distributions measured at different values of ΔV_2. Fig. 7.9b shows the extrapolated average value, which increases almost linearly with ΔV_2. From those data, we can estimate that the 2.5μA and 11 μA variations are consistent with a threshold voltage variation of about -20mV and -90mV, respectively. Assuming that most of the trapped charge is in the middle of the gate oxide, we obtain a trapped charge density of $1.2\cdot10^{11}$cm^{-2} and $5.6\cdot10^{11}$cm^{-2}, respectively. These estimated values are in perfect agreement with other works reported in literature [111],[173].

The presence of the turn-over is not unexpected. In fact, as seen for nanocrystal memories, at high doses the interface trap generation becomes dominant. The interface trap contribution is twofold. In fact, the silicon-to-oxide interface is strongly degraded

at high doses (10Mrad and up), and the radiation-generated interface traps increase the threshold voltage, due to the enhanced subthreshold slope. Moreover, interface traps, not only increase the subthreshold slope, but also reduce the electron mobility (especially at the highest dose). This translates in a higher gate-to-source voltage required to drive the same current, which can be thought as an increased threshold voltage. Hence, at low doses the voltage applied to the GST increases, and at higher doses it progressively decreases.

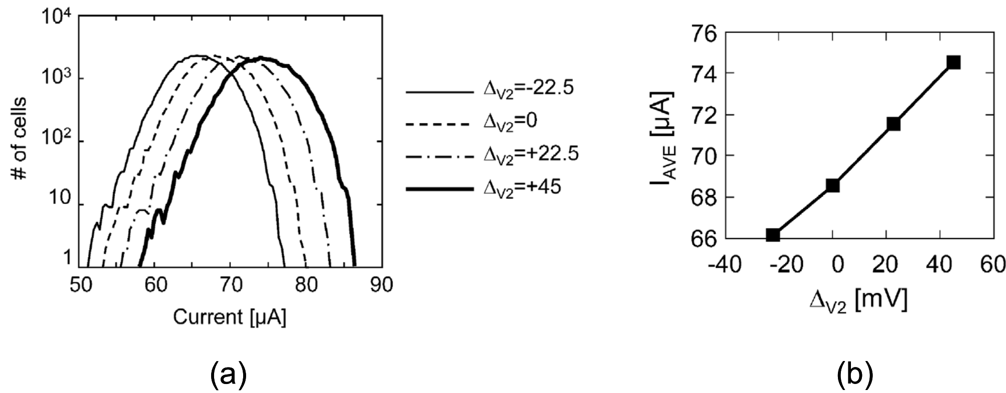

Fig. 7.9. a) SET distributions measured at different values of V_2=0.9V+Δ_{V2}. (b)Average currents of the distributions plotted in Fig. a.

Surprisingly, a large current variation is observed not only on the SET distribution, but also on the RESET distribution. In fact, one should expect that the variation on the voltage applied to the GST (V_X) would induce a variation of the GST current, which is inversely proportional to the GST resistance. Because the GST resistance is at least 20 times higher in RESET state than SET state, the RESET distribution should vary of about 125nA and 550nA after electron proton irradiation, respectively. Nonetheless, it should be observed that the memory array is NOR-like and 2048 cells share the same bit line. Hence, if each cell selector has a leakage as low as 1nA, the overall contribution on the bit-line is already in the μA range. It should be noted that, if the selector has a leakage in the 1-10nA range, its equivalent resistance is much higher than a RESET GST, hence the effect of the GST resistance is negligible. Increased selector leakage can derive by several factors:

1) Oxide trapped charge (especially along the STI, inducing a parasitic conductance)
2) Increased subthreshold slope
3) Degraded drain junction

The third mechanism may come into play due to displacement damage [174], still this effect is somewhat smaller[22]. Oxide trapped charge and increased subthreshold slope are much likely to be the responsible of the increased drain leakage.

[22] In fact the non-ionizing energy loss is very small in our experiments [175].

The increased leakage on the entire bit line also explains the broadening of the primary peak shown in Fig. 7.8a and why the number of cells, which experienced a large current variation, is much higher than expected (1.5M vs 910k cells). At this purpose in Fig. 7.10a, we show the distribution of the differences between the GST currents measured before and after irradiation. We considered then the anomalous cells, which featured a current increase larger that 1 µA: the physical locations of these anomalous cells are shown in Fig. 7.10b, which clearly indicates that these cells share the same bit line of those cells, which were effectively irradiated. As a result, only a part of the selectors are effectively degraded, but their leakage is measured on all the cells sharing the same bit line.

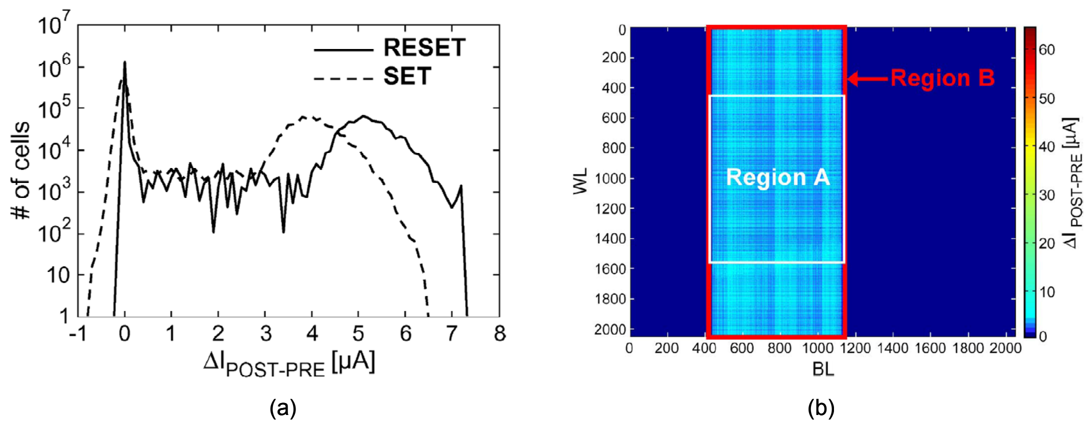

Fig. 7.10. a) Distributions of the differences between the currents read before and after 30-Mrad proton irradiation, for SET and RESET cells. B) Physical location of the cell featuring a current variation larger than 1µA. Only region A was irradiated, but all the cells of region B feature a large current variation. Region A and Region B share the same bit lines.

The irradiation on a small spot also allow to distinguish the effects of the increased read current due to positive charge trapped in M_1, and to the increased bit line leakage. In fact, no bit line selectors are irradiated in this case, hence the observed increased read current is due to the enhanced bit line leakage.

7.3.2 Permanent effects: programmability and annealing

To assess the effect of the ionizing radiation on the programmability of the GST film, half array was programmed with the inverse pattern, read and then restored, after each irradiation step (step 6-9 of Table 8). The results are summarized in Fig. 7.11-Fig. 7.13.

The trends of Fig. 7.11 and Fig. 7.12 match those ones observed in Fig. 7.5 and Fig. 7.6, indicating that there is no strong variation on the programmability, and that the increased currents on the distributions are due the same mechanism discussed in the previous subparagraph. There is a somewhat larger variation on the RESET cells. This is not surprising because, as already stated, immediately after a RESET operation, the cell features an initial lower resistance, which then drifts to its stable, higher value state. Conversely, those cells, which have not been reprogrammed, have been subjected to a

one-month storage time, and they feature a higher resistance. Fig. 7.13 shows the comparison between the reprogrammed cells (dashed line) and the cells, which were not reprogrammed (solid line), and negligible differences can be observed (a part the higher current in the RESET distribution, which arises from the absence of the 1-month storage time). In fact, SET and RESET voltages are not critical [47] and a 20-mV variation corresponds to less than 1% of the programming voltage.

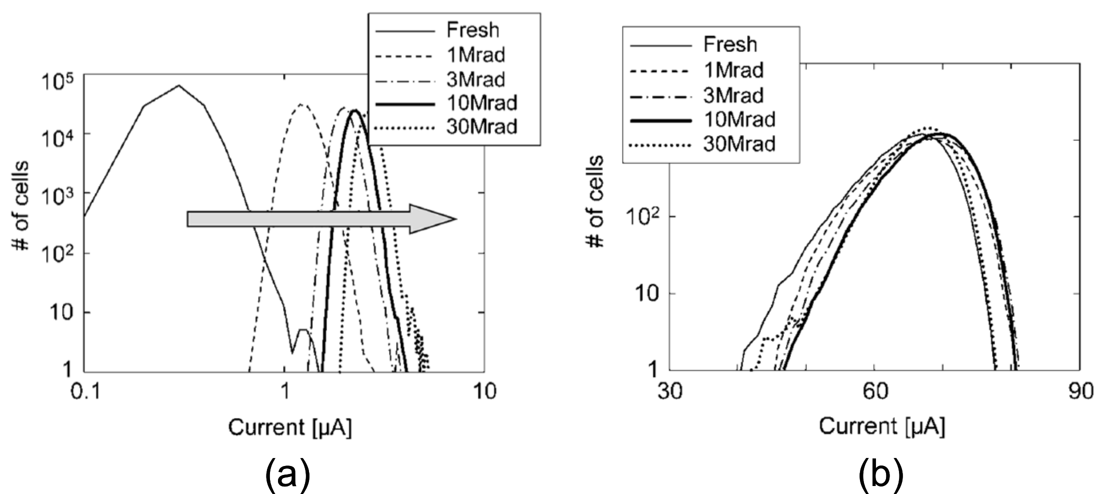

Fig. 7.11. RESET (a) and SET (b) distributions measured just after reprogramming the cells (step 7 of Table 8)

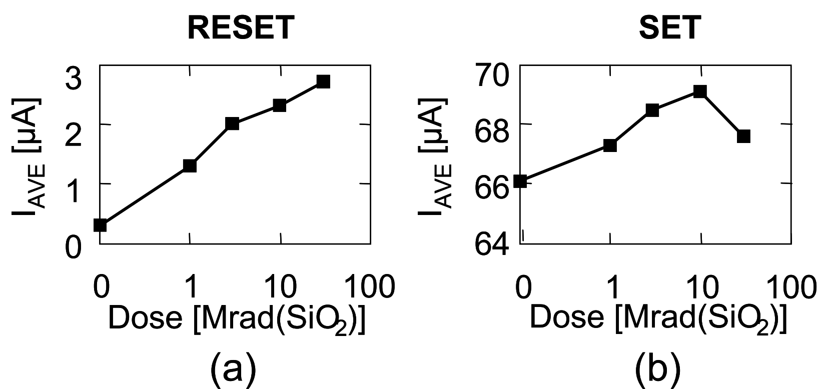

Fig. 7.12. Evolution of the average currents of Fig. 7.11 as a function of the irradiation dose. The average current of the RESET (a) distribution increases monotonically, while the cells in the SET (b) state feature a turn-over.

To assess if the trapped charge anneals, the devices were subjected to a one-month annealing. During this time, the devices were left floating and the current distribution was periodically measured. The distributions and the variations of the respective average values are shown in Fig. 7.14 and Fig. 7.15. As expected, the current decrease in time, indicating the progressive charge detrapping. Noticeably, in the SET distribution the average current returns to a value smaller than the fresh device. This is due to the degraded bit line selector characteristics, induced by interface traps which do not anneal. The permanent degradation is also responsible for the incomplete recovery of the original current value in the RESET distribution: the subthreshold slope of the

cell selectors does not recover to its original value, hence its contribution on the bit line leakage persists.

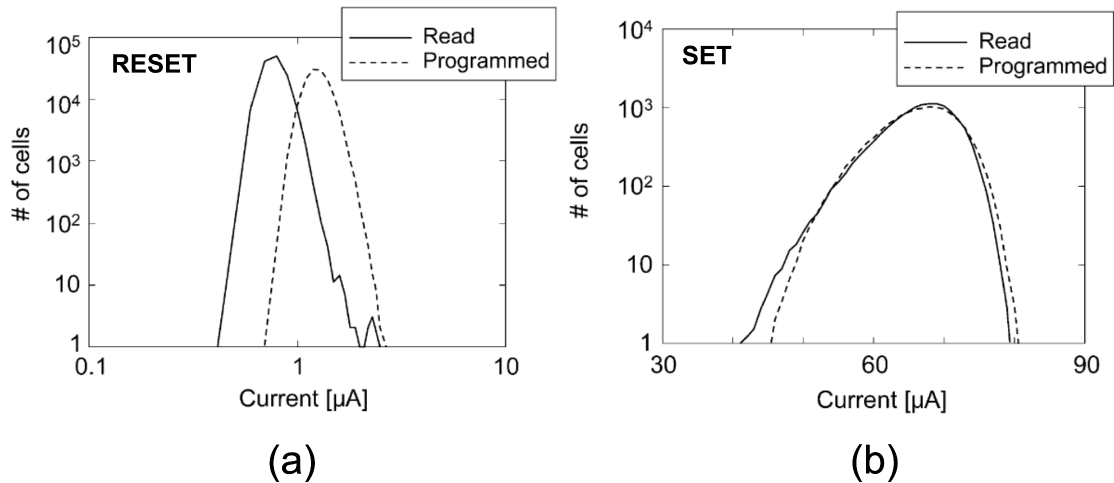

Fig. 7.13. Comparison between the distributions of the cells, which were not reprogrammed (read, step 5 in Table 8) and cells, which were reprogrammed (programmed, step 7 in Table 8)

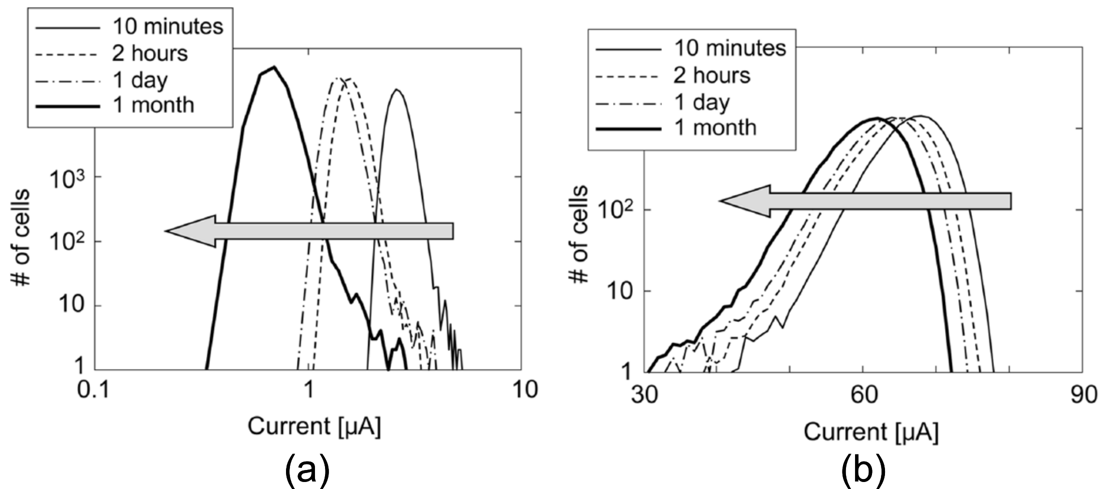

Fig. 7.14. RESET (a) and SET (b) distributions measured in different times after reprogramming (step 9 of Table 8) an array irradiated at 30 Mrad(SiO_2) with electrons.

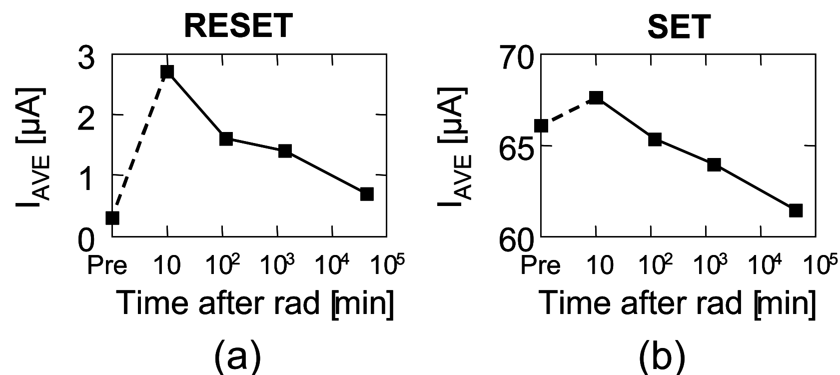

Fig. 7.15. Evolution of the average currents of Fig. 7.14 as a function of the irradiation dose.

It is also worth to remark that when all the die area is irradiated, the bit line selectors are irradiated as well. Hence, annealing reduces the trapped charge, leading to a strong variation on the SET distribution. A limited reduction of the SET and RESET current arises also from the reduced bit line leakage: as the trapped charge is removed from the oxide, the cell selectors, being in deep subthreshold region, feature a strong leakage

current reduction. Hence, even when only a part of the array is irradiated (i.e. when bit line selectors are not irradiated), a current reduction occurs, due to the reduction of the trapped-charge-induced leakage.

7.4 Comparison between BJT and MOSFET selectors

So far, only the radiation effects on PCM with MOSFET selectors have been shown. The results of proton irradiation performed on BJT-based arrays are summarized in Fig. 7.16. The irradiation has been performed on the entire die area. Noticeably, the SET distribution features exactly the same trend measured on the MOSFET based arrays. On the contrary the distribution of the RESET is much different: variations are much more limited.

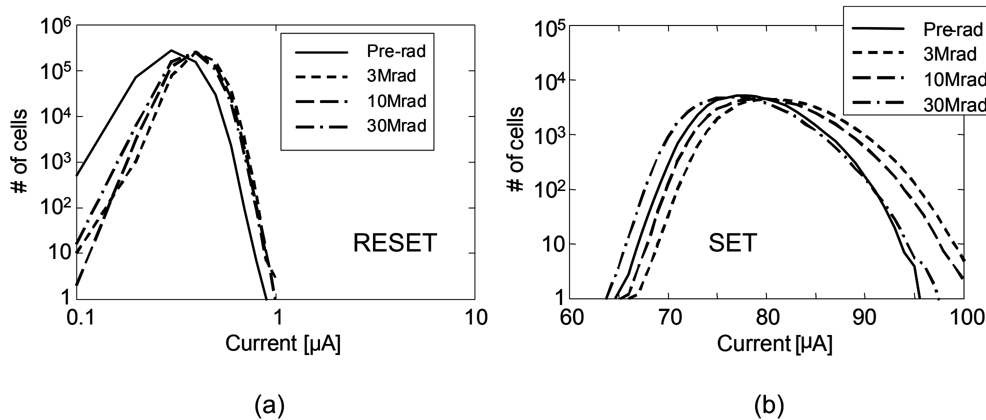

Fig. 7.16. RESET (a) and SET (b) current distributions measured on a BJT array, irradiated ad different doses, with 2-MeV protons. The whole die was irradiated.

The same trend measured on the SET distribution is a confirmation that the positive charge trapping on the bit line selectors (which is a MOSFET, even on BJT-based arrays) plays a dominant role on the increased current. Furthermore, the turnover confirms also that at high doses the permanent degradation becomes dominant. On the other hand, the limited current increase on the RESET distribution of BJT-based arrays confirms also that the positive trapped charge was responsible for the increased bit line leakage on MOSFET-based PCM, which affected also the RESET distribution on those devices. From this point of view, the absence of the MOSFET selector should grant a better immunity. However several considerations should be drawn:

1) BJTs are much less sensitive to ionizing radiation than MOSFETs, but only at high dose rates. In fact, at low dose rates (i.e. those normally encountered in a real operating environment), BJTs suffer from ELDRS (enhanced low dose rate sensitivity), as reported by various works [108]-[110].

2) On the contrary MOSFETs selectors, irradiated at very low dose rates, do not exhibit much variations. In fact, due to the relatively thin gate oxides, the charge anneals before it is accumulated at the levels required to induce an appreciable threshold voltage variation. Furthermore enclosed layouts [176],[177] strongly mitigate the increased leakage due to lateral charge trapping.

3) BJTs degraded by irradiation feature very reduced current gain. This is a concern when the cell must be programmed, because of the very high currents, which may be as high as 600μA per programmed cell[23]. If the gain is too reduced, the program operations could fail, due to the inability of the BJT (or to the charge pump, which generates V_3) to drive the required current. The reduced gain could also impact on the read operations, where currents as high as 100μA per active bit line may flow.

4) The careful selection of the reference current might avoid any increased leakage on the bit line selector.

7.5 Conclusions

Total ionizing dose effects were evaluated on phase change memories. The chalcogenide element seems to be very robust against total ionizing dose. The information stored is not corrupted even at very high doses, and the programmability is not compromised. Furthermore retention is not affected. The most sensitive part of the PCM memory is therefore the peripheral circuitry, which can be degraded by high dose levels, and which can be prone to positive charge trapping. The robustness of the GST elements is confirmed by other works in the literature [178]-[180].

Still, several open issues must be addressed, among the:

- The low dose effects on BJT selectors, and in particular the impact on the program operations.
- The heavy ion effects. Unfortunately the sensitive area of the PCM cell is much smaller than the effective cell area. Hence, to achieve a good statistics, a very high ion fluence should be used. However, with such that ion fluence, the peripheral circuitry and even the cell selector would be severely damaged, impeding to distinguish the effects on the GST from the effects on the MOSFETs. In fact, the cell selector sizes are $40F^2$ and $10F^2$ (f=180nm) for MOSFET and BJT based PCM, respectively, while the GST to heater interface[24] area is only $2000nm^2$. If only 20% of the sensitive elements are hit by one ion, each MOSFET and BJT selector would be hit by 130 and 32 ions, respectively. This very high number of ion hits would completely destroy the cell selector.
- The combined effects of radiation and temperature

Still, despite the strong robustness of the GST element, at least to total ionizing dose effects, PCM memories may suffer in all those environments, characterized by very harsh temperatures, either very high, or low, such as those encountered in satellite applications, space and avionics.

[23] Nonetheless, the programming operation is performed in parallel on 8 bits.
[24] The interface between GST and heater is where the information is actually stored, thus where it is the region where the ion strike should be most effective in degrading the information.

CHAPTER 8

Ionizing radiation effects on Ferroelectric memories

Ferroelectric memory (FRAM or FeRAM) is another advanced memory that, like PCM, is not based on the charge storage. FRAM, in fact, associates the information to the remanent polarization of a ferroelectric material. Since the equivalent capacitance depends on the remanent polarization, the information can be sensed with a number of methods. For more information, the reader may refer to chapter 2 and the references cited therein.

Being the information associated to the remanent polarization, which in turn depends on the positions of the atoms, FRAM does not suffer from charge loss, which is one of the biggest concerns on conventional Flash memories. Hence, FRAM might, in principle, used in radiation harsh environments. The high speed, single bit alterability and practically unlimited endurance could also make FRAM a suitable replacement for SRAMs, which, in turn, suffer from SEU. In fact, an alpha particle is enough to induce a bit flip on SRAMs [20]-[22].

Some early works on ferroelectric cells or capacitors assessed the good potentials of this technology in terms of radiation robustness [55]-[59]. However, these works were based on very old technologies or they consisted only on ferroelectric capacitors. Besides that, no evaluation of the effects on the peripheral circuitry was performed. Furthermore, the study of the combined effects of temperature and irradiation is a field, which is still unexplored. In this chapter the radiation effects will also be evaluated at different temperatures. The main aspects will be the immediate data corruption, the radiation damage dependence on the temperature, the damage recovery following cycling and high temperature annealing and the bias effects. A model will also be provided, which also accounts for the irradiation temperature dependence.

8.1 Experimental setup

Throughout this study, 90 commercial Ramtron FM18L08 FRAM chips were analyzed, featuring 32k × 8 bits, operating at 3.3V, and with PDIP package. The data access and addressing is the same as an asynchronous SRAM. The cell structure is similar to the standard DRAM with 1 transistor and 1 storage capacitor, which employs a PZT ferroelectric film [181]. The PZT thickness is 200nm and the PZT density is $8.6 g/cm^3$ [182].

The irradiation experiments were performed at the Laboratori Nazionali di Legnaro INFN - LNL, Italy, using 10-keV X-Rays and a 5-MeV proton beam. The samples were irradiated both unpowered (with grounded terminals) and powered, in order to establish the effect of supply voltage on the radiation damage. Irradiations were performed at different temperatures ranging from -15°C to 140°C, using ad-hoc instrumentation developed for high and low temperature radiation testing (see Appendix D). Before irradiation the devices were chemically delidded to expose the die for the proton irradiation, and to avoid the X-Ray attenuation due to the packaging materials, which is all but negligible, as it will be shown in the experimental results section.

8.2 Experimental Results

8.2.1 Immediate irradiation effects on unpowered devices

In order to assess the immediate radiation effects, we irradiated FRAM chips at different temperatures and with different memory-patterns. The experimental procedure is depicted in Fig. 8.1. FRAMs were initially programmed with a given pattern and then irradiated. To assess any pattern dependence on the irradiation effects, we used different irradiation pattern, listed in Fig. 8.1.

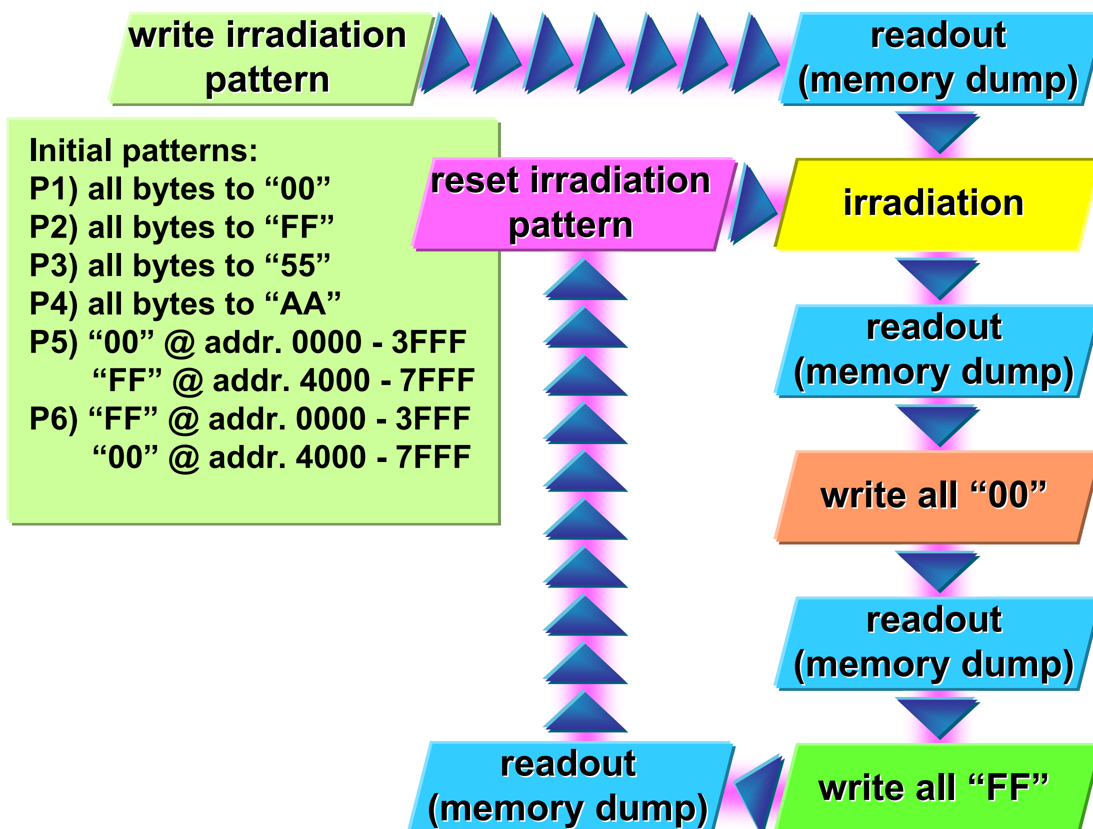

Fig. 8.1. Irradiation experimental procedure. The devices have been programmed with a given pattern before irradiation. Irradiation has been periodically stopped to perform the memory characterization.

Irradiation was periodically stopped to perform the memory characterization. Each characterization cycle was performed at 85°C, which is the maximum operating temperature [181], and it consists of the following steps:

1) readout immediately after irradiation;

2) set all bytes to "00" and memory readout, to assess if there are any stuck bits at 1;

3) set all bytes to "FF" and memory readout, to assess if there are any stuck bits at 0;

4) reset of the initial irradiation pattern and memory readout.

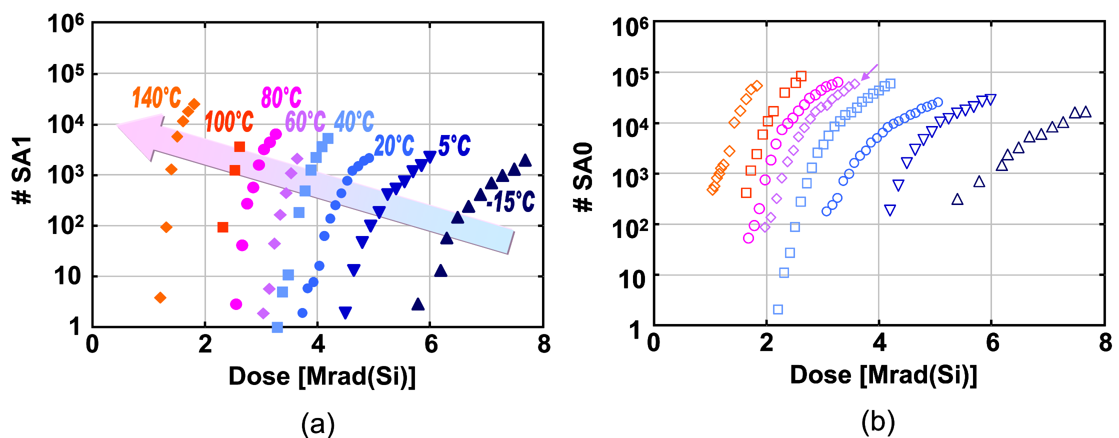

Fig. 8.2. Number of SA1 (a) and SA0 (b) as a function of irradiation dose in different samples irradiated at different temperatures from -15°C to 140°C.

The prompt effects of X-ray irradiation are summarized in Fig. 8.2. Immediately after each irradiation step we did not measure any bit flip, indicating that irradiation is unable to corrupt the stored information, at least at doses as high as 8Mrad(Si). Instead, from the readout of steps 2 and 3 we observed an increasing number of stuck bits during irradiation. In the following, we will refer to SA0 (Stuck At 0) as a bit that is fixed at "0" and it cannot switch to "1", independent of the new programmed value. Similarly, we refer to SA1 as a bit permanently fixed at "1" and unable to switch to "0". Fig. 8.2 shows the evolution of the stuck bit number as a function of radiation dose and irradiation temperature. Noticeably, there is a perfect correlation between the irradiation pattern and the logical value a bit is stuck at. For instance, all samples in Fig. 8.2 were initially programmed with pattern P5, and all the SA0 bits in Fig. 8.2a belong to addresses 0000-3FFF (i.e., those programmed at "00"), while the SA1 bits belong to the portion of memory programmed at "FF" (addresses 4000-7FFF). Such correlation between the initial programmed value and the value a bit is stuck-at is independent of the initial pattern programmed before irradiation. Given the irradiation dose, the number of SA0 and SA1 bits increases with increasing irradiation temperature.

Fig. 8.3 shows the comparison between proton and X-ray irradiation, for two irradiation temperatures (20°C and 80°C). Again, we never observed any bit-flip during irradiation up to 9 Mrad(Si).

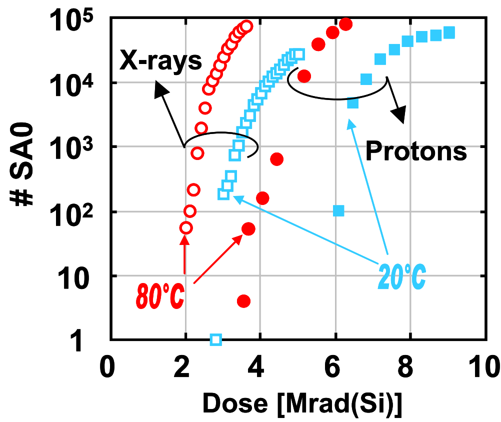

Fig. 8.3. Comparison between proton and X-ray irradiations at two different irradiation temperatures (20°C and 80°C).

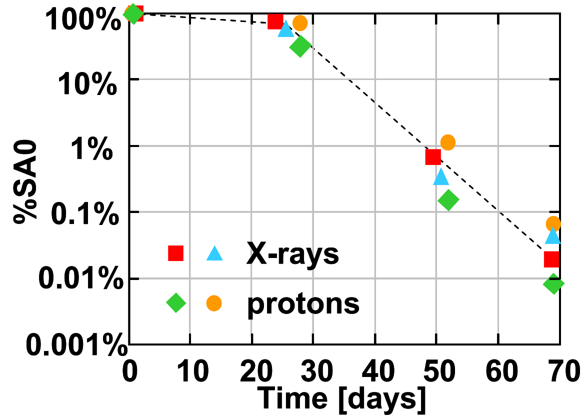

Fig. 8.4. Spontaneous recovery of the stuck bits (SA0) as a function of time at room temperature after X-ray and proton irradiations. The dashed lines are to guide the eyes.

8.2.2 Radiation damage recovery

In order to assess the damage stability, we performed annealing and cycling experiments. In Fig. 8.4 we show the spontaneous reduction of the SA0 and SA1 as a function of time at room temperature. The devices were kept unbiased for a time as long as 70 days. The ionizing radiation damage is almost stable at room temperature over a time as long as 30 days. Later, the radiation damage progressively anneals, approximately with the same rate independent of the radiation source (X-rays or protons).

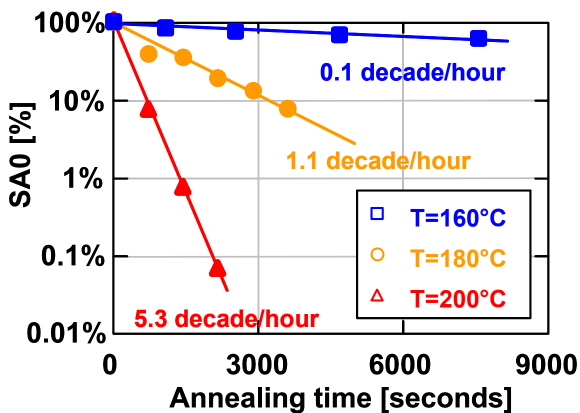

Fig. 8.5. Evolution of the SA0 and SA1 bit number during cycling experiments. The upper x-axis represents the time elapsed during cycling.

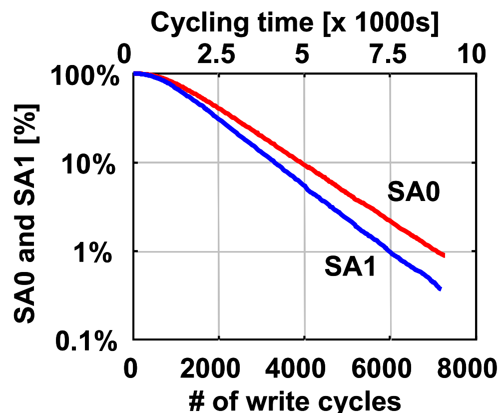

Fig. 8.6. Recovery of SA0 (in percentage with respect to the initial value) as a function of the annealing time at different temperatures. For each curve, we show the decrease rate (in decade/hour).

The recovery time is substantially reduced either if the device is subjected to repeated write/read cycles or if the device is kept at moderately high temperature. Fig.

8.5 shows the evolution of SA0 and SA1 bits as a function of the number of program operations during the cycling experiments. All bytes of the device were repeatedly programmed, switching between 00 and FF.

The radiation damage recovers much faster with a high temperature annealing, even if the devices are kept unbiased. The devices were irradiated at 80°C up to 3.4 Mrad(Si), and then they were subjected to annealing at 160°C, 180°C, and 200°C. Annealing was periodically stopped to measure the FRAMs at 85°C. Fig. 8.6 shows the evolution of the SA0 and SA1 bits as a function of annealing time and temperature. After the annealing steps of Fig. 8.6, we subjected the samples to a one-hour 300-°C annealing, and the recovery was complete, i.e. no stuck bits were observed.

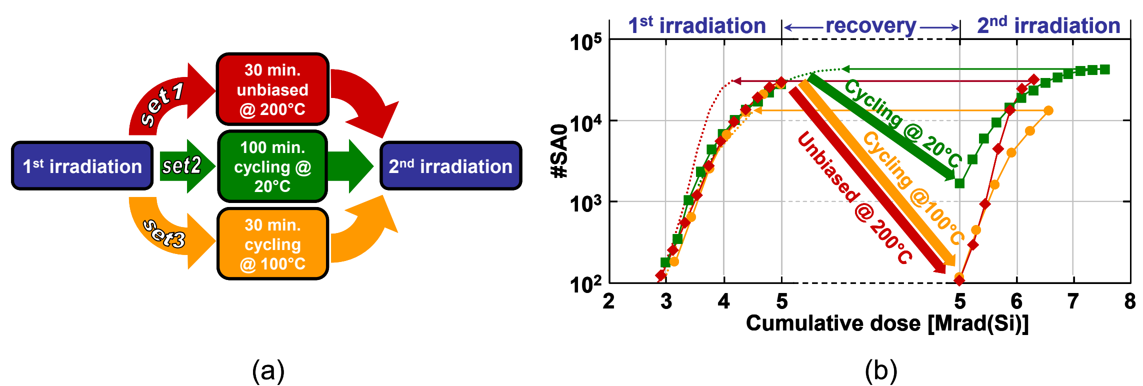

Fig. 8.7. a) Experimental procedure for evaluating passivation/depassivation rate of PZT defects and trapped charge during annealing and cycling. b) SA0 evolution during the first and second X-ray irradiation.

To further understand the stuck bit stability, we performed the experiment illustrated in Fig. 8.7a. We defined three sets of samples (we will refer as set1, set2, and set3 in the following). First, all sets were identically irradiated up to a total dose of 5 Mrad(Si) at 20°C. Then, set1 was annealed unbiased at 200°C for 30 minutes, reducing the SA0 number to the 0.3% of its initial value. Instead, set2 was subjected to 100-minute cycling at 20°C and set3 was subjected to 30-minute cycling at 100°C. Finally, all samples were irradiated again. The same memory characterization of Fig. 8.1 was carried out during both irradiation steps.

Fig. 8.7b shows the SA0 bits detected during the irradiations in the samples of set1, set2, and set3. The second irradiation is able to generate again the SA0 bits recovered by the annealing or cycling, as expected. However, if we shift the SA0 growth curve of the second irradiation so that it overlaps with the first irradiation, the annealed samples from set1 exhibit a faster growth kinetics than the cycled samples of set2 and set3.

8.2.3 Bias and packaging effects

Fig. 8.8 shows the evolution of SA0 as a function of the ionizing dose during X-ray irradiation at 20°C and 60°C for two powered and two unpowered devices. The powered devices were irradiated in stand-by. The degradation of powered devices is

roughly 10 times faster than in the unpowered devices. If the device is powered during X-ray irradiation, it maintains the complete functionality (without read/write errors) up to 280krad(Si). Later, some failing bits appear, but the read/write operations are still possible in the remaining cells. After 400krad(Si), the device suddenly stops working, i.e., read/write operations fail in all 256k cells. Proton irradiation gave similar results. To investigate the bias effects, we performed the following experiment: we irradiated some devices applying a 2-mm lead shield with a small circular hole, in order to irradiate only a small array region. One half of the devices were powered and one half were unpowered during irradiation. The results were compared with those obtained in the same conditions but without the shield. In Fig. 8.9, we show the logical positions of the failing bits in four devices irradiated in different conditions (powered/unpowered, shielded/unshielded). If the device is irradiated unpowered, the failing bits appear only within the irradiated region and they feature a random distribution (see Fig. 8.9b and Fig. 8.9d). On the contrary, if the device is powered during irradiation, the failing bits are mostly arranged along rows and columns, and they appear also outside the irradiated region (see Fig. 8.9c).

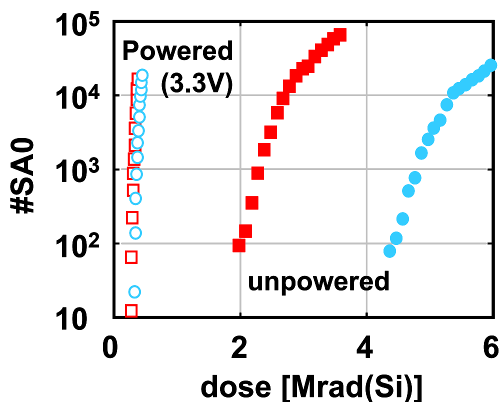

Fig. 8.8. Evolution of SA0 as a function of X-ray dose during irradiation at 20°C and 60°C for two powered and two unpowered devices.

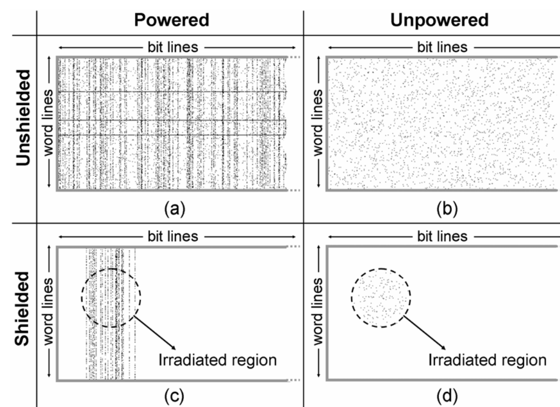

Fig. 8.9. Logical position of the failing bits (in black) in four devices irradiated with different conditions: powered (a,c) / unpowered (b,d), unshielded (a,b) / shielded (c,d) (only half bit lines are shown).

To assess if the damage induced by bias can be annealed, we subjected the samples irradiated powered to the same one-hour 300-°C anneal, previously performed on some devices which were irradiated unpowered (see previous subparagraph). The recovery was not complete, indicating that the damage is permanent if the device is irradiated when powered.

Finally, to evaluate the packaging effects and the X-Ray attenuation, we performed radiation tests at room temperature on packaged, delidded and partially delidded devices. We used the same setup described in the previous sections. The results show that 0.6-mm and 1.4-mm of packaging material attenuate the radiation effects by a factor of 2.5 and 11.8, respectively, corresponding to 0.63-mm attenuation length.

8.3 Discussion

8.3.1 Role of the peripheral circuitry degradation

Ionizing radiation exposure degrades both the memory cell array and the peripheral circuitries. Even though we cannot directly access to each single block (decoders, sense amplifier, memory array, etc.), the behavior of the irradiated devices gives us some information about what block is the most degraded by irradiation. In principle, the memory chip degradation may be ascribed to the following circuitries:

1) Row decoders, column decoders, plate line selectors, sense amplifiers. In this case, we expect clusters of failing bits along rows and/or columns.

2) Pass-transistor cell selector. The cell selector may show: the increase of the leakage current in subthreshold region, the threshold voltage variation, and the transconductance reduction. The leakage current may induce a voltage drop on the selector, which might affect the program operation. This current should flow across the bit line even though the cell is not selected. However, to achieve a sufficient voltage drop, such leakage current should be so high that it would induce a read disturb on all the cells connected to the same bit line. This would produce a cluster of failing bits along the entire bit line, which is not observed in our device, if they are irradiated unpowered. Moreover, several reports in the literature (see for instance [183]) show that in sub-micron MOSFETs the threshold voltage changes by less than 100mV, the transconductance is only marginally affected, and the off-state current is less than 100nA even after 30Mrad(Si) irradiation.

3) The PZT. The failing bits are related to some changes in the PZT hysteresis loop. Due to the cell to cell characteristics dispersion, we expect that the failing bits are uniformly and randomly distributed within the irradiated region.

4) ESD protections, control circuitry, I/O circuitry. At low irradiation doses, the degradation of the ESD protections and the other circuitries may contribute to the increase of the stand-by and operating currents (I_{DD}) together with the decoders and sense amplifiers [184]. Despite the I_{DD} increase, which may exceed the specification values, our devices are still fully functional, i.e., no read/write errors occur at least up to 280krad(Si), if the devices are irradiated powered (see Fig. 8.8). If the degradation of the control circuitry exceeds a critical level, we expect the complete functional failure of the memory chip. In our devices, this occurs after 400krad(Si) irradiation, if the device is powered during irradiation. Noticeably, FRAM devices do not have any charge pumps. This explain the increased robustness with respect to conventional flash memories, which start failing at doses as low as 10-20krad due to the charge pump degradation [133].

Based on the results of Fig. 8.9, we never observed any row or column of failing bits, when the device is irradiated unpowered, indicating that the failing bits are mostly due to the PZT degradation. On the contrary, rows and columns appear, if the devices

are irradiated powered. Taken together with the results of Fig. 8.8, this fact suggests that the read errors of the powered devices derive from the accelerated degradation of the peripheral circuitry, which evolves much faster than the degradation of the PZT. In fact, even though the chip is powered, it is irradiated in stand-by. Hence, the memory cells are always at a high impedance state, independent of the bias conditions during irradiation. On the contrary, the peripheral circuitry is biased only when the chip is powered and the high electrical fields may accelerate the irradiation damage.

Of course, we cannot exclude that the peripheral circuitries is also degraded in unpowered devices. In fact, the I_{DD} increase is a clear signature of the degradation of the peripheral circuitry (such as the row/column decoders, the sense amplifier, etc). In addition, the degradation of the peripheral circuitry might strongly affect important parameters such as the memory access time, which were not considered in this study. However, the peripheral circuitry degradation cannot be the major responsible of the stuck bits in unpowered devices. This is in agreement also to some previous findings [184], which reports that FRAM peripheral circuitry is still working after several Mrads(Si), if irradiated unbiased. Noticeably, in [184] the powered device started having errors around 12.5krad(Si), which is a much lower dose than in our devices. This is not unexpected, because the devices used in [184] were powered at 5V, leading to a more accelerated degradation than in our devices.

As a last remark, the 300-°C annealing show different effects between the devices, which were irradiated powered and those, which were irradiated unbiased. As it will be discussed later, the complete recovery of the devices irradiated unbiased suggest that the radiation damage when high electric fields are not present is much less severe or it has a different nature. When the powered devices are irradiated, the radiation-generated hole-electrons pairs could be accelerated by the high electric fields[25], becoming hot and degrading the silicon-oxide interface by generation of interface traps. Those traps in turn, may not anneal as fast as positive oxide trapped charge, during the 1-hour 300-°C annealing.

8.3.2 PZT degradation in unpowered devices

The behavior of the SA0 and SA1 bits as a function of irradiation dose and temperature can be explained by the photo-induced fatigue-like and imprint-like phenomena of the ferroelectric material. It has been shown in the literature that X-ray and UV irradiations on ferroelectric capacitors affect the remanent polarization ($P_{R\pm}$) in two ways [185]-[188], which are schematically depicted in Fig. 8.10. On one hand, the hysteresis loop width (i.e., the difference between the P_{R+} and P_{R-}) decreases, due to the charge trapping in the volume of the ferroelectric and the consequent domain wall pinning [57],[59],[187],[188]. This produces the fatigue-like phenomenon. On the other hand, if the capacitor is pre-poled with P_{R+}, during irradiation the ferroelectric hysteresis

[25] Especially on the MOSFET in OFF state, which typically have the highest drain-to-source voltage applied.

loop shifts from right to left (see Fig. 8.10b), due to charge trapping at the ferroelectric/electrode interface [57]. The opposite shift occurs by pre-poling the ferroelectric with P_{R-} (see Fig. 8.10c). This is responsible for the imprint-like phenomenon. The combined effects of the fatigue-like and the imprint-like phenomena translate into a reduction and a shift of the hysteresis loop.

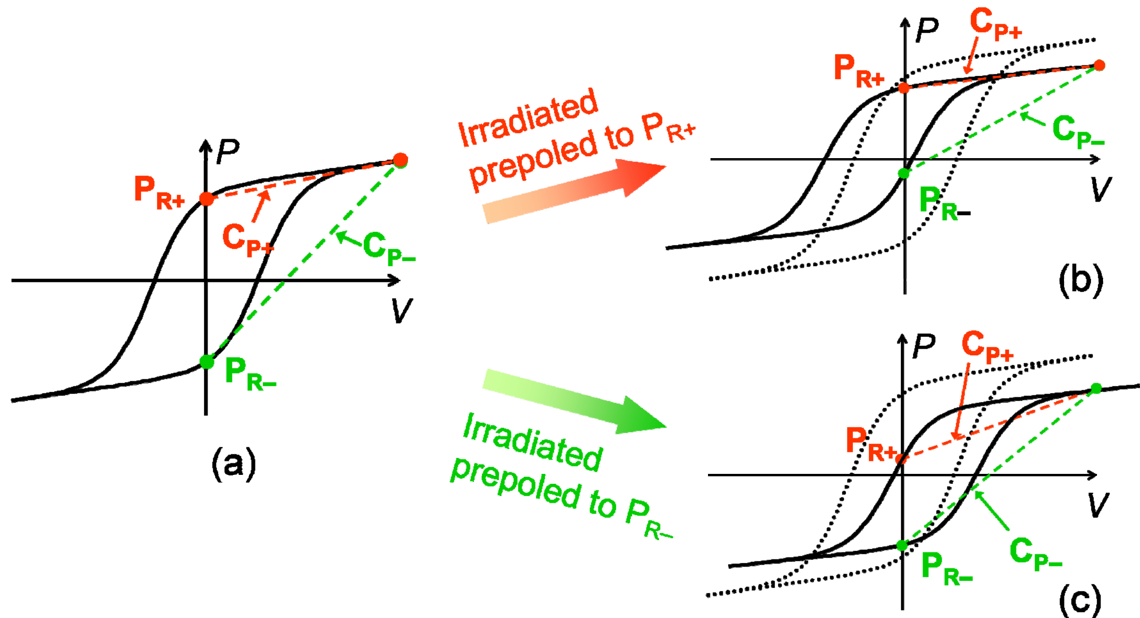

Fig. 8.10. Schematic representation of the radiation induced effects on the hysteresis loop of a ferroelectric: a) fresh ferroelectric loop and equivalent ferroelectric capacitance values C_{P+} and C_{P-} associated with the remanent polarization values P_{R+} and P_{R-}, respectively. b) Reduction and shift of the hysteresis loop after irradiation of a capacitor prepoled to P_{R+} (solid = irradiated; dotted = fresh); c) Hysteresis loop variation of an irradiated ferroelectric capacitor prepoled to P_{R-} (solid = irradiated; dotted = fresh).

In the FRAM cell the binary information is stored into the ferroelectric equivalent capacitance value (C_{P+} or C_{P-}), which in turn depends on the remanent polarization (P_{R+} or P_{R-}). The reduction and shift of the hysteresis loop affect the two capacitance values $C_{P\pm}$. Let us consider, for instance, a cell prepoled with P_{R+} (see Fig. 8.10b). After irradiation, the hysteresis loop reduces and shifts leftward (from dotted to solid line). This produces marginal changes in the capacitance C_{P+}, but the capacitance C_{P-} reduces more strongly. If the degradation of the hysteresis loop is high enough, the capacitance C_{P-} becomes too small and the P_{R-} state cannot be distinguished from P_{R+} (resulting in a stuck bit). The opposite occurs if the capacitor is prepoled with P_{R-}.

We found that the stuck bit number increases, if the operating temperature during measurements increases. In fact, the hysteresis loop width reduces with increasing temperature [189] and, consequently the difference between C_{P+} and C_{P-} decreases. To avoid this problem, the memory characterization has been done at 85°C independent of the irradiation temperature. Consequently, the data in Fig. 8.2 and Fig. 8.3 can be explained only by the radiation damage dependence on the irradiation temperature. We postpone the detailed discussion until the following section.

At the same irradiation dose, X-ray irradiation generates a larger amount of stuck bits than proton irradiation. This is due to the dose enhancement effects caused by the high-Z metals in the silicides [76] and, above all, in the PZT ferroelectrics, which contains 60.7% of lead [182].

The radiation-induced damage is reversible. In [190] it has been shown that some ferroelectric materials, such as SBT, are prone to a rejuvenation of the hysteresis loop when subjected to repeated electrical cycling. Instead, PZT has been reported to be less prone to restoration [185],[190]. Nonetheless, we observed a significant reduction of the number of stuck bits, due to the partial recovery of the radiation damage. This suggests that PZT is moderately degraded with our irradiation doses, and then a partial recovery is still possible. In fact, in [57] it has been shown that some PZTs can survive at doses in the 1-10Mrad(Si) range, depending on the fabrication process.

The irradiation induced fatigue and imprint in PZT based capacitors is due to trapping of photogenerated charge at the domain boundaries. We can argue that this charge is hardly removed if the device is kept unbiased at room temperature (see Fig. 8.4). We can tentatively suppose that these charges are stably trapped in energetically-deep defects at room temperature, being very difficult to escape. Moderate unpinning of the domain walls occurs during electric field cycling, because the domain walls are strongly pinned by the electronic trapped charge. However, the charge detrapping and domain wall unpinning is substantially accelerated at high temperatures. For instance, the stuck bit number reduces at 1% after 9000-seconds cycling at room temperature. This time reduces to 1400 seconds performing a 200-°C annealing (see Fig. 8.6), even though the device is kept unbiased. These data must be compared with the room-temperature annealing (Fig. 8.4), which takes 50 days to reduce the stuck bit at 1%.

Based on the results in Fig. 8.7, after annealing the PZT lattice structure is not recovered as it was before irradiation, but some defects are “patched”, leading to a structure weaker than the original one. It is worthy of remark that the final weak bond generated during the annealing is a metastable structure, which can be easily broken again by the second irradiation (set1 in Fig. 8.7b). On the contrary, in the samples from set2 the second irradiation kinetics perfectly overlaps the first irradiation curves, suggesting that the PZT defects are completely recovered, even though the cycling was carried out at room temperature. This suggests that, even though high temperature annealing is more effective than cycling in neutralizing the positive trapped charge (compare Fig. 8.5 and Fig. 8.6), the domain orientation switching, and the consequent lattice reorganization play a key role in the defect recovery. In fact, the 2-hour annealing at 160°C in Fig. 8.6 recovers the stuck bit only marginally, while a short cycling (30 minutes) at moderately high temperature (100°C) can completely rejuvenate the PZT.

8.4 Degradation Model

The reliability of FRAM memories is related to the positive charge trapping, which affects the remanent polarization inducing imprinting and fatigue. We showed that temperature strongly affects the degradation kinetics (see Fig. 8.2 and Fig. 8.3).

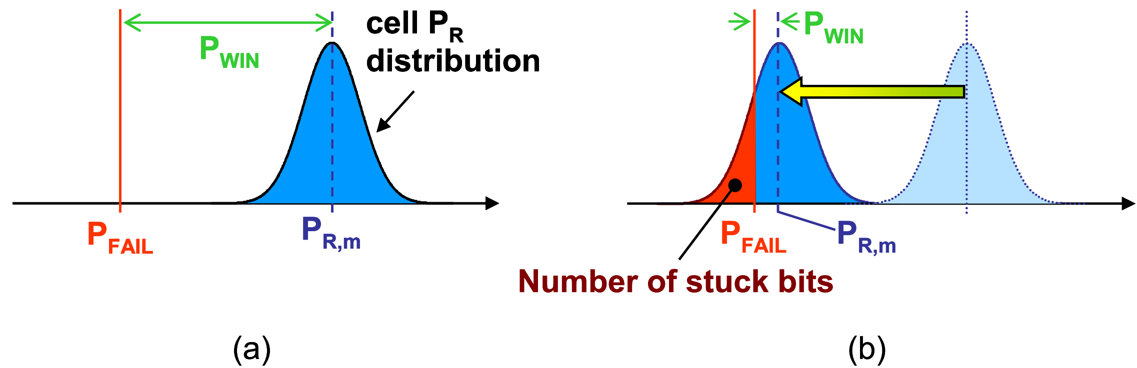

Fig. 8.11. Schematic representation of the degradation model: a) the remanent polarization of the FRAM cells have a Gaussian distribution with mean value $P_{R,m}$. P_{FAIL} is the critical polarization value, which denotes the failure of FRAM cell. b) Irradiation effects on the polarization distribution. Stuck bits are detected when the tail distribution goes beyond P_{FAIL}.

The major difficulty encountered while developing the model is the impossibility of a direct measure of the remanent polarization, because we are dealing with commercial devices. To overcome this limit, we followed a statistical approach and we made the following considerations:

1) Each memory cell fails when the hysteresis loop reaches a given degradation level. This may occur either if the ferroelectric loop width is sufficiently reduced, or if the hysteresis loop shift reaches a critical value (leftward or rightward, depending on the prepole bias as shown in Fig. 8.10), so that the imprint occurs. Hence, we can identify a critical polarization value P_{FAIL}, representing the minimum remanent polarization needed by the sensing circuitry to retrieve the correct binary information from the ferroelectric polarization.

2) Because we are performing total ionizing dose experiments and the ferroelectric capacitor area is 13.2µm^2 [182], the radiation induced fixed charge and defects are expected to be uniformly distributed in the ferroelectric film. In addition, the large ferroelectric thickness (200nm) makes negligible the effects of charge neutralization near the interfaces. Consequently, the shift and the width reduction of the hysteresis loop are supposed to be proportional to the bulk positive charge trapping in the ferroelectric.

3) The remanent polarization of the cell among the array has a Gaussian distribution with a given mean value $\pm P_{R,m}$ and a given standard deviation σ (see Fig. 8.11a). As first approximation, we assumed that the radiation-induced charge trapping modifies the remanent polarization by shifting the distribution, with neither stretching the Gaussian shape, nor generating any tail in the cell distribution, as schematically depicted in Fig.

8.11b. This assumption is reasonable, because we are performing total dose experiment, so that we can argue that all cells are uniformly degraded.

4) The defect recovery can be neglected up to the maximum irradiation temperature (140°C). This is experimentally verified by the data of Fig. 8.6.

Following these assumptions, the percentage of failing cells in the memory array is given by:

$$f = \int_{-\infty}^{P_{FAIL}} \frac{1}{\sqrt{2\pi}\sigma} \exp\left[-\frac{\left(P - P_{R,m}\right)^2}{2\sigma^2} \right] dP = \\ = \frac{1}{2} + \frac{1}{2} erf\left(\frac{P_{FAIL} - P_{R,m}}{\sqrt{2}\sigma} \right) = \frac{1}{2} + \frac{1}{2} erf\left(\frac{P_{WIN}}{\sqrt{2}\sigma} \right) \quad (8.1)$$

In the above expression, we defined a polarization window P_{WIN} (see Fig. 8.11) as the difference between the critical polarization value P_{FAIL} and the average remanent polarization of the cell array $P_{R,m}$, by analogy with the programming window of the Flash memory. P_{WIN} is supposed to decrease linearly with the radiation-induced trapped charge.

We model the positive trapped charge build-up as follows: irradiation generates a number of electron-hole pairs. We define *H* the number of free holes, which survive the prompt recombination. A part of the generated holes is trapped in precursor defects, giving rise to the positive charge trapped *Q*. In turn, the number *N* of these precursor defects includes both the process-induced and the radiation-induced defects. Hence, *N* increases with increasing the irradiation dose.

The increment of free holes *dH* in the time interval *dt* may be written as:

$$dH = a \cdot r \cdot dt - b \cdot H \cdot dt - \frac{dQ}{q} \quad (8.2)$$

In (8.2) a is the number of generated holes per unit dose, r is the dose rate, b is the fraction of holes escaping from the ferroelectric or neutralized/recombined in the time interval *dt*, *q* is the elementary charge, and *dQ/q* represents the number of holes that become trapped in the precursor defects during *dt*.

Similarly to that reported on the irradiation of gate oxides [104], it is conceivable that the irradiation-induced defects responsible for charge trapping come from microstructural transformations of charged defects generated by irradiation, which are field-sensitive. For instance, a neutral trap in silicon dioxide could result from a hole capture at a weak Si-Si covalent bond, which may relax into a Si:- Si+ neutral amphoteric defect, after the hole compensation. Extending this interpretation to ferroelectrics, we can tentatively argue that, during their motion in the ferroelectric, holes may be trapped in weak or dangling bonds especially at the domain boundaries. The detrapping or neutralization of a fraction of them could leave a neutral defect,

which in turn behaves as a precursor for fixed positive charge trapping. Following this interpretation, the defects growth rate is proportional to the number of free holes in the ferroelectric, without saturating, at least for irradiation doses up to 10Mrad(Si). In other words, the defects growth kinetics may be written as:

$$dN = d \cdot H \cdot dt \qquad (8.3)$$

where *d* have the meaning of defect generation probability.

Some free holes may be permanently trapped into the precursor defects at a rate that is proportional to the number of free holes (*H*) and the number of empty defects (*N*-*Q*/*q*):

$$dQ = c \cdot \left(N - \frac{Q}{q} \right) H \cdot dt \qquad (8.4)$$

where the constant *c* accounts for the hole trapping probability.

From (8.2)-(8.4) we obtain the following system of ordinary differential equations:

$$H' = a \cdot r - b \cdot H - \frac{Q'}{q}; \quad N' = d \cdot H; \quad Q' = c \cdot \left(N - \frac{Q}{q} \right) \cdot H; \qquad (8.5)$$

Fig. 8.12 shows a sample solution of (5) calculated with initial conditions $H(0) = 0$, $Q(0) = 0$, $N(0) = 0$.

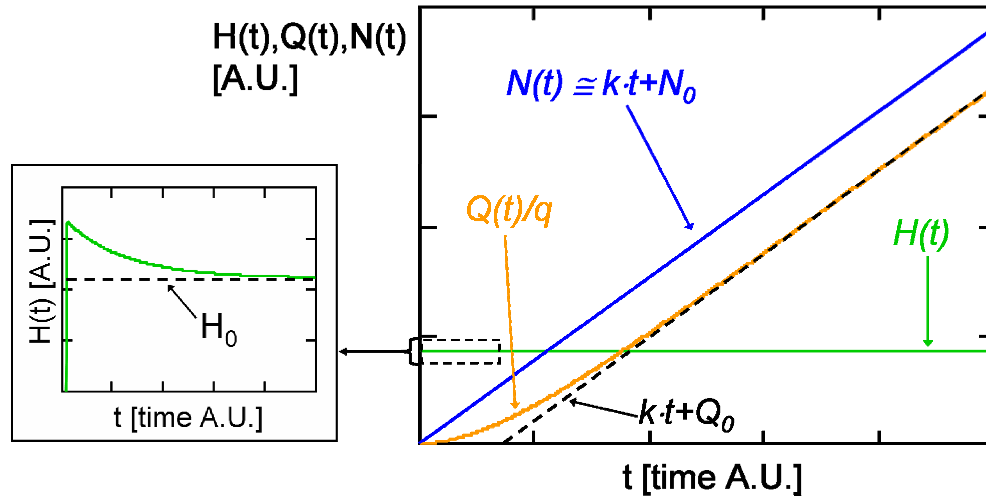

Fig. 8.12. Example of the solution of the system in (8.5). *Q*(*t*)/*q* and *N*(*t*) asymptotically approach two straight lines with the same slope value. As shown in the inset, *H*(*t*) saturates at a constant value H_0.

Once irradiation starts, the free hole density increase rate is obtained combining (8.2) and (8.4):

$$H' = a \cdot r - \left[b + \frac{1}{q} c \cdot \left(N - \frac{Q}{q} \right) \right] \cdot H \qquad (8.6)$$

Because $N > Q/q$, the time constant is smaller than $1/b$. Hence, b provides an upper bound of the H transient length. The constant b is approximately the hole escape rate from PZT and it is correlated to the hole mobility in PZT, which is reported in the range of 10^{-5}-10^{-6} cm^{2}V^{-1}s^{-1} [191]. Just with a PZT electric field as small as 100V/cm, the holes drift out of the 200-nm PZT layer in a time as short as 100ms. Being the minimum irradiation time in the 100-s range, we can correctly assume that the transient fades in less than 1s and the free hole density is mostly constant during irradiation.

Once the H transient is over, H tends to its regime value (H_0) and N linearly increases, (see Fig. 8.12). For larger t values Q asymptotically tends to a straight line with the same slope than N. The asymptotic slope (k) of Q and N is calculated from the model parameters as:

$$k = \frac{a \cdot r}{1 + b/d} \qquad (8.7)$$

After solving (5) for $Q(\phi)$, we write the variation of P_{WIN} as:

$$P_{WIN}(\phi) = P_{WIN}(0) - \alpha \cdot Q(\phi) \qquad (8.8)$$

and we insert (8.8) into (8.1). α is the proportionality constant correlating the trapped charge with the remanent polarization variation, and $\phi = r \cdot t$ is the radiation dose. Fig. 8.13 shows the good fit between experimental data and model. Fig. 8.14 shows the evolution of the slope k (in arbitrary units), which features an Arrhenius-like trend as a function of the irradiation temperature, with activation energies 0.093eV and 0.085eV for SA0 and SA1 bit, respectively.

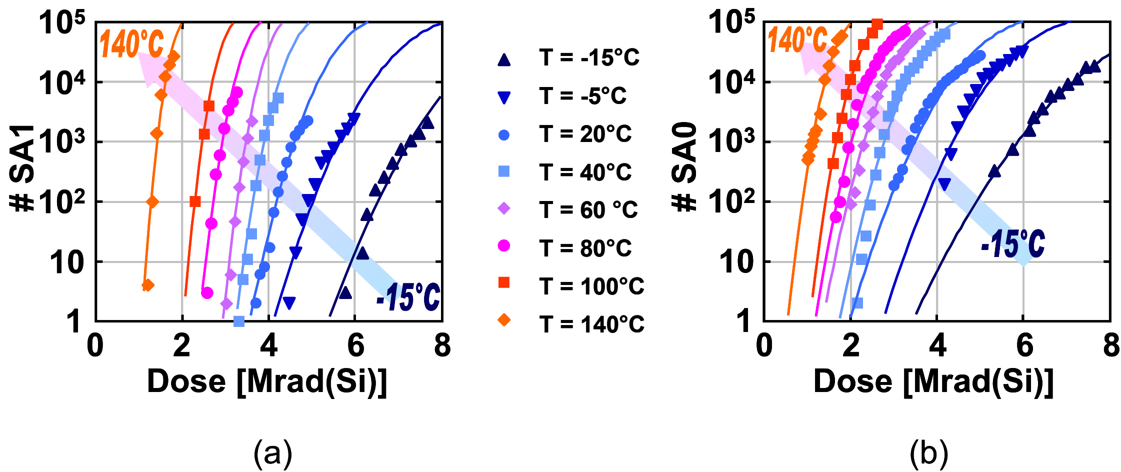

Fig. 8.13. Evolution of the SA0 and SA1 bits as a function of temperature and dose: comparison between model (lines) and experimental data (symbols).

Noticeably, by analyzing the model parameters, the irradiation temperature mostly affects the positive trapped charge build-up, which becomes faster as the temperature increases. Equation (8.7) indicates that the k variation mostly depends on the b/d ratio. In fact, all the irradiations have been done at a constant dose rate r = 600rad(Si)/s, and

the parameter *a* is expected to be almost constant, because it is correlated with the number of holes generated by the irradiation. Such number mostly depends on the target material energy-gap and the radiation source energy, and it may be considered only marginally affected by the temperature. The increase of stuck bits should correlate with the decrease of the *b/d* ratio, instead. This may be due either to the reduction of *b*, i.e., the fraction of holes escaping from the ferroelectric, or the increase of *d*, i.e., the defects generation probability.

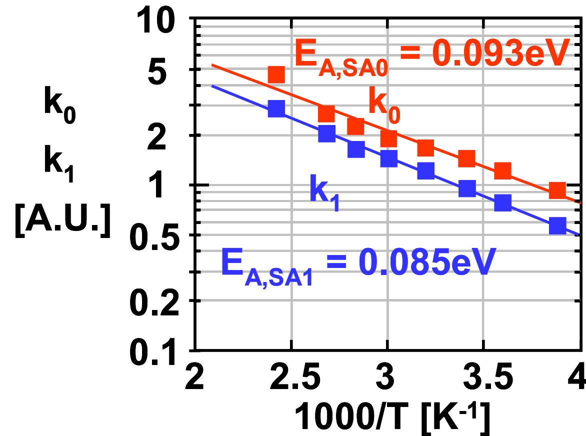

Fig. 8.14. . Irradiation temperature dependence of the slope *k* obtained from (8.7).

In literature the hole mobility has been reported to slightly increase with temperature [192]. This should decrease the escaping time and, consequently, *b* increases, which is apparently in contrast to Fig. 8.14. Hence, the *d* increment should be the dominant effect. The increase of *d* indicates that more defects are generated with increasing temperature, suggesting that the defect generation process is temperature-activated. Noticeably, even though the number of SA1 is always smaller than SA0 (compare Fig. 8.2a and Fig. 8.2b), their growth kinetics feature almost the same activation energy (Fig. 8.14). This suggests that the thermally-activated imprint and fatigue phenomena impact on SA0 and SA1 in the same manner, while the different number of SA0 and SA1 are likely due to the different sensitivity of the peripheral read circuitry.

8.5 Conclusion

We showed the results of radiation tolerance tests on commercial ferroelectric memory chips. The radiation damage strongly depends on the irradiation temperature, and it consists of only stuck bits, with no data corruption immediately after irradiation, at least at doses up to 9Mrad(Si). Furthermore, the radiation tolerance is much higher if the device is unpowered during irradiation. This suggests that a good method to increase the radiation robustness is to physically power off the device, when it is not being used.

The radiation damage anneals in time as long as several weeks. The recovery rate is accelerated by either electrical cycling or high temperature annealing. However, even though high temperature annealing is the most effective in reducing the stuck bits, it does not recover the PZT lattice structure as before irradiation. In fact, the weak bonds generated after annealing are quickly depassivated, if the device is irradiated again. A

complete recovery is reached after cycling, i.e., when the domain orientation is repeatedly switched, allowing the lattice structure reorganization.

For the first time, we developed a model to describe the radiation damage kinetics as a function of the irradiation temperature, which indicates that the defect generation rate is thermally activated.

These data confirm the idea that ferroelectric memories are promising for the application in radiation harsh environments, as possible replacements of both SRAM/DRAM and nonvolatile memories.

Conclusions

Within this thesis, we analyzed the radiation effects on three kinds of advanced memories: nanocrystal memories, phase change memories and ferroelectric memories. As discussed in the previous section, these memories are very different and features both advantages and disadvantages.

The order in which the results have been presented reflect the also the kinds of structures we analyzed. We started from the nanocrystal (and floating gate) MOSFETs (or cell arrays), i.e. performing test on the memory cell alone. After that, measurements on addressable arrays (NCM and PCM) were performed. Addressable arrays include part (or all) the peripheral circuitry of the commercial chip, while maintain the ability to access at low level to the single cell, even if with some limitations. Finally, commercial chips (FRAM), were analyzed. The evaluation of the radiation effects on commercial chips, without access to the single cells, has advantages and disadvantages. Among the advantages, the radiation tolerance of the finished device is evaluated, providing useful reliability data. On the other hand, finding the degradation phenomena and the main responsible for the device failure is somewhat tricky and, as shown in the chapter dedicated to FRAM, several tests are required to assess what are the main degradation phenomena.

The results shown in this thesis have been presented on international conferences and published in international journals, as a testimony of their originality.

For the first time, a detailed analysis on nanocrystal memory, fabricated with state-of-the-art processed, has been performed from the ionizing radiation tolerance viewpoint. Besides, for the first time, a comparative study of the total ionizing dose effects has been carried out between nanocrystal and floating gate memory, fabricated with the same technology. Incidentally, the long term retention after total ionizing dose on modern floating gate memories have been evaluated. Moreover, for the first time, a heavy ion charge loss model for discrete storage memories has been developed. The model, based on a pseudo-3D electrostatic and a Montecarlo simulation provided excellent fits and allowed to estimate the area affected by charge loss induced by heavy ions.

Ionizing radiation effects were also evaluated on PCM test chips, and they allowed to assess that the chalcogenide is effectively very tolerant to ionizing radiation, and that the radiation tolerance bottleneck derives from the peripheral circuitry. The maintained cell programmability even at high doses, and the annealing effects, in fact, suggested that the GST is immune to total ionizing dose, and that the positive charge trapping on the oxides (STI and gate oxide) is the major concern. Still, the effects of alpha particles, heavy ions, etc. on the GST still have to be fully assessed.

Total ionizing dose effects on ferroelectric memories were also analyzed. Not only for the first time, temperature and radiation combined effects on this kind of memory were studied, but also this has been one of the first few works, which evaluated the combined effects of ionizing radiation and temperature on any kind of memory. This was also the first time in which a FRAM degradation model has been provided and the comparison of protons and x-ray effects has been performed on FRAMs. The bias and packaging effects were also analyzed. The results showed that the ferroelectric material is very immune to total ionizing dose, and the bottleneck is the peripheral circuitry, which is strongly degraded if the chip is powered on. However, the absence of high voltage circuitry (charge pumps), which are not required for FRAMS, allowed a much stronger reliability, compared to commercial Flash devices, which may fail even after only few (tens of) krads. Results showed also that packaging effects are all but negligible, and that, for an accurate estimation of the adsorbed dose, the devices must be delidded even when dealing with X-rays.

During the PhD course, some instrumentations have also been developed, in order to perform either the radiation experiments or the electrical measurements. Despite the low cost, these systems proved to be very reliable and precise. These devices have been essential for a good part of this thesis, and for that reason they are briefly described in the appendixes.

In summary, all the analyzed advanced memories feature a much stronger tolerance against ionizing radiation, if compared with the conventional floating gate based Flash. This is achieved either by employing the discrete storage approach (nanocrystal memories), which adds intrinsic redundancy, or by changing the way the information is stored: microstructural properties rather than stored charge.

The improved radiation tolerance of advanced memories is very attracting, from the radiation perspective. In fact, nowadays trends [92] is to use the so called COTS (components off the shelf), which are much less expensive that their radiation hardened counterparts, and to mitigate the effects of radiation by means of system redundancy or error-checking-and correction algorithms. Obviously, if COTS are intrinsically radiation-hardened, there are no drawbacks in switching to consumer devices. Nonetheless, the continuous scaling of the devices, may affect the radiation tolerance even for commercial applications (due to alpha emitters pollutant), because of the smaller energy required to change the stored state. Hence, the evaluation of the

reliability of advanced memories (and, more in general, to nanoscale electronics), will always be an open issue, which is worth to be investigated in future works.

APPENDIX A

Calculation of the midgap voltage variation

In this appendix we show a simple method to evaluate geometrically the midgap voltage variation. The midgap voltage has been calculated exploiting two considerations. First, the drain current in the subthreshold region can be expressed as:

$$I_{DS} = I_{Dmg} \cdot 10^{(V_{GS} - V_{mg,})/S},$$

where, I_{Dmg} is the drain current with $V_{GS} = V_{mg}$, S is the subthrehold slope, V_{mg} is the midgap voltage.

Second, the mobility and in turn, I_{Dmg} do not change significantly at least up to 10 Mrad(SiO_2) and their values can be assumed unaffected by the radiation dose. This is experimentally verified in Fig. A1, which shows only a marginal transconductance variation (less than 3%) of an NCM cell before and after a 10-Mrad(SiO_2) X-ray irradiation.

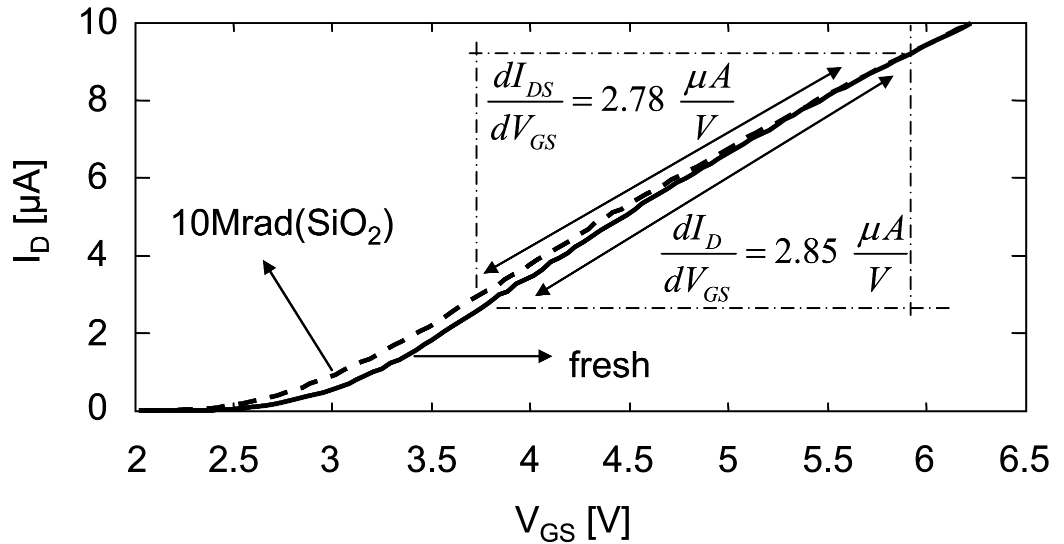

Fig. A1. I_D-V_{GS} curves in linear region of a fresh and an irradiated NCM cell, showing only marginal variations on the transconductance, for doses as high as 10Mrad(SiO_2). The irradiated I_{DS}-V_{GS} curve has been shifted in order to provide a visual estimation of the small difference on the transconductance.

ΔV_{mg}, can be calculated geometrically from Fig. A2:

$$\log_{10} \frac{I_{DTH}}{I_{Dmg}} = \frac{V_{TH,FRESH} - V_{mg,FRESH}}{S_{FRESH}} = \frac{V_{TH,IRR} - V_{mg,IRR}}{S_{IRR}},$$

where the subscripts FRESH and IRR refer to the fresh and irradiated cell, respectively.

Solving this simple linear equation we obtain:

$$\Delta V_{mg} = V_{mg,IRR} - V_{mg,FRESH} = \frac{S_{IRR}\left(V_{mg,FRESH} - V_{TH,FRESH}\right)}{S_{FRESH}} + V_{TH,IRR} - V_{mg,FRESH}$$

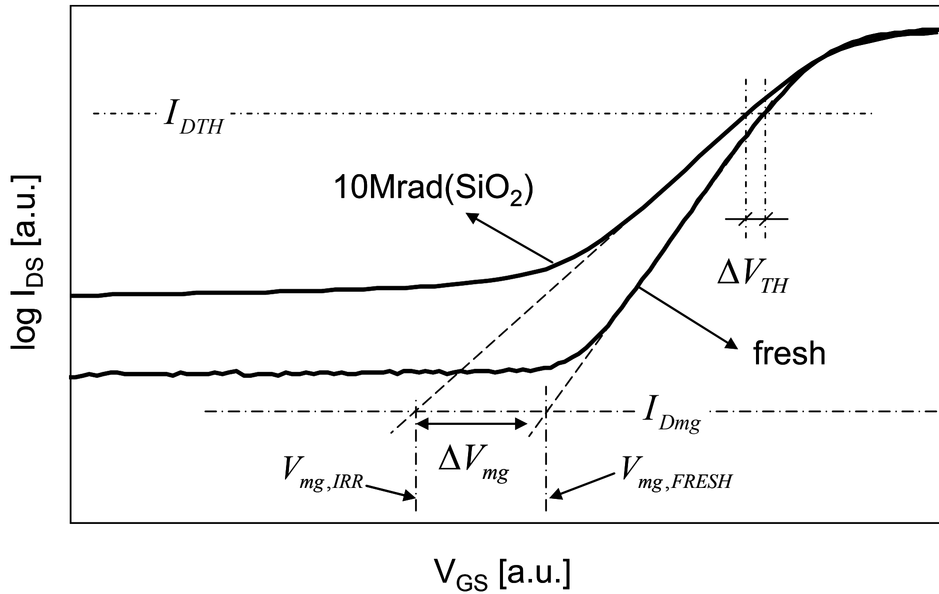

Fig. A2. Calculation of ΔV_{mg} from the measured characteristics.

APPENDIX B

Estimation of the number of multiple ion hits

Here we briefly explain the model adopted to estimate the average number of single and multiple ion hits. We assume that:

1) the ion beam is uniformly distributed all over the surface of the array;

2) the total number of cells is N;

3) the total number of ions hitting the N cells is M. For sake of simplicity, we assume also that each ion hits one and only one cell. In other words, M includes only the ions that actually hit the active area of the cell array, ignoring the hits occurring either over the field oxide between neighbor cells or over the source/drain contacts. In addition we assume that two neighbor cells are spaced enough, so that the ion track cannot affect more than one cell.

We define $n_h(i)$ as the number of cells that have been hit exactly h times after i ions have hit the whole active area of the cell array. Of course, $n_h(i) = 0$ if $h>i$, $n_h(0) = 0$ if $h>0$ and $n_0(0) = N$.

$n_h(i)$ can be calculated recursively as follows. Let's suppose that the value $n_h(i)$ is known. After the $i+1$ hit, we calculate $n_h(i+1)$, i.e., the number of cells that have been hit exactly h times after $i+1$ ion hit in the whole active area.

If $h = 0$:

$$n_0(i+1) = \begin{cases} n_0(i) & \text{if the ion hit a cell that has been previously hit} \\ n_0(i)-1 & \text{if the ion hit a cell that has never been previously hit} \end{cases} \qquad \text{(B.1)}$$

Instead, if $h > 0$:

$$n_h(i+1) = \begin{cases} n_h(i)-1 & \text{if the ion hits a cell that has been hit exactly h times} \\ n_h(i)+1 & \text{if the ion hits a cell that has been hit exactly (h-1) times} \\ n_h(i) & \text{otherwise} \end{cases} \qquad \text{(B.2)}$$

We can rewrite the equations (B.1) and (B.2) as:

$$\begin{aligned} n_0(i+1) &= n_0(i) - H_0(i) && \text{if } h = 0 \\ n_h(i+1) &= n_h(i) - H_h(i) + H_{h-1}(i) && \text{if } h > 0 \end{aligned} \tag{B.3}$$

Where $H_h(i)$ is a binary random variable, which is 1, if the *(i+1)-th* ion hits a cell that has been previously hit exactly *h* times, and 0 otherwise. From assumption 3, for a given *i*, all but one of the $H_h(i)$ variables will be zero.

Our goal is the calculation of the mean value of $n_h(i+1)$, i.e., the mathematical expectation $E[n_h(i+1)]$.We define:

$$\langle n_h(i+1)\rangle \triangleq E\left[n_h(i+1)\right]$$

By exploiting the linearity of the mathematical expectation, from equation (B.3) we recursively calculate $\langle n_h(i+1)\rangle$:

$$\begin{aligned} \langle n_0(i+1)\rangle &= E\left[n_0(i) - H_0(i)\right] = \langle n_0(i)\rangle - E\left[H_0(i)\right] \\ \langle n_h(i+1)\rangle &= E\left[n_h(i) - H_h(i) + H_{h-1}(i)\right] = \\ &= \langle n_h(i)\rangle - E\left[H_h(i)\right] + E\left[H_{h-1}(i)\right] \quad \text{if } h > 0 \end{aligned} \tag{B.4}$$

The mathematical expectation of the binary random variable $H_h(i)$ is given by the probability that $H_h(i) = 1$. With the initial conditions of this problem, it can be shown that:

$$E\left[H_h(i)\right] = \frac{\langle n_h(i)\rangle}{N} \tag{B.5}$$

From equations (B.4) and (B.5) we obtain:

$$\begin{aligned} \langle n_0(i+1)\rangle &= \langle n_0(i)\rangle \left(1 - \frac{1}{N}\right) \\ \langle n_h(i+1)\rangle &= \langle n_h(i)\rangle \left(1 - \frac{1}{N}\right) + \frac{1}{N}\langle n_{h-1}(i)\rangle \quad \text{if } h > 0 \end{aligned} \tag{B.6}$$

Expression (B.6) can be rewritten as a simple linear discrete system, with the matrix **A** is in the Jordan canonical form.

$$\mathbf{n}(i+1) = \frac{1}{N}\mathbf{A}\cdot\mathbf{n}(i)$$

$$\mathbf{n}(i) = \begin{bmatrix} \overline{n_M(i)} \\ \vdots \\ \overline{n_h(i)} \\ \vdots \\ \overline{n_0(i)} \end{bmatrix} \qquad \mathbf{A} = \begin{bmatrix} (N-1) & 1 & 0 & 0 \\ 0 & \ddots & \ddots & 0 \\ \vdots & \ddots & \ddots & 1 \\ 0 & \cdots & 0 & (N-1) \end{bmatrix}$$

In the case of a fresh device, i.e., with i = 0, the initial condition of the recursive solution is:

$$\mathbf{n}(0)=\begin{bmatrix}0\\ \vdots\\ 0\\ N\end{bmatrix}$$

The solution of the system after M ion hits is:

$$\mathbf{n}(M)=\left(\frac{1}{N}\right)^{M}\mathbf{A}^{M}\mathbf{n}(0)$$

With:

$$\mathbf{A}^{M}=\begin{bmatrix}\binom{M}{0}(N-1)^{M} & \binom{M}{1}(N-1)^{M-1} & \binom{M}{2}(N-1)^{M-2} & \cdots\\ 0 & \binom{M}{0}(N-1)^{M} & \binom{M}{1}(N-1)^{M-1} & \cdots\\ 0 & 0 & \binom{M}{0}(N-1)^{M} & \cdots\\ \vdots & \vdots & \vdots & \ddots\end{bmatrix}$$

This gives the following expression for $\langle n_h(M)\rangle$

$$\langle n_h(M)\rangle=\begin{cases}\left(\frac{1}{N}\right)^{M-1}(N-1)^{M-h}\dfrac{M!}{h!(M-h)!} & h\le M\\ 0 & h>M\end{cases}$$

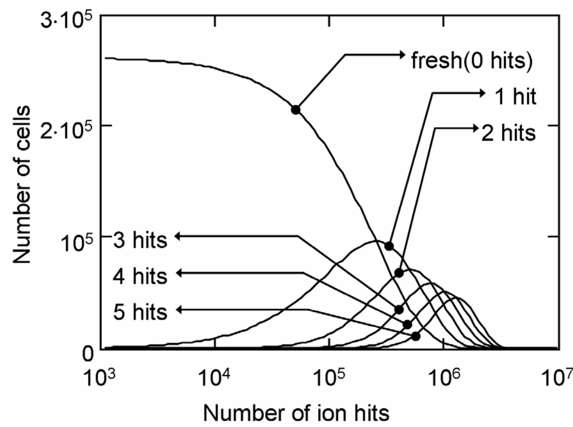

Fig. B1. Average number of cells receiving a given number of hits (up to 5) as a function of the number of ion hits on the array. In our experiment roughly 78000 ions hit the gate active area of the cells programmed at "1".

In Fig. B1 we plot the probability of 0 up to 5 hits on a cell array of 256k cells ($N = 262144$), corresponding to the number of one half of our array of chapter 6, i.e., those cells storing "1" (or storing "0").

Remarkably, the same results can be also obtained considering the probability of having exactly h successes (h hits in a cell) after M trials (M ions struck the whole array), with probability of each ion to hit a certain cell equal to $1/N$, where N is the total number of cells in the array. This is the binomial probability mass function.

APPENDIX C

The PCM array characterization system

The addressable arrays of PCM cells require a particular circuitry for the characterization. At this purpose the miniRifle was developed and built, which consists in a small board, which is connected to the PC through the USB port or RS-232. In the PC, an application allows to communicate with the board and to perform complex measurement tasks, even with nested loops.

The miniRifle allows to perform the following measurements:

1) Memory dump (digital).
2) Memory programming (with selectable SET and RESET voltage).
3) Memory endurance test.
4) Cell stress.
5) Readout of the cell current distributions (analog memory dump).
6) Measurement of the cell I-V characteristics.
7) Measurements of the cell I-Time (with sampling time variable between 20μs to 0.262s)
8) SET, RESET, and READ voltages (as well as the cell selector voltage) selectable between 0 and 5.7V, with 22-mV step. The cell I-V can be performed between 0 and 2.048V with 8-mV step.

The control program also allows to directly evaluate the histograms of the cell current distributions.

The main features of the miniRifle are:

1) Eight force-voltage-measure-current source-measure channels, up to 125ksps.
2) Current ranges: 1mA, 100μA e 10μA.
3) Resolutions: 250nA, 25nA, 2.5nA.
4) Six general purpose voltage generators.

Fig. C1 show the control program and Fig. C2 shows the miniRifle board: the four BNCs allow to connect the PCM to other instrumentations.

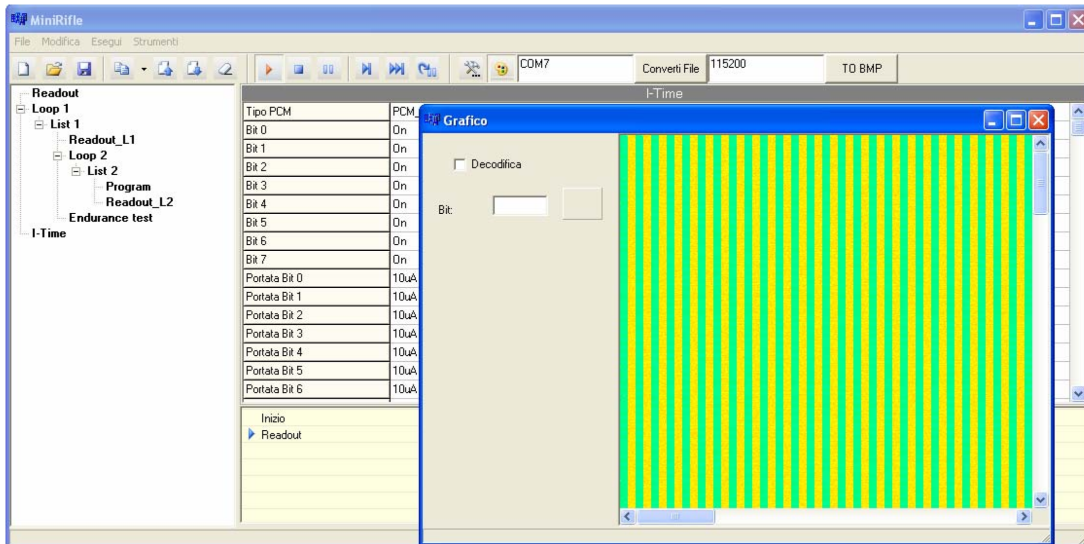

Fig. C1. The control program executing a measurement setup. In particular, the cell current distribution is being read and graphically shown in false colors.

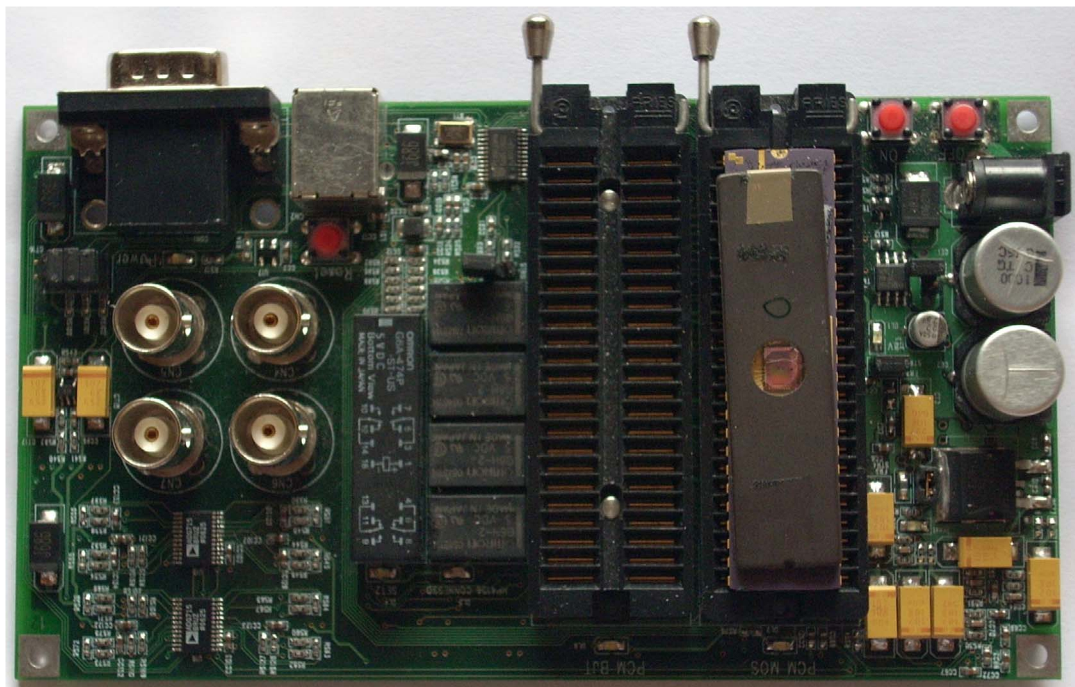

Fig. C2. The miniRifle control board. A MOS PCM array is inserted in its socket.

Fig. C3 shows the schematic block diagram of the miniRifle. There are 4 power supplies, which are grouped in 2 blocks: the digital power supply (which is not controlled by the microcontroller) and the analog and PCM V_{DD} power supply. The analog power supplies consist of 5V and 6V, and they can be powered off, as well as the PCM V_{DD}. The PCM arrays can be disconnected from the digital and analog sections by powering off the analog supply and PCM V_{DD}.

The PCM is connected to the microcontroller using level translators, due to the different PCM and microcontroller working voltages. Because of the high leakage of digital circuitry, the data output of the PCM are not directly connected to the microcontroller, but with a low leakage low R_{ON} analog multiplexer. During the analog

current measurements, the multiplexer connects the data outputs to the 8 force-voltage-measure-current units. On the contrary, when digital operations are required (digital read, configuration, programming) the data lines are connected to the level translator (hence to the microcontroller).

The switch matrix allows to connect the 8 data i/o lines either to the low leakage multiplexer, or to the 4 BNC (of course, only 4 pad at a time). In this way additional measurements can be performed with other instrumentation.

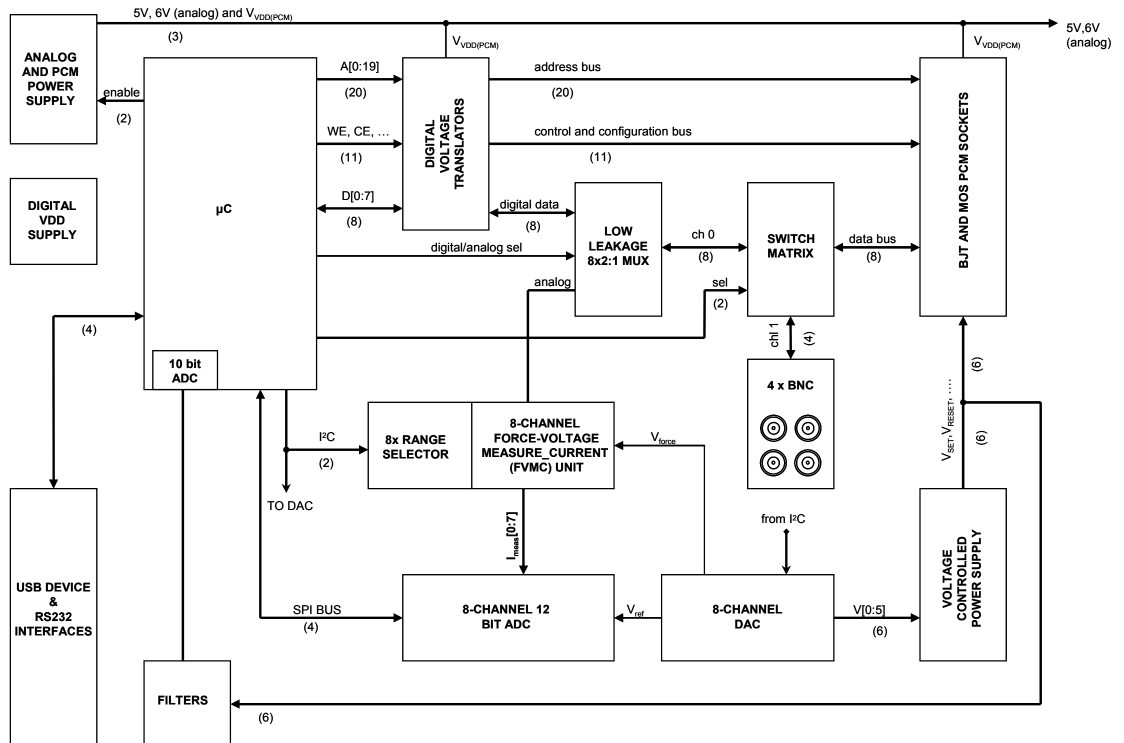

Fig. C3. Block-diagram schematics of the miniRifle board. Thick lines represent grouped signals. Under the thick lines, the numbers of actual signals are shown.

The PCM cell may exhibit very different current levels, depending on the cell state. Hence, the source-measure units have 3 ranges, allowing to maintain good resolutions in each case. In case of short or catastrophic cell failure, the current is limited to about 1mA, avoiding any damage either to the instruments, or to the test chip.

An 8-channel DAC generates the references for the 6 external voltages required for the PCM test chip, the ADC, and the Force-Voltage-Measure-Current units.

APPENDIX D

The temperature controller

To perform radiation experiments under high and low temperatures, a full featured temperature controller and the corresponding heaters/coolers were developed and built. The main features of the controller are:

- Three independent filtered PWM output channels (one for the heater/cooler) Output powers: 250W each channel (500W max combined power output).
- PID control algorithm with selectable PID parameters, to avoid overshoot and to achieve fast transient responses.
- Three inputs for the temperature monitoring: range -129°C +324°C. Sensitivity: 0.01°C. The temperature sensors can be configured as temperature feedback (for the PID algorithm) or monitor.
- Selectable setpoints, and over-temperature shutdown levels with 0.1°C resolution. Sensor 1 also feature a selectable hardware shutdown in case of over temperature.
- On-screen graph of the three measured temperatures. The scale and the interval update can be selected.
- Stand alone or remotely (via PC) controllable.

The heater uses 4 resistors uniformly arranged in the heating plate. It has the following features:

- 175 W heating power.
- dT/dt [30°C to 100°C] = 0.4°C/s.
- 3 additional sample holders can be mounted for 48-pin DIP packages.
- Area (for wafer slices): 6x14 cm^2.
- Temperature range: RT to 250°C.

The heater/cooler uses two high temperature Peltier cells, which are liquid cooled on the hot side. Liquid cooling allows also to operate under vacuum. The main specifications are:

- Temperature ranges: -30°C to 180°C.

- dT/dt [30°C to 100°C]: 1.3°C/s.
- Overshoot recovery (to 0.1°C): less than 2s.
- Power: 120W.
- One sample holder for up to 48-pin DIP package.
- Area (for wafer slices): 4x4 cm^2.

Fig. D1. Photo of the temperature controller.

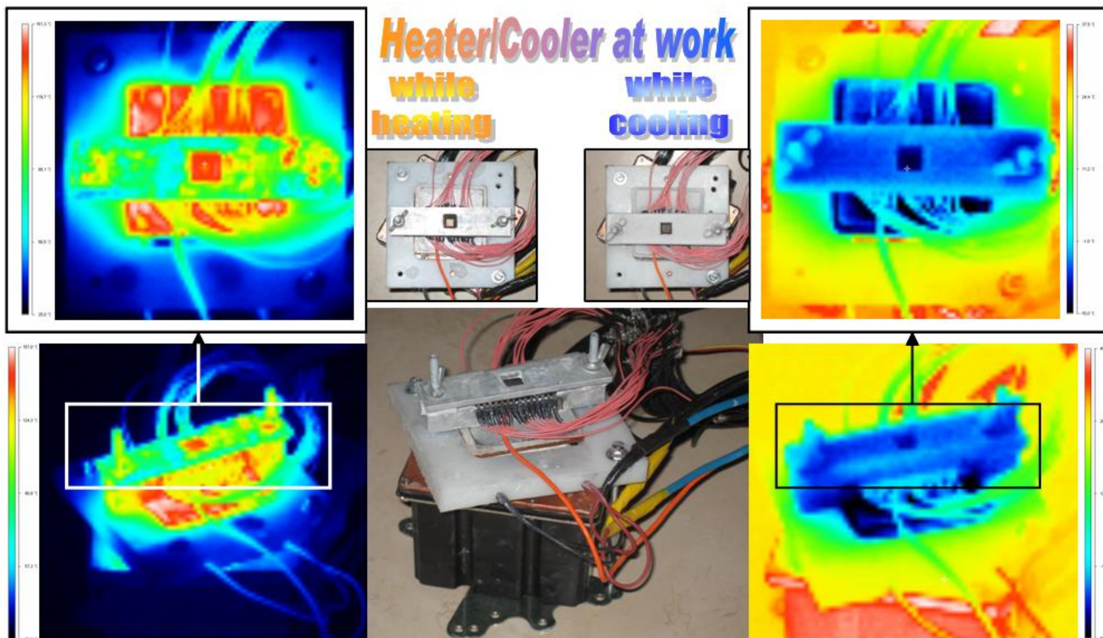

Fig. D2. Photo of the heater/cooler at work and the thermal images captured with the infrared camera.

Fig. D1 shows the temperature controller, while Fig. D2 shows the heater/cooler at work. Fig. D2 also shows the thermal profiles captured with an infrared camera, showing good temperature uniformity on the memory die.

Fig. D3 shows the schematic block diagram of the temperature controller. A standard, low cost, ATX power supply provides the necessary voltages for the controller and for the heater(s) or heater/cooler.

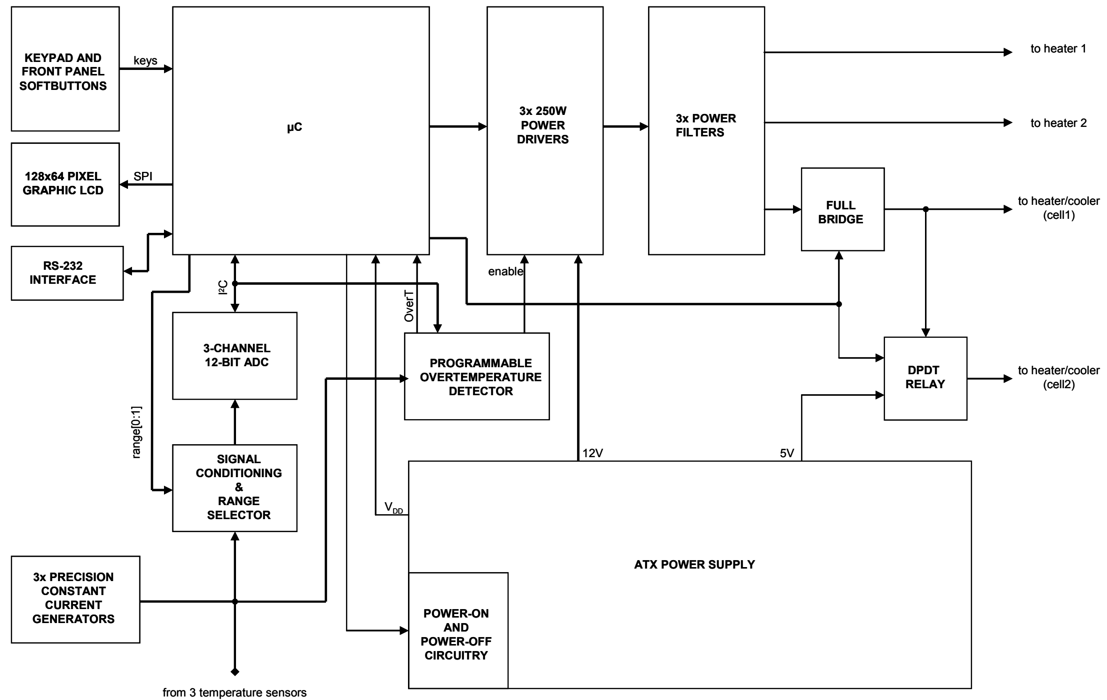

Fig. D3. Block-diagram schematics of the temperature controller. Thick lines represent grouped signals.

Three current generators provide a precise constant current supply for the three temperature sensors. An ADC reads the voltages of the temperature detectors, which linearly scale with the detector temperature. The employment of resistance temperature detectors allows also an intrinsic safety. In fact, if accidentally one connector gets unplugged, or has a failing contact, the resistance is read as infinite and the outputs are disabled. The voltages measured from the three sensors are continuously monitored by the programmable overtemperature detector, which disable the outputs in case of the preset limit is reached. If the outputs are disabled, the microcontroller can enable the outputs back, by providing a pulse (for increased safety, the enable is edge sensitive).

Because of the high power, any switching PWM would irradiate a lot of electrical noise. Hence, all the PWM outputs are filtered. This also reduces the power spikes on the power supply unit.

Peltier cells need to operate either as cooler or as heater. Hence, a full-bridge is implemented. Additionally, Peltier cells require a different driving strategy, depending on the temperature and on their work regime (heater or cooler). When operating as heater, the Peltier cells work in parallel, and a large heat flux is delivered to the sample. This is also the case when the Peltier stack works as cooler in the range above 10°C. This maximizes the cooling power. However, to achieve very low temperatures, the electrical power dissipated by the two Peltier cells becomes a concern and it limits the minimum temperature. Hence, when operating as cooler, as soon as the temperature falls below 10°C, the first cell is switched to to a reduced power supply. This allows to reach a much lower temperature at the expense of the cooling time.

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