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PhD Thesis

Reliability analysis of GaN HEMT for space applications and switching converters based on advanced experimental techniques and two dimensional device simulations

Coordinatore: Ch.mo Prof. Matteo Bertocco

Supervisore: Ch.mo Prof. Enrico Zanoni

Co-Supervisore: Ch.mo Prof. Gaudenzio Meneghesso

Dottorando: Stefano Dalcanale

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Abstract

Gallium Nitride is a promising wide-bandgap material for electronics. With GaN-based devices it is possible to achieve higher operative frequencies and power densities in comparison to Silicon. The first GaN-based High Electron Mobility Transistor (HEMT) has been designed in the 1995, and after twenty years this technology start to be ready to compete in the market with Silicon-based devices. There are several reason why it was necessary all this time to obtain a stable technology. Unlike Silicon, it is still not possible to grow a gallium nitride crystal starting from a seed, with reasonable quality dimensions and costs. Thus, it is necessary to grow it on different substrates, like Silicon Carbide, Sapphire or Silicon. Therefore, the obtained crystals have a high defects concentration that limits the device performances. With the optimization of the process and the introduction suitable nucleation layer on the substrate it is now possible to grow GaN wafers with a tolerable defectivity. The main problems induced by the defects are trap states and reliability issues. The trap states generate problems during dynamic operation, inducing a drop in the output characteristics. In addition to this recoverable phenomena, the GaN-HEMTs can even present problem of reliability, that have been widely explored in the past. Nowadays, the estimated device life time of the last technologies allow to start the production of electronics both for consumer market than for the more demanding space applications.

Within this work it will be presented a summary of the research activity performed during my PhD. In the first part is presented a short summary of the state of the art of GaN-HEMT technology. In the last two years a lot of

new results have been demonstrated in literature, showing the last technological improvements. Then, a short summary on the trapping phenomena and reliability issue is presented, that is fundamental to understand all the obtained results.

The research activities involved the two main GaN-based HEMTs applications: the RF devices and the power switching transistors. For the RF applications the transistor is used as an amplifier, in a frequency range from 1 GHz to 100 GHz. The main applications are radar and telecommunications for mobile phone, radio and satellites. I collaborated in a project of the *European Space Agency*, with subject *"Preliminary Validation of Space Compatible Foundry Processes"*. They will be presented all the results of the reliability assessment carried out within this project. The purpose was to validate a GaN-HEMT technology for space applications, trying to estimate the device lifetime and the failure mechanisms. We will see that the two analysed technologies are very stable, and the estimated life time exceed the twenty years. Nevertheless, not all the failure mechanisms are clear, but we found some degradation signatures that can be related to the gate metallization.

On the side of power switching transistors I will report first the results obtained in a collaboration with *ON Semiconductor* on the development of d-mode MIS-HEMTs. Our role was to give a feedback on the device performance improvement, mainly focused on the on-resistance. It represents indeed one of the main problems of GaN-HEMT working in switching conditions and it is mainly related to trapping phenomena. Then, we developed a new original measurement procedure that allows to test the devices in a condition closer to the operative one. This new setup helps us to demonstrate the impressive stability of the last device generations. Now this technology is ready to work at 600 V in switching operation, with performances better than Silicon.

The second part about the power devices will report the work carried out during the period by the *Ferdinand-Braun-Institut, Leibniz-Institut für Hochfrequenztechnik* (FBH), in Berlin. The target was to investigate the reliability of the p-GaN devices developed by the research center by means of long term on-state

life test. The gate leakage current is suspected to be one of the main problem for the reliability of this kind of device in on-state operation. However, there are not many works in literature that analyse this issue, and we will see how our test helps to consolidate one of the proposed degradation modes. Within this analysis it was fundamental the role of physical based simulations, for which is devoted a separated chapter. The simulations were very helpful for the understanding of the degradation mechanism. They allowed us to have a complete vision of the conduction mechanisms and of the device weakness. In this way we can give fundamental information to the device developers, in particular which device regions need to be improved.

Sommario

Il nitruro di gallio è un promettente materiale a semiconduttore con ampio energy-gap. Tramite dispositivi bastai su GaN è possibile raggiungere frequenze operative e densità di potenza maggiori in confronto al silicio. Il primo transistor HEMT (High Electron Mobility Transistor) basato su GaN è stato sviluppato nel 1995, e dopo vent'anni questa tecnologia inizia ad essere pronta a competere sul mercato con dispositivi basati su silicio. Ci sono diversi motivi per cui è servito del tempo per ottenere una tecnologia stabile. A differenza del silicio, non è possibile crescere cristalli di nitruro di gallio partendo da un seme, non almeno con costi, qualità e dimensioni ragionevoli. Perciò è necessario crescere il nitruro di gallio su substrati diversi, come il carburo di silicio, lo zaffiro o il silicio. Perciò, i cristalli ottenuti hanno una concentrazione di difetti che limita le prestazioni dei dispositivi. Con l'ottimizzazione del processo e l'introduzione di una adeguato strato di transizione, detto *nucleation layer*, è possibile ottenere dei wafer con una difettività tollerabile. Il problema principale introdotto dai difetti sono gli stati trappola e questioni di affidabilità. Gli stati trappola danno problemi durante il funzionamento dei transistor, creando un calo temporaneo della caratteristica di uscita. Oltre a questo fenomeno temporaneo gli HEMT basati su GaN presentano problemi di affidabilità, ampiamente studiati in passato. Al giorno d'oggi il tempo di vita medio stimato delle ultime generazioni di transistor permette la produzione di dispositivi elettronici sia per il settore commerciale che per applicazioni spaziali.

In questo lavoro sarà presentato un riassunto delle attività di ricerca svolte durante il dottorato. Nella prima parte è presentato un riepilogo dello stato dell'arte della tecnologia GaN-HEMT. Negli ultimi due anni in letteratura sono

stati dimostrati nuovi risultati, rivelando un notevole miglioramento tecnologico. Verrà poi presentato un breve riassunto sui fenomeni di trapping e sull'affidabilità, che risulterà fondamentale per comprendere al meglio i risultati ottenuti.

Le attività di ricerca hanno coinvolto le due applicazioni principali dei transistor GaN-HEMT: i dispositivi RF e i transitor di potenza. Per applicazioni RF il transistor è usato come amplificatore, in un range di frequenze tra 1 GHz e 100 GHz. Le applicazioni principali sono radar e telecomunicazioni per telefonia mobile, radio e satellitare. Ho collaborato in un progetto dell'Agenzia Spaziale Europea dal titolo: *"Preliminary Validation of Space Compatible Foundry Processes"*. Verranno presentati i risultati della valutazione dell'affidabilità svolta in questo progetto. Lo scopo era di validare la tecnologia GaN-HEMT per applicazioni spaziali, provando a stimare il tempo di vita dei dispositivi e i meccanismi di guasto. Vedremo come la tecnologia analizzata sia stabile, con un tempo di vita stimato che oltrepassa i vent'anni. Ciò nonostante, non sono ancora chiari tutti i meccanismi di guasto, ma è stata trovata qualche caratteristica tipica del degrado legata alla metallizzazione di gate.

Dal lato dei transistor di potenza verranno riportati prima i risultati ottenuti nella collaborazione con *ON Semiconductor*, nello sviluppo di dispositivi MIS-HEMT *normally-on*. Il nostro ruolo era di dare un feedback all'azienda riguardo alle performance dei dispositivi, in particolare in termini di resistenza in on-state. Questo rappresenta infatti uno dei problemi maggiori dei transistor GaN-HEMT che lavorano in condizioni *switching* ed è dovuto a fenomeni di trapping. Poi, è stato sviluppata una nuova procedura di misura che permette di testare i dispositivi in condizione vicine a quelle operative. Questo nuovo setup è stato d'aiuto per dimostrare l'eccezionale stabilità delle ultime generazioni di trasistor. Ora questa tecnologia è pronta per lavorare a 600 V con prestazioni migliori di quelle del silicio.

La seconda parte relativa ai dispositivi di potenza parlerà del lavoro svolto presso il *Ferdinand-Braun-Institut, Leibniz-Institut für Hochfrequenztechnik* (FBH), a Berlino. L'obiettivo principale era quello di investigare l'affidabilità dei disposi-

tivi p-GaN sviluppati presso il centro di ricerca, tramite stress in on-state a lungo termine. La corrente di leakage di gate è sospettata di essere uno dei problemi principali per l'affidabilità di questo tipo di dispositivi in on-state. Tuttavia, non ci sono tanti lavori in letteratura che analizzano il problema, e si vedrà come i test svolti aiutano a consolidare uno dei modelli proposti. In questa analisi è stato fondamentale il ruolo delle simulazioni, a cui è stato riservato un capitolo a parte. Le simulazioni sono state di grande aiuto nella comprensione dei meccanismi di guasto e hanno permesso di avere una visione completa dei meccanismi di conduzione e dei punti deboli del dispositivo. In questo modo possono essere date informazioni essenziali a chi sviluppa i transistor, in particolare quali sono le regioni del dispositivo che andrebbero migliorate.

Introduction

The semiconductor industry is always looking for new materials, although nowadays most of the electronics is based on Silicon. The wide bandgap semiconductors are very promising for several applications from the telecommunication systems to the energy conversion. As example, two materials that are already in industrial and commercial electronics are Gallium Arsenide an Silicon Carbide. Since twenty years the research is focusing on Gallium Nitride, that exhibit interesting properties, like the high bandgap, the high saturation velocity of electrons and the high mobility. Thanks to these characteristics it is possible to withstand high breakdown electric fields, to obtain a high power density and low noise devices that can reaches operative frequency in the order of 300 GHz. Furthermore, the possibility to build heterostructures allow the realization of the High Electron Mobility Transistor (HEMT). This kind of transistor has a low channel resistance and a high current density, thanks to the high carrier concentration in the channel and the high mobility. This technology finds applications both in radiofrequency devices and in power electronics.

On the radiofrequency side the main applications are in telecommunications, both from satellites, for mobile phones, for fibre optic networks, for cable TV and Internet of Things (IoT). In the fields of defence and aerospace there are power amplifiers for radars and radio communications on earth and from satellites. Furthermore, the GaN technology leads to novel decentralized rf systems, such as beam steering antennas and phase array radars. The main advantage of the GaN devices is the high power density, that allow to decrease the coolers size. Considering also the inherent radiation hardness this is a promising technology

for space applications. In May 2013 the European Space Agency launched *Proba V*, a satellite for environmental monitoring. The power amplifier that send the data on earth is based on Gallium Nitride, and probably it will be the standard technology for the next missions. During my PhD activity I have been working on a project funded by the European Space Agency called *Preliminary Validation of Space Compatible Foundry Processes*. The main purpose was to test the reliability of GaN HEMT devices with short and long-term stress test in order to identify the degradation modes and the failure mechanisms.

For the next generation of mobile communications, the 5G, we will need higher bit-rates in comparison to the currently 4G LTE. This means that the operative frequencies will be increased from the currently 2.7 GHz up to 6 GHz. The GaN technology could play a key role on this side, since it allows to implement power amplifiers for the base stations with high efficiency at those frequencies.

On the side of transistors for power electronics the main applications are the inverters for renewable energies, the automotive, the power management and conversion from consumer market, like power supplies and voltage regulators. In these fields Gallium Nitride allow to design converters with a very high efficiency, with a subsequent energy saving. This is fundamental if we think that in 2014 the worldwide installed power of photovoltaic and wind energy was around 550 GW, with an increasing trend of 15%. It is easy to understand that even a small increase in the efficiency of the inverters could allow to save gigawatts of power. The research activities on power devices, during my PhD were mainly concentrated in collaborations with companies. The purpose was to give a feedback to the foundries in order to understand the best way to follow during the development. The tests that have been carried out were focusing on the dynamic performances of the GaN HEMTs in terms of on-resistance, a parameter that is optimized with a trade-off on the breakdown voltage. In the first year of my PhD I collaborated on the European project *Gan-based normally-off high power switching transistor for efficient power converters* (HiPoSwitch). In the second year of my PhD, at the end of this project, I continued the work on that devices

during the six-months period abroad, by the *Ferdinand-Braun-Institut, Leibniz-Institut für Hochfrequenztechnik* (FBH), in Berlin. During that period I carried out reliability tests and simulations.

In the following is reported the outline of the thesis:

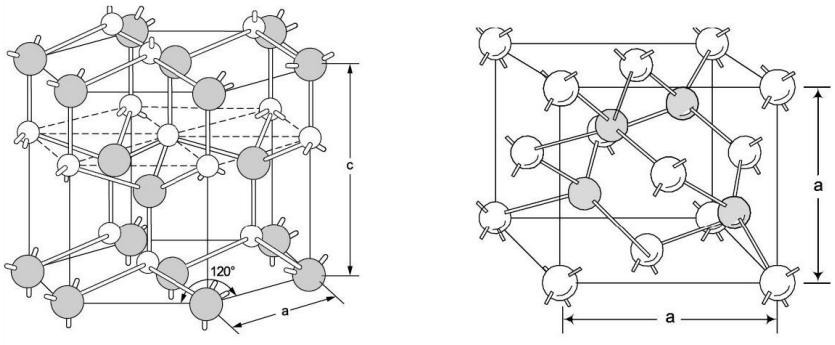
- **Chapter 1:** In the first chapter the main properties of gallium nitride are described.
- **Chapter 2:** Here it is described how the HEMTs transistors work, with a focus on the formation of the conductive channel, the trapping phenomena and the degradation mechanisms.
- **Chapter 3:** This part report a summary of the simulation activity. There will be described the basics of the simulator and the strategies adopted during the simulations.
- **Chapter 4:** This chapter shows the results of the research activities carried out on the high frequency devices. This work has been performed in a project funded by the European Space Agency: *Preliminary Validation of Space Compatible GaN Foundry Process*.
- **Chapter 5:** This chapter cover the part of the research activities carried out on the Power devices. The first part is dedicated to the analysis of the Metal-Insulator Semiconductor technology, while the second part reports the study of the p-GaN HEMTs, carried out during my period by FBH.

Chapter 1

Gallium Nitride properties

1.1 Lattice structure

Gallium Nitride (GaN) is a compound semiconductor, made by one element of the III group of the periodic table, Gallium (Ga) and one of the V group, Nitrogen (N). At room temperature Gallium nitride is in solid phase with two possible crystalline structures: *wurtzite* or *zincblende* (see Figure 1.1). The wurtzite crystallographic structure consists of an elementary tetrahedric cell where each Ga atom is bonded to four N atoms. The subsequent lattice has hexagonal symmetry with planes formed by the same element alternating between them. In this case the lattice parameters are: $a = b = c$, $\alpha = \beta = 90$ and $\gamma = 120$.



(a) Wurtzite lattice. **(b)** Zincblende lattice.

Figure 1.1: Lattice structure of Gallium Nitride.

In the zincblend structure the elementary cells come together, forming a face-centred cubic structure. In this case the lattice parameters are: $a = b = c$, $\alpha = \beta = \gamma = 90$. The zincblend structure is metastable and naturally transmute into wurtzite, that is therefore the one adopted for the electronic devices.

1.2 Band structure and electronic properties

Gallium Nitride is a direct-bandgap semiconductor and, as is possible to see in the diagram in Figure 1.2, the minimum of the conduction band and the maximum of the valence band are at the same value of momentum k. in this way it is possible to have a electron-hole recombination without phonon interactions, making the material a direct bandgap semiconductor.

GaN is a semiconductor with an high energy-gap, therefore it is necessary a very high electric field to have enough energy for the impact ionization and the subsequent breakdown of the device. This make it a robust material toward electric fields, allowing, for the same applied voltage, to decrease the size of the transistors, especially in the gate-drain distance, where there are the higher electric fields. Another advantage is the possibility to work at high temperature. The high energy gap entails a low thermal carrier generation, that limits the intrinsic generation problems when the temperature increases. This feature makes GaN a material suitable for the realization of high performance devices in terms of power and operative frequency [1].

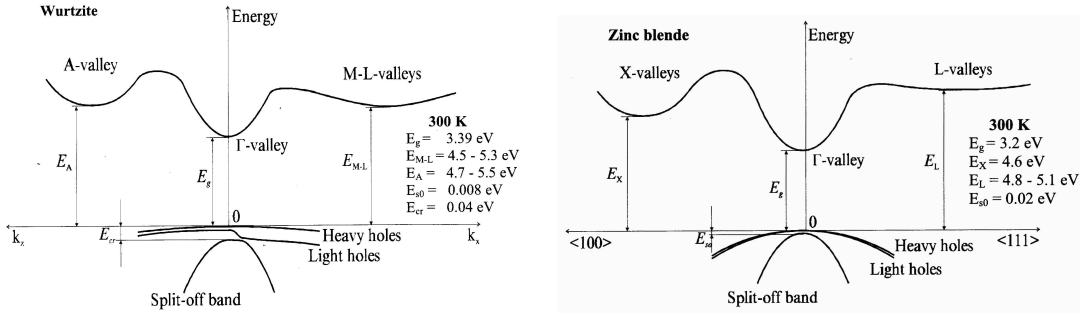


Figure 1.2: GaN band diagrams for the wurtzite and zincblend structures [2].

Table 1.1: Electronic properties of some semiconductors [1].

	GaN	InP	GaAs	SiC	Si
E_g (eV)	3.39	1.35	1.42	3.26	1.1
E_{br} (MV/cm)	3.3	0.5	0.4	3.0	0.3
μ_n (cm^2/V s)	1200–2000	5400	8500	700	1350
v_{sat} (10^7cm/s)	2.5	1	1	2	1
K_{th} (W/cm K)	1.3	0.7	0.43	4.5	1.5
ε_r	9.0	12.5	13.1	10.0	11.8
JM	625	14.7	7.8	400	1

From the parameters reported in Table 1.1 it is possible to notice the high energy-gap, the high breakdown electric field and the higher saturation velocity of GaN in comparison to the others semiconductors. There is a parameter that provide a performance index in term of frequency and power based only on the material properties is JM, i.e. the *Johnoson's figure of merit*; it allows to compare different materials for microwave applications.

$$JM = \frac{E_{br} \cdot v_{sat}}{2\pi} .$$

Another fundamental property to consider, since it is fundamental for the transistor operation, is the material polarization. In Gallium Nitride there are both a spontaneous and a piezoelectric polarization. The spontaneous polarization of GaN arise from the strong difference in electronegativity of the two elements of the material, that creates a dipole moment along the <0001> direction of the crystal. Figure 1.3 shows the two different possible configurations of the lattice: if the top of the crystal ends with a layer of Ga atoms (*Ga-face*) the polarization vector points toward the bottom; in the other case, when the top layer is made of N atoms (*N-face*) the polarization vector points toward the top.

The piezoelectric polarization arises when a stress is applied to the crystal.

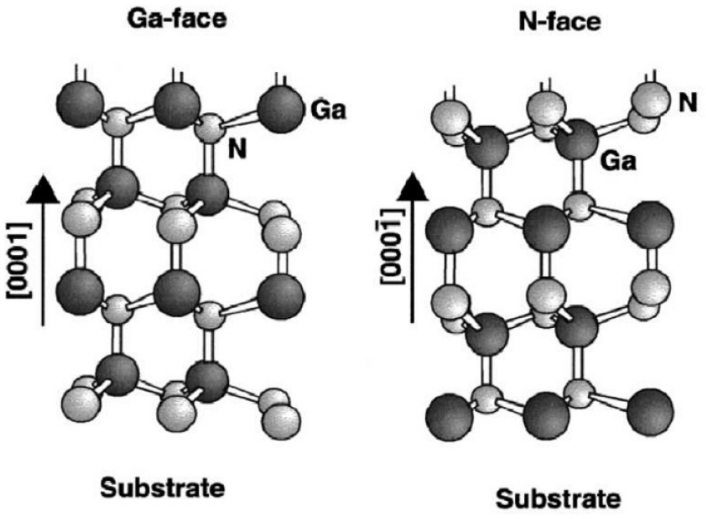


Figure 1.3: Illustration of the GaN wurtzite crystal structures Ga-face and N-face [3].

For example, if the nitride Ga-face crystal is under biaxial tensile stress along the <0001> direction (or under compressive strain along the perpendicular direction) the vertical lattice constant will increase. As consequence, the piezoelectric polarization vector will point toward the <0001> direction. In the opposite case, when the stress along the <0001> direction is compressive, the piezoelectric polarization vector will point toward the opposite direction. The stress can originate from a mechanical strain, or in the case of heterostructures, when two material with different lattice constants are grown on two layers. On the surface between the two materials it could appear a fixed charge due to the sum of the spontaneous and piezoelectric polarization vectors, and consequently an high electric field. This feature is fundamental for the operation of the electronics devices based on nitride heterostructures and will be examined in depth in the next chapter.

Chapter 2

High Electron Mobility Transistor

The High Electron Mobility Transistor (HEMT), called also Heterostructure Field effect Transistor (HFET), is a transistor with a high carrier mobility based on a high energy-gap semiconductors heterostructures. This kind of structure allows to obtain a high carrier concentration with the high mobility of a intrinsic semiconductor, and consequently devices with high current densities.

The first HEMTs were based on a GaAs heterostructure, but, as cited in the previous chapter, GaN has better properties and allows to implement devices with higher operative voltage and power density. In the next section it will be explained the operating principle of the GaN-based HEMTs.

2.1 AlGaN/GaN-based HEMT

The basic structure of a GaN-based HEMT consists of an AlGaN layer grown over a GaN buffer. In the GaN layer, close to the interface to the AlGaN, it forms a quantum well that is usually referred to as Two-dimensional Electron Gas (2DEG) [4]. The origin of this conductive channel comes from the polarization that arise at the interface of the two piezoelectric materials. As previously reported, the lattice mismatch between AlGaN and GaN is the origin of the the piezoelectric polarization, that is in addition to the spontaneous polarization. It is possible to sum the two contributions only choosing a suitable orientation of the

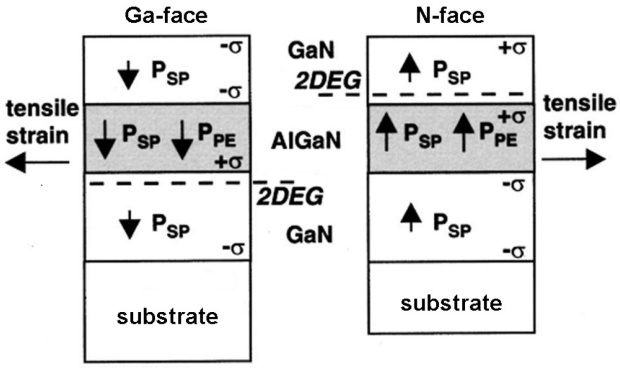


Figure 2.1: Spontaneous an piezoelectric polarization vectors in Ga-face and N-face topologies [5].

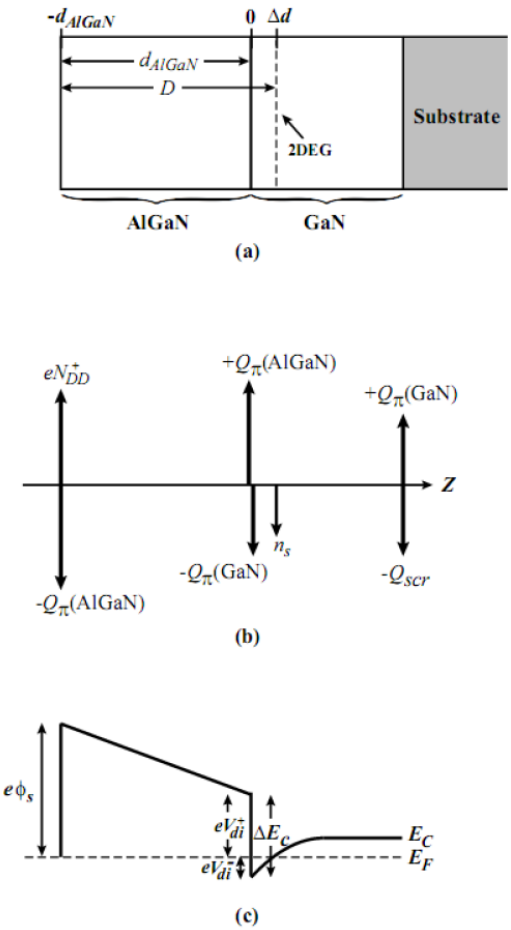


Figure 2.2: (a) AlGaN/GaN heterostructure layer stack, (b) charge distribution and (c) conduction band diagram of the structure [6].

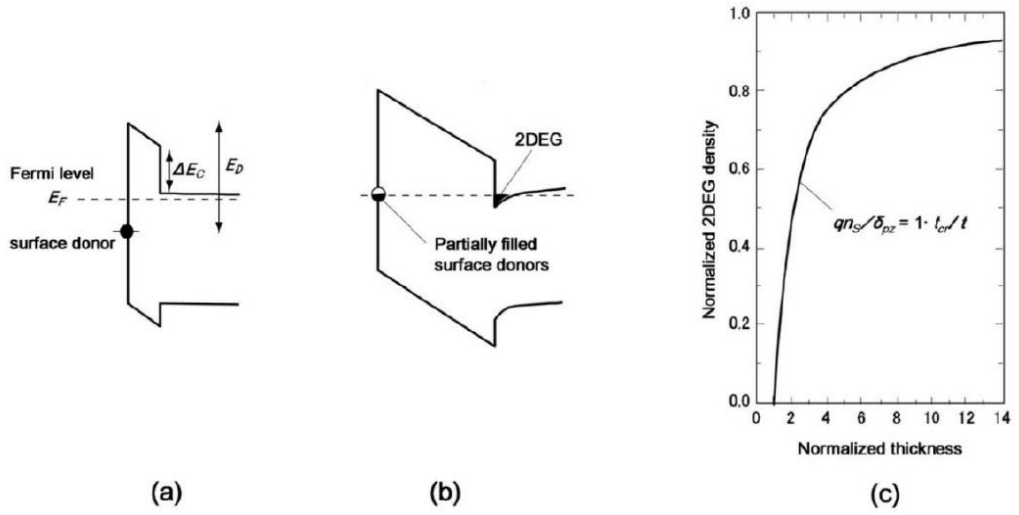


Figure 2.3: Band diagram with (a) smaller and (b) bigger barrier thickness compared to the critical one necessary for the formation of the 2DEG, and (c) channel charge density as a function of the AlGaN thickness [7].

buffer crystal orientation. In Figure 2.1 are reported the two possible choices that induce the formation of the channel with the highest electron concentration, one for the Ga-face and another one for the N-face topology. Currently the most used configuration is the Ga-face, as depicted on the left in Figure 2.1, but without the upper GaN layer. All the following considerations will refer to this topology, but is possible to find studies about devices based on the N-polar configuration [8].

In Figure 2.2 (b) it is possible to see the distribution of the electric charge in a typical AlGaN/GaN heterostructure. The net charge Q_π is the sum of the spontaneous and piezoelectric polarization. The resulting band diagram is sketched in Figure 2.2 (c), where it is possible to see how the conduction band goes under the Fermi level creating the 2DEG. The origin of this huge amount of charge at the interface is not so clear, but the most accepted theory about claims that the charge comes from surface donor trap states [7]. In Figure 2.3 is possible to see that while it is not reached the critical thickness layer, the surface donors can not release their electrons, since they are under the Fermi level (Figure 2.3 (a)). Increasing the AlGaN thickness the donors start to be over the Fermi level, their

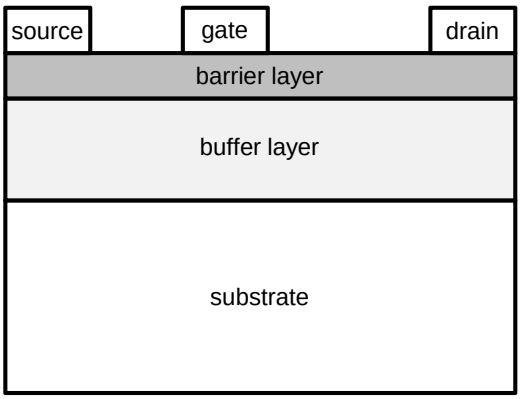


Figure 2.4: Typical structure of an AlGaN/GaN HEMT.

electrons are detrapped and the channel can be formed. The plot in Figure 2.3 (c) resume how the charge density in the 2DEG depends on the AlGaN layer thickness.

Adding two external metal contacts (drain and source) it is possible to create a path for the current throughout the channel. This kind of contacts should have a ohmic behaviour with a resistance lower as possible. For this reason there must be chosen metals with a low work function, often combined in alloys in order to optimize the contact resistance; a typical metal stack is Ti/Al/Ni/Au. Adding even the gate contact it is possible to control the charge flow in the transistor. In this case is required to make a Schottky contact in order to limit the gate leakage current. For this reason they are used metals with a high work function like Ni, Pd, Pt. Also in this case it is possible to form a multi-layer metal stack, adding for example Ti in order to increase the thermal stability, or Al, Au for the conductivity.

In Figure 2.4 is represented a typical structure of an AlGaN/GaN HEMT. The different layer composition and thickness depend on the application of the transistor, as the geometry of the device. In the next part there will be presented the two main applications of the HEMTs: the RF amplifiers and the power switching transistors.

2.2 Microwave Power Amplifiers

The microwave amplifiers were one of the first applications of the GaN-based HEMTs due to their superior properties. In comparison to other materials the main advantages are the higher operating frequency and the reduced parasitic capacitances. The high electron concentration of the channel leads to high transconductance levels with low access resistance. The high breakdown field and the high current density allow to limit the parasitic capacitances, to decrease the device size and to improve the network matching. As seen before, the Johnson's figure of merit (JM) of GaN-based HEMT shows that is possible to reach high frequencies with higher operative voltages (see Figure 2.5). The cut-off frequency f_T is the frequency where the short circuit current gain of the transistor has unit magnitude [9].

$$f_T = \frac{g_m}{2\pi C_G} = \frac{v_s}{2\pi L}$$

In order to reach high cut-off frequencies values it is necessary to have high values of transconductance, low gate capacity and high values of saturation velocity. Theoretically, it is possible to increase f_T scaling the device, and thus decreasing the gate length. However, there can arise some disadvantages that

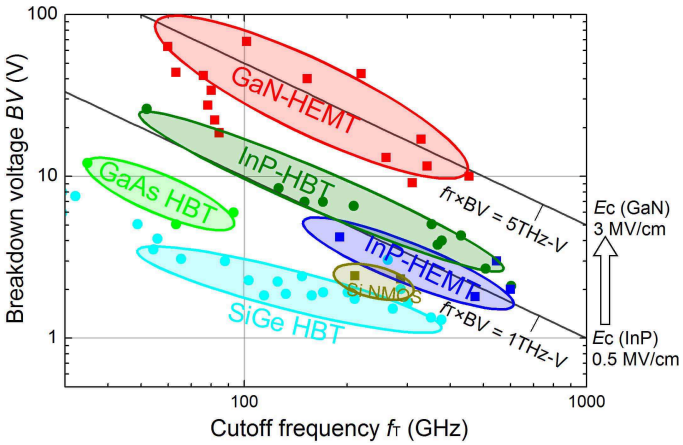


Figure 2.5: Comparison of JM among various high-speed device technologies [10].

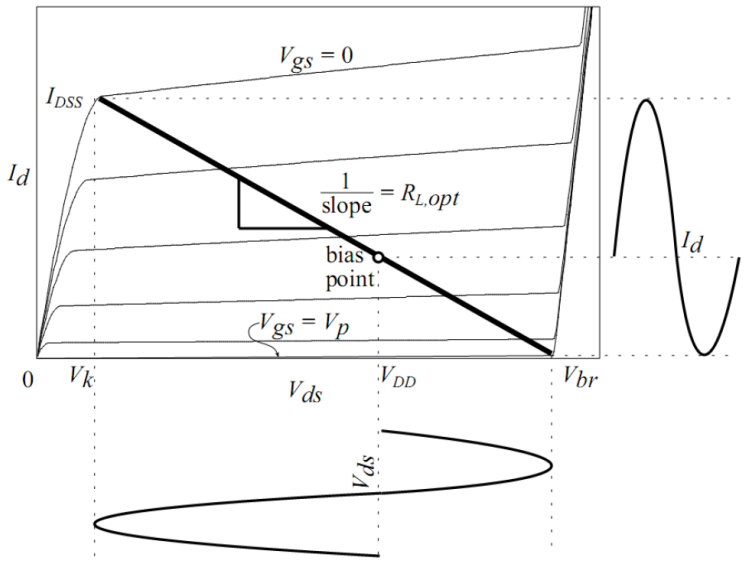


Figure 2.6: Device bias point and load-line for a class-A operation RF amplifier [9].

can limit the device performance, like short channel effects. Different solutions have been improved in order to overcome this problem, like self aligned gate process [10], n^+-GaN ohmic contact regrowth [11], a thin AlN top barrier [12], a InAlN top barrier [13], a AlGaN or InGaN back barrier [14], or N-polar GaN HEMT structure [15].

The typical application of the GaN HEMt in high-frequency is the class-A amplifier for better bandwidth and linearity, class-AB or B operation for higher efficiency. In the class-A configuration the bias point lies in the middle of the load line, that spread form the pinch-off to the knee region of the output characteristic (see Figure 2.6). The main parameters for the evaluation of the RF performances are the gain G, the power added efficiency $PAE\%$, and the maximum output power P_{out}. In order to maximize the available output power it is necessary to increase the critical pinch off voltage and decrease the knee voltage (reducing the on-resistance).

$$P_{out} = \frac{1}{2} \cdot \frac{1}{2}(V_{br} - V_{knee}) \cdot \frac{1}{2} I_{DSS} = \frac{(V_{br} - V_{knee})^2}{8\, R_L}$$

However, in the class-A configuration the power DC consumption is high, due to the bias point position, thus the maximum $PAE\%$ is limited only to 50%. The $PAE\%$ is defined as the ratio of the difference between the RF output and input power and the total DC power. This definition of efficiency takes into account both the RF gain and the energy dissipated by the DC bias.

$$PAE\% = \frac{P_{out} - P_{in}}{P_{DC}} \cdot 100\% = \frac{P_{out}}{P_{DC}} \left(1 - \frac{1}{G}\right) \cdot 100\%$$

Thermal management is fundamental in RF devices in order to be able to reach the maximal output power. The self-heating increases the channel temperature, decreasing the low-field carrier mobility and their saturation velocity. Therefore, it is fundamental to reach a high thermal conductivity and a good thermal management of the whole system, in order to obtain the highest power density and limit the size of the cooler [16][17]. For this reason the choice of the substrate is fundamental and SiC represent the best option. With this substrate it is also possible to obtain the best GaN crystal quality with a higher mobility, that is important for high frequencies operation [18]. Nevertheless, it is possible to use Si as substrate, that reduce the cost but has a worse thermal conduction and layer quality [19]. To improve the thermal conductivity beyond SiC it has been demonstrated that a diamond substrate allow to decrease the channel temperature of 25% at the same power dissipation level [20]. The drawback of this solution is that the diamond needs to be regrowth after the Silicon substrate removal, with an increase of the cost.

Looking at the best performances of RF GaN-based devices, already in 2004 *Wu et al.* demonstrated a 30 W/mm GaN-on-SiC device with 55% PAE at 4 GHz [21]; however, this was only a demonstration of the huge potential of this technology, and the output power was quite small for that frequency ($\approx$ 8 W). Recently *Custer et al.* reported a single transistor with output power of 1.2 kW in L-band at 1 GHz, with a power density of 30 W/mm and drain voltage of

150 V [22]. Fo radar applications in S-Band *Jardel et al.* reported a 30 W MMIC power amplifier with 46% PAE in the range of frequencies 2.7–3.7 GHz [23]. *Lu et al.* designed a power amplifier that can deliver a output power of 107 W at 5 GHZ (C-band) with 72% PAE [24]. Also for GaN-on-Si devices *Lee et al.* reported important RF performances with an 30 W amplifier in X-Band (8 GHz) with a power density of 8 W/mm [25]. In the field of space applications the Japanise JAXA ultra small deep-probe PROCYON, launched on December 2014, is equipped with an X-band telecommunication system based on a 15 W GaN single stage power amplifier [26]. The European Space Agency launched on May 2013 the Earth Observation satellite PROBA V, with a X-band telemetry system based on a 8 W MMIC GaN power amplifier [27]. For satellite communications *Friesicke et al.* realized a 10 W K-band MMIC power amplifier with 30% PAE at 19 GHz [28]; this result represent the state-of-the-art performance with regard to power/efficiency for the K-band. At higher frequencies, in the range off mm-waves, *Mikulla et al.* demonstrated a V-band GaN power amplifier with output power of 0.3 W at 63 GHz [29]. In the W-band *Niida et al.* reported a 1.1 W high-power-density MMIC amplifier with 12% PAE at 86 GHz [30]; its power density of 3.6 W/mm represents the highest performance in this band. At this high frequency range, also the GaN-on-Si technology recently reached remarkable results: *Marti et al.* designed a 68 mW MMIC power amplifier with 9% PAE at 94 GHz, and $f_T/f_{max} = 141/232$ GHz [31]. The best RF performances of GaN-based device reported in literature in terms of frequency are from *Tang et al.*, with $f_T/f_{max} = 454/444$ GHz [32].

2.3 Power Switching Transistors

The large critical electric field of GaN-based devices makes this technology promising for the switching applications. On power switching circuits, like DC-DC converter, there are electronic devices that switch from a high-voltage/low-current condition to a low-voltage/high-current condition. Therefore, the ideal device

should be a switch with no leakage in open condition and a negligible voltage drop in close condition, in order to minimalize the energy losses. Also during the switching phase it should be avoid to have both high voltage and high current conditions, for the optimization of the switching losses. On a real device this translate into a low leakage in off-state with high drain voltage, low on-state resistance and high subthreshold slope. GaN HEMTs can suit all these requirements thanks to the high breakdown voltage and the low resistance of the channel; the possibility to work with fast switching times at high frequency allow to shrink all the passive components.

The main parameter used for the device benchmark is the breakdown voltage limit versus the on-resistance. As is possible to see in Figure 2.7 the theoretical limit of GaN is above the Si technology and even beyond the SiC. The parameter that play a key role in the trade-off between breakdown and on-resistance is L_{GD}, the distance between drain and gate; higher L_{GD} leads to higher breakdown voltage but lower on-resistance; the actual range of L_{GD} for 600 V rated devices is between 15 μm and 20 μm [33].

On the switching applications the requirements in term of maximum frequency are not severe as for the RF devices, making the cheaper Silicon substrate the best

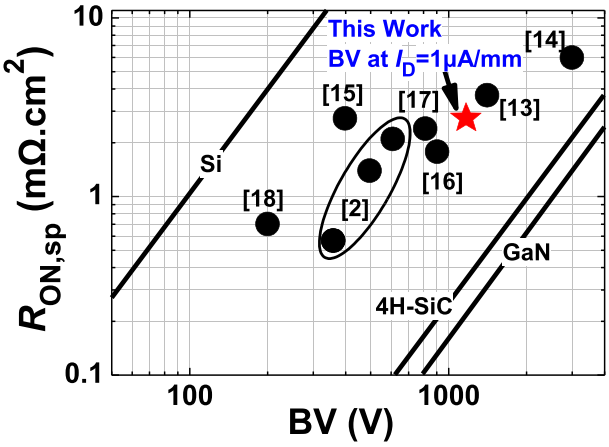


Figure 2.7: Specific on-resistance versus breakdown voltage of AlGaN/GaN MIS–HEMTs reported in the literature [34].

choice. In order to obtain an acceptable GaN crystal quality it is necessary to introduce an AlN nucleation layer between Si and GaN. One of the best solution is the *superlattice* structure proposed by *Ishida et al.* [35]; in this way it is possible to manage in the optimal way both the lattice and the thermal mismatch between Si and GaN. Due to the high voltage operation of the switching device it is fundamental to suppress the vertical leakage from the drain toward the bulk. The solution is to grow an u.i.d. (*unintentionally doped*) GaN for the channel over an insulating buffer layer. This bulk layer could be based on iron-doped GaN, carbon-doped GaN or AlGaN [36].

The devices for switching applications need a positive threshold voltage for safety reasons. In case of problems at the gate driver the gate could be at zero bias when the drain is in high voltage, and only a normally-off device can avoid the device failure in this case. Due to the spontaneous formation of the electron channel, GaN HEMTs born as depletion-mode devices, thus several solutions have been proposed in order to obtain an enhancement-mode device. In Figure 2.8 there is a sketch of the main adopted solutions for the normally-off devices. Growing a p-doped GaN [36] or AlGaN [39] under the gate allows to obtain positive threshold voltage (Figure 2.8 (a) and (b)), but in some cases the gate presented problems of reliability if biased over 5 V [40]. In Figure 2.8 (c) is depicted how by CF_4 is possible to inject negative charges in the AlGaN beneath the gate, depleting the channel at zero gate bias [41]. Another possibility is the etching of the gate as reported by *Anderson et al.* [42] (see Figure 2.8 (d)); in this case it is critical to control the thickness of the recess and there are problems with traps in the insulator. It is even possible to improve an insulated version of the etched device (see Figure 2.8 (e)) as proposed by *Chu et al.* [43]. If the recess is deep enough to completely remove all the AlGaN, the 2DEG is removed under the gate and the resulting structure is called a Hybrid MOS-HFET [44] (see Figure 2.8 (f)). The last method to reach a normally-off device is to incorporate a low-voltage enhancement-mode Si MOSFET in a cascode structure, as shown in Figure 2.8 (g). In this way the gate could be easily controlled, even if cascode

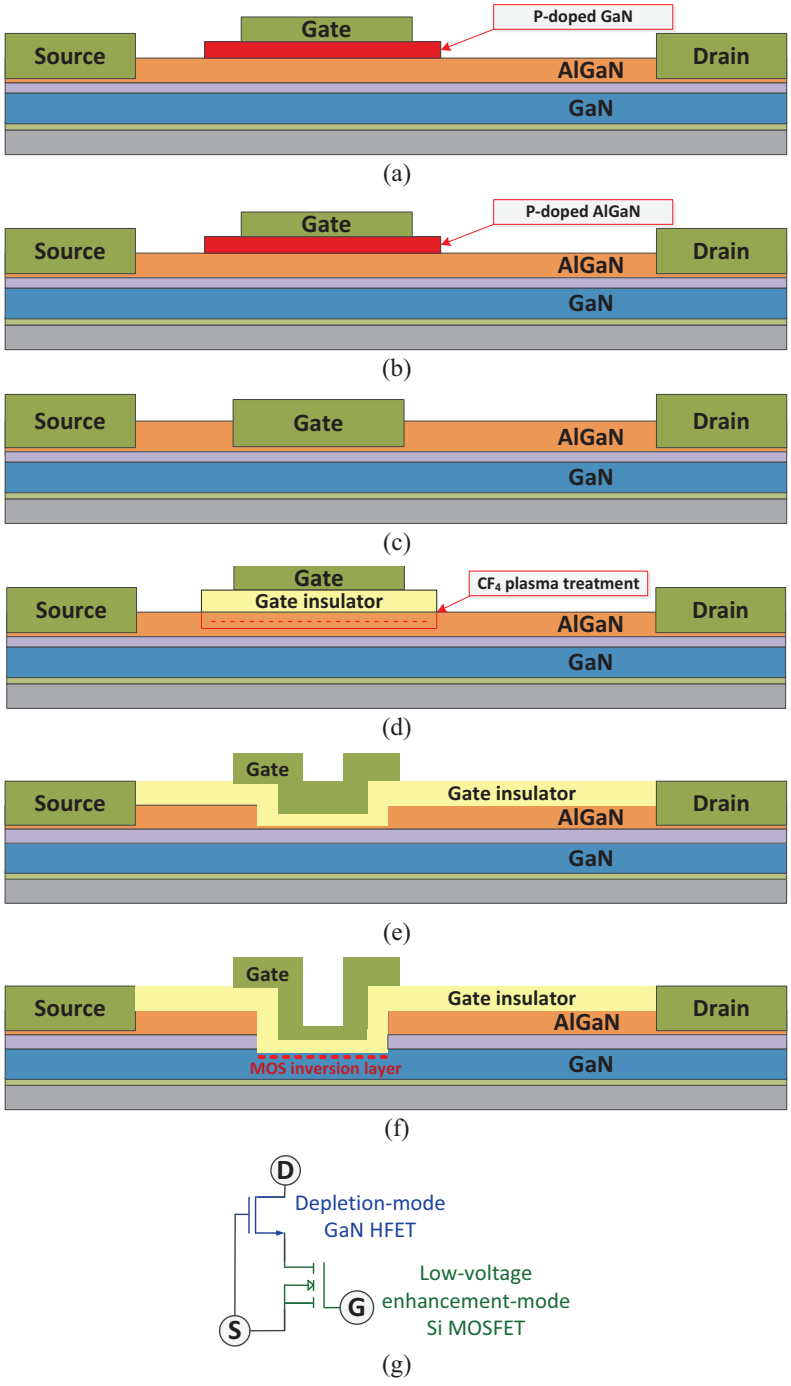


Figure 2.8: Methods to build a normally-off GaN HFET (a) p-doped GaN under gate; (b) p-doped AlGaN under gate; (c) Recessed gate; (d) Plasma treatment under gate; (e) Recessed AlN gate insulator; (f) Hybrid MOS-HFET; (g) cascode structure [37].

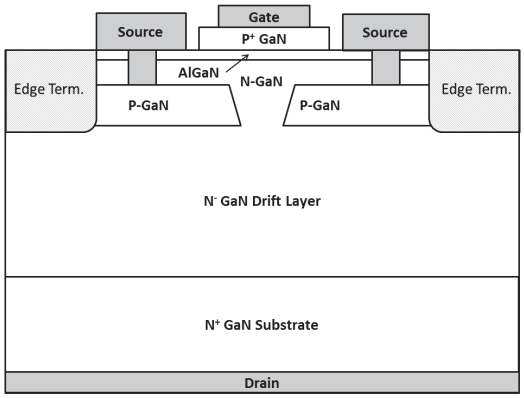


Figure 2.9: Schematic cross-section of the CAVET vertical normally-off GaN transistor [38].

package parasitic could be higher [45]; but with an accurate optimization it is possible to reach remarkable results [46]. Another limitation of the cascode solution is that the HEMT in on-state works always at $V_{GS} = 0\,V$, without the possibility to tune the gate overdrive, and thus exploiting the full transistor potential.

The d-mode devices developed for the cascode configuration are MIS (*Metal-Insulator-Semiconductor*) GaN HEMT. The quality of the insulator between the AlGaN and the gate is fundamental for the device reliability [47]. The insulator could be made of Si_3N_4 [34][48] or Al_2O_3 [49].

Another topology of power HEMT is the CAVET (Current Aperture Vertical Electron Transistor). As is possible to see in Figure 2.9, in this solution the drain is on the bottom, while the source and the gate are on the top. The vertical current flow is no more in the electron channel beneath the gate but is flowing in the u.i.d. GaN. In this way there is no more the necessity to include an insulating bulk layer to prevent the vertical leakage. In order to limit on-resistance the thickness of the drift layer is comparable to the L_{GD} of a lateral device.

Even tough Silicon is the more affordable subsrtate for the power device market, GaN transistrs grown on Silicon Carbide show outstanding performances and better heat dissipation [50]. Recently, *Baltynov et al.* demonstrated a GaN-on-diamond power HEMT [51]; this solution allow a heat dissipation even better

than SiC, that could be crucial for the applications that need to dissipate large amounts of heat power.

Looking at the state of the art of the power GaN HEMT technology, *Hilt et al.* reported a 600 V normally-off transistor with on-resistance of 70 mΩ [52]. For the normally-on devices *Moens et al.* presented 650 V devices with the on-resistance record value of 6 mΩ with a 100 A current; the 1.2 kV rated transistors instead work in the 120 mΩ/20 A range [53]. Considering the applications of the power HEMT, *Ramachandran et al.* demonstrated a 98.8% DC-DC bidirectional isolated converter with output power of 1.7 kW [54]. *Lei et al.* designed a 2 kW inverter with a peak efficiency of 97.6% [55]; in this project the dimensions of the inverter was optimized achieving a power/volume ratio of 13.2 W/cm^3.

2.4 Trapping effects

In the semiconductor materials there is always a lattice defectivity due to atoms vacancies, to undesired elements and to the lattice mismatch. The defects can behave as trap-states with a defined energy level located into the energy gap, leading to dynamic charge trapping phenomena. Since the defectivity and the presence of impurities in the Gallium Nitride is difficult to decrease under a definite level, the trapping effects represent one of the major limiting factor of

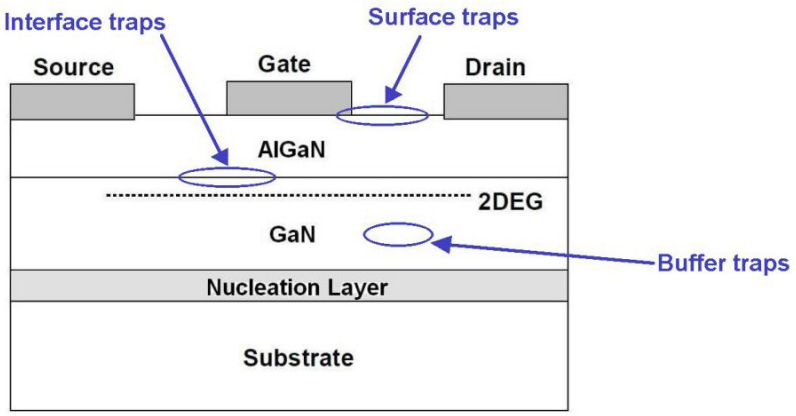


Figure 2.10: Typical localizations of traps in a AlGaN/GaN HEMT.

the GaN HEMT. This was a serious issue in the early stages of the technology, while nowadays a lot of efforts has been made, leading to better devices. As depicted in Fifure 2.10, the traps could be located in different device's regions, like the surface, the interface or the buffer. Due to different operation mode of the RF and the power devices the effects of the traps are different. Therefore, they will be treated separately in the next two sections.

2.4.1 Trapping effects in RF devices

In section 2.2 we have seen how, during the operation of a RF transistor in an amplifier, it spreads over a loadline in the saturation region (see Figure 2.6 at pag. 10). This mean that the transistor alternate from a pinch-off condition with high voltage, to a low-voltage/high-current condition; the loadline could be slightly different, depending on the operation class of the amplifier. When the transistor is close to the off-state condition it could happen that some negative charge is trapped in the gate-drain region, expanding the depletion region beyond the gate. When the transistor is turned on again this charge needs time to detrap, and the additional depletion region acts like a *virtual gate* that keeps the transistor still in a pinch-off condition (see Figure 2.11). The result is that the output characteristics of the transistor is worsening, with a decrease of the output current; this phenomena is well known as *current collapse* [56][57].

In the first generations of AlGaN/GaN HEMTs the charge trapping was mainly due to the surface states over the AlGaN [58]. This problem has been overcome implementing a SiN passivation layer over the AlGaN [59] and with the introduction of *field plate* structures, for decreasing the electric field in the drain access region, and consequently the injection of electrons into the trap states [60].

However, as shown in Figure 2.10, the traps can be located not only at the surface, but even in other device regions. The effect of the charging and discharging of this traps is similar to the virtual gate-effect. When a potential is applied to the gate and/or the drain terminal the band diagram of the structure bends, and it is possible that in some region the position of the Fermi level changes,

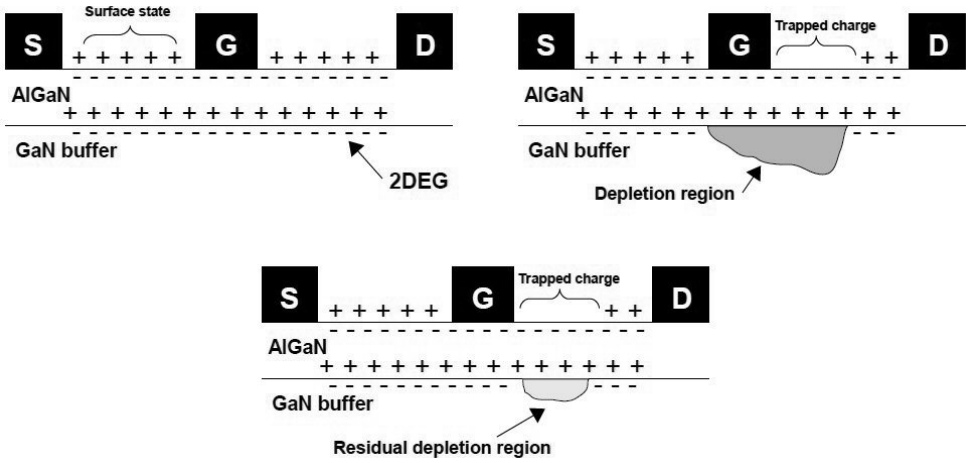


Figure 2.11: Schematic explanation of current collapse in AlGaN/GaN HEMT [61].

and consequently some trap states can be filled or depleted, depending on their position. In Gallium Nitride most of the trap states are donors, located in the upper part of the band-gap, or acceptors in the bottom part (see Figure 2.12). In the case of u.i.d. GaN the Fermi level is typically located at $E_F = E_C - 0.2$ eV, similar to the situation depicted in Figure 2.12 (c). In this case, while is difficult to change the filling of acceptor traps, the Fermi level could be very close to the donor states, and changing its position will change the filling of this traps. For example, if a donor trap that was above E_F goes below it, it needs a definite time to be filled. During this time there will be an additional positive charge that changes the shape of the band diagram. The effects of this processes on the device behaviour is indeed the current collapse, since the 2DEG channel needs time to be fully restored after the trapping phase.

The main techniques to investigate the effects of trapping phenomena on the devices are the pulsed measurements and the DLTS (Deep Level Transient Spectroscopy) [63]. With the pulsed measurements it is possible to see immediately the current collapse on the output characteristic and on the transcharacteristic. In this way it is possible to discriminate how different trapping conditions can affect the pulsed behaviour, and to obtain information about the position of the

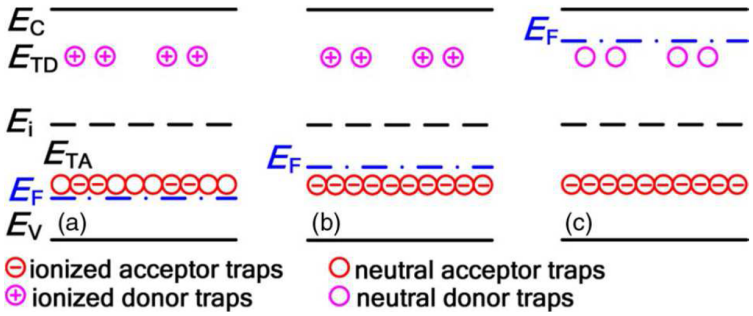


Figure 2.12: Typical localizations of trap states in the band-gap of Gallium Nitride with different positions of the Fermi level E_F [62].

traps in the transistor structure. If the traps are located under the gate region it is possible to see a threshold shift, while if they are located even in the drain access region we will see the current collapse and a decrease in the transconductance peak. The limit of the pulsed measurements is that we can see the effects of the trapping phenomena only for a determinate time scale. The typical pulse timing has a period of 100 μs with the on-state pulse duration of 1 μs. However, the detrapping has a dynamic that get lost looking only at the pulsed measurements. After the trapping pulse, when the trapping phase should be finished, it would be useful to follow the trend of the current recovery in a wide time range. This is the operating principle of the DLTS, where the trend of the current in a determinate bias point is measured over several time decades. This technique has been pioneered by Lang yet in 1974 [64]. The powerful of the DLTS is that it is possible to see the dynamic of the detrapping phenomena over a typical time range of 1 μs - 100 s. This is fundamental to understand how much the trapping can affect the device operation at different operative frequencies. Furthermore, performing the DLTS analysis at different temperatures it is possible to investigate the activation energy and the cross section of the trapping process, that represent the signature of the trap. The activation energy of the detrapping process is related to the distance of the trap from the conduction band (or from the valence band in the case of hole traps). *Bisi et al.* [65] made a collection of several trap signature found in literature, correlating them with the nature and

the origin of the trap. In this way it is possible to compare the data with the database and try to understand the possible origin of the trap. In case the trap is not thermally activated it is possible that the trapping process is not originated from the emission from a deep level, but could be related to some tunnelling process; in some cases this kind of traps originates from interface states (probably at the interface between the AlGaN an the gate metal) and the time constant could be broadened over several time decades, even if it is in general faster than 1 ms.

All the presented trapping characterization techniques can explore several bias points both for trapping and detrapping, but in the real device operation the transistor will work along the loadline with a frequency of many GHz. To understand how the trapping influences the RF operation, recently *Benvegnù et al.* [66] proposed a new technique that uses a large RF signal filling pulse instead of the classical DC one. It this work it is shown how the power of the RF signal and its duration have different impact on trapping.

2.4.2 Trapping effects in power devices

The basic trapping mechanisms presented in the previous section apply as well to the power devices. The main difference is the operation principle: while in the RF devices the transistor works as an amplifier, in the power devices it works as a switch. During the off-state phase of the switching operation the device goes into a trapping condition. The channel is pinched-off and the drain needs to sustain the off-state voltage, that in the current technology is rated at 600 V. In this condition is very easy to inject electrons both from the source and the gate into the drain access region. During the on-state phase the drain voltage goes down to a low value (typically around 1 V), thus, the transistor operates in linear region; this is the reason why for power devices is take into consideration the on-resistance R_{on} as fundamental parameter for minimizing the conduction losses. For power devices we prefer to consider the dynamic R_{on} increase instead of the current collapse; indeed, after a trapping phase, the slope of the I-V curve will become lower, increasing the on-resistance [67].

Since a high voltage is applied to the drain, in the power device the bulk leakage can represent a problem. The small current flowing from the drain to the substrate can lead to a trapping mechanism with a different dynamic. While in general we focus on the detrapping phase, in this case we should consider the trapping phase too. *Bisi et al.* demonstrated that the capture rate of the trapping mechanism can be related to the bulk leakage level [68]; the activation energy of the process could be extracted also for the trapping process, and the bulk current play a key role in this process. Afterwards, *Meneghini et al.* [69] shown how the contribute of the bulk current on the the trapping could be separated comparing measurements with different bias conditions, among which the *backgating*, where a negative bias is applied to the substrate (see schematic in Figure 2.13). The buffer-related trapping could be ascribed to the presence of Carbon in the insulating GaN layer. With a proper buffer design it is possible to limit the vertical leakage, and thus minimizing the dynamic R_{on} increase.

The typical switching frequencies of a converter could be in the range 100 kHz - 1 MHz, but it could be enough to activate the trapping processes. Even tough the trapping time could have time constants of 10 - 100 s, the detrapping is slow too, and the trapping can gradually cumulate, leading to the R_{on} increase.

During the switching operation the device can move from the off-state to the

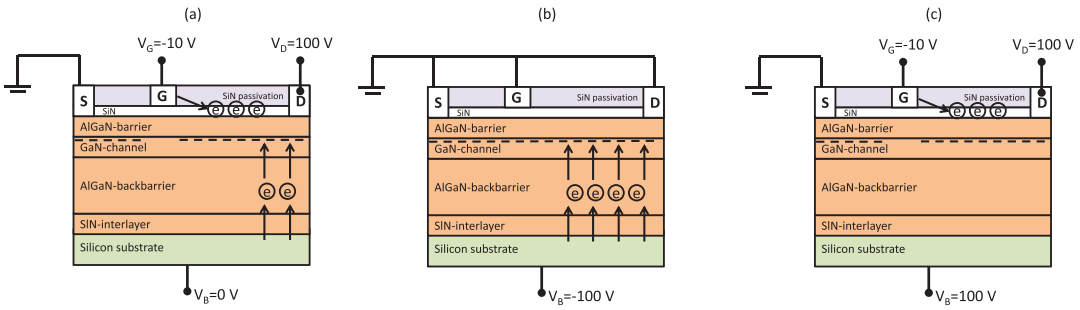


Figure 2.13: Schematic representation of different bias conditions for investigating the buffer-related trapping: (a) off-state; (b) backgating; (c) off-state with positive substrate [69].

on-state bias point through a loadline. Since the load is not resistive this loadline could pass through a high-voltage/high current region (hard switching) or to a low-voltage/low-current region (soft switching), depending on the converter topology. In order to investigate the impact of the different switching modes on the R_{on} increase, *Joh et al.* demonstrated that the hard-switching solution can give better results [70].

2.5 Reliability issues

It is fundamental to guarantee the stability of the performances in the operative conditions for a transistor in all its lifetime. Thus, we need to understand the main degradation mechanisms and failure modes, in order to improve the GaN HEMT technology. The main degradation aspects are represented in Figure 2.14 and can be divided into three typologies:

- mechanisms related to the AlGaN/GaN structure, such as the degradation

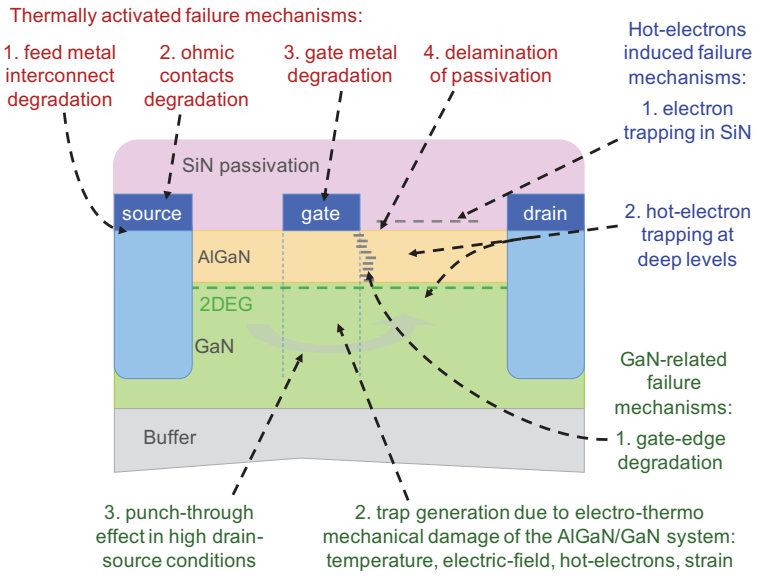


Figure 2.14: Schematic figure representing the main mechanisms that can affect the reliability of GaN-based HEMTs [71].

at the gate edge caused by an high electric field, the creation of defects, and the converse piezoelectric effect;

- effects of hot-electrons, which include the trapping of carriers in several device regions and the increase of defectivity;

- thermally activated failure mechanisms, like changes of the ohmic and Schottky contacts, metal interdiffusion, electrochemical surface degradation and impurities diffusion.

Furthermore, there are some failure modes that are peculiar of power devices and they will be traded separately.

2.5.1 GaN-related failure mechanism

The drain-side gate edge is one of the more critical region of the transistor, since is where the electric field reaches the highest values. In off-state bias, with a high voltage on the drain, a lot of defects can be generated, increasing the gate leakage current driven by trap-assisted tunnelling of electrons from the gate through the AlGaN barrier [72]. One of the reason of the increase in defectivity is the converse piezoelectric effect. Due to piezoelectric properties of AlGaN and GaN, the high electric field level can induce an additional tensile stress in the AlGaN layer, that could be enough to generate lattice defects [73].

Another issue appears when the device is stressed with the gate at negative voltage and at zero drain bias: in the beginning the gate leakage current drops due to the trapping of electrons, then the current starts to be noisy and eventually it exhibits a sharp variation. The dynamic of this process depends on the applied voltage and on the initial leakage value. This phenomenon is well know as time-dependent AlGaN breakdown and it is similar at the dielectric breakdown mechanism. The dynamic creation and fixing of defects is responsible of the noisy current, while the last sudden increase is due to the creation of a large percolative path [74].

During a off-state stress with the drain bias applied is possible to observe the generations of pits at the drain side of the gate. This process depends on the voltage applied to the drain, on the stress time, and on the temperature [75].

2.5.2 Hot electrons-induced failure mechanisms

In presence of high electric filed, some electrons can become more energetic, namely *hot electrons*. They can cause both trapping phenomena and physical damages of the crystal lattice, with defects generation. It is possible to detect the presence of hot electrons since they interact with the lattice by *bremsstrahlung*, with a consequent photon emission, the electroluminescence [77]. This emission

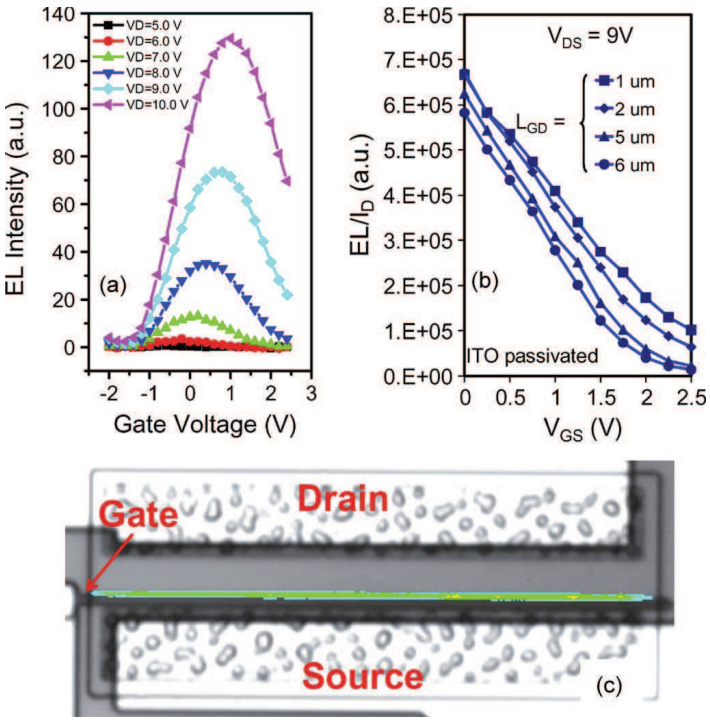


Figure 2.15: (a) Intensity of the EL signal as a function of gate and drain voltage; (b) EL/I_D intensity as a function of the gate voltage level for samples with different gate-drain spacing; (c) false colour image reporting the distribution of EL along the gate [76].

has a typical bell-shaped trend (see Figure 2.15 (a)) as function of the gate voltage, and the level is higher at higher drain voltages. In Figure 2.15 (c) we can see how the emission is concentrated on the drain side edge of the gate, where the electric field is higher.

During an on-state stress it is possible to observe hot electrons-related degradation [78]. During the test is possible to observe a drop in the output current and the degradation rate is strongly dependent on the intensity of the EL signal, which is related to the concentration of hot electrons in the channel. Different tests, carried out at different gate voltages and the same drain voltages show a evident correlation with the current degradation and the EL intensity.

Puzyrev et al. demonstrated, by means of simulations, that the energy distribution of the hot electrons can be related to the dehidrogenation of the Ga vacancy – Hydrogen complex [79]. This work shows in detail how the hot electrons can increase the lattice defectivity, and thus affect the device performances.

2.5.3 Thermally activated failure mechanisms

When the devices are submitted to high temperature stress, is possible to observe a degradation of the contacts, more for the Schottky gate than for the ohmics. Several works in literature report different problems originated from the Au migration thorough the Ni towards the AlGaN. *Vitobello et al.* reported a positive threshold voltage shift [80], while *Zhao et al.* shown an increase of the Schottky barrier height associated with a decrease of the ideality factor [81].

Another process activated by temperature is the diffusion of impurity from the surface to the AlGaN layer during off-state and on-state stress [82]. In this case the generation of new trap levels after the stress has been reported, and the region where the degradation takes place is always the drain side of the gate. This hypothesis is confirmed by another work, whit the aim of UV-light assisted trapping analysis [83].

2.5.4 Degradation mechanism of power devices

In the case of the d-mode MIS GaN-based HEMT, most of the problems reported above still hold [67], excluding the effects related to the Schottky gate, since now there is an insulator in between. It is indeed the insulator to generate other kind of problems related to charge trapping, that sometime are not fully recoverable, or with very slow detrapping time constant, that can represent a reliability issue. It is possible to separate two different situations depending on the gate bias during the stress: in case of forward gate bias we have PBTI (*Positive Bias-induced Threshold voltage Instability*), while in reverse bias we have NBTI (*Negative Bias-induced Threshold voltage Instability*). In the case of PBTI we can observe a positive threshold voltage shift due to negative charge trapping in the AlGaN/dielectric interface and into the insulator [84]. Conversely, for NBTI we observe a negative threshold voltage shift due to the emission of the electron from the insulator [47].

In the case of e-mode pGaN power HEMT there are reliability problems when the gate is in forward bias. The gate overdrive is thus limited from the lifetime of the device, that decrease increasing the gate voltage. The TTF (*Time To Failure*) depends on the stress voltage and is Weibull-distributed [85][40]. Recently, *Smith et al.* reported an extensive life time analysis both in on-state and in off-state conditions, demonstrating that the new technology is ready for commercial and industrial applications [86].

Chapter 3

Physically based device simulations

3.1 Introduction to GaN-based HEMT physically based simulation

GaN-based devices like AlGaN/GaN HEMTs are relatively new type of semiconductor devices and therefore the practical and experimental common knowledge, are, unlike Silicon devices, very limited. During the technological development is very expensive and time consuming to try several design and process solutions. The device designer needs a reliable tool for prediction of the device performances in short time and at low cost before the mask set manufacturing and the epitaxial growth. A common and useful tool for design and prediction of semiconductor devices is the physically-based device simulation, that can predict the electrical characteristics that are associated with specified physical structures and bias conditions. This is achieved by approximating the device operation onto a two dimensional grid, consisting of a number of grid points called nodes. By applying a set of differential equations, derived from Maxwell's laws, onto this grid, we can simulate the carrier transport through the structure. This means that the electrical performances of the device can be modeled in DC, AC or transient operation modes. Physically-based simulation is predictive and provides insight to the device, capturing and visualizing theoretical knowledge. The main reasons why physically-based simulation became very important are, first, because

it is almost always quicker and cheaper than performing experiments; then, it provides information that is difficult or impossible to measure. The drawback of physically-based simulation is that all the relevant physic must be incorporated into a simulator. Then, numerical procedures must be implemented to solve the associate equations [87].

I was introduced in the world of physically based simulation during my period abroad, by FBH in Berlin, thanks to Dr. Eldad Bahat-Treidel. The target was to improve a model developed there, in order to better understand some critical aspects of the devices behaviour. In particular, we wanted to identify the possible degradation mechanisms during the stress test that I carried out during the same period. This one of the case where the simulation can be helpful, not only during the first technology development, but also to deeper understand some details of the device behaviour. For my personal experience I can say that the simulator can play also a "didactic" role. For the students, but also for who approaches for the first time the GaN-based HEMT technology, it can be a powerful instrument that allow to visualize the band diagrams and the device layout. Changing several parameters is possible to see how they can impact on the device performances, giving a immediate and deep understanding of the basic device operation, as the epitaxial growth details.

3.2 Basic modeling of the Physically based simulator

Silvaco ATLAS [88] is a physically based simulator that uses a mathematical model to describe semiconductor devices. This model consists of a set of fundamental equations, which link together the electrostatic potential and the carrier densities, within a simulation domain. These equations, which are solved inside any general purpose device simulator, have been derived from Maxwell's laws and consist of Poisson's equation, the continuity equations and the transport equations. Poisson's equation relates variations in electrostatic potential to local

charge density:

$$div(\varepsilon \nabla \psi) = -\rho \tag{3.1}$$

where ψ is the electrostatic potential, ε is the local permittivity, and ρ is the local space charge density. The local space charge density is the sum of contributions from all mobile and fixed charges, including electrons, holes, and ionized impurities. The electric field is obtained from the gradient of the potential:

$$\vec{E} = -\nabla \psi \tag{3.2}$$

The continuity equations for electrons and holes are defined as:

$$\frac{\partial n}{\partial t} = \frac{1}{q} div \vec{J_n} + G_n - R_n \tag{3.3}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q} div \vec{J_p} + G_p - R_p \tag{3.4}$$

where n and p are the electrons and holes concentration, $\vec{J_n}$ and $\vec{J_p}$ are the electrons and holes current densities, G_n and G_p are the generation rates for electrons and holes, R_n and R_p are the recombination rates for electrons and holes, and q is the electron charge.

Poisson's equation (Eq. 3.1) and the carrier continuity equation (Eq. 3.3 and Eq. 3.4) provide the general framework for device simulation, but further equations are required to specify particular physical models for $\vec{J_n}$, $\vec{J_p}$, G_n, G_p, R_n and R_p. The current density equations, or charge transport models, are usually obtained by applying approximations and simplifications to the Boltzman transport equation. These assumptions can lead to a number of different transport models such as the drift-diffusion model, the energy balance transport model, or the hydrodynamic model. The choice of the charge transport model will then have a major influence on the choice of generation and recombination models.

The simplest model for charge transport is the drift-diffusion model, that has the attractive feature that it does not introduce any independent variables in addition to ψ, n and p. Until few years ago, the drfit-diffusion model was adequate for most of the devices, but became less accurate for smaller feature

size. More advanced energy balance and Hydrodynamic models are therefore becoming popular for simulating deep submicron devices.

Silvaco ATLAS uses an internal 2D device simulator, BLAZE, for III-V, II-IV materials, and devices with position dependent band structure (e.g. heterojunctions). BLAZE accounts for the effects of positionally dependent band structures by modifications of the charge transport equations and Poisson's equation. BLAZE is applicable to a broad range of devices such as: HBTs, HEMTs, LEDs, lasers, heterojunction photodetectors an diodes.

GIGA is an internal simulator that extends ATLAS to account for lattice heat flow and general thermal environments. GIGA implements Wachutka's thermodynamically rigorous model of lattice heating [89], which accounts for Joule heating, heating and cooling due to carrier generation and recombination, the Peltier and the Thomson effects. It accounts for the dependence of material and transport parameters on the lattice temperature. It also supports the specification of general thermal environments using a combination of realistic heat-sink structures, thermal impedances, and specified ambient temperatures. GIGA works with BLAZE and with both the drift-diffusion and energy balance transport models.

3.3 Simulation structures, models and parameters

The following section describes the methodology used in the physically based simulations on nitride based HEMTs devices. It is desired to match the simulation output characteristics to the actual electrical and physical device performance. The simulation manual recommends the models to use and has a built-in material parameters table based on the latest research results. Unfortunately, it is not enough, since the simulator miss some models for an accurate description of a GaN-based HEMT. Therefore, additional models along with empirical modifications in the existing models are required in order to achieve a useful tool for the device designer and researcher as a first order approximation.

3.3.1 Structure and mesh definition for the simulation

Exact definition of the structure for the simulation is one of the basic keys to match the simulated electrical characteristic to the experimental measurements. The structure should match the wafer substrate, the epitaxial layers growth, and the device layers layout.

The transistor generation chosen for the simulation was developed by FBH within the HipoSwitch project and was one of the devices submitted to stress test during my activity by FBH. The structure is based on semi-insulating 4H-SiC substrate. The epitaxial growth layers are defined exactly as in the reference wafer: 50 nm AlN layer, 2.85 μm Fe-doped GaN buffer layer, 850 nm of u.i.d. GaN and 9 nm of $Al_{0.25}Ga_{0.75}N$ barrier layer; over the AlGaN, in the gate region is added a 100 nm of Mg-doped p-GaN layer. In Figure 3.1 it is possible to see the device structure, while in Figure 3.2 we can observe a magnification over the gate area in order to see the details of that region. The device geometry has gate width $W_G = 2 \times 1600\,\mu\text{m} = 3.2\,\text{mm}$, gate length $L_G = 1.1\,\mu\text{m}$, gate-source distance $L_{GS} = 1.0\,\mu\text{m}$, and gate-drain distance $L_{GD} = 15\,\mu\text{m}$.

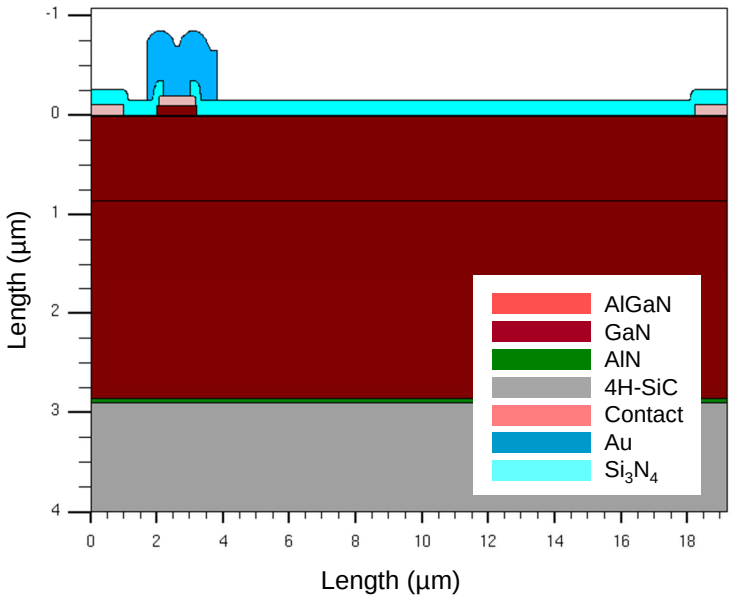


Figure 3.1: Basic simulation structure of the analysed device.

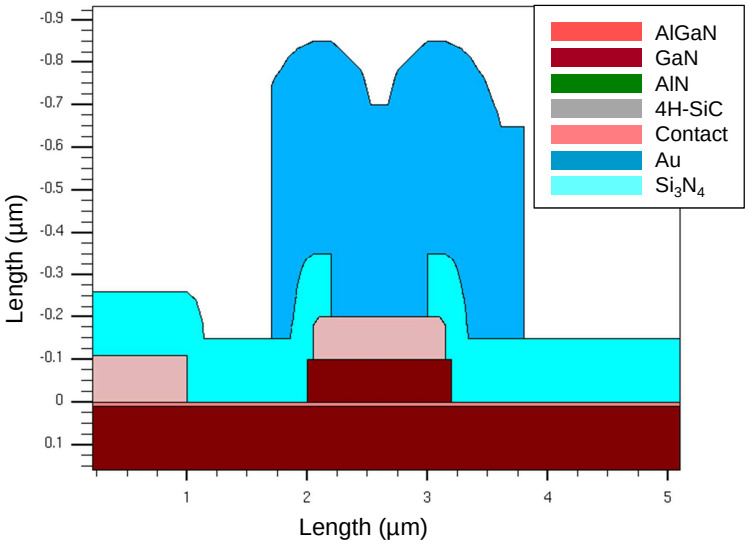


Figure 3.2: Gate area detail of the simulation structure.

Next step after the device structure creation is to generate an adequate mesh which could be used by Silvaco ATLAS simulator. Specifying a good grid is a crucial issue in device simulation. But, there is a trade-off between the requirement of accuracy and numerical efficiency. A fine grid is required to obtain an accurate simulation, while numerical efficiency is greater when fewer grid points is adopted, with a consequential reduction of simulation time. The critical areas to resolve are difficult to generalize because they depend on the technology and the transport phenomena. In general they can be in regions where there is a huge spatial gradient of quantities like current density and electric field. Typical critical areas in Gan-based HEMTs are: around heterojunctions and interfaces and areas with high vertical electric fields, like the AlGaN layer.

3.3.2 Material parameters and physical models

The simulation of GaN-based HEMTs using Silvaco ATLAS requires specific definitions and use of the physical models that describe the material properties of nitride compounds. Silvaco ATLAS contains many built-in physical models and material properties that can be used to simulate the devices. In the following

there are reported the more critical models adopted in my simulations.

Nitride material properties: bandgap, electron affinty, permittivity, and density of state masses

Here are described the relationships between mole fraction x, and the material parameters and various physical models specific to the $Al_xGa_{1-x}N$ system. By default the bandagaps of the binary compounds are computed as function of temperature T using [90]:

$$E_g(\mathrm{GaN}) = 3.507\,\mathrm{eV} - \frac{9.09 \times 10^{-4}\,\mathrm{eV/K} \cdot T^2}{T + 830\,\mathrm{K}} \tag{3.5}$$

$$E_g(\mathrm{AlN}) = 1.994\,\mathrm{eV} - \frac{2.45 \times 10^{-4}\,\mathrm{eV/K} \cdot T^2}{T - 624\,\mathrm{K}} \tag{3.6}$$

Then, the dependence on composition fraction x is described by [91]:

$$E_g(\mathrm{Al_xGa_{1-x}N}) = E_g(\mathrm{AlN})x + E_g(\mathrm{GaN})(1-x) - 1.3\,\mathrm{eV}\,x(1-x) \tag{3.7}$$

The electron affinity is calculated such that the band edge offset ratio is given by [91]:

$$\frac{\Delta E_C}{\Delta E_V} = \frac{0.7}{0.3} \tag{3.8}$$

However, there is the possibility to manually change the heterojunction alignment or to define the electron affinities.

The permittivity of the nitrides as a function of composition fraction x, is given by linear interpolation of the values from the binary compounds [5]:

$$\varepsilon_r(\mathrm{Al_xGa_{1-x}N}) = (-0.3x + 10.4)\,\varepsilon_0 \tag{3.9}$$

The nitride desity of states messes as a function of composition fraction x, is given by linear interpolation of the values from the binary compounds [90]:

$$m_e(\mathrm{Al_xGa_{1-x}N}) = 0.314x + 0.2(1-x) \tag{3.10}$$

$$m_h(\mathrm{Al_xGa_{1-x}N}) = 0.417x + 1.0(1-x) \tag{3.11}$$

Epitaxial strain tensor calculation in wurtzite materials and built-in polarization models

The strain tensor in epitaxial layers is used to calculate the piezoelectric polarization [92][93]. In epitaxial layers, the strain tensor can be represented by the parameters ε_{xx}, ε_{yy}, ε_{zz}, ε_{xy}, ε_{yz}, and ε_{zx}, . The relationships between the various components of the strain tensor are given by:

$$\varepsilon_{xx} = \varepsilon_{yy} = \frac{a_s - a_0}{a_0} \tag{3.12}$$

$$\varepsilon_{zz} = -2\,\frac{C_{13}}{C_{33}}\,\varepsilon_{xx} \tag{3.13}$$

$$\varepsilon_{xy} = \varepsilon_{yz} = \varepsilon_{zx} = 0 \tag{3.14}$$

where C_{13} and C_{33} are the elastic constants, a_0 is the lattice constant in the reference substrate and a_s is the average value of the lattice constants of the layer directly above and below the layer in question. The difference $a_s - a_0$ represents indeed the amount of lattice mismatch.

Polarization in wurtzite materials is characterized by two components: spontaneous polarization P_{sp} and piezoelectric polarization P_{pi}. Therefore, the total polarization P_{total} is given by;

$$P_{total} = P_{sp} + P_{pi} \tag{3.15}$$

The piezoelectric polarization is given by:

$$P_{pi} = 2\,\frac{a_s - a_0}{a_0}\left(e_{31} - \frac{C_{13}}{C_{33}}\,e_{33}\right) \tag{3.16}$$

where e_{31} and e_{33} are piezoelectric constants. The total polarization into the simulation is represented as a positive or negative fixed charges at the heterojunction interface. By default, for the spontaneous polarization, the positive charge is added at the bottom and the negative charge is added on the top. This is in line with the situation in a Ga-face lattice.

In the real lattice the piezoelectric and spontaneous polarization are lower than the theoretical one. It is possible to notice it in the 2DEG at the AlGaN/GaN

interface. Parameters like the threshold voltage and the amount of charge in the channel are very sensitive to the amount of positive polarization charge at that heterojunction. Thus, to match the simulations with the measurements, all the polarization vectors are scaled by 70%.

Carrier mobility models

Unlike Si, GaN exhibits a negative differential mobility for electrons at very high fields, so a dual mobility model approach is necessary for GaN, one for the low field positive differential region and the other for the high field negative differential region [94]. Unlike electrons, the hole mobility does not show a negative differential mobility region and tends to saturate at high fields, thus, it is considered only the low field mobility model for holes.

For the low field mobility I chosen the model developed from *Albrecht et al.* [95]. It is a temperature and ionized impurity concentration dependent model, expressly developed for GaN, based on Monte Carlo simulations. The model is described as follows:

$$\begin{aligned}\frac{1}{\mu_0(N,T)} &= a\left(\frac{N}{10^{17}\,\mathrm{cm}^{-3}}\right)\left(\frac{T}{300\,\mathrm{K}}\right)^{-\frac{3}{2}}\ln\left[1+3\left(\frac{T}{300\,\mathrm{K}}\right)^{2}\left(\frac{N}{10^{17}\,\mathrm{cm}^{-3}}\right)^{-\frac{2}{3}}\right]+ \\ &\quad + b\left(\frac{T}{300\,\mathrm{K}}\right)^{\frac{3}{2}}+\frac{c}{\exp\left(\frac{1065\,\mathrm{K}}{T}\right)-1}\end{aligned} \tag{3.17}$$

where $\mu_0(N,T)$ is the mobility as function of doping N and temperature T, while a, b and c are parameters that should be fitted on the real electrical device output characteristics. The chosen values for my simulations are summarized in Table 3.1. The parameters are specified both for electrons and holes mobility; since in the analysed structure there is a p-doped region it is fundamental to consider also the mobility for holes. However, as is possible to see in Table 1.1, the parameters a and b from holes are several order of magnitude higher that those for electrons. The reason is that the Albrecht model has been developed only for electrons, and in principle could be not valid for holes. However, since the reported temperature trend for the hole mobility is similar to the electron one [96],

Table 3.1: Parameters used in the Albrecht low field mobility model.

parameter	electrons ($V \cdot s/cm^2$)	holes ($V \cdot s/cm^2$)
a	1.5×10^{-4}	1.0×10^{3}
b	1.5×10^{-4}	1.0×10^{3}
c	1.7×10^{-2}	1.7×10^{-2}

we can use the same model, fitting the parameters to the mobility measurements. In my case the measured Hall mobility of the Mg-doped p-GaN was 7 $cm^2/V \cdot s$.

For the high field mobility we need to use a field dependent model, developed by *Farahmand et al.* [97]:

$$\mu(E) = \frac{\mu_0(T,N) + v_{sat}\dfrac{E^{n_1-1}}{E_c^{n_1}}}{1 + a\left(\dfrac{E}{E_c}\right)^{n_2} + \left(\dfrac{E}{E_c}\right)^{n_1}} \tag{3.18}$$

where $\mu_0(T,N)$ is the low field mobility as expressed in Eq. 3.17 and E is the electric field. The parameters in the model (v_{sat}, E_c, a, n_1 and n_2) are determined from Monte Carlo simulation.

3.4 Empirical matching to measured device

In Silvaco ATLAS there are built-in models for the AlGaN/GaN system, but in many cases the semiconductor physical parameters are based on Monte Carlo simulations and not on experimental device electrical measurements. Some parameters chosen for the models were still reported above and others will be reported after. Silvaco ATLAS does not specifically define the models and methods required to simulate a device like the GaN based HEMT but gives general guidelines and multiple freedom of choice to the user. In my cases I started from a model that was still tested, and my objective was to implement it and fit on the analysed device. The task to tuning the simulation to match the experimental

measurements consists in changing several parameters and requires for the user large number of time consuming iterations of trial-and-error to reach his goals. In the following I summarize all the steps of my simulation endeavour by FBH.

As we have seen in Figure 3.1 all the epitaxial layers of the structure are defined as they are in the wafer. However, it is necessary to reproduce also both the u.i.d. GaN defectivity, the Iron and Magnesium doping in different GaN regions. This is fundamental for accurately reproducing the device band diagram and electrical behaviour. The first and fundamental task is to reproduce the trap profile of the GaN bulk layer. Before, it has to be noticed that is fundamental to implement also the AlN layer and the 4H-SiC substrate. In this way it is possible to better simulate the vertical leakage and to give an exact reference for the vertical cut-line of the band diagram.

In Silvaco ATLAS there is the possibility to define trap levels in the semiconductor bandgap. For each trap level it is possible to specify the trap type (acceptor or donor), the position in the bandgap (as distance from the valence or the conduction band), the trap concentration, the carrier capture cross section, and the trap degeneracy factor. Furthermore, it is possible to define a trap concentration profile, to better fit the impurities concentration spatial gradients. In all the simulations the capture cross sections for electrons and holes are fixed to $\sigma = 1 \times 10^{-15}\,\mathrm{cm}^2$. The chosen values of degeneracy factors are 4 for donor traps and 2 for acceptor traps [98].

In literature there are reported several trap levels for GaN [65] and is very difficult to choose the ones to introduce in the simulation model with the proper concentration. So, we can start to observe that in literature the carrier concentration of u.i.d. GaN samples can vary in the range between $10^{17}\,\mathrm{cm}^{-3}$ and $10^{18}\,\mathrm{cm}^{-3}$ [99], even if values of $10^{16}\,\mathrm{cm}^{-3}$ are reported [100]. I decided to start with a more optimistic situation, with a carrier concentration of $1 \times 10^{15}\,\mathrm{cm}^{-3}$; with this value the Fermi level lies at $E_F = E_C - 0.19\,\mathrm{eV}$. In order to implement a trap profile that represents this situation we must chose a donor trap level that is close to the Fermi level. In the actual situation it is possible that the concen-

tration of a donor states located in that energy level makes a Fermi level pinning, while other trap states with lower concentration have only secondary effects on the E_F position. In order to perform all the tests I used an auxiliary simplified structure, where I removed all the layers above GaN. After several tests I discovered that the presence of an acceptor trap in the low side of the bandgap gives a more realistic situation. As you can see in the sketch in Figure 3.3 (a) for the u.i.d. GaN there is an a main donor trap (D_1) located at $E_C - 0.20\,\text{eV}$ with a concentration of $10^{16}\,\text{cm}^{-3}$, and an acceptor trap (A_1) located at $E_V + 0.70\,\text{eV}$ with a concentration of $10^{15}\,\text{cm}^{-3}$. With this configuration we obtained the target values of $E_F = E_C - 0.19\,\text{eV}$ and carrier concentration of $1 \times 10^{15}\,\text{cm}^{-3}$.

For the simulation of the semi insulating Fe-doped GaN we have to look at the carrier concentration levels reported in literature. Unfortunately, there are not to many values reported, but it is possible to obtain information even from the resistivity and for the estimated E_F position, in function of the Fe concentration. This is the only way to obtain reliable results, because there are many possible energy levels of Iron reported literature [101][102], but we need to know the actual effect on the material properties. *Freitas et al.* [99] reported a resistivity of $10^{10}\,\Omega\,\text{cm}$ with a Fe concentration of $1 \times 10^{18}\,\text{cm}^{-3}$; *Kordoš et al.* [103] measured a resistivity of $5.7 \times 10^{8}\,\Omega\,\text{cm}$, a carrier concentration of $3.2 \times 10^{7}\,\text{cm}^{-3}$, and an activation energy of 0.6 eV, but they do not declare the Fe concentration; *Polyakov et al.* [104] estimated the position of the Fermi level at $E_F = E_C - 0.57\,\text{eV}$ with

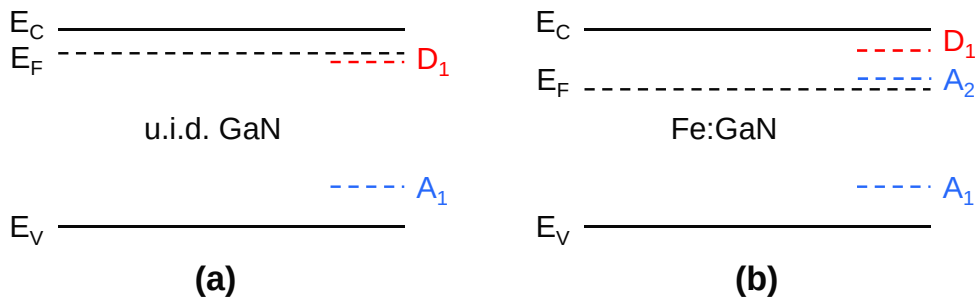


Figure 3.3: Trap levels and Fermi level positions for the simulated (a) u.i.d. GaN; (b) Fe-doped GaN.

an Iron concentration of $3.2 \times 10^{17}\,\mathrm{cm}^{-3}$. The Fe-related trap state is assumed to be an acceptor [104][105]. Comparing these with other data, I decided to set the Fermi level at $E_F = E_C - 0.66\,\mathrm{eV}$ with a carrier concentration of $2 \times 10^{7}\,\mathrm{cm}^{-3}$; In our case the measured Fe concentration was $2 \times 10^{18}\,\mathrm{cm}^{-3}$, so, I added to the u.i.d. GaN model another acceptor trap (A_2) with energy level of $E_C - 0.57\,\mathrm{eV}$ and concentration of $1 \times 10^{18}\,\mathrm{cm}^{-3}$ (see Figure 3.3 (b)).

When during the crystal growth the Fe source is closed, there is a memory effect, and the Fe concentration start to decrease with an exponential trend, till to reach the value of $1 \times 10^{16}\,\mathrm{cm}^{-3}$ after about $800\,\mu\mathrm{m}$ of thickness. It is possible to see this effect in the SIMS measurements in Figure 3.4 (a). Around $700\,\mu\mathrm{m}$ after the Fe-source closure the Iron concentration reaches the lower detection limit of $1 \times 10^{16}\,\mathrm{cm}^{-3}$. This is the reason why in our case the thickness of the u.i.d. GaN layer is of $850\,\mu\mathrm{m}$; in this way, the GaN channel region, where the current will flow, has a low defectivity and a high mobility. In order to build a model that better represent the real situation I implemented in the simulator form the Fe-relate trap state A_2 the trap profile of Figure 3.4 (b).

Also in the 9 nm AlGaN layer it is necessary to model the defectivity, even though it is not critical for the simulation. So, I introduced in the AlGaN layer

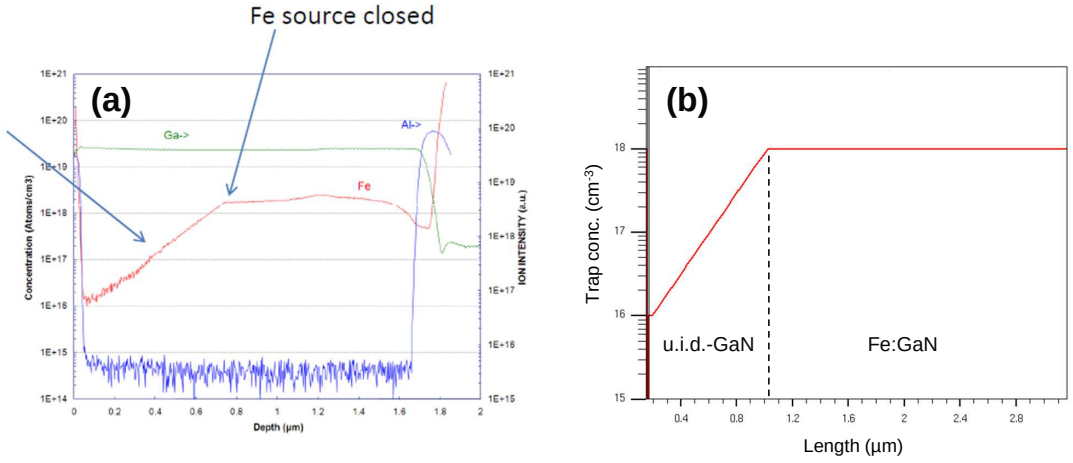


Figure 3.4: (a) SIMS measurement of Fe concentration on a Iron-doped GaN device; (b) trap profile used for the simulations.

a donor trap located at $E_C - 0.60\,\text{eV}$ with concentration of $10^{17}\,\text{cm}^{-3}$.

Regarding the Mg-doped p-GaN it is possible to find in literature values for the activation energies of acceptor states in the range between 120 meV and 160 meV over the valence band [106][107]. The Hall measurements on the p-GaN of the simulated device revealed a hole concentration of $3 \times 10^{17}\,\text{cm}^{-3}$ obtained with a Mg concentration of $10^{19}\,\text{cm}^{-3}$. Thus, I introduced in the p-GaN model an acceptor state located at $E_V + 0.16\,\text{eV}$ with concentration of $10^{19}\,\text{cm}^{-3}$. The simulated holes concentration value is exactly the same of the measured one.

Silvaco ATLAS allows to define the work function for the metal contacts. For the ohmic contacts of source and drain I taken the value $\phi = 3.8$ eV, since it was already used in previous simulations and it match with the work function value reported for Ti [108]. The situation on the p-GaN gate contact is more complicated. Differently from the Schottky-gate device, here we do not need a barrier, but a ohmic contact, since the barrier effect is made by the p-GaN itself. But make an ohmic contact on p-doped GaN is not an easy task. Considering the electron affinity of GaN, $\chi = 4.09$ eV, and the energy gap $E_g = 3.43$ eV, the valence band lies 7.52 eV below the vacuum energy level. It is impossible to find metals with such high value, since only Pt reach 6.3 eV and the others are below 5.5 eV. In the analysed device the contact was made of Ni that has $\phi = 5.1$ eV, but from the diode measurements the estimated barrier on the p-GaN contact is around 0.2 eV. How is possible to explain this discrepancy? We can find the answer in a work from *Ho et al.* [109]. Here it is reported how, with the deposition of a Ni/Au film and a heat treatment that transforms the Ni in NiO, it is possible to obtain a barrier height on the p-GaN contact of 0.185 eV. This value is in line with the estimated one in our device. So, the gate contact work function used in the simulations was 7.32 eV, in order to fit the barrier height of 0.2 eV.

3.5 Simulation results

After the parameters matching we can take a look on the simulation results, starting from the band diagrams. In Figure 3.5 (a) it is possible to observe a vertical cutline of the band diagram in the gate region along the whole vertical height. It is evident the huge barrier created by the AlN layer between the GaN and the 4H-SiC, that limits the bulk current. In Figure 3.5 (b) we can see a detail under the gate region, where it is clear that the channel is in pinch-off.

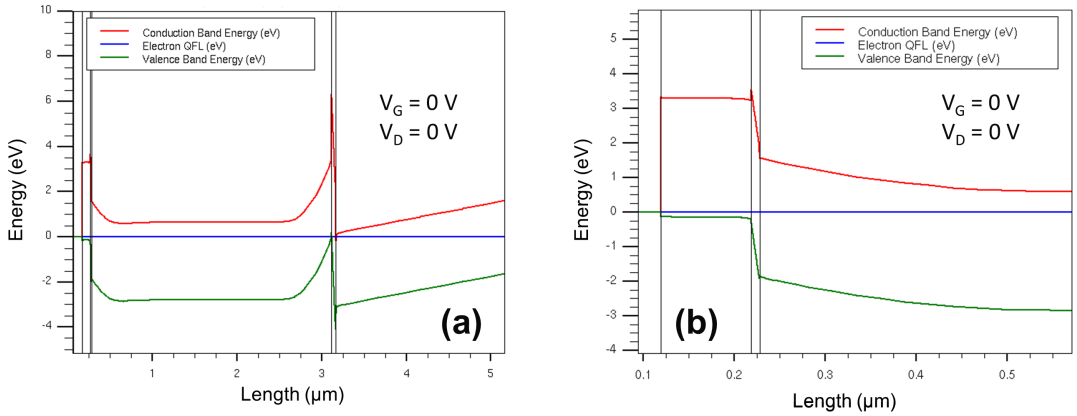


Figure 3.5: Band diagram vertical cutline at $V_G = 0\,V$, $V_D = 0\,V$ for: (a) the whole vertical structure; (b) a detail of the gate region.

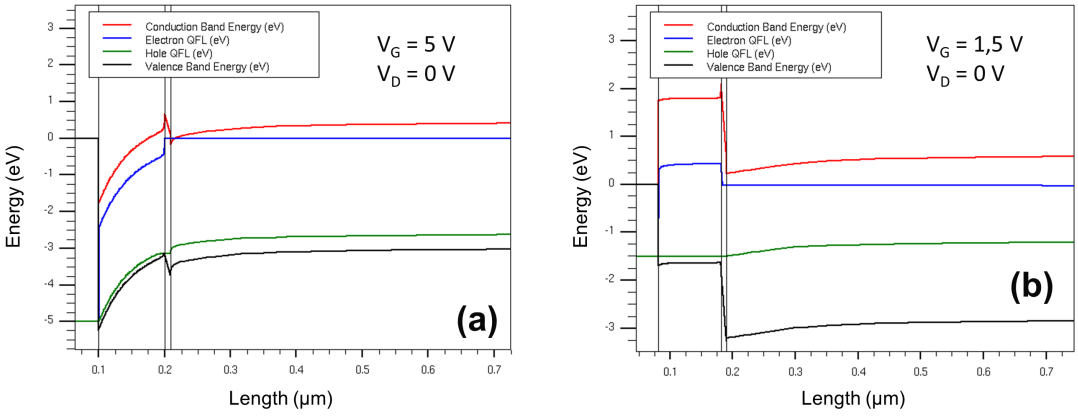


Figure 3.6: Band diagram vertical cutline in two different bias conditions: (a) $V_G = 5\,V$, $V_D = 0\,V$; (b) $V_G = 1.5\,V$, $V_D = 0\,V$.

In Figure 3.6 (a) we can observe the simulated band diagram with a gate bias of 5 V. In this situation it is evident how both carriers could flow thorough the barrier, leading to a enhancement region that extends below the gate. But since we are in a wide bandgap material, even if the quasi-Fermi level for holes seem to be close to the valence band, the hole concentration is not so high (see Figure 3.7 (d)). In Figure 3.6 (a) we can observe the simulated band diagram with a gate bias of 1.5 V; in this case the barrier of the p-GaN is still too high for both carriers, and the leakage cannot flow thorough the barrier, but maybe could flow on the surface.

In the following, there are reported a series of plots that represent some simulated device parameters in the gate region for the same bias condition of the band diagram of Figure 3.6 (a): $V_G = 5\,V$, $V_D = 0\,V$. In Figure 3.7 (a) is reported the contour plot of the electron concentration, while in Figure 3.7 (b) we can see the electron concentration profile along the black bold cutline. We can observe the peak of carriers in the 2DEG channel, and a not negligible concentration in the p-GaN. In Figure 3.7 (c) is reported the contour plot of the hole concentration, while in Figure 3.7 (d) we can see the hole concentration profile along the black bold cutline; it is evident how the hole concentration drops rapidly in the GaN channel region. In Figure 3.7 (e) is reported the contour plot of the recombination rate, while in Figure 3.7 (f) we can see the recombination rate profile along the black bold cutline. We can notice how the recombination rate is relatively low in the GaN channel region and it is located on the source-side of the gate. Conversely, in the p-GaN the recombination rate is at least ten order of magnitude higher, indicating that the conduction through the gate diode is not bipolar but seems to be dominated from electrons. For some reason the holes cannot overcome the barrier so easily, even though this is not clear if we look only at the band diagram of Figure 3.6 (a).

In Figure 3.8 is reported a comparison of the measured and the simulated gate current trend in forward bias. How is possible to see the two curves does not match because it was not possible to correctly simulate it. The main reason is that, for

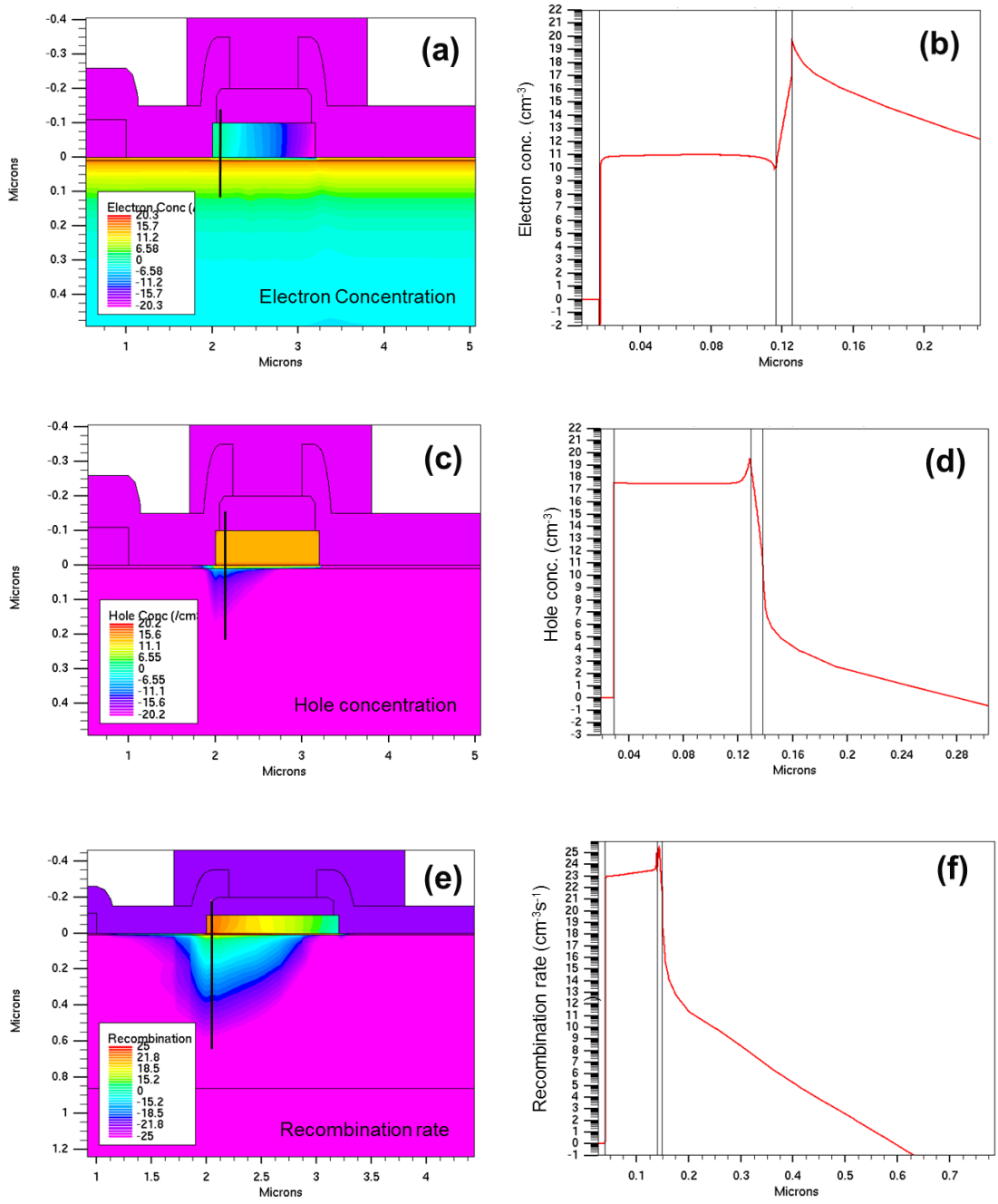


Figure 3.7: (a) contour plot of the electron concentration; (b) electron concentration profile along the black cutline; (c) contour plot of the hole concentration; (d) hole concentration profile along the black cutline; (e) contour plot of the recombination rate; (f) recombination rate profile along the black cutline.

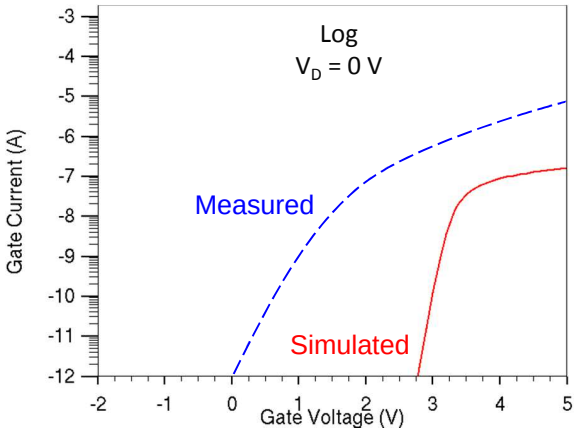


Figure 3.8: Comparison of the measured and simulated gate current in forward bias.

gate voltages lower than 3 V we do not expected to have a leakage current (see band diagram in Figure 3.6 (b)). The origin of this leakage could be on the surface, with a hopping mechanism, as proposed by *Bae et al.* [110]. This hypothesis could be valid in our situation too, but it should be confirmed by further analysis. For $V_G > 5\,V$ it seems that the simulation can reproduce the leakage mechanism, maybe with some additional matching of the parameters. This has to be verified in the future, since from the diode measurements the activation energy of the gate current is very low (around 20 meV) and the conduction mechanism could not be thermionic, but maybe such kind of tunnelling. Up to now there is still not a model for this mechanism and hopefully it will developed soon in the future.

As we mentioned in the beginning, the main simulation targets were not only to match as better as possible the device electrical characteristics, but also to try to simulate the device degradation during the on-state stress test. The purpose was to understand which device area can be more critical, and to try to understand if it is possible to model the modification of some parameters during the stress. In Figures 3.9 (a) and (b) it is possible to see a typical trend of the transfer characteristic taken at $V_D = 10\,V$ for different steps of the constant current stress. In linear scale (Figure 3.9 (a)) we can observe only a decrease in

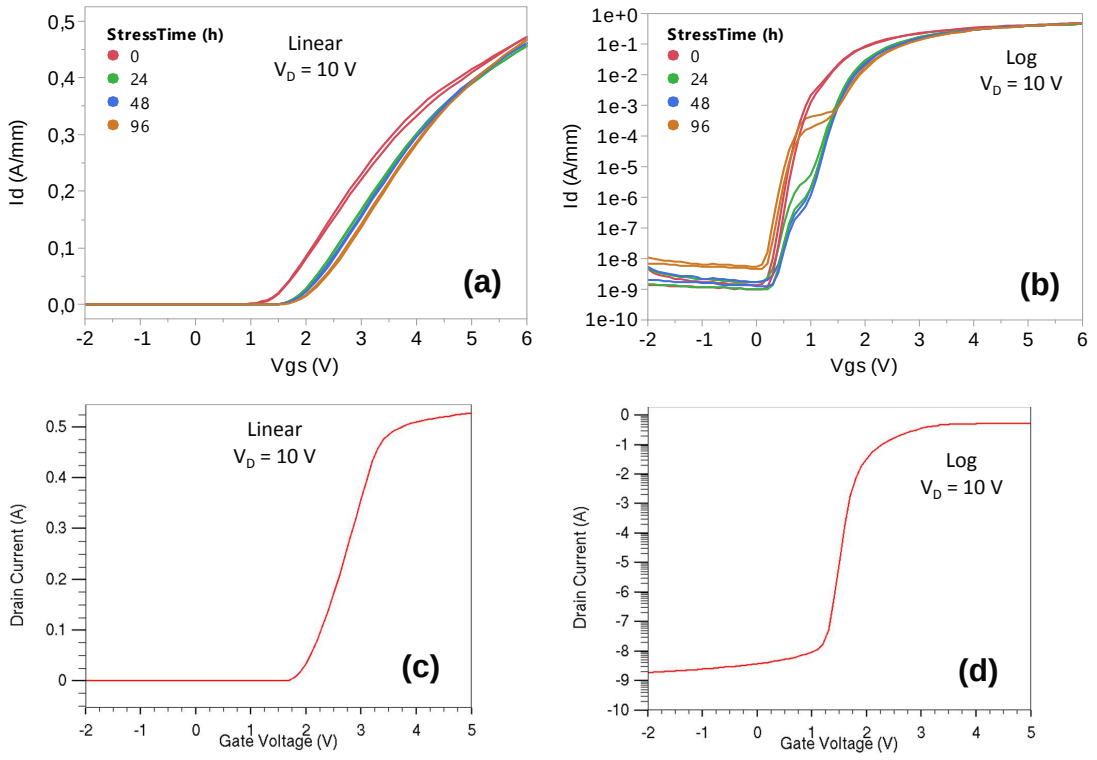


Figure 3.9: Transfer characteristic of a device during an on-state stress test (a) linear scale; (b) log scale. Simulated transfer characteristic (c) linear scale; (d) log scale.

the output current, but in log scale (Figure 3.9 (b)) we can see appearing a subthreshold hump. The origin of this hump is still not clear and it was not possible to reproduce it with the simulations. However, the different simulations attempts told us that is unlikelihood that this process is related to some modification of the GaN channel area or the whole p-GaN, while it could be very close to the AlGaN barrier. The mechanism remain still not clear, but it could be localized only in the source-side of the gate, since, as we have seen in Figures 3.7 (c) and (e) the hole injection is concentrated in that area.

In Figures 3.9 (c) and (d) the simulated transfer characteristic has been reported, and we can see that there is still a bis discrepancy with the measurements, in particular in linear scale. This is due to the inaccuracy of the parameter fitting. Unfortunately, I needed a lot of time to implement the structure, and when it was

time to match the other model parameters my time by FBH was over, and the work remained incomplete. We can observe a discrepancy of the threshold voltage in the log scale plot (Figure 3.9 (f)), the simulated one is around 1 V higher. One of the reason is that some interface state at the p-GaN/AlGaN interface shift the threshold to the left. I implemented them in the simulation model, but the simulation time was increasing unreasonably, and I neglected them, at least until a good matching of other parameter was reached. The amount of the simulated left threshold shift was around 0.4 V. Finally, we can observe in Figure 3.9 (d) that the simulated off-state leakage level match the measured one; the reason is that this was a fundamental fit parameter when the GaN buffer trap profile has been implemented.

As conclusion of this chapter I can say that, even though all the simulation targets have not been reached, I was able to build a simulation structure for p-GaN device that represents the beginning for future analysis. Then, this experience helped me to deeply understand several device details that would be impossible to comprehend in other ways. This demonstrates that the simulator represents a complementary analysis instrument for who studies the physics of semiconductor, since allow to integrate and improve the experimental information.

Chapter 4

High frequency devices

In this chapter it will be summarized the main activity performed within the research collaboration with the European Space Agency (ESA), with topic *"Preliminary Validation of Space Compatible Foundry Processes"*. The main targets of this project have been to validate the reliability of the GaN technologies developed in Europe, to develop short-term techniques for the evaluation of the reliability of GaN HEMT technologies, focused on the understanding of physical failure mechanisms, and to assess the radiation hardness of RF power transistors. The processes considered within this project were GaN-on-SiC HEMTs for RF space applications. The tested technologies can be divided in two different generations:

1. GH50: gate length $L_G = 0.50\,\mu$m, operative frequency < 6 GHz, for L-, S- and C-band.

2. GH25: gate length $L_G = 0.25\,\mu$m, operative frequency < 20 GHz, for C-, X- and Ku-band.

This project has been lasting four years, and has generated a huge amount of results. It is not possible to report here all of them, so I will summarize only the results of the reliability tests, that was the part where I contributed more.

4.1 Short-term reliability tests

4.1.1 Device and test description

In the following they will be reported the results of the short-term stresses on both the GH50 an GH25 technologies. The tests consists in step-stress and 24-h DC life tests. The aim of the step stress is to identify the critical drain voltages from the off-state to the on-state conditions. The purpose of the 24-h DC life test is to identify the failure mode under different bias conditions, together with the degradation accelerating factors. All these tests have been performed on on-wafer devices. Details about the tested transistors are reported in Table 4.1, while the layout geometry is represented in the sketch of Figure 4.1. All the tests have been carried out at room temperature.

Step-stress

The step-stress test is a quick procedure that allow to find the maximum operative voltage that a device can withstand, at different gate voltages (from off-state to on-state). The tests will be performed in three different operative bias points:

- Off-state: $V_G = -7$ V;
- Semi on-state: $V_G = -2$ V;
- On-state: $V_G = 0$.

Starting from $V_{DS} = 20$ V the drain voltage is increased at 10 V steps up to the device catastrophic failure. The stress voltage is applied for 2 minutes

Table 4.1: Layout geometry of the tested devices.

Technology	Device name	L_G (μm)	W_G (μm)	STFP (μm)	L_{GS} (μm)	L_{GD} (μm)
GH50-ITN3	4000-1500-A	0.50	80	2.3	1.5	4.0
GH25-ITN2a	2×40_V1	0.25	80	0	0.8	2.7

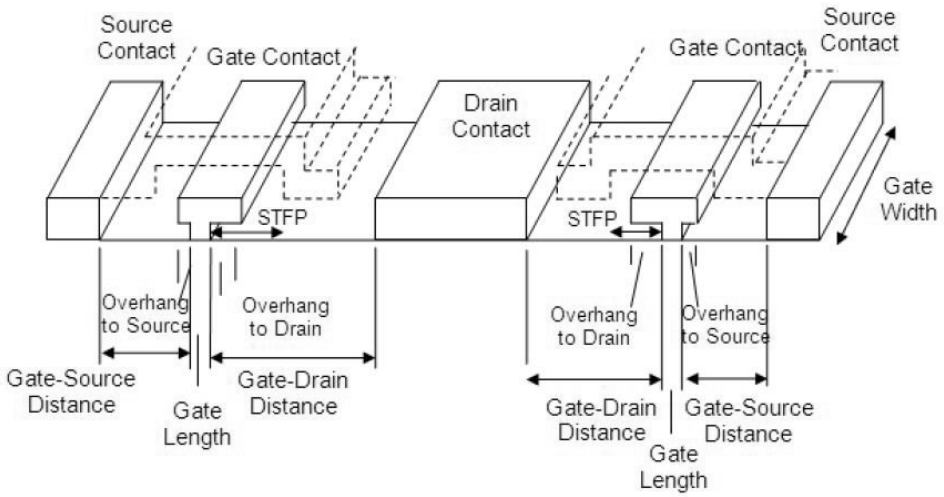


Figure 4.1: Sketch of the HEMT layout.

and at each step, and after 5 minutes of rest, a standard characterization and electroluminescence emission measurements are carried out. The latter are fundamental because we can observe the current spatial distribution under several bias conditions:

- Off-state: $V_G = -10$ V, $V_D = 0$ V;
- On-state: $V_G = 0$ V, $V_D = 20$ V;
- Stress: $V_G = 0$ V, $V_D = V_{Dstress}$.

24-hours DC stress

Starting from the step-stress results we can plan the test conditions for the 24-h DC stresses. Carrying out tests at different bias points it is possible to better investigate which parameters are involved in the device degradation, like the electric filed, the hot electrons, or the dissipated power. Furthermore, the 24-h DC stress are short-term tests long enough to give a first time evolution of the device degradation.

During the test the device is biased at the defined stress bias point, stopping the test at fixed times, to perform the standard characterization and electrolu-

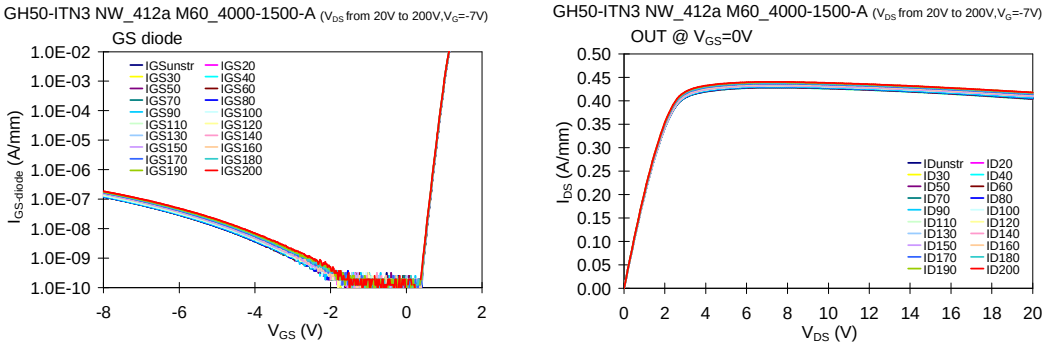
minescence analysis, after 10 minutes of rest. The test stop times are: after 10 min, after 30 min, after 1 h, and then, every hour up to the end. Before and after the test the devices have been fully characterized with DC, pulsed and electroluminescence measurements.

4.1.2 Short-term tests for the GH50 technology

GH50 step-stress results

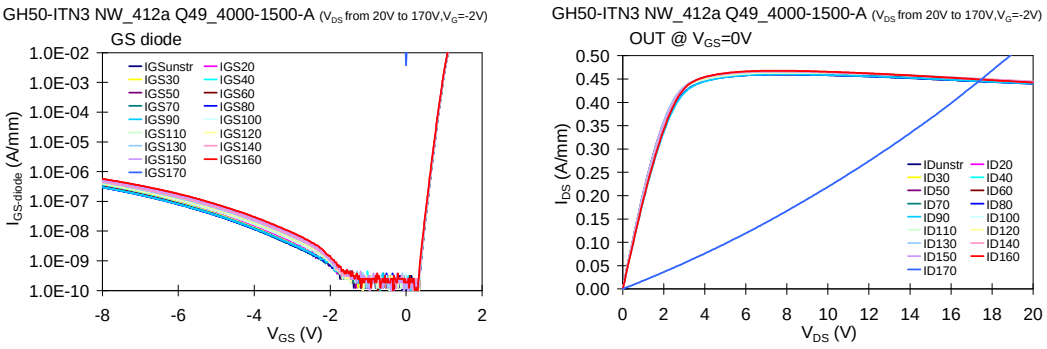
Summarizing the results gathered from the step-stress activity, we have observed a really stable behaviour of GH50-ITN3 samples on typical operating conditions as well as on really extreme bias conditions from off- to on-state, highlighting the capability of this technology to work even close to the points where the device fails catastrophically (see Figure 4.2, Figure 4.3 and Figure 4.4). The V_{DS} catastrophic failure-point has decreased from off-state to on-state, suggesting the influence of the dissipated power on the final device failure, rather than of the electric-field (max dissipated power of 37 W/mm on on-state step-stress), but the limited electrical parameters variation observed during the intermediate steps (within 5%) have not allowed to identify any other clear signature of failure. Other variations of the device behaviour were:

- in on-state/high-power step-stress, small variation of the output current in the knee region, highlighted by a 5% decrease of I_{DS} and g_m, while in all other operating regions device parameters kept stable values;
- slight negative threshold voltage shift happening where the drain stress current started to be higher than the gate stress current, sign of a reduction of the capability of gate terminal to keep the channel closed, visible in all the step-stresses.



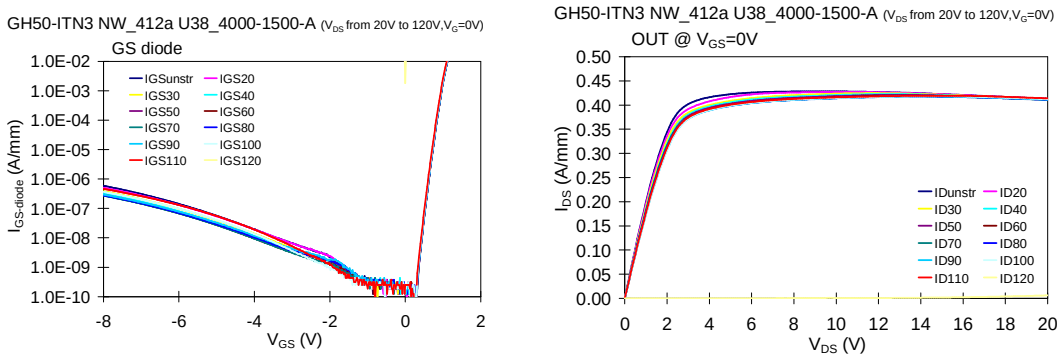
(a) GS diode characteristic. (b) output characteristics at V_G=0 V

Figure 4.2: (a) GS diode and (b) output drain current characteristics collected at each step during the off-state step-stress on a GH50-ITN3 device.



(a) GS diode characteristic. (b) output characteristics at V_G=0 V

Figure 4.3: (a) GS diode and (b) output drain current characteristics collected at each step during the semi-on state step-stress on a GH50-ITN3 device.



(a) GS diode characteristic. (b) output characteristics at V_G=0 V

Figure 4.4: (a) GS diode and (b) output drain current characteristics collected at each step during the on-state step-stress on a GH50-ITN3 device.

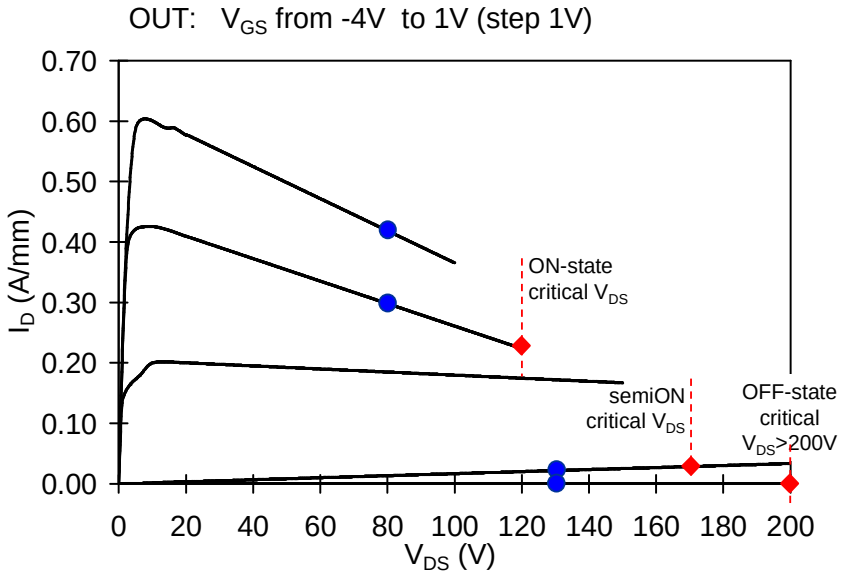


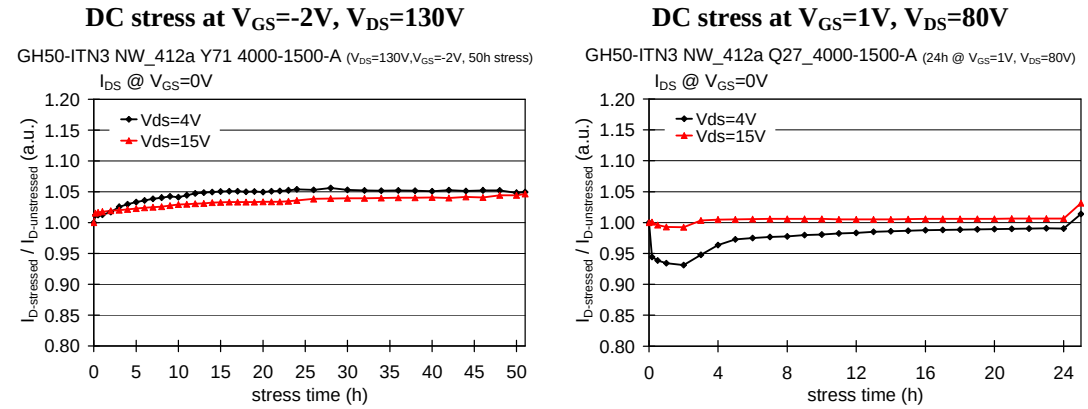
Figure 4.5: Schematic representation of the catastrophic failure voltages measured by means of step-stress tests on GH50-ITN3 samples (red diamonds), and position of the bias-points used for 24-h stress (blue bullets).

GH50 24-hours DC stress results

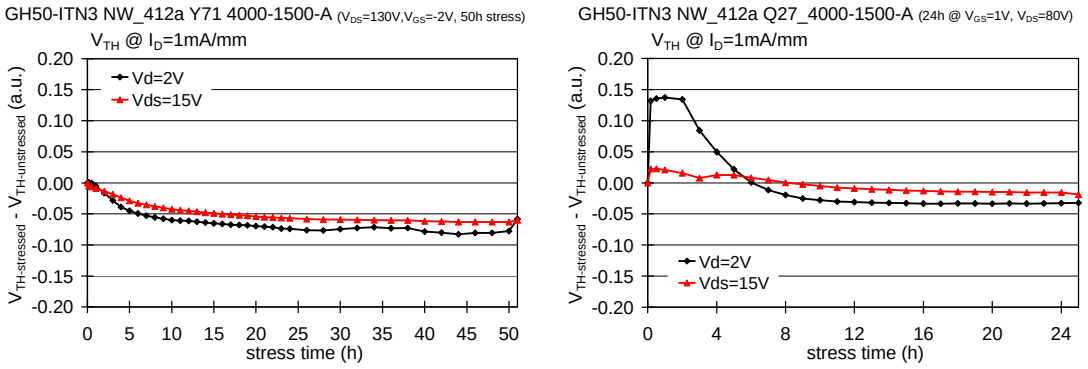
Summarizing the results from the 24-h reliability tests carried out in really high-field and high-power conditions (schematic representation in Figure 4.5), we confirmed the preliminary results highlighted by the step-stress tests and the outstanding robustness of GH50-ITN3 technology even in really extreme bias conditions, at least for medium stress times. In particular, we have observed that it is still difficult to identify a clear failure signature on this technology due to the limited variation of all device parameters (within 5-6% for I_{DS} or g_m, and within 3-4 times for leakage; see Figure 4.6). Nevertheless, we can draw some hypothesis from the reported results:

- it seems that high electric-field alone is not sufficient to cause significant damages on this technology, like gate-leakage degradation or performance drift, but only a small gradual threshold voltage left shift enhanced by the presence of highly energetic carriers;
- the simultaneous presence of really high junction temperatures (higher than 250°C) and high-electric field can enhance the device degradation (like in the high-power stress) with some leakage increase and I_{DS} and g_m reduction, even if final damages remain within 5%.

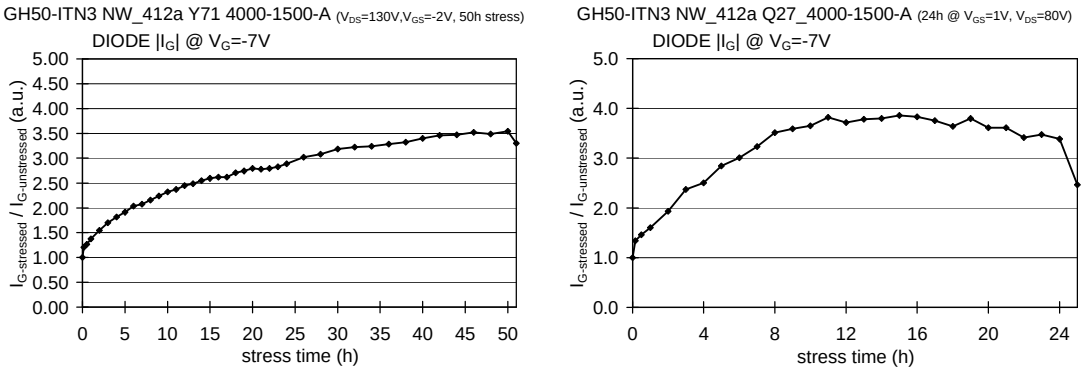
These tests highlight the role of the dissipated power, thus of the temperature, on device degradation, while the threshold voltage seems to be more influenced by the V_{DS} voltage. Nonetheless, 36 W/mm of dissipated power caused only a small decrease of the transconductance peak (4%), thanks to the really low thermal resistance of this wafer technology ($\approx$ 6 K $\cdot$ mm/W) which keeps a pretty low junction temperature, estimated around 250°C.



(a) Normalized drain saturation current at $V_G = 0$ V.



(b) Normalized threshold voltage.



(c) Normalized gate-source diode leakage at $V_G = -7$ V.

Figure 4.6: Variation of the main electrical parameters of the GH50-ITN3 samples submitted to high-filed/low-current (left plots) and extreme high power (right plots) DC stress.

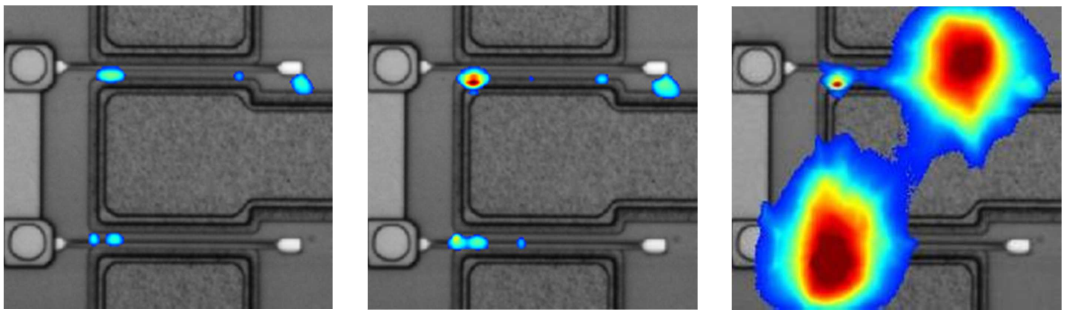
4.1.3 Short-term tests for the GH25 technology

In the case of the GH25 technology two different wafer generations have been compared. The new GH25-ITN2a process is an improvement of the older GH25-ITN2. In the graphs the GH25-ITN2 technology is indicated with the respective wafer name "PW 45", while for GH25-ITN2a the wafer is the "PW 51b".

GH25 step-stress results

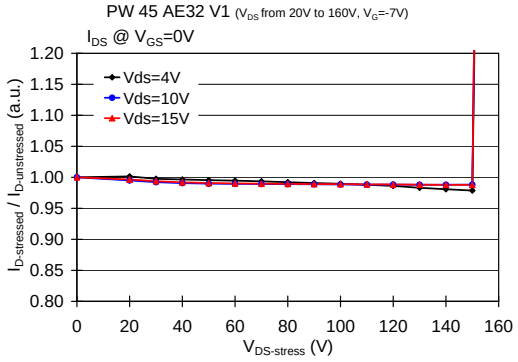
In the following they are reported the results of the step-stress on the GH25-ITN2 and GH25-ITN2a technologies, with the plots for the main stress parameters during the tests.

The GH25-ITN2a technology demonstrated an excellent robustness in comparison to the GH25-ITN2. The off-state stress carried out on both wafers technologies shown similar behaviour (see Figure 4.8), with low I_{DS} variation and V_{th} shift (less than 5% and 50 mV respectively). Leakage current did not show any increase up to catastrophic failure occurring at around 150-160 V, ruling out gate-edge degradation mechanisms (no off-state hotspots) at least at this temperature and on a short-time scale. In Figure 4.7 we can notice a very low emission from some spot before the catastrophic failure, even at high voltages, indicating the low degradation level.

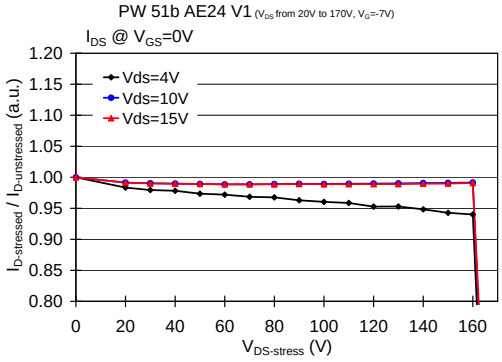


(a) $V_{DS} = 120$ V. (b) $V_{DS} = 150$ V. (c) $V_{DS} = 170$ V.

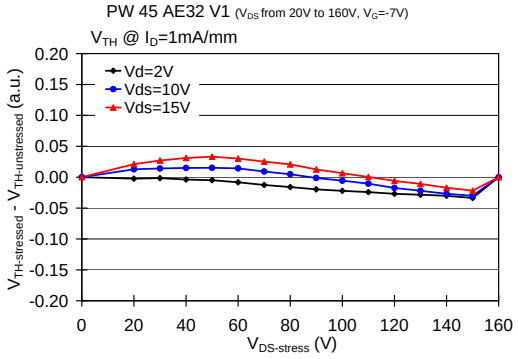
Figure 4.7: Emission images captured during the off-state step-stress for the device AE32 of the wafer GH25-ITN2a.



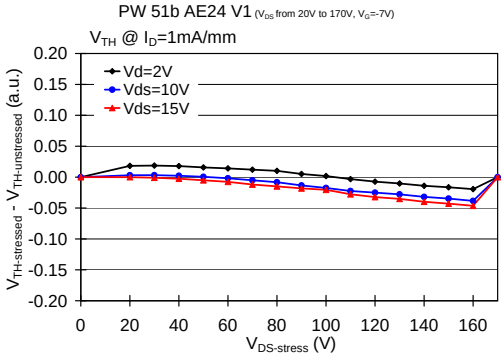
(a) I_{DS} on ITN2.



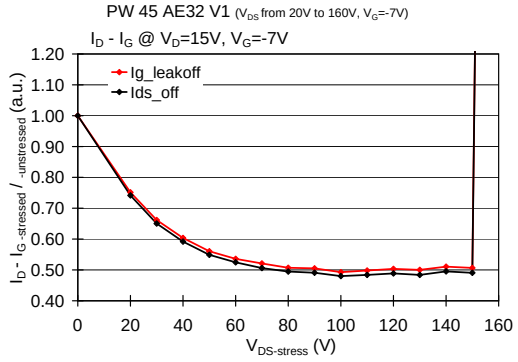
(b) I_{DS} on ITN2a.



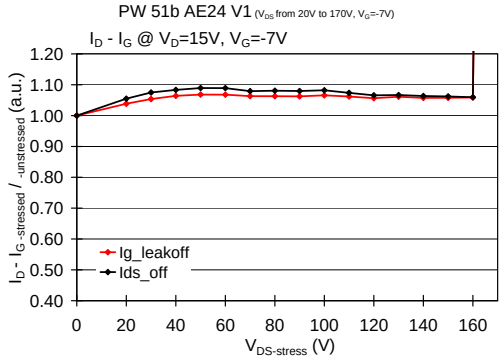
(c) V_{th} on ITN2.



(d) V_{th} on ITN2a.

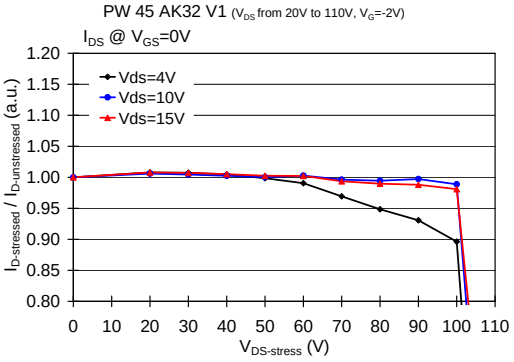


(e) Off-state leakage currents on ITN2.

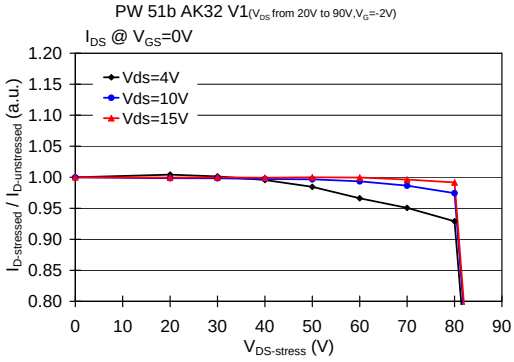


(f) Off-state leakage currents on ITN2a.

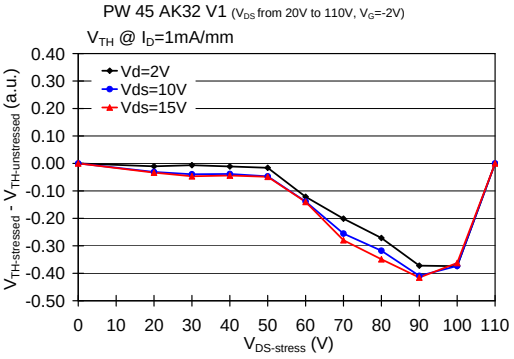
Figure 4.8: Off-state step stress comparison between GH25-ITN2 wafer (left side) and GH25-ITN2a wafer (right side).



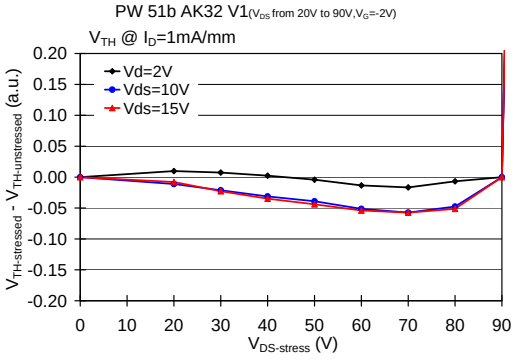
(a) I_{DS} on ITN2.



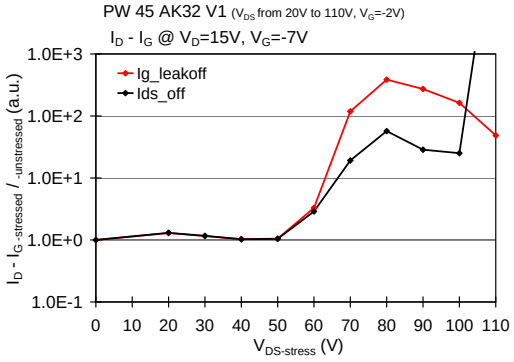
(b) I_{DS} on ITN2a.



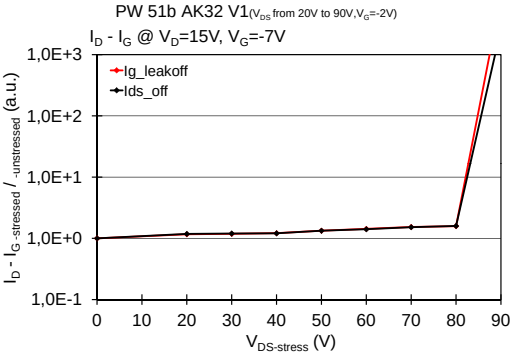
(c) V_{th} on ITN2.



(d) V_{th} on ITN2a.

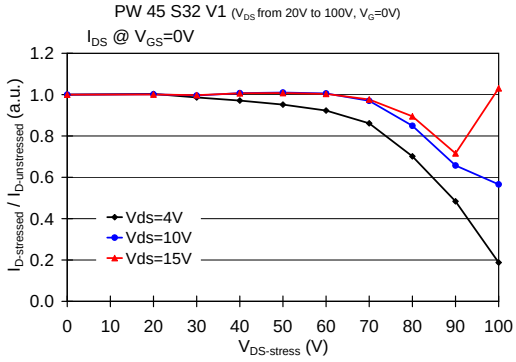


(e) Off-state leakage currents on ITN2.

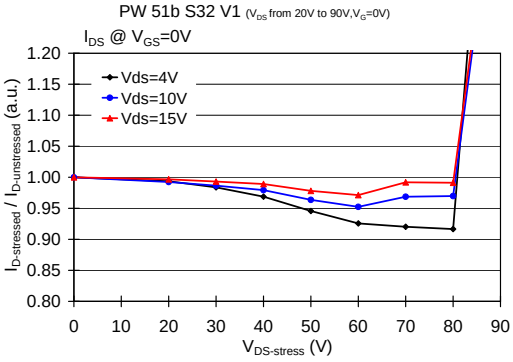


(f) Off-state leakage currents on ITN2a.

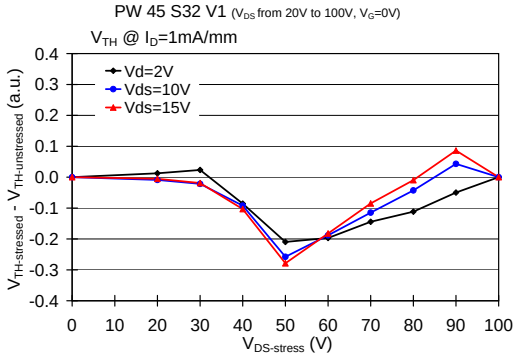
Figure 4.9: Semi-on state step stress comparison between GH25-ITN2 wafer (left side) and GH25-ITN2a wafer (right side).



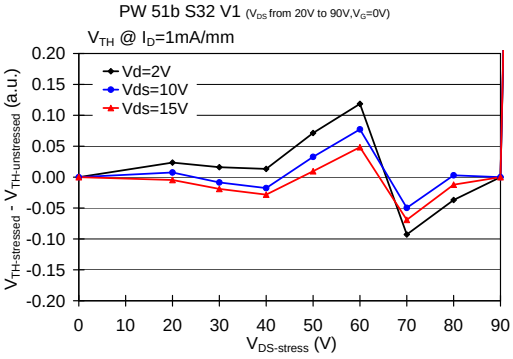
(a) I_{DS} on ITN2.



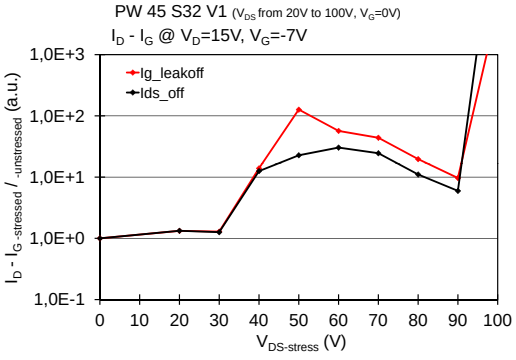
(b) I_{DS} on ITN2a.



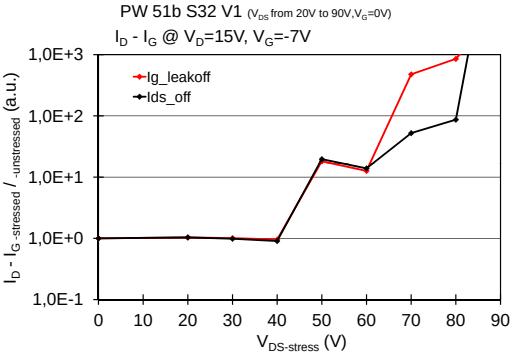
(c) V_{th} on ITN2.



(d) V_{th} on ITN2a.



(e) Off-state leakage currents on ITN2.



(f) Off-state leakage currents on ITN2a.

Figure 4.10: On-state step stress comparison between GH25-ITN2 wafer (left side) and GH25-ITN2a wafer (right side).

As is possible to see in the comparison of Figure 4.9, during semi-on state step-stress, ITN2 samples show a parametric degradation of device parameters, starting from the step at $V_{DS} = 60$ V, consisting of a gradual negative shift (-0.4 V) of V_{th} and a significant increase ($100\times$) of the gate leakage. This degradation is correlated with a significant change of the subthreshold behaviour, possibly due to the formation of a parasitic drain-source conductive path that lowers the threshold voltage. The leakage current increase depends on the dissipated power, and tends to have a non-monotonic behaviour as a function of V_{DS}. On the contrary, the ITN2a sample shows much more stable threshold voltage and leakage currents, the latter which slightly increases, probably influenced by the small negative V_{th} shift.

In Figure 4.10 we can notice that the on-state step-stress tests induces the same failure modes observed at the semi-on bias point: in the beginning, a sharp increase of the gate leakage (1-2 orders of magnitude), accompanied by a small decrease of the main performances (I_{DSSAT}, g_{m-MAX}) and a left V_{th} shift; subsequently, a second failure mode takes place, which induces a right V_{th} shift and significantly reduces both I_{DSSAT} and g_{m-MAX}, without further changes in the leakage current. The first degradation mechanism (leakage increase) has been observed on both ITN2 and ITN2a wafers, but at significantly different V_{DS}: on the ITN2 device degradation started at 40 V, while on the new ITN2a device the degradation began at 70 V, one step before the catastrophic failure. The second degradation mechanism occurs only in the ITN2 samples, starting at the step with $V_{DS} = 60$ V, and does not affect ITN2a devices.

Looking at all these results, we have tried to individuate the main failure "signatures", i.e. some typical modification of the electrical parameters that characterize a definite degradation mechanism. In Table 4.2 and Table 4.3 are summarized the conditions where the signatures appear.

- Signature 1: Sudden increase of the gate leakage (1-2 orders of magnitude) followed by a performance drop (I_D, g_m, R_{on}) mainly in the knee region, and by a left V_{th} shift.

Table 4.2: Signature 1.

Wafer ITN2	Wafer ITN2a
$V_{GS} = -2$ V, $V_{DS} = 60$ V (semi-on state)	–
$V_{GS} = 0$ V, $V_{DS} = 40$ V (on-state)	$V_{GS} = 0$ V, $V_{DS} = 70$ V (on-state)

- Signature 2: Significant performance drop (I_D, g_m, R_{on}) with a right V_{th} shift; gate leakage variation not discernible from signature 1.

Table 4.3: Signature 2.

Wafer ITN2	Wafer ITN2a
$V_{GS} = 0$ V, $V_{DS} = 60$ V (on-state)	–

GH25 24-hours DC stress results

Considering the step-stress results it is possible to design the bias points set for the 24-hours DC tests, with a safety margin from the catastrophic failure. The bias points have been chosen following these three guidelines:

- Bias points with constant gate voltage, for looking at the effects of the electric filed and the dissipated power on the device performances.
- Bias points with constant drain voltages, for observing hot electrons and power dissipation effects on the device performances.
- Bias points with constant dissipated power, for looking at the electric field and hot electrons effects on the device performances.

Figure 4.11 shows all the bias points adopted for short-term testing of GH25 devices; blue and red diamonds refer to the absolute V_{DS} limits identified by

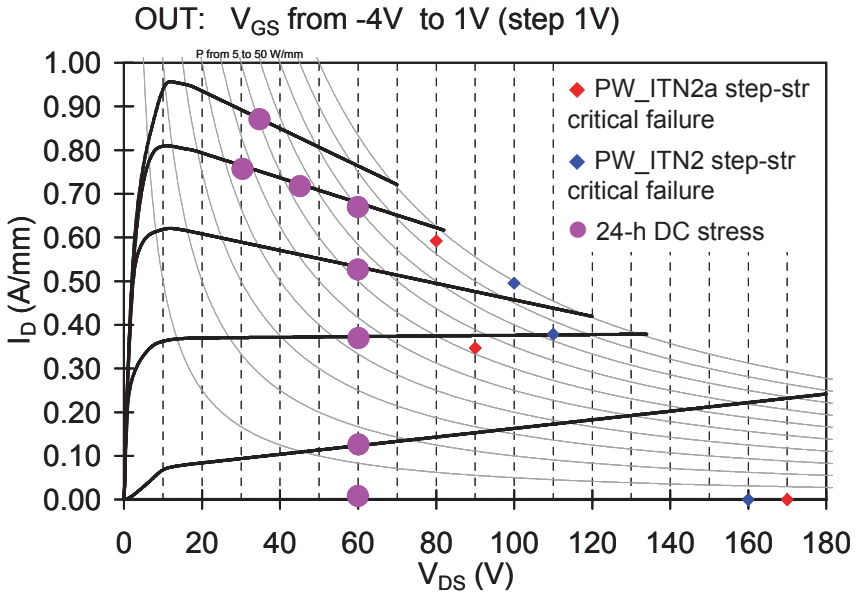


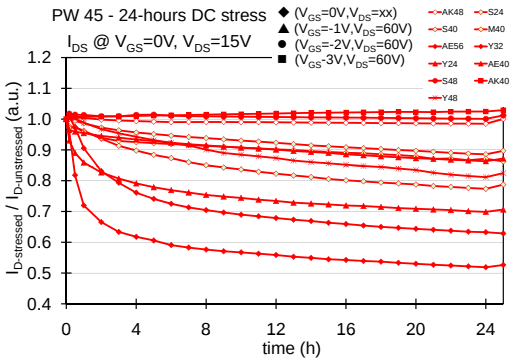
Figure 4.11: Schematic representation of the step stress failure points on ITN2 and ITN2a technology (red and blue diamond points), and of the bias-points of the 24-hours DC stress, on a typical GH25 output diagram.

means of the step-stress tests, while purple bullets refer to the 24-h test bias points.

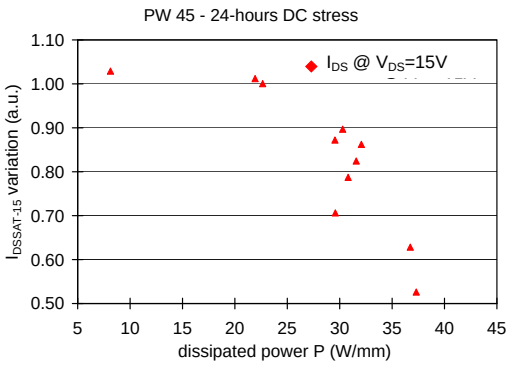
We will start first analysing the results obtained on the wafer ITN2. In Figure 4.12 are reported the main parameter's variations of all ITN2 samples submitted to the 24-hours high-power stress. Looking at the threshold voltage, it is possible to recognize two of the failure signatures observed during the step-stress tests (see Figure 4.12 (e) and (k)). For low dissipated power, the threshold voltage shifts toward more negative values (sharply after few minutes of stress or gradually during the stress); for high dissipated power, the threshold shifts toward more positive voltages, further reducing the main device performances, with a gradual or sharp behaviour depending on the bias-point.

Concerning the leakage current, all bias points have caused a sudden increase of the gate leakage from 2 to 4 orders of magnitude, which slowly decreases during the 24-hours of stress (see Figure 4.12 (g)). This effect seems to be caused by the

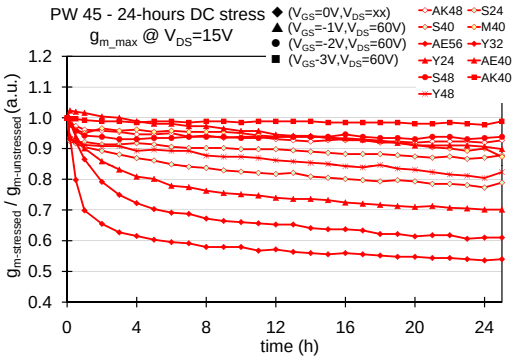
high device temperature reached at the beginning of the stress, but there is not a clear and linear dependence between the leakage degradation and the dissipated



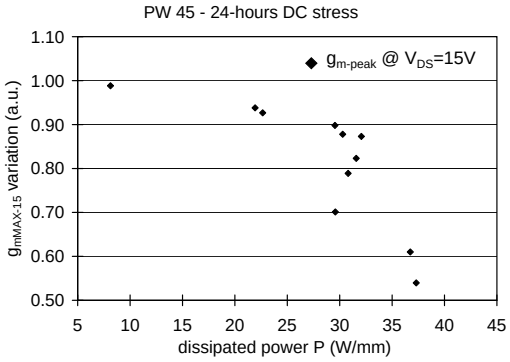
(a) $I_{DSSAT-15}$ variation.



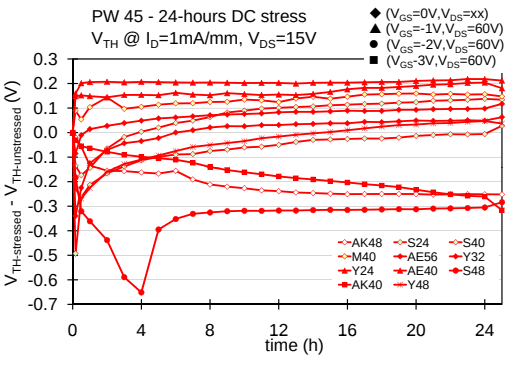
(b) $I_{DSSAT-15}$ degradation vs. dissipated power.



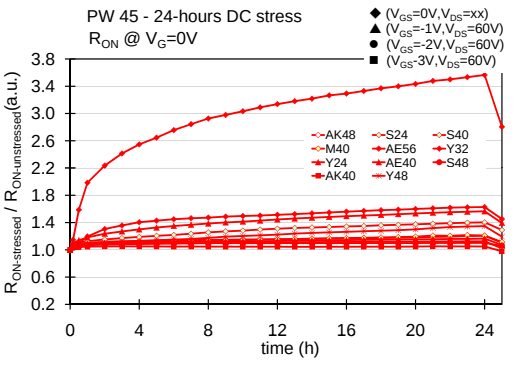
(c) $g_{mMAX-15}$ variation.



(d) $g_{mMAX-15}$ degradation vs. dissipated power.

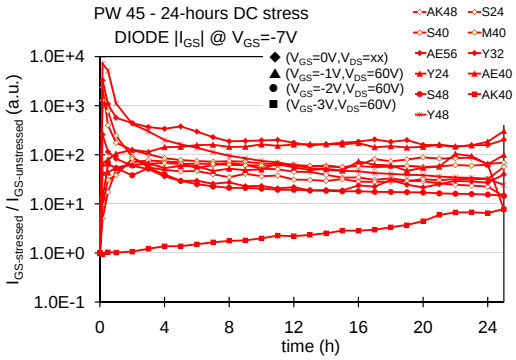


(e) V_{TH-15} variation.

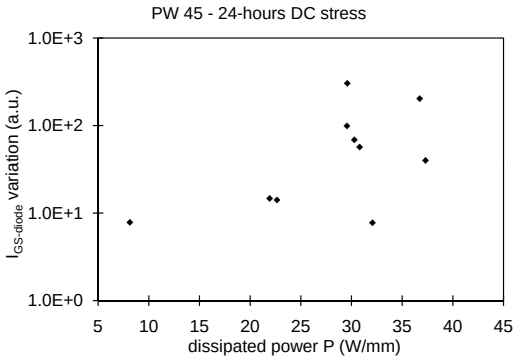


(f) On-resistance R_{ON} variation.

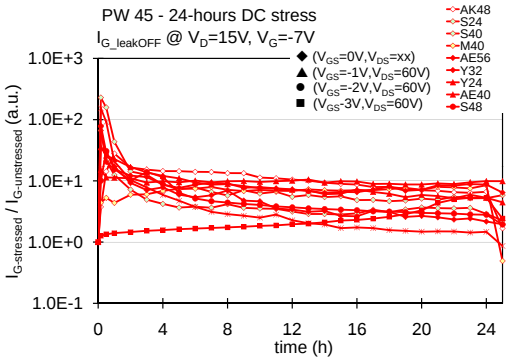
Figure 4.12: Comparison of the main parameters monitored during the 24-h DC stress on the wafer ITN2.



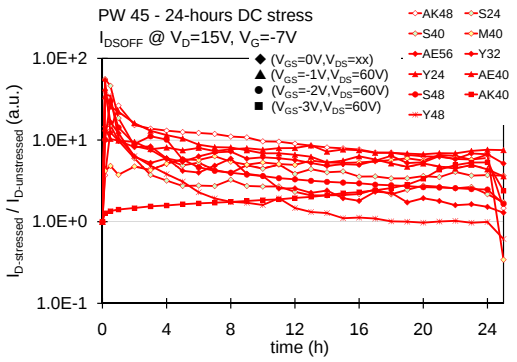
(g) I_{GS} diode variation.



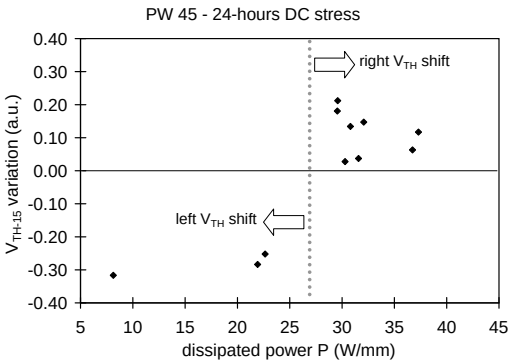
(h) I_{GS} diode increase vs. dissipated power.



(i) $I_{leak-OFF-15}$ variation.



(j) $I_{DSOFF-15}$ variation.

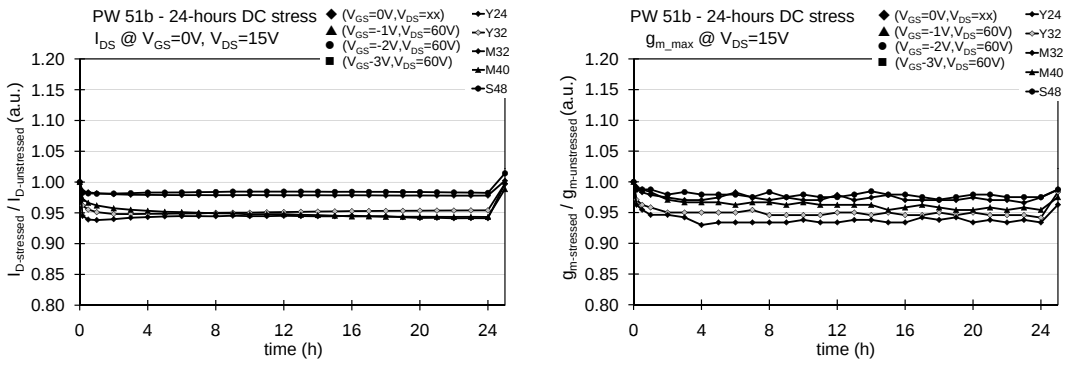


(k) V_{TH} variation vs. dissipated power.

Figure 4.12: Comparison of the main parameters monitored during the 24-h DC stress on the wafer ITN2.

power, due to the different variation of the leakage during the following hours of stress, or to some inhomogeneity on the local junction temperature (see Figure 4.12 (h)). Only devices biased at (-3 V, 60 V) bias point have shown limited leakage increase, due to the relatively low dissipated power (< 10 W/mm) and to a gradual left threshold voltage shift.

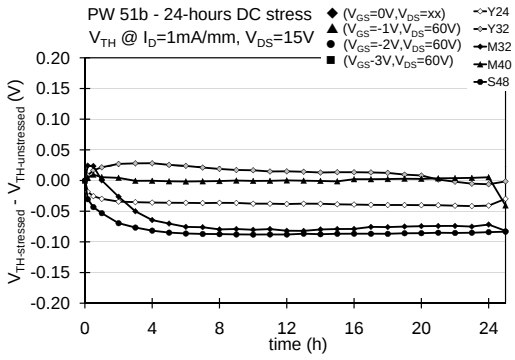
The wafer ITN2a demonstrates to be much more robust under the 24-hours stress, as is possible to see in the plots of Figure 4.13. The drain current and the transconductance show a limited degradation, that is partially recovered in the detrapping phase at the end of the stress (see Figures 4.13 (a) and (b)). Differently from wafer ITN2, the threshold voltage does not show significant variations. Even the degradation of the gate diode current is less pronounced, and increase significantly only for dissipated power greater than 30 W/mm; over this level the leakage increases even of three orders of magnitude, without affecting any others device parameters (see Figures 4.13 (e) and (f)).



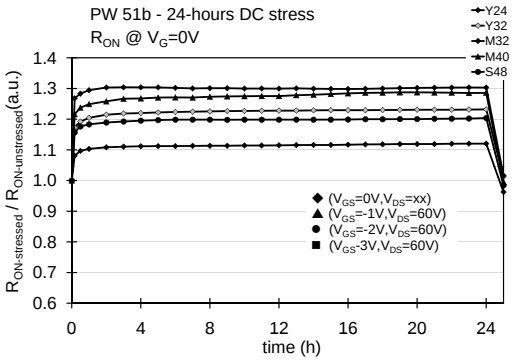
(a) $I_{DSSAT-15}$ variation.

(b) $g_{mMAX-15}$ variation.

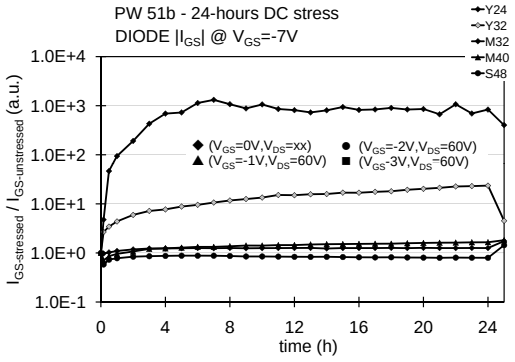
Figure 4.13: Comparison of the main parameters monitored during the 24-h DC stress on the wafer ITN2a.



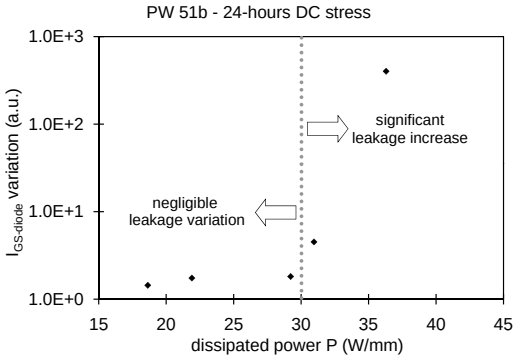
(c) V_{TH-15} variation.



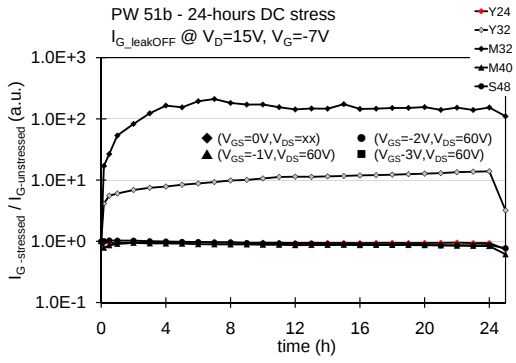
(d) On-resistance R_{ON} variation.



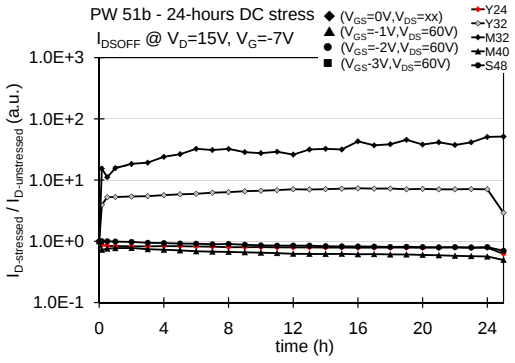
(e) I_{GS} diode variation.



(f) I_{GS} increase vs. dissipated power.



(g) $I_{leak-OFF-15}$ variation.



(h) $I_{DSOFF-15}$ variation.

Figure 4.13: Comparison of the main parameters monitored during the 24-h DC stress on the wafer ITN2a.

Like for the step-stress, at the end of the 24-hours DC stresses we try to found the failure signatures. The different robustness and the temperature influence on the device degradation is clearly highlighted in the bias points that show the degradation signature.

- Signature 1: sudden gate leakage increase (more than 10×) activated from high temperature.

Table 4.4: Signature 1.

Wafer ITN2	Wafer ITN2a
$V_{GS} = -2$ V, $V_{DS} = 60$ V	–
$V_{GS} = -1$ V, $V_{DS} = 60$ V	–
$V_{GS} = 0$ V, $V_{DS} = 60$ V	$V_{GS} = 0$ V, $V_{DS} = 60$ V
$V_{GS} = 0$ V, $V_{DS} = 45$ V	$V_{GS} = 0$ V, $V_{DS} = 45$ V
$V_{GS} = 0$ V, $V_{DS} = 30$ V	–
$V_{GS} = 1$ V, $V_{DS} = 38$ V	–

- Signature 2: limited performance drop (I_D, g_m, R_{on}) mainly focused on the knee region, even with a left threshold shift activated from the electric field.

Table 4.5: Signature 2.

Wafer ITN2	Wafer ITN2a
$V_{GS} = -2$ V, $V_{DS} = 60$ V	$V_{GS} = -2$ V, $V_{DS} = 60$ V
$V_{GS} = 0$ V, $V_{DS} = 30$ V	$V_{GS} = -1$ V, $V_{DS} = 60$ V
–	$V_{GS} = 0$ V, $V_{DS} = 60$ V

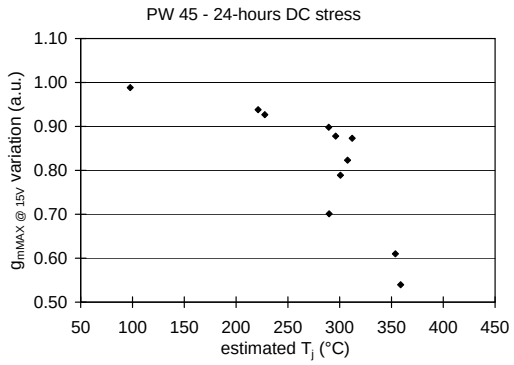
- Signature 3: significant performance drop (I_D, g_m, R_{on}) with a right threshold shift, activated over a certain temperature ($> 250°C$).

Table 4.6: Signature 3.

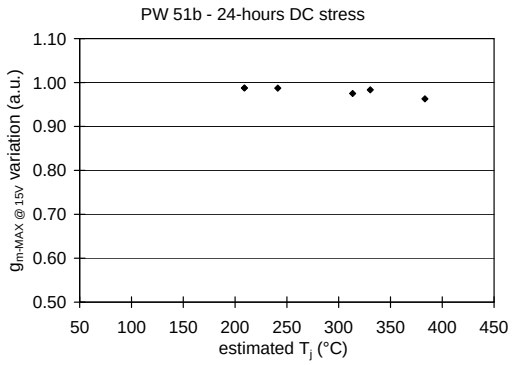
Wafer ITN2	Wafer ITN2a
$V_{GS} = -1$ V, $V_{DS} = 60$ V	–
$V_{GS} = 0$ V, $V_{DS} = 60$ V	–
$V_{GS} = 0$ V, $V_{DS} = 45$ V	–
$V_{GS} = 1$ V, $V_{DS} = 38$ V	–

The different behaviour of the two technologies to the high power tests is summarized in the graphs of Figure 4.14. Here, in order to better compare the effects of the dissipated power, it has been converted in junction temperature, estimated by means of the thermal resistance. As we can see in the plots, still at 250°C, the wafer ITN2 shows a not negligible degradation, that becomes more pronounced between 300°C and 350°C. In addition to the role of temperature in the device degradation, it seems that other elements (like hot electrons) can further accelerate the degradation process. Concerning the leakage current, it starts to rise still at low temperatures, suggesting a limited robustness of the gate for this technology.

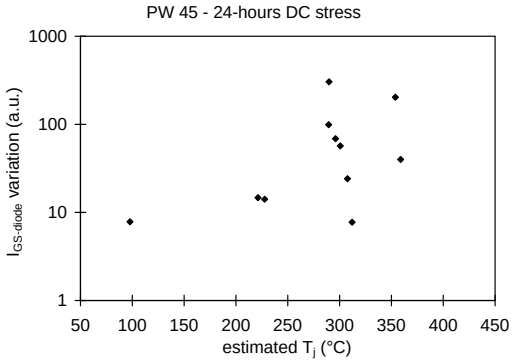
Conversely, the wafer ITN2a shows a limited performance drop up to 400°C, while only the gate diode leakage seems to have a sudden increase for temperatures higher than 320°C.



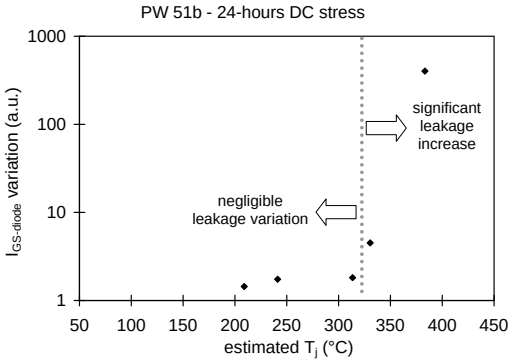
(a) g_m variation vs. T_j in ITN2.



(b) g_m variation vs. T_j in ITN2a.



(c) I_{GS} diode variation vs. T_j in ITN2.



(d) I_{GS} diode variation vs. T_j in ITN2a.

Figure 4.14: Plots of g_m e I_{GS} versus the estimated junction temperature T_j for the wafers ITN2 (left) and ITN2a (right).

4.2 Long-term reliability tests

4.2.1 Device and test description

In the following they will be reported the results of the long-term stresses on both the GH50 an GH25 technologies. This activity consists of three main type of tests:

- conventional three-temperature storage tests (4000-hours);
- DC accelerated life-tests in different operating conditions (4000-hours);
- RF accelerated life-tests in one single operating conditions close to the real target of the tested technology (500-hours).

These tests will give important information about the failure mechanisms really happening on the normal (or "accelerated") operating conditions, finding the "activating" factors of each failure mode (temperature, voltage, ...), and allowing the comparison of these phenomena with the signatures and failure mechanisms suggested by the short-term tests part.

Storage tests have been carried out on two wafers: one of the GH50-ITN3 technology and another of the of GH25-ITN2a. The wafers were divided in 4 quarters in order to use each part for a single storage temperature. For each quarter, we have tested a large amount of samples and passive components to increase the statistics of the measured data and to follow both the change of the main device performances and the variation of the basic device components, like the Schottky or the ohmic contact. As result, the tested samples were:

- 12 2x40 μm PCM samples;
- 12 4x400 μm large periphery transistors;
- 9 large area FATFET samples;
- 3 TLM structures.

Table 4.7: Layout of the packaged devices submitted to the life test activity.

Technology	Device name	L_G (μm)	W_G (μm)	STFP (μm)	L_{GS} (μm)	L_{GD} (μm)
GH50-ITN3	1x4x400_50_V1	0.50	1600	2.3	1.5	4.0
GH25-ITN2a	DEC XBAND MS V1	0.25	1000	1.0	0.8	2.7
GH25-ITN2a	DEC XBAND MS V3F	0.25	1000	1.0	0.8	1.7

Storage tests have been performed in air atmosphere at the same three temperatures for both technologies: $T_1 = 300°C$, $T_2 = 325°C$ and $T_3 = 350°C$.

For the life-test activities (DC and RF), we used large periphery devices of both GH50-ITN3 and GH25-ITN2a technologies, soldered inside a high-frequency high-temperature Schott package. The layout of the packaged sample are reported in Table 4.7. The details of the stress conditions of the life tests will be reported in the related sections.

Before the beginning of each long-term reliability test, samples have been submitted to a standard characterization routine (DC, pulsed, thermal resistance), in order to extract the main performance parameters useful for the following tests. For packaged devices two testing systems have been adopted: a burn-in system from *i-Test* and an accelerated system from *AccelRF*; with the latter, RF characterization suite has been performed as well before the beginning of the test. Tests have been interrupted at specific target times, defined according to a 1h, 2h, 5h, 10h, 20h, 50h, 100h scheme up to 4000h, where complete DC characterization has been repeated following the variation of the static parameters, while pulsed measurements have only been measured at every decade of stress time (i.e. 10h, 100h, 1000h, 4000h).

4.2.2 Long-term tests for the GH50 technology

Thermal storage

In the following we will report the main results gathered from the storage test on GH50 technology, confirming its really good stability and the capability to withstand really high temperatures with no significant degradation effects. In particular:

- Figure 4.15 reports on the electrical characteristics of small periphery transistors ($W_G = 2x40\,\mu m$);
- Figure 4.16 reports on the electrical characteristics of the large periphery transistors ($W_G = 4x400\,\mu m$);
- Figure 4.17 reports on the electrical characteristics of FATFET Schottky diodes;
- Figure 4.18 reports on the electrical characteristics of TLM ohmic contacts;

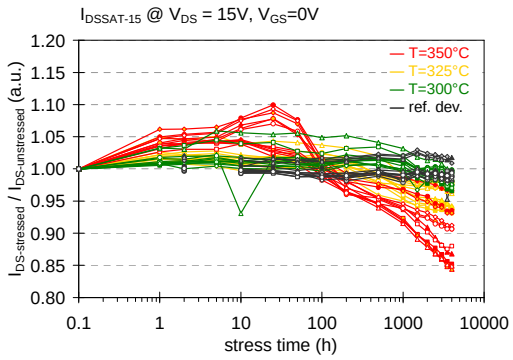
In all these figures, red curves report data at $T_3 = 350°C$ storage temperature, yellow curves report data at $T_2 = 325°C$ storage temperature, green curves report data at $T_1 = 300°C$ storage temperature, while black curves refer to reference devices.

Looking at the main parameters like the drain saturation current I_{DSSAT} or the transconductance g_{m-MAX}, small and large periphery devices showed a common behaviour, with a gradual reduction of the I_{DSSAT} depending on the test temperature: at $T_3 = 350°C$ the reduction starts after 100-hours reaching final variations of 10–15%; at $T_2 = 325°C$ the decrease starts later than 500-hours with final degradation in the order of 5%, although some recovery seen on $4x400\,\mu m$ transistors; at $T_3 = 350°C$ the decrease is almost negligible, with values below 4% which are quite comparable with reference samples. On the contrary, transconductance and R_{ON} seems to be not influenced by the high temperature, with variation below 5% with no clear dependence on the test temperature, suggesting

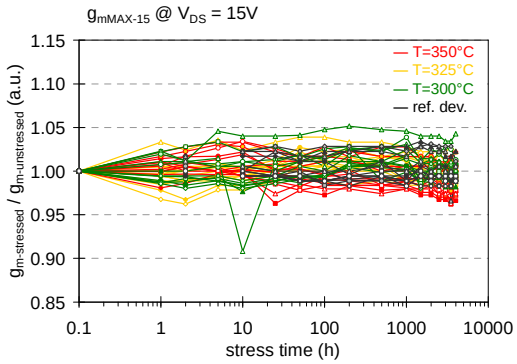
the slow but gradual positive V_{th} shift as the main origin of the drain current degradation, in the range of 200-250 mV at $T_3 = 350°C$.

The second most evident effect of the storage test is the behaviour of the leakage currents (in off-state or in GS diode), which shows a sudden increase during the first hours of test and then recovers from 200 to 2000-hours depending on the storage temperature. This effect is clearly present in small periphery devices (see Figure 4.15 (e) and (f)), large periphery devices (see Figure 4.16 (e) and (f)), as well as FATFET Schottky diodes (Figure 4.17 (a)), independently from the starting value of the leakage or to the geometry. The only difference is (i) the time at which the leakage stop increasing, lower on devices with higher initial leakage, (ii) the amount of the drain leakage increase, more pronounced on 2x40 μm devices, and generally higher at $T_3 = 350°C$, and (iii) the duration of the effect. Leakage on samples tested at $T_3 = 350°C$ started at 0h and finished after 100-200h; leakage on samples tested at $T_2 = 325°C$ started after 1-2h and recover after 1000h; leakages on samples at $T_1 = 300°C$ started after 2-10h (depending on the geometry) and are still increasing after 4000h. The effect seems to be thermally activated, but the big variation of the subthreshold behaviour, especially at the low temperatures, is contributing to the leakage growth. In fact, while on small devices the off-state drain current (I_{DS-OFF}) is following the off-state gate leakage behaviour on all three test temperatures, on large devices the worsening of the subthreshold properties drives the off-state drain current toward higher values, in the order of 100 μA/mm for all three temperatures.

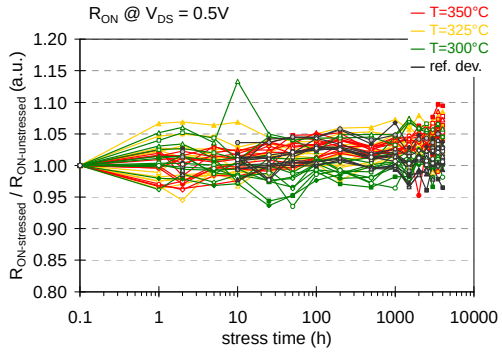
Passive structures evaluated on FATFET samples and TLM structures are confirming what observed in transistor characteristics, with the same behaviour of the gate leakage (see Figure 4.17) and a good stability of the ohmic resistance (see Figure 4.18). The variation of the series resistance on some FATFET samples highlighted in Figure 4.17 (b) does not seem to be correlated with a real diode degradation, but on the contrary to a sort of annealing step which brought the diode series resistance at the same value of the other "better" tested samples.



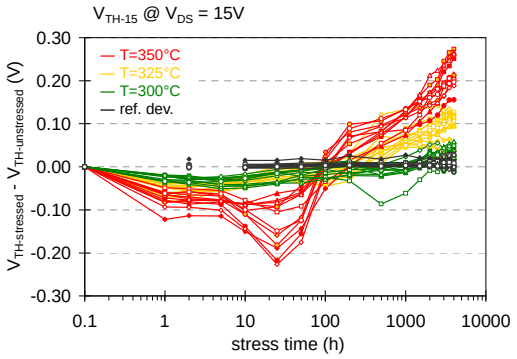
(a) I_{DS} variation.



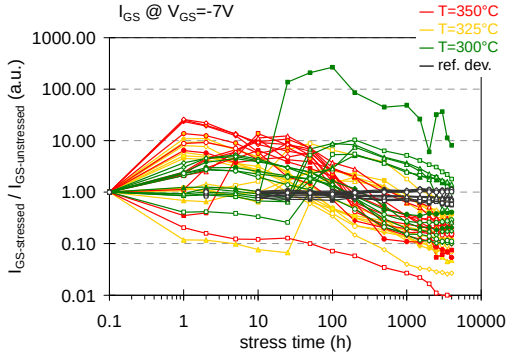
(b) g_m peak variation.



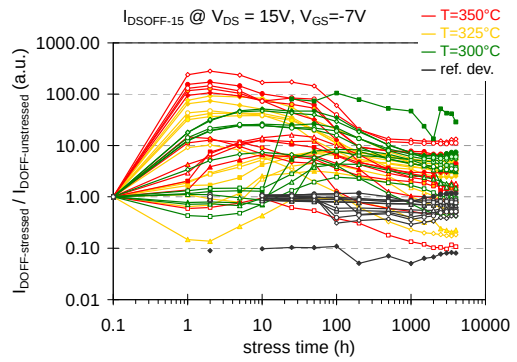
(c) R_{ON} variation.



(d) V_{th} variation.

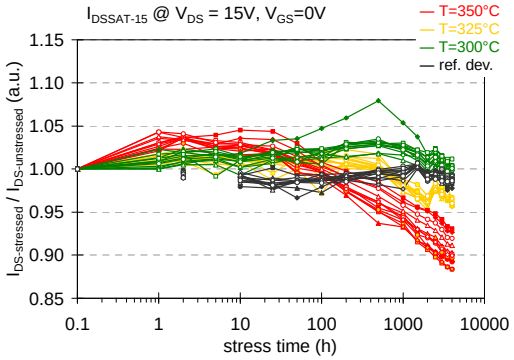


(e) I_{GS} diode variation.

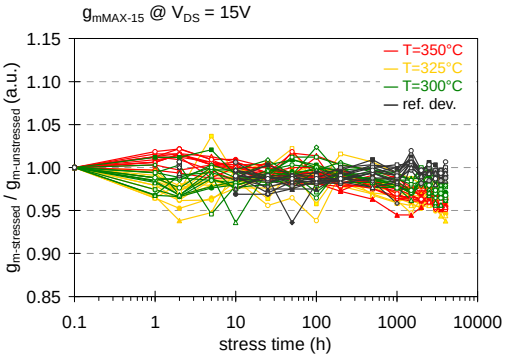


(f) I_{DS} leakage variation.

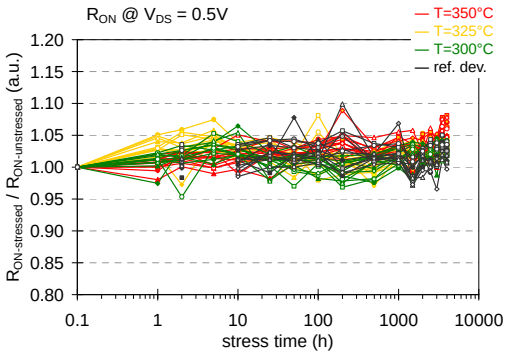
Figure 4.15: Variation of the main electrical parameters of 2x40 μm transistors submitted to storage tests. Red curves refer to device tested at $T_3 = 350°C$, yellow curves refer to device tested at $T_2 = 325°C$, green curves refer to device tested at $T_1 = 300°C$, while black curves refer to reference devices.



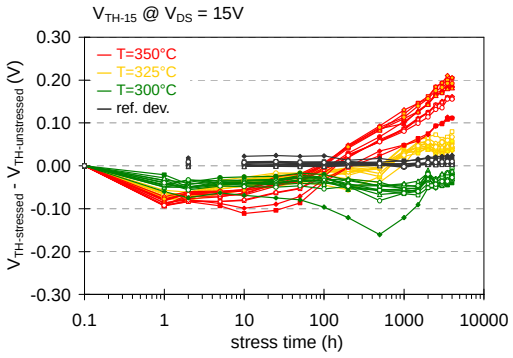
(a) I_{DS} variation.



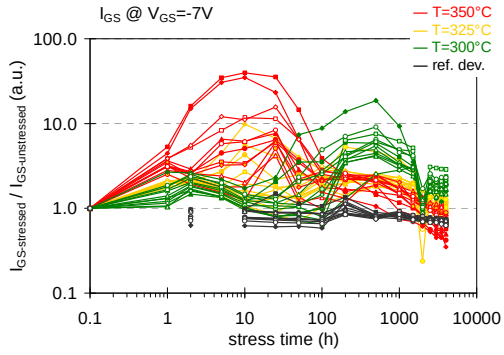
(b) g_m peak variation.



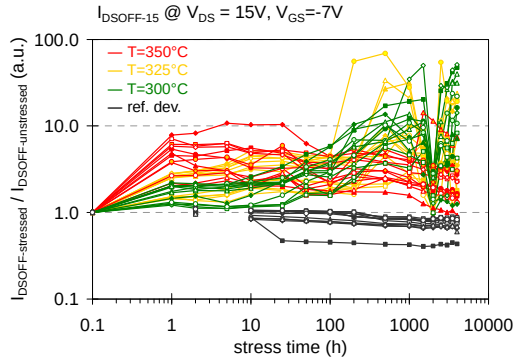
(c) R_{ON} variation.



(d) V_{th} variation.

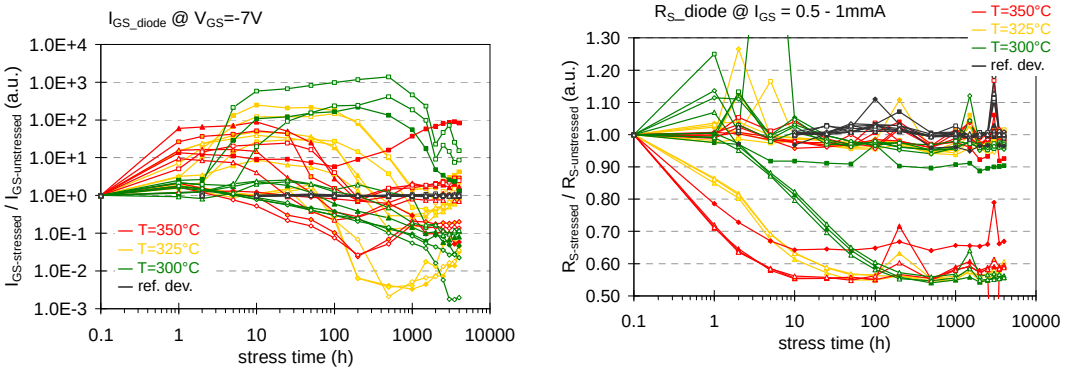


(e) I_{GS} diode variation.



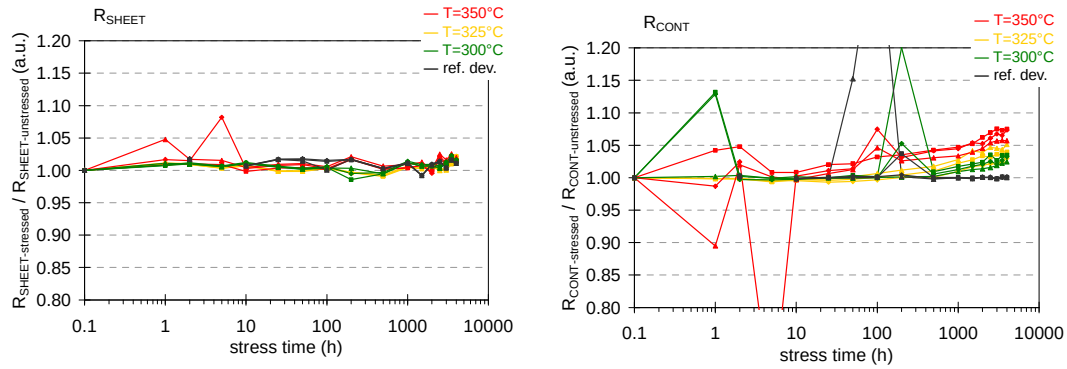
(f) I_{DS} leakage variation.

Figure 4.16: Variation of the main electrical parameters of 4x400 μm transistors submitted to storage tests. Red curves refer to device tested at $T_3 = 350°C$, yellow curves refer to device tested at $T_2 = 325°C$, green curves refer to device tested at $T_1 = 300°C$, while black curves refer to reference devices.



(a) Schottky diode leakage variation. (b) Schottky diode series resistance variation.

Figure 4.17: Variation of the electrical parameters of FATFET samples submitted to storage tests in term of diode leakage and parasitic series resistance. Red curves refer to device tested at $T_3 = 350°C$, yellow curves refer to device tested at $T_2 = 325°C$, green curves refer to device tested at $T_1 = 300°C$, while black curves refer to reference devices.



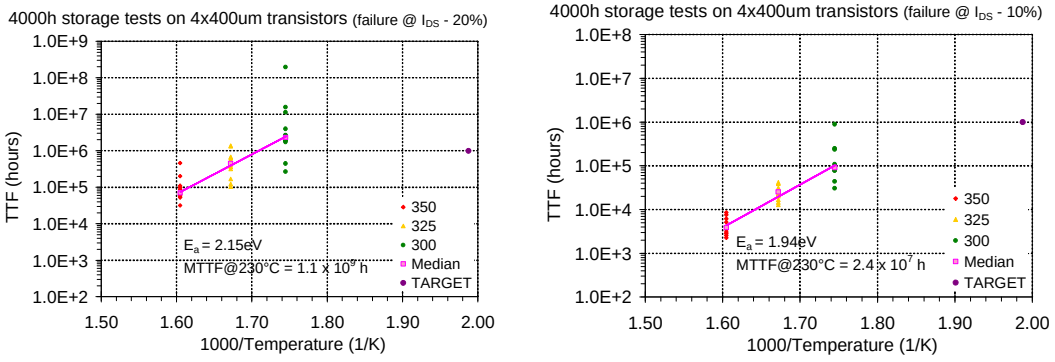
(a) Sheet resistance variation. (b) Contact resistance variation.

Figure 4.18: Variation of the electrical parameters of TLM structure submitted to storage tests, in term of sheet and contact resistance. Red curves refer to device tested at $T_3 = 350°C$, yellow curves refer to device tested at $T_2 = 325°C$, green curves refer to device tested at $T_1 = 300°C$, while black curves refer to reference devices.

Summarizing the results obtained from three temperature storage tests in GH50 technology, we can underline the following degradation modes:

1. Looking at the failure criteria, the drain current gradually decreases following the evolution of the threshold voltage, with a small increase after the first hours of test (V_{th} left shift) and a slow gradual decrease of I_{DS} values (V_{th} positive shift) happening from 100 to 1000-hours. This mechanism is activated by the temperature, due to the different starting point of the drain current worsening. Preliminary extraction of the MTTF at T = 230°C (20% I_{DS} degradation) provides an expected life-time of 10^9 hours, since most of the samples have exceeded the 4000-hours without reaching the failure criteria (see Figure 4.19). If we change this limit at 10% (I_{DS}) decrease, the estimated life-time is 2.4×10^7 hours, which is still quite longer than the expected target of 10^6 hours.

2. A sudden increase of all leakage currents, which starts at the beginning of the storage and then recovers from 200 to 2000-hours of test, depending on the test temperature. This effect is clearly visible in all tested samples (from transistor to Schottky diodes) even if it is still not clear which physical phenomena drive this double trend of the leakage behaviour.

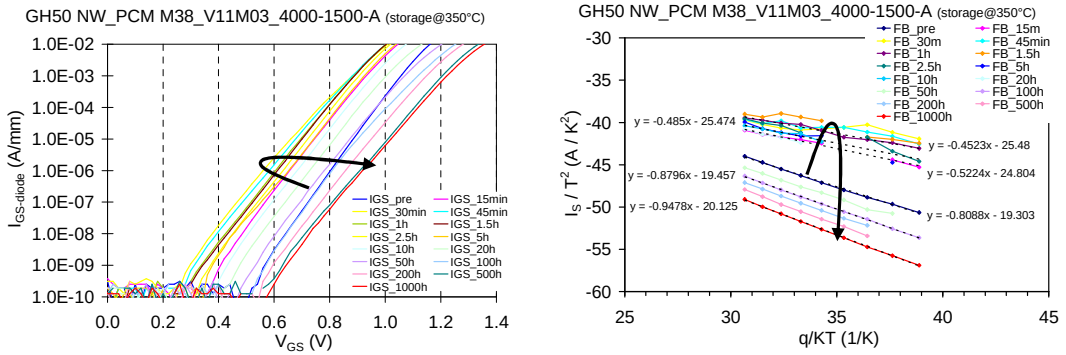


(a) Failure criterion at 20% I_{DS} decrease. (b) Failure criterion at 10% I_{DS} decrease

Figure 4.19: Evaluation of Time-to-Failure over temperature extracted from the long-term storage tests on large periphery GH50 transistors, for 20% I_{DS} decrease (a) and 10% I_{DS} decrease (b).

3. Further tests aimed at following the kinetics of the barrier height gives us more information, showing (i) a decrease of the barrier height during the first hour of about 0.3/0.4 eV (with some worsening of the ideality factor of 0.1/0.2), followed by (ii) a complete recovery of both elements in 20-50 hours, and (iii) stable diode parameters from 100 to 1000-hours which provide only a slightly higher barrier (0.1 eV) and a slightly lower ideality factors. At the end of the test, the main variation is represented by a shift of the curve in the Richardson plot (see Figure 4.20).

4. All other characteristics correlated with the series resistance (like the Schottky series resistance, the ohmic contacts, the R_{ON} or the g_m) has not been influenced by the storage, with variations within 5%, as well as the transistor dynamic behaviour.



(a) GS forward characteristics.

(b) Richardson plot

Figure 4.20: Analysis of the barrier height kinetics during storage test at $T_3 = 350°C$ on one typical small periphery sample ($W_G = 4x400\,\mu m$).

DC life-tests

DC life-test activity consisted in a set of 4000-hours stress carried out at different accelerated bias conditions, with the main purpose of extracting the mean time-to-failure of the tested technology at the target operating bias-point and to investigate the long-term effects of particular extreme bias conditions (like high-voltage or high-current points) on the device behaviour. Tested samples were 4x400 μm transistors belonging to the GH50-ITN3 technology. Samples were packaged on a 2-pin Schott package.

The DC bias points have been chosen to investigate not only the effect of temperature on device degradation (from 250°C to 350°C of junction temperature T_{jmax}), but also the effect of the high-field ($V_{DS} = 100\,V$) or the high drain-current ($I_{DS} \approx 500$ mA).

Base plate temperature has then been adjusted according to the R_{TH} formula that estimates the peak and the average junction temperature of GH50 4x400 μm packaged samples by means of a calibrated 3D electro-thermal simulation:

$$R_{TH,T_{max}}(P_D, T_{BP}) = 4.36\,(K/W) + 0.188\,(K/W^2) \cdot P_D + 0.003145\,(1/W)\,T_{BP}$$

$$R_{TH,T_{avg}}(P_D, T_{BP}) = 4.42\,(K/W) + 0.182\,(K/W^2) \cdot P_D + 0.002798\,(1/W)\,T_{BP}$$

By means of these formulas, we have used the target temperatures (250, 300 and 350°C) and the defined bias conditions in order to obtain the correct base-plate temperature. As a result, in Table 4.8 and Figure 4.21 are reported the list of the 5 adopted bias-points which have been used for GH50 DC life-test activity.

Table 4.8: List of bias-points adopted for the long-term DC life-tests on GH50 technology.

	I_{DS} (A/mm)	V_{DS} (V)	P_D (W)	T_{BP} (°C)	$R_{TH,T_{max}}$ (K/W)	$R_{TH,T_{avg}}$ (K/W)	T_{jmax} (°C)	T_{javg} (°C)	# dev
BP1	0.125	50	10	80	17.34	16.12	253.4	241.2	4
BP2	0.125	50	10	120	18.60	17.24	306.0	292.4	5
BP3	0.125	50	10	155	19.70	18.22	352.0	337.2	5
BP4	0.300	25	12	125	19.13	17.74	354.6	337.9	2
BP5	0.050	100	8	150	19.17	17.71	303.3	291.7	2

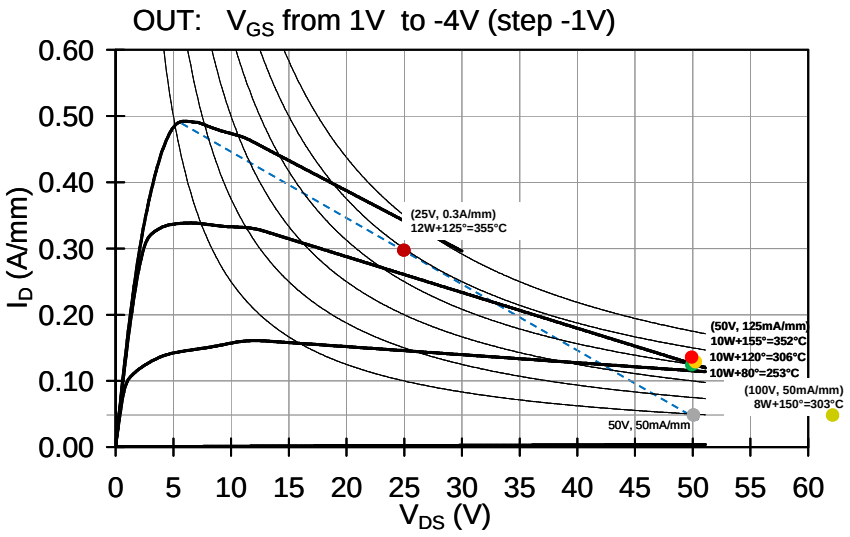
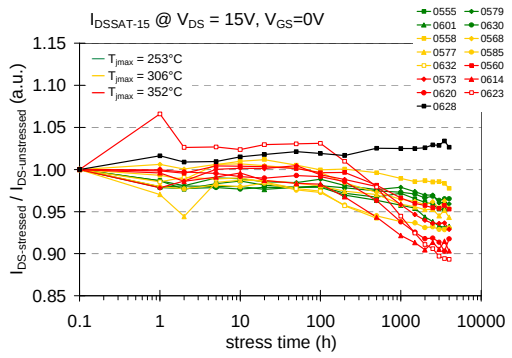
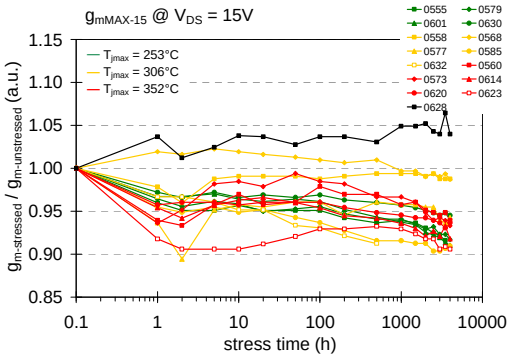


Figure 4.21: Schematic representation of the bias-points adopted for the long-term DC life tests on GH50 technology.

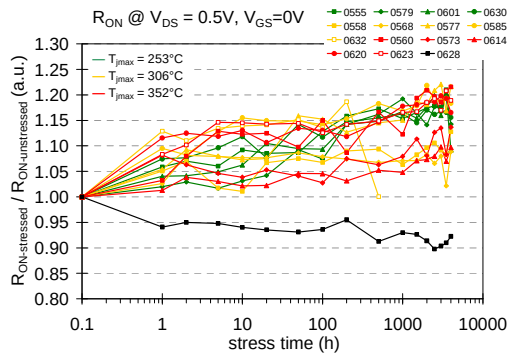
Figure 4.22 reports the results of the DC life test at the BP1, BP2 and BP3 bias points for the GH50-ITN3 technology. The first hours of test have caused a sudden variation of the main performances on almost all tested samples and in all test temperatures, with a 5% maximum reduction of the g_m and a small V_{th} shift. On the contrary, the drain current has kept stable values within 2% variation. Up to 100-hours we have not observed any other significant variation of device performances. After that point, we have seen a slow decrease of the main performances (I_{DS} and g_m) followed by a small and gradual increase of the on-resistance (around 10-15%); Typical I_{DS} degradation have reached 8-10% at $T_j = 350°C$ (see Figure 4.22 (a)) and almost 5% at $T_j = 300°C$, while the transconductance shows more confused results not so correlated with the device junction temperature T_j. Concerning the leakage currents, five samples have experienced a sudden large gate degradation during the first hour of stress (three from BP2 and two from BP3), reaching high values of gate and drain leakage in the order of 100 μA/mm or higher, but this high leakage contribution has not caused any visible static parameter modification on the tested devices, at least up to 1000-hours. On the contrary, the other samples have shown a behaviour quite correlated with the junction temperature, pretty similar to what observed in storage tests. Devices at BP3 at $T_j = 350°C$ have shown a sudden increase of the gate leakage up to 10-times during the first hours which then recovered after about 200 hours of life-test, followed by a small decrease of the off-state drain current. Devices in BP2 at $T_j = 300°C$ have exhibited the same behaviour on the longer time scale, while devices in BP1 at $T_j = 250°C$ have shown a very limited leakage variation, with stable or slightly decreasing leakage values. After 500-1000 hours, when the transient behaviour of the leakage was almost finished, we can notice the permanent effects on the device behaviour. The reduction of the drain current was partially driven by the limited g_m reduction, and mainly driven by a positive threshold voltage shift. After 1000-h, the V_{th} variation induced by the increase of the off-state drain current was finished, resulting in a positive shift of threshold voltage, which is the main reason of the I_D degradation.



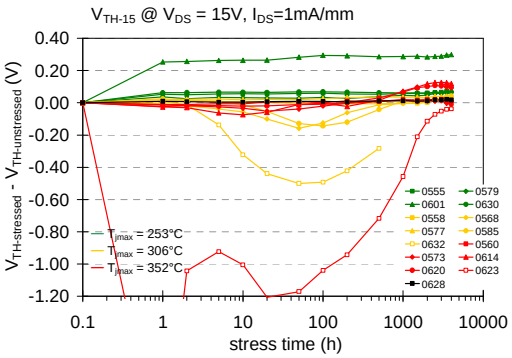
(a) I_{DS} variation.



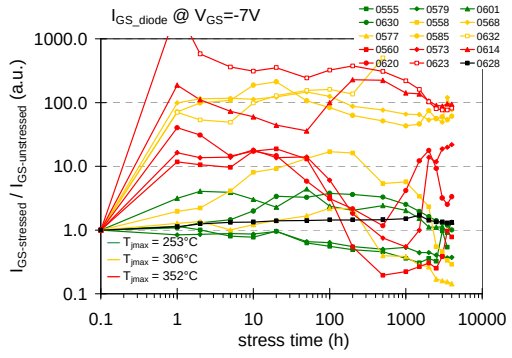
(b) g_m peak variation.



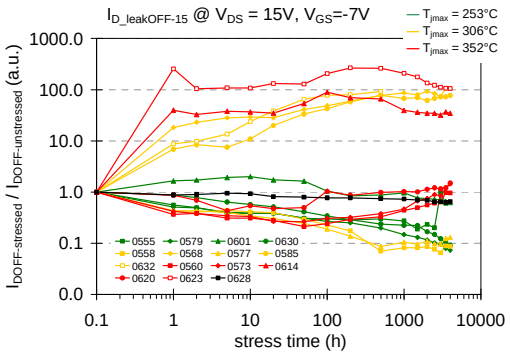
(c) R_{ON} variation.



(d) V_{th} variation.



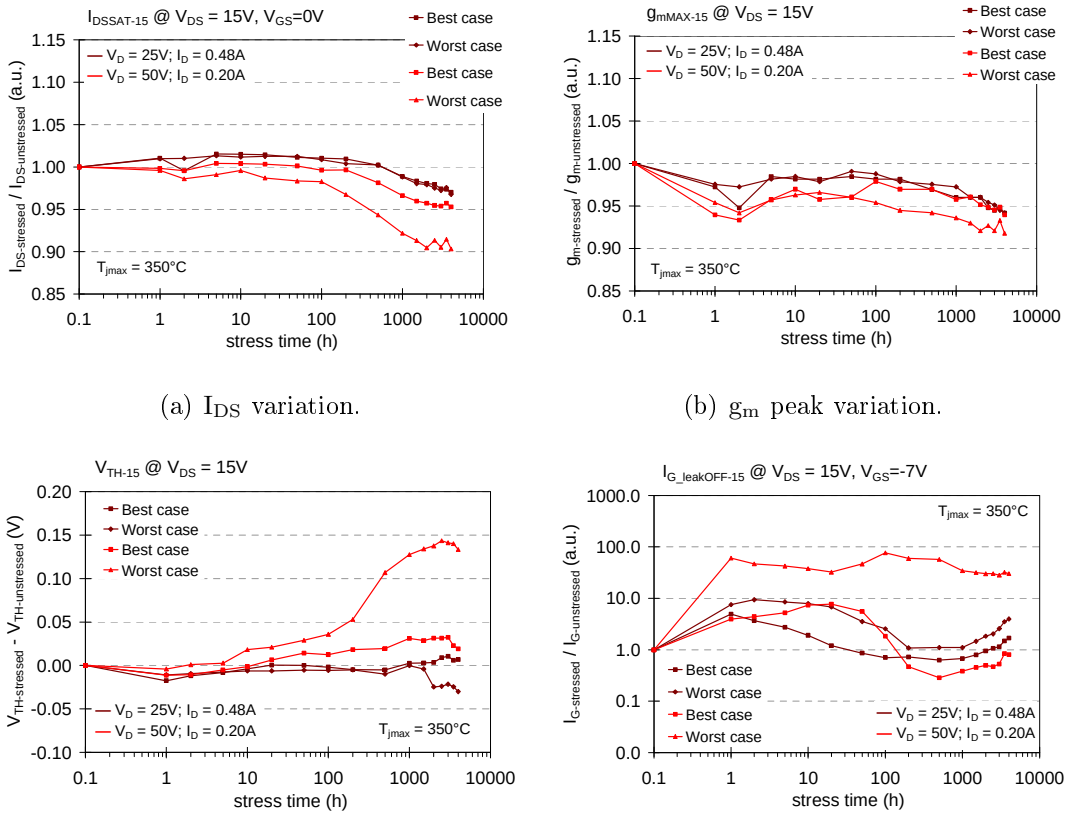
(e) I_{GS} diode variation.



(f) I_{DS} leakage variation.

Figure 4.22: Variation of the main electrical parameters of GH50 on-package samples submitted to BP1 (green curves), BP2 (yellow curves) and BP3 (red curves) life-test conditions. The black curves refer to the reference sample.

For the bias points BP4 and BP5 we will report some comparison graphs with the other bias points. For the sake of clarity we show only the worst and the best case for each bias point. Figure 4.23 compares the best and worst result obtained during life test at bias point BP3 ($V_{DS} = 50\,V$, $I_D = 200\,mA$) and BP4 ($V_{DS} = 25\,V$, $I_D = 480\,mA$), nominally at the same junction temperature of 350°C. These figures suggest either a contribution of electric field/hot electrons in accelerating the degradation, or a different thermal distribution within the device, resulting in enhanced thermal effects. Figure 4.24 compares the best and worst results obtained during life test at bias point BP2 ($V_{DS} = 50\,V$, $I_D = 200\,mA$) and BP5 ($V_{DS} = 100\,V$, $I_D = 80\,mA$), nominally at the same junction temperature of 300°C.



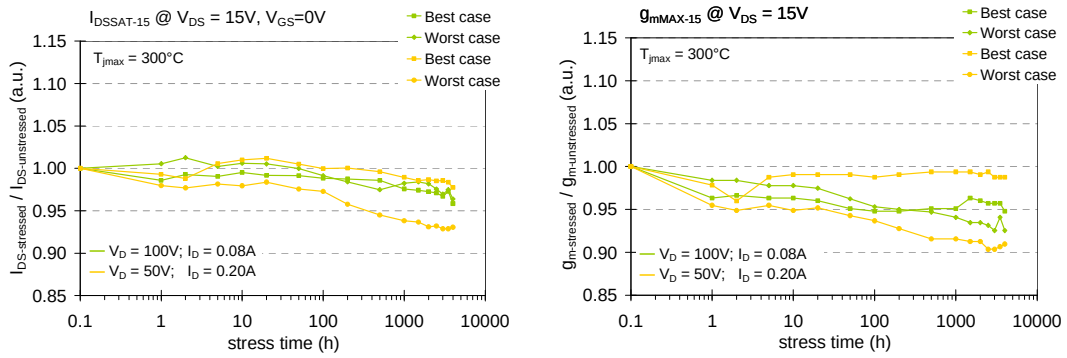
(a) I_{DS} variation.

(b) g_m peak variation.

(c) V_{th} variation.

(d) Off-state leakage I_g variation.

Figure 4.23: Best and worst case for the GH50 DC life-test (BP3, BP4).



(a) I_{DS} variation. (b) g_m peak variation.

Figure 4.24: Best and worst case for the GH50 DC life-test (BP2, BP5).

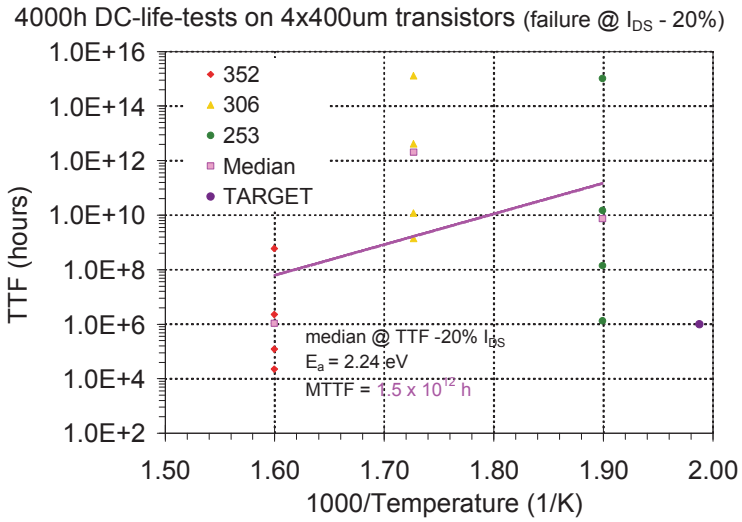


Figure 4.25: Evaluation of Time-to-Failure over temperature extracted from BP1, BP2 and BP3 DC life-tests on packaged GH50 transistors; the failure criterion is 20% I_{DS} decrease.

The degradation of GH50-ITN3 devices submitted to DC life tests at high temperature appears therefore to be due to two effects: (i) a thermally-accelerated threshold voltage shift, similar to that observed during storage tests, enhanced by the electric field or by hot electrons; (ii) a degradation of the gate-drain access region, due to hot-electrons or field-induced damage, inducing an increase of on-resistance and a decrease of the maximum transconductance value.

The extrapolated device life-time based on 20% I_{DS} decrease, reported in Figure 4.25, provides an activation energy $E_a = 2.2\,eV$, and shows that the estimated life-time is really high at the target temperature of 230°C ($> 10^{12}$ hours). This value is only a rough estimation, and widely exceed the target of 10^6 hours; the confidence is not too high due to the wide spread of the TTF values for both three test temperatures. However, even in the worst case of the lower test temperature (250°C), the target life-time is reached; so, we can trust that in any case the life time at 230°C exceeds the target.

RF life-tests

The last long-term reliability activity of GH50 samples was the RF life-test activity, carried out on 6 GH50-ITN3 packaged samples using the *AARTS AccelRF* system. The RF life-test activity consisted in 500-hours stress carried out at the nominal bias condition ($V_{DS} = 50\,V$, $I_{DS} = 50\,mA/mm$, P_{in} @ peak PAE, $f = 1.7\,GHz$) in accelerated temperature conditions ($T_j = 350°C$), with the main purpose of speeding up the thermally activated failure mechanisms and of extracting the typical time-to-failure of the tested technology. Tested samples were 4x400 μm transistors belonging to the GH50-ITN3 technology with the main layout details reported in Table 4.7 at pag. 73.

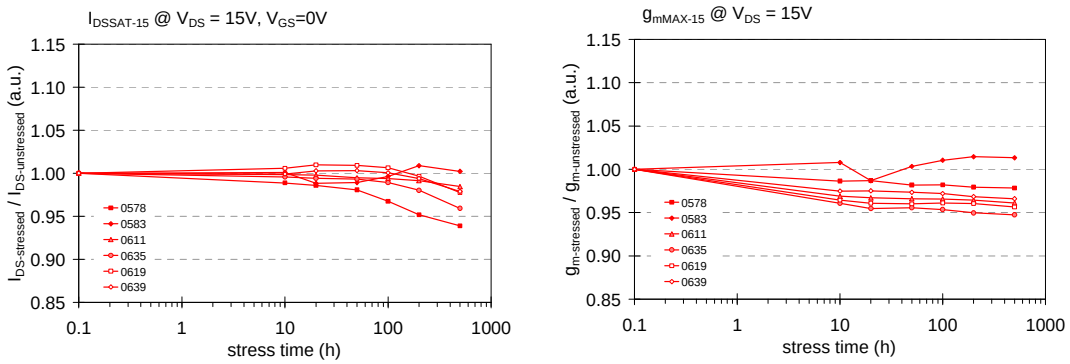
The test has been interrupted at the following test-times: 10h, 20h, 50h, 100h, 200h, and 500h; at each step, DC and GC (gain-compression) characterizations have been performed at 50°C. Double-pulse measurements, carried out on a different test bench, have been performed only when P_{out} reached half of the failure criteria (0.5 dB P_{out} decrease), as well as at the beginning and at the end of the life-test.

The GC characterization suite has been performed at the following conditions:

- $V_{DS} = 50\,V$; V_{GS0} @ $I_{DS} = 50\,mA/mm = 80\,mA$
- P_{in} from 8 dBm to 28 dBm (or $I_G < 10\,mA/mm$)
- $T_{BasePlate} = 50°C$

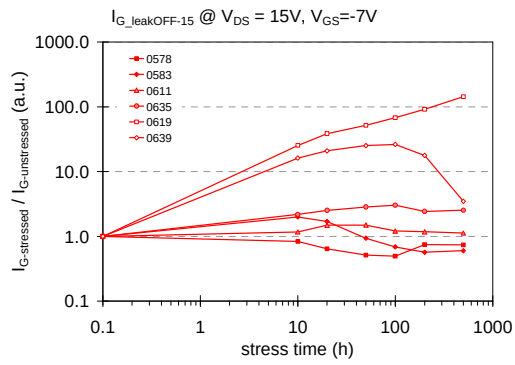
Results reported in Figure 4.26, Figure 4.27, and Figure 4.28 summarize the behaviour of the six GH50 samples submitted to 500-hours RF life-test at 350°C of junction temperature. In these diagrams we can observe the really good stability of this technology during RF life-test, but the gradual degradation of the large-signal performances suggests the presence of a different failure mechanism, which has not been observed in long-term DC or storage tests.

The main DC performances show variations within 6%, with a general slow reduction of the transconductance and a gradual decrease of the drain current starting from 50-100 hours of test (see Figure 4.26 (a) and (b)). These results follow what already observed during comparable DC life-tests at $T_j \approx 350$°C and storage tests at 350°C, confirming the influence of the transconductance reduction

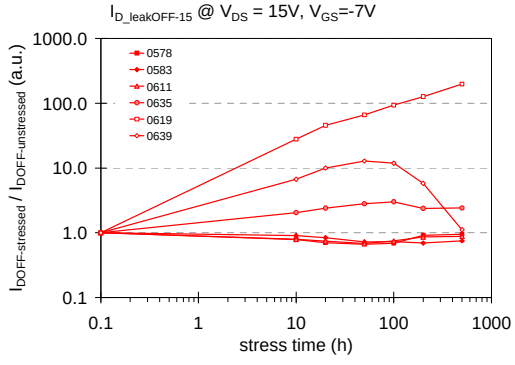


(a) I_{DS} variation.

(b) g_m peak variation.



(c) Off-state gate leakage variation.



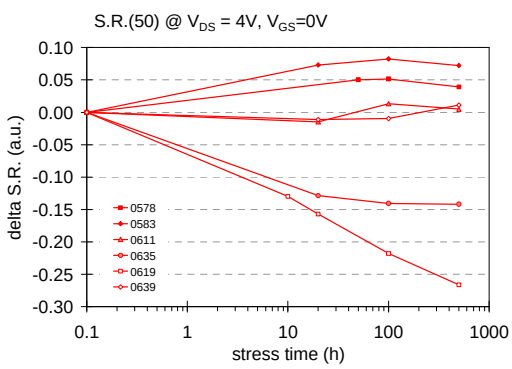
(d) Off-state drain leakage variation.

Figure 4.26: Variation of the main DC electrical parameters of five samples submitted to RF life-test at $T_j = 350$°C.

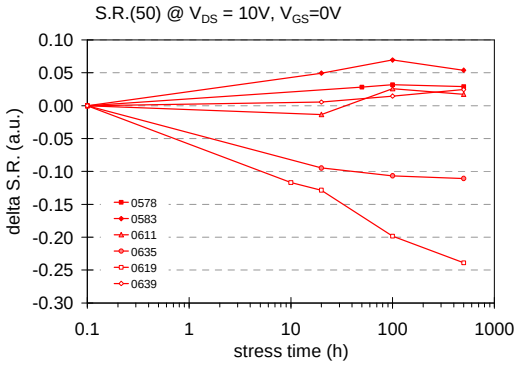
on the first I_{DS} decrease, and that the positive V_{th} shift should start after 500-1000 hours, here not reached by the lower target time.

On the contrary, leakage currents have not shown the gate and drain leakage parabolic behaviour seen on both storage and DC life-tests at 350°C, but only a small leakage reduction and a slight variation of the GS diode characteristic. Three of the six samples, however (0619, 0635, 0639) show non recoverable 10x-100x increase of gate leakage current similar to what happened in BP2 and BP3 DC life-test conditions, suggesting that bias conditions close to $T_j \approx 350$°C could be critical for the stability of the gate junction.

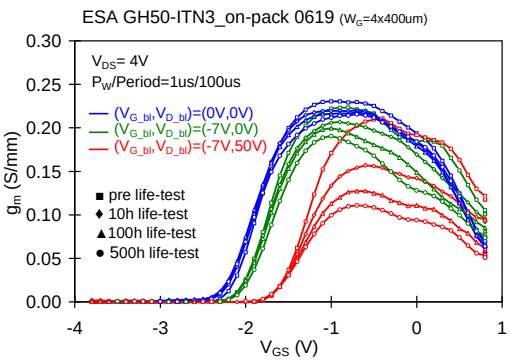
Looking at the pulsed measurements of Figure 4.27 we can see that only two



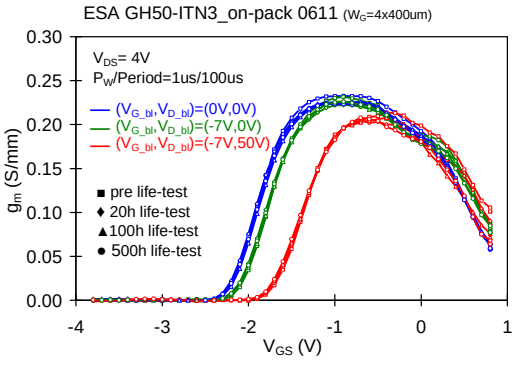
(a) S.R. in knee region at $V_{DS} = 4$ V.



(b) S.R. in saturation region at $V_{DS} = 10$ V.



(c) High-leakage sample.

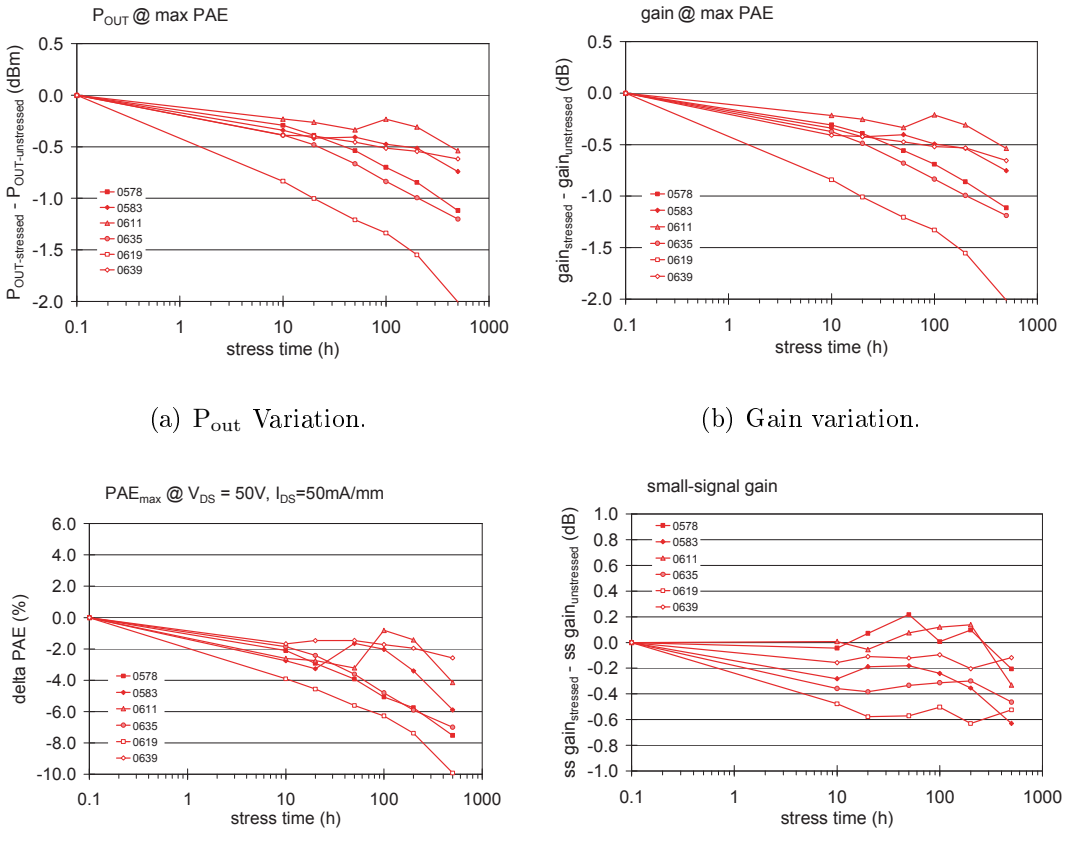


(d) Normal low-leakage sample.

Figure 4.27: Variation of the main pulsed electrical parameters of five samples submitted to RF life-test at $T_j = 350$°C (a) and (b); detail of the pulsed transconductance reduction in one leakage device (c) and one low-leakage device (d).

devices show a Slump-Ratio drop, while the others are substantially stable during the RF life-test. As we can see in the comparison of Figure 4.29 (a) the drop in pulsed performance is correlated with the leakage increase.

Concerning the RF performance, results of GC sweeps show significant changes of device performances, reaching the failure criteria decrease of 1 dBm-P_{out} in three out of six tested samples, around 200h, 350h, and around 20-hours respectively. In the last case, the really low time-to-failure places this device out of the total device statistics. The RF degradation is gradual on the 500-hours stress, and mainly related to the large signal performance, like P_{out} and large-signal gain, while the PAEs decrease ranges from 3% (better device) to 10% (worse device), see Figure 4.28. On the contrary, small signal performances exhibit less than



(a) P_{out} Variation.

(b) Gain variation.

(c) PAE variation.

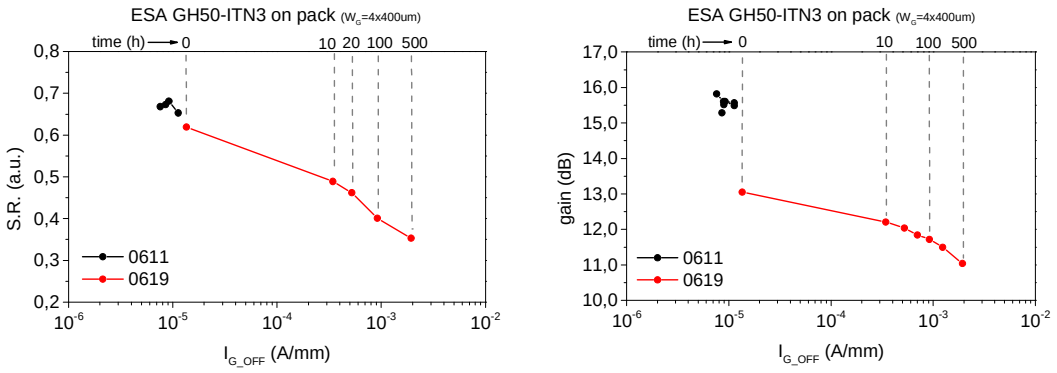
(d) Small signal gain variation.

Figure 4.28: Variation of the main RF performances of the five samples submitted to RF life-test at $T_j = 350°C$.

0.6 dB reduction. The faster degradation has been reached by the samples which presented the higher gate leakage level, suggesting a correlation between gate leakage during the RF stress and performance degradation. If we use the activation energy of the DC life-tests on the same device technology ($E_a = 2.24\,eV$), we could extract a MTTF of $1.8 \cdot 10^7$ hours at -1 dBm decrease of P_{out}.

Probably the 350°C T_j RF life-test is an over-stress condition for GH50 technology, possibly inducing unrealistic failure mechanisms. However, this result indicates that the mean behaviour will ensure the lifetime requested by the application (10^6 hours), while the worse sample which experienced the fastest performance decrease will still provide a life-time higher than 20 years ($4.1 \cdot 10^5$ hours, see Figure 4.30).

In conclusion, RF life tests at 350°C represent the harshest condition for GH50 devices: in the worst case 500 hours of RF test correspond to 4000 hours DC life tests at the same temperature considering a 20% I_{DS} decrease as failure criteria. It should be stressed, however, that devices which show low and stable leakage current typically show very reduced degradation of rf parameters, and that gate leakage current, slump ratio and rf performance drop are correlated, see Figure 4.29.



(a) P_{out} Variation. (b) Gain variation.

Figure 4.29: Correlation between (a) slump ratio and gate leakage in off-state and (b) RF gain and gate leakage during the GH50 RF stress.

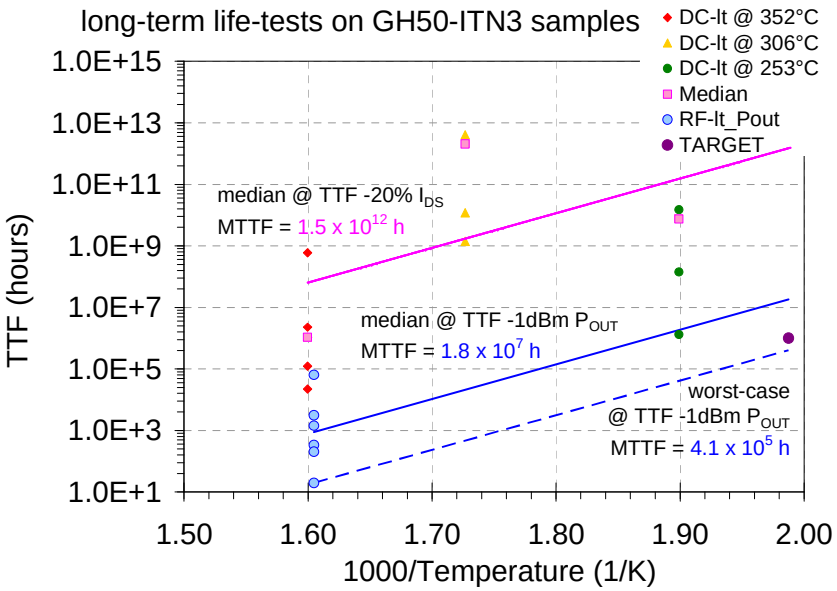


Figure 4.30: Estimated life-time on GH50 RF life-tests based on the activation energy extracted from the DC life-tests of the same device technology. Expected MTTF of $1.8 \cdot 10^7$ hours at -1 dBm P_{OUT} decrease for the median of sample population, while $4.1 \cdot 10^5$ hours MTTF for the worst case.

4.2.3 Long-term tests for the GH25 technology

Thermal storage

In the following we will report the main results gathered from the storage test on GH25 technology, confirming its really good stability and the capability to withstand really high temperatures with no significant degradation effects. In particular:

- Figure 4.31 reports on the electrical characteristics of small periphery transistors (W_G = 2x40 μm);
- Figure 4.32 reports on the electrical characteristics of the large periphery transistors (W_G = 4x400 μm);
- Figure 4.33 reports on the electrical characteristics of FATFET Schottky diodes;
- Figure 4.34 reports on the electrical characteristics of TLM ohmic contacts;

In all these figures, red curves report data at T_3 = 350°C storage temperature, yellow curves report data at T_2 = 325°C storage temperature, green curves report data at T_1 = 300°C storage temperature, while black curves refer to reference devices.

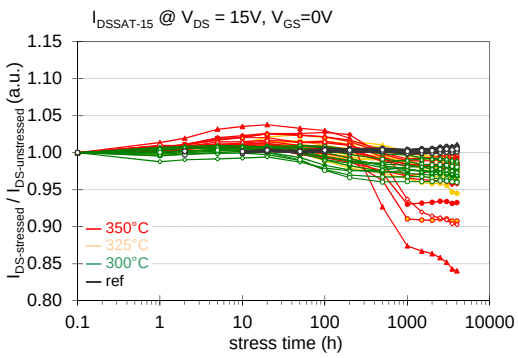
The 4000-hours of storage test shown a good stability of tested devices with a not homogenous behaviour on device performances and some critical effects on the leakage currents. Looking at small and large periphery transistors, we have observed really stable performances on all test temperatures up to 500-hours (3-4% maximum degradation); but after that point, some samples at 350°C have exhibited a sharp degradation of both I_{DS} and g_m values (see red curves in Figures 4.31 (a) and (b) and Figures 4.32 (a) and (b)).

Concerning gate leakage, we have seen a common behaviour between small and large periphery devices. At 350°C we have observed a double trend of gate and drain leakages (similar to what observed in GH50 technology), which at first

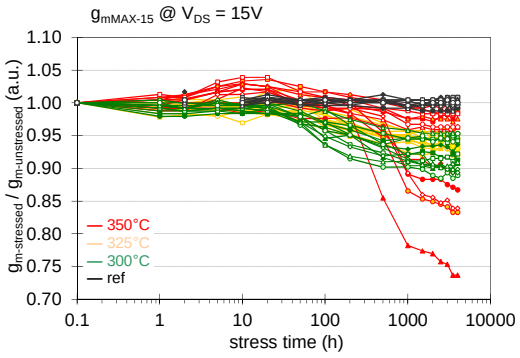
increased up to 10-times in 100-200 hours, and then slowly decreased (see Figures 4.31 (e) and (f) and Figures 4.32 (e) and (f)). But since the last points after 1000-hours are providing almost stable leakage values, it suggests a permanent leakage current phenomenon rather than a temporary effect (like of GH50). At lower temperatures, the mechanisms is similar but delayed in time, suggesting a thermal activation of the effect. The mechanism of gate/drain leakage increase is strictly followed by the threshold voltage, which have shown a significant left shift in the first phase up to 400 mV and are then coming back toward the positive direction (see Figure 4.31 (d) and Figure 4.32 (d)); only after this point we have observed the sudden degradation of I_{DS} and g_m.

Therefore we can underline a strong correlation between the threshold voltage and drain/gate off-state leakage, characterised by a parabolic behaviour of both parameters activated by the stress temperature and a correlation in parameter's changes, since bigger leakage increase causes bigger left V_{th} shift.

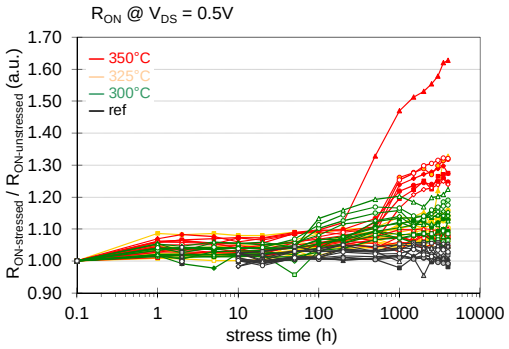
Passive component evaluated on FATFET samples and TLM structures are somehow confirming what observed in transistor characteristics. Leakage behaviour evaluated on large area Schottky devices have shown the same failure mode, but with a clear thermal activation and a sharp 2- to 3-orders of magnitude increase, much more severe than on transistor devices (see Figure 4.33). This difference suggests an area dependent phenomenon, while on small and large periphery devices the long gate perimeter could partially limit the effect. In the case of FATFET samples, it has been possible to extract the activation energy ($E_a = 2.12$ eV), and the estimated life-time for 10-times leakage increase at 230°C, which is equal to $2.56 \cdot 10^5$ hours, quite close to the 10^6 hours target time. Concerning the ohmic characteristic, results are showing again a thermally activated degradation of the contact resistance (as observed in GH50 devices), while the sheet resistance shows stable and consistent values at all temperatures.



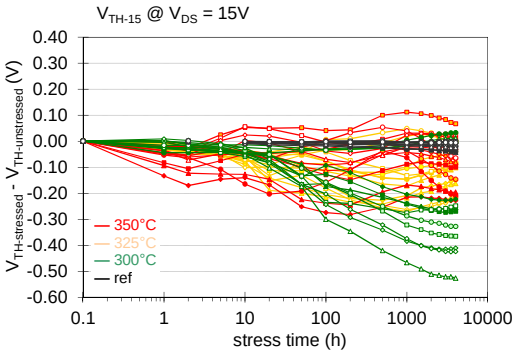
(a) I_{DS} variation.



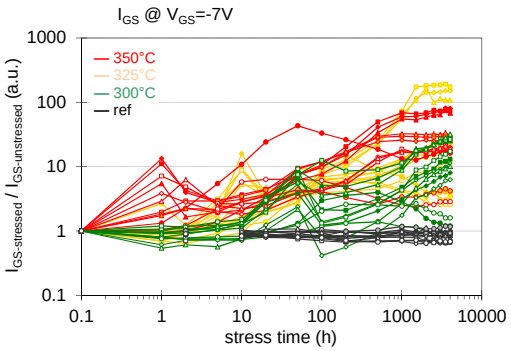
(b) g_m peak variation.



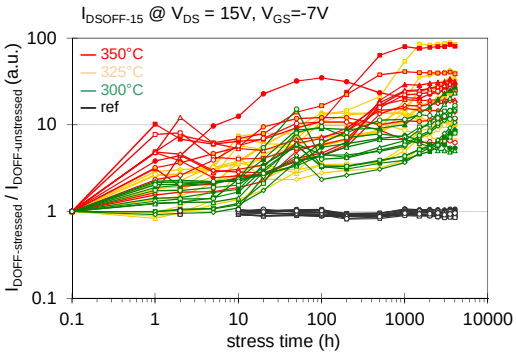
(c) R_{ON} variation.



(d) V_{th} variation.

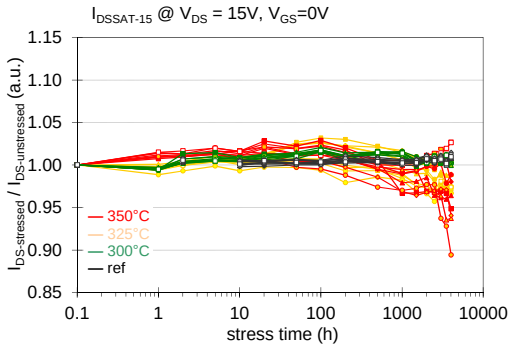


(e) I_{GS} diode variation.

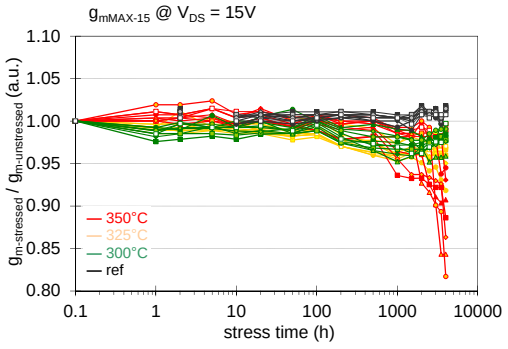


(f) I_{DS} leakage variation.

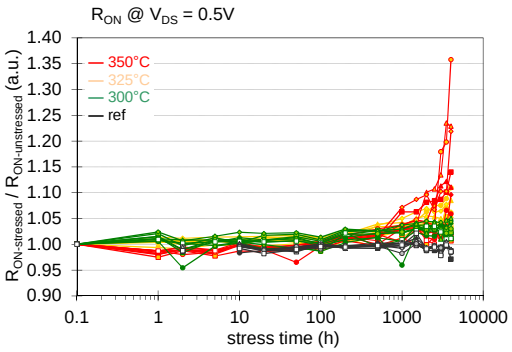
Figure 4.31: Variation of the main electrical parameters of 2x40 μm transistors submitted to storage tests. Red curves refer to device tested at $T_3 = 350°C$, yellow curves refer to device tested at $T_2 = 325°C$, green curves refer to device tested at $T_1 = 300°C$, while black curves refer to reference devices.



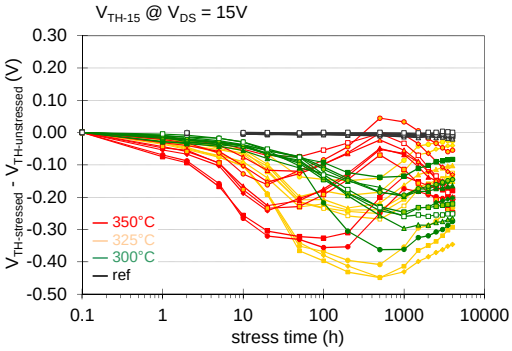
(a) I_{DS} variation.



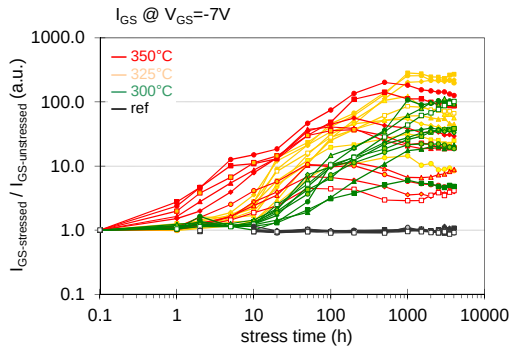
(b) g_m peak variation.



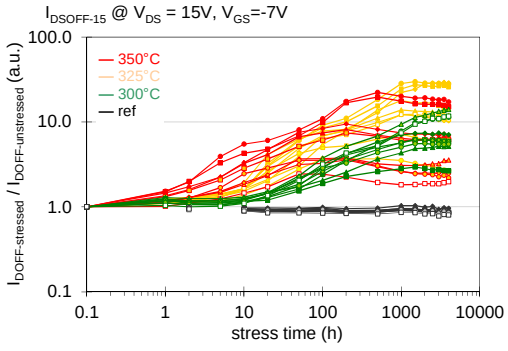
(c) R_{ON} variation.



(d) V_{th} variation.

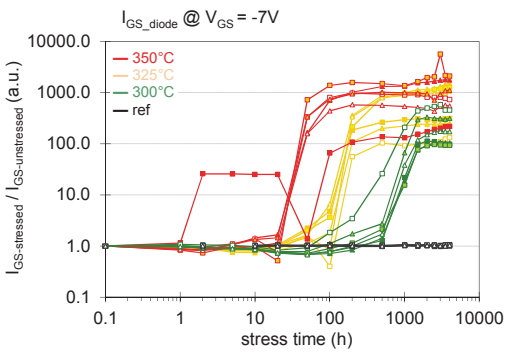


(e) I_{GS} diode variation.

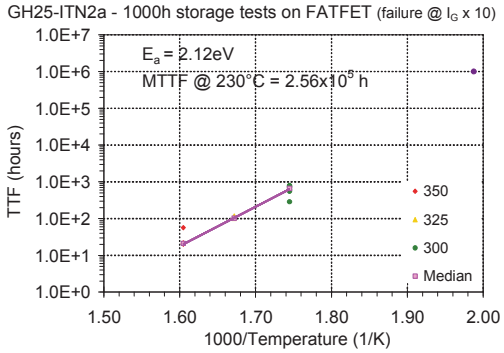


(f) I_{DS} leakage variation.

Figure 4.32: Variation of the main electrical parameters of 4x400 μm transistors submitted to storage tests. Red curves refer to device tested at $T_3 = 350°C$, yellow curves refer to device tested at $T_2 = 325°C$, green curves refer to device tested at $T_1 = 300°C$, while black curves refer to reference devices.

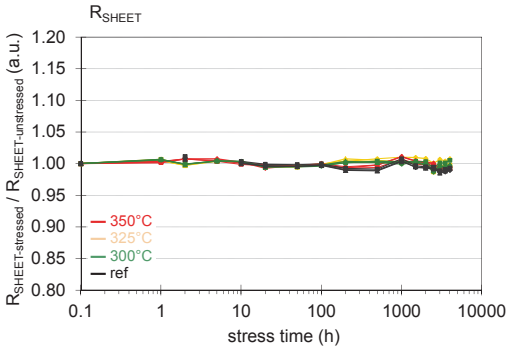


(a) Schottky diode leakage variation.

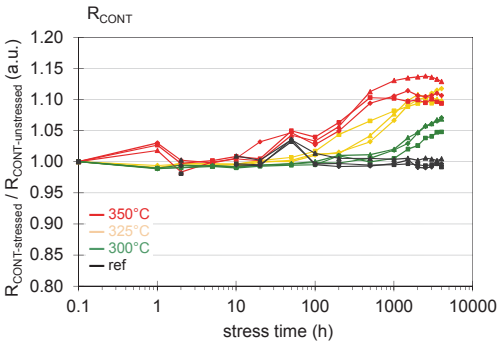


(b) Arrhenius plot of the failure mode.

Figure 4.33: (a) Variation of the diode leakage of FATFET samples submitted to storage test; (b) Arrhenius plot of the failure mode (10x leakage increase).



(a) Sheet resistance variation.



(b) Contact resistance variation.

Figure 4.34: Variation of the electrical parameters of TLM structure submitted to storage tests, in term of sheet and contact resistance. Red curves refer to device tested at $T_3 = 350°C$, yellow curves refer to device tested at $T_2 = 325°C$, green curves refer to device tested at $T_1 = 300°C$, while black curves refer to reference devices.

Summarizing the results obtained from three temperature storage tests in GH25 technology, we can underline the following degradation modes:

- Looking at the failure criteria on I_{DS} and g_m, some samples at 350°C have exhibited a sharp degradation of both I_{DS} and g_m values which in one case overcame the limit of the 20% decrease. At the moment, the failure mechanism somehow stopped after the first decrease and it has not been noticed at lower temperatures, but if the failure will start again, or if the first jump will already overcome the 20%, this failure mode must be carefully controlled.

- Concerning gate leakage, we have seen a common behaviour between small and large periphery devices, as well as on large area Schottky diodes, characterised by a gradual increase of both gate and drain leakage (much more sharp on large area diodes) activated by the stress temperature and dependent on the area of the Schottky gate under test. This mechanisms is not temporary as on GH50, but it seems to permanently affect the device performances with different effect depending on the presence of the field-plate structure. Activation energy obtained from large area diodes highlights a critical estimated life-time value ($\approx 2.56 \cdot 10^5$ hours) in the case of a 10-times increase of the leakage, which is slightly lower than the final target.

- Strong correlation between the threshold voltage and drain (and gate) off-state leakage, which have shown a significant negative V_{th} shift in the first phase up to 400 mV (big leakage increase) followed by a slow positive V_{th} shift (small leakage decrease). At lower temperatures, more severe left variation of the threshold voltage up to 500 mV, in particular on small samples (at 300°C).

- Results on passive structures have shown a thermally activated degradation of the contact resistance (as observed in GH50 devices), with 10-15% maximum increase of the R_{cont} at 350°C.

DC life-tests

Like for the GH50 technology, DC life-test activity consisted in a set of 4000-hours stress carried out at different accelerated bias conditions. Tested samples were DEC circuit based on a 8x125 μm transistor belonging to the GH25 technology, with the main layout details reported in Table 4.7 at pag. 73. All sample were of the DEC_V3F type, packaged on Schott package.

For this test we have chosen 4 bias-conditions, for investigating the effect of temperature on device degradation (from 250°C to 350°C of junction temperature) close to the normal operating point ($V_{DS} = 100$, $I_{DS} = 250\,mA/mm$), and the effect of the high-field ($V_{DS} = 60\,V$) in device reliability. Due to the limited statistics we avoided to use a fifth bias-point in high-current condition, since the lower V_{DS} and the quite comparable gate voltage would be less critical than the other bias-points concerning the device stability and reliability.

Base plate temperature has then been adjusted according to the R_{TH} formula that estimates the peak and the average junction temperature on DEC_V3F packaged samples by means of a calibrated 3D electro-thermal simulation:

$$R_{TH,T_{max}}(P_D, T_{BP}) = 3.45\,(K/W) + 0.517\,(K/W^2) \cdot P_D + 0.05083\,(1/W)\,T_{BP}$$

$$R_{TH,T_{avg}}(P_D, T_{BP}) = 3.24\,(K/W) + 0.528\,(K/W^2) \cdot P_D + 0.04640\,(1/W)\,T_{BP}$$

By means of these formulas, we have used the target temperatures (250, 300 and 350°C) and the defined bias conditions in order to obtain the correct base-plate temperature. As a result, in Table 4.9 and Figure 4.35 are reported the list of the 4 adopted bias-points which have been used for GH25 DC life-test activity.

Table 4.9: List of bias-points adopted for the long-term DC life-tests on GH25 DEC_V3F samples.

	I_{DS} (A/mm)	V_{DS} (V)	P_D (W)	T_{BP} (°C)	$R_{TH,T_{max}}$ (K/W)	$R_{TH,T_{avg}}$ (K/W)	T_{jmax} (°C)	T_{javg} (°C)	# dev
BP1	0.250	30	7.5	70	24.76	23.12	255.7	243.4	3
BP2	0.250	30	7.5	105	26.54	24.74	304.1	290.5	3
BP3	0.250	30	7.5	140	28.32	26.36	352.4	337.7	4
BP4	0.100	60	6.0	140	27.54	17.74	305.3	293.4	2

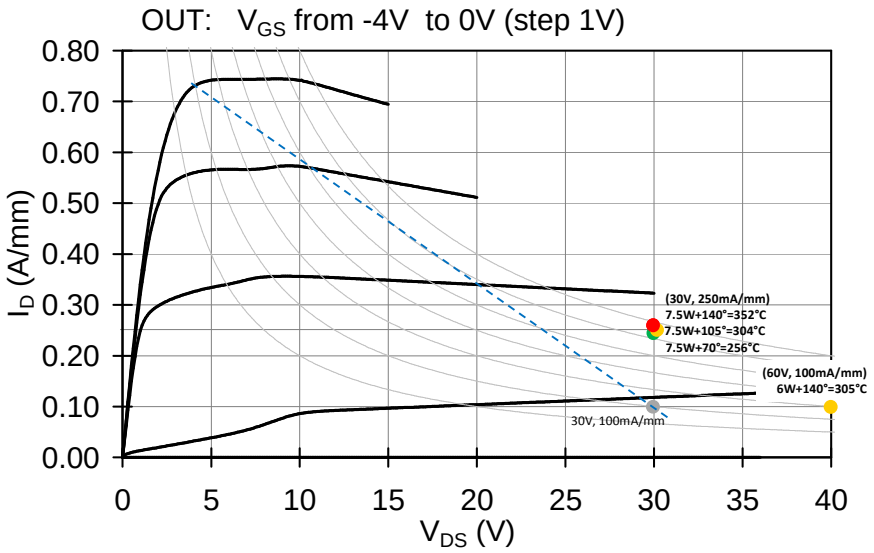
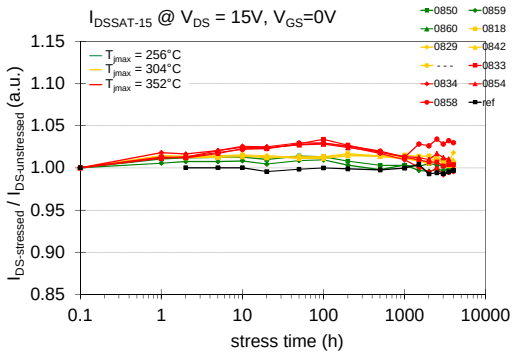


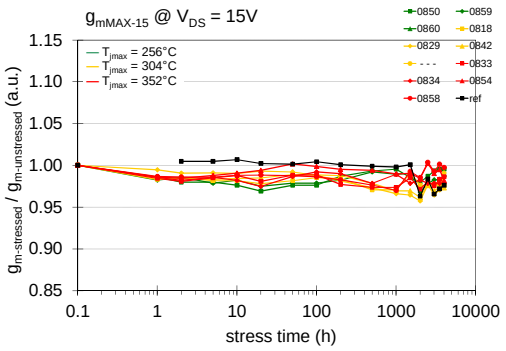
Figure 4.35: Schematic representation of the bias-points adopted for the long-term DC life tests on GH25 technology.

Figure 4.36 reports the results obtained on the BP1, BP2 and BP3 DC life-test operating conditions. First hours of test have shown really stable performance of GH25 DEC_V3F devices in term of drain current I_{DS} and transconductance peak g_{mMAX}, within 3-4% maximum degradation (see Figure 4.36 (a) and (b)). A small increase has only been noticed on the I_{DS}, caused by (i) a sudden reduction of the threshold voltage happening at the beginning of all life-tests (independently on the used bias-point) and to (ii) a further left shift of the V_{th} which gradually changed the pinch-off value of about -300 mV from 5 to 100-hours stress (see Figure 4.36 (d)). A small reduction of g_{mMAX} has compensated the large V_{th} left shift on I_{DS}. This threshold variation is strictly correlated with a gradual increase of the gate and drain leakages, which have shown the same kinetics. Final diode leakage have increased of about 10-times, while off-state gate and drain leakage have exhibited degradations below 10-times (see Figure 4.36 (e) and (f)). This mechanism is really similar to what observed in previously described storage tests, in which the leakage increase was thermally activated with a similar dynamics, and V_{th} shifted following the drain leakage increase; in this test the leakage increase and the V_{th} left shift seem to be thermally activated as well, since we are observing the same failure mode on BP2 at $T_j = 300°C$ (see yellow curves in Figure 4.36 (d) and (e)). Finally, the on-resistance is showing a more pronounced increase with respect to the g_{mMAX} peak, sign of a bigger degradation of the ohmic path in linear region, well in line with ohmic contact degradation observed in storage tests (see Figure 4.34 (b) and Figure 4.36 (c)).

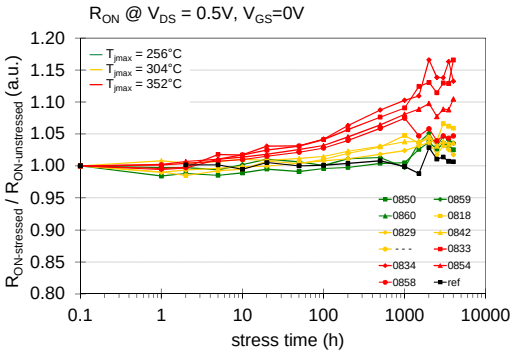
BP4 represents the bias-point in high-voltage conditions which purpose is testing the high-field robustness of GH25 DEC_V3F samples for long times and in high temperature conditions. Figure 4.37 reports some comparison graphs for BP2 and BP4 (at the same $T_j = 300°C$), where only the best and worst case are reported. The two bias points show a very similar behaviour in the parameter degradation; for bias point BP3 ($V_{DS} = 60\,V$, $I_D = 100\,mA$) there is a higher I_{DS} drop and V_{th} left shift in comparison to BP4 ($V_{DS} = 30\,V$, $I_D = 250\,mA$), indicating that the role of electric field in the degradation is secondary.



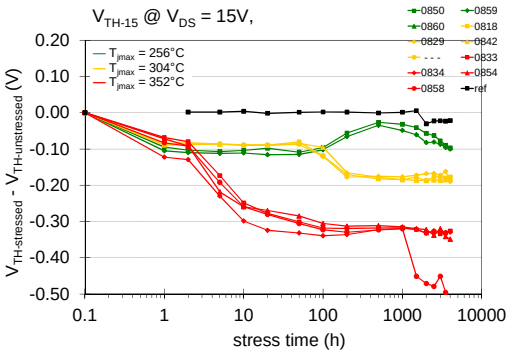
(a) I_{DS} variation.



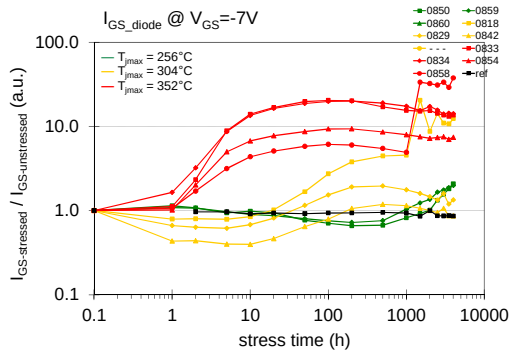
(b) g_m peak variation.



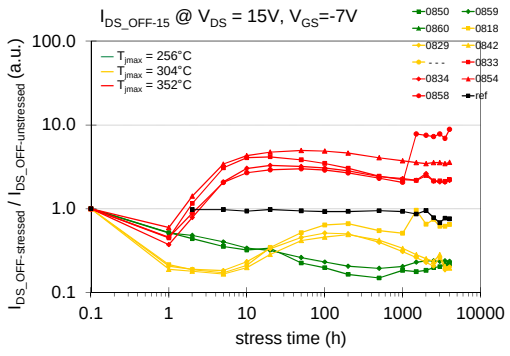
(c) R_{ON} variation.



(d) V_{th} variation.

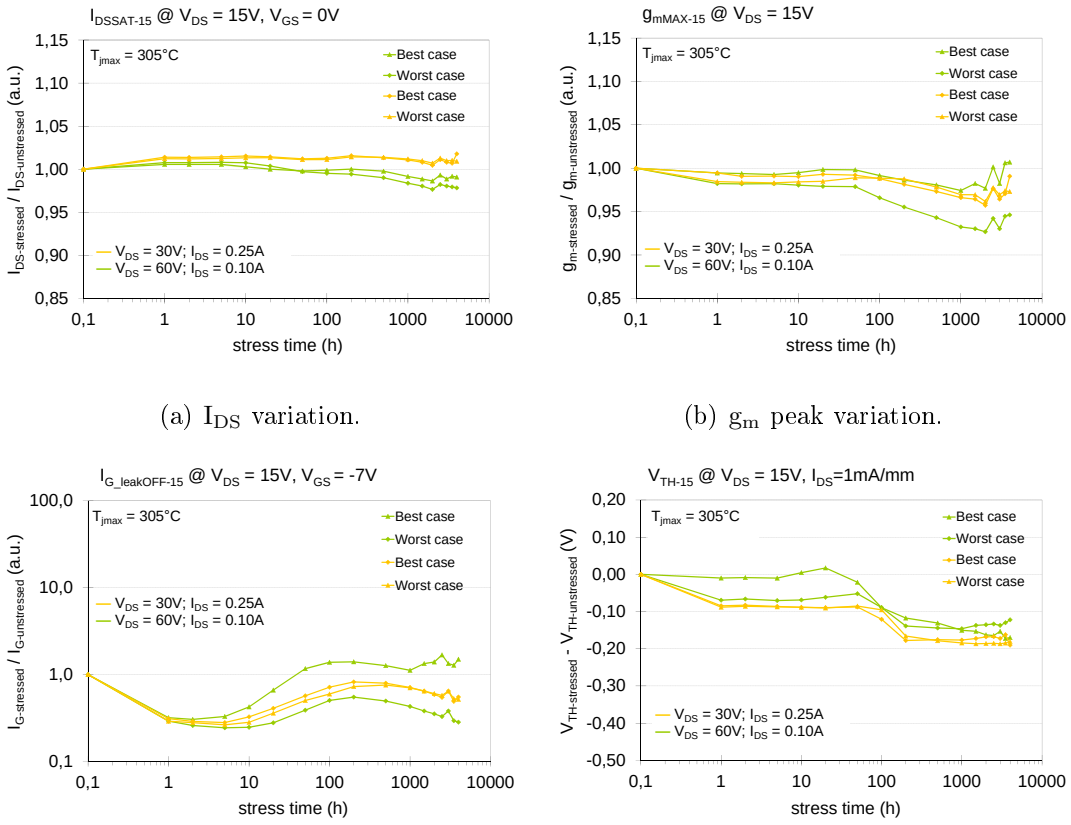


(e) I_{GS} diode variation.



(f) I_{DS} leakage variation.

Figure 4.36: Variation of the main electrical parameters of GH25 on-package samples submitted to BP1 (green curves), BP2 (yellow curves) and BP3 (red curves) life-test conditions. The black curves refer to the reference sample.



(a) I_{DS} variation.

(b) g_m peak variation.

(c) V_{th} variation.

(d) Off-state leakage I_g variation.

Figure 4.37: Best and worst case for the GH25 life-test (BP2, BP4).

In conclusion, the accelerated DC life-tests in GH25-ITN2a technology have shown a robust reliability behaviour of this technology on both high-temperature bias conditions and in high-voltage bias conditions. The main observed failure signatures are:

- a gradual increase of the gate and drain leakages, which have reached 10-times increase at 350°C, and with a smaller and slower increase at the bias-points at lower device temperature (300°C on BP2 and BP4). This mechanism seems to be thermally activated, with a kinetic very similar to leakage degradation in storage tests.

- a gradual left shift of the threshold voltage that starts at the same point of the leakage increase, and gradually changes the pinch-off value of about −300 mV from 5 to 100-hours stress. Even in this case, the small changes

of the V_{th} noticed at BP2 and BP4 ($T_j \approx 300°C$) suggest the thermal activation of this mechanism, well correlated with the leakage increase.

- small increase of the on-resistance at 350°C, which suggests a bigger degradation of the ohmic path in linear region, in line with ohmic contact degradation observed in storage tests.

RF life-tests

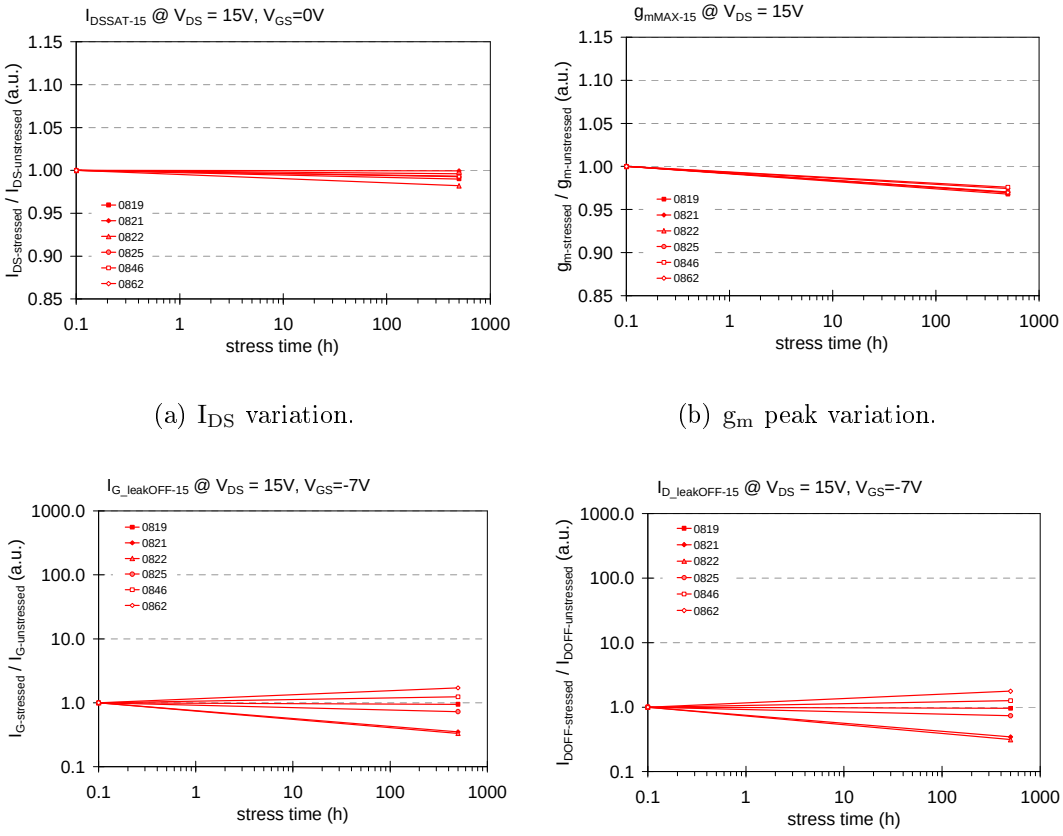
Six GH25-ITN2a amplifier devices in package have been submitted to the rf life-test activity using the *AARTS AccelRF* system. The test consisted in 500-hours stress carried out at the nominal bias condition ($V_{DS} = 30\,V$, $I_{DS} = 100\,mA/mm$, P_{in} @ peak PAE, $f = 9\,GHz$) in accelerated temperature conditions ($T_j = 325°C$). Tested samples were DEC_XBAND_MS_V1 amplifiers belonging to the GH25-ITN2a technology with the main layout details reported in Table 4.7 at pag. 73. Differently from the GH50 rf life test, this stress has been performed without any interruption, up to the end, at 500h. Before and after the stress, DC, pulsed and GC characterizations have been performed.

The GC characterization suite has been performed at the following conditions:

- $V_{DS} = 30\,V$; V_{GS0} @ $I_{DS} = 100\,mA/mm = 100\,mA$
- P_{in} from 8 dBm to 28 dBm (or $I_G < 10\,mA/mm$)
- $T_{BasePlate} = 50°C$

Results reported in Figure 4.38, Figure 4.39, and Figure 4.40 summarize the behaviour of the six GH25 samples submitted to 500-hours RF life-test at 325°C of junction temperature. In these diagrams we can observe the really improved stability of this technology during RF life-test, in comparison to the GH50 devices. Even if the junction temperature of this stress was 25°C lower, compared to the GH50 test, it cannot be the only reason of the observed differences.

The main DC performances of all GH25 samples show negligible variations (within 2-3% for both I_D and g_m). Even the leakage current levels are very stable, with any appreciable increase after the test (see Figure 4.38).



(a) I_{DS} variation.

(b) g_m peak variation.

(c) Off-state gate leakage variation.

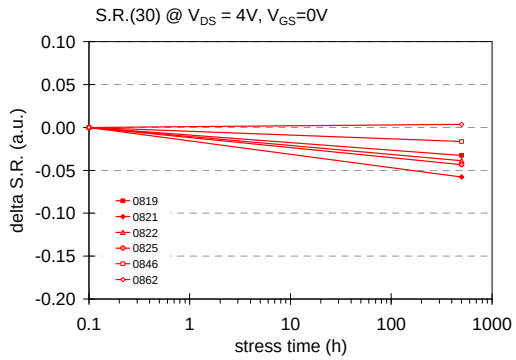
(d) Off-state drain leakage variation.

Figure 4.38: Variation of the main DC electrical parameters of GH25 samples submitted to RF life-test at $T_j = 325°C$.

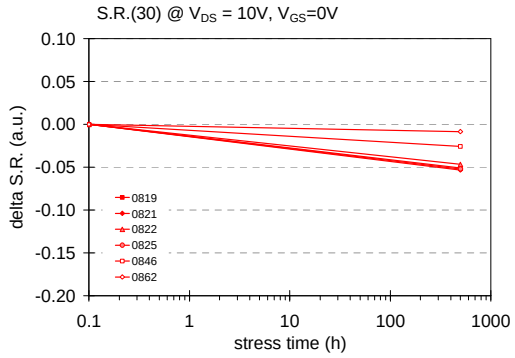
A small current collapse increase is observed (around +5%, see Figure 4.39 (a) and (b)), which explains a slight decrease (−0.5 dB) of rf power and gain. In Figure 4.39 (c) and (d) pulsed transconductance curves demonstrate that in this case, as it was for GH50 devices, the degradation is entirely due to a decrease of the transconductance peak, thus confirming that most degradation occurs in the high-field region between gate and drain, due to electric-field- or hot-electrons-induced crystal damage.

Concerning the RF performance the results are even better than for GH50 technology, because the failure criteria decrease of 1 dBm-P_{out} is not reached at the end of the stress; for this samples the average output power loss is only 0.5 dBm (see Figure 4.40 (a)). The PAE drop is limited to values between 1%

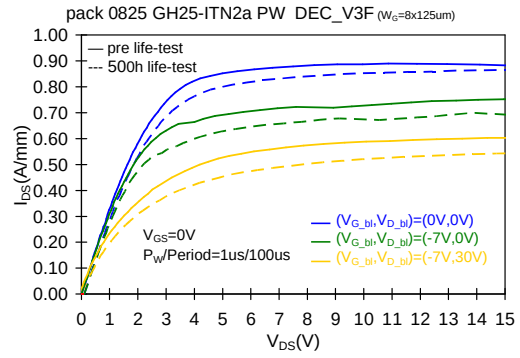
and 2.5% (in the GH50 was from 4% to 10%), while the small signal performance drop is only around $-0.1/-0.2\,\mathrm{dB}$. For this life-time test we have not extracted any activation energy, since with only two points (before and after the stress) is difficult to understand the real parameters trend, and it is possible to overestimate the device lifetime.



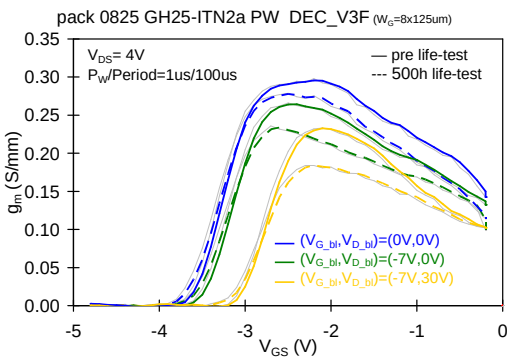
(a) S.R. in knee region at $V_{DS} = 4\,V$.



(b) S.R. in saturation region at $V_{DS} = 10\,V$.

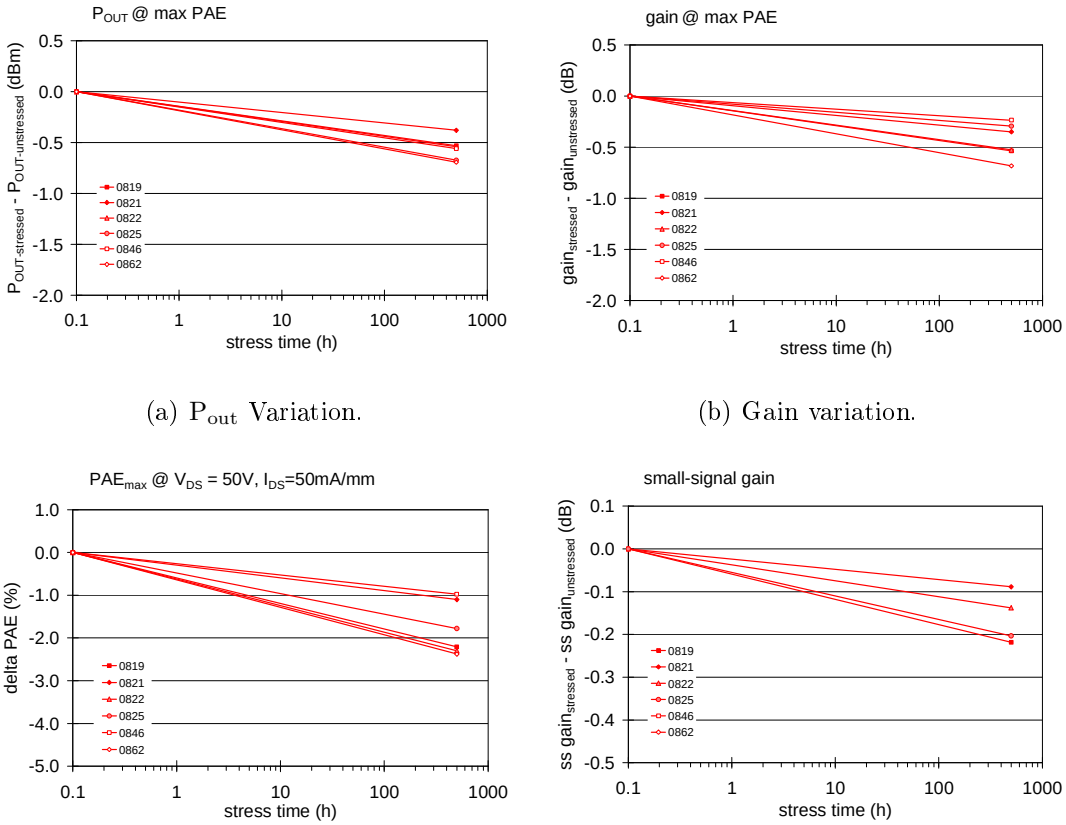


(c) Pulsed output before and after the stress.



(d) Pulsed g_m before and after the stress.

Figure 4.39: Variation of the main pulsed electrical parameters of GH25 samples submitted to RF life-test at $T_j = 325°C$ (a) and (b); pulsed characterization before and after the RF life-test on sample 0825 (c) and (d).



(a) P_{out} Variation.

(b) Gain variation.

(c) PAE variation.

(d) Small signal gain variation.

Figure 4.40: Variation of the main RF performances of the GH25 samples submitted to RF life-test at $T_j = 325°C$.

4.3 DLTS analisys

The *Deep Level Transient Spectroscopy* (DLTS) is a very powerful technique for analysing the effect of deep level traps on the device performance. In particular, with the drain current transient it is possible to follow the recovery of I_{DS} over several time decades, after a trapping condition. We started to perform DLTS analysis on the devices submitted to the thermal storage, looking for changes in the detrapping transient after the stress. Unfortunately it was impossible to perform the same analysis on the packaged devices submitted to the DC and RF life-test, since their current levels are too high for our measurements system. Then, we performed DLTS also on GH25 devices submitted to the short-term 24-h stress and to radiation test. We will see in the following how we can compare all the results from all this different kind of stresses.

For the device submitted to the thermal storage at $T_j = 350°C$ we measured small sample of both GH25-ITN2a and GH50-ITN3 technology ($W_g = 80\,\mu m$) with the same layout of the ones used for the short term stress (see details in Table 4.1 at pag. 50). The off-state trapping bias point was the same adopted for all the pulsed measurements ($V_G = -7\,V$, $V_{DS} = 30\,V$), while the on state bias point depends on the technology; in order to stay in the knee region and have similar current levels the chosen on-state bias points were ($V_G = 0\,V$, $V_{DS} = 3\,V$) for GH50 devices, and ($V_G = -1\,V$, $V_{DS} = 4\,V$) for GH25. For fitting the drain current trend, we adopted a stretched multiexponential method, in order to extract the characteristic times for each detrapping process.

Figure 4.41 reports the DLTS results on the GH50-ITN3 technology. The graphs labelled with "Storage RT" refer to the reference device, that has been stored at room temperature of 25°C. From the derivative plots of Figures 4.41 (b) and (c) we can obtain a lot of information; we can see three main processes: two emission (with positive derivative peak) and one capture (with negative derivative peak). After the storage it appears another slow trap with activation energy $E_a = 0.79\,eV$ (see the Arrhenius plot in Figure 4.41 (f)). Looking at the Arrhnius plots, we can notice that beside this additional trap there is an increase

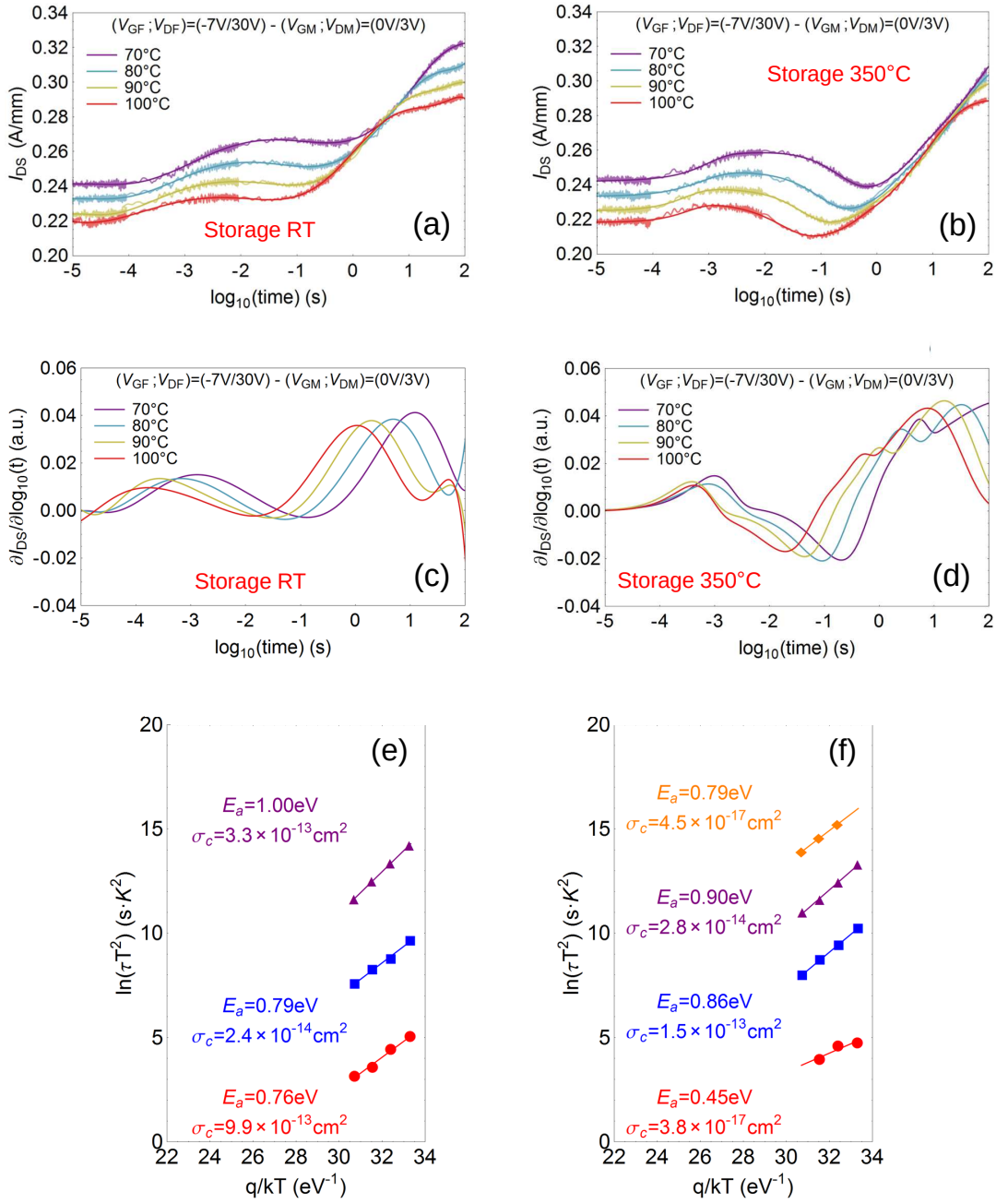


Figure 4.41: Drain current transient comparison for GH50 devices after thermal storage at RT and 350°C; (a) and (b) drain current transient; (c) and (d) derivative of the stretched exponential fit; (e) and (f) Arrhenis plots.

of the capture process with activation energy $E_a = 0.86\,eV$ after the stress; the derivative peak of this process increases, indicating an higher trap concentration. This trap could be ascribed to the presence of Carbon as impurity in the GaN layer [111]. The inaccuracy in the detection of the slower process after the stress ($E_a = 0.76\,eV$ before and $E_a = 0.45\,eV$ after) is due to the influence of the second process, that is higher after the stress.

In the case of the GH25 technology the situation is different. Starting from the plots of Figures 4.42 (a) and (b) we can observe a very different dynamics of the current recovery after the stress. In the derivative plots of Figures 4.42 (c) and (d) is clear how the peak of the faster trap seems to decrease, while the peak of the slower process increases. The extraction of the activation energies in this situation was more complicated, but we can observe that the trap with $E_a = 0.83\,eV$ appears only after the stress; it seems to be the same trap observed also in the GH50 samples after the test, so we start to think that it is related to the increase of some trap states concentration, induced by temperature.

In the case of the short term stress we performed the DLTS analysis only on a GH25-ITN2a device with the same geometry of the one measured in the storage test. The bias point of the 24-h DC stress was $V_G = 1\,V$, $V_{DS} = 60\,V$, while the on-state bias point for the detrapping was $V_G = 0\,V$, $V_{DS} = 6\,V$. Even though this bias point is already in saturation, and not in the knee region as in the storage case, we can observe some similarities. Figure 4.43 (a) reports the drain current recovery at $T = 40°C$ before and after the stress, and it is similar to what we have seen in the storage. In the DLTS spectrum of Figure 4.43 (b) the resemblances are more evident: there is an increase of the trap with $E_a = 1.00\,eV$ that coincide with the trap at $E_a = 1.05\,eV$ in Figure 4.42 (f). Furthermore, it appears another time the slow trap with $E_a = 0.77\,eV$, in line with the values found in the previous two cases.

The last DLTS measurement concerns the radiation test. As mentioned in the beginning of this chapter, this project covered a wide spread of different activities that are not reported here, and one of them is the radiation tests. Within radi-

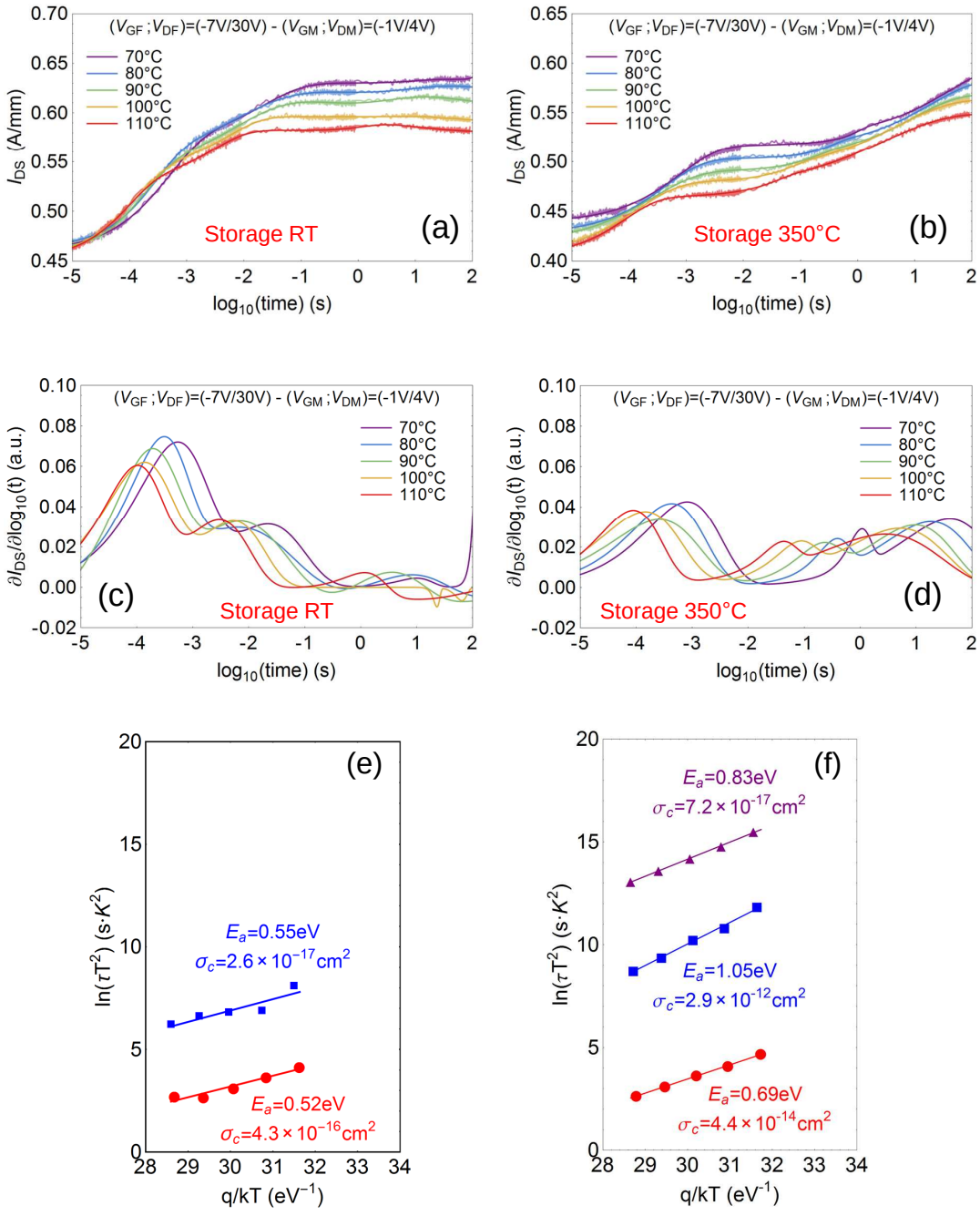


Figure 4.42: Drain current transient comparison for GH25 devices after thermal storage at RT and 350°C; (a) and (b) drain current transient; (c) and (d) derivative of the stretched exponential fit; (e) and (f) Arrhenis plots.

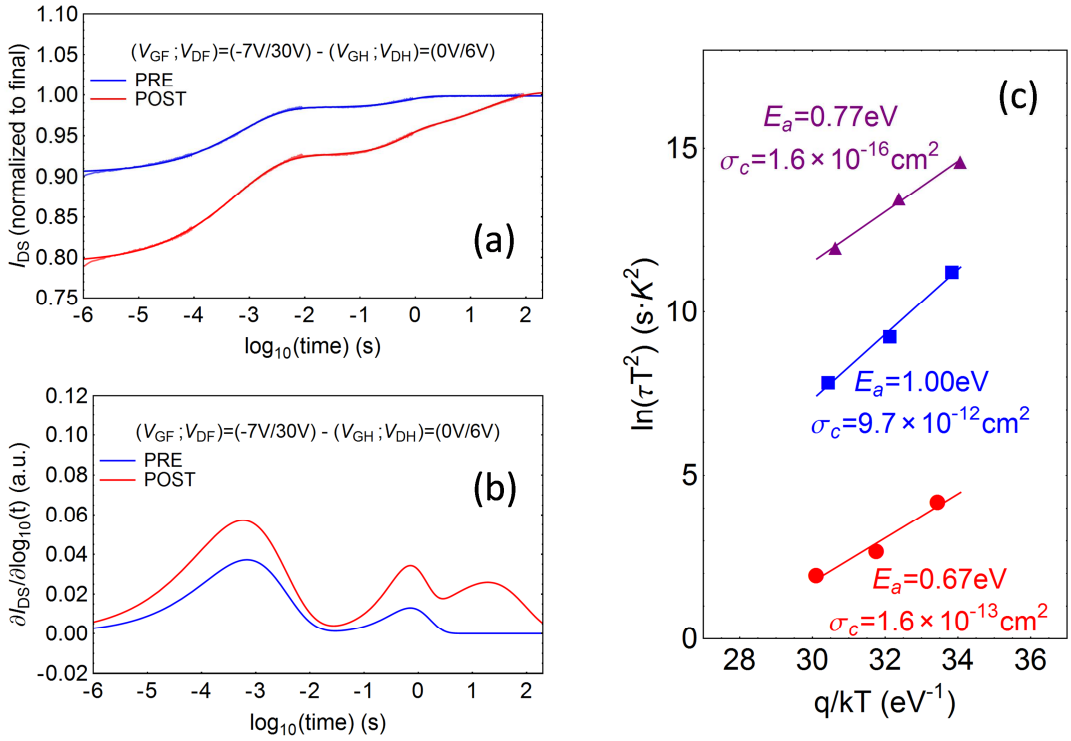


Figure 4.43: Current-DLTS measurements performed at T = 40°C on GH25-ITN2a technology before and after the 24-h DC stress (a), derivative of the stretched exponential fit, highlighting deep-levels emission processes (b), and Arrhenius plot with the correspondent activation energies of the traps (c).

ation activity we performed both displacement damage and single-event effects tests. The drain current transient analysis has been performed before and after a displacement test with proton irradiation. This results have been published at ESREF 2014 conference and on Microelectronics Reliability [112]. The tested device were the small samples ($W_g = 80\,\mu m$) of the GH25-ITN2a technology, like the one considered for the storage test; the fluence level of the proton irradiation was 10^{14} p/cm^2. The on-state bias point adopted for the current recovery transient was $V_G = -2\,V$, $V_{DS} = 3\,V$; even though it is not the same as the previous ones there are not so many differences since we are still in the knee region.

Figure 4.44 reports the results of the drain current transient measurements before and after the radiation test. Looking at the derivative of the stretched exponential function used to fit the experimental data (see Figure 4.44 (b)), an

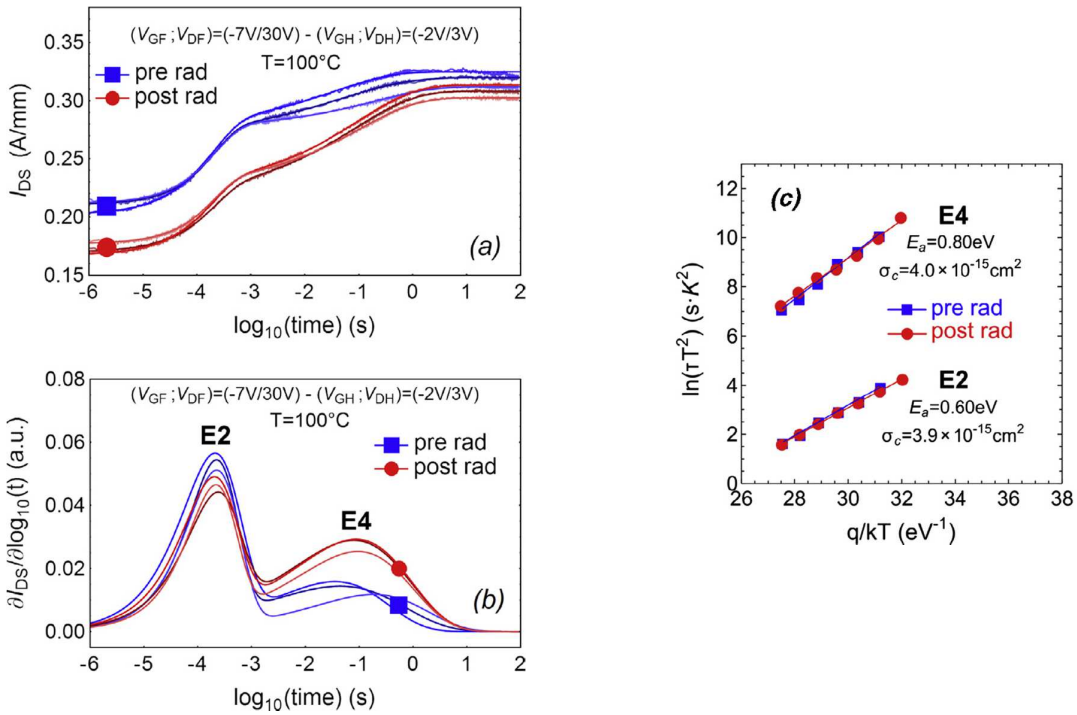


Figure 4.44: (a) Variation of the drain-current transient measurements at T = 100°C before and after the radiation test; (b) derivative of the stretched exponential fit of the corresponding curves; (c) Arrhenius plot of the signatures detected.

increase of the second trap signature E4 is clearly visible, followed by a limited reduction of the first signature E2. This effect is exactly the same observed for both the short-term and storage tests on the same technology, indicating a possible common origin of the changes in the trap spectra. The only difference is that after the radiation test the additional slow trap with $E_a \approx 0.8\,eV$ is not observed.

The small reduction of E2 signature does not seem to be a direct consequence of the induced displacement damage, but could be mainly caused by a partial emission of trapped electrons from E2 defect to E4 defect. This is in line with the DLTS spectra for the short-term stress and storage test (see Figure 4.43 (b) and Figure 4.42 (b)). A possible explanation is that the increased trapping force of E4 level can move some electrons from E2 to E4, causing the small reduction of the

first trap signature, as reported by *Bisi et al.* [65]. Concerning the physical nature of the defects, while E2 is a level often ascribed to a native defect existent in GaN materials, for the signature E4 there are still some discrepancies between what it is typically reported on displacement simulations and the observed signatures of the traps. Results from DLTS analysis on other irradiated samples [113][114][115], together with the results reported here, suggest the presence of a deep electron trap placed 0.80 eV from the conduction band as the responsible for the slower (and enhanced after radiation) current transient.

Even though we was not able to perform the DLTS analysis on the devices after the RF-stress, we can find some information in the literature. Recently, *Arehart et al.* [116] reported the correlation between rf degradation and the modification of the DLTS spectra. Only devices with output power degradation higher than 1 dB show significant changes in the trap profile. The difference from our analysis is that they report an higher increase after the RF-stress of the faster trap with $E_a = 0.57\,eV$ (that correspond to our E2 level), in comparison to the slower one with $E_a = 0.75\,eV$ (that correspond to our E4 level).

In conclusion, we can say that our analysis demonstrates for the first time a correlation between changes in the DLTS trap spectra after very different stress-tests like proton irradiation, thermal storage, and DC-stress. While in literature these results are reported only separately, in our original work we show how they can appear on the same technology in different stress conditions. This could be an indication that the difference in the drain current transient before and after a stress could be related to the concentration increase of some native GaN-defect located in the GaN bulk, even though we have still not enough information to speculate more about the origin of these defects.

4.4 Conclusions

The reliability investigations carried out in GH50 and GH25 technologies have shown the really stable behaviour of both technologies in high-temperature and high-power conditions, from short to long-time of stress, making the identification of the failure modes and mechanisms really difficult for the extreme bias- and time-conditions requested to gain a not negligible damage of the device behaviour. Nevertheless, some conclusions can be done from the large amount of performed tests:

For GH50 technology:

- All reliability tests have highlighted the really stable behaviour of GH50-ITN3 technology, which has shown a 10% maximum degradation of main performances (I_{DS}, g_m) in all testing conditions. Preliminary life-time evaluation based on long-term storage- and DC life-tests clearly assess the stability of this technology for 20 years operation at 230°C, because of estimated life-times higher than 10^9 hours at 230°C of T_j in the worst case condition. Based on this results, 20% decrease of I_{DS} seems to be too low as failure criteria, due to the large error we can make for extrapolating the 20% drain current decrease (not reached by the stress), while 10% I_{DS} decrease will ensure more reliable results, providing a MTTF still within the target life-time.

- Only RF life-tests seem to not respect this evaluation, since the gate leakage degradation happening during the first step of operation at really higher temperature can bring the output performances (P_{out}) out of the limit in less than 500-hours. At the moment, we do not know the activation energy of this phenomenon, or if it is triggered only at temperatures close to 350°C, but using the activation energy extracted from DC life-tests, estimated MTTF is higher than 10^7 hours.

- From short-term tests we have observed that the high electric-field alone

is not sufficient to cause significant damages on this technology, while the simultaneous presence of really high temperatures (higher than 250°C) and high-electric field can enhance device degradation. Consequently, junction temperatures lower than 300°C are too low for causing a significant damage on tested samples in a reasonable short period of time, allowing this technology to work for relatively long times (24-hours) even close to the breakdown limits at this temperature conditions. This result confirms the really limited degradation reached during on-wafer tests, where despite the extreme dissipated power, the low thermal resistance makes final junction temperature below 250°C. In this case, the use of large periphery devices (which provides higher R_{TH} values) or of on-package long-term life-tests are the only feasible experiments which can provide significant degradations of the devices under test, and therefore suitable to understand the failure modes and mechanism behind that.

- For temperatures higher than 300°C, long-term tests highlighted a common degradation mode happening on the leakage current, which causes a 1 to 2 orders of magnitude increase of the gate leakage starting from different stress times activated by the device temperature, but that completely recovers in the following hours. A deep investigation of the Schottky diode behaviour have underlined a (i) clear left shift of the diode threshold caused by a decrease of the Schottky barrier height (about 0.3/0.4 eV) during the first hour, followed by (ii) a complete recovery of both elements in 20-50 hours, and (iii) a final long-term gradual shift of the curve in the Richardson plot. At the moment it is difficult to correlate these electrical parameter changes with the corresponding physical mechanisms, like gate sinking or gate-metal interdiffusion, since a not homogenous phenomenon on the gate surface affected by some strain effect at the gate edges can make the analysis much more complicated.

- Among samples tested at the same junction temperature, a higher leakage content seems to influence the drain current with a faster degradation.

In fact, the permanent leakage increase observed during the first steps of stress on many samples submitted to DC and RF life-tests suggests that a sudden failure of the gate terminal, happening at the beginning of the stress, can lead to a faster performances degradation. Nevertheless, the final degradation stayed within the failure limits after 4000-hours of test.

- Concerning dynamic and RF performances, results underline a clear correlation among gate leakage, dynamic performance and RF large-signal characteristics, with a higher degradation on samples which experienced the higher gate leakage degradation and the following higher dynamic performance reduction (0.6-0.8 dB decrease of P_{out} and 40-50% decrease of dynamic transconductance).

From the collected evidences, we can suggest a burn-in preliminary screening procedure able to stabilise the device performances and to put into evidence the sample characterized by a shorter life-time. 24-50 hours at 300°C of T_j in biased conditions (like BP2 DC bias-point or the RF bias-point) will be sufficient to separate the two device's populations in a short time. By looking at the I_{DS-OFF} as the target parameter (≈10x increase) we can easily separate those characterised by a normal performance degradation (temporary increase/decrease of the leakage), from those characterised by a faster DC and RF performance (early large diode degradation around 10-100 times increase). However, if we want to deeper investigate the failure mechanism the short-term stress are not able to show most of the degradation modes observed during the long-term tests. Thus, in order to estimate the device life-time and understand the failure modes the long-term stress analysis is the only way to follow.

For GH25 technology:

- All reliability tests performed on the new ITN2a iteration of the GH25 process have highlighted the really stable behaviour of this technology, which has shown outstanding results concerning high-voltage and high-

temperature stability (degradation below 5%), as well as stable device performances in long-term tests which are still far from any failure criteria.

- During short-term tests we have deeply investigated the difference between the old ITN2 technology and the new ITN2a technology, highlighting the significant improvement of the new one in term of performances and robustness. In the ITN2 technology, we have observed the presence of two failure mechanisms activated by temperature, while the new ITN2a technology have only shown a 5% maximum degradation of drain current and transconductance at an estimated junction temperature T_j close to 400°C, ruling out the critical failure mechanism observed in ITN2.

- Results from the long-term tests are confirming the stability of this technology on long-time scale, even at really high junction temperatures. The increase of the gate leakage observed in high temperature long tests, from small periphery to FATFET structures, are quite in line with preliminary result gathered from short-tests, which states that temperatures higher than 320°C cause an increase of gate leakage. Long-term tests indicate (i) the permanent nature of the gradual increase of both gate and drain leakage, (ii) the dependence of the failure mode to the stress temperature rather than to the stress voltage and (iii) the dependence on the area of the tested sample. Activation energy extracted for 10-times increase of the leakage, highlights an estimated life-time value of $2.56 \cdot 10^5$ hours, which is slightly lower than the final target. Nevertheless, the limited increase of the gate leakage and the stable device performances (I_{DS} and g_m) during this phase suggest a limited influence of this failure mode on the long-term reliability behaviour.

- Strong correlation between the threshold voltage and off-state leakages has been found in both storage and DC life-tests, characterized by (i) a significant negative V_{th} shift up to 400 mV accelerated by device temperature, correlated with the leakage increase, (ii) followed by a slow positive shift

when the leakage stops increasing. The failure mode described by the negative V_{th} shift can be the enhanced version of the *signature 2* effect observed in ITN2a devices in medium-term tests, with a clear thermal activation.

- Concerning the failure criteria on I_{DS} and g_m, at the moment we can not provide a clear estimation of the device life-time, since tested samples have only exhibited a sharp degradation of both I_{DS} and g_m values which in one case overcame the failure limit. At the moment, the failure mode is not characterized by a gradual performance variation, but on some sudden changes of the drain current, thus requesting few other steps of stress in order to better evaluate the involved failure mechanism.

Concluding, at the moment it is not completely clear which are the physical mechanisms beyond the failure modes observed in GH25-ITN2a devices, but results suggest the decisive role of the gate contact on device reliability, as on GH50 technology. In fact, gate metal diffusion or intermixing could explain both the threshold voltage variations and the leakage increase.

Chapter 5

Power devices

In the following they will be summarized the main results obtained in the research activities on the GaN-based power HEMTs. The chapter is divided in two sections: the first is about MIS-HEMTs, while the second concerns the p-GaN technology. This two technologies have been developed for the same applicative target in power systems, like DC-DC converters. They have two completely different design approaches: the MIS-HEMTs are normally-on devices while the p-GaN are normally-off. So, the ways to reach the operative targets are different, even though some problems to solve are the same.

5.1 GaN-based MIS HEMTs

In this part we will focus on the analysis of power MIS-HEMTs technology. The research activity consist in a collaboration with *ON Semiconductor*; our role is to give them a feedback on their improvements during the technology development. The analysed devices are all 600 V–rated MIS HEMTs grown on a p-type Si-conductive substrate. Over the Silicon is grown a C-doped GaN buffer, a u.i.d GaN channel layer, an $Al_{0.25}Ga_{0.75}N$ barrier and MIS structure, using *in situ* grown SiN as gate dielectric. For all the characterizations we used small devices with gate width $W_G = 0.2\,mm$. The devices have both a source and gate field plate [33]. In the following we will try to summarize the most relevant results

obtained during the three-years activity.

5.1.1 The dynamic on-resistance

The power devices that work in switching converters, during the on-state conductive phase suffer of conductance losses . Thus, it is fundamental to keep the on-resistance R_{ON} as lower as possible. However, there is a trade-off between the on-resistance and the device breakdown voltage, and it is necessary to optimize the device layout. In the on-state switching phase the drain voltage V_{DS} reaches values around 1 V and the transistor works in linear region, acting like a resistor. We can measure the value of R_{ON} from the I-V characteristic in linear region. Differently from the RF devices, we do not need to characterize the transistor in saturation, and all the analysis will be performed in linear region. However, measuring the on-resistance in DC is not enough since the transistor has to work in switching conditions from off- to on-state. Thus, we need to analyse the dynamic R_{ON}, i.e. the value of on-resistance during the switching conditions. When the GaN-based HEMT goes in off state, with the gate in pinch-off and a high bias applied to the drain, trapping phenomena take place; when the device is turned on again we can see an effect similar to the current collapse in RF devices. Since in this case we are looking at the on-resistance we will observe a dynamic-R_{ON} increase, i.e. the drop of the slope of the I-V output characteristic in linear region.

It is possible to measure the dynamic-R_{ON} by means of pulsed measurements. The standard pulsed conditions are $T_{ON} = 1\,\mu s$, $T_{OFF} = 99\,\mu s$, for drain voltages up to 200 V. In case we need to reach the 600 V level the pulsed conditions are limited to $T_{ON} = 20\,\mu s$, $T_{OFF} = 2\,ms$.

We carried out one of the first analysis to compare the performances of three of the first GaN-based HEMT generations in term of dynamic-R_{ON} [69]. During the preliminary dynamic-R_{ON} analysis we observed that increasing the temperature the pulsed performances was dramatically dropping. This effect was something never reported for RF devices and we start to investigate the possible reason of this effect.

For a first evaluation of the temperature-dependent dynamic-R_{ON} increase we carried out I-V pulsed measurements with two different quiescent bias points: (i) zero bias $(V_{GS}, V_{DS}) = (0\,V, 0\,V)$, (ii) off-state $(V_{GS}, V_{DS}) = (-10\,V, 100\,V)$. Figure 5.1 (a) reports the pulsed measurements carried out at the temperatures of 30°C (red curves) and 140°C (blue curves), on the first device generation. We can notice that while at 30°C the dynamic-R_{ON} is almost negligible, at 140°C the situation becomes serious, with a huge drop of R_{ON}. In Figure 5.1 (b) is reported the temperature trend of the percentage dynamic-R_{ON} increase, that indicates the existence of a thermally activate process. In order to better understand the dynamic of this process we decided to perform further trapping measurements.

During the I-V pulsed measurements the dynamic-R_{ON} increase is acquired only for a trapping time that is fixed by the off-state pulse duration, that in this case is 99 μs. In this way the dynamic of the trapping process get lost. Unlike RF devices, the trapping time of power transistors can be in the order of 10-100 s and it would be interesting to follow its dynamic. In most of the drain current transients for DLTS analysis the trend of the current is acquired after a

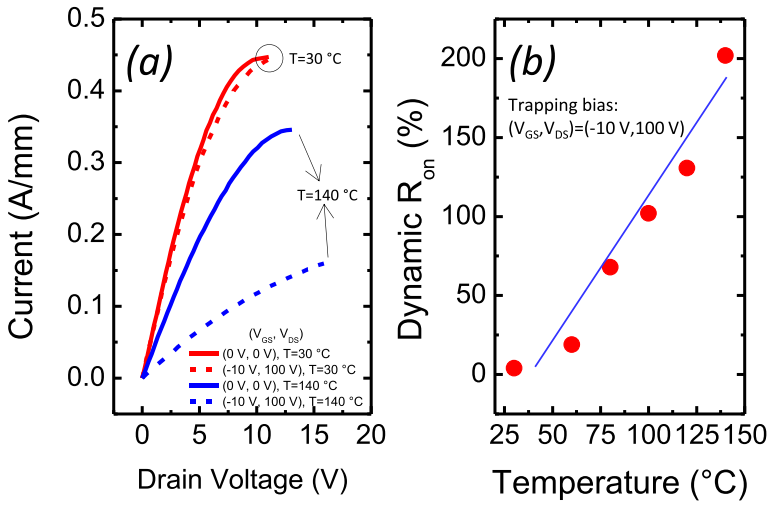


Figure 5.1: (a) Pulsed I-V measurements with zero bias and trapping quiescent points at the temperatures of 30°C and 140°C; (b) Dependence of dynamic-R_{ON} on Temperature.

period of trapping. Instead, we would like to follow the trend of the trapping phase too. For this purpose we developed an experimental procedure: we keep the device in the trapping condition for 1000 s; each second, the R_{ON} variation is evaluated switching the device in on-state ($V_{GS}, = 0\,V, V_{DS} = 1\,V$) by means of short pulses. The pulse duration is around 50 ms, much more shorter than the typical detrapping time of the defects (in the order of 1-10 s). At the end of this measurements it is possible to follow even the detrapping, as in a classical drain current transient, using for the next 1000 s the zero bias condition ($V_{GS} = 0\,V$, $V_{DS} = 0\,V$).

In Figure 5.2 (a) is reported a trapping measurements in off-state condition ($V_{GS}, = -10\,V, V_{DS} = 100\,V$) at different temperatures with the stretched multi-

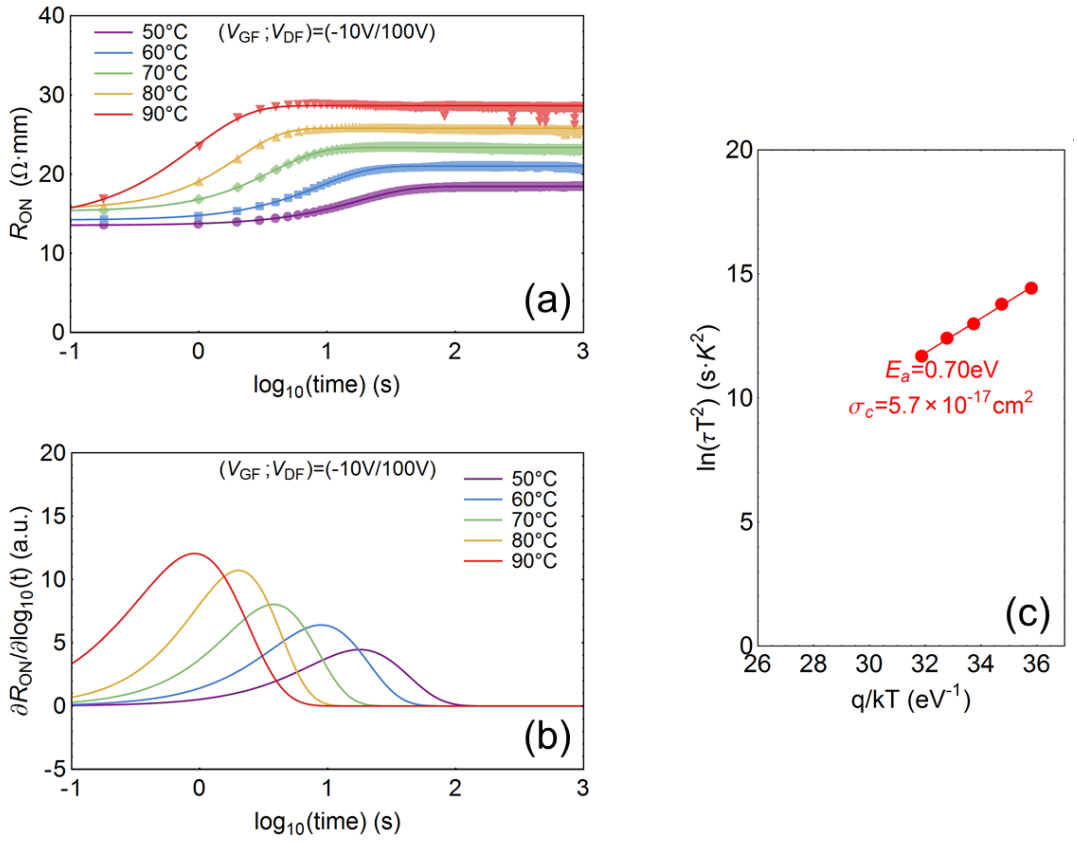


Figure 5.2: (a) Trapping measurement in off-state ($V_{GS}, = -10\,V, V_{DS} = 100\,V$); (b) derivative of the stretched exponential fit; (c) Arrhenius plot.

exponential fit; in Figure 5.2 (b) we can see the derivative of the fitting, while in Figure 5.2 (c) the relative Arrhenius plot. It is possible to see how the process is thermally activated with an activation energy $E_a = 0.70\,eV$. Unlike the detrapping, the estimated activation energy is not related to the distance of the trap state from the conduction (or the valence) band. The value of E_a for the trapping is instead related to the number of carriers, that increases with temperature in steady-stead condition, depending on the position of the Fermi-level. However, if some leakage current is involved, it can provide the carrier to fill the traps, and the resulting activation energy is related to the leakage [68].

In Figure 5.3 we can see an example of a detrapping measurements after the

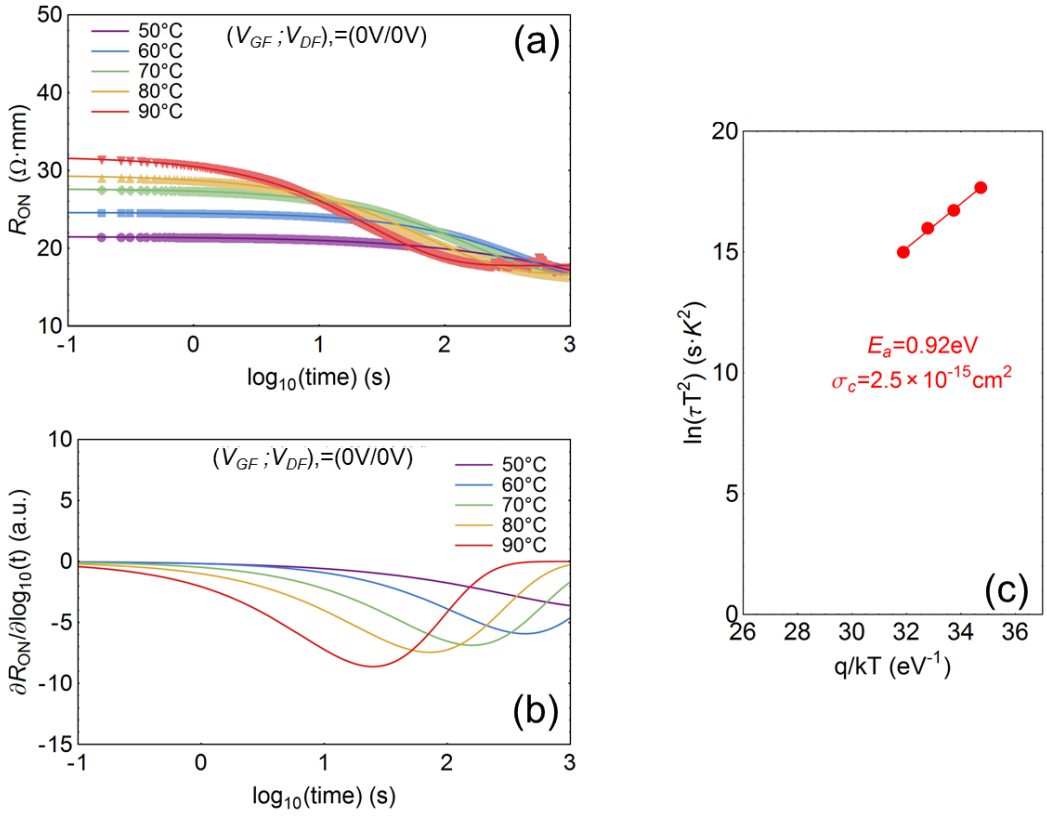


Figure 5.3: (a) Detrapping measurement after 1000 s of trapping in off-state bias ($V_{GS}, = -10\,V, V_{DS} = 100\,V$); (b) Derivative of the stretched exponential fit; (c) Arrhenius plot.

1000 s of trapping in off-state condition ($V_{GS}, = -10\,V, V_{DS} = 100\,V$). In the graph of Figure 5.3 (a) we can see that after 1000 s there is a full recovery of R_{ON}, at least for temperature higher than 70°C; at lower temperatures the recovery is slower, but it reaches anyway the starting value. This demonstrates that the dynamic-R_{ON} originates only from trapping phenomena, while there is no permanent device degradation. Off course, before to increase the temperature and perform the next trapping measurements we need to have a full detrapping, for starting always at the same condition, without residual trapping. The detrapping measurements are like the classical drain current transient with two main differences: (i) while in the DCT the acquisition of the current is continuous, in the detrapping measurements the current is measured only every second, with a short pulse, during the rest condition ($V_{GS}, = 0\,V, V_{DS} = 0\,V$); (ii) the DCT can span a time range from 1 μs up to 100 s, while the detrapping measurements is limited in the 0.1–1000 s range. However, the obtained results of the two measurement systems are comparable, even though they can differently highlight processes with different time constants.

Comparing the trapping and detrapping measurements we can notice two dynamics with different time constants: 2 s for the trapping and around 90 s for detrapping, both at 80°C (see Figures 5.2 (b) and 5.3 (b)). Furthermore, we can see in the Arrhenius plot of Figure 5.3 (c) an activation energy $E_a = 0.92\,eV$ that could be associated to the presence of Carbon-related defects in GaN [117]. For this detrapping measurement the activation energy could be related to the distance of the deep-level from the conduction (or valence) band.

However, this analysis is more focused on the trapping phase. During the preliminary routine characterization we detected in our samples a not negligible drain-to-substrate current, thus we decided to investigate if it could play some role in the R_{ON} increase. For this reason we need to find a way to separate the effects of surface- and buffer- related trapping, since in the off- state condition we could have injection of electrons to the drain both from the gate and from the bulk [118]. Thus, we decided to perform the trapping measurements in three

different bias points:

1. Off-state bias ($V_{GS}, = -10\,V$, $V_{DS} = 100\,V, V_B = 0\,V$), which induces both lateral trapping (injection of the electrons at the gate-drain surface) and vertical trapping (injection of electrons from the substrate), see Figure 5.4 (a);

2. backgating condition ($V_{GS}, = 0\,V, V_{DS} = 0\,V, V_B = -100\,V$), which induces pure vertical trapping (high vertical field between drain and substrate), with negligible surface trapping (no bias between gate and drain, see Figure 5.4 (b);

3. Off-state condition with positive substrate bias ($V_{GS}, = -10\,V, V_{DS} = 100\,V$, $V_B = 100\,V$), which induces pure lateral trapping (in the gate-drain surface, due to the high lateral field), with negligible vertical trapping (the drain-bulk bias is zero), see Figure 5.4 (c).

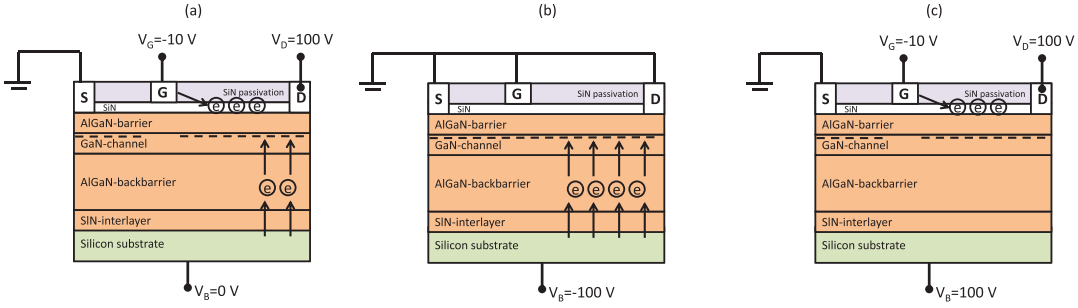
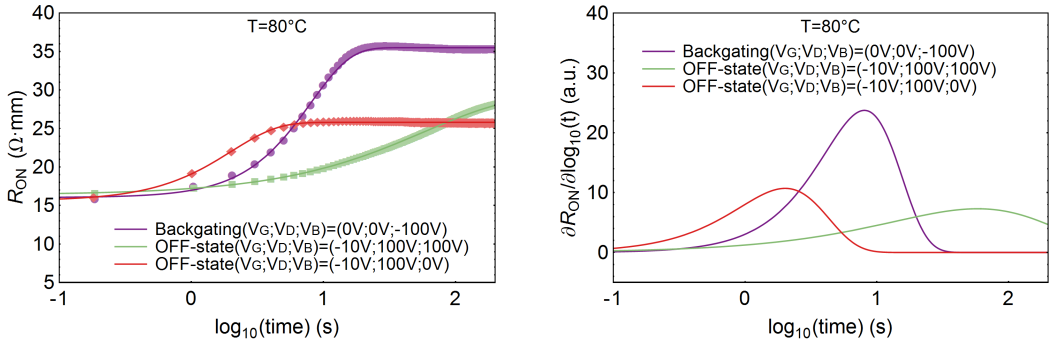


Figure 5.4: Schematic of the bias conditions used for separately investigating the surface- and buffer-related trapping processes. (a) Typical off-state condition, which can induce the trapping of electrons both at the surface and in the buffer; (b) backgating condition, in which trapping mostly occurs in the buffer, without any significant surface effect; (c) positive substrate (off-state) operation, which induces a significant surface trapping, while preventing any vertical effect.

In Figure 5.5 we can see that all the trapping bias points induce a significant R_{ON} increase at 80°C. The off-state condition with positive bias (pure lateral trapping, Figure 5.4 (c)) induces a slow R_{ON} transient with a stretched exponential behaviour, i.e. of the form $\sim \exp(-t/\tau)^{\beta}$, with $\beta = 0.66$. In the case of an ideal exponential kinetics the value of the stretching parameter is $\beta = 1$, while for values lower than 1 the shape of the transient is stretched along the time axis. The observed stretched behaviour, with relatively long time constant (in the range of 80-100 s at 80°C) are typical signatures of surface trapping [119]; the trapping process is slowed by the limited amount of surface states and by the repulsive effect of the already trapped electrons. Under this condition only a lateral field is applied to the device, and electrons are injected from the gate into the gate insulator or the surface states, proceeding by hopping toward the drain [120]. This trapping mechanism is thermally accelerated (see Figure 5.6 (c)), since high temperatures may favour the injection of electrons from the gate toward the gate-drain access region; the activation energy of this surface related process is equal to 1.23 eV (Figure 5.6 (d)).

As described above, buffer-related trapping processes can be effectively investigated by applying a backgating bias (negative substrate voltage); under this condition the lateral field is zero and the surface-related trapping effects are neg-



(a) R_{ON} trapping transient. (b) Derivative of the stretched exponential fit.

Figure 5.5: (a) R_{ON} transient during 1000 s trapping measurements under the three bias conditions of Figure 5.4 performed at 80°C ; (b) time constant spectra of the R_{ON} transient.

ligible. In the backgating condition R_{ON} increases exponentially over time as shown in Figure 5.5 (a); the time constant is in the range of 5-10 s at 80°C (see Figure 5.5 (b)). An increase of the temperature results in a significant acceleration of the trapping kinetics (see Figure 5.6 (b)); the related activation energy is equal to 0.80 eV (see Figure 5.6 (d)). In the backgating condition a strong vertical field is applied between drain and substrate, inducing pure vertical trapping with negligible surface effects; the R_{ON} increase could be ascribed to the injection

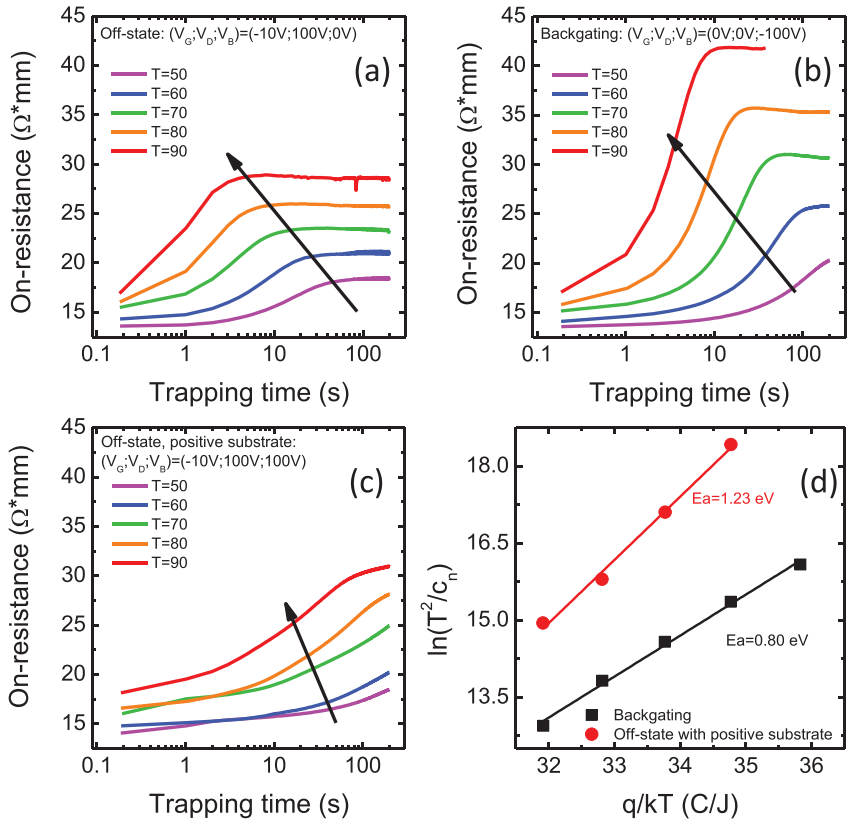


Figure 5.6: (a)-(c) Temperature dependent R_{ON} increase for the three trapping conditions of Figure 5.4; (d) Arrhenius plot of the trapping process under pure vertical trapping and pure lateral trapping. The Arrhenius plot has not been reported here for the off-state trapping (a), since in this case the two discussed trapping mechanism are superimposed; the plot is reported separately in Figure 5.2 (c).

of electrons from substrate into trap states located below the two-dimensional electron gas (either in the buffer or in the GaN channel layer).

Looking again at the plots of Figure 5.5 and 5.6 we can observe that the off-state condition is not merely the superimposition of the effects of vertical and lateral trapping. Indeed, the percentage dynamic-R_{ON} increase is 56% for the off-state condition and 120% for the backgating. A possible explanation is that during the backgating electrons are injected from the substrate, along all the device structure, from the source to the drain (see Figure 5.4 (b)); in the off-state condition, the voltage level of 100 V drop form the drain to the gate, with a trend that depends on the resistivity of the different GaN layers; thus, the vertical potential along the whole device structure is not so high as in the backgating condition. Even comparing the off-state condition with the off-state with positive substrate bias (Figures 5.6 (a) and (c)), the latter clearly induces a slightly higher R_{ON} increase, even though at 200 s the trapping process is still not finished; the reason of this difference could be that when both the vertical and lateral trapping take place, the injection of electrons from the substrate can affect somehow the lateral trapping, decreasing its effect; instead, when only the lateral field is applied the surface trapping fully appears.

In the second part of our analysis we try to confirm the hypothesis that the buffer leakage current is involved in the dynamic-R_{ON} increase. For this purpose temperature dependent trapping and I_D-V_D measurements have been carried out (see Figure 5.7).

For high drain-substrate fields, the charge trapping rate (i.e. the reciprocal of the trapping time constant) is linearly correlated to the drain-bulk leakage current (see Figure 5.7); an increase in temperature induces a significant acceleration of the trapping kinetics. In particular, we can see from the graph of Figure 5.7 (b) that the thermal activation of both capture rate and buffer leakage is very similar. This means that the activation energy of 0.80 eV found for the backgating trapping process (see Figure 5.6 (d)) is the same as the bulk current; this confirm without doubts the origin of the backgating R_{ON} increase.

All the measurements presented up to now referred to the first of three device generations. Then, we started to analyse even the improved second and third device generations; the layout was identical, but the buffer was improved, with lower buffer leakage. As we can see in Figure 5.8 samples with lower vertical leakage show a smaller R_{ON} increase, compared with devices with high drain-bulk leakage (first generation). This is clearly explained in Figures 5.8 (a)-(c), which report the increase in R_{ON} measured on the three wafers, and in Figure 5.8 (d) and (e), which report a quantitative comparison of the three wafers in terms of R_{ON} increase and buffer leakage. This results are consistent with the hypothesis that in backgating the trapping rate depends on the supply of electrons from the buffer, and indicate that the buffer optimization is a necessary step toward the reduction of high-temperature dynamic-R_{ON}.

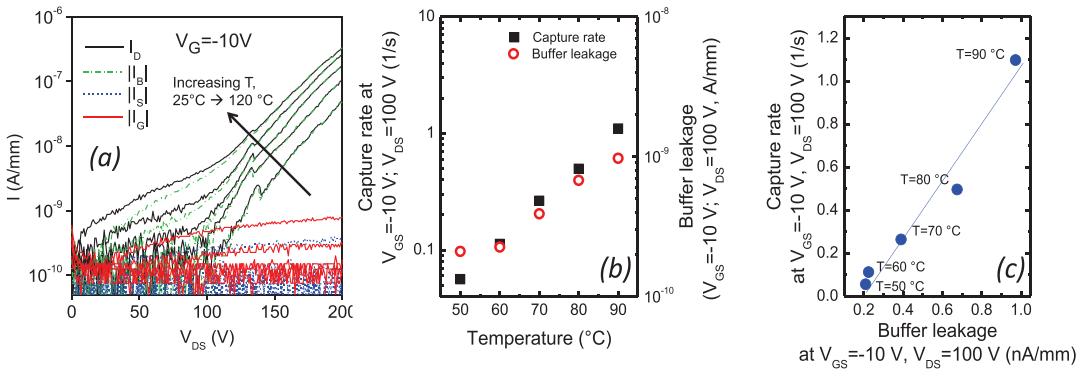


Figure 5.7: (a) Off-state I_D-V_D curves measured on one of the analysed sample (generation 1) at increasing temperature levels; (b) dependence of the capture rate and of buffer leakage (both measured at $(V_{GS}, = -10\,V, V_{DS} = 100\,V, V_B = 0\,V)$ on temperature; (c) linear correlation between capture rate and buffer leakage.

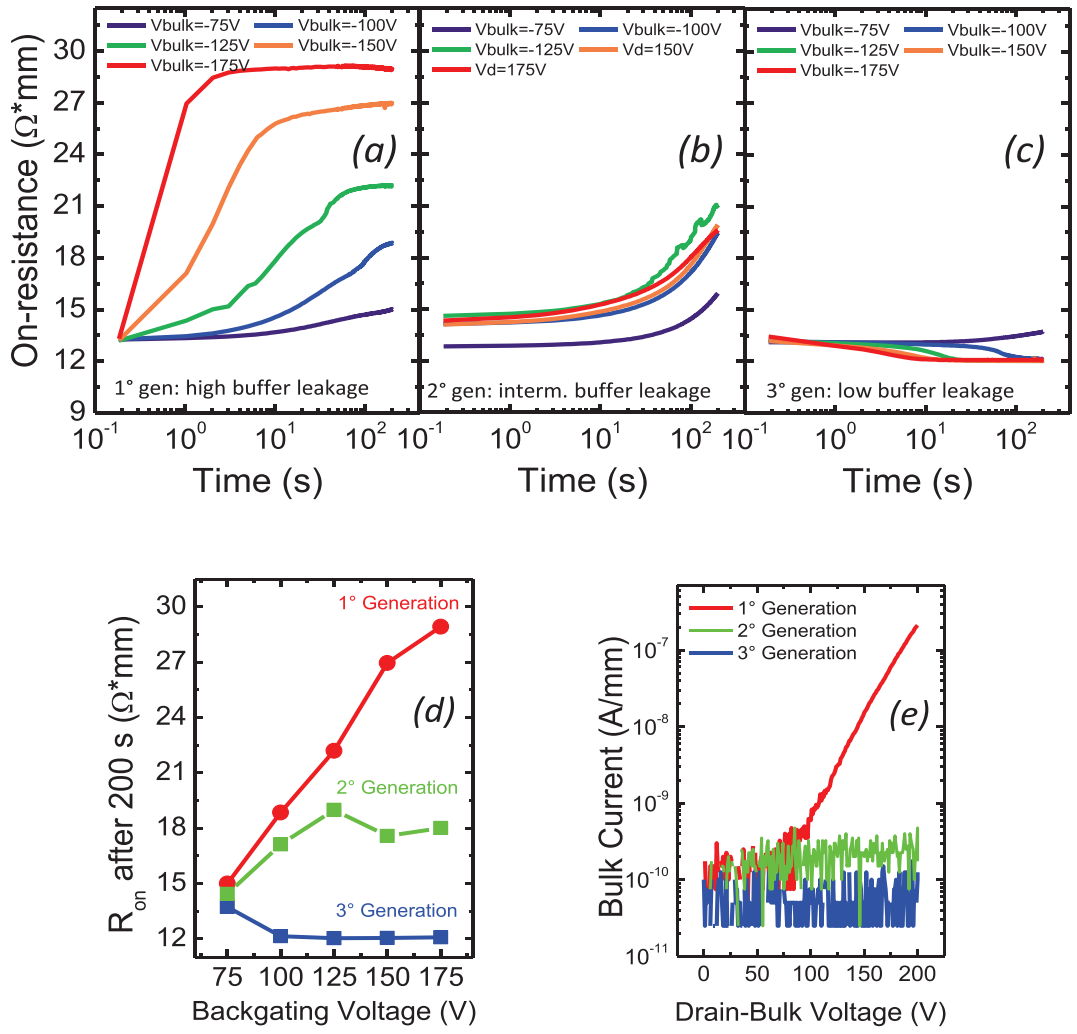


Figure 5.8: Variation in R_{ON} induced by increasing backgating voltages for three different buffers with (a) high, (b) intermediate, and (c) low drain-substrate leakage; (d) change in R_{ON} induced by 200 s of trapping in backgating condition on the same three wafers; (e) bulk leakage as a function of drain-bulk voltage for the same three wafers. The measurements have been carried out at 40°C.

All the results presented so far have been published in a paper in March 2015 [69]. In the next period a lot of efforts have been made, and one year later the device were dramatically improved. Most of the trapping and pulsed measurements reported until now have been performed with a drain voltage of 100 V. However, this Gan-based HEMT technology is designed to work up to 650 V, therefore, we developed a new pulsed system that can work up to 600 V. As mentioned before, in the case of the 600 V pulsed system, the pulse timing is limited to $T_{ON} = 20\,\mu s$, $T_{OFF} = 2\,ms$. With the new GaN-based HEMT generations the 600 V pulsed measurements became a routine-test for checking the results of the last device improvements in terms of dynamic-R_{ON}.

In the following are reported the outstanding results obtained with the last de-

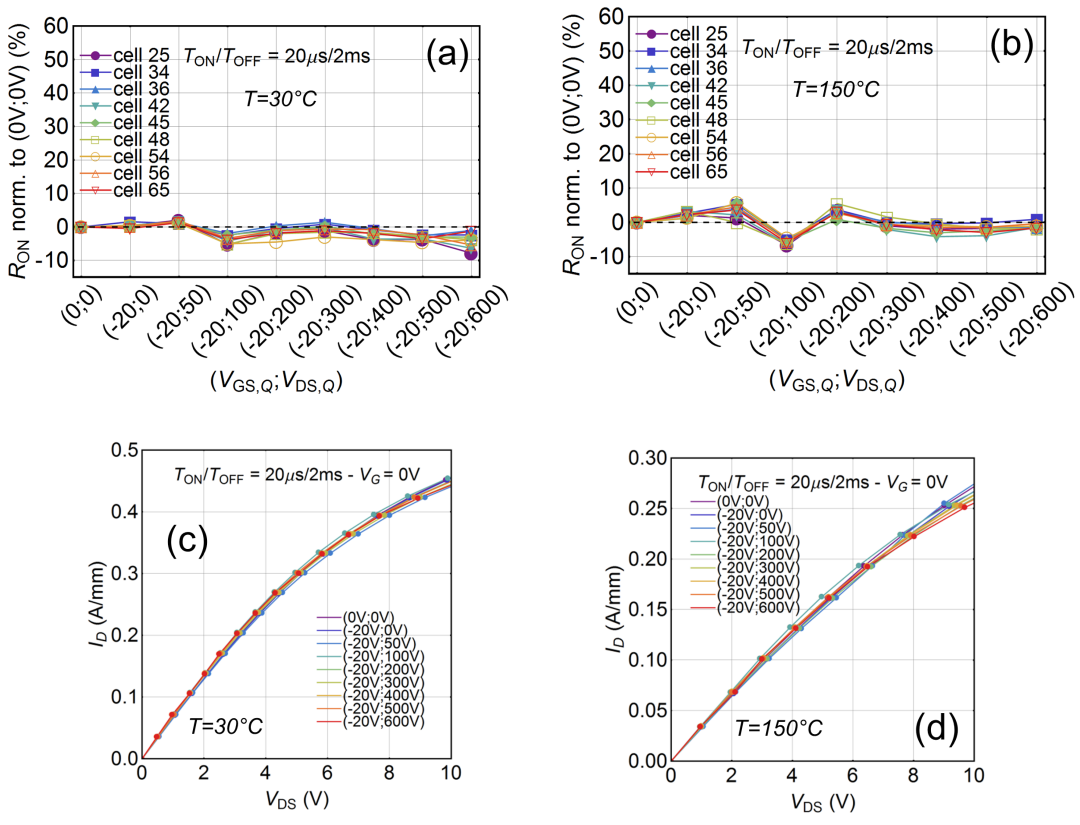


Figure 5.9: Percentage dynamic-R_{ON} up to $V_{DS} = 600\,V$ for 9 samples at (a) room-temperature and (b) T = 150°C; double pulsed I-V characteristics for 1 sample (c) room-temperature and (d) T = 150°C.

vice generation, recently presented in a conference [53]. In Figure 5.9 is reported the dynamic-R_{ON} characterization at room temperature and 150°C for drain voltages up to 600 V. In the graphs of Figures 5.9 (a) and (b) we can observe the high homogeneity of the nine devices measured over the whole wafer area. In Figures 5.9 (c) and (d) are reported the I-V characterizations for one sample at room- and high-temperature conditions. We can observe that the stability of the output characteristics extends over the linear region, up to $V_{DS} = 10\,V$. This results demonstrate that now this technology is fully current collapse free, over the whole temperature and voltage window.

5.1.2 High temperature tests

The next step in the research activity, after the pulsed and trapping measurements, was to analyse the stability of the device submitted to high temperature/reverse gate bias conditions (HTRB). In GaN-based MIS-HEMTs submitted to off-state stress it is possible to observe a negative bias induced threshold instability (NBTI) [47]. In order to investigate the NBTI we defined an experimental procedure for the HTRB tests.

During the test the device is biased for 4000 s in off-state/high voltage condition ($V_G = -30\,V$, $V_{DS} = 520\,V$), at 150°C. In order to monitor the trend of the on-resistance and the threshold voltage the stress is interrupted at log-scaled time intervals to perform a fast I_D-V_D and a fast I_D-V_G characterization. The I_D-V_D is performed at $V_G = 0\,V$, with V_D from 0 V to 0.5 V, while the I_D-V_G is performed at $V_D = 5\,V$, and on a V_G range wide enough to measure the threshold shift during the stress. The value of R_{ON} is extrapolated from the slope of the I_D-V_D, while V_{th} is calculate at a current level of $1\,\mu A/mm$. The duration of these measurements is around 5 s, short enough if compared with the detrapping process time constants. A preliminary test without bias applied confirm that the I_D-V_G itself has negligible impact on the threshold shift. Just before the stress start we perform a preliminary fast characterization, indicated as "after DC" in the plots. After each stress we carried out a 4000 s recovery phase with no bias

applied and with the same series of fast characterizations.

Figure 5.10 reports the V_{th} shift during the off-state test. Just after 1 s of stress the V_{th} is already shifted to negative values with a ΔV_{th} of -4 V; after this first stage the shift trend becomes slower, and after 1000 s reaches a saturation around $\Delta V_{th} = -5.5$ V. During the recovery the V_{th} starts to come back with a very slow dynamic, and at the end of the test there is still a shift of $\Delta V_{th} = -3.5$ V, nevertheless the high temperature condition.

This shift is ascribable to the detrapping of electrons from trap states located at the AlGaN/SiN interface, or in the gate insulator [47][84]. A schematic illustration of the trapping mechanism is shown in Figure 5.11. The defects, are represented for simplicity as donor states in the insulator, neglecting the interface

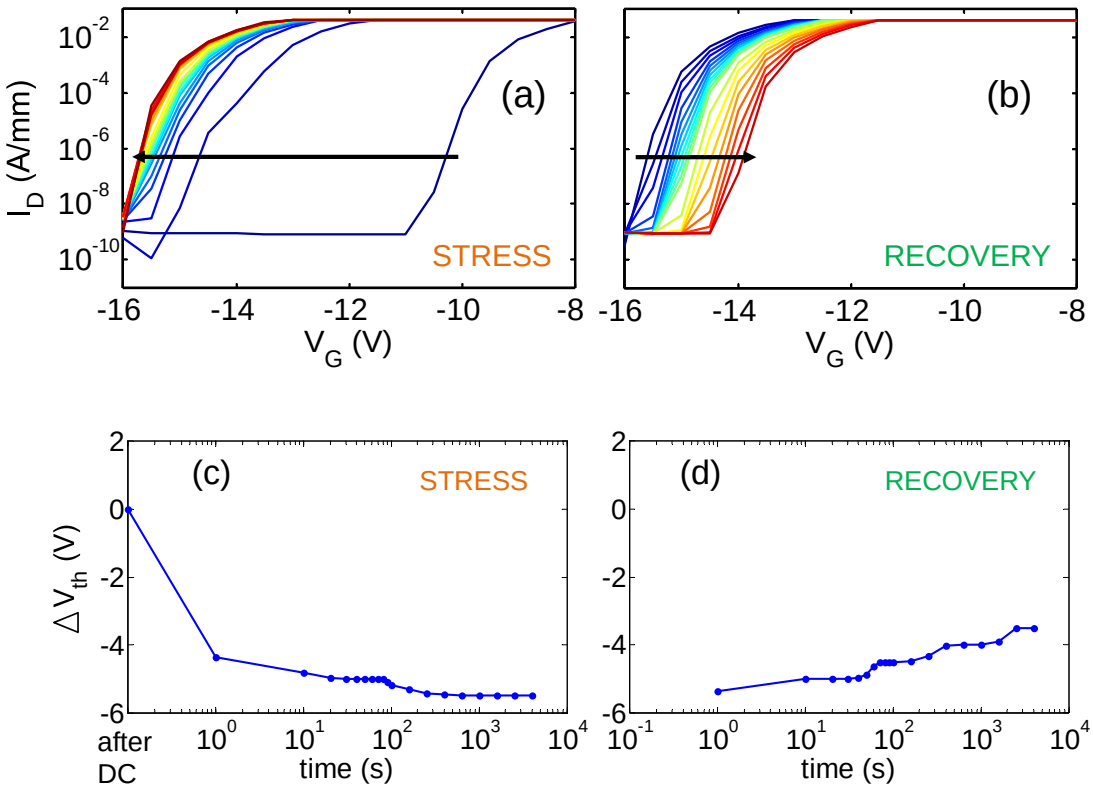
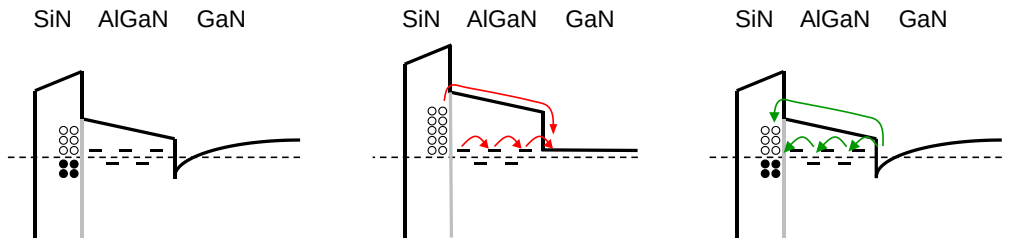


Figure 5.10: Fast I_D-V_G measurements taken (a) during the HTRB test ($V_G = -30$ V, $V_{DS} = 520$ V) and (b) during the recovery. Threshold voltage shift ΔV_{th} calculated at 1 μA/mm for the stress (c) and the recovery (d). The test temperature was T = 150°C.



(a) Before stress (V_G=0 V) (b) Stress (V_G<0 V) (c) Recovery (V_G=0 V)

Figure 5.11: Schematic representation of the process responsible for the negative V_{th} shift (a) before the stress, (b) during the off-state stress and (c) during the recovery.

states. The defects below the Fermi level are neutral, while the ones above are positively charged (see Figure 5.11 (a)). When a negative bias is applied to the gate, the trap states are depleted, either thermally, by tunnelling through the AlGaN, or via defect-assisted conduction, possibly involving dislocations [121] (see Figure 5.11 (b)). The depletion of the defects results in a net positive charge, that shift the threshold towards more negative values. When the gate bias comes back to zero, during the recovery, the defects fall again below the Fermi level and start to be filled again with electrons (see Figure 5.11 (c)). This process is slow, since the electrons have to move back through the AlGaN barrier by defect assisted conduction. The recovery process is self-limited, due to the repulsive electrostatic action of electrons that already reached the defects, and to the limited amount of defects available for conduction through the barrier [121]. This self-limited behaviour explains the logarithmic time dependence of the recovery phase (see Figure 5.10 (d)). We can notice that at the end of the recovery, the threshold shift is still $\Delta V_{th} = -3.5\,V$. Measurements carried out in a post-following after 10 months confirm that the recovery is still not full, with a residual $\Delta V_{th} \approx -2\,V$. This shows how part of the trapped charge can be permanently stored in the insulator.

The next two steps are to understand the role of the drain voltage in the

NBTI process and to observe the variation of the on-resistance during the HTRB test. In Figure 5.12 (c) and (d) we can observe that for $V_{DS} = 0\,V$ the V_{th} shift is limited at the value of 2 V. Whit a positive drain voltage, already at $V_{DS} = 150\,V$ the ΔV_{th} reaches values around -6 V. The amount of threshold shift seems to be almost independent from the applied V_{DS}; we noticed that the value of ΔV_{th} is more dependent on its initial value: more positive is the starting V_{th}, higher is the threshold shift, with final V_{th} values that are very homogeneous. This fact indicates that even though there is a limited variability of the threshold voltage in the wafer area, it does not affect the final value of the threshold at the end of the stress. A possible explanation is that the variability of V_{th} is caused by

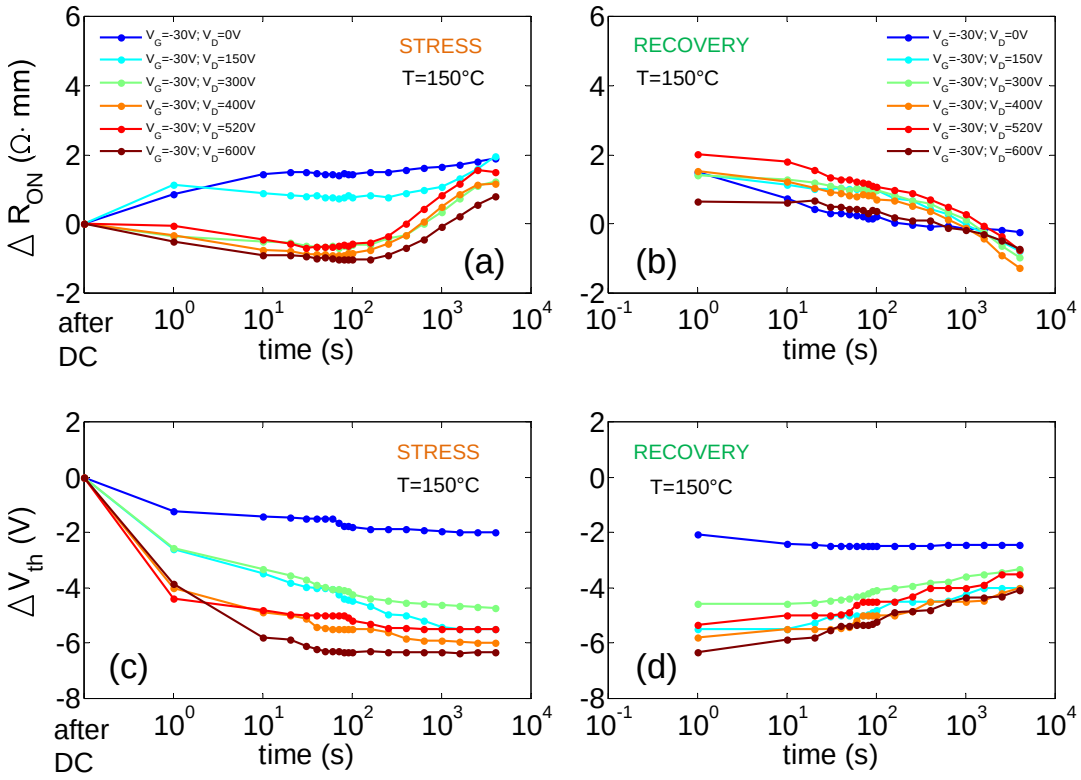


Figure 5.12: On-resistance variation ΔR_{ON} during the HTRB stress (a) and recovery (b). Threshold voltage shift ΔV_{th} calculated at $1\,\mu A/mm$ for the stress (c) and the recovery (d). The drain voltage spans form 0 V up to 600 V. The test temperature was $T = 150°C$.

some differences in interface trap states concentration, that are then fully depleted during the stress. The main influence of the V_{DS} on the stress is that the dynamic of the V_{th} is slower for $V_{DS} \leq 300\,V$.

The increase of V_{DS} during the stress is reported in Figure 5.12 (a). We can observe that for $V_{DS} \geq 300\,V$ there is a slight V_{DS} decrease in the first 100 s of stress, followed by an increase, lower than 2 $\Omega \cdot$ mm, and comparable with the final result of the stress with lower or no drain bias applied. The origin of this behaviour remain unclear, even though at higher drain voltages the high lateral filed can induce some trapping phenomena, resulting in an increase of R_{ON}. An additional HTRB stress, carried out up to 10^5 s, confirm that the R_{ON} increase

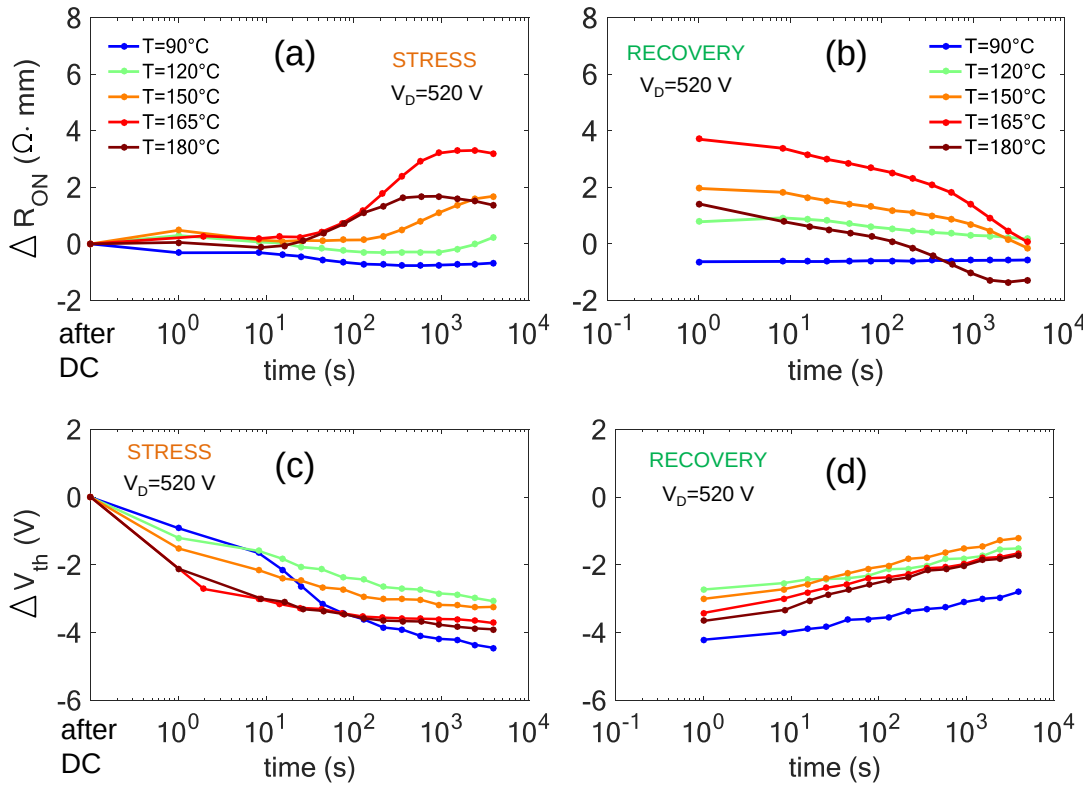


Figure 5.13: On-resistance variation ΔR_{ON} during the HTRB stress (a) and recovery (b). Threshold voltage shift ΔV_{th} calculated at 1 μA/mm for the stress (c) and recovery (d). The drain voltage was 520 V. The test temperature range was between 90°C and 180°C.

saturates for long times.

In order to investigate the thermal dependence of the observed trapping process we carried out HTRB stresses at different temperatures, form 90°C to 180°C (see graphs of Figure 5.13). For temperatures lower than 150°C the ΔR_{ON} is negligible, and the process time constant becomes faster at higher temperatures; at T = 180°C the peak of the ΔR_{ON} is lower, respect to the one observed at 150°C, but the process is anyway faster.

In this case we adopted a polynomial data fit, instead of the stretched exponential, obtaining the time constants from the derivative's peaks (see Figure 5.14 (b)); the estimated activation energy of this process is 0.94 eV (see Arrhenius plot in Figure 5.14 (c)).

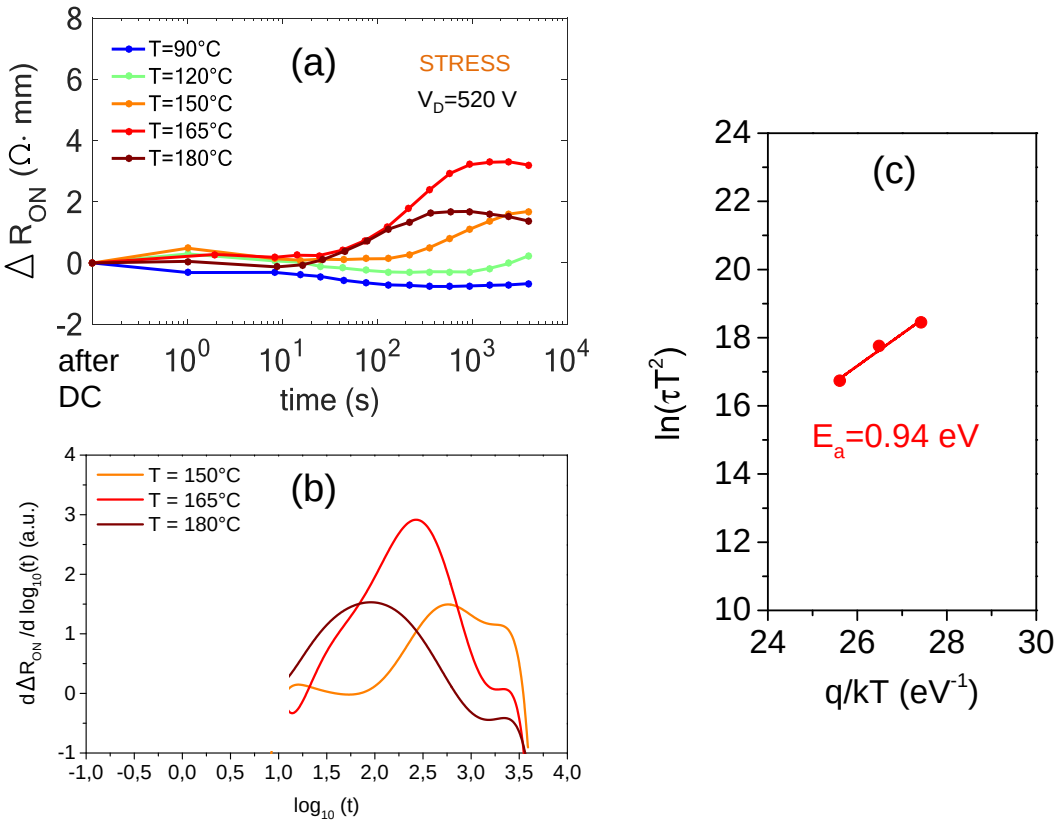


Figure 5.14: On-resistance variation ΔR_{ON} during the HTRB stress (a); derivative of the polynomial fit (b); Arrhenius plot (c). The drain voltage was 520 V. The test temperature range was between 90°C and 180°C.

In the previous analysis we reported the effect of the NBTI under off-state condition, but the GaN-based MIS-HEMTs are d-mode devices typically implemented in cascode configuration with an e-mode Si-MOSFET (see sketch of Figure 5.15). The potential at the common node between the source of the HEMT and the drain of the MOSFET is floating, and when the MOSFET is turned off the value of ΔV_{GS} of the HEMT is in principle unknown. In this configuration, the proper design of the off-state leakage currents of both the MOSFET and the HEMT is fundamental. The off-state leakage current of the MOSFET should be slightly higher than the HEMT one; in this way, when the MOSFET is turned off, its leakage current need to flow trough the HEMT, that goes in a sub-threshold condition very close to the off-state; the ΔV_{GS} potential can thus stabilize on a value that depends on the V_{th} , with typical values in the range between -8 V and -14 V.

In order to test the device in a condition that is closer to the real operative one, we develop an original experimental procedure. We named this new test HTSC since it is an high-temperature stress with a current forced to flowing out of the source (at high drain voltage condition); in this way we reproduce the same situation of the cascode configuration. The differences between the HTRB

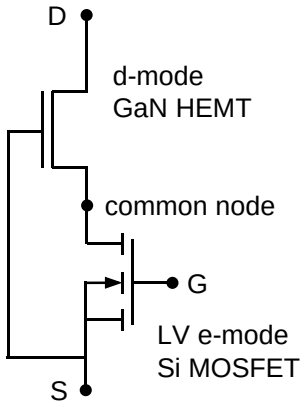


Figure 5.15: Schematic representation of a cascoded e-mode GaN-based HEMT. At the bottom side is connected a low-voltage d-mode Si-MOSFET. The potential at the common node is floating.

an the HTSC systems is that for the former the gate voltage is kept constant, while for the latter a constant current is forced to flow out of the source; the other measurement procedures are exactly the same as the HTRB stress. The minimum value for the source current is determined by the off-state leakage level with high drain voltage bias. In our case this level is around 2 nA, thus we decided to keep as first stress-current level the value of 5 nA.

In Figure 5.16 are reported the results of the HTSC test for three different source current levels (5 nA, 20 nA, and 200 nA), superimposed to the results of the HTRB test. Regarding the ΔR_{ON}, the situation is worse than in the HTRB case, with a R_{ON} increase that depends on the source current level: higher I_S

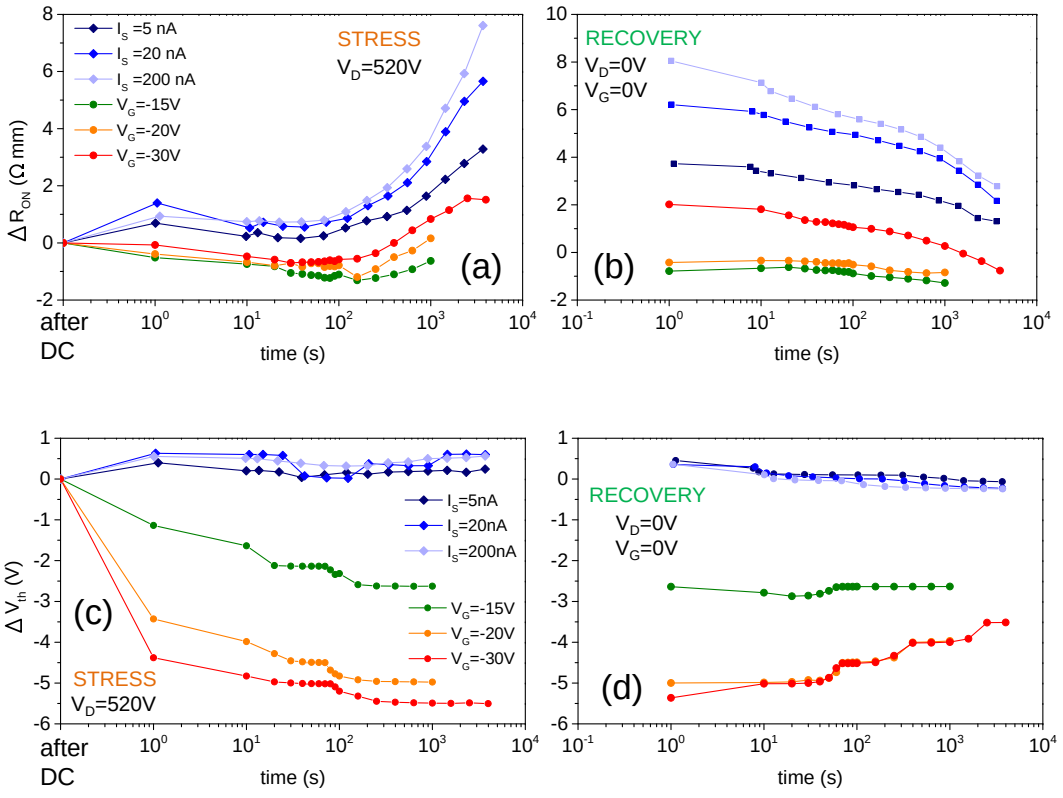


Figure 5.16: On-resistance variation ΔR_{ON} during the HTSC and the HTRB stress (a) and recovery (b). Threshold voltage shift ΔV_{th} calculated at 1 μA/mm for the stress (c) and the recovery (d). The drain voltage was 520 V. The test temperature was 150°C.

leads to higher ΔR_{ON}. The time constant of the process remain the same for all current levels, with values around 1000 s; the dynamic seems very similar to that one of the HTRB, but with a slightly higher ΔR_{ON} even at the lower current level. For the R_{ON} recovery process (Figure 5.16 (b)), the dynamic of the HTSC test indicates that the detrapping mechanism is the same.

Regarding the threshold voltage shift, we can observe in Figure5.16 (c) that in the case of the HTSC test there is any negative ΔV_{th}; the shift is instead positive (≈ 0.5 V), and is fully recoverable. The reason of this different behaviour is that for the HTSC stress the device is biased in sub-threshold (around $V_G = -12\,V$) and the band diagram is not bended enough to let start the detrapping process described for the HTRB test (see Figure 5.11 (b) at pag. 136).

An additional comparison that is reported in Figure 5.16 is the HTRB test performed at different gate voltages (-15 V, -20 V, and -30 V). For a matter of time the tests at $V_G = -15\,V$ and $V_G = -20\,V$ were stopped at 1000 s. However, we can observe that for less negative gate voltages there is a lower ΔR_{ON} (see Figure 5.16 (a)). The V_{th} shift is less severe at $V_G = -15\,V$, since the band diagram is closer to the sub-threshold condition, and even if the dynamic is the same, the final ΔV_{th} is lower (-2.5 V), if compared with the stress at

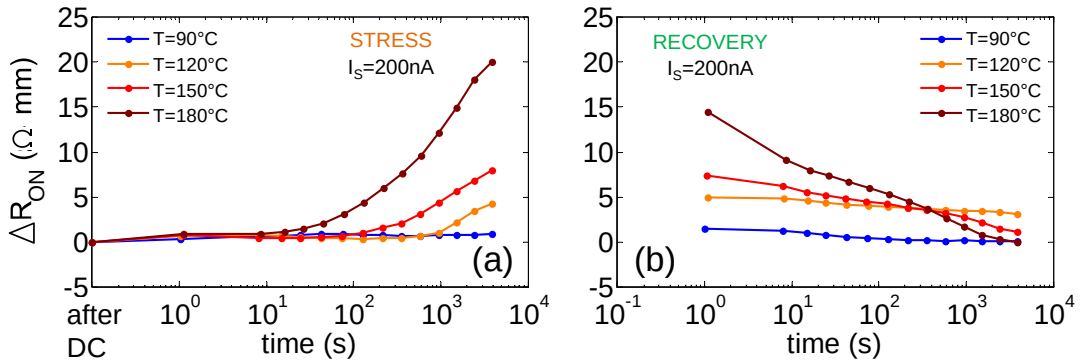


Figure 5.17: On-resistance variation ΔR_{ON} during the HTSC stress (a) and recovery (b). The drain voltage was 520 V, and the source current was 200 nA. The test temperature range was between 90°C and 180°C.

$V_G = -20\,V$ ($\Delta V_{th} = 5\,V$). As last observation, if we look at the recovery graph in Figure 5.16 (b), the yellow and green curves of the HTRB present a ΔR_{ON} value that is permanently below the pre-stress one. It seems that this ΔR_{ON} decrease is not recoverable, as the stress had a positive effect on the device.

In order to investigate the R_{ON} increase during the HTSC test we performed tests at different temperatures (from 90°C to 180°C). In the plots of Figure 5.17 we can see an higher ΔR_{ON} at higher temperatures; The dynamic of the recovery is faster at higher temperatures, but the trend is not the typical stretched exponential observed in the drain current transients; this indicates that the involved trapping phenomena can not be the typical emission from deep states.

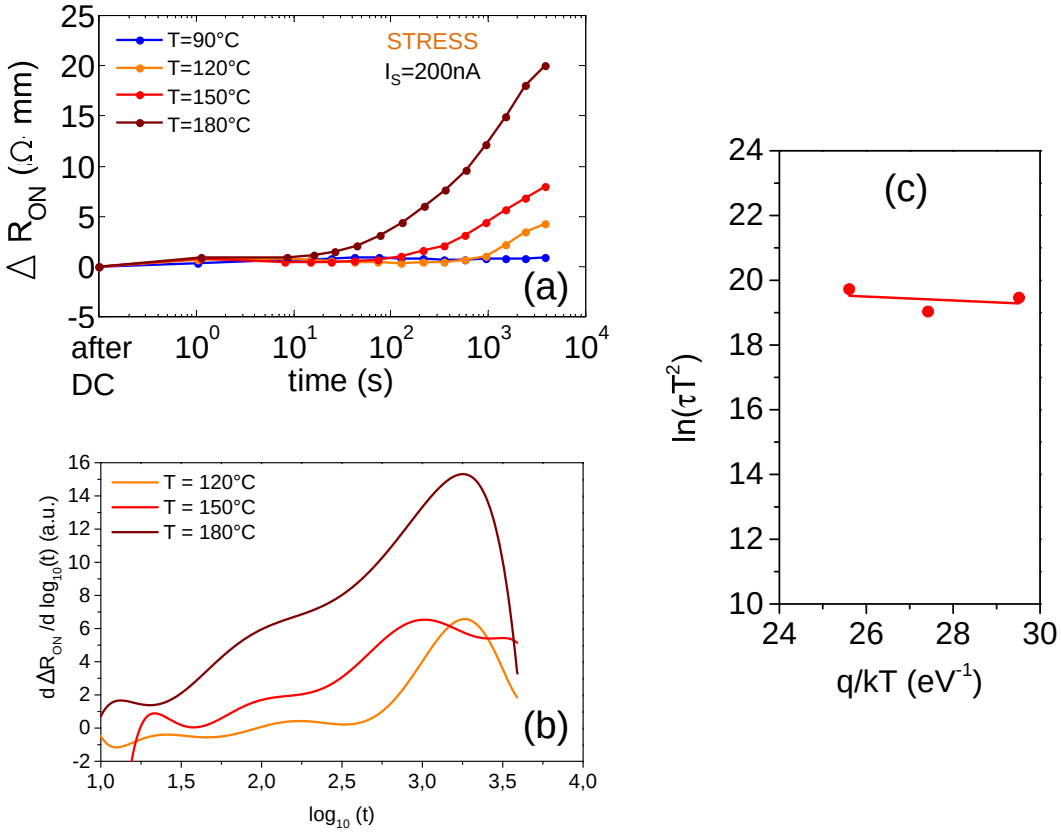


Figure 5.18: On-resistance variation ΔR_{ON} during the HTSC stress (a); derivative of the polynomial fit (b); Arrhenius plot (c). The drain voltage was 520 V. The test temperature range was between 90°C and 180°C.

In Figure 5.18 we can see that the trapping process is not thermally activated, even if the peak of the derivative increases at higher temperatures, as the final ΔR_{ON} value. No many works in literature report such trapping dynamic; the originality of our work is that we found these results within a test that emulates the operative device conditions. However, it is still under debate which trapping mechanism is involved in this process, but we can list some observations about:

- In comparison to the DLTS reported above, there are many differences: higher drain voltages, higher temperatures, and longer times. In particular, the higher drain voltage applied generates higher electric fields, and thus hot carriers, that can be involved in trapping mechanisms. Then, the devices analysed in the DLTS are from older generations and can not be fully compare with the last one.

- The insulating-GaN layer under the channel is Carbon-doped. This implies that even hole-related phenomena can be involved in the trapping process. Since we can see only the effects of these processes, it is hard to draw conclusions about.

- In literature is reported a not-thermally activated process for GaN-based MIS-HEMTs [122]. In that work it has been performed a drain current transient at $V_{DS} = 250\,V$; the difference with our measurements is that here has been considered a detrapping process. Anyway, the increasing of both the peak of DLTS spectra and the R_{ON} value are very similar to our case. The proposed explanation for the phenomenon is that in high drain voltage condition there are peaks of the electric field located under the the field plates edge; this can cause a massive injection of electrons by hot carrier injection or Zener tunnelling [123]. This mechanism is a tunnelling from the valence band into defects states, triggered by the high electric field.

After the results of the HTRB and HTSC test a lot of efforts have been made to work out the increase of on-resistance. We can see the outstanding results of the last technology in the graph of Figure 5.19 (a). The wafer analysed above is indicated as 1st gen., and the new technology as 2nd gen. We can observe that in the new generation there is any R_{ON} increase either in HTRB and HTSC tests; the ΔR_{ON} is limited only to $1\,\Omega \cdot \text{mm}$. As conclusion, we can say that this technology, in addition to be current collapse free, can work in a cascode system with stable performance in high temperature condition.

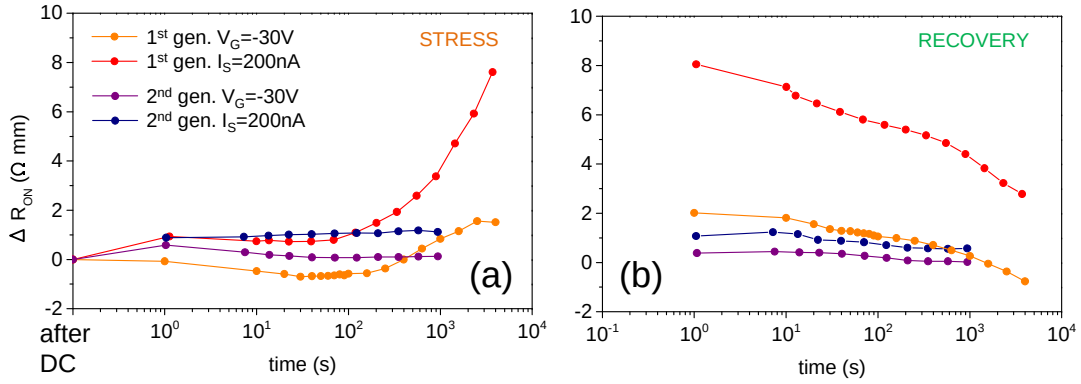


Figure 5.19: Comparison between two wafer generations: on-resistance variation ΔR_{ON} during the HTSC and the HTRB stress (a) and recovery (b). The drain voltage was 520 V. The test temperature was 150°C.

5.2 GaN-based p-type gate HEMTs

In the following we will report the results of the research activities on the GaN-based p-tpye gate HEMTs, or briefly, p-GaN HEMTs. These results were obtained during my period abroad, by FBH in Berlin.

Among the different solutions to obtain e-mode GaN-based HEMTs, the p-GaN technology is one of the more promising, and it is already possible to find commercial products with this technology inside. Unlike the cascode solution for the d-mode transistors, the possibility to have a single normally-off device on a monolithic chip is better, especially for the reduction of the device parasitics. However, the p-GaN technology has pros and cons, and some aspects of the device operation and reliability are not yet fully understood.

In Chapter 3 we have already presented a part of the work carried out on the p-GaN devices, since the simulations deserved to be treated separately. However, some simulation results will be showed again, since they can help to clarify some measurements details.

When I went abroad, the *Hiposwitch* project was at its conclusion, after three years. For this reason I would like to skip all the results obtained within that project, for better concentrating on the results of my research activity in Berlin. The *Hiposwitch* project was founded by the European Community, and a lot of partners have been involved, including universities, companies, and research centres from many European countries. FBH was the research centre that developed the technology, and at the end of *Hiposwitch* the research activity on the p-GaN devices was still going on. Thus, the purpose of my work there was to perform on-state stresses in high temperature, to investigate the device degradation mechanisms.

5.2.1 On-state stress

The aim of the on-state stress is to investigate the device degradation mechanisms in a condition that is close to the operative one. During the on-state stage of a power switching system this transistors work with a low drain voltages ($\approx 1\,V$) and high drain currents ($\approx 10\,A$). With the on-state stress we have a continuous current, not a switching condition, but we can anyway study the long term effects of the stress on the devices.

Devices and test description

The analysed devices were three generations of normally-off p-GaN HEMTs developed by FBH. The details of the wafers GEN1, GEN2, and GEN3 are reported in Table 5.1; most parameters of the technology GEN3 were not disclosed. The tested transistors were on package devices with layout geometry indicated in Table 5.2. The stress conditions chosen for all tests were:

- $V_G = 5\,V$;
- $I_D = 50\,mA/mm$;
- $V_D \approx 1\,V$;
- $T = 150°C$;

Table 5.1: Details of the tested wafers.

Technology	Substrate	AlN thickn. (nm)	Buffer type	Buffer thickn. (μm)	Channel thickn. (nm)	AlGaN thickn. (nm)	p-GaN thickn. (nm)
GEN1	4H:SiC	50	GaN:Fe	2.85	850	9	99
GEN2	Si(111)	100	AlGaN	2.30	135	15	100
GEN3	Si(111)	n.d.	n.d.	n.d.	n.d.	n.d.	n.d.

The target test time was of 1000 hours. A complete DC characterization has been performed before each test and when the test was stopped at defined time steps: 24h, 48h, 96h, 192h, 384h, 768h and 1000h. Even though the stress current density of 50 mA/mm seems to be not so high, it corresponds to the rated operative current of 10 A in the bigger 200 mm devices. The stress is in constant drain current and constant gate voltage; the drain voltage can slightly change during the stress, but its value remains close to 1 V (see the stress bias point represented in Figure 5.20).

The critical parameter measured during the stress was the gate current. For the DC characterization we are more interested in the GS-diode and I_D-V_G plots.

On-state stress results

The first result that we can observe in the plots of Figure 5.21 is the variation of the gate leakage current during the test. For a matter of time, for devices of technology GEN3 the test has been interrupted at 384 hours; however, as we can see in Figure 5.21 (c) the gate leakage increase seems to saturate after 200 h.

The leakage increases in most samples with a stretched exponential trend

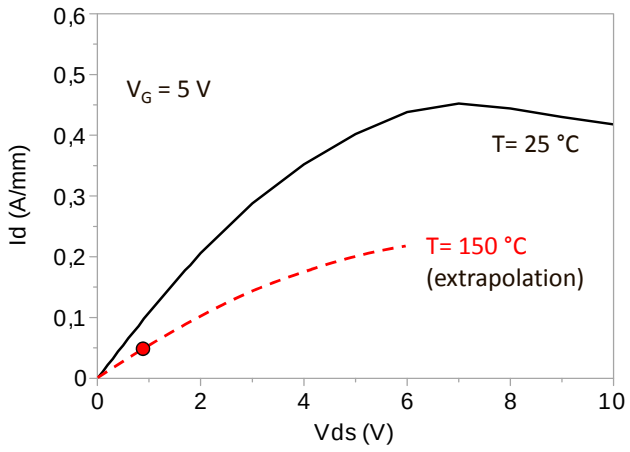


Figure 5.20: I_D-V_D curve of a tested device at T = 25°C (black line) and extrapolation at the stress temperature of 150°C; the red dot indicates the stress bias point.

during the test. However, each time the test restarts after the characterization, the leakage current starts again from levels closer to the initial one. Since most of the leakage increase is recoverable, it can be only ascribed to trapping phenomena, that are superimposed to a permanent device degradation. It can also be noticed that for some devices of GEN2 and GEN3 wafers there is an irregular trend of the

Table 5.2: Details of the tested devices.

Technology	L_{GD} (μm)	L_{GS} (μm)	L_G (μm)	W_G (mm)	# dev
GEN1	15	1.0	1.1	3.2	4
GEN2	15	1.0	1.1	2.1	4
GEN3	15	1.0	1.1	2.3	6

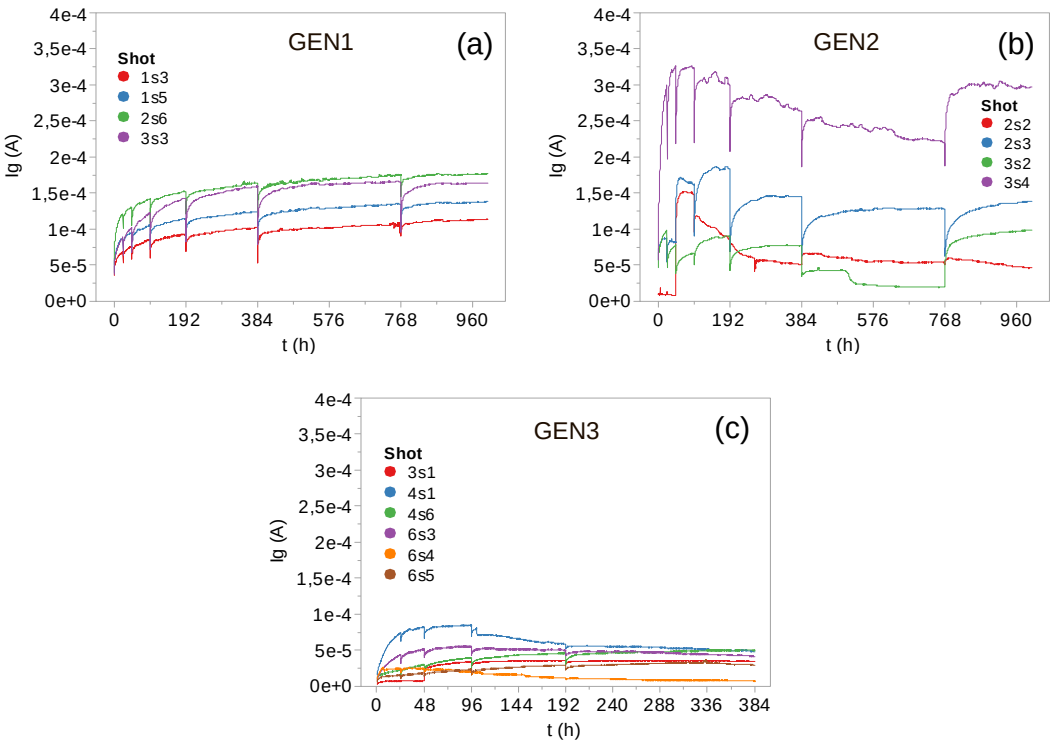


Figure 5.21: Gate current I_G variation during the stress for GEN1 (a), GEN2 (b), and GEN3 (c) devices.

gate leakage; the reason of this behaviour is not clear but it is an indication that the trapping/degradation processes could be influenced by several effects induced by the stress. It could be involved the diffusion of Mg from the p-GaN into the AlGaN, or some other degradation process of the barrier.

In Figure 5.22 is reported the trend of the GS-diode characterization taken during the stress for one representative device for each technology. We can see that the leakage increase is not so relevant, either in off- or in on-state. We can observe that the leakage increase in on-state is correlate with the leakage increase during the stress, even though the values are ten times lower.

In Figure 5.23 is reported the sequence of I_D-V_G transcharacteristics taken throughout the stress. The graphs are reported either in linear scale (left side) that in log scale (right side) for one device for each technology.

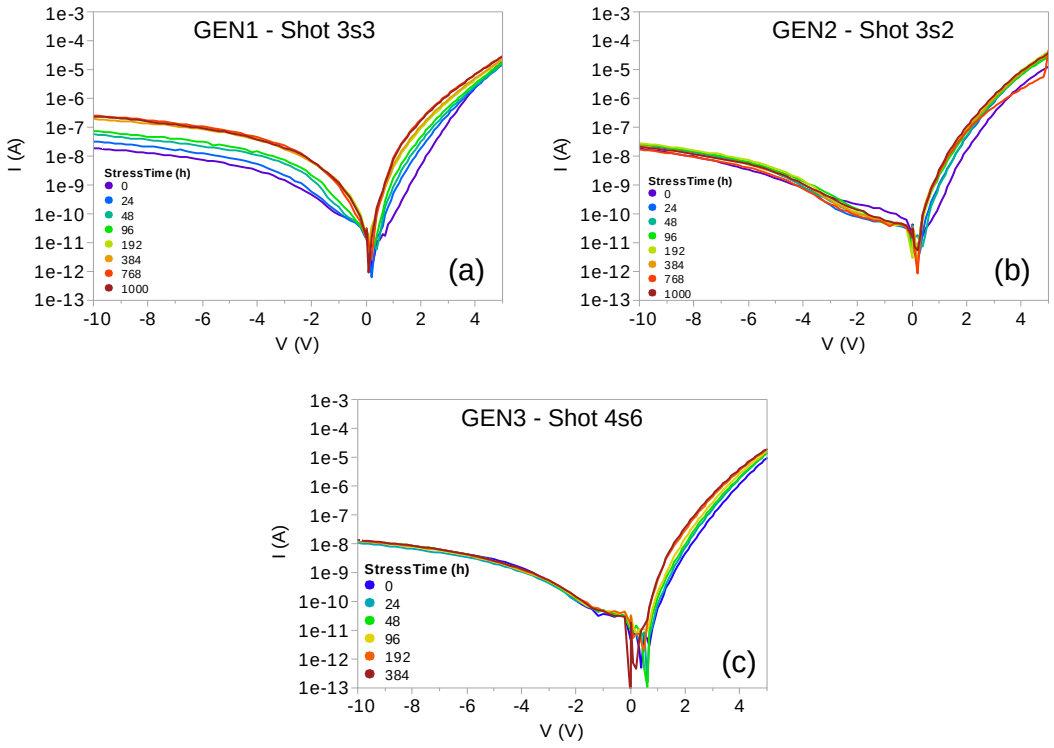


Figure 5.22: Gate-source diode current variation during the stress for a representative sample of GEN1 (a), one of GEN2 (b), and one of GEN3 (c) devices.

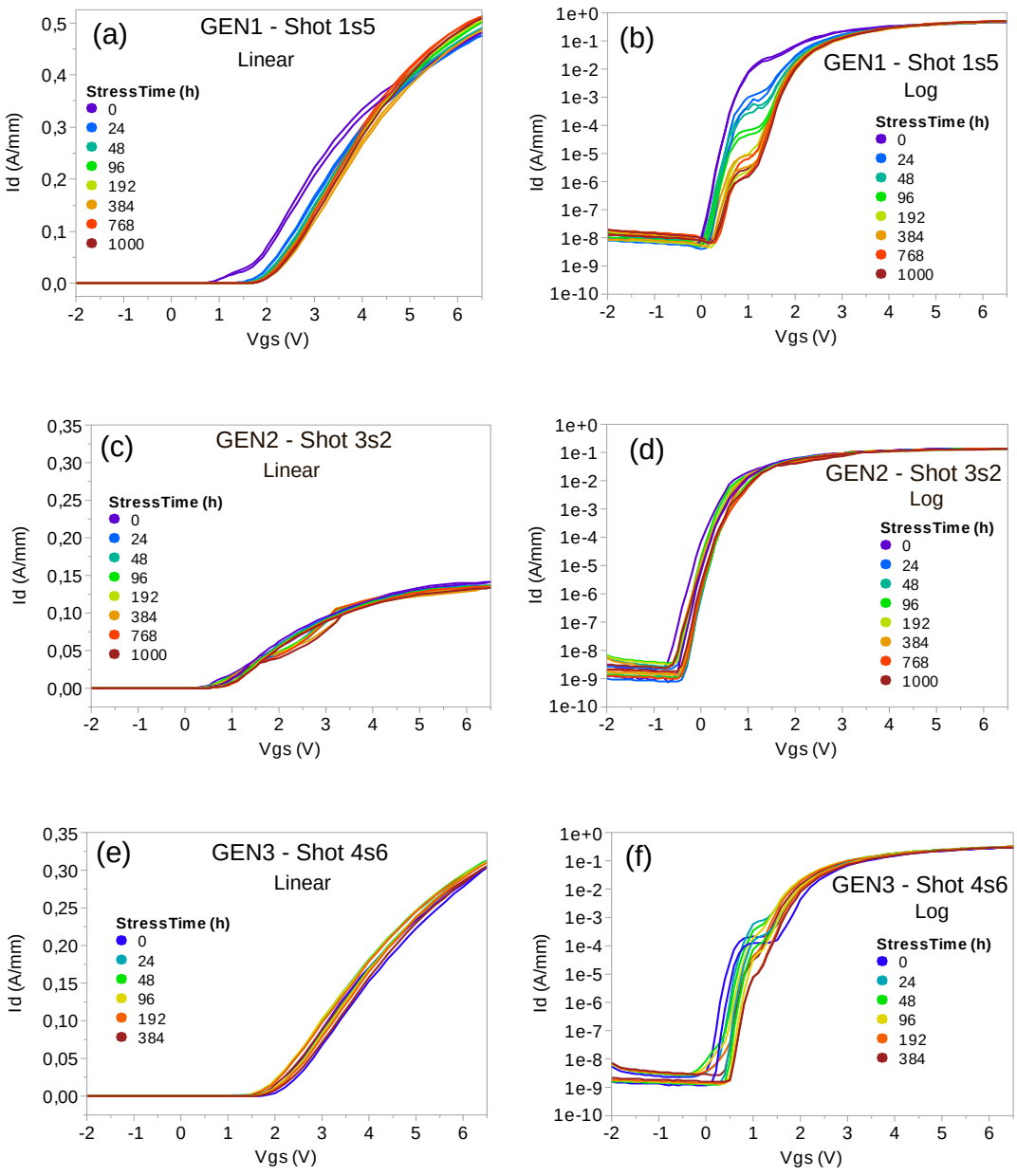


Figure 5.23: Transfer characteristics I_D-V_G variation during the stress for a representative sample of GEN1 (a) and (b), one of GEN2 (c) and (d), and one of GEN3 (e) and (f) technologies. The drain voltage was $V_D = 10\,V$.

This measurements have been acquired with a forward-backward system, i.e. the voltage span from negative to positive values and then comes back; thus in the graphs are reported two curves with the same color, one for the forward an another for the backward direction. We reported both of them in order to show the hysteresis.

In the case of GEN1 we can observe the generation of a hump in the log-scaled plot (see Figure 5.23 (b)). A similar behaviour is present even in GEN3 samples, while in GEN2 the phenomenon is limited and masked by the hysteresis. It has to be noticed that devices of the same technology show a similar but not homogeneous behaviour. The origin of the hump in subthreshold is still not clear, but we can observe how the drain voltage influences this phenomenon in Figure 5.24. After the 1000 hours of stress, a GEN1 device has been characterized with different drain voltages from 0.1 V to 10 V; it is evident that the hump appears only for $V_D > 2\,V$. The off-state leakage dependence on the drain voltage is instead ascribable to the drain-induced barrier lowering (DIBL) effect (at higher drain voltages the pinch-off of the channel becomes less effective). Looking carefully at the graph of Figure 5.23 (b) we can observe that the hump was already noticeable before the stress, like a small curve imperfection, and then it starts to move during the stress. A similar behaviour is observed when in the device

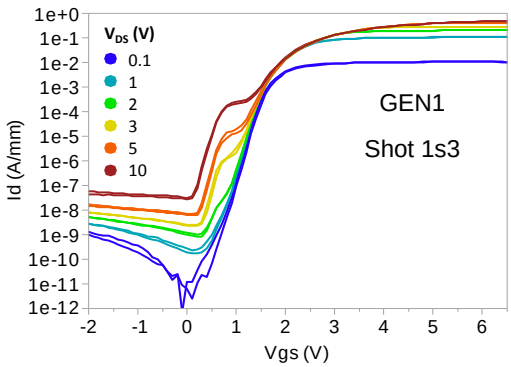


Figure 5.24: Transfer characteristics I_D-V_G taken after the stress for a sample of GEN1 technology. The drain voltage goes from $V_D = 0.1\,V$ to $V_D = 10\,V$.

there is a parasitic path with a different threshold voltage that modulates part of the channel. However, this implies some lateral inhomogeneity that changes during stress, and we do not think that is the case here. It is more likely that the hump originates from distribution of defects at the p-GaN/AlGaN interface, or in the barrier, since this is the more critical area that modulates the current in sub-threshold. This is not the first time that such a hump is reported, but it has been observed on several p-GaN technologies, even in some former sample analysed within the *Hiposwitch* project. This is a clue that it could be related to some crucial aspect of the p-GaN layout, even though for the moment we cannot speculate more about.

In Figure 5.25 is reported the evolution of the gate current I_G-V_G character-

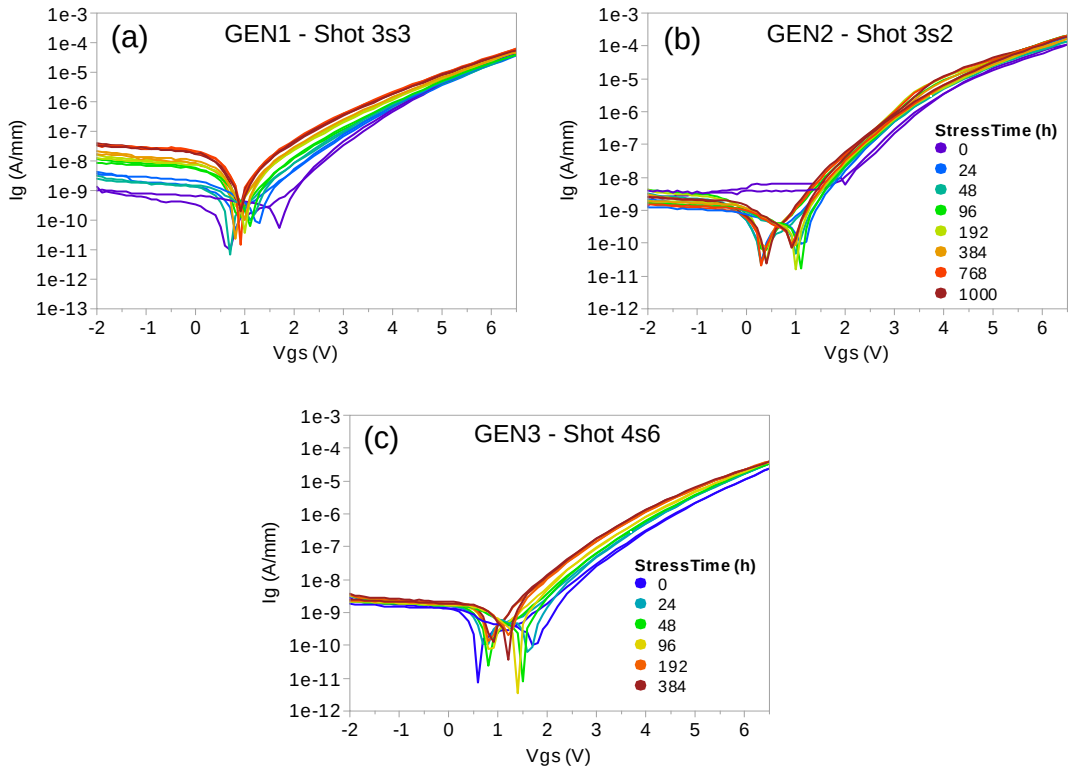


Figure 5.25: Gate leakage I_G-V_G variation during the stress for a representative sample of GEN1 (a), one of GEN2 (b), and one of GEN3 (c) technologies. The drain voltage was $V_D = 10\,V$.

ized for $V_D = 10V$. We can observe a trend similar to the GS-diode, with some differences. The point where the leakage current reverses is around $V_G = 1\,V$, with some differences for the forward and backward curve. For $V_D = 10V$ the potential under the gate is not zero, but a positive value that depends on the voltage drop from the drain to the source (that changes with the material conductivity and device geometry).

We can observe, that in on-state there is a moderate leakage increase, that represents the non-recoverable degradation of the gate leakage during the stress. In Figure 5.26 is presented a comparison between the variation of the gate leakage during the stress and the value of I_G measured in the intermediate characterizations at $V_G = 5\,V$, $V_D = 10\,V$. The graphs of Figures 5.26 (a) and (b) have the same I_G range, and is thus possible to observe that the permanent leakage degra-

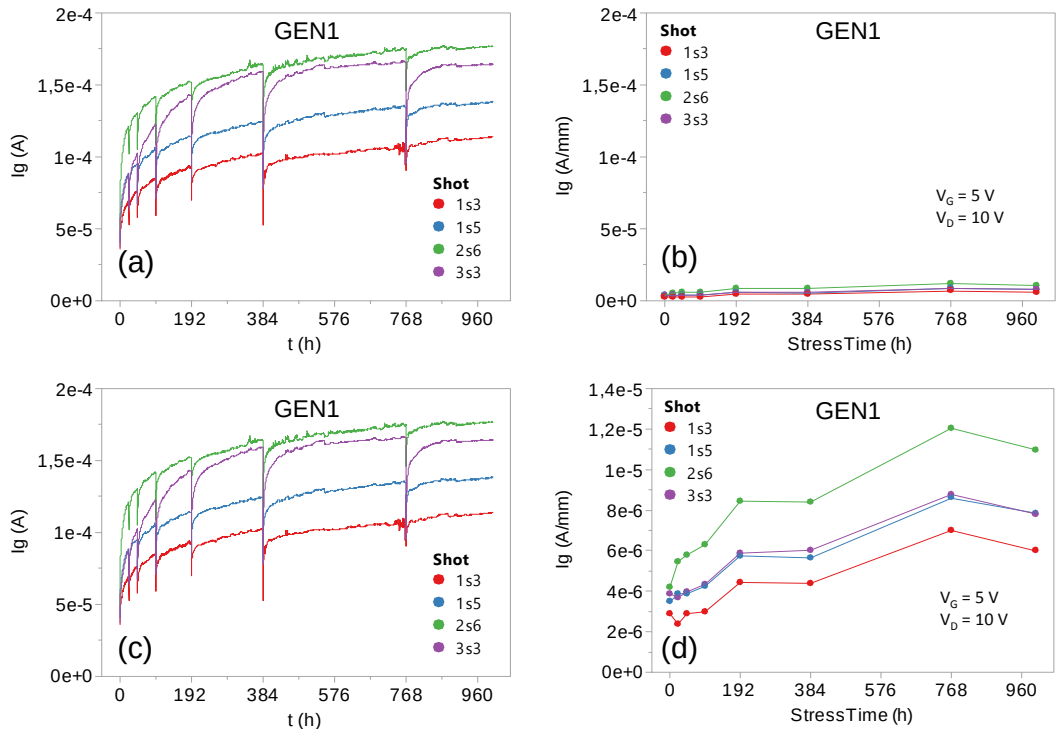


Figure 5.26: Gate current I_G variation during the stress for GEN1 (a) and (c) compared to the values of I_G measured during the characterizations for $V_G = 5\,V$, $V_D = 10\,V$ (b) and (d).

dation is negligible if compared with the stress one. This confirms that most of the gate current increase during the stress is ascribable to trapping phenomena. However, if we expand the range of the graph in Figure 5.26 (b) we can observe, in Figures 5.26 (c) and (d), that the two current trends over time are very similar.

This correlation holds even for the technologies GEN2 and GEN3, as we can see in the graphs of Figure 5.27. It is possible that both the permanent gate leakage degradation and the recoverable trapping have the same origin. It is even possible that something causes the permanent degradation, that in turn induces the trapping, or vice versa; in principle we cannot exclude any hypothesis. The degradation should be anyway located in the AlGaN region or nearby, since the gate current in forward is modulated by the barrier. However, few works in literature explain the conduction mechanism of the gate leakage current for p-

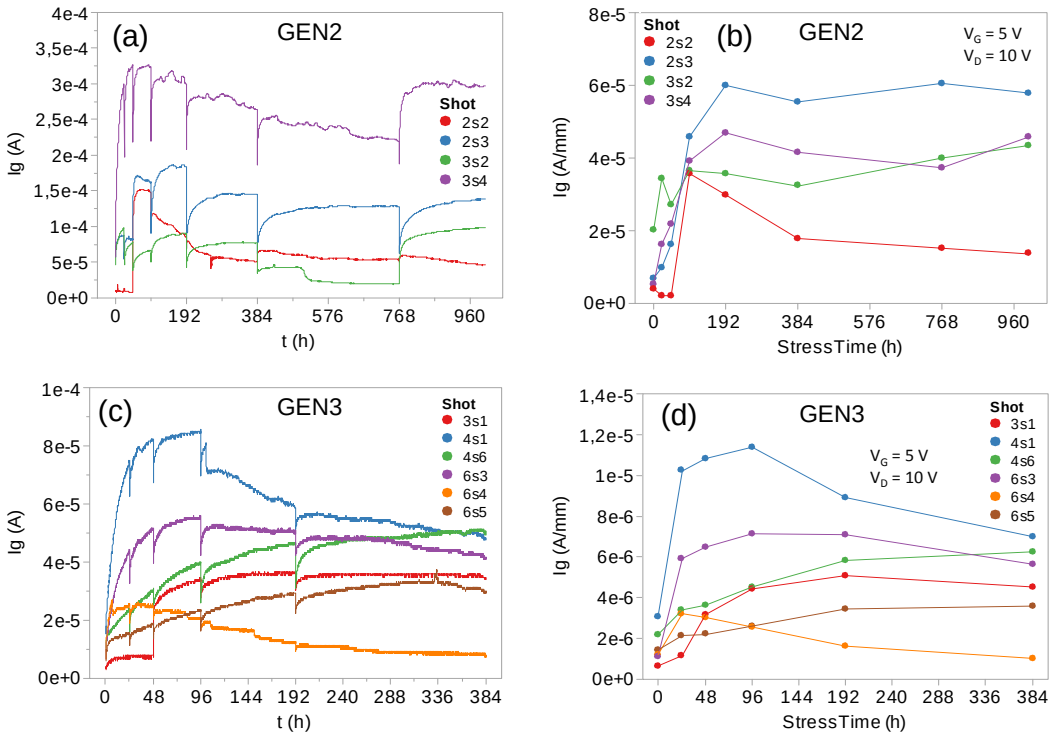


Figure 5.27: Gate current I_G variation during the stress for GEN2 (a), and for GEN3 (c), compared to the values of I_G measured during the characterizations for $V_G = 5\,V$, $V_D = 10\,V$, on a GEN2 sample (b) and a GEN3 (d).

GaN devices, and without a clear knowledge about, it is hard to understand the degradation mechanisms.

In order to analyse the dynamics of the leakage increase during the stress we considered some of the more regular curves and we fitted them with a stretched exponential function of the form $\sim \exp(-t/\tau)^{\beta}$. We can see the results in Figure 5.28 with a sample for each device generation. The fitting times for GEN2 and GEN3 are lower than 1000 h because then the trend changes, and we are more interested in the first, more regular, part.

The fitting has been done on all the cases where it was sensible; the numerical fitting results are reported in Table 5.3. From this data we can notice that the time constants τ for GEN2 and GEN3 are faster that for GEN1, and this is not easy to estimate only looking at the plots. Then, the stretching parameter β is

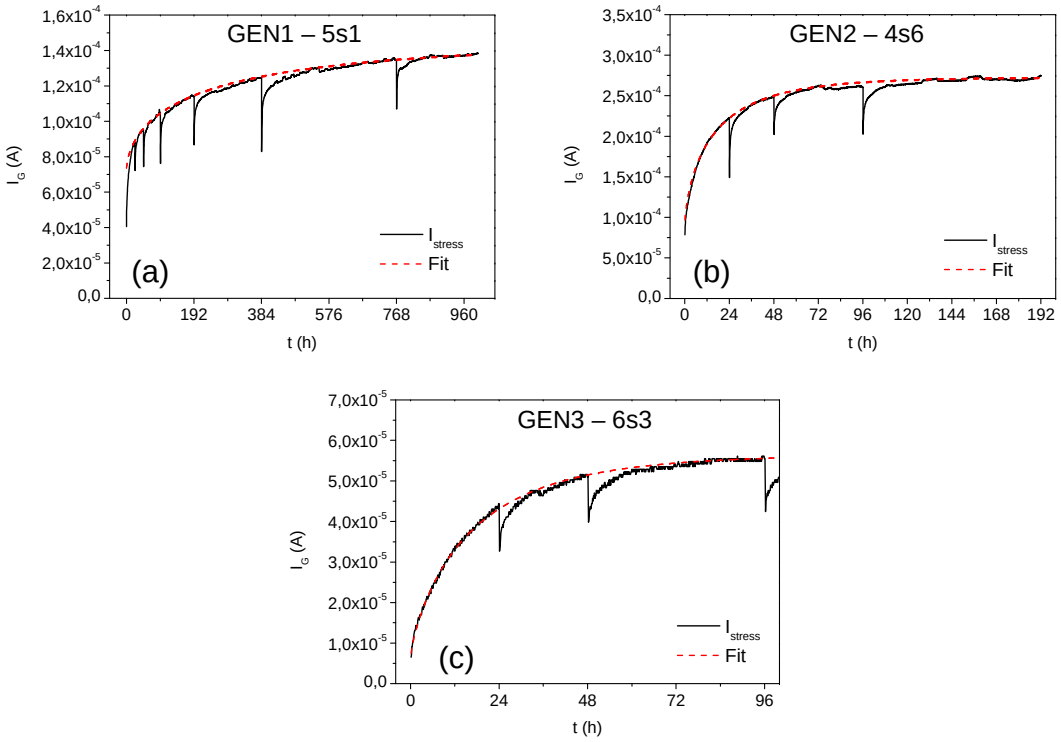


Figure 5.28: Stretched exponential fitting of the gate current I_G variation during the stress for: (a) a GEN1 sample up to 1000 h; (b) a GEN2 sample up to 192 h; (a) a GEN3 sample up to 96 h.

lower for GEN1 samples, higher for GEN2, and even higher for GEN3. Low β values represent an exponential process that is stretched along the time axis, as noticeable in the graphs of Figure 5.28; in the case of GEN1 sample the shape is obviously different from a not-stretched exponential, with $\beta = 1$. If β reaches values close to zero the function is more similar to a step than to an exponential. This data cannot give us specific information about the trapping mechanism, but the value of the time constants and the stretching parameter represent a signature that allows to compare different technologies.

It would be interesting to analyse even the dynamic of the gate current increase after each time the stress restarts. The procedure is the same as before, but we take for brevity only some step for one sample of each technology. The results are summarized in Table 5.4, while in the graphs of Figure 5.29 is reported the fitting for the GEN1 sample at three different times. In this case the values of τ and β are more homogeneous, but with very low β, indicating that the trapping dynamic is not the same if we consider each step instead of the whole stress.

Table 5.3: Parameters for the stretched exponential fitting of the gate current trend during several steps of the stress.

Technology	Device	Fitting range (h)	τ (h)	β
GEN1	1s3	1000	190	0.55
GEN1	2s6	1000	190	0.60
GEN1	1s5	1000	250	0.57
GEN1	3s3	1000	120	0.84
GEN2	4s6	192	17	0.70
GEN2	5s7	96	16	0.70
GEN3	4s1	96	13	0.95
GEN3	4s1	96	17	0.80

Table 5.4: Parameters for the stretched exponential fitting of the gate current trend during some steps of the stress. The fitting time is 4 hours.

Technology	Device	Fitting start (h)	τ (h)	β
GEN1	1s5	24	0.10	0.35
GEN1	1s5	48	0.10	0.33
GEN1	1s5	192	0.16	0.43
GEN2	4s6	24	0.18	0.30
GEN2	4s6	48	0.19	0.35
GEN3	5s7	24	0.30	0.40
GEN3	5s7	48	0.16	0.37

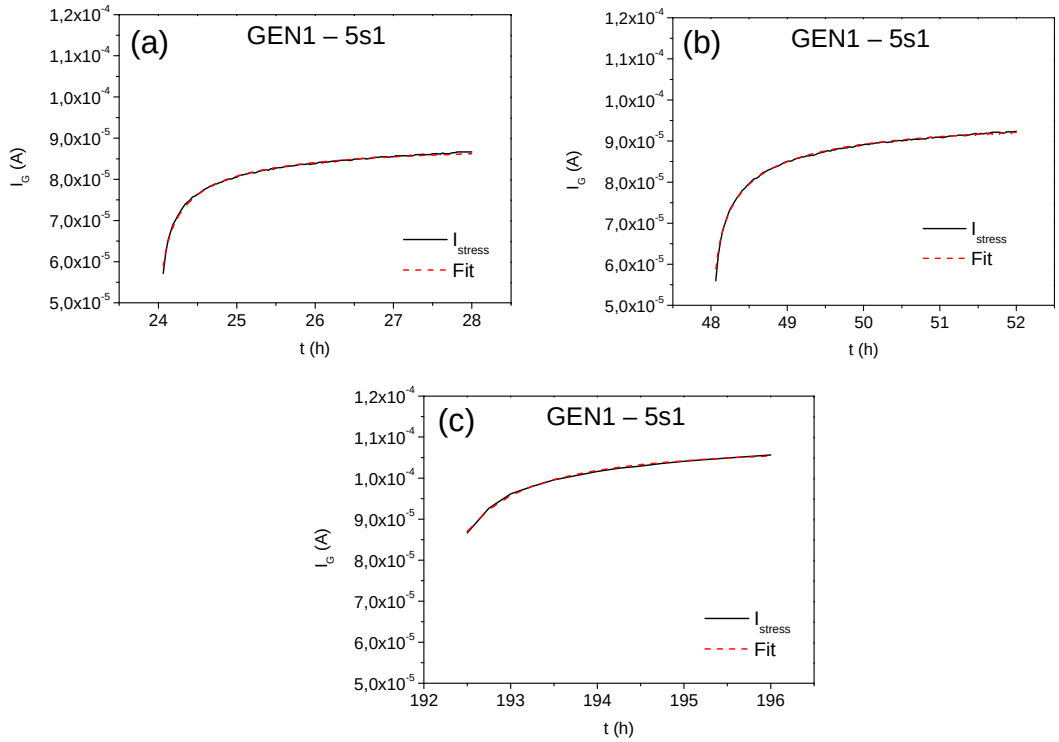


Figure 5.29: Stretched exponential fitting of the gate current I_G variation during the first 4 hours of some steps of the stress of a GEN1 sample; the starting time are: 24 h (a), 48 h (b), and 192 h (c).

Gate leakage current analysis

One of the few works that makes a comprehensive analysis of the gate leakage current in p-GaN HEMTs is from *Bae et al.* [110]. We would try to verify if their models hold even in our case, with the purpose to add further information to the leakage mechanism of p-GaN HEMTs. However, the p-GaN structures developed in different locations are not all the same, and they can present differences in the metal contact on the p-GaN and/or in the thickness and quality of the AlGaN layer. For this reason some results cannot be completely comparable, but we need to concentrate on the similarities and on the distinctive device features.

For the leakage current analysis we taken two fresh devices, one for the technology GEN1 and another for GEN2. The GS-diode current measurements have been performed either in backward and forward bias, from $V_G = -20\,V$ to $V_G = 7\,V$ (see plots in Figure 5.30). The drain voltage was kept to 0 V, while the temperature range spans from 30°C to 150°C with step of 30°C.

For the sake of clarity we report also two simulated band diagrams at the gate biases of $V_G = 5\,V$ and $V_G = 1.5\,V$ (see respectively Figure 5.31 (a) and (b)). From the band diagram at $V_G = 1.5\,V$ we can observe that there is still a barrier around 1.5 eV for both electrons and holes, thus, the current cannot cross the barrier, and must follow a different path. This observation holds indeed in off-state, where the barrier is even higher ($\approx 2\,eV$). The hypothesis proposed in [110] is that the conduction mechanism is the electron hopping through AlGaN surface states, as already reported by *Kotani et al.* [124]. The model is the two-dimensional variable range (2D-VRH) taken from a book of Mott [125]; the temperature dependence of the conductivity based on the 2D-VRH model is: $\sigma(T) \propto \exp[-(1/T)^{1/3}]$. However, fitting the data in the paper of *Kotani* the relationship is not so clear, since they fit as well with a temperature dependence of the form $\sigma(T) \propto \exp[-(1/T)]$, assuming the current proportional to the conductivity; the estimated activation energy is of 0.5 eV.

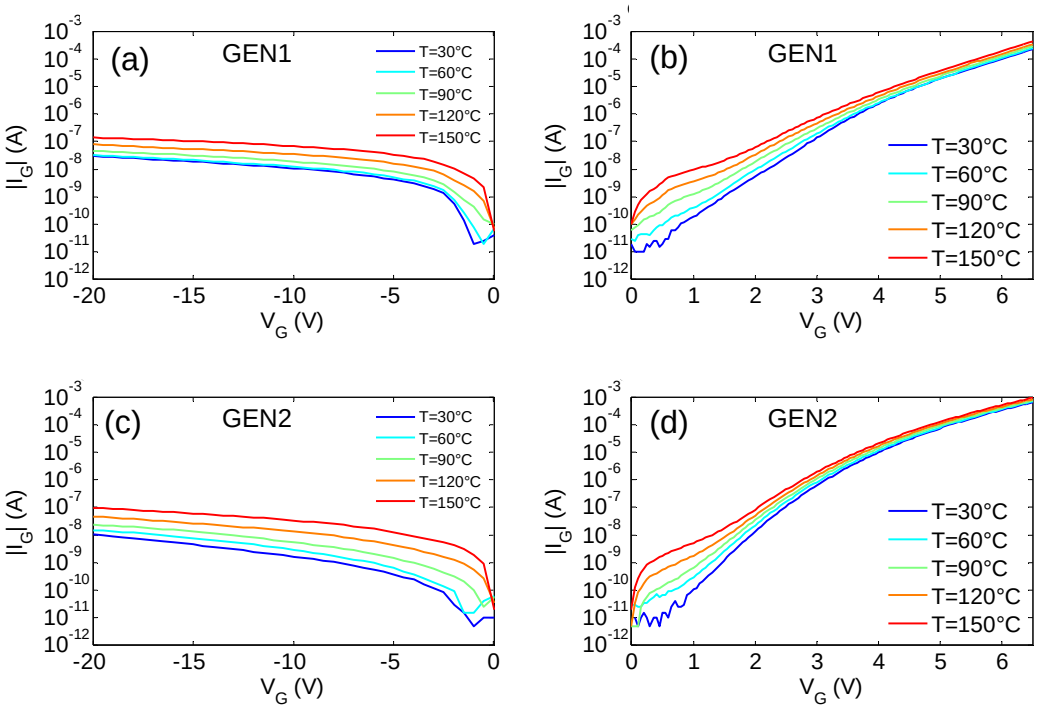


Figure 5.30: GS-diode current measured from $V_G = -20\,V$ to $V_G = 7\,V$ in the temperature range 30°C-150°C; I_G of a GEN1 device in backward (a) and forward bias (b); I_G of a GEN2 device in backward (c) and forward bias (d).

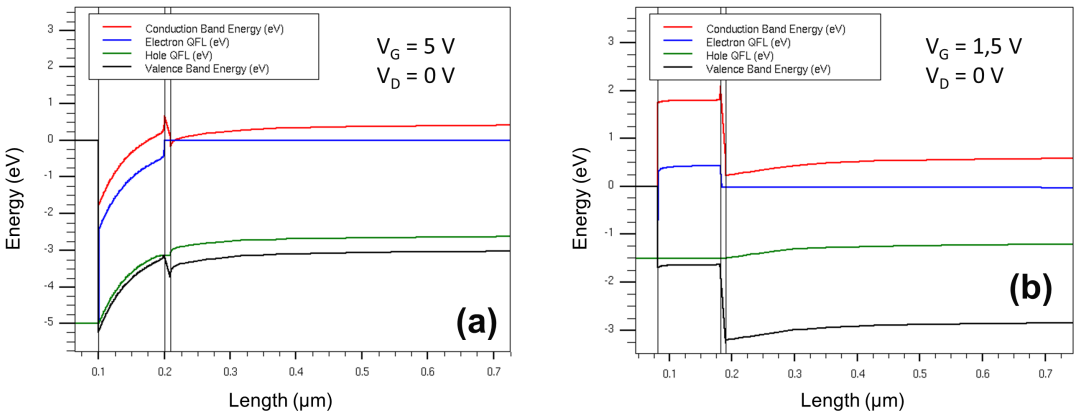


Figure 5.31: Simulated band diagram vertical cutline in two different bias conditions: (a) $V_G = 5\,V$, $V_D = 0\,V$; (b) $V_G = 1.5\,V$, $V_D = 0\,V$.

In Figure 5.32 is reported the activation energy E_a versus the gate voltage, for the diode measurements showed above. We can observe that the trend is similar for both technologies GEN1 and GEN2. We can assume that even in our devices the off state leakage is ascribable to hopping through AlGaN surface states. In principle we cannot exclude that the observed activation energy for the reverse current is relate to the hopping process itself, but in that case E_a should be constant over the whole gate voltage sweep. Thus, is more likely that the observed activation energy is related to the barrier at the metal/p-GaN contact. We already proposed this hypothesis in the chapter of the simulations and this measurements seems to confirm it. Looking at the plots of Figures 5.32 (a) and (c) we can observe that in the range of V_G from 0 V to −3 V there is a barrier around 0.2 eV; for more negative voltages the barrier is lowered by the applied bias and the holes can be easily injected from the gate contact.

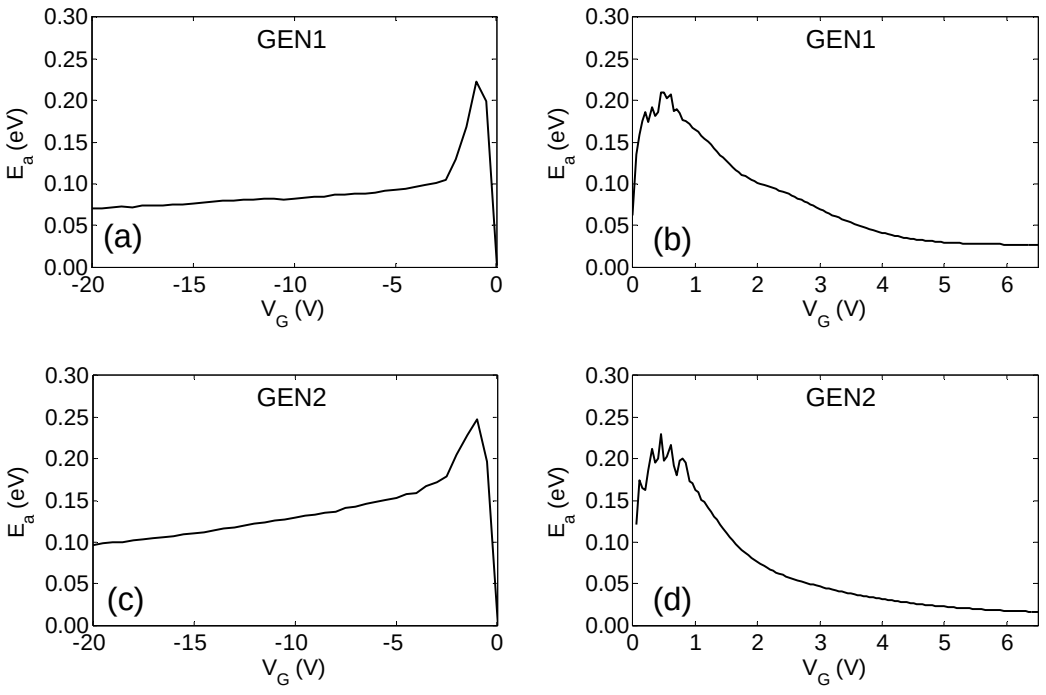


Figure 5.32: Activation energy E_a vs. gate bias V_G of the GS-diode current for a GEN1 device in backward (a) and forward bias (b), and for a GEN2 device in backward (c) and forward bias (d).

In forward bias, for $V_G < 2$ V the situation is similar (see Figures 5.32 (b) and (d)), but then, the activation energy value drops. In this case we expected a stable value of barrier height, since the junction metal/pGaN is in reverse bias. A possible explanation is that for $V_G > 2$ V it starts another conduction mechanism, that becomes dominant increasing the gate bias. The activation energy of this second mechanism is very low ($\approx$ 30 meV for $V_G = 5$ V). This mean that the conduction mechanism is weakly thermally activated and could not be ascribed to a thermionic emission.

From the simulations we observed that for $V_G = 5$ V, the estimated electron concentration in the p-GaN is five orders of magnitude higher than the holes one in the Gan-channel and the differences in the recombination rate is even higher. This means that the bipolar junction divided by the AlGaN barrier is asymmetric, since there are more injected electrons that holes. The electrons injected from the channel into the p-GaN recombines with the holes that come from the gate. We need to point out that the simulated gate leakage current started only for $V_G > 3$ V, but the adopted model was that one of thermionic emission of electrons from the 2DEG into the p-GaN, when the barrier is lowered. The activation energy of the leakage current indicates that maybe there is some other dominating mechanism that cover the thermionic emission. I have tried to implement several built-in simulation models to find an alternative conduction mechanism, but all them failed. The low activation energy of the process suggests the presence of some kind of tunnelling process; a direct tunnelling is possible, at least over gate voltages that lower enough the barrier. However, since for GEN1 the AlGaN thickness is 9 nm, and for GEN2 is 15 nm, we expect to see some differences in either forward currents trend, instead they are very similar. But we cannot exclude it at all, since the simulated barrier has a triangular shape and even a Fowler-Nordheim mechanism is plausible. Then, I have tried to apply several models that works for reverse biased Schottky junctions (and not only), like the trapping-assisted tunnelling [126], multiphonon-assisted tunnelling [127] and Poole-Frenkel effect [128]. However, they cannot be applied in our case, since

the electric field in the AlGaN barrier points toward the p-GaN, and with all these model the tunnelling probability, that is influenced also from the electric field, is higher in the opposite direction, i.e. toward the channel.

The more likely explanation comes again from the work of *Bae et al.* [110], since they demonstrate the existence of percolation paths in the barrier, generated by Ga-rich regions in the AlGaN layer. Furthermore, *Nath et al.* [129] show experimentally and by means of simulations the role of random fluctuations of Al-composition in the AlGaN on the percolation-based charge transport. Even for GaN-based LED, *Wu et al.* [130] reported a percolation transport study considering random alloy fluctuation.

If we assume that the main conduction mechanism of the forward gate leakage current of p-GaN HEMTs (at least for $V_G = 5$ V) is based on percolation mechanism we can list some observations:

- The permanent current increase observed during the on-state stress could be ascribable to an increase in the number and/or the size of the percolation paths. Since the recoverable leakage increase during the stress has a correlation with the permanent one, it is likely that the induced trapping mechanism is originated in the AlGaN layer. Holes captured in the barrier can connect momentarily some percolation paths that were not covering all the barrier thickness. When the forward bias is removed the holes in the AlGaN are emitted and the current level comes back to a value close to the initial one. However, it is possible that some percolation paths remain permanently open, leading to a not-recoverable leakage increase. The observed correlation between recoverable and non-recoverable degradation can be ascribed to this common mechanism, that could be related to the difference in percolation paths concentration among the devices. This hypothesis can even explain some sudden and anomalous change of the leakage current observed in some devices.

- The thermionic emission of electrons from the channel, and holes from the p-GaN is not absent, but it could be only a secondary mechanism, since

the simulated one at $V_G = 5$ V is one order of magnitude lower than the measured one. This indicates that the thermionic emission could be masked by the main conduction mechanism, with the proposed percolation model. However, if during the stress some positive charge accumulates at the interface between p-GaN and AlGaN it can lower the barrier and increase the contribute of the thermionic emission. In principle we cannot say which is the dominant mechanism responsible of the leakage increase, both hypothesis are plausible.

- The key role of trapping phenomena located in the AlGaN layer has been recently demonstrated by *Li et al.* [131]. In this case they noticed changes in the on-resistance after an on-state stress, confirming again that the barrier is one of the most critical region of the device.

- The percolation paths model for the forward leakage current can be a step forward in the explanation of the failure mechanisms of the p-GaN devices submitted to high gate forward bias. The role of percolation paths has already been demonstrated for AlGaN/GaN HEMT Shottky junction in reverse bias [74]; in that case the high electric field in the barrier plays a key role in the degradation mechanism. In our case the electric field in the barrier is very low, but as proposed above even the effects of forward bias can be detrimental. Ťapajna *et al.* [132][133] proposed the percolation paths as possible mechanism for the time dependent breakdown in forward bias. It is worth noticing that the analysed technology of that work is very similar to the one of my stresses, even developed by FBH. Recently, other mechanisms have been proposed for the time dependent breakdown in forward bias [40][134]; in these works it is supposed that the breakdown append in the p-GaN. This is an interesting hypothesis, that explore an alternative explanation for the breakdown. However, we must always pay attention when we compare different p-GaN technologies, since some differences in the device structure could lead to different operation mode and degradation mechanisms.

- In order to decrease the effects of the percolation path is possible to try to improve the quality of the AlGaN layer, if it is feasible.

As conclusion we can stress again that the AlGaN barrier should always be take in consideration as a pivotal point, since it has a blocking function for the forward gate current, independently of the conduction mechanism. It is obvious that when we see a degradation of the leakage current, we think immediately at some change in the barrier. But without the knowledge of the conduction mechanism we cannot formulate sensible hypothesis. We propose the percolation model as the more likely, and we showed how it can explain the leakage increase during the on-state stress. However, if we go beyond the operative gate voltage to investigate the reliability, other mechanisms can be responsible of the device breakdown. Finally, we demonstrated how physical-based simulations can be a powerful investigation instrument, that helps us to validate hypothesis and models.

Conclusions

During my PhD I have had the opportunity to work both on RF and power GaN-based HEMTs. In this way I was able to observe some similarities, since the structures are based on the same material, and even the differences, related to the different operation and applications of the two technologies. Within this thesis, I have tried to give an overview of the main issues and achievements obtained. It was not possible to cover all the analysis carried out in the three years, nevertheless the reported works are a complete summary of the more relevant results. We have seen, in particular for power devices, how it was possible to observe outstanding improvements only in one-two years span. This was possible thanks to the joint efforts from companies, universities and research centres. The feedback and advice we have given to the companies demonstrated to be fundamental in the development process.

In Chapter 2 we have seen how in the last two years, the reported device performances have been improved, on both RF and power devices. The environmental monitoring satellite from the European Space Agency, *Proba V*, is working since May 2013, sending the telemetry data with a GaN HEMT-based amplifier. This is a demonstration that GaN-based technology is ready for space applications.

Concerning the simulations, we have seen how it can be hard tu build an effective model for a GaN-based HEMTs. Unlike Silicon, there is not so much experience in the simulation of GaN-based devices, nevertheless in the last years a lot of improvements have been made. Since Silicon is grown with a very low defectivity, it could be approximate with a perfect crystalline structure, and the

models improved in simulators represent accurately the real situation. For Gallium Nitride instead the crystal defectivity is higher, and several trap states lie in the bandgap. Thus the simulations are more difficult, and some aspects, related to the material defectivity are not yet implemented in an accurate model. However, we have seen that with a first order simplified model we can gather a lot of central information. Physical based simulations demonstrated to be an indispensable and complementary instrument, even for GaN-based transistors.

For RF devices, two different technologies (GH50 and GH25) have been submitted to reliability tests, within the ESA project *"Preliminary Validation of Space Compatible Foundry Processes"*. The results show the high performance stability of both two processes, even under severe stress conditions. The identification of the failure modes was difficult, since to observe some device degradation it was necessary to push the devices in high temperature and high power dissipation conditions. However, the large amount of tests allows us to draw some conclusions.

The GH50 technology demonstrates to exceed the target life time of 20 years at the operative temperature of 230°C. The only exception was the RF life test, where some devices reach the failure criterion before the end of the 500 hours. We do not know the activation energy of this process, thus is difficult to estimate the life time. But in the RF tests we noticed a correlation between the Rf performances drop and the leakage increase. At high temperatures, all the long term tests show a parabolic trend of both the gate leakage and the threshold voltage, that could be ascribed to the degradation of the gate Schottky barrier.

Even though the scaling of the gate length, the GH25 technology show comparable or even better performances that the GH50 devices. Only the life time extracted for the leakage increase during thermal storage is of 29 years, while the others are higher. The observed degradation mechanism during the life tests are similar to the GH50 technology. Only in the RF life test the GH25 samples shown a RF performance degradation that was the half in comparison to the GH50. In conclusion not all the failure mechanisms are clear, but it is possible

that some metal interdiffusion in the gate stack can explain both the variation of threshold voltage and leakage increase. The extrapolation of the device life time can be difficult, since not all the degradation mechanisms are accelerated only by temperature, but even the power dissipation and the drain voltage level (or their combined effect) can play a fundamental role in the failure dynamic.

Regarding the GaN-based HEMTs for power switching applications, we have seen how for MIS-devices the collaboration with *ON Semiconductor* results in an improvement of the device performance. During these three years we mainly focused on the dynamic-R_{ON} and on the threshold voltage shift during off-state conditions. We proposed a set of tests that allows to verify the device stability under high temperature conditions. In particular, we demonstrated a new test methodology that mimics the real operative conditions of the d-mode HEMTs in cascode configuration. This new kind of test shows how the last device generations are stable, both in term of on-resistance and threshold voltage. Thus, this technology is ready to afford the market of 600 V-rated power switching transistors. The next step will be to improve the test setup, in order to test the device in switching conditions, to better emulate the real device operation. In this way we could estimate even the effects of the different gate driving like hard-switching and soft-switching.

In the last part, we have seen the analysis carried out on the p-GaN power HEMTs, by FBH, in Berlin. This tests, joined with the relative simulation results allow us to investigate one of the big issue of this technology: the gate leakage in forward bias. By means of on-state accelerated life test we proposed a model for the conduction mechanisms, that confirm some hypothesis found in literature. We show how a percolation-based conduction mechanism through the AlGaN layer can explain both the experimental GS diode measurements and the observed degradation mechanism. This is a fundamental discovery for the process developers, since they know which is the more critical device area.

List of Publications

Journal papers

1. A. Stocco, S. Gerardin, D. Bisi, S. Dalcanale, F. Rampazzo, M. Meneghini, G. Meneghesso, J. Grünenpütt, B. Lambert, H. Blanck, E. Zanoni, "Proton induced trapping effect on space compatible GaN HEMTs", *Microelectronic Reliability*, vol. 54, pp. 2213-2216, 2014.

2. A. Stocco, S. Dalcanale, F. Rampazzo, M. Meneghini, G. Meneghesso, J. Grünenpütt, B. Lambert, H. Blanck, E. Zanoni, "Failure signatures on 0.25 μm GaN HEMTs for high-power RF applications", *Microelectronic Reliability*, vol. 54, pp. 2237-2241, 2014.

3. M. Meneghini, P. Vanmeerbeek, R. Silvestri, S. Dalcanale, A. Banerjee, D. Bisi, E. Zanoni, G. Meneghesso, P. Moens, "Temperature-Dependent Dynamic R_{ON} in GaN-Based MIS-HEMTs: Role of Surface Traps and Buffer Leakage", *Transaction on Electron Devices*, vol. 62, n. 3, pp. 782-787, 2015.

4. M. Meneghini, O. Hilt, C. Fleury, R. Silvestri, M. Capriotti, G. Strasser, D. Pogany, E. Bahat-Treidel, F. Brunner, A. Knauer, J.Würfl, I. Rossetto, E. Zanoni, G. Meneghesso, S. Dalcanale, "Normally-off GaN-HEMTs with p-type gate: Off-state degradation, forward gate stress and ESD failure", *Microelectronic Reliability*, vol. 58, pp. 177-184, 2016.

5. I. Rossetto, M. Meneghini, O. Hilt, E. Bahat-Treidel C. De Santi, S. Dalcanale, J. Würfl, E. Zanoni, G. Meneghesso, "Time-Dependent Failure of GaN-on-Si Power HEMTs With p-GaN Gate", *Transaction on Electron Devices*, vol. 63, n. 6, pp. 2334-2339, 2016.

Conference Proceedings

1. S. Dalcanale, A. Stocco, F. Rampazzo, M. Meneghini, G. Meneghesso, E. Zanoni, "Reliability improvement of AlGaN/GaN HEMTs for space applications", 38^{th} *Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE 2014)*, pp. 127-128, 15-18 Jun 2014, Delphi - Greece.

2. A. Stocco, S. Dalcanale, F. Rampazzo, M. Meneghini, G. Meneghesso, J. Grünenpütt, B. Lambert, H. Blanck, E. Zanoni, "Simple technique for failure modes detection on high-performances space designed GaN HEMTs", 7^{th} *ESA Wide Band Gap Semiconductors & Components Workshop*, 11-12 Sep 2014, Frascati - Italy.

3. I. Rossetto, M. Meneghini, O. Hilt, E. Bahat-Treidel, J. Würfl, R. Silvestri, S. Dalcanale, E. Zanoni, G. Meneghesso, "Experimental Demonstration of Weibull Distributed Failure in p-type GaN High Electron Mobility Transistors under high forward bias stress", 28^{th} *International Symposium of Power Semiconductor Devices and ICs (ISPSD 2016)*, pp. 35-38, 15-18 Jun 2016, Prague - Czech Republic.

4. E. Zanoni, S. Dalcanale, A. Stocco, F. Rampazzo, M. Meneghini, G.Meneghesso, A. Chini, G. Verzellesi, J. Grünenpütt, B. Lambert, and H. Blanck "A comprehensive reliability evaluation of high-performance AlGaN/GaN HEMTs for space applications", 8^{th} *ESA Wide Band Gap Semiconductors & Components Workshop*, 12-13 Sep 2016, Harwell - United Kingdom.

Acronyms

2DEG	Two Dimensional Electron Gas
4H-SiC	4H crystalline polytype of Silicon Carbide
Al	Aluminium
Al_2O_3	Aluminium Oxide / Sapphire
AlN	Aluminium Nitride
Au	Golden
AlGaN	Aluminium and Gallium Nitride
CF_4	Tetrafluoromethane
CAVET	Current Aperture Vertical Electron Transistor
DCT	Drain Current Transient
DEC	Dynamic Evaluation Circuit
DIBL	Drain Induced Barrier Lowering
DLTS	Deep Level Transient Spectroscopy
EL	Electro-Luminescence
FATFET	Large area Schottky diode
Ga	Gallium
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GC	Gain Compression
GS	Gate-Source
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
HFET	Heterostructure Field Effect Transistor

HTRB	High Temperature Reverse Bias
HTSC	High Temperature Source Current
InAlN	Indium Aluminium Nitride
InGaN	Indium Gallium Nitride
InP	Indium Phosphide
JM	Johnson's figure of Merit
MIS	Metal-Insulator-Semiconductor
Mg	Magnesium
MMIC	Monolithic Microwave Integrated Circuit
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MTTF	Mean Time-to-Failure
N	Nitrogen
NBTI	Negative Bias-induced Threshold voltage Instability
Ni	Nickel
NiO	Nickel Oxide
p-GaN	p-doped Gallium Nitride
PAE	Power Added Efficiency
PBTI	Positive Bias-induced Threshold voltage Instability
PCM	Process Control Monitoring
Pd	Palladium
Pt	Platinum
RF	Radio Frequency
Si	Silicon
SiC	Silicon Carbide
SIMS	Secondary Ion Mass Spectrometry
SiN	Silicon Nitride
SR	Slump Ratio
Ti	Titanium
TLM	Transfer Length Model
TTF	Time-to-Failure

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