



UNIVERSITÀ
DEGLI STUDI
DI PADOVA

Sede Amministrativa: Università degli Studi di Padova

Dipartimento di Ingegneria dell'Informazione

SCUOLA DI DOTTORATO DI RICERCA IN INGEGNERIA DELL'INFORMAZIONE

INDIRIZZO: SCIENZA E TECNOLOGIA DELL'INFORMAZIONE

CICLO: XXVIII

Control of Electronic Power Converters for Low-Voltage Microgrids

Direttore della Scuola: Ch.mo Prof. Matteo Bertocco

Coordinatore di Indirizzo: Ch.mo Prof. Carlo Ferrari

Supervisore: Ch.mo Prof. Paolo Tenti

Co-supervisore: Ch.mo Prof. Simone Buso

Dottorando: Tommaso Caldognetto

Contents

| | |
|---|--------------|
| List of Acronyms | vii |
| List of Figures | xi |
| List of Tables | xvii |
| Abstract | xix |
| Sommario | xxiii |
| Acknowledgments | xxvii |
| 1 Introduction | 1 |
| 1.1 Investigated Aspects and Contribution | 5 |
| 1.1.1 Microgrid Architecture | 5 |
| 1.1.2 Current Controllers for Grid-Tied Converters | 6 |
| 1.1.3 Control Algorithm for DERs Interfacing Converters | 7 |
| 1.1.4 Control of Voltage Profiles | 8 |
| 1.2 Dissertation Outline | 9 |
| 2 Control in Smart Microgrids: State-of-the-Art | 13 |
| 2.1 Control Hierarchy | 15 |
| 2.2 Zero-level Control | 18 |
| 2.2.1 Linear Control | 19 |
| 2.2.2 Predictive Control | 22 |

| | | |
|----------|--|-----------|
| 2.2.3 | Hysteresis Control | 24 |
| 2.3 | Primary Control | 25 |
| 2.3.1 | Converters Behaviour | 26 |
| 2.3.2 | Controllers for Enhanced Power Quality | 31 |
| 2.4 | Secondary Control | 37 |
| 2.4.1 | Operation of Parallel Connected Converters | 37 |
| 2.4.2 | Coordination of Power Contributions | 40 |
| 2.5 | Tertiary Control | 42 |
| 2.5.1 | Microgrid Synchronization | 42 |
| 2.5.2 | Detection of Islanded Operation | 44 |
| 2.5.3 | Power Flow Scheduling with the Mains | 45 |
| 2.6 | Summary | 46 |
| 3 | Development Methodology and Toolset | 47 |
| 3.1 | Controllers for EPPs in the Microgrid Scenario | 48 |
| 3.2 | System Architecture and Implementation Tools | 50 |
| 3.2.1 | Control System Organization | 51 |
| 3.2.2 | Implementation Issues | 52 |
| 3.2.3 | User Interface | 57 |
| 3.3 | Controller Development and Test Methodology | 58 |
| 3.3.1 | Simulink Model | 60 |
| 3.3.2 | Hardware-In-the-Loop Real-Time Simulation | 61 |
| 3.3.3 | Experimental Tests | 63 |
| 3.3.4 | Extension to More Complex Scenarios | 64 |
| 3.4 | Accuracy Improvements by Model Partitioning | 66 |
| 3.5 | Summary | 72 |
| 4 | Theoretical and Technical Background | 73 |
| 4.1 | Distribution Loss Minimization | 74 |
| 4.1.1 | Optimum Node Currents | 75 |
| 4.1.2 | Minimization of Local Distribution Losses | 76 |

| | | |
|----------|---|------------|
| 4.1.3 | Locally Optimal Node Voltages | 79 |
| 4.2 | Control Approaches | 80 |
| 4.2.1 | Optimum Current Control | 81 |
| 4.2.2 | Distance-Based Control | 81 |
| 4.2.3 | Surround Control | 83 |
| 4.3 | Power Control of Distributed Energy Resources | 84 |
| 4.3.1 | CPT Elemental Quantities | 85 |
| 4.3.2 | Current and Power Decomposition | 85 |
| 4.3.3 | Compensation Based on Instantaneous Power Terms | 87 |
| 4.3.4 | Actual Power Commands Generation | 88 |
| 4.3.5 | Harmonic Sequence Compensation Commands | 90 |
| 4.4 | Summary | 91 |
| 5 | Low-Voltage Microgrid Architecture | 93 |
| 5.1 | Master/Slave Architecture | 93 |
| 5.1.1 | General Control Principle | 96 |
| 5.1.2 | General Control Structure | 97 |
| 5.1.3 | Relations with IEEE Standard P2030.2 | 100 |
| 5.1.4 | Comparison with Droop-Based Approaches | 101 |
| 5.2 | Utility Interface | 102 |
| 5.2.1 | Utility Interface Control Principle | 104 |
| 5.2.2 | Control Structure Analysis | 106 |
| 5.2.3 | Control Design | 107 |
| 5.2.4 | Islanding Detection | 110 |
| 5.2.5 | Case Study | 114 |
| 5.3 | Summary | 131 |
| 6 | Controllers for Distributed Energy Resources | 133 |
| 6.1 | Hysteresis Current Controller | 135 |
| 6.1.1 | Fixed Frequency Hysteresis Controller | 136 |
| 6.1.2 | Small-Signal Behavior | 146 |

| | | |
|----------|--|------------|
| 6.1.3 | Experimental Test | 147 |
| 6.2 | Predictive Current Controller | 149 |
| 6.2.1 | Dead-Beat Controller | 150 |
| 6.2.2 | Small-Signal Behavior | 156 |
| 6.2.3 | Large-Signal Response Improvement | 158 |
| 6.2.4 | Experimental Test | 162 |
| 6.3 | Comparison | 165 |
| 6.3.1 | The Conventional Oversampled PI Current controller | 165 |
| 6.3.2 | Experimental Results | 168 |
| 6.4 | Summary | 174 |
| 7 | The Power-Based Control | 175 |
| 7.1 | Microgrid Architecture and Control | 176 |
| 7.2 | Data Collection | 176 |
| 7.3 | Preprocessing | 179 |
| 7.4 | Setpoint Computation | 181 |
| 7.4.1 | Active Power Control | 181 |
| 7.4.2 | Reactive Power Control | 184 |
| 7.4.3 | Grid-Connected Mode: Active and Reactive Power Control | 185 |
| 7.5 | Remarks on Voltage Control | 186 |
| 7.6 | Control Analysis | 187 |
| 7.6.1 | Power-Based Principle Analysis | 187 |
| 7.6.2 | System Analysis | 190 |
| 7.7 | Application Example | 194 |
| 7.8 | Summary | 204 |
| 8 | Test Case | 205 |
| 8.1 | Microgrid Laboratory Testbed | 205 |
| 8.2 | Experimental Results | 208 |
| 8.2.1 | Load Step During Islanded Operation | 209 |
| 8.2.2 | Connection Process | 209 |

| | | |
|----------|---|------------|
| 8.2.3 | Load Step During Grid Connected Operation | 210 |
| 8.2.4 | Transition to the Islanded Operation | 210 |
| 8.2.5 | Management of Overvoltage Conditions | 210 |
| 8.2.6 | Communication Failure | 214 |
| 8.3 | Summary | 215 |
| 9 | Conclusions | 217 |
| A | Current Sensor Board | 219 |

List of Acronyms

AC Alternate Current

ADC Analog to Digital Converter

CB Circuit Breaker

CC-EPP Current Controlled Electronic Power Processor

CCM Current Control Mode

CF Crest Factor

CPT Conservative Power Theory

DC Direct Current

DER Distributed Energy Resource

DFT Discrete Fourier Transform

DG Distributed Generator

DSO Distribution System Operator

DSP Digital Signal Processor

EG Energy Gateway

EPP Electronic Power Processor

ES Energy Storage

ESR Equivalent Series Resistance

FPGA Field Programmable Gate Array

GPIC General Purpose Inverter Controller Board

HDL Hardware Description Language

HIL Hardware-In-the-Loop

HV High Voltage

ICT Information and Communication Technology

LCO Limit Cycle Oscillation

LCU Local Control Unit

LSB Least Significant Bit

LV Low-Voltage

LVN Low-Voltage Network

MC Master Controller

MPPT Maximum Power Point Tracking

MSB Most Significant Bit

MV Medium-Voltage

OLTC On-Load Tap Changer

PB Power-Based

PCC Point of Common Coupling

PI Proportional Integral

PID Proportional Integral Derivative

PLC Power-Line Communication

PLL Phase Locked Loop

PMU Phase Measurement Unit

PR Proportional Resonant

PV Photo-voltaic

PWM Pulse Width Modulation

PWMD Digital Pulse Width Modulation

RCP Rapid Control Prototyping

RD Run-Down

RMS Root Mean Square

RT Real-Time

RTOS Real-Time Operation System

RU Run-Up

SF Synchronous Frame

SM Smart Meter

SNR Signal to Noise Ratio

SOC State Of Charge

SoC System on Chip

SRFC Synchronous Reference Frame Controllers

THD Total Harmonic Distortion

UI Utility Interface

UPS Uninterruptible Power Supply

VC-EPP Voltage Controlled Electronic Power Processor

VCM Voltage Control Mode

VSI Voltage Source Inverter

ZOH Zero-Order Hold

List of Figures

| | | |
|-----|--|----|
| 1-1 | Growth in world electricity demand and related CO ₂ emissions since 1990. | 2 |
| 1-2 | Evolution of European solar PV cumulative installed capacity. | 2 |
| 1-3 | Evolution of the electric power system. | 4 |
| 1-4 | Structure of the dissertation. | 11 |
| 2-1 | Repetitive controller | 21 |
| 2-2 | Resonant, multiple resonant, and repetitive. | 21 |
| 2-3 | Predictive control of a three-phase active filter | 23 |
| 2-4 | Scheme of a hysteresis controller. | 25 |
| 2-5 | Variables of the hysteresis controller. | 25 |
| 2-6 | Interaction between two voltage controlled sources. | 29 |
| 2-7 | Harmonic compensation scheme for current controlled converters. | 36 |
| 2-8 | Harmonic compensation scheme for voltage controlled converters. | 36 |
| 2-9 | Harmonic compensation scheme for a hybrid V and I controlled converters. | 36 |
| 3-1 | Structure and functionalities of a DER-interfacing EPP | 49 |
| 3-2 | Basic representation of the typical DC/AC stage of a DER-interfacing EPP. | 51 |
| 3-3 | DER-interfacing EPP controller implementation | 55 |
| 3-4 | Typical system configuration with user interface. | 58 |
| 3-5 | Zoom-in view of the PC interface. | 59 |
| 3-6 | HIL simulation set-up | 62 |
| 3-7 | View of the experimental testbed for DER-interfacing EPPs. | 64 |
| 3-8 | Comparison of PC, real-time simulations, and experimental measurements. | 65 |
| 3-9 | Application of RCP to the distance-based microgrid supervisor. | 67 |

| | | |
|------|---|-----|
| 3-10 | Bode plots of the open loop transfer functions T_{i0} and $T_{i0}^{(DA)}$ | 68 |
| 3-11 | Effect of model partitioning. | 70 |
| 3-12 | Effect of model partitioning in reducing simulation artifacts | 71 |
| 3-13 | Example of an implemented LabVIEW program for HIL tests | 71 |
| 4-1 | Representation of distribution line between two active nodes A and B | 77 |
| 4-2 | Representation of a grid section converging in an active node. | 79 |
| 5-1 | Considered microgrid scenario. | 94 |
| 5-2 | Master/slave microgrid architecture. | 94 |
| 5-3 | Generic structure of an energy gateway (EG) | 98 |
| 5-4 | Master/slave control principle. | 100 |
| 5-5 | The utility interface (UI). | 103 |
| 5-6 | UI control scheme. | 105 |
| 5-7 | Open loop gain of UI voltage control loop. | 108 |
| 5-8 | Open loop gain of the compensated UI outer current control loop. | 110 |
| 5-9 | Poles and zeros of $H_{v_{MG}^*}^{v_{MG}}$ with different static gains and dynamics for $W_{i_L^*}^{i_L}$ | 111 |
| 5-10 | Poles and zeros of $W_{i_G^*}^{i_G}$ for different values of L_G and R_G | 111 |
| 5-11 | Zoom-in view of resonant poles and zeros of Fig. 5-10. | 111 |
| 5-12 | Islanding detection scheme. | 112 |
| 5-13 | Microgrid's possible operating modes and transitions. | 113 |
| 5-14 | UI voltage reference generator (per phase). | 114 |
| 5-15 | UI test circuit. | 116 |
| 5-16 | Real-Time (RT) simulation testbed of the UI. | 118 |
| 5-17 | Connection of non-linear load. | 121 |
| 5-18 | Response to 5% variation of grid voltage (RT-simulations). | 121 |
| 5-19 | Transition to islanded operation (RT-simulations). | 122 |
| 5-20 | Transition to grid connected operation (RT-simulations). | 122 |
| 5-21 | System behavior along the entire sequence of events (RT-simulations). | 123 |
| 5-22 | Measured THD along the entire sequence of events (RT-simulations). | 123 |
| 5-23 | Islanded operation with non-linear load. | 124 |

| | | |
|------|---|-----|
| 5-24 | Connection of non-linear load during grid connected operation. | 125 |
| 5-25 | Grid connected operation with non-linear load. | 125 |
| 5-26 | Grid connected operation with non-linear load and distorted grid voltage. . . | 126 |
| 5-27 | Transition form islanded to grid connected operation. | 127 |
| 5-28 | Zoomed-in view around the connection displayed in Fig. 5-27. | 127 |
| 5-29 | Non-intentional transition to islanded operation. | 129 |
| 5-30 | Voltage parameters during non-intentional transition. | 129 |
| 5-31 | Intentional transition to islanded operation due to voltage out of range. . . . | 130 |
| 5-32 | RMS voltage across an intentional islanding transition due to overvoltage. . . | 130 |
| | | |
| 6-1 | Simplified schematic of the considered full bridge inverter test bench. . . . | 134 |
| 6-2 | Current error acquisition and processing circuit of the hysteresis controller. . | 136 |
| 6-3 | Diagram of the hysteresis' FPGA circuit organization with control signals. . | 138 |
| 6-4 | Operation of the proposed hysteresis controller. | 139 |
| 6-5 | Operation of the hysteresis current control with respect to non-idealities. . . | 142 |
| 6-6 | AC step reference change. | 148 |
| 6-7 | Switching frequency error of hysteresis controller. | 149 |
| 6-8 | Converter equivalent circuit. | 151 |
| 6-9 | Operation of the proposed dead-beat controller. | 152 |
| 6-10 | Small-signal step response in ideal conditions. | 157 |
| 6-11 | Small-signal step response as in Fig. 6-10, but with $\Delta L/L = +0.35$ | 157 |
| 6-12 | Current error acquisition and processing circuit of dead-beat controller. . . | 159 |
| 6-13 | Diagram of the dead-beat's FPGA circuit organization with control signals. . | 159 |
| 6-14 | Response of the dead-beat controller to a large-signal step change. | 160 |
| 6-15 | Response of the dead-beat controller to an AC reference change. | 163 |
| 6-16 | Response of the dead-beat controller to a DC step change. | 164 |
| 6-17 | Current error acquisition and processing circuit of the PI controller. | 165 |
| 6-18 | Operation of the considered oversampled PI controller. | 166 |
| 6-19 | Comparison of the small-signal responses. | 170 |
| 6-20 | Comparison of the responses to reference step changes (#1/2) | 172 |

| | | |
|------|--|-----|
| 6-21 | Comparison of the responses to reference step changes (#2/2) | 173 |
| 7-1 | Master/slave microgrid architecture with power-based control. | 177 |
| 7-2 | Simplified model of the power-based control. | 188 |
| 7-3 | Considered LV power system. | 195 |
| 7-4 | Active power profiles without PB control. | 198 |
| 7-5 | Active power profiles with PB control. | 198 |
| 7-6 | Active power profiles with PB control and energy storage. | 198 |
| 7-7 | Active power at PCC. | 199 |
| 7-8 | Distribution power losses over the grid. | 200 |
| 7-9 | Voltage deviation at EG ₂ node. | 201 |
| 7-10 | Total power production from PV sources. | 201 |
| 7-11 | State of charge of energy storage devices (<i>Case C</i>). | 201 |
| 7-12 | Behavior of coefficients α_p and α_q (<i>Case C</i>). | 202 |
| 7-13 | Reactive power contributions. | 203 |
| 8-1 | Diagram of the experimental testbed | 206 |
| 8-2 | Photo of the implemented microgrid testbed (more details in Fig. 8-3). | 207 |
| 8-3 | Photo of the implemented microgrid testbed (details of Fig. 8-2). | 207 |
| 8-4 | Schematic of the laboratory microgrid prototype. | 208 |
| 8-5 | Load step (0 to 2 kW) during islanded operation | 211 |
| 8-6 | Process of connection to the mains | 211 |
| 8-7 | Load step (0 to 2 kW) during grid-connected operation | 211 |
| 8-8 | Load step (2 to 4 kW) during grid-connected operation | 212 |
| 8-9 | Intentional transition to islanded operation | 212 |
| 8-10 | Non-intentional transition to islanded operation | 212 |
| 8-11 | Experimental measurement of EG managing an overvoltage condition. | 213 |
| 8-12 | Communication failure. | 214 |
| A-1 | Simplified circuit diagram of the current sensor board. | 220 |
| A-2 | Current sensor board (top view). | 221 |

A-3 Current sensor board (bottom view). 222

List of Tables

| | | |
|-----|--|-----|
| 2.1 | Typical control hierarchy for microgrids | 16 |
| 2.2 | Proposed control hierarchy for low-voltage microgrids | 17 |
| 2.3 | Harmonic current distortion limits for systems rated 120 V through 69 kV | 32 |
| 3.1 | Control function stack of a DER-interfacing EPP | 52 |
| 3.2 | Characteristics of the chosen control platform (GPIC) | 56 |
| 3.3 | Characteristics of the chosen simulation platform (cRIO-9082) | 57 |
| 3.4 | Inverter and PI current controller parameters | 60 |
| 3.5 | Grid parameters | 61 |
| 5.1 | Test circuit parameters | 115 |
| 5.2 | Distortion measurements in steady-state from the prototype of Fig. 5-15 | 126 |
| 6.1 | Converter parameters | 134 |
| 6.2 | Hysteresis controller parameters | 147 |
| 6.3 | Dead-beat controller parameters | 161 |
| 6.4 | Experimental results for the current controllers | 171 |
| 7.1 | Distribution grid parameters | 196 |
| 7.2 | First energy gateway parameters (EG #1) | 196 |
| 7.3 | Second energy gateway parameters (EG #2) | 196 |
| 7.4 | Performance indexes computed at microgrid PCC | 203 |
| 8.1 | Parameters of the laboratory microgrid prototype | 209 |
| A.1 | Current Sensor Board Parameters | 220 |

Abstract

The term *smart grid* indicates an electrical network that aims at solving the weaknesses of conventional electrical grids by taking advantage of extensive use of information and communication technologies in the production, transmission, distribution, and usage of electricity. The main purpose is to attain the highest level of sustainability with respect to the environment and flexibility in hosting the increasing number of consumers.

The various challenging issues, the potential market involved by related products and services, and the expected benefit for the society linked to the development of the new electricity grid paradigm have attracted a wide interest from academia, industry, and governments in the last ten years.

Advanced technologies, such as advanced automation infrastructures and model predictive management approaches, are already used for the operation of transmission networks, where the recent advances are driven by the need of infrastructural changes. Low-voltage distribution grids, instead, were devised to serve groups of residential or small industrial consumers, that were traditionally seen as purely passive (i.e., no generation of active power) and non-controllable loads, with limited monitoring and control functionalities. Therefore, low-voltage grids are now required to undergo a deep evolution to fulfill the smart grid functionality.

The widespread integration of renewable resources in low-voltage grids, seen in recent years, is the starting point of this evolution. While, on the one hand, this integration enables consumers to satisfy their energy needs more economically and with a lower impact on the environment, on the other hand, the high penetration of distributed generation in low-voltage grids calls for specific provisions to ensure efficient operation regimes.

Specifically, some of the main issues that need to be addressed are: unwanted reac-

tive power circulation, intermittent power injections from renewables, distortion of voltage profiles along distribution lines, harmonic current circulation, unbalance in three-phase systems. In addition, further issues are expected to emerge in the future in case of adoption of other particular loads/resources, such as the electric vehicles and local electrical storage devices. A promising approach to tackle these issues is to cluster loads and distributed energy resources to make them behaving like a single entity with a higher level of controllability, seen from the point of view of the main grid. These clusters, referred to as *smart microgrids*, play as the basic tiles of the smart grid scenario.

The main goal of the work presented herein is to identify and analyze a scalable architecture for low-voltage microgrids together with a suitable control system for the distributed energy resources that may be connected. The defined solution should improve low-voltage grids performance in terms of *i*) capacity of hosting distributed generators, *ii*) continuity of operation during faults affecting the mains, and *iii*) regulation of the power and power quality at the interface with the main grid.

In the first part of this dissertation, a general overview of control aspects and issues in low-voltage microgrids is provided, together with some preliminary theoretical considerations. This first part prepares the ground to introduce the proposed microgrid architecture and control approach. The central part of the work focuses on the proposed master/slave microgrid architecture and control algorithm. In the considered architecture, distributed energy resources (DERs) are interfaced to the grid by means of conventional current-driven power electronics interfaces and the microgrid is interfaced to the mains via a voltage-driven utility interface converter. The control algorithm, the so called *power-based control*, is then introduced and adopted to regulate the contribution to microgrid needs from the different energy resources available. The control approach ensures an accurate active and reactive power sharing among DERs that takes into account both local (i.e., DER level) and global (i.e., microgrid level) constraints. The power-based control approach lies on the conservative power theory, which offers a meaningful, robust, and computationally efficient method to manage power quantities referring to different grid nodes. The advantages of the presented solution can be summarized as follows:

- no need of tight synchronization of measurements or control actions among control

agents;

- no need of plants models;
- no need of measures from passive nodes;
- no circulation currents among generators;
- light calculation and communication requirements;
- prompt regulation of the power flow at the microgrids point of coupling with the mains;
- fair exploitation of distributed energy resources that may also take into account particular local constraints.

From the implementation point of view, the crucial aspects related to the control of power electronics converters interfacing distributed energy resources to the grid, as well as the microgrid to the mains, are addressed in detail. The purpose of this latter activity is to identify the better performing controller to implement the current control loops of grid-tied converters, with a particular focus on utility interface converters. To this end, a couple of novel, high-performance, fully digital current controllers are introduced, analyzed, and characterized; the excellent large-signal and small-signal dynamic behaviors that can be obtained are shown by means of analytical, simulation, and experimental results.

The actual behavior of the proposed solutions is demonstrated on a laboratory-scale microgrid prototype that has been specifically implemented. The development of the prototype took advantage of rapid-control-prototyping techniques, while hardware-in-the-loop real-time simulation supported the debugging of the control techniques and algorithms.

Sommario

Con rete elettrica intelligente (*smart grid*) si intende una rete elettrica che mira a risolvere le criticità delle reti elettriche convenzionali sfruttando in modo trasversale le tecnologie dell'informazione e della comunicazione nella produzione, trasmissione, distribuzione e impiego dell'energia elettrica. L'obiettivo principale è quello di raggiungere il più alto livello di sostenibilità dal punto di vista ambientale e flessibilità nel servire il crescente numero di consumatori.

Le interessanti problematiche, il potenziale mercato di prodotti e servizi e i benefici per la società legati allo sviluppo del nuovo paradigma di rete elettrica hanno attirato negli ultimi dieci anni l'interesse del mondo accademico, industriale e delle istituzioni governative. Tecnologie all'avanguardia, come sono le infrastrutture di automazione avanzata e approcci di gestione predittivi basati su modelli, sono già impiegati per il funzionamento delle reti di trasmissione, nelle quali i recenti progressi sono principalmente guidati dalla necessità di cambiamenti infrastrutturali. Invece, le reti di distribuzione a bassa tensione sono concepite per servire gruppi di piccoli consumatori industriali o residenziali, che, tradizionalmente, si comportano come carichi puramente passivi e non controllabili, con funzionalità di monitoraggio e controllo limitato. Perciò, le reti a bassa tensione saranno soggette ad una profonda evoluzione per soddisfare la funzionalità delle smart grid.

La diffusa integrazione di fonti rinnovabili nelle reti di bassa tensione che ha avuto luogo negli ultimi anni è il punto di partenza di questa evoluzione. Mentre, da un lato, l'integrazione di sorgenti rinnovabili permette ai consumatori di soddisfare il loro fabbisogno energetico più economicamente e con un minor impatto ambientale, d'altra parte, l'ampia diffusione di generazione distribuita richiede provvedimenti specifici per garantire regimi di funzionamento efficienti.

In particolare, alcuni dei principali problemi che devono essere affrontati sono: la circolazione di potenza reattiva, la generazione intermittente da parte delle risorse energetiche rinnovabili, l'alterazione dei profili di tensione lungo le linee di distribuzione, la circolazione di corrente armonica, lo squilibrio in sistemi trifase. Inoltre si prevede l'emergere di ulteriori necessità nel caso particolari tecnologie prendano piede in futuro, come, ad esempio, i veicoli elettrici e i dispositivi di immagazzinamento dell'energia. Un promettente approccio per affrontare questi problemi è quello di raggruppare carichi e risorse energetiche affinché siano visti, nel loro insieme, dalla rete principale come una singola entità elettrica con funzionalità di controllo estese. Questi raggruppamenti, denominati microreti (*microgrid*), rappresentano i tasselli che comporranno lo scenario delle smart grid.

L'obiettivo principale del lavoro qui presentato è quello di individuare e analizzare un'architettura scalabile per microreti a bassa tensione che integri un sistema di controllo adeguato a gestire le risorse energetiche connesse. La soluzione definita dovrebbe migliorare le prestazioni delle reti a bassa tensione, in termini di *i*) capacità di ospitare generazione distribuita, *ii*) continuità di funzionamento anche in caso di guasti che interessano la rete principale e *iii*) qualità e capacità di regolazione del flusso di potenza all'interfaccia tra microrete e rete principale.

Nella tesi, i primi capitoli forniscono una panoramica generale delle questioni relative al controllo delle microreti a bassa tensione, introducono il metodo di sviluppo adottato e descrivono il contesto che ha dato origine al lavoro presentato nei capitoli centrali. La parte centrale del lavoro riguarda una architettura di tipo master/slave per microreti. Nell'architettura considerata, le risorse energetiche distribuite (DERs) sono interfacciate alla microrete per mezzo di convenzionali convertitori di potenza elettronici e, a sua volta, la microrete è interfacciata alla rete principale tramite un convertitore pilotato in tensione. L'algoritmo di controllo, il cosiddetto controllo basato sulle potenze (*power-based control*), viene descritto e adottato per regolare il contributo da parte delle diverse risorse energetiche disponibili alle esigenze della microrete. L'approccio di controllo proposto garantisce un'accurata suddivisione della potenza attiva e reattiva tra DERs, che tiene conto sia di necessità locali (i.e., a livello di DER) sia di vincoli globali (i.e., a livello di microrete). L'approccio basato sulle potenze poggia sulla teoria conservativa delle potenze, che offre

un metodo significativo, robusto e computazionalmente efficiente per elaborare quantità di potenza che si riferiscono a nodi differenti. I vantaggi della soluzione presentata possono essere riassunti nei punti seguenti:

- nessuna necessità di sincronizzazioni critiche nelle misure o nelle azioni di controllo tra gli agenti;
- funzionamento indipendente dalla conoscenza del modello dell'impianto controllato;
- non sono richieste capacità di misura o comunicazione da parte dei nodi passivi;
- assenza di correnti di circolazione tra i generatori;
- limitate esigenze computazionali e di comunicazione;
- accurata regolazione del flusso di potenza al punto di connessione con la rete principale;
- equa redistribuzione del carico tra le risorse energetiche distribuite, con la possibilità di tener conto di vincoli locali.

Dal punto di vista implementativo, gli aspetti di maggior importanza relativi al controllo dei convertitori di potenza elettronici che interfacciano le risorse energetiche distribuite alla rete, e anche la microrete stessa alla rete principale, sono analizzati in dettaglio. Lo scopo di quest'ultima attività è di identificare i controllori maggiormente performanti come regolatori di corrente per convertitori connessi alla rete, con particolare attenzione ai convertitori d'interfaccia al nodo di saldo della microrete. A tal fine, una coppia di controllori digitali innovativi e ad alte prestazioni sono descritti, analizzati e caratterizzati; la bontà dei comportamenti dinamici sia al grande che al piccolo segnale è mostrata mediante valutazioni analitiche, al simulatore, e sperimentali.

L'effettivo comportamento delle soluzioni proposte è dimostrato utilizzando un prototipo di microrete realizzato, a tale scopo, in laboratorio. Lo sviluppo del prototipo si è avvantaggiato di tecniche di *rapid-control-prototyping*, mentre tecniche di simulazione in tempo reale *hardware-in-the-loop* hanno supportato la messa a punto degli algoritmi e delle tecniche di controllo.

Acknowledgments

Keep your eyes on the stars, and your
feet on the ground.

Theodoore Roosevelt

First of all, I would like to thank my supervisors Prof. Paolo Tenti and Prof. Simone Buso for their invaluable support. They have wisely and carefully guided me on the research activities, always ready to provide the finest help and advice when needed, no matter the specific argument. All the positive scientific results I achieved during these last years, as well as most of my personal growth, are owe to them.

With them, I would like to thank all the people of the Power Electronics Group of the University of Padova, Prof. Paolo Mattavelli, Prof. Giorgio Spiazzi, Prof. Leopoldo Rossetto, Prof. Luca Corradini, Dr. Marco Stellini, and Mr. Renato Sartorello, for the important contribution they have given, in many and different ways, to my professional education. Also, I would like to thank Dr. Alessandro Costabeber for his help in the first part of my Ph.D. studies and Dr. Francesco Sichirollo for his careful support and teachings.

Special thanks go to the lab manager and dear friend Dr. Marco Stellini. Besides having the pleasure of sharing with him the joy of working together in many intriguing projects, he has always been a source of thoughtful advice.

Special thanks go also to my Ph.D. colleagues Stefano Lissandron and Luca Scandola, who have been the ideal companion in such a challenging path, always ready to help, exchange views, and share experiences. My gratitude goes also to my dear, long-term classmates Davide Biadene and Francesco Cavazzana, with whom I share all the phases of our University experience.

A particular mention is for my lab partner and dear friend Dr. Danilo Iglesias Brandão. An intense, fruitful, and enjoyable collaboration among us characterized the period in which he staid in Padova. This dissertation encompasses some of the outcomes of the experimental activities that we carried on together.

I want also to express my gratitude to all the people of the Institute for Automation of Complex Power Systems (ACS) of the University of Aachen, Germany. In particular, to the Director of the ACS Institute, Prof. Antonello Monti, and to Prof. Ferdinanda Ponci for giving me the possibility of taking part to such a stimulating environment like is their research group. A special thank goes to Dr. Antonino Riccobono for his very much appreciated scientific and personal support, and his family, for their warm hospitality. Also I would like to thank all the very dedicated research assistants and master students with whom I could collaborate, in particular, Dr. Marco Cupelli, Dr. Jing Wang, Joaquín Mascareñas Hinojosa, Syed Khurram Abbas Naqvi, Waqas Ahmad Raazi, and Markus Mirtz; and the friends with whom I had pleasurable lunches and that gave me good memories: Bernardino Spanu, Eran Schweitzer, Gianluca Lipari.

Finally, endless thanks to my family for having, from the outside, unconditionally supported me in each and every phase of my studies.

Padova, January 2016

Tommaso Caldognetto

Chapter 1

Introduction

An electrical power system is a technological system designed to generate and distribute electrical power for the benefit of human activities. Traditionally, electrical power systems are characterized by a hierarchical organization where few, large centralized generators deliver power to the users. This model arose in the late nineteenth century owing to pioneers such as Thomas Alva Edison, George Westinghouse, Nikola Tesla. Since then, electrical power systems have steadily expanded and evolved, although maintaining a centralized organization for both power generation and control.

The European power system became the largest technological system ever built, playing a crucial role in supporting the energy needs of the modern society. Nowadays, due to its importance, two critical issues are driving the choices for the future architectural and infrastructural developments: the need of minimizing environmental impacts in terms of greenhouse gas emissions and of supporting the future energy demand. Indeed, according to [1], the electric power sector is the largest source of energy-related CO₂ emissions and the greatest focus (to date) of energy sector efforts to decarbonise. As well, to invest in an *efficient* and an even more *widespread* use of electricity (process known as electrification) is regarded as a key element to achieve global commitments to decarbonization. These aspects are summarized by the International Energy Agency (iea) by using Fig. 1-1, which displays higher energy needs by more than 40% and further increases of CO₂ emissions by 2030.

The first provision taken at international level to tackle these issues has been to incre-

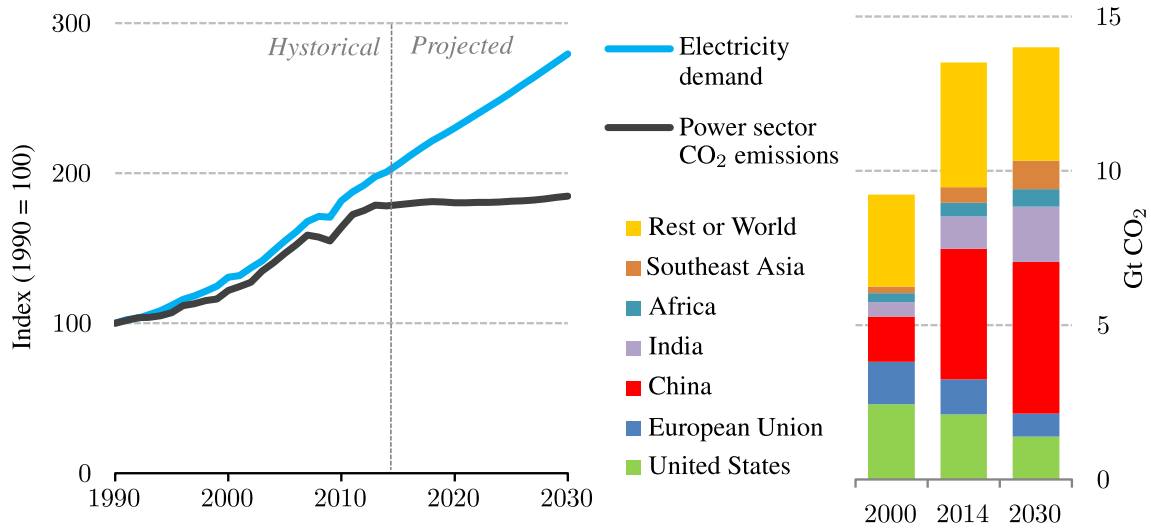


Figure 1-1: Growth in world electricity demand and related CO₂ emissions since 1990 (left) and related CO₂ emissions by region (right) [1].

ment the share of energy production from renewables, which exploit resources not subjected to depletion and do not produce unwanted emissions during operation. In particular, solar and wind energy sources installed distributedly around the territory have seen a wide adoption in Europe. Fig. 1-2 shows the totally installed capacity from photovoltaic sources since 2000 [2]; notably, the shown steep increase in photovoltaic installations is characterized by a significant contribution from plants connected to the low-voltage distribution

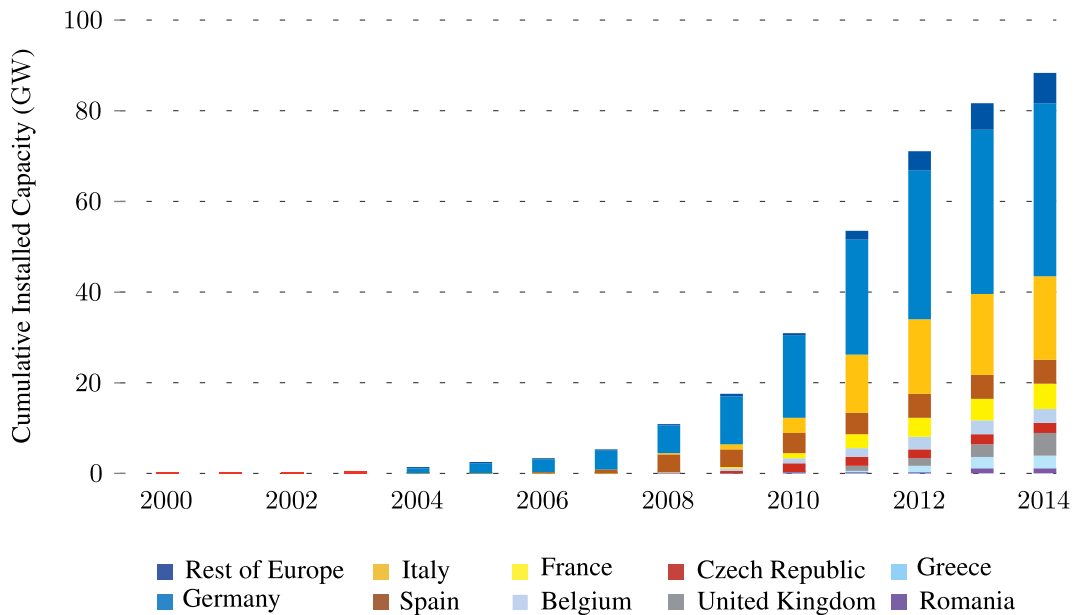


Figure 1-2: Evolution of European solar PV cumulative installed capacity [2].

system (e.g., 98 % of total plant installations in Germany [3]). The practice of siting resources close to the users—actually, at the users’ premises—is counterposed to the initially mentioned traditional centralized structure of electrical power systems. This trend is now a fact concerning photovoltaic sources and it is expected to encompass, in the next decades, energy resources in general (i.e., for both source and storage devices).

Actually, a broader range of changes are foreseen to honor countries’ pledges to reduce greenhouse emissions and sustaining the development of society. In [1], these changes are represented by means of the illustrations in Fig. 1-3, where Fig. 1-3(a) shows the situation in 2014, whereas Fig. 1-3(b) shows the foreseen situation in 2030. A plethora of advanced technologies, including distributed renewable sources, distributed storage, advanced automation technologies, are expected to be integrated-in or interact-with the electrical system. Power electronics is the enabling technology of the highlighted evolution [4, 5]. It has been demonstrated that its adoption in this sector brings numerous valuable features, such as, controllability, natural connection with other information and communication technologies, high efficiency, small size, relatively cheap solutions, ease of coupling different physics domains.

Generally, high technology readiness levels may be claimed for the individual technologies of Fig: 1-3(b) (see, for example, the TOSA project [6] for what concerns transportation), although, many open issues about how to efficiently combine, control, and coordinate resources are present. Prospective solutions should provide effective and harmonious means to tackle peculiar limitations of current low-voltage grids in view of the foreseen evolution; in particular, considering the aspects that follow.

- Hosting capacity, that is, the maximum penetration of distributed energy resources (DERs) for which the power system operates satisfactorily, should be maximized to allow the wider collection of power from renewables.
- Full exploitation of resources, which is essential to maximize the return from the investment. This implies to involve, rationally, all distributed resources to cooperate for the benefit of the whole grid.
- Efficient operation, which is not limited at only minimizing the power loss during

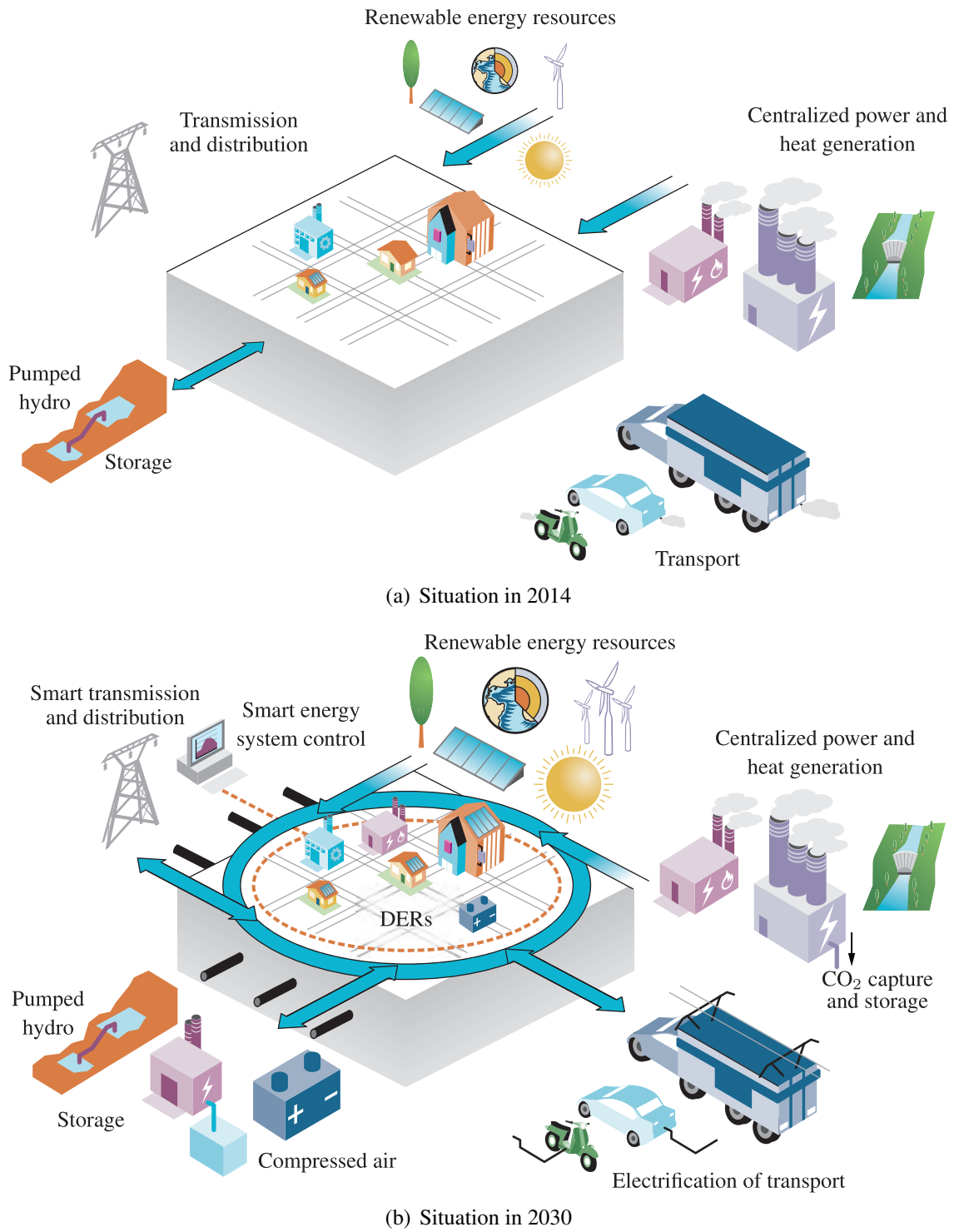


Figure 1-3: Evolution of the electric power system [1].

operation, but also means to take into account the impact that specific control actions have on components' reliability and lifetime.

- Power quality, to increase the efficiency of distribution networks by reducing the circulation of unwanted reactive, harmonic, and unbalance currents and, simultaneously, improve the quality of the voltage provided to the consumers.
- Reliability, that is, to keep on normal operation for grid subsections in case of fault of the main grid. This, in particular, would allow to ensure energy supply to critical loads in the wake of disasters, so that to support recovery and rebuilding efforts.

A promising approach to tackle these issues is to cluster DERs and loads to make them behaving like a single entity with a higher level of controllability, seen from the point of view of the main grid. In this way, control functions can be demanded to these clusters, which can more easily perform, locally, the most appropriate control actions. Such clusters are referred to as *smart microgrids* and represent a bottom-up approach to the development of the next generation electric power system.

1.1 Investigated Aspects and Contribution

Within the scenario outlined above, this dissertation investigates some critical aspects related to the control of electronic power converters in low-voltage microgrids. The challenges on which the dissertation is focused on and the proposed solutions are summarized in the following subsections.

1.1.1 Microgrid Architecture

Challenge. Microgrids are requested to be able to integrate all the heterogeneous energy resources that may be deployed to manage electricity more efficiently and with a reduced impact on the environment. Besides, microgrids should extend the operating ranges of traditional low-voltage grids, so as to increase the reliability in serving loads, in particular when faults affect the mains [7]. From this point of view, the possibility for the microgrid

of operating connected-to as well as islanded-from the mains, with seamless transitions between the two operating modes, is an extremely valuable feature for such kind of power systems.

Contribution. Proposal of a master/slave architecture to coordinate DERs in smart microgrids. The architecture is composed of two main elements: a voltage-driven utility interface converter and distributed energy gateways. The utility interface interfaces the microgrid with the mains, supervises the voltage at the point of connection of the microgrid, and embeds a centralized microgrid controller playing the role of *master control unit* for distributed resources; the energy gateways interface DERs to the microgrid, and embed local control units playing the role of *slave units*. Global control needs are managed centrally by the master controller, whereas local control needs are managed in a decentralized manner by the slave units. A control algorithm making use of conservative power terms is employed to ensure synergy among the two (i.e., local and global) control levels. The proposed architecture shows the advantages of enabling a low-voltage grid section to operate both grid connected and islanded, decoupling local and global control objectives, and posing small communication requirements.

1.1.2 Current Controllers for Grid-Tied Converters

Challenge. According to grid connection standards, the currents generated by grid-tied converters should follow given references with high accuracy, without being affected by voltage disturbances and, possibly, uncertainties in the grid model. In addition, in applications concerning voltage-driven inverters, typically referred to, for example, in droop-controlled power electronics systems, prompt current controllers can improve the dynamic response in sustaining fast load transients and compensating harmonic currents and, in addition, protect the converter from dangerous overload conditions.

Contribution. Proposal of a couple of high performance current controllers for grid-tied converters. Both the current controllers exploit oversampling to enhance control capability in terms of small- and large- signal responses. The first controller is a fully digital,

non-linear, wide bandwidth current controller that mimics an analog hysteresis current controller, but does not employ analog comparators, digital to analog converters, or any other analog signal pre- or post- processing circuitry. Indeed, it fully virtualizes the hysteresis controllers operation and drives the power converter at almost constant switching frequency. It offers the same excellent dynamic performance of the analog hysteresis controller and, at the same time, solves most of the related problems. The second controller is a digital dead-beat current controller. The controller updates, with negligible computation delay, the duty-cycle twice in a switching period, so that the error in tracking the reference current is nulled in half a modulation period, maximizing the controllers small-signal bandwidth. The devised controller includes a transient detection circuit to enhance the large-signal response. Thanks to the high performance shown by both the proposed solutions, these controllers can be employed directly as current controllers for current-driven converters or as inner current controllers for voltage-driven converters to achieve superior quality in generating currents or voltages.

1.1.3 Control Algorithm for DERs Interfacing Converters

Challenge. During grid connected operation, a deterministic power exchange with consumers is highly desirable from the point of view of utilities, which can exploit this knowledge to plan optimized modes of operation. Smart microgrids can exert this feature by making use of their available energy resources (e.g., controllable generators, storage). In particular, distributed resources, potentially, can be coordinated according to their state to attain a particular power profile previously negotiated with the DSO; this *flexibility* provided by the microgrid by means of a proper control system may be rewarded by the DSO. Further, the possibility of regulating the power exchange at microgrid PCC by adopting architectures analogous to the one in Sec. 1.1.1 is a critical aspect during islanded operation, in particular, to control the energy status of the voltage-driven converter connected at the PCC.

Contribution. Proposal of a master/slave control algorithm to regulate the power exchange at microgrid's PCC by properly driving DERs according to their power ratings and

power availability. The power availability is measured by means of a set of power quantities that are modulated individually by each DER according to their status and local needs. Power needs within the microgrid are estimated without involving any communication with passive nodes (i.e., loads), but only making use of the information provided by distributed resources and the measured power absorption at the PCC. On the basis of that principle, the control algorithm is devised to exploit the available resources in a fair way in both grid connected and islanded operation, with a regulation capability that suitably fulfills the requirements in the two modes of operation.

1.1.4 Control of Voltage Profiles

Challenge. As the adoption of renewables increases, specific technical challenges linked to hosting capacity limitations of low-voltage networks become more intense; the alteration of voltage profiles along distribution lines is a relevant issue from this standpoint. Beyond the obvious solution of upgrading the distribution infrastructure (grid reinforcement), control techniques based on on-load tap changers (OLTC), reactive power control, and active power curtailment have been investigated in the literature to tackle this issue. Techniques based on OLTCs can effectively adjust the voltage at the point of connection of the feeder, according to specific requirements on voltage profiles, but are penalized by wearing of components and limited flexibility in regulating the voltages along the grid, especially for those nodes that are far from the OLTC. Appealing solutions may be found by exploiting the available apparent power capacity of the electronic power processors interfacing DERs to the grid. Unlike in medium-voltage or high-voltage networks, voltage magnitudes in low-voltage networks are mainly affected by active power flows, due to the typically high R/X ratios, making provisions based on reactive power control less effective.

Contribution. Proposal of a dynamic overvoltage control technique for low-voltage microgrids integrated within the master/slave framework mentioned above (see Sec. 1.1.1 and Sec. 1.1.3). During normal operating conditions, a centralized controller shares the microgrid power needs among DERs in proportion to their local power availability, whereas, during overvoltage operating conditions, DERs are locally controlled so as to limit their

active power injection and maintain node voltages within nominal ranges. When integrated to Sec. 1.1.3, the control of the power flow (taking place centrally, at microgrid PCC) and the local overvoltage control (performed distributedly, at each DER) cooperate so that both the power flow at microgrid PCC and the voltage magnitudes at the point of connection of DERs can be simultaneously regulated. This technique unavoidably causes a certain reduction in the total power injection. However, this drawback can be eliminated by integrating storage devices at specific critical nodes. The approach shows advantages in its simplicity, flexibility to accommodate local operational constraints, and limited needs in terms of computation and communication resources. It is more efficient than reducing DER installations, controlling OLTC, or commanding cut-offs of the PV systems during peak production.

1.2 Dissertation Outline

The dissertation consists of nine chapters (see Fig. 1-4). The current chapter, Ch. 1, introduces the considered research topic, highlighting the main aspects on which the research activity reported herein is focused. The next two chapters, Ch. 2 and Ch. 3, together, represent the basis on which the central part of the dissertation develops; Ch. 2 provides a more in-depth overview of some of the most important issues in microgrid control, from the perspective of power electronics, while Ch. 3 describes the methodology applied to develop and experimentally validate each proposed solution of the following chapters. Ch. 4 retraces the studies that brought to the development of the techniques discussed in the central chapters of the dissertation; this chapter reports the main general results and discusses the advantages and drawbacks of possible control actions suggested by theoretical considerations. Eventually, it is shown how the conservative power theory [8] can be applied to attain a general technique to coordinate the operation of geographically distributed power sources. Ch. 5 to Ch. 7 describe the proposed solutions to the control of electronic power converters interfacing renewable sources for low-voltage microgrids. In particular, Ch. 5 describes the master/slave architecture proposed for resource integration and coordination. The elements composing the introduced architecture may take full advantage of the current controllers considered in Ch. 6. In this chapter, a couple of innovative, high performance,

fully digital current controllers for grid-tied converters are described, whose operation principle can, actually, be applied to DC-AC and DC-DC voltage source converters. Next, Ch. 7 presents a model-free control algorithm, called power-based control, suitable to be applied to the architecture described in Ch. 5. It is shown how, with a master/slave architecture integrating the power-based control, DERs can take part to microgrid control in an effective manner, so that the microgrid can be seen, from the utility, as an aggregated prosumer with extended power capacity and wide control functions while not neglecting local optimization needs. The proposed architecture and control system are validated experimentally in Ch. 8, which also describes the experimental setup employed for testing activities. Finally, Ch. 9 reports the conclusions drawn from the research work.

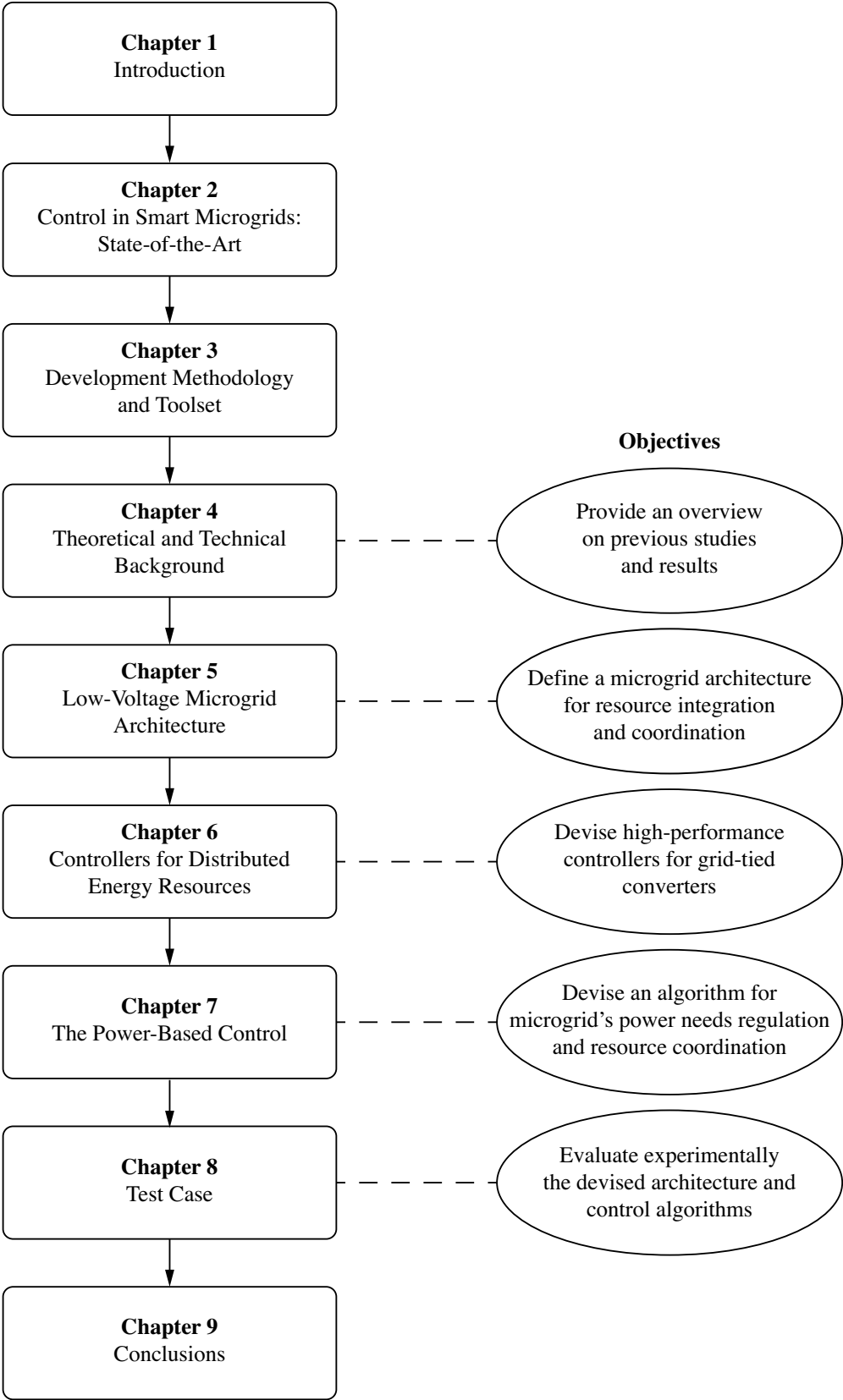


Figure 1-4: Structure of the dissertation.

Chapter 2

Control in Smart Microgrids: State-of-the-Art

Microgrids are distributed, interconnected, interdependent, heterogeneous systems of systems that need to operate effectively and efficiently. The particular objectives of the interacting agents give rise to a number of control needs and control issues [9]. These can be summarized with the following principal themes:

- stable regulation of DC link voltage, output current, output voltage of distributed energy resources [10–14, 14–20];
- harmonic damping and local/distributed harmonic compensation [21, 21–32];
- robust DERs synchronization with grid voltage [33, 34];
- reliable detection and management of islanding operation [35, 36];
- exploitation of energy storage systems [37–41];
- power balancing and proper load sharing among distributed generators [38, 42–48];
- local/distributed compensation of reactive power [28, 49–53];
- support of voltage profiles along feeders [44, 50, 54, 55];
- management of distribution network congestions [56, 57];

-
- adaptation to varying operating conditions (islanding/grid-connected operation) [58–63];
 - load current balancing among phases [31, 43];
 - reliable microgrid synchronization with the main grid voltage [64–66];
 - regulation and scheduling of the power exchange at microgrid’s PCC.

Specific *control hierarchies* are usually referred to in the literature to cope with the complexity of the control scenario. For what concerns the widely known droop-based microgrids [67], their principle of operation is inspired by the behaviour of traditional electricity systems [68], for which the natural droop of the magnitude and frequency of the voltage produced by electric generators, varying according to generation/absorption conditions, allows a stable operation of multiple parallel-connected converters. According to this principle, higher level control algorithms making use of a communication infrastructure are needed to restore grid voltage parameters as soon as generation or consumption varies. Taking into account the need of *i*) coordinating load power sharing, *ii*) restoring the magnitude and frequency of voltages, and *iii*) managing the interactions with the main grid, the literature typically refers to the control hierarchy of Table 2.1 [69–72]. The zero-level control concerns the innermost control loops of grid-tied power devices, namely, the output current and voltage control loops (e.g., [10]). The primary control concerns the regulation of the electrical quantity (i.e., current or voltage, like in [73] or in [63], respectively) generated by the grid-tied power devices in terms of magnitude and phase/frequency; also, it concerns in sustaining the local grid voltage and obtaining a favorable power contribution of generators to microgrid’s needs (e.g., [74]). The secondary control is responsible of restoring grid voltage parameters (e.g., [75]) and resynchronizing the microgrid to the main grid in view of transitions to the grid-connected operation (e.g., [65]). Finally, the tertiary control, supervises the power flow with the main grid.

This description stems from the characteristic challenges of droop-based approaches, such that, to easily summarize the peculiarities of the three uppermost control levels, some authors associate the primary control to droop control, the secondary control to frequency

and voltage restoration and resynchronization, and the tertiary control to power import and export at the connection with the mains [9]. This organization makes it difficult to describe management schemes (e.g., see [76, 77]) that may not directly reflect the hierarchy adopted for droop-based microgrids. Therefore, a slightly different hierarchy is considered herein to ease the description of generic microgrid architectures. The proposed hierarchization of control functions is done, instead of considering particular control needs (e.g., power sharing, voltage restoration, interaction with the mains), looking at the scope of control functions. So doing, herein, the *zero-level control* concerns the control of voltage and currents inside electronic power converters; the *primary control* is relevant to the behaviour of individual converters connected to a microgrid; the *secondary control* concerns the coordination of the set of resources that form the microgrid; finally, the *tertiary control* concerns the interaction among the microgrid and the main grid.

The next section defines the adopted hierarchy. The main solutions presented in the literature on microgrid control are overviewed in the remaining sections.

2.1 Control Hierarchy

The control hierarchy considered herein is composed of the four control layers that are described in the following.

- *Zero-level control*: comprises all the elemental control functions that electronic power converters (EPPs) managing power exchange with local resources (e.g., renewable source, energy storage device) have to perform [78, 79]. Essentially, there are two main control functions: current control and voltage control.
- *Primary control*: comprises control functions that can be exploited by employing only local information. The definition includes every control function that can be done locally, without inputs from the rest of the microgrid. Besides the functionalities that are necessary for microgrid operation, the primary control layer includes: compensation of reactive power and currents generated by local loads, management of local energy storage, support of local voltage if limits are exceeded, emergency

Table 2.1: Typical control hierarchy for microgrids [71, 80]

| Control Layer | Functionalities |
|----------------------|--|
| <i>Zero-level</i> | <ul style="list-style-type: none"> – Control of output currents and voltages |
| <i>Primary</i> | <ul style="list-style-type: none"> – Current and voltage stability provision – Frequency stability preserving – Plug-and-play capability of DERs – Circulating current avoidance among DGs – Damping of electrical behaviors |
| <i>Secondary</i> | <ul style="list-style-type: none"> – Compensating voltage deviations caused by primary control functionalities – Compensating frequency deviations caused by primary control functionalities – Ensuring that electrical levels (specifically, frequency and magnitude of microgrid voltage) into the microgrid are within nominal ranges – Providing synchronization with the mains for seamless transitions among the grid-connected and islanded operation |
| <i>Tertiary</i> | <ul style="list-style-type: none"> – Optimal operation in both the grid-connected and islanded modes of operation – Power flow control in grid-tied mode |

Table 2.2: Proposed control hierarchy for low-voltage microgrids [81]

| Control Layer | Functionalities |
|----------------------|---|
| <i>Zero-level</i> | <ul style="list-style-type: none"> – Control of output currents and voltages – Resonance damping |
| <i>Primary</i> | <ul style="list-style-type: none"> – Management of local energy sources (e.g., smoothing of power profiles, control of ES device) – Reactive and harmonic compensation of local loads – Local voltage stabilization (e.g., overvoltage provisions) – Current and voltage stability provision – Damping of long-term electrical behaviors |
| <i>Secondary</i> | <ul style="list-style-type: none"> – Load power sharing – Exploitation of DERs for microgrid needs – Achieve general optimization objectives (e.g., minimization of losses, restore the magnitude and frequency of microgrid voltage) – Ensuring that electrical levels (specifically, frequency and magnitude of grid voltage) of the microgrid are within nominal ranges – Adaptation to particular operating conditions (e.g., grid-connected/islanded operation) |
| <i>Tertiary</i> | <ul style="list-style-type: none"> – Power flow scheduling between microgrid and main grid – Power flow control in grid-tied mode (including unbalance, reactive, and harmonic compensation) – Fault and islanding detection and management at microgrid level – Microgrid synchronization with the main grid |

supply to local loads in case of microgrid failure.

- *Secondary control*: comprises control functions that require additional information than those belonging to the primary control layer (e.g., measures from neighboring units). It includes every control function that may require a coordination among agents and that may be implemented to *improve* the global operation of the microgrid. Examples are: stabilization of voltage profiles, reduction of distribution and conversion losses, effective load power sharing among EPPs, prevention of potential instabilities caused by saturation of EPPs' power limits or of storage devices.
- *Tertiary control*: comprises control functions involving a direct interaction of the microgrid with the main grid (e.g., the distribution system operator). Tertiary control is then committed to manage the interaction between microgrid and utility in grid-connected mode, ensure effective control of the power flow at the utility terminals and provide smooth transitions from grid-connected to islanded mode and *vice-versa*.

The control functions organized according to the hierarchy referred to in [71, 80] and the hierarchy considered herein are reported in Table 2.1 and Table 2.2, respectively. In the following the control techniques of the various control layers are classified and reviewed.

2.2 Zero-level Control

Electronic power converters (EPPs) interfacing DERs to the grid are commonly controlled as current sources. Current controlled EPPs (CC-EPPs) present the main advantage of having a minimal impact on the impedance seen at the point of connection, which is beneficial to preserve the stability of the hosting electrical system. In addition, CC-EPPs present fast dynamic response and robustness against perturbations and parameter variations. The main disadvantages lie on the fact that the generated quantity by CC-EPP (i.e., output current) depends on a locally generated reference, which has to be properly shaped in order to fulfill network needs. Voltage controlled EPPs (VC-EPPs) are often considered in the literature, especially when droop-based networks are concerned. The advantages of controlling EPPs

as voltage sources owe to the fact that, if properly synchronized, parallel connected VC-EPPs may naturally guarantee a controlled voltage at the point of connection, regardless of the presence of a stiff voltage source within the hosting electrical system. This implies an inherent capability of operating islanded from the main grid and an automatic ability to contribute to the needs of current within the electrical system. On the other hand, specific provisions are required to regulate, or, in case of multiple VC-EPPs, coordinate, the provided current contributions; indeed, the main issues of adopting VC-EPPs in microgrids stem from the intrinsic criticalities in operating voltage sources connected in parallel via small interconnection impedances (this falls in the scope of primary control).

The operation of grid-tied EPPs in microgrid applications presents various technical challenges. EPPs connected to microgrids are expected to operate reliably and contribute in improving the quality of electrical supply in an environment characterized by:

- transitory phenomena, occurring during transitions in operating modes (e.g., transitions to and from the islanded operation);
- intermittencies, introduced by abruptly varying inputs (e.g., discontinuous generation from renewables, connection of loads);
- widely varying system parameters, caused by the natural variability of the system structure (e.g., islanded operation *versus* grid-connected operation, connection of new resources);
- parameter uncertainty, due to the complexity and adaptability of the system;
- disturbances, caused by distorted voltage waveforms and circulating currents.

These issues are tackled in the literature in two ways, by devising new high performance control techniques and by devising optimum design methods. The most significant techniques and methods from the point of view of the following chapters are now described.

2.2.1 Linear Control

Linear controllers, specifically, the proportional integrative derivative (PID) and the proportional integrative (PI) compensators, have been the most popular controllers for many

years. By adopting the basic PI or PID implementations satisfactory performances and robustness to parameter variations can be obtained, on the other hand, they easily suffer of non-negligible steady-state errors. Solutions based on the internal model principle are commonly employed to reduce steady-state errors in AC applications. The internal model principle states that the tracking errors reduce asymptotically to zero if a model of the exogenous inputs is included in the control loop [82].¹ Accordingly, resonant or multiple-resonant and repetitive blocks are included in the regulator to minimize steady-state errors [9, 28, 33, 83–89].

Equation (2.1) represents a proportional-resonant (PR) regulator:

$$G_{PR}(s) = k_p + \frac{k_i s}{s^2 + \omega_c s + \omega_0^2}, \quad (2.1)$$

where k_p is the proportional gain, k_i the resonant gain term, ω_c is the resonant bandwidth, and ω_0 the resonant frequency [9, 28, 33]. Analogously, the *multiple resonant* version of the filter is:

$$G_{PMR}(s) = k_p + \sum_{h=1,3,\dots} \frac{k_{i,h} s}{s^2 + \omega_{c,h} s + \omega_{0,h}^2}. \quad (2.2)$$

For what concerns *resonant filters*, that is, those filters including a virtually infinite number of resonances, different implementation techniques are discussed in the literature [84, 85, 88, 89]. Recently, the resonant filter reported in Fig 2-1 has been successfully employed to enhance steady-state performances of H^∞ controllers [82, 84, 86, 90, 91]. It can be derived considering a unity gain amplifier with a positive feedback block constituted of a delay (i.e., e^{-sT_r}):

$$G_R(s) = \frac{1}{1 - e^{-sT_r}}. \quad (2.3)$$

The filter G_R presents a series of poles with resonant frequencies $w_k = k\omega_r = k/T_r$, $k \in \mathbb{N}$. With the purpose of not altering the frequency band concerning the stability of the final system, a low pass filter [i.e., $1/(1 + s\tau_p)$] is introduced. Besides the beneficial damping effect given at high frequency, the low pass filter slightly affects the value of the resonant

¹For example, if a $1/s$ block is suitably included in the control loop of a system, then it shows zero asymptotic tracking error to a constant input signal; if $1/s^2$ is included, zero asymptotic error is achieved for ramp signals.

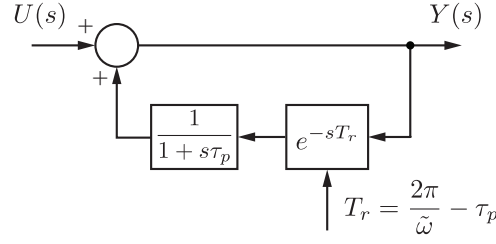


Figure 2-1: Repetitive controller described in [84].

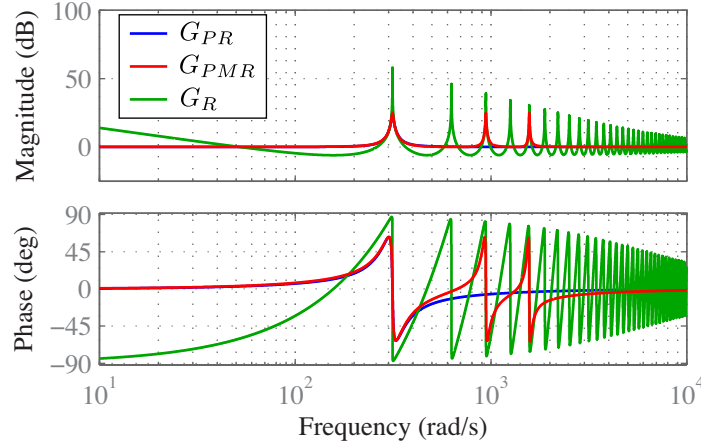


Figure 2-2: Resonant, multiple resonant, and repetitive.

frequencies. The correction term $-\tau_p$ of Fig. 2-1 is added to the time delay T_d to compensate this effect [84].

Even though effectively reducing to zero unwanted steady-state errors, these approaches are affected by some drawbacks correlated to the *learning time* of the internal models. Notably, resonant internal models present response dynamics lasting at least one cycle of the target frequency, which, consequently, cannot improve transient performances; instead, they can trigger unwanted oscillations in case of temporary perturbations. In addition, the effectiveness of the technique clearly depends on an adequate tuning of filter parameters (namely, the frequency of resonances), which may further increase the complexity of the final behavior and implementation. For these reasons in the following (specifically, in Ch. 6) the interest is focused on intrinsically fast controllers, especially for the inner control loops of EPPs.

Design Methods. Design methods from the optimal and robust control theory have been investigated for grid-tied converters. When the controlled plant is described by a set of

linear differential equations and performance is measured by a quadratic cost function, the design of a linear-quadratic regulator (LQR) provides the optimum control law. In this way a multivariable proportional regulator that considers all system variables can be obtained. Steady-state errors can be cancelled by adding the integrals of state variables in the model of the system. This approach is adopted in [92] to simultaneously regulate dc-link voltage, power factor, and dc-link neutral-point voltage balance of a three-level neutral-point-clamped voltage source inverter (VSI). If measured variables are highly affected by noise or some states of an observable system cannot be conveniently measured, then a Kalman filter can be combined with the LQR, obtaining in this way a linear-quadratic-gaussian (LQG) controller [93]. This approach is applied in [15] to design the controller of a grid-tied VSI with *LCL* output filter, under the assumptions of measurements highly affected by noise and small uncertainties in the plant description. Another approach employed to synthesize optimum controllers is the H^∞ method, which allows to find a stabilizing regulator featuring a defined degree of robustness against disturbances. The design process gives an optimum regulator, which is typically simplified in the PI or PID structure for implementation convenience. The advantages of the H^∞ method are often obtained by sacrificing speed of response and tracking accuracy. A method to overcome the issue on tracking accuracy is by adopting the internal model principle, as done, for example, in [84]. The application of H^∞ control to power converters for renewable energy and smart grid integration has been widely investigated by Zhong *et al.*, the results of the research are described in [82].

2.2.2 Predictive Control

The predictive control is generally a non-linear control approach that exploits the information available about the controlled plant to predict the values control variables have to assume to track, as best as possible, the given input references. In practice, the model of the controlled system is used to select, on the basis of a specific optimization criterion, the most suitable control action to achieve optimum reference tracking in the given operating condition.

Actually, predictive control comprises a family of different approaches [94]: dead-beat,

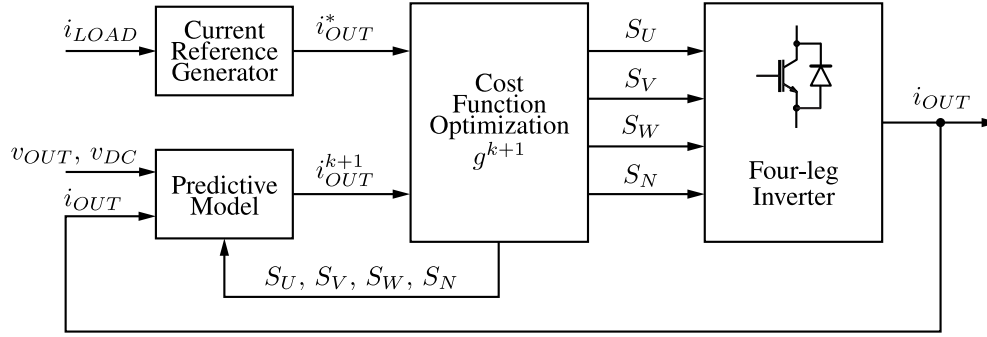


Figure 2-3: Predictive control of a three-phase active filter adapted from [101].

hysteresis-based predictive control, trajectory-based predictive control, model predictive control. Among these, the dead-beat technique [20,95–97] has been successfully employed in the control of active filters and drives for nearly four decades, while the model predictive control technique [98–101] is recently attracting significant interest thanks to its effectiveness and the availability of low cost, reliable, high performance computing platforms that allow its use to a broader range of applications, including the field of industrial and consumer power electronics [102]. A representative application example of the model predictive control to an active power filter for renewable power generation systems is presented in [101]. The general idea is represented in Fig. 2-3: for each state of the four-leg inverter, the *predictive model* block estimates the output current value (i_{OUT}^{k+1}) at the next sampling period, then the *cost function optimization* block chooses the state of the four-leg inverter that produces the minimum distance between the reference current i_{OUT}^* and the estimated current i_{OUT}^{k+1} with respect to a particular *cost function* (g^{k+1}).

For what concerns the dead-beat control, the control target is to make zero the control error in a predefined number of control steps. This is done by computing the needed control actions on the basis of the state and the model of the plant [103]. Model predictive controllers [98] differs from dead-beat controllers for having the more generic target of minimizing a cost function over a finite *prediction horizon*. The controller predicts the plant states that would be assumed with the application of a set of possible input values. The prediction is done using a model of the controlled plant initialized with the latest measured, or estimated, state variable values. Finally, a constrained minimization method computes the optimum sequence of input values, of which only the first element is eventually actuated.

The definition of proper cost functions is a critical aspect for which there is still a lack of accepted methodology [104].

The family of predictive controllers are characterized by good regulation performances, the capability of easily handling non-linearities of the controlled system, and the possibility of taking into account multiple control objectives. On the other hand, accurate modeling of the plant and knowledge of system parameters are necessary, especially for dead-beat controllers. To this purpose on-line parameter estimation techniques [105, 106] (i.e., self-tuning) may be included in the implementation, which, though, increase controller complexity.

2.2.3 Hysteresis Control

Hysteresis control is a non-linear control approach whose operation principle is to maintain the difference (ϵ_x) of the controlled variable with its reference within a defined range of values $[\beta^-, \beta^+]$, called the *hysteresis band*, by driving the system with control signals making the controlled variable to increase as soon as $\epsilon_x \leq \beta^-$ and to decrease as soon as $\epsilon_x \geq \beta^+$. Fig. 2-4 represents the principle of operation of hysteresis controllers, Fig. 2-5 defines the relevant control quantities.

Hysteresis control is characterized by a couple of very valuable features, namely, the unconditional stability and the capability of achieving the maximum—hardware allowed—speed of response in the presence of large-signal perturbations of converter's operating conditions. In the control of VSIs, these features come with the drawback of a switching frequency that is dependent on input and output voltages and on variations of reference signals. This leads to various negative effects, such as poor filter performance, possible excitation of resonances, and audible noise. Extensive research aiming at achieving constant switching frequency is reported in the literature. The first fundamental contributions to this topic were given by Malesani, Tenti *et al.* [107–109] and by Holmes, Yao *et al.* [110, 111].

Besides a continuous activity on improving the frequency stability of hysteresis controllers, a significant research effort has been recently dedicated to the transition to fully digital implementations, not requiring, for example, analog comparators nor digital-to-

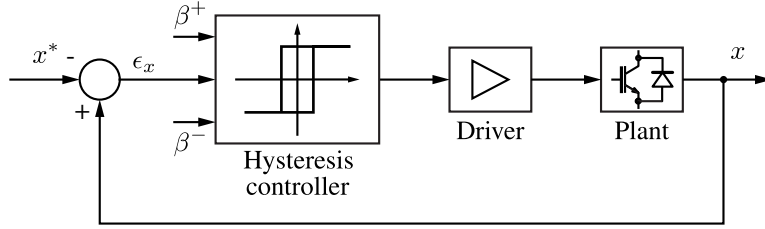


Figure 2-4: Scheme of a hysteresis controller.

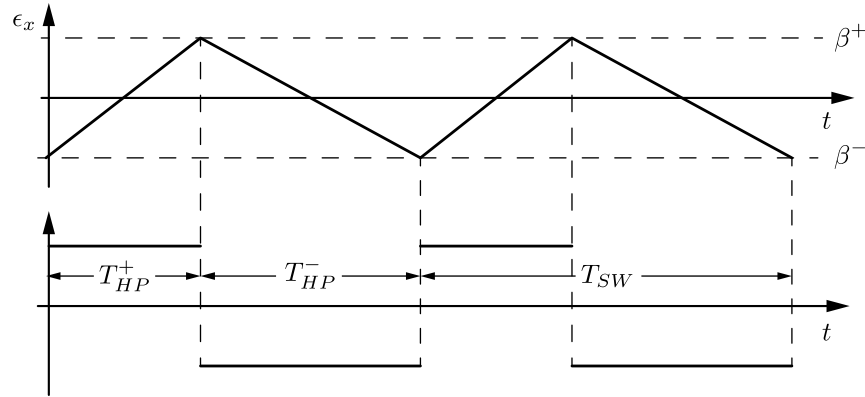


Figure 2-5: Variables of the hysteresis controller.

analog converters, but only an analog-to-digital converter [112, 113]. The advantages brought by fully digital implementations include the elimination of all typical analog circuit undesired effects (e.g., thermal drifts, offsets, noise sensitivity) and a considerable simplification of the circuit design and tuning.

2.3 Primary Control

Primary control provides the inputs to the zero-level control on the basis of the internal state of the EPP and the measured or estimated state of the microgrid. The primary control determines how DERs tend to contribute to microgrid operation in terms of delivered power, response to non-ideal grid conditions, response to anomalous grid conditions. These aspects are considered in this section. The possible behaviours of EPPs interfacing DERs are first generically described according to what reported in the literature, then more specific controllers aiming at improving the quality of the power delivered at the point of connection are discussed.

2.3.1 Converters Behaviour

The three classes of converters behaviour referred to in literature, that is, the grid-forming, grid-feeding, and grid-supporting behaviours [9, 114], are described in the following paragraphs.

Grid-Forming Converters

Grid-forming converters are controlled as ideal voltage sources with a typically sinusoidal reference voltage of amplitude E^* and frequency ω^* . Grid-forming converters are usually employed in stand alone applications to define the voltage of an isolated power system or in UPS applications [20, 87, 115]. Multiple grid-forming converters may also be employed connected in parallel. In [46] multiple voltage controlled sources receiving a common voltage reference are connected in parallel to constitute a power system with UPS features. Parallelism control circuits, which resemble the behaviour of virtual output impedances, are added to attenuate the negative effects (e.g., circulating currents) caused by non-idealities and improve the current sharing between the converters. Though, due to the very small output impedances, parallel connections of multiple grid-forming converters are usually avoided. Indeed, any mismatch in voltage references or inaccuracy in converter control and hardware may lead to unacceptable behaviours in terms of circulating currents.

Grid-Feeding Converters

Grid-feeding converters are controlled as ideal current sources, operating with a reference current corresponding to a given power reference (P^* , Q^*). Their control scheme is not meant to cause, intentionally, particular modifications to the voltage at the point of connection of the converter, therefore, grid-feeding converters can be safely connected in parallel to any stiff grid-voltage source without causing stability problems. Besides the traditional application in the connection of energy resources to the distribution grid, the combination of grid-feeding with grid-forming converters can be found in UPS power systems [116] and microgrid applications [117].

The resources connected—directly, or via a DC-DC converter—at the DC-link of a

converter can be renewable sources (e.g., PV source) or energy storage devices. For what concerns the active power reference generation (P^*), in the former case, it is done on the basis of the local active power production, which is driven by a maximum power point tracking (MPPT) algorithm; for the latter case, instead, various management approaches are proposed in the literature to optimize specific performance figures by exploiting the control flexibility brought by local energy storage. In both cases particular grid conditions may require limitations on the maximum active power injection from grid-connected converters. The definition of the reactive power reference (Q^*) is done referring to relevant grid codes (e.g., [118]), which commonly expect a reactive power generation that increases in proportion to the voltage deviation from the nominal grid voltage. The same concept is applied in more advanced control techniques in order to limit voltage variations in case of anomalous voltage conditions, these include reactive power absorption when grid voltage amplitudes transcend upper voltage limits; an example can be found in [119], where the Thevenin equivalent computed at the point of connection of the renewable source is employed to regulate the reactive power injection in case of overvoltage conditions.

Grid-Supporting Converters

Grid-supporting converters can be controlled as ideal current sources or ideal voltage sources, with references that are meant to contribute in sustaining the voltage at the point of connection. The behaviour is inspired by the self-regulation capability of synchronous generators, for which the delivered active power increases as grid frequency decreases, and the delivered reactive power increases as grid voltage magnitude decreases [120]. This behaviour, which appears favorable at least to improve voltage stability,² is commonly recommended in grid connection standards [73, 118], and inspired several authors in the development of local converter controllers with capabilities that resembles those of synchronous generators [66, 121, 122].

A significant study on current controlled grid-supporting converters applied to microgrids is reported in [123–125], which propose to exploit the intrinsic droop characteristics

²Indeed, further investigations on the effects of grid supporting functionalities are needed, like shown, for example, in [35] on the issue of unintentional islanding operation.

of resonant current controllers to sustain the grid voltage of *islanded* microgrids. In particular, it is shown that the physiologic deviation of the grid voltage frequency observable with a mismatch between generation and absorption causes resonant current regulators to introduce errors in the injected current that leads the phase angle of the injected current to match those of the current absorbed by loads. A voltage amplitude regulation and a power sharing approach based on local measurements are also developed. Instead, the effect of distorting loads on grid voltage quality is not discussed.

Despite of the fact that current controlled voltage-supporting converters may provide a valuable contribution in voltage regulation, the instantaneous output voltage at their output terminals is not regulated, making the use of current controlled grid-supporting converters alone delicate for the islanded operation. On the other hand, voltage controlled grid-supporting converters are capable to maintain a suitable quality of the grid voltage, and, therefore, can autonomously operate in islanded sub-grids. Because of that, the voltage controlled version is more popular in the literature [9], commonly constituting the elemental building block of droop controlled microgrids.

To explain, in general, the operating principle of grid-supporting converters, the circuit shown in Fig. 2-6 is now considered. At first, let's highlight how the power delivered by a voltage controlled source depends on other system parameters.

The complex power $\dot{S} := P + jQ$ delivered by source E to source V_0 is equal to:

$$\dot{S} = \bar{V}_0 \cdot \bar{I}_0^* = V_0 \cdot \left(\frac{Ee^{j\delta} - V_0}{Ze^{j\theta}} \right)^* , \quad (2.4)$$

by evaluating (2.4), the active power P and reactive power Q are then obtained as:

$$P = \left(\frac{V_0 E}{Z} \cos \delta - \frac{V_0^2}{Z} \right) \cos \theta + \frac{V_0 E}{Z} \sin \delta \sin \theta , \quad (2.5)$$

$$Q = \left(\frac{V_0 E}{Z} \cos \delta - \frac{V_0^2}{Z} \right) \sin \theta - \frac{V_0 E}{Z} \sin \delta \cos \theta . \quad (2.6)$$

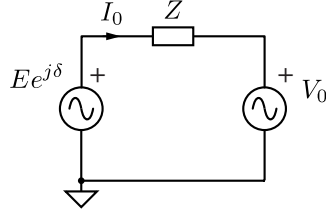


Figure 2-6: Interaction between two voltage controlled sources connected by an impedance.

Equations (2.5) and (2.6) can be written in matrix form as:

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} \sin \theta & \cos \theta \\ -\cos \theta & \sin \theta \end{bmatrix} \begin{bmatrix} \frac{V_0 E}{Z} \sin \delta \\ \frac{V_0 E}{Z} \cos \delta - \frac{V_0^2}{Z} \end{bmatrix}, \quad (2.7)$$

from which it is possible to define:

$$\mathbf{S} = \begin{bmatrix} P \\ Q \end{bmatrix}, \quad \mathbf{T} = \begin{bmatrix} \sin \theta & \cos \theta \\ -\cos \theta & \sin \theta \end{bmatrix}, \quad \mathbf{S}' = \begin{bmatrix} P' \\ Q' \end{bmatrix} = \begin{bmatrix} \frac{V_0 E}{Z} \sin \delta \\ \frac{V_0 (E \cos \delta - V_0)}{Z} \end{bmatrix}. \quad (2.8)$$

Equation (2.7) describes how the power delivered by the source depends on the equivalent line impedance and the difference in voltage magnitude and phase shift of the sources' output voltages.

In actual distribution networks only small phase shifts among generators occur, so that the approximation $\sin \delta \simeq \delta$ and $\cos \delta \simeq 1$ may be employed. Then, considering the network parameter $Z e^{j\theta}$, the following significant cases can be distinguished.

- *Resistive networks*, or, more generally, when it is possible to assume $\theta = 0$, active and reactive power terms result:

$$P = \frac{V_0}{Z} (E - V_0), \quad (2.9)$$

$$Q = -\frac{V_0 E}{Z} \delta, \quad (2.10)$$

which shows that in networks that are predominantly resistive (i.e., high R/X grids), active and reactive power contributions can be regulated by adjusting, respectively, the magnitude and the phase of the reference output voltage of grid-supporting converters. Also, the control actions are, in a first order approximation, decoupled. In

this case, the basic droop law to be employed to provide a stabilizing effect on the operation of grid-supporting converters is:

$$V_{ref} = E \sin(\omega t) \quad \text{with:} \quad \begin{cases} E = E_{\text{rated}} - k_n P \\ \omega = \omega_{\text{rated}} + k_m Q \end{cases} . \quad (2.11)$$

- *Inductive networks*, or, more generally, when it is possible to assume $\theta = \pi/2$, active and reactive power terms result:

$$P = \frac{V_0 E}{Z} \delta, \quad (2.12)$$

$$Q = \frac{V_0}{Z} (E - V_0), \quad (2.13)$$

which shows that in networks that are predominantly inductive (i.e., low R/X grids), active and reactive power contributions can be regulated by adjusting, respectively, the phase and the magnitude of the reference output voltage of grid-supporting converters. As observed in the previous case, the control actions are, in a first order approximation, decoupled. In this case, the droop law to be employed is:

$$V_{ref} = E \sin(\omega t) \quad \text{with:} \quad \begin{cases} E = E_{\text{rated}} - k_n P \\ \omega = \omega_{\text{rated}} - k_m Q \end{cases} . \quad (2.14)$$

Equations (2.11) and (2.14) represent the fundamental relations on which the conventional droop control of voltage controlled grid-supporting converters is based.

For the generic case in which neither of the two main behaviours (i.e., resistive or inductive) dominates, an approach taking into account the effect of generic output impedances is presented, for example, in [42]. The transformation (2.7) is directly applied to map, via \mathbf{T}^{-1} , the delivered output power (P , Q) in a space where the transformed components (P' , Q') can still be controlled by employing (2.14). This principle constitutes the basis of droop control strategies [42,63,126]. Clearly, applying \mathbf{T}^{-1} to decouple the control actions requires the adoption of proper tools to estimate parameter θ (e.g., [127,128]), which may

increase the overall implementation complexity. Other approaches propose to compensate the lack of knowledge on grid parameters by adding virtual impedances to the voltage control loop of voltage controlled grid-supporting converters [69, 129]. Virtual output impedances are also employed in [130] to improve harmonic current sharing among converters, though, it can result in higher voltage distortion in case of islanded operation. Recently, by allowing communication among converters, or with a centralized controller, strategies that further improve the reactive and harmonic power sharing performances of droop controlled systems have been proposed, like, for example, those described in [28, 65]. These are discussed further in Sec. 2.4.

2.3.2 Controllers for Enhanced Power Quality

The proliferation of non-linear loads and grid-interface converters in low-voltage grids has risen some concerns on the quality of the power delivered to converters. The absorption of distorted currents by non-linear loads has detrimental effects on grid voltage quality [131–133], in particular in case of weak grids (i.e., in grids with non-negligible connection impedances), such that grid connection standards define stringent limitations for harmonic current injections (see, e.g., Table 2.3 [134]). In addition, to limit switching noise injection and attenuate the generated electromagnetic interferences [135] DER-interfacing converters are equipped with LC or LCL output filters that, on the other hand, may trigger resonances with other components of the grid (e.g., line inductances, passive compensators), as shown in [136]. Research papers recently published on these issues—to be more specific, the former issue concerning harmonic compensation, the latter concerning harmonic damping—show that the interfaces of DERs based on power electronics converters, indeed, may help to improve both the aspects (see, e.g., [137]).

Recent research contributions are based on the harmonic voltage detection technique, which was firstly explored by Akagi *et al.* to damp power system resonances, prevent harmonic propagation, and contribute in providing locally the harmonic currents needed by the loads [138]. Notably, the focus is here on investigating the application of such method to manage harmonic issues in low-voltage distribution grids or in power electronics based

Table 2.3: Harmonic current distortion limits for systems rated 120 V through 69 kV [134]

| | Individual harmonic order (odd) ^(a) | | | | | TDD |
|---------------------|--|-------|-------|-------|-------|-----|
| | < 11 | 11-16 | 17-22 | 23-34 | 35-50 | |
| Maximum current THD | 4.0 | 2.0 | 1.5 | 0.6 | 0.3 | 5.0 |

^(a) Even harmonics are limited to 25% of the odd harmonic limits above.

power systems. Representative examples that deserve to be reported can be found in [137], where the integration of such methods in DG-interfacing converters (e.g., PV converters) to compensate harmonic currents in low-voltage grids is evaluated; and in [29], where an active damper aiming at stabilizing power electronics based AC systems is studied, the Middlebrook stability criterion [139] is adopted for stability assessment.

Further details on harmonic provisions for EPPs interfacing DERs are discussed in the following. Control schemes based on voltage control, current control, and hybrid voltage and current control are discussed individually.

Current Control Based

Fig. 2-7 represents the control scheme for harmonic compensation in a *current controlled* converter. The converter can be controlled to attain one of the following objectives:

- compensation of the harmonics contained in the line current i_G ;
- compensation of the harmonics contained in the local load current i_{LL} ;
- compensation of the harmonic currents distorting the local voltage v_{PCC} .

To the purpose, compensator G_C can be employed to tightly control or to simply damp the dynamics of the inductor current i_L . The grid current compensator G_C^{grid} aims at controlling the line current i_G . In [27], a proportional gain constitutes compensator G_C , and a proportional controller with multiple resonances constitutes the grid current controller G_C^{grid} . G_C^{grid} presents a resonance at grid frequency, which allows to regulate the power exchanged with the main grid, and a series of resonances at the odd multiples of the grid frequency (e.g., 3-rd, 5-th, 7-th) to regulate the corresponding harmonics. The reference

for the fundamental current $i_{G,f}$ may be built by using the parallel and orthogonal components given by a synchronization block (e.g., a PLL) to regulate the output power flow to match references P^* and Q^* . On the other hand, harmonic compensation depends on how current reference $i_{G,h}^*$ is defined. In [27] three possibilities are contemplated, which are also reported in Fig. 2-7, namely:

- $i_{G,h}^*$ equal to zero. This makes the grid current i_G injected by the power converter ideally free of harmonic components, as recommended by grid connection standards [134].
- $i_{G,h}^*$ derived from the measured local load current i_{LL} with an harmonic extraction block (H_D). This allows to cancel, in steady-state, the harmonic currents generated by the local load i_{LL} .
- $i_{G,h}^*$ derived from the measured PCC voltage v_{PCC} with an harmonic extraction block (H_D) and the multiplication with $-1/R_V$. In this case, the converter emulates a virtual resistance of value R_V for the selected harmonics, allowing to eliminate (or at least reduce), in steady-state, the distortion that would affect the PCC voltage due to the distorted current absorption from the local load (i_{LL}) and the other grid-connected non-linear loads (i_{ML}). This has a double beneficial effect, firstly it allows to damp resonances due to the interactions between the reactive elements of the electrical infrastructure (e.g., line impedances) and other devices connected to the grid (e.g., capacitor banks, or employed for reactive power compensation); secondly, it reduces the equivalent output impedance of the converter, making it to naturally provide the harmonic currents required by non-linear loads, which, therefore, will not propagate to the main grid.

Voltage Control Based

Fig. 2-8 represents the control scheme for harmonic compensation in a *voltage controlled* converter. The converter can be controlled to attain one of the following objectives:

- compensation of the harmonics contained in the line current i_G ;

- compensation of the harmonic currents distorting the local voltage v_{PCC} .

To the purpose, compensator G_C can be employed to tightly control or to simply damp the dynamics of the inductor current i_L . The output voltage compensator G_V aims at controlling the generated voltage v_C . In [140], a proportional gain constitutes compensator G_C , and a proportional controller with multiple resonances constitutes the voltage controller G_V . G_V presents a resonance at grid frequency, which allows to regulate the power exchanged with the main grid, and a series of resonances at the odd multiples of the grid frequency (e.g., 3-rd, 5-th, 7-th) to regulate the corresponding harmonics. The reference for the fundamental voltage $v_{G,f}$ is computed according to the operation principle of grid-supporting converters, discussed in Sec. 2.3.1. The contribution on harmonic compensation depends on how voltage reference $v_{C,h}^*$ is defined. In [140] the harmonic term $v_{C,h}^*$ is derived from the measured PCC voltage, constituting the harmonic voltage control loop that involves the block τH_D in Fig. 2-8, which allows to modify the converter output impedance Z_{out} to $Z_{out}/(1 + \tau)$. The control scheme foresees three possibilities:

- $\tau > 0$, which further reduces the equivalent output impedance of the power converter, improving the quality of the voltage waveform.
- $-1 < \tau < 0$, which increases the equivalent output impedance of the power converter. This tends to reduce the output voltage quality if load currents i_{LL} or i_{ML} are distorted, though, it attenuates the harmonic current at the output of the voltage controlled converter (e.g., to comply with grid connection standards) and reduces harmonic current circulation among voltage controlled converters.
- τ equal to zero. With respect to the previous cases, this corresponds to an intermediate situation in which the converter behaves as a conventional grid-supporting converter. In this case the harmonic load current is shared between the converter and the grid in inverse proportion of the connection impedances.

It is possible to observe that the advantage of having the control of the voltage at the output of the converter is traded off with flexibility and effectiveness in harmonic-damping / harmonic-compensation with respect to the CCM case.

Hybrid Voltage/Current Control

Fig. 2-9 represents the control scheme for harmonic compensation based on the hybrid *voltage and current control* scheme proposed in [16, 21]. The control scheme combines the advantages of CCM and VCM that are described above, notably, the control of the harmonic currents and the control of the grid voltage fundamental component. Harmonic compensation control is able to attain one of the following objectives:

- compensation of the harmonics contained in the line current i_G ;
- compensation of the harmonic currents generated by the local load i_{MG} ;
- compensation of the harmonic currents distorting the local voltage v_{PCC} .

While, the control of the fundamental grid voltage component is employed to control the output power flow and enables the operation islanded from the main grid.

This control scheme is presented in [16]. The compensator G_C is a simple proportional gain used to damp the dynamics of the inductor current i_L , the grid current compensator G_C^{grid} aims at controlling the *harmonic* content of the line current i_G and is implemented with a resonant filter with multiple resonances and a small proportional gain, the grid voltage compensator G_V aims at regulating the output voltage *fundamental* component and is implemented with a single-resonance filter. G_C^{grid} presents resonances *only* at the odd multiples of the grid frequency (e.g., 3-rd, 5-th, 7-th), limiting its effect to the harmonics of the fundamental quantities; whereas G_V is tuned at the grid voltage fundamental frequency, with the purpose of regulating the power exchanged with the main grid. The reference for the fundamental voltage $v_{G,f}$ is computed according to the operation principle of grid-supporting converters, discussed in Sec. 2.3.1. On the other hand, the behaviour from the point of view of harmonic compensation depends on how current reference $i_{G,h}^*$ is defined, which can be set as described in the previous case, relevant to the CCM scheme.

2.3. Primary Control

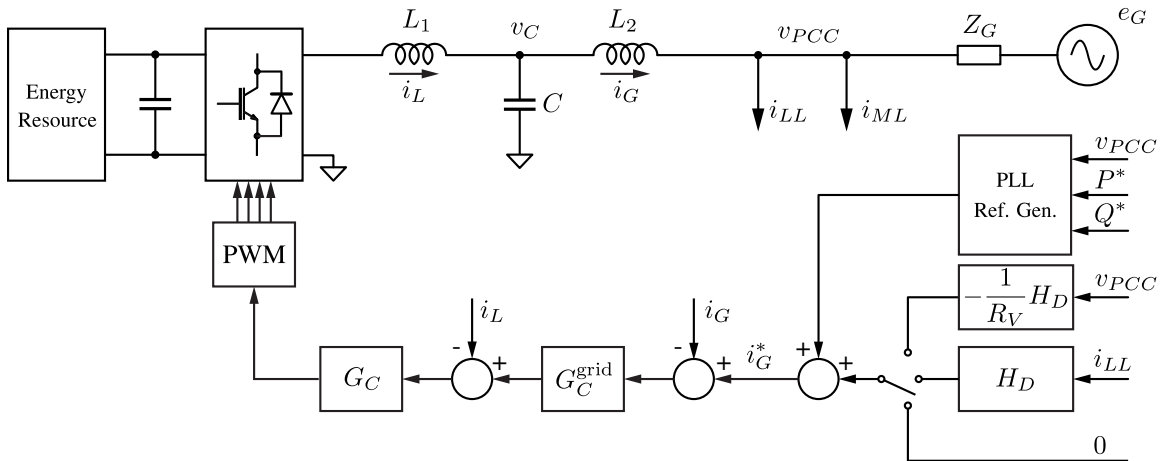


Figure 2-7: Harmonic compensation scheme for current controlled converters.

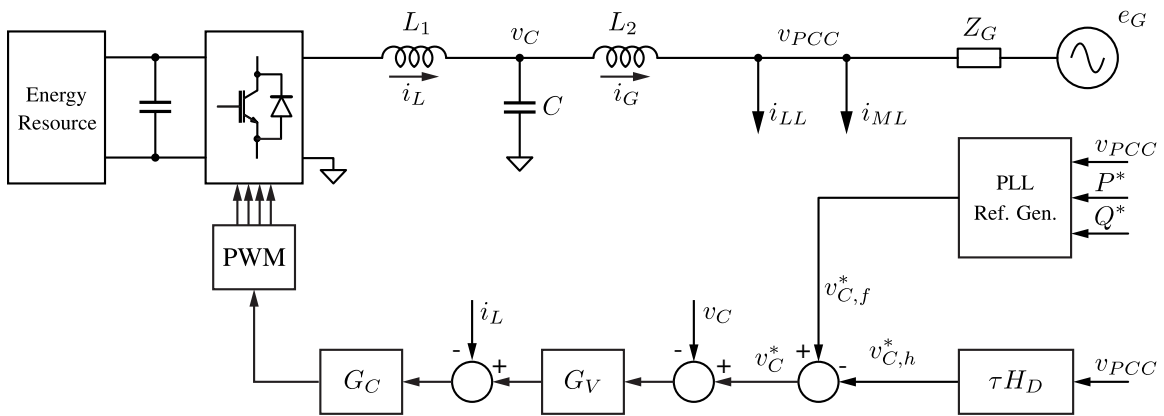


Figure 2-8: Harmonic compensation scheme for voltage controlled converters.

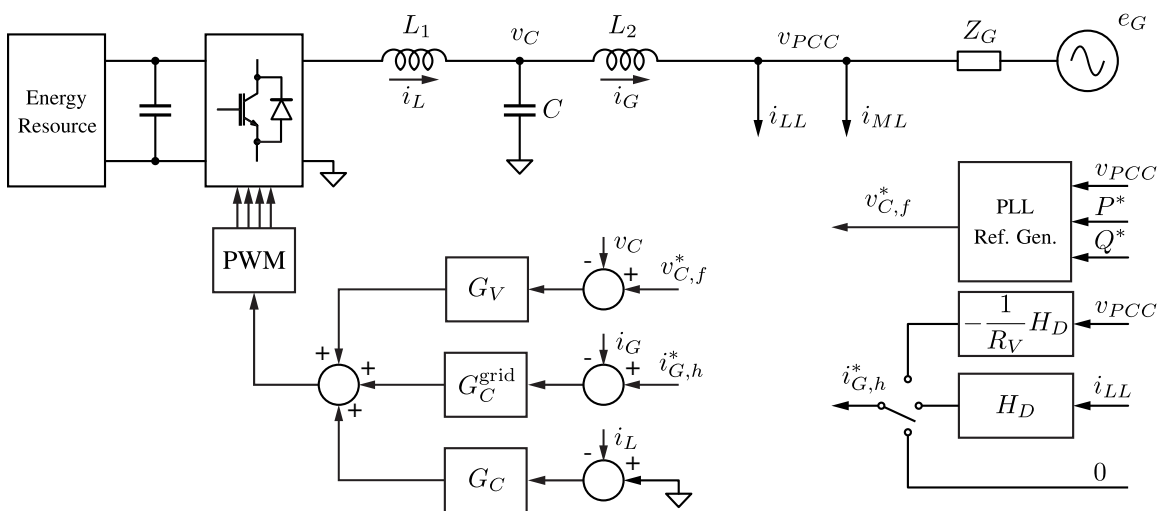


Figure 2-9: Harmonic compensation scheme for a hybrid voltage and current controlled converters.

2.4 Secondary Control

Secondary control concerns the operation of multiple interconnected DGs. It provides the inputs to the primary control on the basis of generation and loading conditions to allow a stable operation of DGs and loads. This can be achieved by properly assigning tasks to DGs and defining how these contribute to the needs of the microgrid. In this section these aspects are presented in two subsections. The first describes the principal ways parallel connected converters can be organized to obtain systems able to supply loads effectively. The second subsection reports some of the approaches proposed in the literature to define power references to DGs in order to fulfill power needs in an optimized fashion.

2.4.1 Operation of Parallel Connected Converters

The coordination of multiple parallel connected converters to effectively supply load's needs can be achieved in different ways. The most popular techniques are described in the following. A systematic review on the subject can be found in [76, 77, 141].

Centralized Control

In the centralized control approach distributed converters are controlled as current sources with a reference current set by a centralized controller. The centralized controller knows the total load current absorbed by loads and shares this current, by a feedforward loop, to the distributed converters. An outer feedback loop measures the voltage across the load and compensates, in steady-state, for uncertainties of the model (e.g., faults of some distributed converters). This approach can achieve an accurate power sharing among converters and shows a moderate degree of robustness with respect to failures affecting some decentralized converters. Among the drawbacks, the need of high-speed, low-noise communication channels to support measurement and reference exchange and the presence of the single point of failure constituted by the centralized controller. An enhanced variant is the one proposed in [48] for islanded microgrids. By means of frequency partitioning, the control is partitioned between a low-bandwidth controller that is placed centrally and supplies part of the reference current to the converters and high-bandwidth controllers distributed lo-

cally to each converter. With this approach, the set of converters behaves as a single, large converter with a full bandwidth controller, while the communication channel can present limited bandwidth.

Master/Slave Control

In the master/slave approach one voltage-driven converter behaves as control master and the other converters are current-driven and behave as control slaves. Slave units embed the functionalities to define their output power, so that the master unit has only to guide the behaviour of slave units and provide transient currents. The fundamental operation of such control organization with a pre-defined sharing criterion was firstly described in [142] for stand alone power systems; in [116] an enhanced version of the approach is proposed, where communication requirements are lessened by communicating to slave units only the average (RMS) value of reference currents. As described, these particular master/slave approaches require relatively high-speed, low-noise communication channels to operate properly.

Average Load Sharing

In the average load sharing approach all the converters are voltage-driven, and communication channels are employed to provide synchronization (via a synchronization bus) and load power sharing (via a power-sharing bus) [143, 144]. To that purpose each converter communicates, through the power-sharing bus, its output current and receives as response the average power delivered by all the converters. This approach brings redundancy, due to the non-centralized structure and the operation of multiple voltage-driven converters; on the other hand, it requires dedicated communication buses for synchronization, and active and reactive power sharing. Approaches aiming at reducing communication busses have been investigated as well; in [46], for example, only the synchronization bus is used to synchronize the voltage-driven converters, while a *parallelism control* loop, embedded in the control structure of each converter, adjusts the generated voltage to ensure equal power sharing.

Droop-Based Control

According to [77], the droop method is based on a well-known concept in large-scale power systems, which consists of drooping the frequency of the AC generator when its output power increases. In the case of parallel-connected UPS inverters, the active and reactive powers supplied to the AC bus are sensed and averaged, and the resulting signals are used to adjust the frequency and amplitude of the UPS inverter output-voltage reference. To follow on from what is discussed in Sec. 2.3.1, droop control consists in coordinating the operation of parallel connected voltage-driven grid-supporting converters. This technique can achieve a stable interconnection of voltage-driven converters without requiring communication and, in addition, can increase the reliability of islanded power systems thanks to the presence of multiple voltage-driven sources. These features make droop methods compelling approaches, such that their application to islanded power systems in general and, in the last decade, to microgrids has been widely investigated by different research communities (e.g, automatic control [145–147], power electronics [63, 114, 148], power systems [64, 73]). Various issues have been pinpointed by the research activity and specific solutions proposed; even so, some of these issues are still open (see, for example, section VII in [141] or paragraph II.C in [80]).

The main challenges in designing droop-based microgrids that are capable of operating in both grid connected and islanded modes stem from the absence of communication in the solutions that were firstly proposed [126, 149], such that, as studies developed, communication has been gradually introduced to cope with specific issues. To give some examples, some interesting solutions are now reported. The general control hierarchy for microgrids that is usually taken as reference [80, 114] is formalized in [71], where low-bandwidth non-critical communication is regarded as unavoidable to control microgrid's frequency and voltage amplitude. Contribution [28] aims at achieving accurate reactive power sharing and harmonic compensation in single-phase microgrids, the goal is attained by a microgrid-level controller communicating with distributed converters to define reactive power sharing and guide harmonic compensation. In [150] the issue of load voltage regulation is tackled by using a local controller receiving the information on load's RMS voltage.

2.4.2 Coordination of Power Contributions

The highest priority objectives pursued in microgrid control are: *i)* ensure power balance during islanded operation, *ii)* attain efficient operating regimes during grid connected operation. Therefore, the control of power injection from DGs is a crucial aspect in microgrids operation. In principle, DGs in the interconnection scheme introduced in Sec. 2.4.1 can accept power-injection set-points provided by specific power sharing algorithms. Typically, these algorithms aim at calculating set-points for DGs so that to fulfill microgrid's power needs in a way that is *optimum* with respect to specific measures, which may include, for example, distribution losses, converter losses, voltage deviations, financial costs. In the following some representative approaches are reported.

In [151] a load sharing distributed algorithm based on the Additive Increase Multiplicative Decrease (AIMD) approach is described. In practice, according to the basic AIMD, which is taken from communication network theory, a DG increases with constant steps its power injection if load's power demand is not satisfied (additive increase), otherwise, if power demand is satisfied, the DG decreases its power injection of a defined ratio (multiplicative decrease). The paper extends the algorithm to achieve the optimum distribution of load's power demand among DGs with respect to their cost of operation. To this end each DG has only to know its cost function and receive the notification announcing if total power generation meets demand. The effectiveness of the algorithm is based on the assumption that costs of operation can be represented by quadratic cost functions.

The approach proposed in [152] tackles the problem of power sharing in two steps. Firstly it uses a so called day-ahead scheduler to pre-calculate the power each DG should produce along the following day, then it uses an intra-day scheduler to calculate the actual power set-points to be assigned to DGs. The day-ahead scheduler computes power set-points with the aim of minimizing the cost of operation given energy prices, generation constraints (i.e., saturation levels of DGs), status of energy storage devices, and forecasts on load absorption and DERs production. Then the intra-day scheduler computes the power set-points with the aim of minimizing the weighted sum of power deviations from the output of the day-ahead scheduler, distribution loss, and voltage deviations from nom-

inal values, and take into account the line ampacity constraints. Due to the non-linearity of the problem, the solution is found by iteratively solving a mixed-integer linear programming problem where the terms corresponding to losses and voltage deviations are linked to power injections from DGs by means of sensitivity coefficients calculated at the particular operating point.

In [153] the task of optimal power flow is tackled by means of a dynamic programming approach. Each microgrid component is accurately modeled, including operation efficiency and power and voltage constraints to obtain exact solutions. A peculiar drawback of the approach is that the numerical complexity rapidly grows as the number of DGs grows, it is reported that with four or five DGs the approach is feasible only if the system contains a few busses.

In [49] the problem of optimal reactive power compensation for the minimization of distribution losses is considered. To that purpose, the distribution grid is clustered into sections and the optimal reactive power flow is solved distributedly for each cluster.

As a common drawback of the approaches above, it may be remarked the fact of requiring the knowledge of the controlled power system and its status. Indeed, the topology and parameters of low-voltage distribution grids are typically not known and difficult to be retrieved automatically by grid-connected devices; in addition, the status of controlled systems varies significantly in time. Therefore, such kind of approaches may be fully effective in future highly automated distribution grids, whereas, at the moment, they would require premature, large investments in infrastructure to be deployed. From this viewpoint, other approaches, less demanding in terms of needed ICT infrastructures, have also been investigated to ease the penetration of such technologies in current low-voltage distribution grids. Examples are local compensation methods [154]—which, according to [155], can achieve almost 80% of savings in losses when compared to a centralized control that is based on solving the full optimization problem—or, typically, heuristic approaches to the optimal management of power contributions from DGs.

2.5 Tertiary Control

Tertiary control concerns the interaction of a system of DGs with the main grid. The interaction includes the alignment of voltage parameters, detection of the islanded operation, and regulation of the power flow with the mains. Tertiary control involves interactions with the mains to negotiate power profiles and with the microgrid to estimate its operating condition and to regulate the power and current exchange at the interface between the two systems. The following subsections describe some the approaches that are typically used to pursue the goals of the tertiary control considered herein.

2.5.1 Microgrid Synchronization

A power system may operate islanded or connected to the main grid, and switch between these two modes of operation. When islanded, the system may present voltage amplitude, frequency, or phase that are different from those of the main's voltage, therefore, resynchronization with the mains is necessary prior to transitioning to the grid-connected operation. Various synchronization techniques suitable for specific microgrid configurations are discussed in the literature. Some representative techniques proposed for microgrids with the master/slave and the droop-based control schemes are reported next.

Synchronization in Master/Slave Approaches

The synchronization of the microgrid with the mains in the master/slave approach is performed by the master DG. These are typically based on Phase-Locked Loops (PLLs). In [156] a SRF-PLL (synchronous-reference-frame-PLL) is employed to ensure accurate active and reactive power control during grid-connected operation and steady grid voltage parameters during islanded operation. To that purpose the parameters of the PLL's loop filter are changed on-line so as to adapt the speed of response to the specific operating situation. During resynchronization or grid connected operation, the PLL is fed with the voltage of the mains, otherwise the value of the q -axis projection performed in the SRF-PLL is overridden to zero so that the reference phase provided by the PLL only depends by a pre-assigned nominal frequency. A similar approach is also investigated in [157].

In [158] a second order generalized integrator frequency-locked loop (SOGI-FLL) is employed to provide the frequency and the magnitude reference to the master unit in both grid-connected and islanded operation. In particular, during the islanded operation, the damping factor of the SOGI filter is set to zero, so as to operate the SOGI filter like an oscillator. The structure of the SOGI-FLL is modified to be adaptive to the frequency of the mains. In [159] the problem of synchronizing with the voltage of the main grid DGs operating islanded is tackled with a different approach. The proposed solution makes use of the 1PPS signal provided by Global Positioning System (GPS) modules; the signal is composed of pulses that are spaced at intervals of one second and are synchronous between different modules. The approach employs a centralized controller that measures the mains' voltage and communicates, at each zero crossing of the main's voltage, the phase given by a PLL locked to its GPS signal; the distributed units compute, at each zero crossing of the local reference that is being synchronized, the difference of the phase transmitted by the centralized controller with the phase that is given by a local PLL locked to the GPS signal of the particular distributed unit; the computed difference is employed to synchronize the local reference by means of a further PLL.

Synchronization in Droop-Based Approaches

The synchronization of the microgrid with the mains in droop-based approaches is typically coordinated by a centralized controller, as in [160], or a DG leading the synchronization process, as in [64]. In [160] a microgrid where DGs embed active power *versus* voltage's phase (i.e., P/θ) and reactive power *versus* voltage's magnitude (Q/E) droop controllers is considered. The phase and frequency synchronization of the microgrid with the mains is achieved by means of a frequency variation command broadcasted to all the DGs, which use this command to modify the phase of their voltage reference. The frequency variation command is modified with the purpose of matching the microgrid frequency with a given frequency reference. This last frequency reference, on its hand, is equal to a nominal microgrid frequency plus an adjustment term that is modified in order to achieve synchronization of the whole microgrid with the mains. The adjustment term is produced by multiplying the mains' voltage with the quadrature component of the microgrid voltage (this multipli-

cation gives a measure of the phase shift between the two quantities). The same approach is adopted to obtain the synchronization of the magnitude of the microgrid voltage. In [64] the problem of synchronizing a microgrid populated by DGs implementing the voltage-based droop (VBD) is considered. The VBD is a variant of droop control that is suitable for resistive networks and can take into account the less dispatchable nature of renewables. According to the proposed approach, the synchronization procedure is exploited by making use of a special DG, chosen among those of adequate size installed near the PCC. The droop controller of this unit is modified to allow, by means of ramp functions, a gradual alienation of the converter's voltage, frequency, and phase to the one of the main grid. Thanks to the VBD, the other converters of the microgrid naturally accommodate these voltage adjustments without being affected, in steady state, by the varying microgrid voltage.

2.5.2 Detection of Islanded Operation

Islanded operation occurs when a microgrid is energized solely by one or more local sources while it is electrically separated from the main grid. The islanded condition is considered an unwanted situation in traditional power systems, because they are not equipped with the infrastructure needed to autonomously control their grid voltage. In this case, the islanded condition must be detected to undertake the necessary provisions (i.e., make distributed generators to disconnect). Differently, microgrids are equipped with controllers and energy resources that can support autonomous operation if a disconnection from the mains occurs. Still, a prompt detection of the islanded condition is necessary to ensure a smooth transition to the new operating mode.

Islanding detection techniques can be classified as active, passive, or hybrid. *Passive techniques* detect islanding conditions only on the basis of the analysis of measured grid quantities. The analysis may concern voltage amplitude ranges, presence of phase jumps, variations in harmonic content, variation of grid-impedance (with non-active measurement technique, like, for example [161]) presence of voltage unbalance in three-phase systems. The disadvantages of these methods are the difficulties in setting the thresholds that delimit different connection conditions, and potentially large non-detection zones. *Active*

techniques detect islanding conditions by observing how the power system react to perturbations that tend to modify in a particular manner the frequency, amplitude, or phase of the grid voltage. If the system is operating connected to the mains then the grid voltage is negligibly perturbed by this behaviour of DGs, otherwise, the affected parameter would transcend normal ranges. Though very effective, active techniques are characterized by impairing power quality and stability of the examined system. *Hybrid approaches* combine passive and active techniques by applying active techniques only in case an islanding condition is detected by a passive one. So doing non-detection zones and perturbation injections can be reduced as compared to the case of passive and active techniques, respectively.

A systematic review on islanding detection techniques is provided in [162].

2.5.3 Power Flow Scheduling with the Mains

The energy resources of a microgrid are coordinated to improve the quality of the interaction with the mains. The ability of scheduling resources to fulfill internal objectives is a crucial feature, on the basis of that a negotiation with the main grid can take place, allowing to accommodate, eventually, the requirements on both microgrid's side and mains' side. Aspects that are relevant here are:

- planning of energy exchange, which is linked with the costs associated with energy production and consumption;
- scheduling of daily power profiles for a more *deterministic* microgrid behaviour, indeed, the mains may reward the ability of a microgrid of bounding its power absorption within specified limits or—ideally—of following a pre-defined power profile;
- defining power quality requirements, in particular, in terms of unbalance in three-phase systems, reactive power flow, and harmonic content of the current flowing through the interface with the mains.

Such a planning/negotiation is a critical task requiring to process complex information (e.g., forecasts on power needs, trends in energy prices). The multi-agent systems technology [163] shows valuable features for such a control problem; a detailed discussion on this topic is provided, for example, by [164].

2.6 Summary

This chapter reviews the main issues in the control of electronic power processors in low-voltage microgrids. Microgrids are complex systems, such that to devise suitable ways to coordinate the interaction among constituting parts requires a careful analysis of multiple aspects. For the sake of generality, the matter is organized in four control layers, as follows.

- Zero-level control, concerning the elemental current and voltage control of electronic power processors. Within its scope, linear, predictive, and hysteresis techniques are introduced.
- Primary control, concerning the local behaviour of grid-tied electronic power processors. The grid-feeding, grid-forming, and grid-supporting converters' behaviour are described also reporting relevant examples from the literature.
- Secondary control, concerning the coordination of electronic power processors operating in parallel. Interconnection schemes and how microgrid's power needs may be shared among sources to obtain optimum operating regimes are described.
- Tertiary control, concerning the interaction of a group of electronic power processors forming a microgrid with the main grid. Within this scope, microgrid synchronization with the mains, islanding detection, and the interaction with the mains are described.

The discussion of the various aspects is supported by references to relevant literature so as to provide an overview of both the open issues and the state-of-the-art in microgrid control, from a power electronics' perspective.

Chapter 3

Development Methodology and Toolset

The aim of this dissertation is two-sided. From the one side, to propose effective control techniques for EPPs in low-voltage microgrids; activities within this scope are carried-on in the light of the literature review reported in Ch. 2. From the other side, to demonstrate the behaviour of the devised techniques when employed in operating conditions that are realistic and replicable in a laboratory environment. For what concerns the latter aspect, this chapter describes the methodology applied to develop and experimentally validate the techniques described in the following chapters (specifically, from Ch. 5 to Ch. 7). To cope with the complexity of the microgrid scenario, a *development methodology* based on rapid-control-prototyping and hardware-in-the-loop approaches, supported by a general purpose, flexible, scalable, and powerful *development environment* are employed. The methodology and the development environment are described in the following sections. The potential benefits and limitations of the chosen tools, whose application to the field of power electronics has been rarely documented before, are discussed by considering the development of an EPP interfacing DERs to the grid as a first reference application case. Applying the described methodology with the identified platform has allowed to *i)* smoothly transit between development phases, from concept to final realization, *ii)* rapidly develop controllers and testbeds integrating different systems interacting with each other.

3.1 Controllers for EPPs in the Microgrid Scenario

In order to illustrate the applied methodology and the chosen development environment, the following sections consider the control, and integration to a control architecture, of the fundamental power electronics building block [165] of the microgrid scenario, namely, the DER-interfacing EPP (i.e., an EPP that interfaces energy resources to the grid). As explained in Sec. 3.3.4, these concepts can be employed to manage more general cases. This is done in Ch. 5, for the development of the so called utility interface converters, in Ch. 6, for the development of high performance current controllers, and in Ch. 8, to allow the development of a complete, laboratory-scale microgrid experiment.

In future microgrids grid-tied EPPs will perform a variety of control functions. In the light of the state-of-the-art overview provided in Ch. 2, the operation of DER-interfacing EPPs will be the result of the application of decentralized control strategies, autonomous and local, and of the remote supervision by a centralized grid controller or dispatcher (e.g., [160, 166]), linked to the numerous EPPs by means of a suitable communication channel and a properly defined protocol [167]. Consequently, a lot of different stacked control functions have to be implemented in each single converter, ranging from the low level ones (e.g., pulse width modulation), to the high level ones, which include autonomous decision making algorithms and communication protocols. Digital control is applied at all levels of the stack, making the EPP's controller a complex, multilayer digital device [168, 169]. An example is provided in Fig. 3-1 for an EPP managing a PV source and a storage device; basic, specific, and ancillary services are indicated in the figure to remind that diverse functions have to be carried out concurrently.

Basically, two different approaches can be followed for EPP controller implementation. In the most conventional one, all control functions are developed in the form of software routines, executed by a digital signal processor (DSP) or, less frequently nowadays, a microcontroller. Another, more recent, approach takes advantage of the availability of easily affordable reconfigurable logic circuitry. In this case, control functions are actually defined in some hardware description language (HDL) and turned into application specific digital circuits. The former approach has the maximum flexibility, the latter guarantees higher

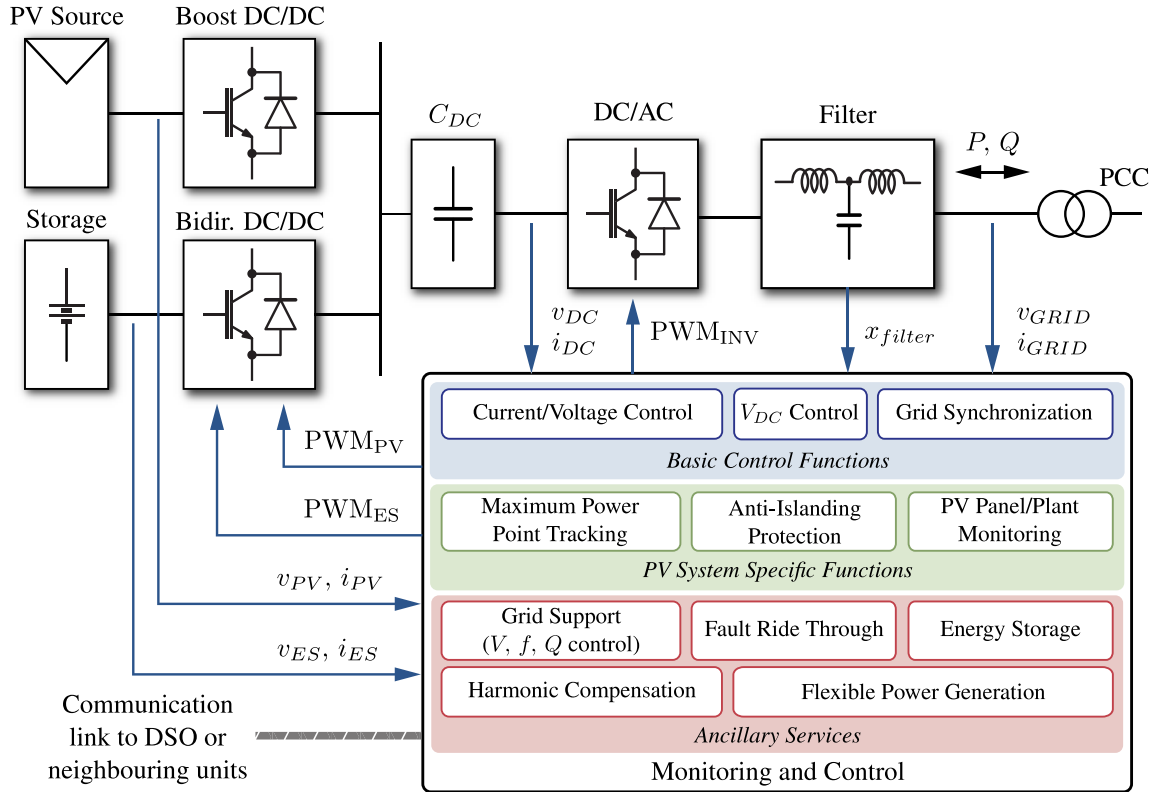


Figure 3-1: General structure of an electronic power processor that interfaces energy resources to the grid. Highlighted its local controller with the main control functions (adapted from [170]).

performance, mainly in terms of achievable sampling frequencies and control bandwidths.

In an attempt to meet the needs of complex applications, where both flexibility and performance, with particular reference to determinism, are simultaneously needed, new control platforms are being proposed on the market. Some are based on multi-platform systems integrated at board level, typically supporting real-time operating systems (RTOS); examples are those described in [171], which features RT Linux, and [172] that uses a proprietary system. In these devices, a processor—a DSP or a general purpose processor (GPP)—and an FPGA are combined. Other, radically different, solutions are represented by system on chip (SoC) architectures, like [173], where a DSP, a programmable logic device, and a so called *analog compute engine* are integrated on a *single chip*.

In this context, the following sections aims at *i*) identify typical requirements and implementation issues that are involved in the choice of a digital control platform for modern smart grid applications, *ii*) introduce a digital controller development and test methodology that integrates the spreading practice of real-time simulation [174–176] in the proto-

typing process of power electronics devices, *iii*) show the application of LabVIEW hardware/software toolsets as an effective means to rapidly prototype digital controllers and test set-ups for power electronic systems. To the purpose, a board-integrated multi-platform controller [172] is considered and used to develop the digital control stack for a 3 kVA voltage source inverter, meant to be used as the grid interface of a DERs-coupling EPP in microgrid experiments. The implemented functions include current control, phase-locked loop (PLL) based synchronization, real and reactive power control, fault detection, data logging, and communication with an external supervisor via an Ethernet communication channel. The chosen development platform, as compared to other state-of-the-art toolsets, offers several advantageous features, such as high performance, ease of use, different hardware configurations to meet specific end application requirements, and affirmed and widespread use—although mainly in other academic and industrial engineering fields.

3.2 System Architecture and Implementation Tools

The typical configuration of a DER-interfacing EPP in a single-phase low-voltage grid is shown in Fig. 3-1. In particular, it comprises a DC/DC stage, which deals with the management of local energy resources (e.g., PV source, fuel-cell, storage device), and a DC/AC (i.e., inverter) stage, which deals with grid interfacing. As can be seen, the two stages typically share a single control board. Only to the *second* stage, whose basic electrical scheme is shown in Fig. 3-2, is referred to in this chapter. The main purpose of the inverter controller is to guarantee locally synchronized current injection/absorption, so as to *i*) guarantee the maximum exploitation of the energy source or the appropriate utilization of the storage element and *ii*) concur to the determination of a satisfactory power quality throughout the grid. While the former objective can be met using locally available data, the latter may require the interaction with other EPPs or with a centralized microgrid controller (see, e.g., [28]).

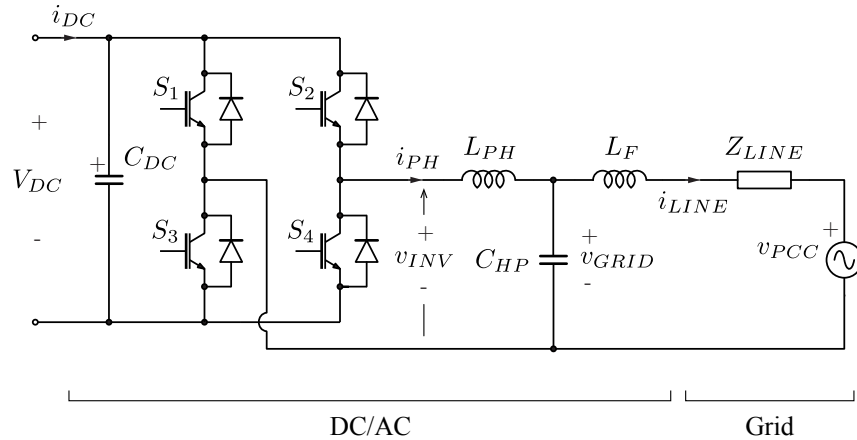


Figure 3-2: Basic representation of the typical DC/AC stage of a DER-interfacing EPP.

3.2.1 Control System Organization

In general, the controller's functions can be represented as a stack where lower level functions receive inputs from upper level ones. In turn, they provide data to the upper level functions that are used in the decision making algorithms, governing, for example, the power exchange with the grid. The typical structure of the control stack is shown in Table 3.1. As shown, the lower level functions (e.g., PWM, synchronization, electrical variable supervisors) are supposed to be implemented on a programmable logic device, like an FPGA. The basic reason is that they do not involve elaborate signal processing (fixed point arithmetic is perfectly viable), but require relatively high cycle frequencies, in the tens of kHz range. In addition, they require internal, jitter-free synchronization techniques (e.g., those between sampling and modulation processes) and highly reliable fault detection mechanisms. These features are easily implemented in a configurable digital chip. Instead, higher level functions, such as output power control or local grid characterization and optimization algorithms (see, e.g., [128]), make extensive use of signal processing functions (floating point is recommended) and, especially in the case of distributed implementations, of advanced communication capabilities. On the other hand, they do not necessarily require tight synchronization or strictly constant cycle frequencies. As a result, the natural implementation hardware for these functions is a DSP or, more and more frequently, a general purpose processor (GPP). Both devices are programmable in high level languages, which increases abstraction and flexibility. The GPP normally has the advantage of sup-

Table 3.1: Control function stack of a DER-interfacing EPP

| Subsystem | Functionality | Scope | Target |
|-----------|-----------------------------|-------------------|--------|
| Inverter | PWM | Local | FPGA |
| | PLL | Local | |
| | Current loop | Local | |
| | Fault detection | Local | |
| | P loop | Local | RT GPP |
| | Q loop | Local/Distributed | |
| | Grid voltage control | Local/Distributed | |
| | Grid characterization | Local/Distributed | |
| | Global optimization | Distributed | |
| DC/DC | PWM | Local | FPGA |
| | Input V/I control | Local | |
| | Source/storage optimization | Local/Remote | RT GPP |

porting real-time operating systems (RTOS), a very useful resource for this application, where reliability and determinism are crucial.

In the light of the discussion above, it is possible to conclude that the better suited controller for DER-interfacing EPPs is a multi-platform digital device comprising two domains *i*) a high performance hardware programmable device (e.g., a FPGA) and *ii*) a DSP or GPP, possibly supporting a RTOS. Further discussion on digital devices suitable for smart grid inverter control can be found in [168].

3.2.2 Implementation Issues

The main issues related to the implementation on multi-platform hardware of the control stack described by Table 3.1 can be identified in the following:

1. analog to digital conversion (ADC);
2. data consistency between platforms;
3. development tools;
4. debugging.

ADC

Using FPGAs for low level converter control normally requires the design of additional hardware including the ADC chip, signal conditioning, and data bus synchronization circuitry. This complicates significantly the controller development. In some systems, like the one described in [172] or [173], the ADC unit, and a lot of other I/O functions, are natively interfaced to the FPGA, so that the user does not need to implement the data path between the different devices. For SoC architectures, this comes with virtually no performance limitation (i.e., peripherals determine the maximum data throughput), while in multi-platform boards a certain degree of latency is introduced, which limits the maximum data update frequency to about 100 Mbit/s. In any case, it should be possible to design and easily integrate in the control system custom acquisition circuits to satisfy particular needs; this approach has been adopted in Ch. 6, where the sensing board described in Appendix A is used to implement the proposed high performance, digital current controllers.

Data Consistency

Perhaps the most complex issue in using multi-platform controllers, however, is guaranteeing data consistency among the different levels of the control function stack. The basic approach, where the logic circuitry is treated as a memory mapped external peripheral unit while data exchange and task scheduling in the DSP is regulated by interrupts, suffers from latency and often leads to timing jitter. Unless data processing functions are relatively limited in number or computationally light (not our case), establishing a consistent data exchange mechanism can become the system's bottleneck. It is worth remarking that this is a peculiar condition of this application field, where the computational burden of the DSP/GPP subsystem is, generally, quite heavy and articulated in several concurrent functions. A more efficient approach exploits a RTOS, where multi tasking and efficient data exchange mechanisms [e.g., based on direct memory access (DMA)] are built in the OS I/O functions and are almost transparent to the user. DMA channels typically offer multi Mbit/s bandwidths at minimum or even zero latency, which makes their usage compatible with the applications discussed herein. In systems on chip, like the one described in [173],

the data exchange between GPP and FPGA can reach the maximum performance, because the FPGA, the I/O resources, and the processor natively share the same data bus and memory, operating at the system's clock frequency. Still, to attain the efficient scheduling of functions can be a difficult task for the developer.

Development Tools

Integrated design environments (IDE) for multi-platform systems, when available, are often complicated to use, involving simultaneously both the typical tools for firmware/software development and those for HDL driven logic chip design. They require a skilled user that dominates both sides of hardware/software co-design or, possibly, a team of specialist users concurrently working on the same project. Some systems, like [172], offer instead a truly integrated design environment, namely, a common programming framework that unifies the FPGA and the DSP/GPP domains, greatly reducing development time. This is possible because the above mentioned issues, about the integration of I/O functions within the FPGA domain and the implementation of efficient data exchange mechanisms between the two domains, are managed almost transparently to the designer. For these reasons, the controllers considered herein has been developed on one of such systems. In addition, the chosen GPIC platform [172], is conceived to enable (relatively) low cost controller board designs, where a multi-platform structure and a single common programming design environment are always maintained, but the computational resources and I/O channel availability can be tailored to the specific application. The main features of the controller are listed in Table 3.2.

The resulting controller organization for a DER-interfacing EPP is shown in Fig. 3-3. In particular, in the lower part (light blue shaded area), the adopted partitioning of the different stacked control functions is detailed. In the upper part of the figure (light yellow shaded box), instead, the centralized controller is indicated, which supervises the correct operation of the microgrid and exchanges information with distributed EPPs through a suitable communication link.

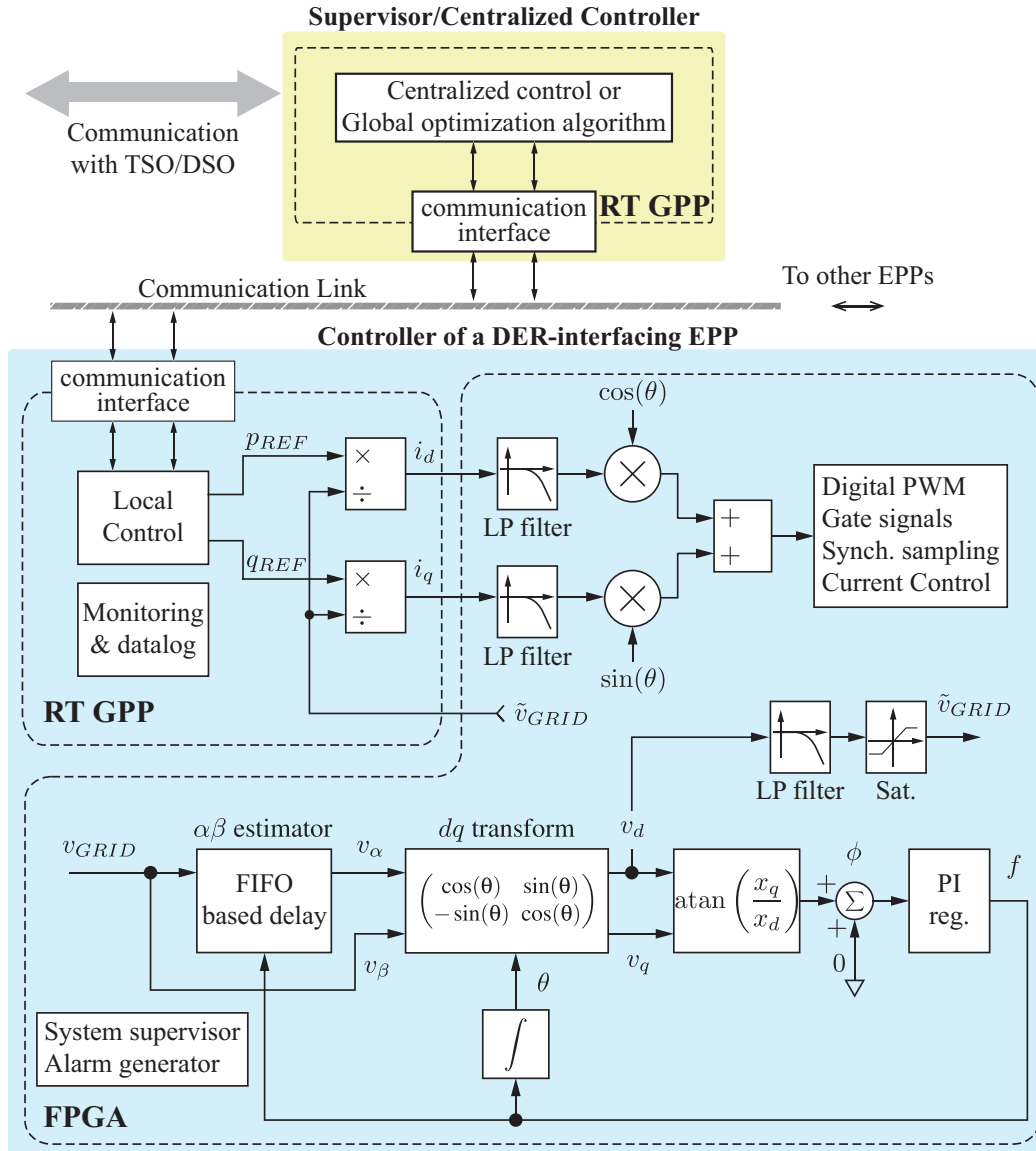


Figure 3-3: Schematic representation of the controller implementation on a multi-platform board of a DER-interfacing EPP: the controller is partly deployed on the FPGA module, partly on a RT GPP. The RT GPP hosts the higher level control functions and manages data logging and communication with the centralized grid supervisor through the Ethernet. In the upper-part the centralized controller, with indicated the communication with a distribution, or transmission, system operator (DSO, TSO).

Table 3.2: Characteristics of the chosen control platform (GPIC)

| Feature | Parameter | Value |
|----------------------|-------------------|---|
| Processor | Model | PowerPC |
| | Processor Speed | 400 MHz |
| Memory | Nonvolatile | 512 MB |
| | System | 256 MB |
| FPGA | Model | Xilinx Spartan-6 LX45 |
| | # Slices | 6822 |
| | # DSP48s | 58 |
| Network | Network interface | IEEE 802.3 Ethernet |
| Communication | Port | RS-232, RS-485 CAN, USB |
| Peripherals | Channel | 16 AI, 12-bit, ± 10 V, 100 kHz 14 ch., 500 kHz gate drivers ⁽¹⁾ |

⁽¹⁾ Only the used subset of the NI 9683 mezzanine-card ports is reported.

Debugging

Debugging a complex digital controller of the type described by Table 3.1 requires a long time and exposes the power converter hardware to damage hazards. In addition, the dynamic behavior of grid optimization algorithms is rather complicated to predict by pencil and paper calculations, while conventional simulation software requires very long computing times to produce useful results in non-trivial cases. Both of these issues can be solved by hardware-in-the-loop (HIL) real-time simulation. According to the methodology here adopted, the digital controller of the EPP has been developed and tested off-line, without even connecting it to the power converter, until its operational capability has been fully assessed. Thanks to a reconfigurable controller module of the type [177] a discrete time model of the grid interfacing stage of the EPP (including the full bridge, the output filter, and the grid) has been implemented and connected to the EPP's controller. This allows not only to significantly accelerate the simulation with respect to a standard simulation performed on a PC, but also to verify the functionality of the very same controller that will be connected to the physical converter.

Table 3.3: Characteristics of the chosen simulation platform (cRIO-9082)

| Feature | Parameter | Value |
|----------------------|-------------------|--|
| Processor | Model | Intel Core i7-660UE |
| | Processor Speed | 1.33 to 2.4 GHz |
| Memory | Nonvolatile | 32 GB (min.) |
| | System | 2 GB (min.) |
| FPGA | Model | Spartan-6 LX150 |
| | # Slices | 23038 |
| | # DSP48s | 180 |
| Network | Network interface | IEEE 802.3 Ethernet |
| Communication | Port | RS-232, RS-485/422, USB VGA, CAN, MXI-Express |
| Peripherals | Channel | 4 AO, 16-bit, ± 10 V, 100 kHz 8 Digital Input/Output ⁽¹⁾ |

⁽¹⁾ Specs of the used digital (NI 9401) and analog (NI 9263) modules.

The main features of the adopted RT simulation platform are listed in Table 3.3.

3.2.3 User Interface

The hardware/software integrated development environment (IDE) considered herein is LabVIEW. In this environment, the interaction with the user or the developer is achieved by means of *front panels*, which allow to organize the peripherals of the controller's hardware. When the FPGA program, called VI, is launched from the IDE, the corresponding front panel is automatically displayed on the development PC, enabling the user to set controls and view indicators. This allows the interaction with the FPGA VI at a typical rate of several updates per second, which is adequate to the purpose of monitoring the application during debugging, especially when real-time simulation is used. An even more flexible interface can be set-up through the RT GPP on board the GPIC control device which, in addition, provides a deterministic access to the FPGA application. More specifically, in this case, access to controls and indicators is programmed by the user, employing ready to use functions, and executed by the RT GPP. The RT GPP can be further programmed to

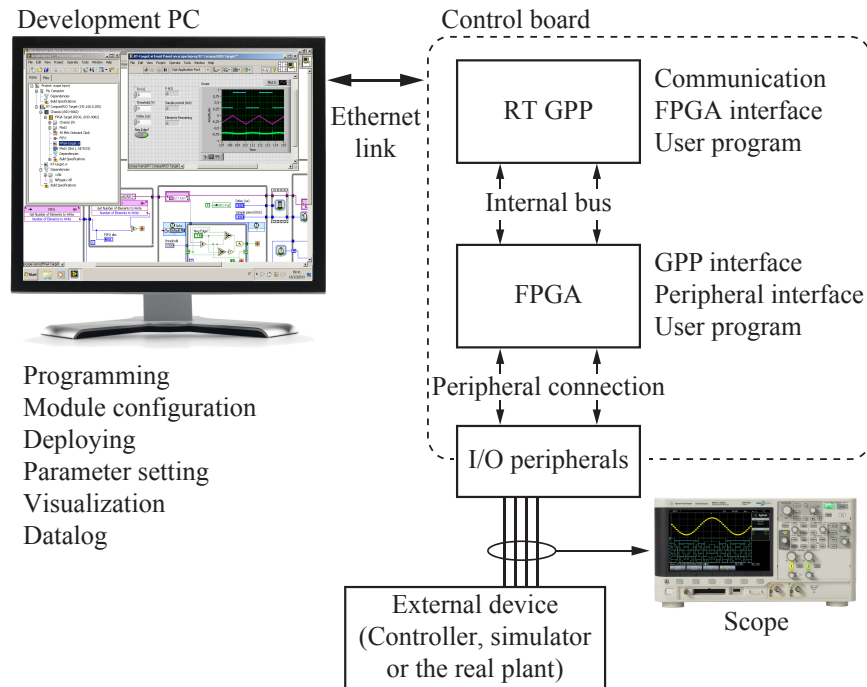


Figure 3-4: Typical system configuration with user interface.

generate stimulus signals, to acquire the system response, and to present data to the user (e.g., graphically via the front panel of its LabVIEW program). The communication between the development PC and the control board is provided by an Ethernet link, as shown in Fig. 3-4. A zoomed in view of the PC interface is provided in Fig. 3-5, where the characteristic graphical interface of the LabVIEW development environment and the appearance of the software interface (upper-right) can be better appreciated.

3.3 Controller Development and Test Methodology

The control stack for the DERs-coupling EPP of Fig. 3-2 has been developed according to the scheme of Fig. 3-3. As can be seen, basic low-level control functions are considered, whose design procedures are well known and whose implementation is straightforward. To complete the information conveyed by Fig. 3-3, symmetrical, centered pulse modulation has been implemented, with an equivalent 12.4 bit resolution. A proportional-integral (PI) current controller with a 2 kHz bandwidth and 60° phase margin has been used, together with output voltage feed-forward at the modulator input, so as to guarantee acceptable

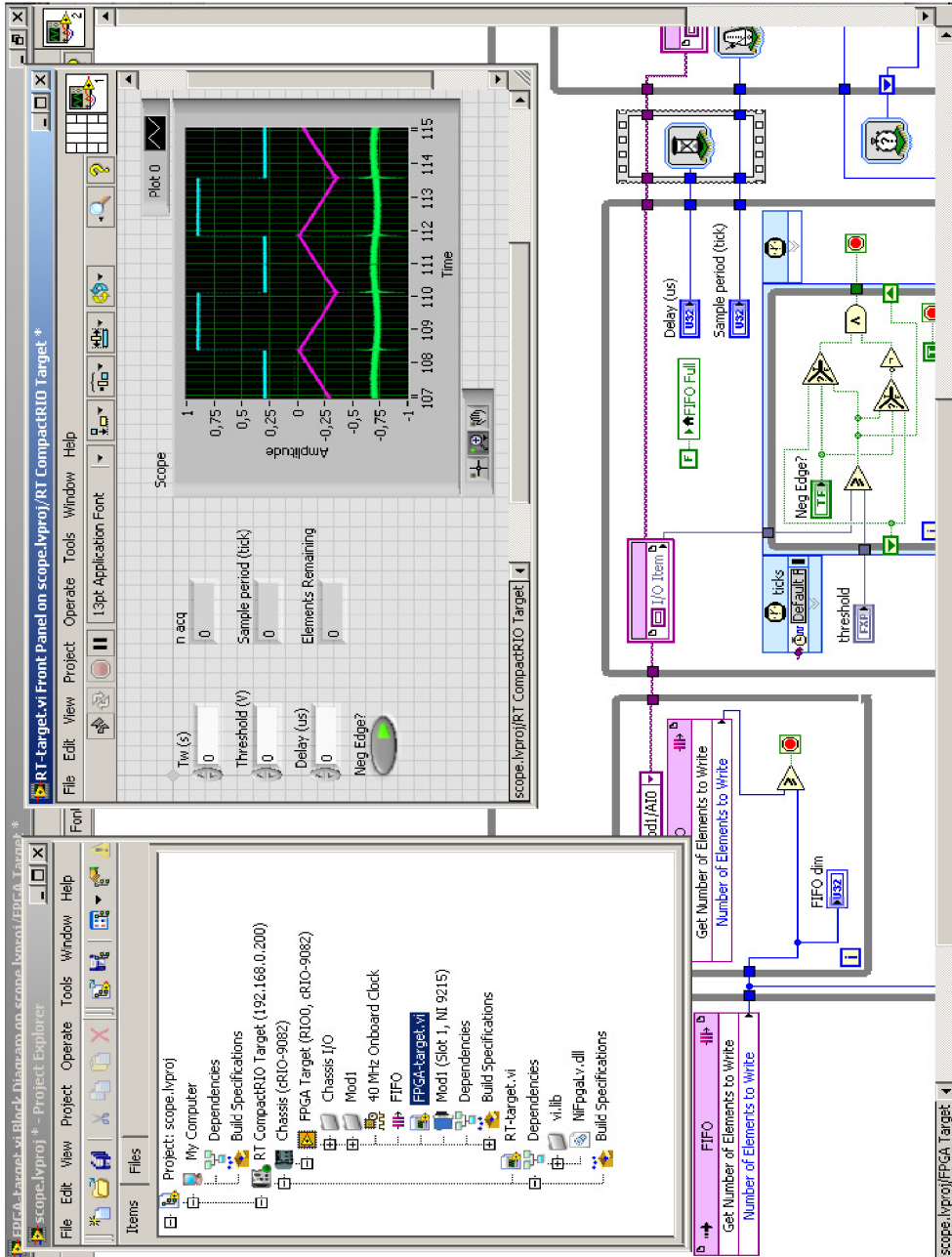


Figure 3-5: Zoom-in view of the PC interface.

rejection of disturbances at fundamental and lower order harmonic frequency. The parameters of the controller and of the hardware part shown in Fig. 3-2 are listed in Table 3.4.

Table 3.4: Inverter and PI current controller parameters

| Parameter | Symbol | Value | |
|----------------------------|-------------------|------------|------------|
| Nominal input voltage | V_{DC} | 400 | V |
| Switching frequency | f_s | 18 | kHz |
| Filter inductance | L_{PH} | 1.2 | mH |
| Series inductor resistance | $r_{s,PH}$ | 50 | m Ω |
| Output filter capacitance | C_{PH} | 10 | μ F |
| Output filter inductance | L_F | 45 | μ H |
| Current sense gain | $K_{sense,i}$ | 375 | mV/A |
| Voltage sense gain | $K_{sense,v}$ | 17.25 | mV/V |
| Rated power | S_o | 3 | kVA |
| Crossover frequency | f_{CR} | 2 | kHz |
| Phase margin | Φ_M | 60 | $^\circ$ |
| Carrier amplitude | $\pm A_r$ | ± 2777 | |
| A/D conversion delay | Δt_{AD} | 10 | μ s |
| PI calculation delay | Δt_{calc} | 0.1 | μ s |

The controller has been extensively tested in the three different ways that are described in the following subsections; in all cases, the results of the same experiment are shown. The experiment is represented by a step transition from 0 to 2 kW of injected real power, P , with reactive power, Q , set to zero, followed by a second step change where the injected power is transferred abruptly from the real (d) to the reactive (q) power axis. It is worth mentioning that DER-interfacing EPPs will hardly ever experiment such abrupt transients in real life, but, as usual, demanding test conditions are better suited to highlight the achievable performance levels. The considered grid parameters are listed in Table 3.5.

3.3.1 Simulink Model

As a first verification, the controller has been simulated on a PC, whose benchmarking score for Matlab is: [0.22 0.23 0.20 0.25 0.84 1.07]. In order to do that, a model of the system configuration that is shown in Fig. 3-2 has been developed. At the same time, the different control blocks of Fig. 3-3 have been modeled with adequate detail, emulating

Table 3.5: Grid parameters

| Parameter | Symbol | Value | |
|------------------------|------------|-------|------------------|
| Branch resistance | R_{LINE} | 1 | Ω |
| Branch inductance | L_{LINE} | 150 | μH |
| Branch length | l_b | 260 | m |
| Nominal grid voltage | V_{PCC} | 230 | V_{rms} |
| Nominal grid frequency | f_0 | 50 | Hz |

fixed point arithmetic where applicable, control delays (due to ADC operation and PWM update), and finite PWM resolution. The results are shown on Fig. 3-8(a). As can be seen, the basic functionality of the controller has been assessed. However, this type of system level simulation simply allows to verify the stability of regulators, the quality of steady state operation and to estimate the achievable speed of response. None of the practical issues related to the implementation of the controller can be effectively addressed at this level. Indeed, encountering an unexpected dynamic behavior, or even instabilities, once the simulation model is turned into a physical controller is a common experience.

3.3.2 Hardware-In-the-Loop Real-Time Simulation

To validate control and plant models, improve the quality of the simulation (by reducing its execution time), and safely test the physical control hardware to be later deployed on the DER-interfacing EPP, HIL real-time simulation is employed. This term indicates the direct connection between a high performance computer, where a model of the controlled plant is simulated, and the inverter control board, where all the algorithms described above run. Thanks to a multichannel digital to analog converter (DAC) module, the computer is capable of generating high speed analog outputs, which are sampled by the controller as if they were coming from the physical system. Therefore, controller operation is strictly real-time, with no time dilation whatsoever. A graphical view of the HIL simulation organization is given in Fig. 3-6.

There are several practical issues to solve before HIL simulations can be run, as also pointed out in [178] and discussed in [179]. First, computationally efficient, numerical

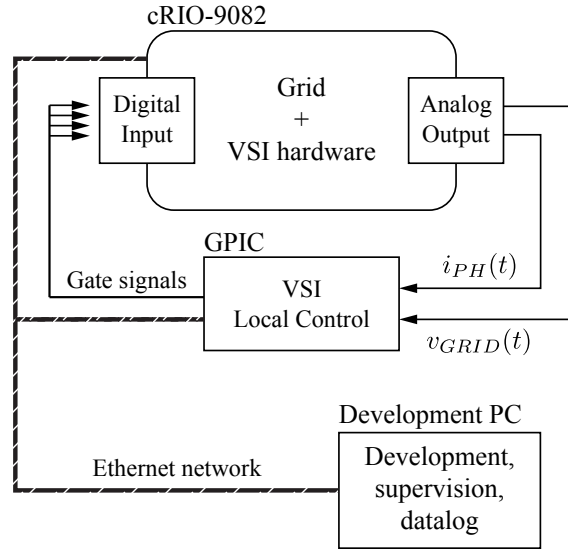


Figure 3-6: Connection between the high performance computer (cRIO) and the control hardware (GPIC).

model of the controlled system has to be set-up. To this purpose, a set of network building blocks have been developed, where the discrete time equivalent of the algebraic and differential equations for the fundamental electrical elements (e.g., resistor, capacitor, inductor) have been formulated to be efficiently solved in an FPGA. As an example, the implemented equation for a reactive element looks like:

$$x(k + 1) = x(k) + \alpha u(k) \quad (3.1)$$

where x represents the state variable, α represents the inverse of the value of the electrical parameter (e.g., inductance L) multiplied by the integration step (e.g., $\frac{\Delta T}{L}$), and u is the electrical dual of the considered state variable. The electrical topology of the system has been set-up manually, applying Kirchhoff voltage and current laws. Finally, the full-bridge converter switches have been modeled at the purely logic level, idealizing their physical characteristics.

As a result, after compiling the code, the model of the plant runs on the FPGA chip available within the adopted processor [177] and the set of differential equations that describes the system of Fig. 3-2 is numerically solved by a customized digital hardware. As implied by (3.1), the integration method is the simple first order Euler, with integration step

equal to $T_{sim} = 100$ ns. Fixed point arithmetic is also mandatory to preserve computational efficiency, but, due to a 32 bit internal representation of variables, no rounding or truncation effects have been detected.

The second issue to be solved is the generation of the analog signals feeding the controller inputs. In the experiment a relatively slow DAC, featuring a sampling rate of 100 kSample/s, has been used so as to occupy a single output module and avoid possible synchronization issues. This choice turned out to pose some limitation on the achievable simulation quality. Indeed, the DAC update delay, together with input and output quantization noises, affects the simulation stability, introducing an undesired numerical noise, which is clearly visible on the waveforms presented in Fig. 3-8(b). Better results can be achieved by adopting the provisions described in Sec. 3.4.

However, it is worth remarking that the purpose of RT simulations is to provide a significant test for the controlling hardware. If the simulation artifacts do not impair controller operation, they may be neglected; indeed, they will not be found in the experimental tests [see Fig. 3-8(c)]. From this standpoint, HIL simulation allows to verify the complete functionality of the controller in the considered application, practically confirming the results of conventional numerical simulations.

3.3.3 Experimental Tests

The final step of the controller development is represented by experimental tests. To this aim, the controller is connected to a 3 kVA VSI (see Table 3.4). The resulting experimental set-up is shown in Fig. 3-7. As can be seen, the digital controller is bridging the lower level inverter control functions and the higher level ones, required by the grid and hosted by a remote PC, which is connected via an Ethernet cable. The test results are shown in Fig. 3-8(c). Clearly, the power control loops behave exactly as expected. This result demonstrates several achievements of the proposed control development methodology. In the first place, it is possible to notice that local control is performed exactly as in a conventional DSP, or FPGA, based organization. But here, the RT GPP on board the controller and the remote PC supervising the grid are connected by Ethernet and exchange data without interfering

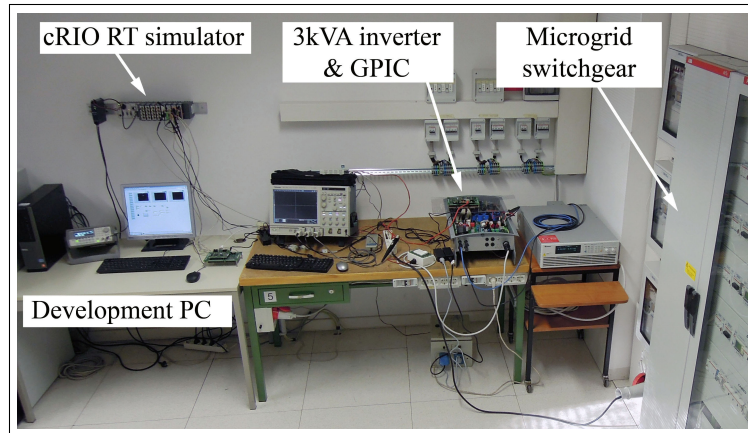
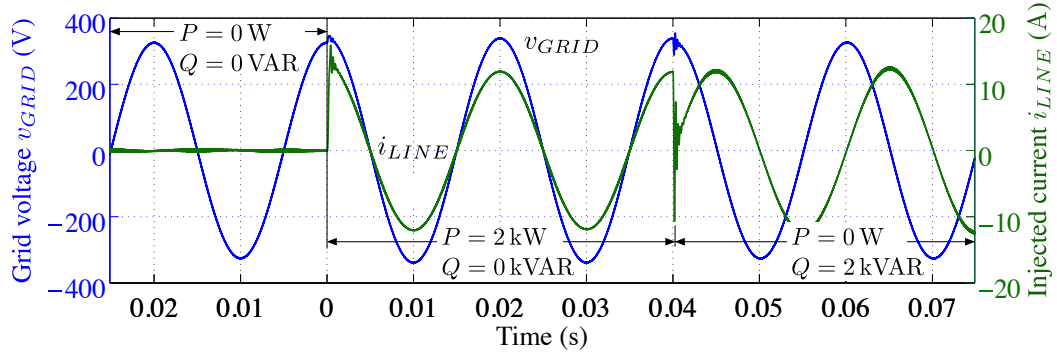


Figure 3-7: View of the experimental testbed for DER-interfacing EPPs, comprising the platform for HIL simulations, RCP, and the final experimental set-up. In particular: cRIO RT simulator is employed as HIL platform running the model of the controlled plant; GPIC is the controller supporting the RCP of the EPP's controller; the microgrid switchboard allows to interface the EPP to a grid emulator, low-voltage interconnection lines, and energy resources (PV sources, batteries, fuel-cells); the development PC runs the IDE and allows to configure and supervise experiments.

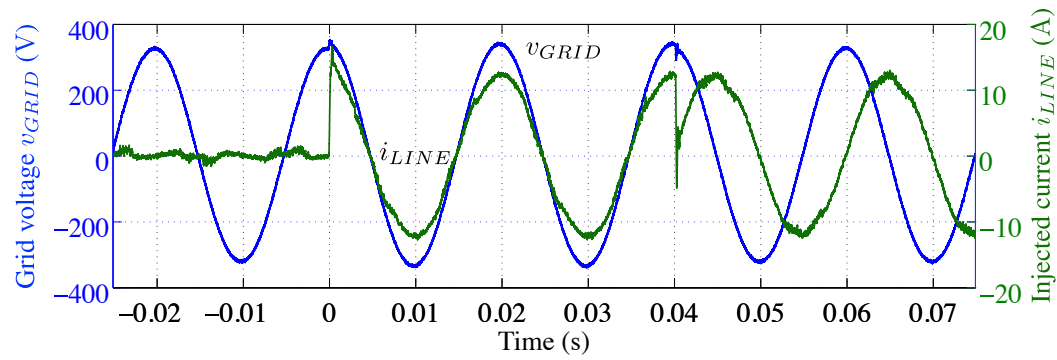
with the low level control activities. Thanks to the RTOS, there is no practical limit to the information that can be transferred between the two systems, a fundamental requirement to safely operate a microgrid experiment (and possibly a real one). Finally, the proposed HIL simulation methodology offers a reliable method to verify the functionality of the controller before serious electrical power comes into play.

3.3.4 Extension to More Complex Scenarios

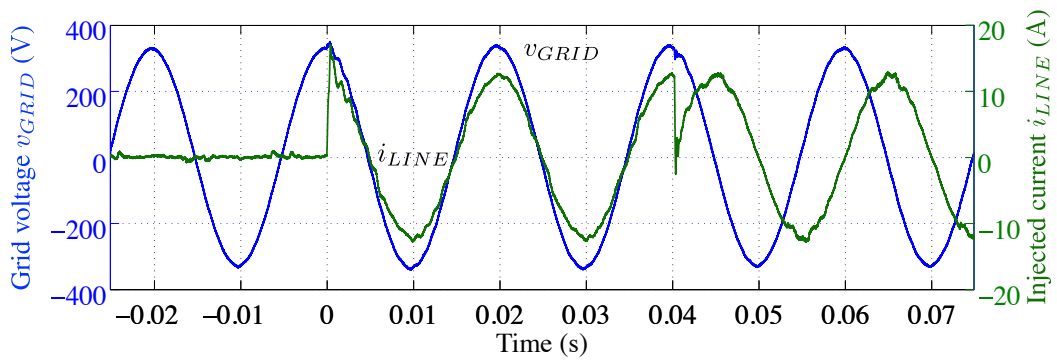
The considered control and HIL simulation platform can scale with the complexity of the target case study thanks to its modularity. Depending on the final application, a variable number of digital I/O lines (employed, for example, to generate or acquire PWM signals) and a variable number of analog input or output channels (employed, for example, to represent controlled analog quantities) can be available. The number of I/O digital or analog channels can range from tens to hundreds. For what concerns real-time simulations, the computational burden in running plant or control technique models can be distributed among various processor cores and FPGA modules operating in parallel and managed through the same LabVIEW high-level graphical programming language and development environment.



(a) Simulink simulation



(b) Real-time simulation



(c) Prototype measurements

Figure 3-8: Results of control stack test activity: a step reference change is applied successively for the active power and the reactive power: (a) simulation in Matlab Simulink, (b) hardware in the loop real-time simulation, and (c) experimental test measurements.

The described development methodology and toolset have been adopted to more complex cases, for example, to validate the algorithms proposed in [180] and in [181]. In [180] the described approach is applied to implement a control strategy for microgrids with a centralized controller. The control algorithm—whose principle of operation is described in Sec. 4.2.2 whereas it is now referred just as an application case—is devised so that the centralized controller commits distributed EPPs to generate the power requested by loads in a way that is inversely proportional to loads-to-EPPs distances. Moreover, to the purpose of taking into account inverters' power limits, the so called β coefficients [180] are defined to convey the information on the saturation level of inverters; in particular, $\beta_{EPP_x} = 1$ if the power demand to EPP_x is below its maximum power limit p_x^{\max} . With the aim to test such control algorithm, the code of the centralized controller has been developed and deployed on a cRIO platform, and the behavior of beta coefficients has been recorded while varying the maximum active power of two EPPs, namely p_1^{\max} and p_2^{\max} , from 0 to 3 kW. The obtained results have been logged and checked off-line; Fig. 3-9 displays a sample of the results. The figure refers to the case in which a load of 23.5Ω is connected between the two EPPs, at a distance of 400 m from EPP_1 and 700 m from EPP_2 . Thus, neglecting the voltage drop across interconnecting cables, in this situation the total power absorption is equal to 2.25 kW and the ideal power sharing among EPP_1 and EPP_2 is 1.4 kW and 0.8 kW, respectively. Indeed, Fig. 3-9 shows that EPP_1 exits saturation when its maximum injectable power p_1^{\max} is nearly equal to the total load power, and EPP_2 exits saturation when p_2^{\max} is approximately 0.8 kW. These results are in agreement with theoretical expectations, discussed in [180].

3.4 Accuracy Improvements by Model Partitioning

As mentioned in Sec. 3.3.2, even if state-of-the-art hardware is adopted, obtaining accurate simulation results requires some typical problems to be tackled. The first one is represented by the accurate generation of the analog output signals feeding the control board. In principle, these need to be as close as possible to the ones that would be generated by the physical plant, and, as such, characterized by negligible quantization noise and other arti-

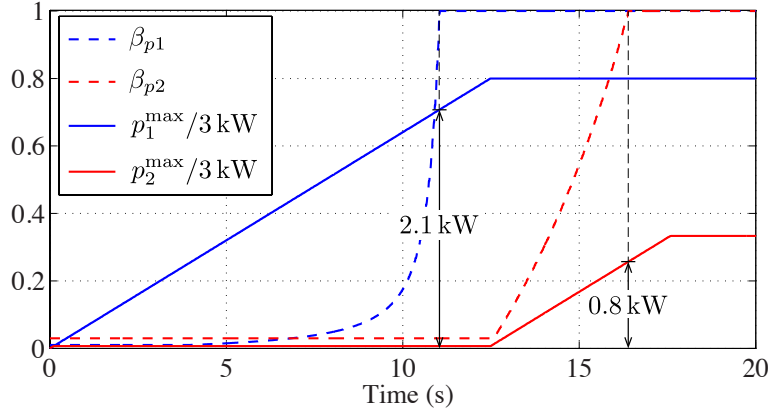


Figure 3-9: Test results from the application of the rapid prototyping approach to the microgrid supervisor described in [180].

facts. In the first experiment discussed in Sec. 3.3.2, the DAC update frequency is limited to 100 kHz. This resulted in a measurable update delay, clearly not taken into account in the controller design. An estimation of worst case phase margin reduction determined by such DAC delay is given by (3.2):

$$\Delta\phi = -\pi \frac{f_{CR}}{f_{DAC}} \frac{180}{\pi} = 180 \frac{f_{CR}}{f_{DAC}}, \quad (3.2)$$

where f_{CR} is the current controller crossover frequency and f_{DAC} is the DAC update frequency. Equation (3.2) assumes the plant model to be continuous time (it is actually discrete time with 10 MHz sampling frequency) and expresses the phase rotation at the desired crossover frequency according to a simple zero-order hold (ZOH) approximation of the DAC. In our case, this turns out to be equal to -3.6° . The phase rotation can be better calculated numerically, exploiting (3.3), representing the complete transfer function of the plant:

$$T_{i0}(s) = \frac{V_{DC} \cdot \frac{k_{sense,i}}{A_r} \cdot e^{-s \Delta t_{ctrl}}}{s L_{PH} + \frac{1}{s C_{PH}} // (s L_{GRID} + R_{GRID})}, \quad (3.3)$$

where Δt_{ctrl} is the sum of the AD conversion time (Δt_{AD}), the PI regulator calculation time (Δt_{calc}), given in Table 3.4, and the PWM modulation delay (Δt_{PWM}). Because the proposed implementation adopts a double update PWM [103], the modulator delay can be estimated to be equal to one half of the switching period (i.e., $\frac{1}{2f_s}$). Fig. 3-10 shows the Bode plots of two discrete time versions of (3.3), both with and without the DAC delay,

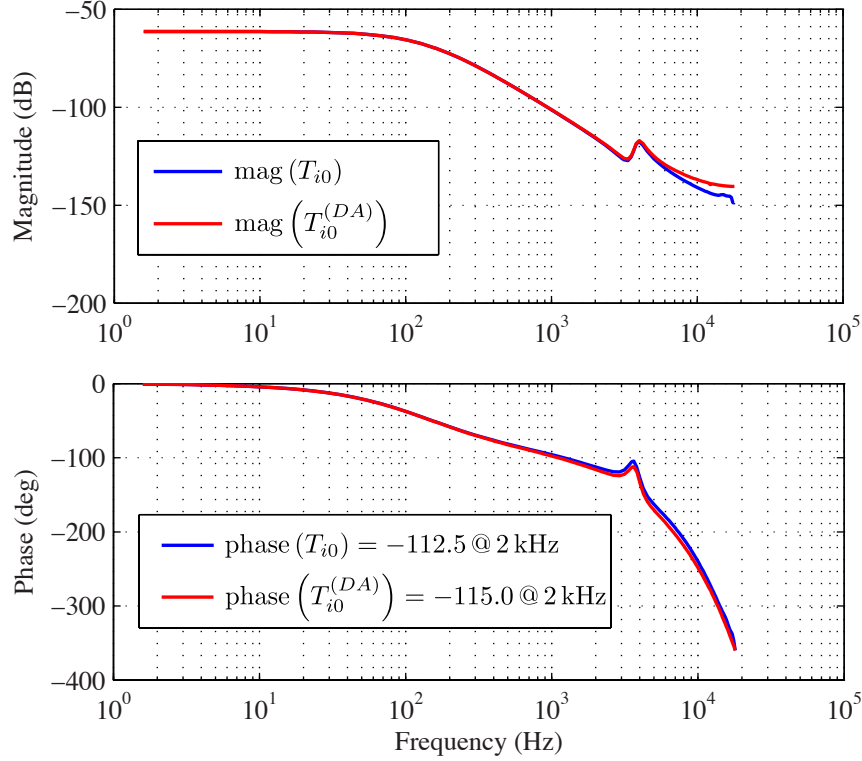


Figure 3-10: Bode plots of the open loop transfer functions T_{i0} and $T_{i0}^{(DA)}$.

giving in the former case a -2.5° additional phase rotation. The limited DAC resolution has a much heavier impact on the current controller since, in the worst case, only 2 to 3 samples are generated during the current ripple run-up (and run-down) phase, which determines a relative error on the average current measurement, $\frac{\Delta I_{ph_{avg}}}{I_{ph_{pk}}}$, given by:

$$\frac{1}{3} \frac{\Delta I_{ph_{pk2pk}}}{I_{ph_{pk}}} \leq \frac{\Delta I_{ph_{avg}}}{I_{ph_{pk}}} \leq \frac{1}{2} \frac{\Delta I_{ph_{pk2pk}}}{I_{ph_{pk}}}, \quad (3.4)$$

where $\frac{\Delta I_{ph_{pk2pk}}}{I_{ph_{pk}}}$ represents the relative peak to peak inductor current ripple, which, in our inverter, occupies, at its maximum, about 16% of the ADC full scale range. As a result, the worst case relative error on the average current turns out to be between about 6% and 8%, a non-negligible disturbance at the modulation frequency. Both problems can be solved using faster DACs. Indeed, by simulations it is possible to notice that if the ratio $\frac{f_{CR}}{f_{DAC}}$ is below 0.05 then negligible distortion can be obtained. As a first attempt to alleviate the problem, the use of a dedicated output module has been considered for the generation of the inductor current signal, allowing to achieve an update rate of 360 kSample/s, thus providing enough

points per commutation period to make both the quantization noise and the update delay less relevant.

On the model input side, care must be taken as well. Indeed, the organization of Fig. 3-6 implies a reduction in the actual PWM resolution, as if a lower number of bits were used to represent the duty-cycle. Indeed, although the simulation time step, $T_{sim} = 100$ ns, is adequate to accurately compute the dynamics of the system's state variables, it is significantly longer than the minimum voltage pulse duration at the PWM adopted resolution. The number of lost bits can be expressed as:

$$n_{b_{lost}} = \log_2 (f_{clk} \cdot T_{sim}) = \log_2 (f_s \cdot (2A_r + 1) \cdot T_{sim}) , \quad (3.5)$$

where f_{clk} represents the digital PWM counter clock. Its explicit relation with switching frequency and carrier amplitude is given in the right hand side of the equation. The lost bits are partially recovered in the simulation, thanks to the dithering effect caused by the *asynchronous* operation of the controller and the simulation platform. Decreasing the simulation time step of the model, reaching the condition $T_{sim} \cdot f_{clk} \leq 1$, it would be possible to read the input gate signals with their full time resolution. However, from the implementation point of view, it is not practical to decrease the simulation time step of the *whole* model to this extent, because this would limit the amount of computable equations and, therefore, the size of the model. A more effective method to tackle the problem is by partitioning the model, identifying those sections that really need to be simulated at shorter time steps. This approach allows to manage both complexity and time constraints.

Specifically, in the considered case study, the phase inductor L_{PH} is the only component that is exposed to high speed signals, notably, the bridge voltage v_{INV} . Therefore, only its discrete model actually requires to be computed at a high rate. If this is done properly, it is possible to achieve better accuracy, while keeping the execution rate of the remaining part of the model at lower values. The remaining parts of the model experience signals that are dominated by controller dynamics (limited to a few kHz) and, as a result, can be simulated at a slower pace.

To highlight the benefit of partitioning, Fig. 3-11 displays the difference between two

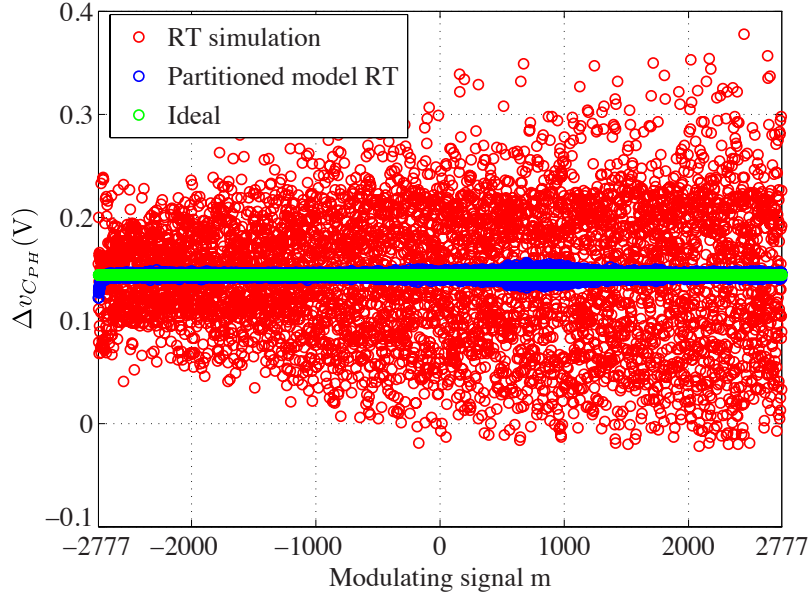
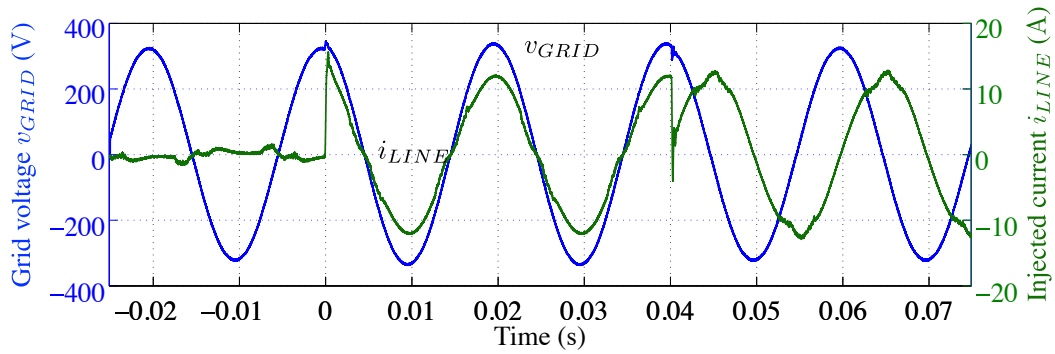


Figure 3-11: Differential increase between two successive samples of a filtered version of the inverter output voltage v_{GRID} .

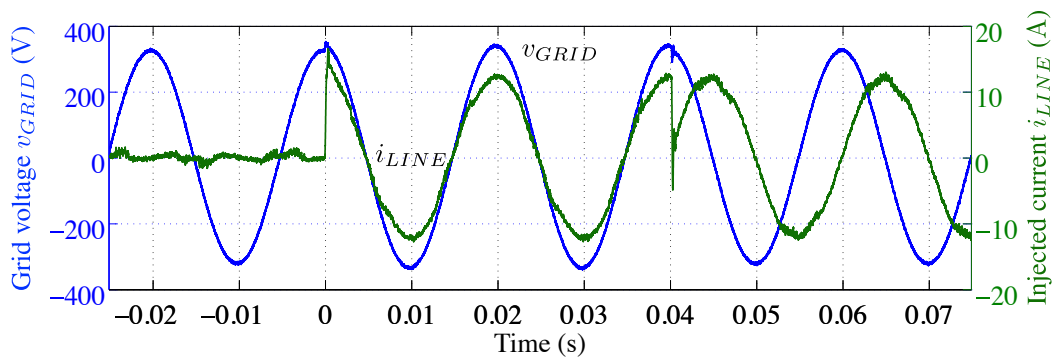
successive samples of a low pass filtered version (with 100 Hz cut-off frequency) of the inverter bridge instantaneous output voltage v_B , for a gradual increase of the modulating signal from $-A_r$ to $+A_r$. It shows that, thanks to the smaller simulation step of the most critical part of the plant model, it is possible to acquire the signal generated by the modulator almost at its full resolution, that is, equal to $V_{BUS}/A_r \simeq 144$ mV.

Fig. 3-13 represents the implementation of the described concept for the considered simple case. The program is loaded on the FPGA unit of the cRIO-9082 (see Table 3.3); the corresponding FPGA resource utilization is: Total Slices 8.1%, Slice Registers 2.3%, Slice LTU 4.8%, DSP48 16.1%, Block RAM 0%. In Fig. 3-12(a), the measured results from the corresponding partitioned model HIL RT simulation are shown.

In particular, the comparison proposed in Fig. 3-12, which refers to the measures from the HIL RT simulation in Fig. 3-12(b), and the partitioned model HIL RT simulation in Fig. 3-12(a), highlights the reduction in simulation artifacts.



(a) Partitioned model real-time simulation



(b) Real-time simulation

Figure 3-12: Reduction in the simulation artifacts by model partitioning. (a) Partitioned model HIL RT simulation; (b) HIL RT simulation.

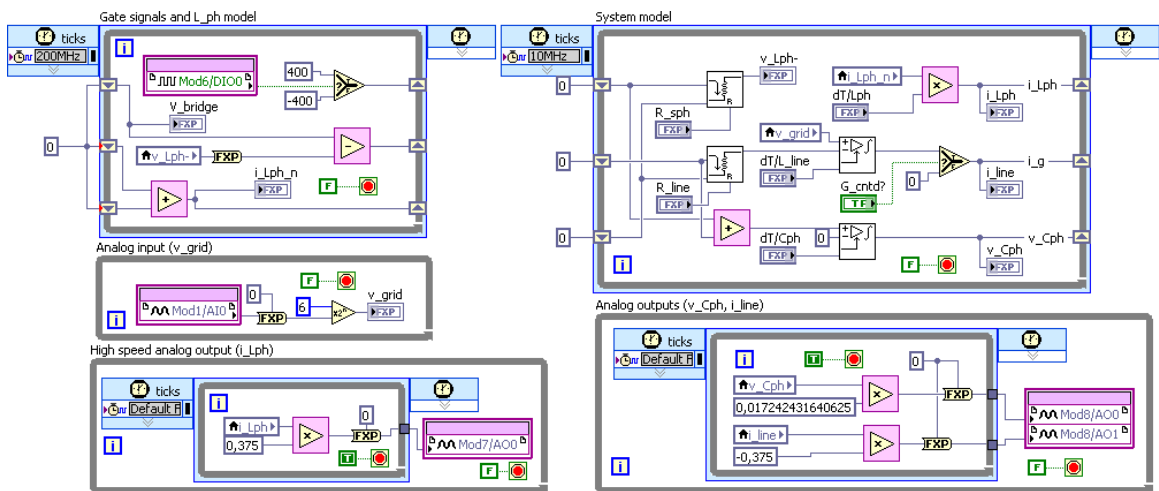


Figure 3-13: LabVIEW program of the controlled plant model (partitioned model)—Controlled model computation time step: $T_{sim} = 100$ ns.

3.5 Summary

The chapter describes the methodology and the set of hardware and software tools that have been adopted to develop and experimentally validate all the solutions described in this dissertation. The applied methodology makes use of rapid-control-prototyping (RCP) and hardware-in-the-loop (HIL) technologies, besides, organizes the development phases in three fundamental steps. The first step is to employ conventional computer simulations to verify the design of controllers; the second step is to develop the designed controllers by using rapid-control-prototyping platforms and to test the implementation by applying hardware-in-the-loop simulations, which allows not only to validate the controllers in their final form, but also to interface models or control techniques to realistic inputs or, even, inputs from the field; the last step is to tune the behavior of the developed controllers while operating in the final application. The platforms that have been chosen and studied to perform RCP and HIL tests are described. The concepts are explained considering the development of a digital controller for the inverter section of a DER-coupling EPP. The utility interface converter described in Ch. 5, the current controllers described in Ch. 6, the master/slave architecture with the power-based control described in Ch. 7 and finally verified experimentally in Ch. 8 have been developed by applying the concepts described in this chapter. The main advantages brought by the introduced method and hardware/software toolset are *i)* to fully validate controllers before being connected to the real plant, *ii)* to have an almost direct transition between the development phase and the final deployment, and *iii)* to ease the management of complex set-ups by exploiting the flexibility given by the general purpose integrated-development-environment and the rapid-control-prototyping platforms.

Chapter 4

Theoretical and Technical Background

This chapter outlines the theoretical background of the control techniques presented herein. The problem of exploiting distributed energy resources in order to bring benefit to the distribution grid is addressed with the first aim of reducing the distribution loss. The distribution loss is a relevant figure to look at because it is directly linked to various performance indices, such as, distribution efficiency, hosting capacity, uniformity of voltage profiles.

The following Sec. 4.1 formalizes the problem of distribution loss minimization and describes how this problem can be tackled from three different points of view. Three corresponding control solutions are introduced in Sec. 4.2. The control algorithm presented in Ch. 7, based on the results of this preliminary study, represents the progression of the investigation presented in [43, 44, 182], on the effective control of distributed energy resources in low-voltage networks.

The theoretical discussion reported in Sec. 4.3 supports the master/slave architecture presented in Ch. 5. This latter section defines a *paradigm*, for the control of distributed energy resources, that makes use of conservative power terms to selectively compensate power components flowing through the point of common coupling of a distribution network. By exploiting accordingly the conservativeness of power terms, control approaches can significantly reduce synchronization and information processing requirements, as shown in the following chapters.

4.1 Distribution Loss Minimization

Let's consider a microgrid fed by the mains at the point of common coupling (PCC) and let 0 indicate that node. From a mathematical point of view, the distribution network can be modeled as a directed weighted graph $\mathcal{G} = (\mathcal{V}, \mathcal{E}, \sigma, \tau)$ where \mathcal{V} is the set of nodes (i.e., the *buses* of the electric grid), \mathcal{E} is the set of edges representing the power lines (i.e., the branches of the electric grid), and $\sigma, \tau : \mathcal{E} \rightarrow \mathcal{V}$ are two functions such that edge e goes from the source node $\sigma(e)$ to the terminal node $\tau(e)$. The incidence matrix $\mathbf{A}_{\mathcal{G}}$ of graph \mathcal{G} is defined as:

$$[\mathbf{A}_{\mathcal{G}}]_{ev} = \begin{cases} -1 & \text{if } v = \sigma(e) \\ 1 & \text{if } v = \tau(e) \\ 0 & \text{otherwise} \end{cases} . \quad (4.1)$$

To each edge $e \in \mathcal{E}$ is associated a weight that corresponds to the value of the impedance Z_e of the electric line represented by e ; specifically $Z_e = R_e + jX_e$, where R_e and X_e are, respectively, the resistive and the inductive component of the electric line. Nodes in \mathcal{V} are passive, if they link-up loads, or active, if they link-up DGs.

Assuming a *tree-shaped* grid and excluding node 0, the number N of grid nodes coincides with the number of distribution paths (grid branches) and its associated incidence matrix \mathbf{A} , obtained from $\mathbf{A}_{\mathcal{G}}$ by eliminating the column corresponding to node 0, is squared and invertible. Assuming also, for simplicity, that the grid voltages and currents are purely sinusoidal, they can be represented by phasors.¹

Let $\underline{\xi}$ be the vector of branch currents phasors and \underline{i} be the vector of absorbed node currents phasors (loads and DGs), the Kirchhoff's equations at the grid nodes can be expressed in the form:

$$\underline{i} = \mathbf{A}^T \underline{\xi} . \quad (4.2)$$

By inversion of \mathbf{A}^T we obtain:

$$\underline{\xi} = (\mathbf{A}^T)^{-1} \underline{i} . \quad (4.3)$$

¹Given the generic sinusoidal quantities: x_1, \dots, x_i, \dots in the time domain; hereinafter a phasor is indicated as \underline{x}_i , a vector [e.g., $(x_1, \dots, x_i)^T$] is indicated as \mathbf{x} . Accordingly, $\underline{\mathbf{x}}$ indicate a vector of phasors.

The distribution losses are generally expressed by:

$$p_{loss} = \underline{\boldsymbol{\xi}}^* \mathbf{R} \underline{\boldsymbol{\xi}}, \quad (4.4)$$

where symbol $*$ means conjugate transpose and \mathbf{R} is the real part of branch impedance matrix $\mathbf{Z} = \text{diag}(Z_1, Z_2, \dots, Z_N)$. Owing to (4.3) the losses can also be expressed as a function of the load currents by:

$$p_{loss} = \underline{\boldsymbol{i}}^* \mathbf{B} \underline{\boldsymbol{i}}, \quad (4.5)$$

where $\mathbf{B} = \mathbf{A}^{-1} \mathbf{R} (\mathbf{A}^{-1})^T$. Note that, by definition, matrix \mathbf{B} is symmetrical and function p_{loss} is real.

The computation is more complex in case of meshed grids, where the incidence matrix is not invertible. Even in this case, however, equation (4.5) holds and the optimum control approach described hereafter remains valid [183].

In the following subsections, the problem of distribution loss minimization is analyzed from three different perspectives. Firstly it is analyzed by considering the set of grid current injections corresponding to the minimum distribution loss; then, looking at a particular source, the locally optimum current injections are derived by means of the currents absorbed by nearby loads; the same local approach is finally adopted to find the voltage that a particular source should impose to locally minimize the distribution loss. The reported analysis set the basis to devise the control approaches described in Sec. 4.2.

4.1.1 Optimum Node Currents

Let $\underline{\boldsymbol{i}}_a$ be the currents fed by the DGs into *active nodes* and $\underline{\boldsymbol{i}}_p$ be the currents injected by the loads at *passive nodes*. Equation (4.5) can be partitioned in the form:

$$p_{loss} = \begin{bmatrix} \underline{\boldsymbol{i}}_a^* & \underline{\boldsymbol{i}}_p^* \end{bmatrix} \begin{bmatrix} \mathbf{B}_{a,a} & \mathbf{B}_{a,p} \\ \mathbf{B}_{p,a} & \mathbf{B}_{p,p} \end{bmatrix} \begin{bmatrix} \underline{\boldsymbol{i}}_a \\ \underline{\boldsymbol{i}}_p \end{bmatrix} = \underline{\boldsymbol{i}}_a^* \mathbf{B}_{a,a} \underline{\boldsymbol{i}}_a + 2\Re(\underline{\boldsymbol{i}}_a^* \mathbf{B}_{a,p} \underline{\boldsymbol{i}}_p) + \underline{\boldsymbol{i}}_p^* \mathbf{B}_{p,p} \underline{\boldsymbol{i}}_p. \quad (4.6)$$

Optimum DG currents result by computing the minimum of the multivariable function p_{loss} , which gives:

$$\underline{i}_a^{\text{opt}} = -\mathbf{B}_{a,a}^{-1} \mathbf{B}_{a,p} \underline{i}_p. \quad (4.7)$$

Equation (4.7) sets the theoretical basis for optimum control of DGs, because it gives the optimum DG currents as a function of grid parameters and load demand. The approach can be extended to entail also the boundaries set by the DG current limits and by the islanded operation, which requires zeroing of the current at node 0. Note finally that (4.7) is separately valid for the real and imaginary part of the currents, thus allowing the independent control of active and reactive power.

The described approach aims at minimizing distribution losses by considering *globally* the network. A *local* minimization, less demanding in terms of knowledge on network parameters, can be pursued as well; from this standpoint, the control principles proposed in [44, 184, 185] and outlined in the next two subsections have been devised.

4.1.2 Minimization of Local Distribution Losses

Fig. 4-1 shows a simplified single-phase representation of a homogeneous distribution path (i.e., constant impedances per unit of length) connecting two neighbor active nodes A and B and feeding loads connected to K nodes. Assuming that node voltages and currents are sinusoidal, let's refer to node voltage phasors \underline{v}_A and \underline{v}_B . Similarly, $\underline{\xi}_{AB}$ and $\underline{\xi}_{BA}$ represent the phasors of the currents fed by nodes A and B into path $A-B$.

Let \underline{i}_{L_k} , $k \in \{0, \dots, K\}$, be the current absorbed by the k -th load connected along path $A-B$ (here $i_{L_0} = 0$), Δ_k the distance between loads k and $k + 1$, and $\underline{\xi}_k$ the line current flowing in branch Δ_k . By defining:

$$\underline{\xi}_k = \underline{\xi}_{AB} - \sum_{\ell=0}^k \underline{i}_{L_\ell}, \quad (4.8)$$

the power loss in path $A-B$ can be written as:

$$p_{loss} = \sum_{k=0}^K r \Delta_k |\underline{\xi}_k|^2 = r \sum_{k=0}^K \Delta_k (\underline{\xi}_{AB} - \underline{i}_{\Sigma k}) (\underline{\xi}_{AB} - \underline{i}_{\Sigma k})^*, \quad (4.9)$$

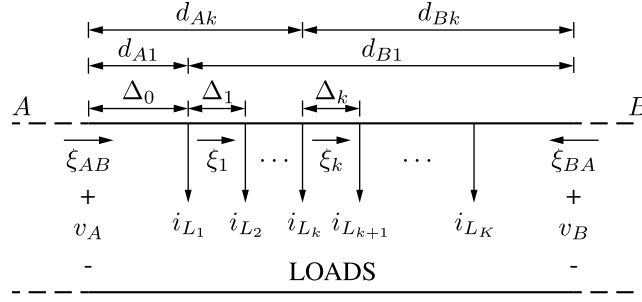


Figure 4-1: Representation of distribution line between two active nodes A and B .

where r is the resistance per unit of length of the distribution line and $i_{\Sigma k}$ represents the summation in (4.8). By differentiating (4.9) with respect to the real and imaginary part of the injected current $\underline{\xi}_{AB} = \xi_{AB}^R + j\xi_{AB}^I$ and setting the derivative to zero it is possible to obtain the optimum value of injected current ξ_{AB}^{opt} to minimize the power dissipated along the distribution lines:

$$\begin{cases} \frac{\partial p_{\text{loss}}}{\partial \xi_{AB}^R} = 2r \sum_{k=0}^K \Delta_k (\xi_{AB}^R - i_{\Sigma k}^R) = 0 \Rightarrow \xi_{AB}^R \sum_{k=0}^K \Delta_k = \sum_{k=0}^K \Delta_k i_{\Sigma k}^R \\ \frac{\partial p_{\text{loss}}}{\partial \xi_{AB}^I} = 2r \sum_{k=0}^K \Delta_k (\xi_{AB}^I - i_{\Sigma k}^I) = 0 \Rightarrow \xi_{AB}^I \sum_{k=0}^K \Delta_k = \sum_{k=0}^K \Delta_k i_{\Sigma k}^I \end{cases} ; \quad (4.10)$$

therefore, the value of ξ_{AB} that brings to the minimum distribution loss is:

$$\xi_{AB}^{\text{opt}} = \frac{1}{d_{AB}} \sum_{k=0}^K \Delta_k i_{\Sigma k} = \frac{1}{d_{AB}} \sum_{k=0}^K i_{Lk} d_{Bk}, \quad (4.11)$$

where d_{AB} is the path length, and d_{Ak} and d_{Bk} are the distances between load k and node A and B , respectively. (The the last equivalence of (4.11) can be derived by inspection.)

Correspondingly, since $\xi_{AB} + \xi_{BA} = \sum_{k=0}^K i_{Lk}$, currents ξ_{AB} and ξ_{BA} take the following optimum values:

$$\begin{cases} \xi_{AB}^{\text{opt}} = \frac{1}{d_{AB}} \sum_{k=0}^K i_{Lk} d_{Bk} \\ \xi_{BA}^{\text{opt}} = \frac{1}{d_{AB}} \sum_{k=0}^K i_{Lk} d_{Ak} \end{cases} . \quad (4.12)$$

Equation (4.12) shows that the optimum currents demanded to the active nodes *depend only on the load distribution* along path A - B .

If optimum currents (4.12) are applied, then $v_A = v_B$. Indeed, if $v_A \neq v_B$, a circulation

current appears and the currents fed by nodes A and B become:

$$\begin{cases} \underline{\xi}_{AB} = \underline{\xi}_{AB}^{\text{opt}} + \frac{v_A - v_B}{z d_{AB}} = \underline{\xi}_{AB}^{\text{opt}} + \underline{\xi}_{AB}^{\text{circ}} \\ \underline{\xi}_{BA} = \underline{\xi}_{BA}^{\text{opt}} + \frac{v_B - v_A}{z d_{AB}} = \underline{\xi}_{BA}^{\text{opt}} + \underline{\xi}_{BA}^{\text{circ}} \end{cases} \quad (4.13)$$

Equation (4.9) can be rewritten to highlight the effect of circulating current $\underline{\xi}^{\text{circ}}$ on power loss p_{loss} , namely:

$$\begin{aligned} p_{\text{loss}} &= r \sum_{k=1}^K \Delta_k (\underline{\xi}_{AB} - i_{\Sigma k}) (\underline{\xi}_{AB} - i_{\Sigma k})^* = \\ &= r \sum \Delta_k (\underline{\xi}_{AB} \underline{\xi}_{AB}^* - 2\Re(\underline{\xi}_{AB}^* i_{\Sigma k}) + i_{\Sigma k} i_{\Sigma k}^*) = \\ &= r d_{AB} \underline{\xi}_{AB} \underline{\xi}_{AB}^* - 2r \Re\left(\underline{\xi}_{AB}^* \sum_{k=0}^K \Delta_k i_{\Sigma k}\right) + r \sum_{k=0}^K \Delta_k |i_{\Sigma k}|^2 = \\ &= r d_{AB} \underline{\xi}_{AB} \underline{\xi}_{AB}^* - 2r d_{AB} \Re(\underline{\xi}_{AB}^* \underline{\xi}_{AB}^{\text{opt}}) + r \sum_{k=0}^K \Delta_k |i_{\Sigma k}|^2, \end{aligned} \quad (4.14)$$

by substituting $\underline{\xi}_{AB} = \underline{\xi}_{AB}^{\text{opt}} + \underline{\xi}_{AB}^{\text{circ}}$ the following expression can be obtained:

$$\begin{aligned} p_{\text{loss}} &= r d_{AB} (\underline{\xi}_{AB}^{\text{opt}} + \underline{\xi}_{AB}^{\text{circ}}) (\underline{\xi}_{AB}^{\text{opt}} + \underline{\xi}_{AB}^{\text{circ}})^* + \\ &\quad - 2r d_{AB} \Re((\underline{\xi}_{AB}^{\text{opt}} + \underline{\xi}_{AB}^{\text{circ}})^* \underline{\xi}_{AB}^{\text{opt}}) + r \sum_{k=0}^K \Delta_k |i_{\Sigma k}|^2 = \\ &= r \left(\sum_{k=0}^K \Delta_k |i_{\Sigma k}|^2 - d_{AB} |\underline{\xi}_{AB}^{\text{opt}}|^2 + d_{AB} |\underline{\xi}_{AB}^{\text{circ}}|^2 \right) = p_{\text{loss}}^{\text{opt}} + r d_{AB} |\underline{\xi}_{AB}^{\text{circ}}|^2, \end{aligned} \quad (4.15)$$

where $p_{\text{loss}}^{\text{opt}}$ represents the minimum value of the total power dissipation in feeding loads i_{Lk} , $k = 1, \dots, K$. From (4.15), the power loss in path A - B may also be expressed in the simple form:

$$p_{\text{loss}} = p_{\text{loss}}^{\text{opt}} + R_{AB} \left| \frac{v_A - v_B}{Z_{AB}} \right|^2, \quad (4.16)$$

where $Z_{AB} = R_{AB} + jX_{AB}$ is the line impedance of path A - B .

The first addendum of (4.16) corresponds to the minimum distribution losses, which occurs in the optimum condition (4.12) and depends only on the load currents and their distribution along path A - B . The second addendum pertains to the circulation currents and

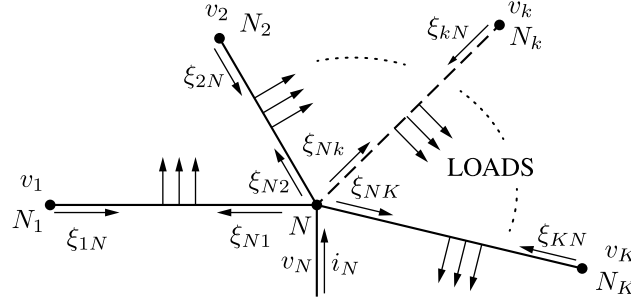


Figure 4-2: Representation of a grid section converging in an active node (N).

depends on the voltage difference between nodes A and B . Equation (4.16) indicates that the minimum distribution losses occur when $\underline{v}_A = \underline{v}_B$ and the circulation current vanishes.

4.1.3 Locally Optimal Node Voltages

Consider now a radial section of a microgrid, sketched in Fig. 4-2, where active node N links to surrounding active nodes N_1, \dots, N_K through distribution paths L_1, \dots, L_K .

Let \underline{v}_N be the voltage phasor of node N , \underline{v}_k ($k = 1, \dots, K$) those of surrounding nodes, and \underline{i}_N the current injected at node N by a local DG. Current \underline{i}_N is equal to the sum of all terms corresponding to paths L_1, \dots, L_K and, on the light of (4.13), it can be written as:

$$\underline{i}_N = \sum_{k=1}^K \xi_{\underline{v}_{Nk}} = \underbrace{\sum_{k=1}^K \xi_{\underline{v}_{Nk}}^{\text{opt}}}_{\underline{i}_N^{\text{opt}}} + \underbrace{\sum_{k=1}^K \frac{\underline{v}_N - \underline{v}_k}{Z_k}}_{\underline{i}_N^{\text{circ}}} = \underline{i}_N^{\text{opt}} + \underline{i}_N^{\text{circ}}, \quad (4.17)$$

where $Z_k = R_k + jX_k$ are the path impedances. Optimum current $\underline{i}_N^{\text{opt}}$ depends on the loads distribution along paths L_1, \dots, L_K , according to (4.12), while total circulation current $\underline{i}_N^{\text{circ}}$ depends on the voltage differences between node N and the surrounding nodes. By extending (4.16), the total distribution loss in paths L_1, \dots, L_K can be derived in the form:

$$p_{\text{loss}}^{\text{tot}} = \sum_{k=1}^K p_{k,\text{loss}}^{\text{opt}} + \sum_{k=1}^K R_k \frac{|\underline{v}_N - \underline{v}_k|^2}{Z_k^2}. \quad (4.18)$$

This local distribution loss is minimized if voltage \underline{v}_N takes the value:

$$\underline{v}_N^{\text{opt}} = \frac{\sum_{k=1}^K \frac{R_k}{Z_k^2} \underline{v}_k}{\sum_{k=1}^K \frac{R_k}{Z_k^2}}. \quad (4.19)$$

If all distribution paths L_1, \dots, L_N have the same impedance per unit of length, equation (4.19) simplifies in the form:

$$\underline{v}_N^{\text{opt}} = \frac{\sum_{k=1}^K \frac{v_k}{d_k}}{\sum_{k=1}^K \frac{1}{d_k}} \quad (4.20)$$

where d_k are the length of paths L_1, \dots, L_K .

Equations (4.19)-(4.20) give the value of node voltage \underline{v}_N which minimizes the local distribution loss, setting therefore the basis for *quasi-optimum* control. In fact, each DG can compute its voltage reference by (4.19)-(4.20), provided that the parameters of distribution paths are given and that the surrounding node voltages are known by infra-node communication.

From the point of view of controlling the power injection of power sources, as compared to the approaches presented in Sec. 4.1.1 and Sec. 4.1.2, this method has some advantages:

- it requires only local knowledge of network topology and parameters; in a first approximation, controlling an active node requires only to know the neighbor nodes and their distance.
- it fits well with distributed control, since each active node performs independently and needs to communicate only with neighbor nodes.

By recalling (4.11), note also that minimizing the local distribution losses means that each load is fed by the power sources nearby. Thus, quasi-optimum control behaves similarly to optimum control, and local voltage stabilization is ensured also in this case.

4.2 Control Approaches

The approaches to distribution loss minimization described in the previous section can be employed to devise control techniques for electronics power converters connected to the distribution grids. These, described in more detail in [181], are outlined in the following subsections.

4.2.1 Optimum Current Control

Equation (4.7) can be directly employed to control DGs in order to attain the minimum distribution loss. As previously shown, distribution losses are minimized when the loads are fed by neighboring power sources, so that the active and reactive current flow across the distribution lines reduces and the voltage drops on the line impedances reduce too. Besides, from the application point of view, it is worth noting the following facts.

- Applying the optimum control technique expressed by (4.7) requires a full knowledge on the microgrid, including topology, cables, loads, and generators, which is reasonable for medium-voltage distribution grids but may be difficult for low-voltage residential grids.
- The optimum control approach is well suited if all data are managed by a central control hub, while it is difficult to apply in presence of a distributed control environment, which is typical of smart microgrids.
- The DG active currents are usually constrained by the power available from local energy resources. However, optimum control can profitably be applied to reactive currents, which are only limited by the VA ratings of DGs.

For these peculiarities, the optimum control performance can be effectively regarded as a benchmark for any other control technique, whereas it poses some challenging issues from the point of view of the implementation, as shown in [183].

4.2.2 Distance-Based Control

Control approaches like the one referred to in the previous subsection, taking into account grid topology, with its parameters, and connection configurations, can bring to the optimal sharing of the power needs, but require a complete knowledge of the controlled system and involve onerous computations. Instead, on the basis of result (4.12), a control approach aiming at minimizing the distribution loss while avoiding overloading of DGs can be devised from a simplified and intuitive perspective.

Indeed, (4.12) indicates that the distribution losses tend to decrease if each DG feeds the active and reactive power demanded by the loads nearby. A control method can therefore be devised in which the loads split their power demand among the different sources in inverse proportion of the distance. Such an approach, which only requires the knowledge of node-to-node distances, may be applied in both tree-shaped and meshed grids and leads to an operating condition very close to optimum [180]. Clearly, from the point of view of the implementation, a bidirectional communication link is needed between loads and generators.

This kind of distributed control, which shares a load among its neighboring sources in inverse proportion of the distance, is called *distance-based criterion*. Its basic principle of operation is now briefly described.

Distance-Based Criterion

Let \dot{a}_l be the complex power absorbed at passive grid node l ($l \in \{1, \dots, L\}$) and be the complex power fed by the DG at the active node n ($n \in \{1, \dots, N\}$):

$$\dot{a}_l = p_l + jq_l, \quad (4.21)$$

$$\dot{a}_n = p_n + jq_n. \quad (4.22)$$

In a first instance, the control system shares the power demand \dot{a}_l of each passive node among all active nodes (including the utility at PCC) in inverse proportion of their distances d_l^n from node l . Accordingly, the complex power \dot{a}_l^n requested from passive node l to active node n is:

$$\dot{a}_l^n = \dot{a}_l \frac{1}{d_l^n} \left(\sum_{n=1}^N \frac{1}{d_l^n} \right)^{-1}, \quad (4.23)$$

therefore, each active node n receives L power requests by the loads connected at passive nodes, for a total amount:

$$\dot{a}_n = \sum_{l=1}^L \dot{a}_l^n. \quad (4.24)$$

Note that, in order to implement control algorithms (4.23)-(4.24), the knowledge of node-to-node distances is required. While the meaning of node-to-node distance is clear

and unique in tree-shaped networks, it may be ambiguous in meshed grids, where multiple paths can connect any pair of nodes. In practice, this ambiguity can be overcome by defining the node-to-node distance as the length of the shortest path connecting two nodes. By the way, this information may be obtained, for example, by using PLC ranging techniques based on time of arrival measurements [185, 186].

In [180] the sharing criteria described by (4.23)-(4.24) is enhanced to automatically take into account the finite power availability from distributed sources. In particular, this latter formulation of the algorithm allows to redistribute the exceeding power demand—with respect to the local power availability—to a particular source among other non-saturating sources. Further details concerning the description, analysis, and experimental verification of the distance-based control algorithm are reported in [180].

4.2.3 Surround Control

The *surround control* is a control algorithm that exploits (4.19)-(4.20) to define the behaviour of distributed sources. Its implementation may be supported by the token ring technique, in order to avoid detrimental interactions among sources. With this control technique, at each iteration of the surround control algorithm one particular source, chosen according to predefined priority criteria, is enabled while all the other sources are in a *hold* state, meaning that their control references are not varied. The source that is enabled acquires the phasors of the node voltages measured by the neighboring active nodes, and then computes the new locally optimal node voltage by using (4.19), or (4.20), and its new control reference. The actual control reference may be the calculated optimal voltage itself, or the power injection that corresponds to the desired optimum voltage, given the Thévenin equivalent seen at the output terminals of the particular source.

In order to implement the surround control, first of all, it is necessary to identify the active nodes in the microgrid. In residential settlements, active nodes physically coincide with the power meters of each prosumer (customer equipped with energy sources or energy storage capability). Furthermore, the following assumptions should be verified:

1. active nodes are capable of narrowband communication (e.g., by Power-Line Com-

munication protocols);

2. the communication infrastructure ensures the needed accuracy and security of data, and sufficient bandwidth to allow synchronization of voltage and current phasors;
3. the map of active nodes and their distances is updated at the time of installation of each new active node (given the distribution grid layout), or is dynamically adjusted by ranging techniques.

Correspondingly, each active node cyclically addresses an inquiry to neighbor active nodes, which return their voltage and/or current phasors. The local controller then computes the voltage reference, as described above, and commits this reference to the DG.

4.3 Power Control of Distributed Energy Resources

The approaches described in the preceding paragraphs (i.e., optimum node currents, surround, distance-based approach) pursue the objective of feeding the load within a portion of distribution network by involving distributed resources so that the distribution loss is minimized. To this aim these approaches rely on distribution network models or complex measurement devices, which may not always be available, especially in low-voltage grids. Instead, a paradigm to selectively meet requirements given at the PCC of a distribution network without posing any exacting assumption is considered in this section. By this method, power needs are computed centrally and shared among the distributed resources in a pre-defined manner by means of instantaneous power commands. As shown in the succeeding chapters, this paradigm set the basis for the development of effective model-free control techniques.

In principle, a synergy in controlling the DGs by means of instantaneous power commands is possible only if power commands are additive, which means that they must refer to conservative power terms. For this reason, the instantaneous power terms defined by the Conservative Power Theory (CPT) [8] are considered herein and introduced in the following.

4.3.1 CPT Elemental Quantities

According to the CPT, for a generic W -phase network, the following instantaneous power quantities are defined:

$$\tilde{p}(t) = \mathbf{v} \cdot \mathbf{i}(t) = \sum_{w=1}^W v_w(t) i_w(t) \quad (4.25)$$

$$\tilde{q}(t) = \omega_f \hat{\mathbf{v}} \cdot \mathbf{i}(t) = \omega_f \sum_{w=1}^W \hat{v}_w(t) i_w(t) \quad (4.26)$$

where \mathbf{v} and \mathbf{i} are the vectors of instantaneous phase voltages (v_w) and currents (i_w) measured at a generic network port, $\hat{\mathbf{v}}$ is the vector of unbiased voltage integrals (i.e., voltage integrals without DC component), ω_f is the fundamental angular line frequency, and symbol \cdot means dot product. Note that computation of (4.25) and (4.26) requires integration over a line period ($T_f = 2\pi/\omega_f$) to eliminate DC terms; thus the unbiased voltage integrals $\hat{\mathbf{v}}$ filling the vector $\hat{\mathbf{v}}$ are low-pass filtered variables.

The average values p and q of the above quantities are the active and reactive powers, defined by:

$$p(t) = \langle v, i \rangle(t) = \frac{1}{T_f} \sum_{w=1}^W \int_{t-T_f}^t v_w(\tau) i_w(\tau) d\tau \quad (4.27)$$

$$q(t) = \omega_f \langle \hat{v}, i \rangle(t) = \frac{\omega_f}{T_f} \sum_{w=1}^W \int_{t-T_f}^t \hat{v}_w(\tau) i_w(\tau) d\tau \quad (4.28)$$

where $\langle \cdot, \cdot \rangle$ represents the mean value of the dot product.

4.3.2 Current and Power Decomposition

For a three-phase system under stationary operation the phase currents can be split into fundamental (f) and harmonic, or distortion, (d) terms. Further, the fundamental and harmonic terms can be split in positive-sequence (p), negative-sequence (n), and homo-polar, or zero-sequence, (h) components, namely:

$$\mathbf{i} = \mathbf{i}^f + \mathbf{i}^d = \mathbf{i}^{f,p} + \mathbf{i}^{f,n} + \mathbf{i}^{f,h} + \sum_{k=2}^{+\infty} (\mathbf{i}^{k,p} + \mathbf{i}^{k,n} + \mathbf{i}^{k,h}), \quad (4.29)$$

where k indicates the harmonic order. It is easy to show that all current terms in (4.29) obey independently to the Kirchhoff's Law applied to a generic node of the three-phase distribution network. In fact, harmonic terms cannot instantaneously balance the fundamental ones and, similarly, components of different sequences cannot balance with each other. Thus the Tellegen's theorem applies, which means that it is possible to further split quantities \tilde{p} and \tilde{q} , defined by (4.25) and (4.26), into *conservative power terms* related to sequence and harmonic components, that is:

$$\tilde{p} = \sum_{k=1}^{+\infty} (\mathbf{v} \cdot \mathbf{i}^{k,p} + \mathbf{v} \cdot \mathbf{i}^{k,n} + \mathbf{v} \cdot \mathbf{i}^{k,h}) = \tilde{p}^{f,p} + \tilde{p}^{f,n} + \tilde{p}^{f,h} + \sum_{k=2}^{+\infty} (\tilde{p}^{k,p} + \tilde{p}^{k,n} + \tilde{p}^{k,h}), \quad (4.30)$$

$$\tilde{q} = \sum_{k=1}^{+\infty} (\hat{\mathbf{v}} \cdot \mathbf{i}^{k,p} + \hat{\mathbf{v}} \cdot \mathbf{i}^{k,n} + \hat{\mathbf{v}} \cdot \mathbf{i}^{k,h}) = \tilde{q}^{f,p} + \tilde{q}^{f,n} + \tilde{q}^{f,h} + \sum_{k=2}^{+\infty} (\tilde{q}^{k,p} + \tilde{q}^{k,n} + \tilde{q}^{k,h}). \quad (4.31)$$

Decomposition (4.30) and (4.31) associate each current component to a conservative power and energy term and sets the basis for distributed approaches to the compensation of load unbalance, harmonics, and reactive power. In fact, the load unbalance seen at a generic port of a radial distribution system (e.g., at PCC) is compensated if the fundamental negative-sequence currents absorbed at that port is eliminated. This, in turn, can be achieved by instructing the downstream EPPs to feed the opposite of active power $\tilde{p}^{f,n}$ and reactive power $\tilde{q}^{f,n}$ measured at the port. Similarly, to mitigate distortion, DGs may be committed to feed the opposite of power terms \tilde{p}^d and \tilde{q}^d .

Note finally that the average value q^p of instantaneous reactive power \tilde{q}^p coincides with usual reactive power definition, which is associated to positive-sequence fundamental currents only. Thus, compensating for instantaneous quantity \tilde{q}^p causes the reactive power to vanish.

The advantage of driving the DGs by power commands, instead of current commands, is that power terms (4.30) and (4.31) are not affected by voltage and phase shift caused by transformers. Instead, they can be affected by the power loss and energy storage in line impedances. This phenomenon is marginal at fundamental frequency, but becomes increasingly relevant at higher frequencies, thus significantly reducing the effectiveness of the above compensation approach beyond few hundred Hz.

4.3.3 Compensation Based on Instantaneous Power Terms

In order to generate the power commands for distributed DGs, the central controller processes the voltage and current data measured at PCC (\mathbf{v}_{PCC} , \mathbf{i}_{PCC}), or at any other node requiring compensation. Let i_{PCC}^{rms} be the collective rms value of the currents at PCC, defined by:

$$i_{PCC}^{rms}(t) = \sqrt{\sum_{w=1}^W i_{PCC,w}^{rms2}(t)} = \sqrt{\sum_{w=1}^W \frac{1}{T_f} \int_{t-T_f}^t i_{PCC,w}^2(\tau) d\tau}. \quad (4.32)$$

Since sequence and harmonic terms are orthogonal to each other, term i_{PCC} can be split as:

$$i_{PCC}^{rms} = \sqrt{i_{PCC}^{rms f,p2} + i_{PCC}^{rms f,n2} + i_{PCC}^{rms f,h2} + i_{PCC}^{rms d2}}. \quad (4.33)$$

Correspondingly, the apparent power a_{PCC} can be decomposed as:

$$a_{PCC} = v_{PCC}^{rms} i_{PCC}^{rms} = \sqrt{p_{PCC}^2 + q_{PCC}^2 + n_{PCC}^2 + h_{PCC}^2 + d_{PCC}^2}, \quad (4.34)$$

where, by indicating with ϕ^p the phase shift of positive-sequence currents, the power terms in (4.34) are defined as:

$$p_{PCC} = v_{PCC}^{rms} i_{PCC}^{rms f,p} \cos \phi^p \quad \text{active power} \quad (4.35)$$

$$q_{PCC} = v_{PCC}^{rms} i_{PCC}^{rms f,p} \sin \phi^p \quad \text{reactive power} \quad (4.36)$$

$$n_{PCC} = v_{PCC}^{rms} i_{PCC}^{rms f,n} \quad \text{unbalance power} \quad (4.37)$$

$$h_{PCC} = v_{PCC}^{rms} i_{PCC}^{rms f,h} \quad \text{homo-polar power} \quad (4.38)$$

$$d_{PCC} = v_{PCC}^{rms} i_{PCC}^{rms f,d} \quad \text{distortion power} \quad (4.39)$$

Given power terms (4.35)-(4.39), the central controller defines the goal of compensation, namely, the relative amounts γ_q , γ_n , and γ_d of, respectively, reactive, unbalance, and distortion power to be eliminated. The instantaneous compensation power commands are then

generated as:

$$\tilde{p}_{comp}^* = -\mathbf{v}_{PCC}^{f,p} \cdot (\gamma_n \mathbf{i}_{PCC}^{f,n} + \gamma_d \mathbf{i}_{PCC}^d), \quad (4.40)$$

$$\tilde{q}_{comp}^* = -\omega_f \widehat{\mathbf{v}}_{PCC}^{f,p} \cdot (\gamma_q \mathbf{i}_{PCC}^{f,p} + \gamma_n \mathbf{i}_{PCC}^{f,n} + \gamma_d \mathbf{i}_{PCC}^d). \quad (4.41)$$

Observe that in (4.40)-(4.41) only the fundamental positive-sequence voltages are considered. This is because DGs cannot compensate for the voltage asymmetry and distortion which are inherent to the mains, but only for those generated by the loads fed by the distribution grid. To deparure the effects of the source non-ideality, power commands (4.40)-(4.41) are created by considering only the fundamental positive-sequence voltages measured at PCC \mathbf{v}_{PCC}^p in place of total voltages \mathbf{v}_{PCC} . This avoids the risk to generate instabilities by trying to compensate voltage components which are outside our control capability.

Power commands (4.40)-(4.41) are then shared among EPPs depending on their power capability and distance from the loads requiring compensation. In this way, the compensation duty is primarily demanded to the EPPs that are closer to the disturbing loads, thus minimizing any useless power flow in the distribution lines and eventually improving the distribution efficiency.

In the following homo-polar power terms are disregarded. In fact, zero-sequence voltages at PCC are usually negligible. Moreover, homo-polar currents are often eliminated by MV/LV transformers and can be compensated only on a local basis.

4.3.4 Actual Power Commands Generation

In order to properly instruct the distributed EPPs for selective compensation, the central controller processes separately the positive- and negative-sequence power terms for each current harmonics. As shown before, in fact, these power terms are independent from each other and convey the information needed to selectively compensate the corresponding harmonic sequence components.

Let \mathbf{a} be the positive-sequence operator, \mathbf{a}^* the negative-sequence operator (i.e., the

complex conjugate of \mathbf{a}), $\mathbf{1}$ the unity vector (homo-polar operator), defined by:

$$\mathbf{a} = \begin{bmatrix} 1 \\ e^{-j\frac{2\pi}{3}} \\ e^{+j\frac{2\pi}{3}} \end{bmatrix}, \quad \mathbf{a}^* = \begin{bmatrix} 1 \\ e^{+j\frac{2\pi}{3}} \\ e^{-j\frac{2\pi}{3}} \end{bmatrix}, \quad \mathbf{1} = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}. \quad (4.42)$$

Assuming that all DGs share the same time reference, let's define the rotating reference vector \dot{r}^k at the k -th harmonic as:

$$\dot{r}^k = e^{jk\omega_f t} = \cos k\omega_f t + j \sin k\omega_f t. \quad (4.43)$$

Any set of three-phase variables \mathbf{x}_n , measured at generic grid node n , can therefore be represented by the phasors of its harmonic sequence components (whose amplitude is the rms value), defined by:

$$\underline{x}_n^{k,p} = \frac{\sqrt{2}}{3} \langle \mathbf{x}_n, \mathbf{a} \cdot \dot{r}^k \rangle, \quad (4.44)$$

$$\underline{x}_n^{k,n} = \frac{\sqrt{2}}{3} \langle \mathbf{x}_n, \mathbf{a}^* \cdot \dot{r}^k \rangle, \quad (4.45)$$

$$\underline{x}_n^{k,h} = \frac{\sqrt{2}}{3} \langle \mathbf{x}_n, \mathbf{1} \cdot \dot{r}^k \rangle. \quad (4.46)$$

In applying (4.44)-(4.46), recall that the scalar product of two complex vectors equals the first vector times the complex conjugate of the second vector.

Conversely, given the phasors of the harmonic sequence components, the variables in the time domain can be obtained by applying the inverse relations (symbol \Re means real part):

$$\mathbf{x}_n^{k,p} = \Re \left(\sqrt{2} \underline{x}_n^{k,p} \cdot \mathbf{a} \cdot \dot{r}^k \right) \quad (4.47)$$

$$\mathbf{x}_n^{k,n} = \Re \left(\sqrt{2} \underline{x}_n^{k,n} \cdot \mathbf{a}^* \cdot \dot{r}^k \right) \quad (4.48)$$

$$\mathbf{x}_n^{k,h} = \Re \left(\sqrt{2} \underline{x}_n^{k,h} \cdot \mathbf{1} \cdot \dot{r}^k \right) \quad (4.49)$$

4.3.5 Harmonic Sequence Compensation Commands

Based on previous definitions, the central controller determines by (4.44)-(4.46) the positive and negative sequence components of every (k -th) harmonic term of the currents measured at PCC, including the fundamental, as:

$$\underline{i}_{PCC}^{k,p} = \frac{\sqrt{2}}{3} \langle \mathbf{i}_{PCC}, \mathbf{a} \cdot \dot{r}^k \rangle, \quad \underline{i}_{PCC}^{k,n} = \frac{\sqrt{2}}{3} \langle \mathbf{i}_{PCC}, \mathbf{a}^* \cdot \dot{r}^k \rangle. \quad (4.50)$$

As said before, the homo-polar terms are neglected. Similarly, the fundamental positive-sequence phasor of the voltages at PCC is determined as:

$$\underline{v}_{PCC}^{f,p} = \frac{\sqrt{2}}{3} \langle \mathbf{v}_{PCC}, \mathbf{a} \cdot \dot{r}^f \rangle = v_{PCC}^{rms f,p} e^{j\phi_{PCC}^{f,p}}. \quad (4.51)$$

To compensate for the power terms $\dot{a}_n^{k,p}$ and $\dot{a}_n^{k,n}$ assigned by the central controller, the DG must provide the current terms:

$$\underline{i}_n^{f,p} = \left(-\frac{\dot{a}_n^{k,p}}{\underline{v}_n^{k,p}} \right)^*, \quad \underline{i}_n^{f,n} = \left(-\frac{\dot{a}_n^{k,n}}{\underline{v}_n^{k,n}} \right)^*. \quad (4.52)$$

The DG current references \mathbf{i}_n^{ref} are finally obtained by converting (4.52) in the time domain, namely:

$$\mathbf{i}_n^{ref} = \sum_{k=1}^K (\mathbf{i}_n^{ref k,p} + \mathbf{i}_n^{ref k,n}) = \sum_{k=1}^K \sqrt{2} \Re \left((\underline{i}_n^{k,p} \mathbf{a} + \underline{i}_n^{k,n} \mathbf{a}^*) \dot{r}^k \right), \quad (4.53)$$

where K is the order of the highest harmonic to be compensated. These current references are executed by the DG according to usual current control techniques.

In general, compensation of distortion power is less effective for high-frequency harmonics. In fact the line impedances increase with frequency, causing higher voltage drops which affect control accuracy. For this reason, the proposed control method is applicable only to compensate for harmonic distortion in the lower frequency range (few hundred Hz).

4.4 Summary

The chapter lays out the theoretical considerations at the basis of the work presented in the following chapters. The issue of distribution loss minimization is analyzed from both a global and local perspective. Three control techniques applicable to smart microgrids are discussed, highlighting the main advantages and disadvantages of specific approaches. Optimum and quasi-optimum control approaches are described, which attain maximally efficient operating regimes, but require knowledge on grid topology and parameters, or relies on critical measurements. The distance-based control has been proposed to relax these requirements while retaining beneficial effects on distribution efficiency. The distance-based control uses conservative power quantities, which can be univocally interpreted by units that are geographically distributed, for both measure the loading condition of the microgrid and to commit control signals to DGs. Though, in general, local constraints (e.g., inverter saturation) are difficult to fit in the control scheme and, in addition, none of the approaches is totally independent of critical information.

In the final part of the chapter, a paradigm for the control of DGs based only on power quantities is introduced, which enables control approaches not to rely on microgrid's models nor on strict synchronization on measurement or control processes.

Chapter 5

Low-Voltage Microgrid Architecture

This chapter introduces the microgrid architecture that is proposed to coordinate the operation of distributed resources in low-voltage grids. The aim of the architecture is to enable low-voltage grids to efficiently support the functionalities that characterize smart microgrids, such as, high distribution efficiency, demand response, islanded operation, improved power quality at PCC.

The first part of the chapter describes the master/slave architecture with its constituting components. A general control framework for the control of distributed energy resources based on the power control paradigm defined in Sec. 4.3 is proposed to be applied to the master/slave architecture. In the second part of the chapter, the utility interface, which plays a key role for the microgrid while operating islanded from the mains, is presented and analyzed.

5.1 Master/Slave Architecture

The microgrid scenario considered herein concerns low-voltage networks with high penetration of DERs. The microgrid structure proposed to efficiently use the available resources is outlined in Fig. 5-1. There, DERs are interfaced to the distribution network by means of so called *energy gateways*, and the microgrid is interfaced to the utility by means of a *utility interface*; an information and communication technology (ICT) infrastructure that links the resources is assumed to be available for slow-speed data collection and data exchange.

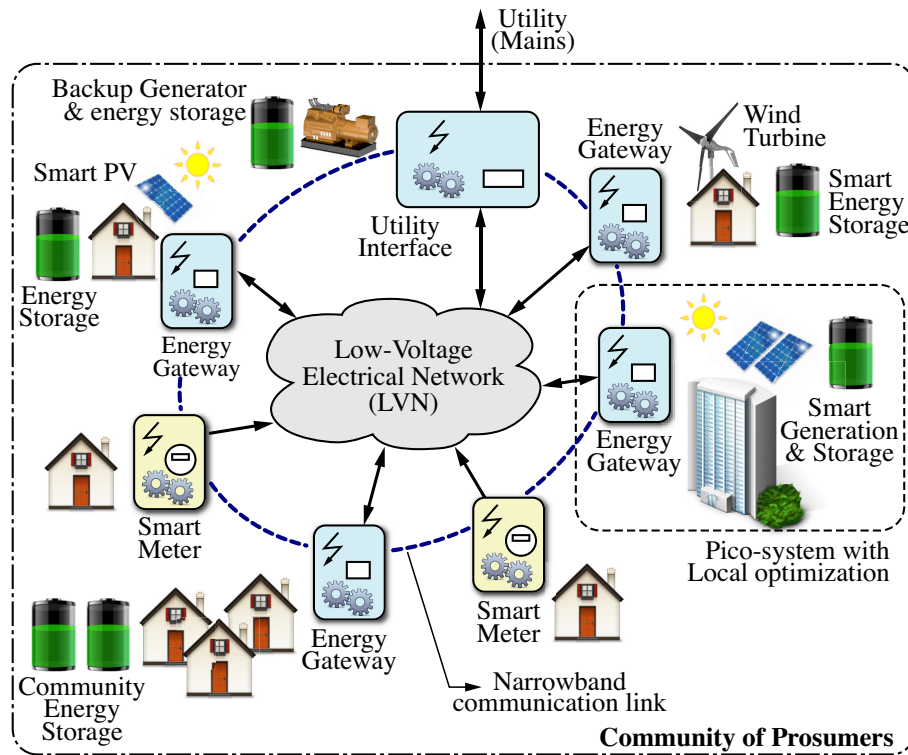


Figure 5-1: Considered microgrid scenario.

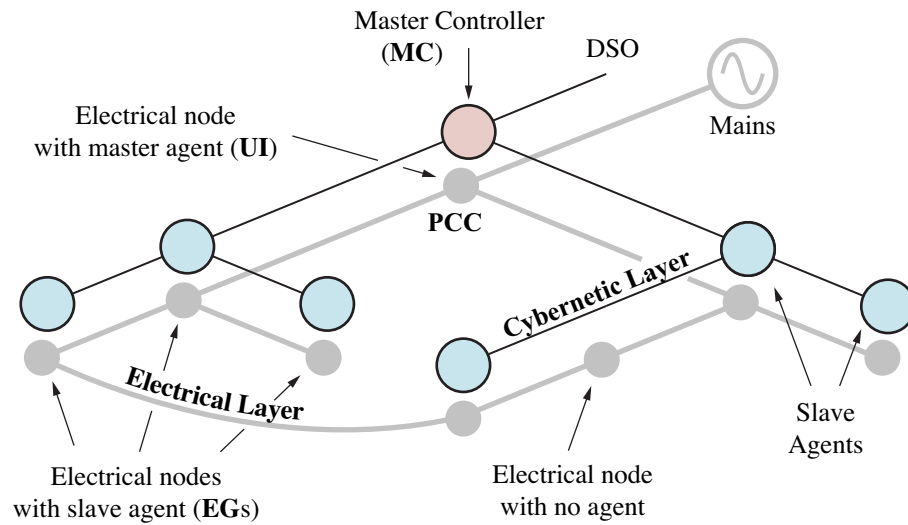


Figure 5-2: Master/slave microgrid architecture.

The microgrid architecture proposed to manage the delineated scenario is shown in Fig. 5-2. The figure highlights the two layers composing the microgrid architecture: the electrical layer and the cybernetic layer. The electrical layer represents the electrical infrastructure, which comprises, in particular, the mains, the distributed energy resources, and the electrical distribution network. The cybernetic layer represents the ICT infrastructure needed for the monitoring and control of the electrical layer, and comprises the sensors, the computation units, and the communication modules and links.

The main devices constituting the architecture are described in detail in the following.

- *Utility Interface (UI)*. The UI is an electronic power processor equipped with energy storage and connected at the point of common coupling (PCC) of the microgrid with the utility. In grid-connected mode, the UI performs as a voltage-driven voltage support source synchronized with the mains, while in islanded mode it becomes the voltage-forming device for the whole microgrid (see Sec. 2.3.1). The UI constitutes by itself a controllable energy resource that can be employed to improve the microgrid behavior seen by the mains. To that purpose, the local control unit of the UI may interact with other intelligent devices via the cybernetic layer.
- *Energy Gateway (EG)*. An EG is a distributed energy resource that can be controlled to contribute to microgrid power needs. In addition to the energy resource, which can be a combination of renewable sources and storage devices, an EG is equipped with a local control unit (LCU) and an electronic power processor (EPP). Its structure can be the one represented in Fig. 3-1. The local control unit collects all the quantities needed to determine the state of the local resources and generates the reference set-point of the power to be injected to the grid. The references calculated by the local control unit are then actuated by the EPP, which electrically interfaces the energy resources to the grid. The EG interacts through the EPP with the electrical layer, and through the local control unit with the cybernetic layer. A node connecting an EG to the grid is referred to as an *active node*.
- *Passive nodes*. The remaining nodes that host passive devices, namely, link-up loads only, are referred to as *passive nodes*. Though not necessarily endowed with any

particular kind of intelligent measurement or control device, passive nodes may be equipped with smart meters (SM) performing local measurements and handling one-way communication to a centralized microgrid controller.

In the cybernetic layer displayed in Fig. 5-2, a master/slave control is considered to supervise the operation of the controllable devices introduced above, namely, the UI and the EGs. It is assumed that the microgrid's *master controller* (MC) is deployed in the UI, whereas the EGs, which are geographically distributed, play the role of the slave agents. The master unit (i.e., the MC) can communicate with the slave units (i.e., the EGs) via a communication channel (e.g., via power-line communication).¹

5.1.1 General Control Principle

In the proposed microgrid architecture it is assumed that the UI permanently performs as a voltage source while EGs are driven as current sources. In grid-connected operation the UI behaves as grid-supporting voltage source and can implement ancillary control functions (e.g., management of UI's energy storage, compensation of residual load unbalance and distortion). Since the power balance is ensured by the mains, the local control needs may prevail, and each active node makes available only its residual power and energy capacity for microgrid control. In spite of this limitation, the power flow from EGs can be adjusted by the MC to meet global needs (e.g., grid voltage stabilization, power loss minimization, peak power shaving, demand response, day-ahead planning, low-voltage ride through).

A different scenario occurs in islanded operation, during transitions from on-grid to off-grid, and under black start. In these cases, the UI acts as grid-forming voltage source, and the MC manages the entire energy reserve of the microgrid to ensure power balance. The EGs keep behaving as current sources, but the whole energy generated and stored locally is made available to sustain microgrid operation. The EGs can also be driven to a controlled overload condition to meet temporary energy constraints.

In all cases the distributed units cooperate to fulfill microgrid's needs. However, while

¹A detailed investigation about the feasibility of such approaches in terms of the performance required to the communication channel is provided by Angioni *et al.* in [187], referring to, specifically, the Long-Term Evolution (LTE) technology.

in grid-connected operation local requirements may prevail, in any other operating condition the microgrid needs are given higher priority. This change of priority does not require modification of control algorithms; it is simply determined by the MC, which knows the overall power capacity of DERs, by properly assigning power commands to EGs.

5.1.2 General Control Structure

A general structure of the control algorithm is defined as follows. At the beginning of each control period T (lasting few line cycles) the MC in the UI polls all the nodes of the microgrid. The active nodes return the values of active and reactive power which are available for microgrid control, while passive nodes may return their active and reactive power consumption. More in detail, the data packet sent by the n -th EG to MC includes:

1. the power rating of the grid-tied electronic power processor (a_n);
2. the active and reactive power (p_n, q_n) exchanged with the grid;
3. the active and reactive power (p_l, q_l) absorbed by local loads;
4. the estimated active power \hat{p}_n generated by local power sources;
5. the estimated maximum additional energy that can be stored in the ES unit ($\hat{e}_{S,n}^{\text{in}}$) and maximum energy that can be extracted from the ES unit ($\hat{e}_{S,n}^{\text{out}}$);
6. the estimated upper and lower limit ($\hat{p}_n^{\text{min}}, \hat{p}_n^{\text{max}}$) of the active power deliverable by the EG, including ES power limits ($\hat{p}_{S,n}^{\text{in}}, \hat{p}_{S,n}^{\text{out}}$), local constraints on admissible power injection at the node, other needs that are specific to the particular node.

The same data structure can be used for passive nodes, by disregarding the fields related to power generation. Fig. 5-3 represents schematically the generic structure of an EG and reports all the relevant parameters; management algorithms may use all, or a subset of, these parameters for control purposes.

After collecting data from all the nodes, the MC can compute a set of quantities defining the power and energy state of the microgrid. The MC then executes a control algorithm that depends on the operating mode (grid-connected or islanded) and the relative amount

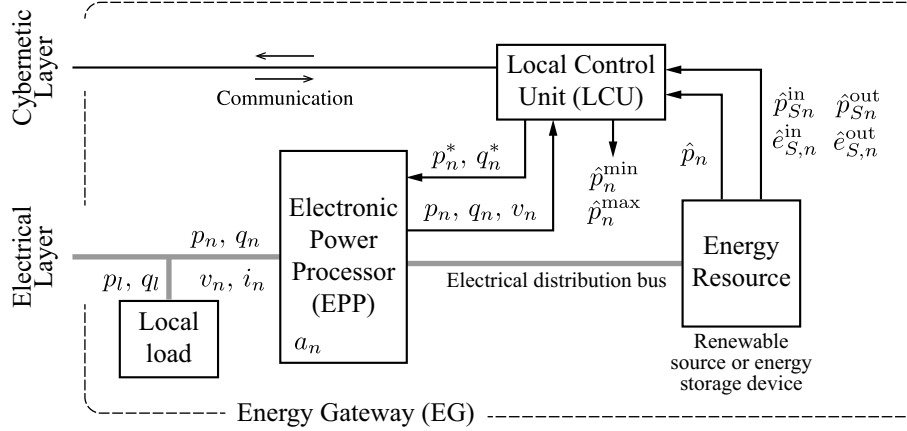


Figure 5-3: Generic structure of an energy gateway.

of generated and absorbed power. To that purpose, the MC computes the total power consumed ($p_{l,tot}$) and the range of power that can be generated ($\hat{p}_{l,tot}$, $\hat{p}_{l,tot}^{\min}$, $\hat{p}_{l,tot}^{\max}$) within the microgrid as:

$$p_{l,tot} = \sum_{l=1}^L p_l, \quad \hat{p}_{n,tot} = \sum_{n=1}^N \hat{p}_n, \quad \hat{p}_{n,tot}^{\min} = \sum_{n=1}^N \hat{p}_n^{\min}, \quad \hat{p}_{n,tot}^{\max} = \sum_{n=1}^N \hat{p}_n^{\max}. \quad (5.1)$$

and identify the most appropriate control action to be demanded to EGs. The following cases are identified.

Grid-connected operation

In this case, power control is non-critical since the mains ensure the power balance. Thus the LCUs of EGs can choose the power to deliver, their actual choice being dependent on the kind of local power source and energy needs. In fact, renewable energy sources (e.g., wind or PV) should be fully exploited, while cost/benefit issues can drive the choice for other types of sources (e.g., small hydro, fuel-cells, gas turbines). In any case, EGs can feed reactive power to support loads demand, so that to reduce distribution losses, improve node voltage stability, and increase the power factor at PCC. By request of the MC, EGs can also adjust their active power flow. This can be done to meet special needs of the microgrid (e.g., voltage support, thermal limitation in feeders, intentional islanding conditions), or to respond to requests from the utility (e.g., demand-response).

Islanded Operation

In this case the power balance must be ensured within the microgrid. Two situations can be distinguished.

- *Over-generation* ($\hat{p}_{n,tot} > p_{l,tot}$). In this situation, the total power generated by distributed sources exceeds the loads consumption. Under steady-state conditions, the extra-power is stored in distributed ES devices according to their state of charge, and the EGs are driven accordingly.

Under transient conditions, the dynamic power unbalance is temporarily faced at the expense of the energy stored in the UI, since the UI acts as voltage source and automatically fulfills every dynamic power request. However, within few line cycles the EGs power commands are adapted to the new situation and the load power demand is shared among DERs. The state of charge of the UI's energy storage is promptly restored to ensure the capability to face new transients.

If over-generation lasts too long, the power generated by renewable sources is scaled down to meet the actual power consumption, according to a suitable sharing criterion. Within their kVA ratings, the EGs can also feed reactive power to meet load demand and stabilize node voltages.

- *Under-generation* ($\hat{p}_{n,tot} < p_{l,tot}$). In this situation, the power generated within the microgrid is not enough to fulfill the demand from loads. The power balance must therefore be ensured by taking advantage of the distributed ES units, according to their energy availability. Clearly, this kind of operation can be maintained for a limited time. Then, non-priority loads must be disconnected to prevent full discharge of ES units and, in particular, of UI's energy storage. Also in this case, EGs can feed reactive power, within their power capability, in order to stabilize node voltages and reduce distribution losses.

The control structure described above is represented in Fig. 5-4.

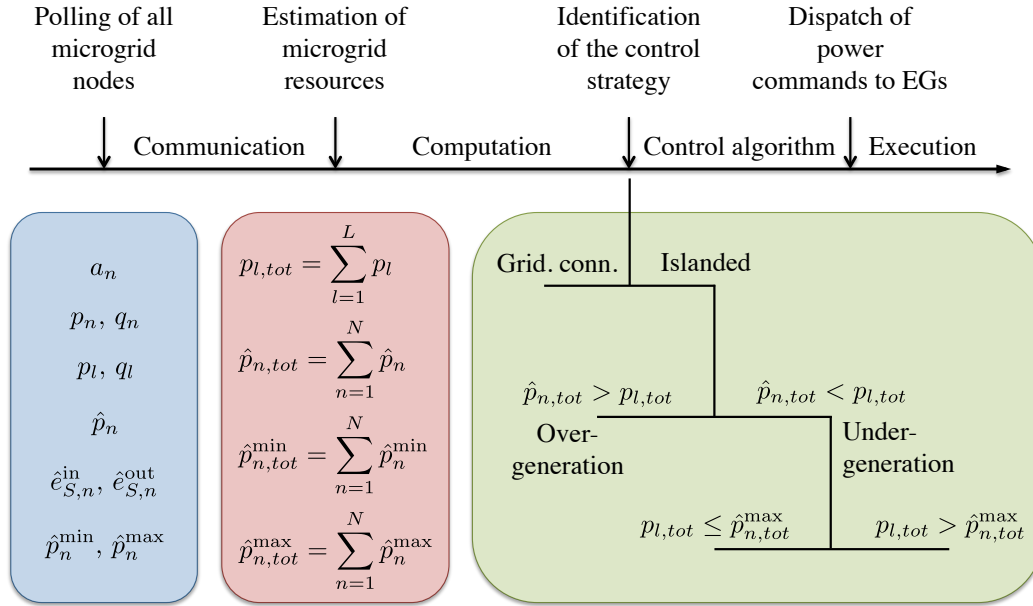


Figure 5-4: Master/slave control principle.

5.1.3 Relations with IEEE Standard P2030.2

From the implementation point of view, it is worth mentioning the forthcoming IEEE standard P2030.2 [188], concerning the interoperability of energy storage systems integrated with the electric power infrastructure. The main energy storage applications classified by the standard, namely, the power, the capacity, and the energy applications, are relevant to the architectural and management frame introduced above. In particular, the UI falls into the category of power applications, which are characterized in providing high power output for relatively short periods of time (a few seconds to a few minutes) in case of transient and temporary imbalance. The EGs fall into the category of capacity applications, which are characterized in requiring relatively limited amount of energy storage, feature employed to defer or to reduce the need for other equipment. Finally, energy application services, featuring the possibility to supply relatively large amounts of energy for an extended period of time (minutes to hours), are provided by the aggregation of all the EGs.

Furthermore, the functionalities included in the architecture find correspondence in the functionalities regulated by the standard. Indeed, most of the functionalities performed by the algorithm are therein mentioned and classified, like, for example, the load following functionality at the PCC of the microgrid, the enhanced electric service reliability (shield-

ing the local loads from issues in the main grid by operating in the islanded mode), the transmission congestion relief during periods of peak production, the filtering of the intermittent power generation profile at PCC (i.e., renewable capacity firming).

The standard is therefore pertinent to the considered application, offering an official means to define and eventually implement the various aspects of the specific architecture that are related to the power system, the communication, and the information technology interoperability.

5.1.4 Comparison with Droop-Based Approaches

The microgrid architecture considered here significantly differs from those based on the droop control. Droop control [77] represents the most known method to control parallel connected sources. It has been widely investigated in the literature [189], employed in industrial applications, and, recently, in AC and DC experimental microgrids [67, 166]. In a power system composed of multiple loads and sources the main advantage of the droop control is the possibility to share the load power needs among generators without requiring any explicit communication among the units. Another peculiar advantage is the intrinsic redundancy of such a scheme, since all the converters operate as voltage sources with the same control algorithm, so that the failure of a subset of the generators does not compromise the integrity of the system. These advantageous features are not present in the considered approach. In particular, the functionalities performed by the UI (chiefly the islanded operation) cannot be fulfilled if the UI is damaged, even though the control algorithm may actually keep a proper control of EGs during grid connected operation. On the other hand, the conventional droop control presents some disadvantages that may not appear in the considered architecture, such as non-constant magnitude and frequency of the grid voltage, sensitiveness to grid parameters, limited circulating and harmonic current controllability, limited accuracy in reactive power sharing (specially in grids with high R/X ratios), and slow response times. These issues are not present in the considered architecture.

Finally, for what concerns the proposed architecture, it is also worth remarking that:

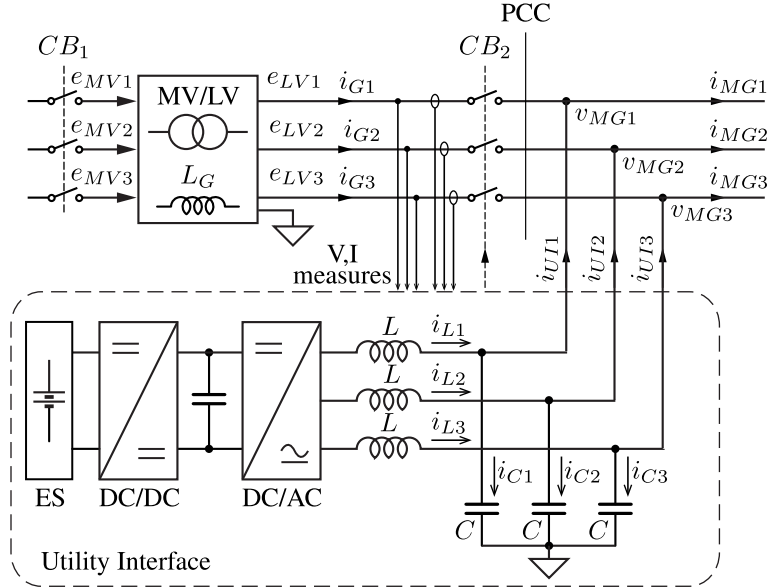
- the need for a communication infrastructure is not a critical aspect in the considered scenario, indeed the presence of communication is a key feature of smart microgrids [169, 190];
- a communication loss does not jeopardize the system: a loss of communication simply downgrades an EG to a standard current controlled source (which can maintain its local control functionalities);
- the need of communication does not represent a disadvantage with respect to other control techniques (e.g., see [126, 160]) whose final application requires a communication network for effective operation.

5.2 Utility Interface

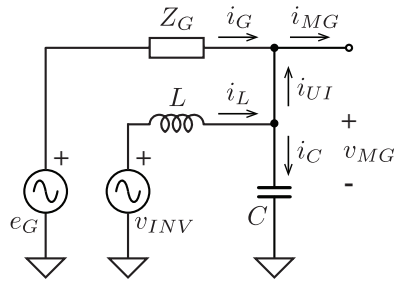
In the master/slave architecture the role of the UI is crucial to assure smooth operation of the microgrid [59, 191] and to solve some open problems, in particular, the management of black starts, that is, when the microgrid starts up without grid support, and unintentional islanding, that is, when the mains suddenly disconnects itself and the microgrid stands alone. In this section the control requirements of the UI are stated and an instance of UI is proposed and designed.

The typical configuration of the UI is shown in Fig. 5-5(a). It is located at the PCC between the utility grid and the microgrid, namely, at the output terminals of the step-down power transformer feeding the 4-wire low-voltage distribution grid. The UI is made up of: three-phase grid-connected inverter with line-side LC filter, to provide low output impedance at high frequency; a storage device for power application that enables the control of the power flow at the PCC; a local control unit. Within the master/slave architecture the MC can be deployed in the local control unit of the UI, which collects data from the utility and the microgrid and computes control commands for the UI itself and, possibly, for EGs.

The following subsections consider a multi-functional control system for the UI that can provide all the needed features, namely:



(a) Connection scheme.



(b) Equivalent simplified model.

Figure 5-5: The utility interface.

- operation as grid-supporting voltage source, capable of compensating reactive, unbalance, and distortion currents drawn by the loads during grid connected operation;
- operation as grid-forming voltage source, setting the voltage and frequency for the entire microgrid during islanded operation;
- operation as active smoothing device, ensuring soft transitions even for unintentional islanding or black start, during the transition to islanded operation.
- operation as active decoupling device, avoiding perturbations to propagate from load to supply and vice-versa.

These features extends those of usual line-interactive UPS systems [37] and allow effective and fast interaction between utility and microgrid.

5.2.1 Utility Interface Control Principle

For simplicity, let us consider the equivalent single-phase (phase-to-neutral) representation of the UI shown in Fig. 5-5(b). The utility supplies AC voltage e_G through impedance Z_G made of a series resistive component R_G and a series inductive component L_G . The UI inverter feeds AC current i_L through filter inductance L . This current is partially absorbed by shunt filter capacitor C , and partially flows to the PCC (i_{UI}), where load current i_{MG} is drawn.

As mentioned before, the UI must perform as a voltage source with low internal impedance, so that to be capable of sustaining fast power changes. A voltage control loop is therefore needed, complemented by a fast internal current loop to improve dynamic response and prevent over-currents. A slow external current loop is also needed that, in the long term, adjusts the inverter currents so as to compensate for voltage harmonics, load unbalance, and reactive power.

A single-phase, equivalent scheme of UI control is sketched in Fig. 5-6. It includes the three control loops mentioned above. The outer current loop has a limited bandwidth (few Hz) and enforces line current i_G to track reference i_G^* at low frequency, for compensation purposes. The intermediate voltage loop has a wider bandwidth (a few hundred Hz), and

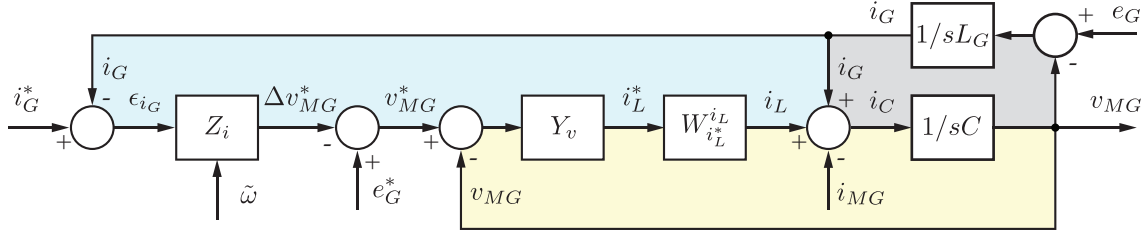


Figure 5-6: UI control scheme.

enforces phase voltage v_{MG} to track reference v_{MG}^* in the mid-frequency range, thus providing the voltage source feature required by the UI. The inner current loop has a large bandwidth (a few thousand Hz), and enforces inverter current i_L to track reference i_L^* in the high-frequency range. In the following, it is assumed that this loop performs almost ideally, in particular, that the transfer function between i_L^* and i_L [$W_{i_L^*}^{i_L}$ in Fig. 5-6] is nearly unity; Ch. 6 is dedicated to high performance current controllers that easily fulfill this assumption. Note that actual voltage reference v_{MG}^* is obtained from the estimate of the utility voltage e_G^* (specified in next section) by subtracting voltage error Δv_{MG}^* , which is derived by amplifying the line current error $\epsilon_{i_G} = i_G^* - i_G$.

The proposed control structure allows soft transitions from grid connected to islanded operation. To this purpose, it is sufficient to set line current reference i_G^* to zero; within the response time of the external loop, the line current vanishes and the voltage loop brings the PCC voltage at reference value v_{MG}^* . In case of non-intentional islanding the behavior is the same, with the additional delay time needed to detect the islanded condition.

In general the control performs as follows.

- In grid connected operation, the UI performs as a grid-supporting voltage source and the UI output voltage v_{MG} is adjusted to enforce line current i_G to track reference i_G^* . If i_G^* is properly chosen (purely sinusoidal positive-sequence), a slow control action occurs, which removes the reactive and unbalance current terms at the fundamental frequency, thus improving the power factor at PCC. Moreover, if the voltage loop is fast enough and grid current regulator Z_i is appropriately designed, voltage error Δv_{MG}^* drives the inverter to compensate for the harmonic currents that may be generated by the load, thus reducing the THD as well.

- In islanded operation, line current i_G and reference i_G^* vanish, so that error signals ϵ_{i_G} vanishes too and inverter voltage reference v_{MG}^* coincides with e_G^* . Therefore, the UI performs as a grid-forming unit and keeps the PCC voltage at the specified amplitude and frequency. Controller Y_v must damp the oscillations caused by the resonance of filter capacitor C with the series inductive component L_G of Z_G . Moreover, it must provide enough control bandwidth to preserve the voltage purity at PCC in spite of load current harmonics.
- The transitions from grid connected to islanded operation run smoothly since control discontinuities are prevented. This is obtained by driving to zero the voltage error Δv_{MG}^* .

5.2.2 Control Structure Analysis

In this subsection the main transfer functions needed to design the controllers of the block scheme in Fig. 5-6 are determined.

Let's consider first the resonant loop shown in the upper-right part of Fig. 5-6 and derive the transfer functions from input i_L to outputs v_{MG} and i_G in the form G_{in}^{out} :

$$G_{i_L}^{v_{MG}}(s) = \frac{Z_G}{1 + sZ_G C}, \quad (5.2)$$

$$G_{i_L}^{i_G}(s) = \frac{1}{1 + sZ_G C}. \quad (5.3)$$

Then, let's consider the voltage control loop and determine the closed-loop transfer functions between input v_{MG}^* to output v_{MG} in the form H_{in}^{out} :

$$H_{v_{MG}^*}^{v_{MG}} = \frac{Y_v W_{i_L^*}^{i_L} G_{i_L}^{v_{MG}}}{1 + Y_v W_{i_L^*}^{i_L} G_{i_L}^{v_{MG}}} \quad (5.4)$$

where $W_{i_L^*}^{i_L}$ is the closed-loop transfer function of the inner inductor current control loop. As discussed in [192], $W_{i_L^*}^{i_L}$ can be modeled by a low-pass filter or a pure delay. The effect of the static gain and cut-off frequency parameters of $W_{i_L^*}^{i_L}$ are evaluated in Fig. 5-9.

Finally, the closed-loop transfer function of the outer grid current control loop can be

expressed in the form W_{in}^{out} as:

$$W_{i_G^*}^{i_G} = \frac{\frac{Z_i H_{v_{MG}^*}^{v_{MG}}}{Z_G}}{1 + \frac{Z_i H_{v_{MG}^*}^{v_{MG}}}{Z_G}} \quad (5.5)$$

In (5.4) and (5.5), the terms Y_v and Z_i are, respectively, the regulator of the intermediate voltage control loop and the outer grid current control loop. These regulators can be designed on the basis of the open voltage control loop and the open grid current control loop transfer functions.

Note that all transfer functions depend on line impedance Z_G , that can be estimated from the short circuit impedance of MV/LV transformer and distribution line impedance, measured off-line, or measured on-line by using techniques like the one described in [128].

5.2.3 Control Design

On the basis of the previous considerations, it is possible to show that by a design of control parameters and selection of current and voltage references, the UI can provide all the required features. In general, the control of multifunctional grid-tied converters for microgrid applications is a delicate subject. The main aspects to be tackled in the design are steady-state accuracy, large-signal dynamic response, stability robustness, and grid synchronization [10, 11]. Various approaches have been analyzed in the literature to address the various aspects. In [87] it is shown that, for voltage controlled VSI, a PID plus resonant controller provides satisfactory behavior over a wide range of operating modes, while grid current feed-forward and load current feed-forward can degrade stability in particular load conditions. Instead, [115] proposes the analysis and design of synchronous reference frame controllers (SRFC) applied to single-phase VSIs. Though the advantages of this approach are, in general, still not well defined, the paper shows that SRFC, combined with capacitor current active damping, grid voltage feed-forward, and multi-resonant harmonic compensation, can lead to effective solutions. In [84, 90] the H^∞ design approach combined with repetitive controllers is applied for robust control of grid-tied voltage controlled VSIs. As concerns grid synchronization, new PLL-free synchronization strategies

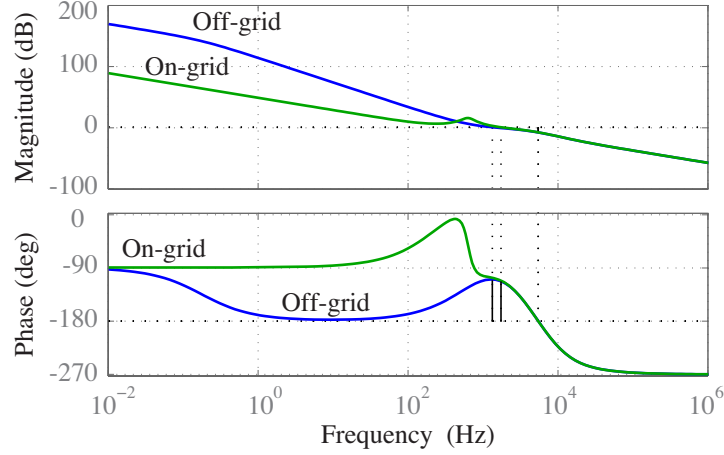


Figure 5-7: Open loop gain of UI voltage control loop.

have been recently proposed and implemented [21, 66]; nevertheless, solutions based on conventional SRF-PLL still attract interest for their flexibility.

All that considered, the devised UI control scheme is shown in Fig. 5-6. The considered implementation took advantage of the fixed frequency digital hysteresis controller outlined in Sec. 6.1 and detailed in [109] for the current loop and a PID regulator for the intermediate voltage loop. Other large bandwidth solutions for the current regulator, like a dead-beat controller, can be equally effective in providing the expected performance. The reference for the voltage loop is obtained from grid voltage reference e_G^* corrected by term Δv_{MG}^* , which is generated by grid current controller Z_i so as to regulate the current absorption at PCC. Controller Z_i is implemented as in Fig. 2-1 [84], and integrates a repetitive filter tuned to grid frequency to minimize the steady-state tracking error.

Finally, a synchronous reference frame phase locked loop (SRF-PLL) is used to estimate the fundamental grid voltage \tilde{E}_G and angular frequency $\tilde{\omega}$ for automatic tuning of the repetitive controller.

For the design of regulators Y_v and Z_i , shown in Fig. 5-6, let's consider the islanded operation with no load. In this situation, assuming that $W_{i_L}^{i_L}$ in the frequency range of interest for the design of voltage regulator Y_v , a suitable PID regulator can easily be devised. Then, its performance should be verified also in the grid-connected case. Fig. 5-7 shows the Bode plots of the open loop gain obtained by a PID regulator with target phase margin, during islanded operation with no load, of 70° and crossover frequency of 1.5 kHz.

At this point it is possible to define the outer current control loop regulator Z_i . To that purpose, let's refer to transfer function:

$$H_{\Delta v_{MG}^*}^{i_G} = \frac{Y_v W_{i_L^*}^{i_L} G_{i_L}^{v_{MG}}}{1 + Y_v W_{i_L^*}^{i_L} G_{i_L}^{v_{MG}}} \cdot \frac{1}{Z_G} = \frac{Y_v W_{i_L^*}^{i_L} G_{i_L}^{i_G}}{1 + Y_v W_{i_L^*}^{i_L} G_{i_L}^{v_{MG}}}. \quad (5.6)$$

To select the regulator, it is firstly convenient to consider the two principal control objectives of the control loop. The main one is to control the power flow at PCC; the second, ancillary, is to compensate the harmonic currents at PCC in the steady-state. These two goals can be accomplished by the use of a repetitive controller tuned to grid frequency. The implementation of the repetitive controller is shown in Fig. 2-1 and has the form described in [84, 193]:

$$R(s) = \frac{1}{1 - G_R(s)e^{-sT_r}}, \quad G_R(s) = \frac{1}{1 + s\tau_p}, \quad (5.7)$$

where G_R is a first order low pass filter that has the effect of limiting the resonances of R at high frequencies, thus preserving the stability of the final system, as mentioned in Sec. 2.2.1. As shown in [84], or by considering the minima of the denominator magnitude, the filter R resonances can be located close to the frequencies:

$$f_{r,k} = \frac{k}{T_r + \tau_p}, \quad k \in \{0, 1, \dots, \infty\}. \quad (5.8)$$

Note that delay T_r can be adjusted to effectively tune the filter resonances to grid frequency. Fig. 5-8 shows the open loop gain of the outer current control loop, where is set to 1 ms. The stability of the system can be verified by inspection of the Bode plot, as in [11].

Effects of Current Controller and Grid Impedance

System stability in islanded operation. The effectiveness of the voltage control loop is crucial while the UI operates islanded from the mains. Therefore, the voltage control loop is here evaluated considering such mode of operation, in the worst loading condition (i.e., no-load). Fig. 5-9 reports the poles and zeros of $H_{v_{MG}^*}^{v_{MG}}$ in (5.4) assuming a low-pass filter behavior for $W_{i_L^*}^{i_L}$. The poles and zeros are plotted for different values of static gain and cut-off frequency. The static gain assumes values from 0.5 to 1.5 with steps of 0.1, while

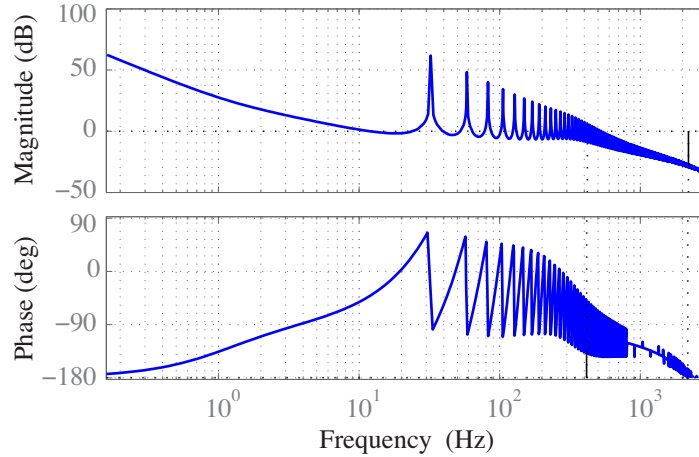


Figure 5-8: Open loop gain of the compensated UI outer current control loop.

the cut-off frequency assumes values 1 kHz, 2 kHz, and 4 kHz. It is possible to observe that the static gain of $W_{i_L}^{i_L}$ affects the damping of the system, whereas that slower current controllers dynamics affect both damping and decay ratio. Noticeably, there are no poles at the right-half plane.

System stability in grid-connected operation. To analyze the external grid current control loop, the poles and zeros of (5.5), varying L_G from 0.2 mH to 2 mH with steps of 0.2 mH and R_G from 0.1 Ω to 1 Ω with steps of 0.1 Ω , are shown in Fig. 5-10. A zoomed-in view of Fig. 5-10 is provided in Fig. 5-11. No poles at the right-half plane are present for the considered range of values.

5.2.4 Islanding Detection

Islanded operation occurs when the microgrid is energized solely by one or more local sources while it is electrically separated from the main grid. Referring to Fig. 5-5(a), this means that circuit breaker CB_1 (externally driven) or CB_2 (UI driven) are open. The UI drives CB_2 to open when an *islanded* condition is detected, notably, when CB_1 is opened or the voltage quality at PCC transcends allowable limits (*grid absent* condition). In any case, at the transition to islanded operation, the UI automatically becomes the grid-forming device for the islanded system, having to autonomously and timely adapt its voltage reference to guarantee a seamless operation. To this end, effective islanding detection and

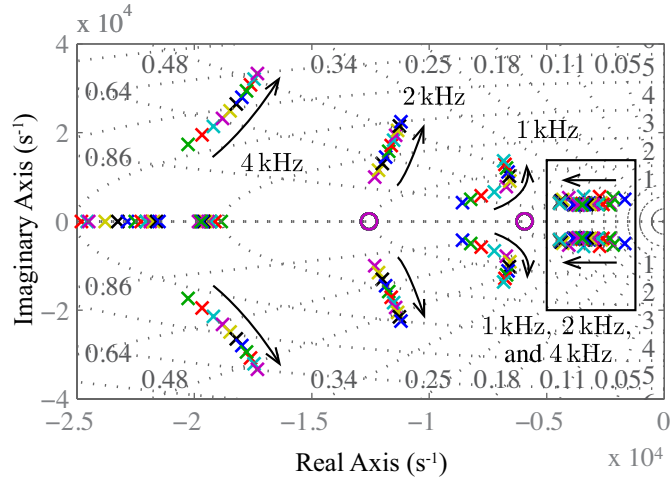


Figure 5-9: Poles (\times) and zeros (\circ) of $H_{v_{MG}^*}^{v_{MG}}$ with different static gains and dynamics for $W_{i_L^*}^{i_L}$.

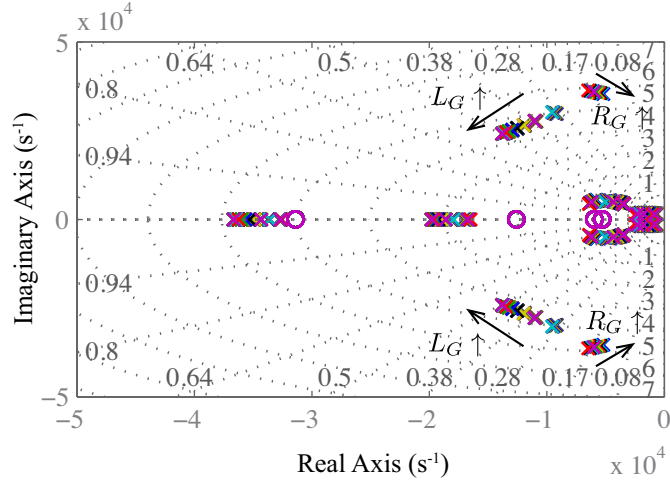


Figure 5-10: Poles (\times) and zeros (\circ) of $W_{i_G^*}^{i_G}$ for different values of L_G and R_G .

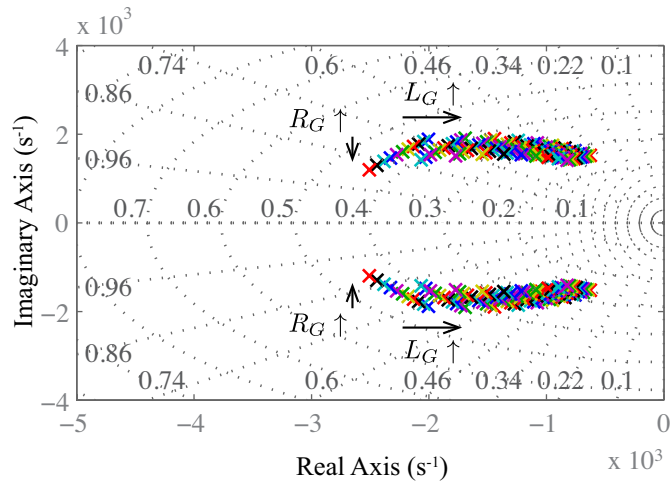


Figure 5-11: Zoom-in view of resonant poles (\times) and zeros (\circ) of Fig. 5-10.

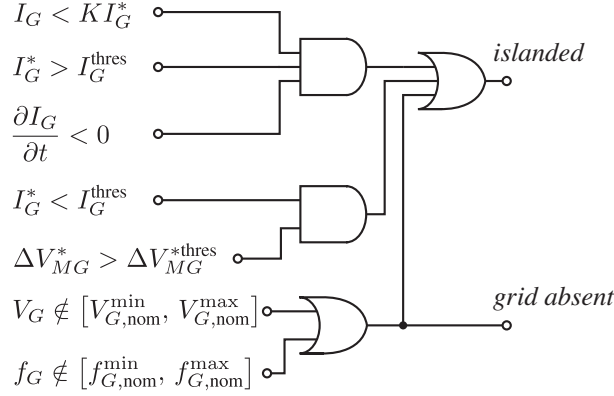


Figure 5-12: Islanding detection scheme.

synchronization techniques are necessary.

Islanding Detection

The islanded detection technique here adopted is represented in Fig. 5-12. To describe its operation principle, let's assume to operate in steady-state before transition, that is, by indicating with capital letters the rms values of considered quantities, $I_G \simeq I_G^*$ owing to the resonant properties of Z_i . By denoting with I_G^* a threshold for rms value of currents that is small as compared to the nominal grid current, two cases of operation can be distinguished:

- $I_G^* > I_G^{\text{thres}}$: in this case the transition to islanded operation is characterized by the reduction of measured value of grid current I_G with respect to reference value I_G^* . Under these conditions, the islanded operation is triggered when the current error becomes significant, namely, when $I_G^* - I_G > I_G^{\text{thres}}$ while $\partial I_G / \partial t < 0 < \partial I_G^* / \partial t$.
- $I_G^* < I_G^{\text{thres}}$: in this case the transition to islanded operation, though having little effect on the measured I_G , opens the grid current control loop, thus leading regulator Z_i to deviate from the ideal equilibrium point $(i_G^*, i_G, \Delta v_{MG}^*) = \mathbf{0}$ due to the noise and non-idealities present in the real application. Then, under these conditions the *islanded* operation is triggered when the voltage correction term ΔV_{MG}^* becomes significant, namely, when $\Delta V_{MG}^* > \Delta V_{MG}^{*\text{thres}}$.

The distinction made above allows a prompt islanding detection if islanding occurs while the microgrid is exchanging power with the mains, and a method that is resilient to

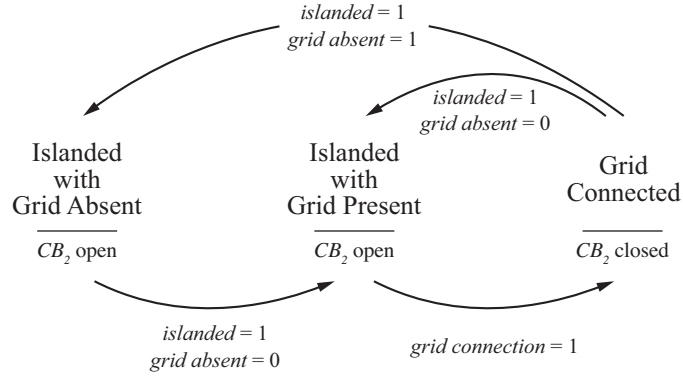


Figure 5-13: Microgrid's possible operating modes and transitions.

external noise if the islanding event occurs while there is a negligible current exchange at the PCC.

Finally, the *grid absent* condition can easily be detected by verifying whether the measured grid voltage satisfies the allowed limits in terms of both amplitude and frequency.

The possible operating modes and transitions, along with the corresponding state of circuit breaker CB_2 , driven by the UI, are synthetically represented in Fig. 5-13.

Grid Synchronization

Fig. 5-14 shows how grid current reference i_G^* and grid voltage reference E_G^* are determined. If grid voltage is present and can be measured (i.e., *grid absent* signal of Fig. 5-12 is not asserted), phase voltage reference E_G^* is set as a positive-sequence sinusoid with frequency $\tilde{\omega}$ and amplitude \tilde{E}_G . Instead, if grid voltage is not present (i.e., *grid absent* signal of Fig. 5-12 is asserted), E_G^* is set as positive-sequence sinusoid at nominal frequency ω_{nom}^* and nominal amplitude E_{nom}^* . As concerns current reference i_G^* , in grid-connected operation it is determined according to the desired active and reactive power absorption from the grid (p_G, q_G), while in islanded operation it is set to zero. For what concerns the transitions of amplitude and frequency parameters, these are performed gradually by employing slew rate limiting blocks. Finally we notice that PLL frequency is bounded around the nominal grid frequency within values $\omega_{nom} \pm \Delta\omega_{nom}$. The width of the band is dynamically changed during operating mode transitions, in particular, the band is gradually reduced to zero in the transition to the *islanded* operation with *grid absent*, thus making the islanded micro-

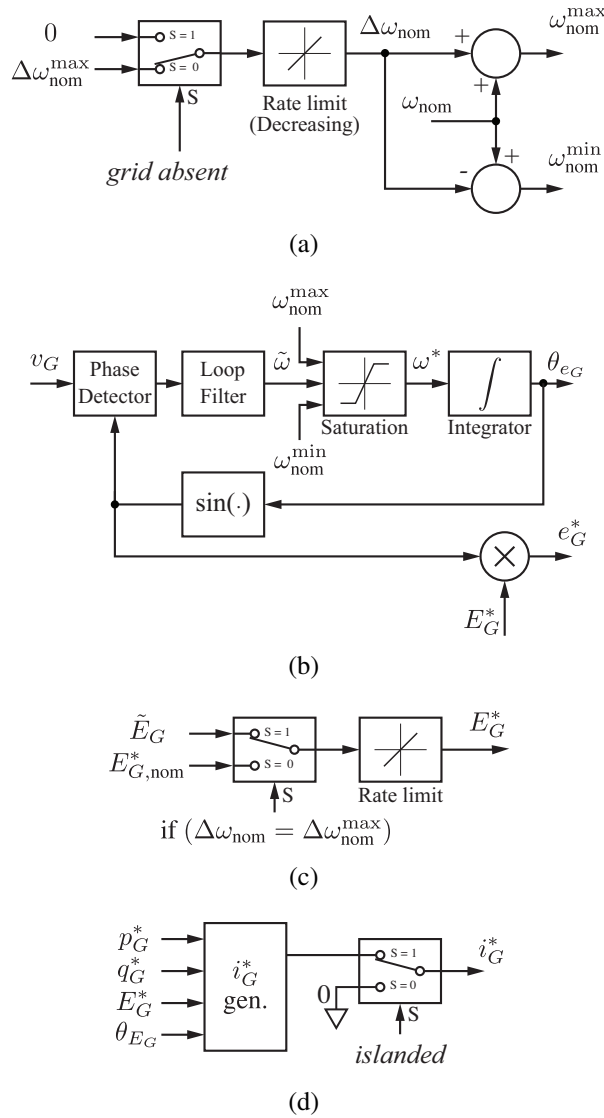


Figure 5-14: UI voltage reference generator (per phase).

grid to operate at nominal voltage and frequency, and reinitiated to the maximum allowed frequency variation when the voltage of the main grid is restored.

5.2.5 Case Study

The proposed UI control scheme has been tested in different operating conditions, both static and dynamic, in grid connected and islanded mode, by employing, in particular, real-time simulations and a laboratory-scale prototype.

This section deals with a fundamental application example, displayed in Fig. 5-15, that

Table 5.1: Test circuit parameters

| Parameter | Symbol | Value |
|-------------------------|-------------|-------------------|
| Grid inductance | L_G | 0.65 mH |
| Grid resistance | R_G | 0.91 Ω |
| LC filter inductance | L | 1.2 mH |
| LC filter capacitance | C | 100 μF |
| UI power rating | A_{UI} | 3.0 VA |
| Nominal grid voltage | E_G | 230 V |
| Nominal grid frequency | f_{rated} | 50 Hz |
| Nominal load power | P_{LOAD} | 2 kW |

allows to show the main features of the proposed control scheme. The test circuit includes the UI and a non-linear load connected to a low-voltage, single-phase distribution system. A commercial PV inverter compliant to all applicable regulations in EU is included in the setup to show transitions among grid connected and islanded operating modes.

Besides the inner current and voltage regulators (Sec. 5.2.3), the grid current regulator (Sec. 5.2.3), and the islanded connection block (Sec. 5.2.4) discussed above, the final setup of Fig. 5-15 employs also a *grid connection block*. This block aims at preventing high inrush currents at the connection of the islanded system to the main grid and at guaranteeing a non-saturated operation of Z_i . Indeed, while Z_i should be active at the connection with the mains to keep control on grid current i_G , the actual status of the grid depends on the response delay of electromechanical circuit breaker CB_2 (typically ranging from tens to thousands of milliseconds), that is, in general, not known. During this time interval the regulator Z_i operates in open loop: it reacts to spurious error signals introduced by the current sensor, which may cause saturation. To alleviate these problems the connection block ignores the current error ϵ_{i_G} below a suitable threshold, which is removed once the response time of CB_1 is, confidently, elapsed. This allows both to limit inrush currents exceeding the deadband and to prevent spurious signals to perturb the regulator while CB_2 has not yet finalized the committed reclosure.

The supply reference i_G^* is set to be proportional to v_G and to draw the full load power from the utility. The setup parameters are detailed in Table 5.1.

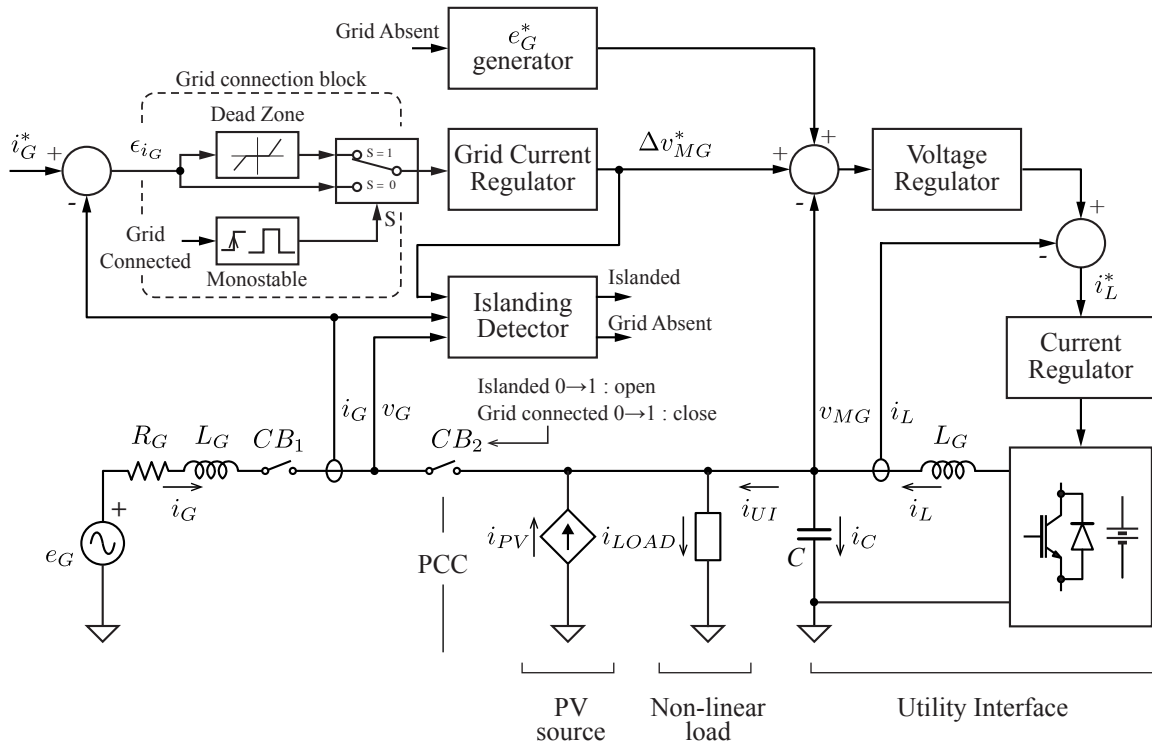


Figure 5-15: Schematic representation of control part (top) and power system part (bottom) of the considered case study. The control part, from left to right, includes: the grid connection block, the grid voltage reference (e_G^*) generator of Fig. 5-14, the islanding detection block of Fig. 5-12, and the regulators discussed in Sec. 5.2.3. The power system setup includes: the externally driven mechanical circuit breaker CB_1 , the distribution line Z_G of length 130 m, the UI-driven electromechanical circuit breaker CB_2 , the commercial PV inverter connected to a string of PV panels, the distorting non-linear load, and the UI hardware.

Real-Time Simulation Results

The results reported in the following paragraphs have been obtained with the real-time simulation setup displayed in Fig. 5-16. The average model of the plant in Fig. 5-15 along with the control algorithms discussed in Sec. 5.2.3 and in Sec. 5.2.4 have been implemented in Matlab/Simulink and then compiled into a dynamic-link library (DLL). Then, a real-time simulation platform, namely, a NI-PXI, has been configured and programmed to execute the compiled model with a time step equal to $t_{STEP} = 40 \mu\text{s}$. Moreover, to consider a realistic grid voltage behavior—which is a critical aspect to UI control validation—the instantaneous grid voltage used in the simulation is that measured in the real distribution line, thus carrying realistic features of typical low-voltage grid nodes. This measure is performed by the device labeled “grid voltage emulator” in Fig. 5-16. The grid voltage emulator and the real-time simulator are connected to an I/O interconnection fixture, that allows all relevant signals to be acquired. The simulation results are made available, synchronously with the wall-clock, by FPGA-based programmable I/O interfaces on board of the real-time simulator.

The system response has been tested under the following sequence of events.

Connection of non-linear load. Fig. 5-17 shows the system response to the connection of a non-linear load constituted of a full-bridge diode rectifier with 25Ω resistive load and $500 \mu\text{F}$ DC filter capacitor. It generates the typical distortion shown by trace i_{LOAD} . Thanks to the effective current regulation accomplished by the outer regulation loop, the current i_G drawn at PCC is purely active and nearly distortion-free in the steady-state. Notably, load current harmonics are supplied by UI, as clearly shown by trace i_{UI} .

Grid voltage perturbation. In low-voltage distribution grids with high penetration of renewable sources, step voltage variations may occur due to the intermittent nature of wind and PV generation. The system response to a 5% voltage step-up at PCC above the nominal value is now considered. Fig. 5-18 shows the acquired quantities. While the load current i_{LOAD} remains substantially unchanged, the UI adapts promptly its current i_{UI} to the voltage step, so that the measured grid current i_G returns to be purely active in less than one

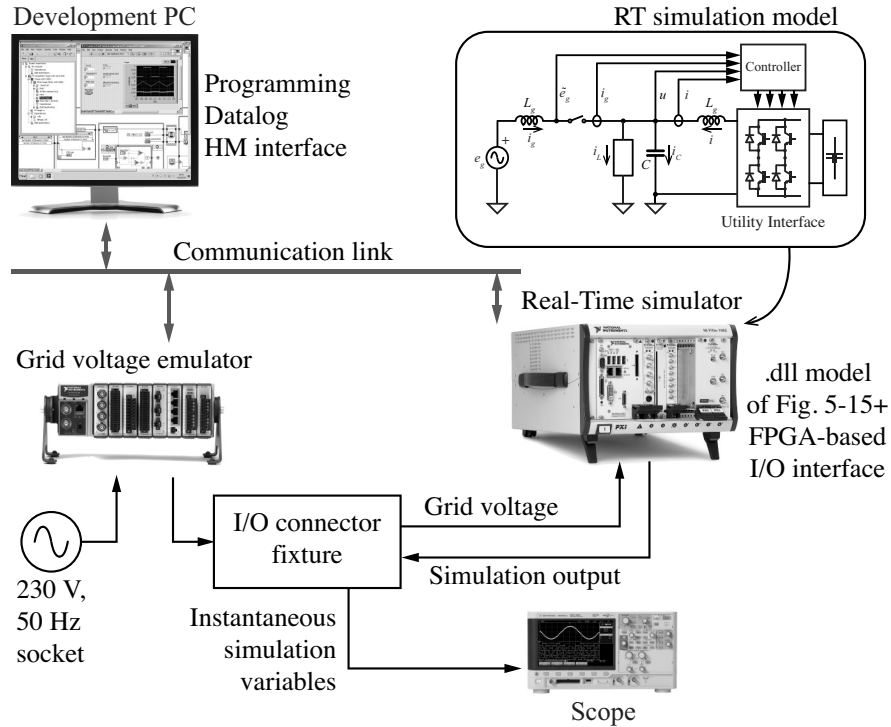


Figure 5-16: Real-Time (RT) simulation testbed of the UI.

grid cycle.

Transition to islanded operation. Fig. 5-19 displays the behavior of the system around an intentional islanding transition. In the considered case the grid voltage is always within nominal values, thus the voltage magnitude and frequency selectors of Fig. 5-14 are maintained in the grid present condition, keeping the synchronization of the UI with the grid voltage. At the transition, the PCC current reference selector is switched to the islanded condition to impose a consistent zero current reference for i_G . In particular, Fig. 5-19 shows load current i_{LOAD} , UI current i_{UI} , grid current i_G , and UI voltage v_{UI} . Before the transition, the steady-state behavior of voltages and currents that is established when the non-linear load is connected and the system is grid connected are displayed. In particular, the shape of UI voltage is defined by the voltage imposed by the mains, the current drawn from the PCC is nearly sinusoidal, and the load harmonic currents are provided by the UI. When the transition occurs, the grid current vanishes and the UI voltage control loop promptly intervenes to maintain the local grid voltage, and the whole load power is natu-

rally fed by the UI. This leads to a seamless transition between the two operating modes, as can be clearly noticed in the figure.

Transition to grid-connected operation. Before the transition, the voltage and frequency selectors of Fig. 5-14 are set to the grid present condition and UI synchronizes its voltage with the mains. At the transition, the current reference selector of Fig. 5-14 switches to the state that corresponds to the islanded condition, thus feeding the proper current reference i_G^* to UI. Fig. 5-20 displays the system transition from islanded to the grid connected operation. In particular, Fig. 5-20 shows load current i_{LOAD} , UI current i_{UI} , grid current i_G , and UI voltage v_{UI} . Before the transition we observe the steady-state behavior of voltages and currents when $i_G^* = 0$. The load voltage equals the fundamental of the mains' voltage, the current at PCC is zero, and the load is fully fed by UI. When the transition occurs, the outer current control loop of the UI intervenes and the grid current progressively becomes purely active, so as to comply with load power absorption. In fact, the line current shows small oscillations immediately after connecting to the mains, however they vanish within few line cycles as the repetitive controller settles to the new situation. Correspondingly, the UI progressively reduces the active current fed to the load, and eventually provides just the current harmonics.

System's behavior along the sequence of events. Fig. 5-21 summarizes the grid behavior corresponding to the sequential application of the four dynamic events described above. Initially the system operates grid connected and the non-linear load is disconnected. Reference i_G^* keeps zero, since there is no power absorption. The UI operates as a grid-supporting unit, impressing at its output terminals a replica of the distorted voltage fed by the utility at PCC (THD of voltages are shown in Fig. 5-22). In this condition, current i_G should vanish. Its actual behavior, shown by the magenta trace in Fig. 5-22, is indeed very close to zero, with a small error due to the limited bandwidth of the outer current control loop. The non-linear load is switched on at time $t = 1$ s. After that, the load current absorption is shared between the grid and UI. Since the voltage loop ensures small output impedance for voltage source UI, the load current is initially delivered by the UI, as shown in Fig. 5-17. A

steady-state condition is then reached, when the grid provides the load active current and the UI feeds load current harmonics only. Note that, despite the highly distorted load current, thanks to UI control, the purity of supply current i_G keeps good (THD equal to 3.2%). At instant $t = 6$ s the circuit breaker CB_1 at PCC is switched off, and the system turns to islanded operation. UI becomes the grid-forming voltage source and autonomously manages the load power needs, whose details are shown in Fig. 5-19. During islanded operation, corrective term Δv_{MG}^* vanishes and UI tracks the nominal voltage reference. Finally, at instant $t = 8$ s circuit breaker CB_1 is switched on again, and the system returns to initial condition.

The system response to the above dynamic events confirms the correctness of the chosen control structure, algorithms, and parameters.

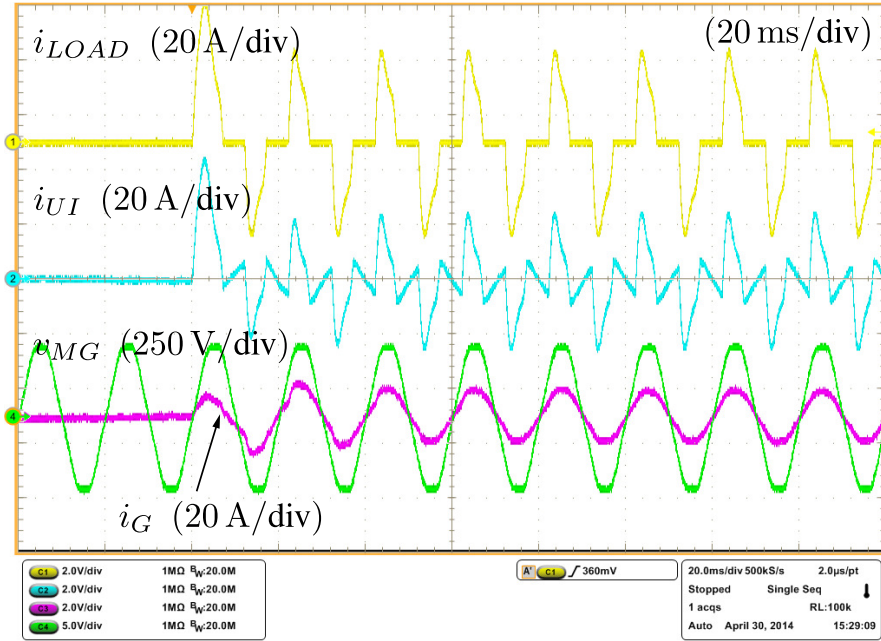


Figure 5-17: Connection of non-linear load.

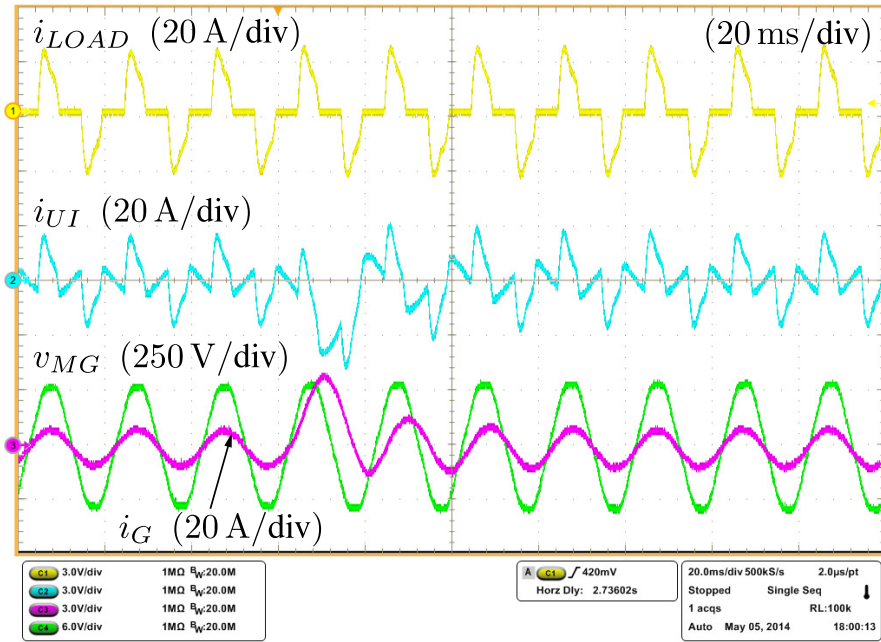


Figure 5-18: Response to 5% variation of grid voltage

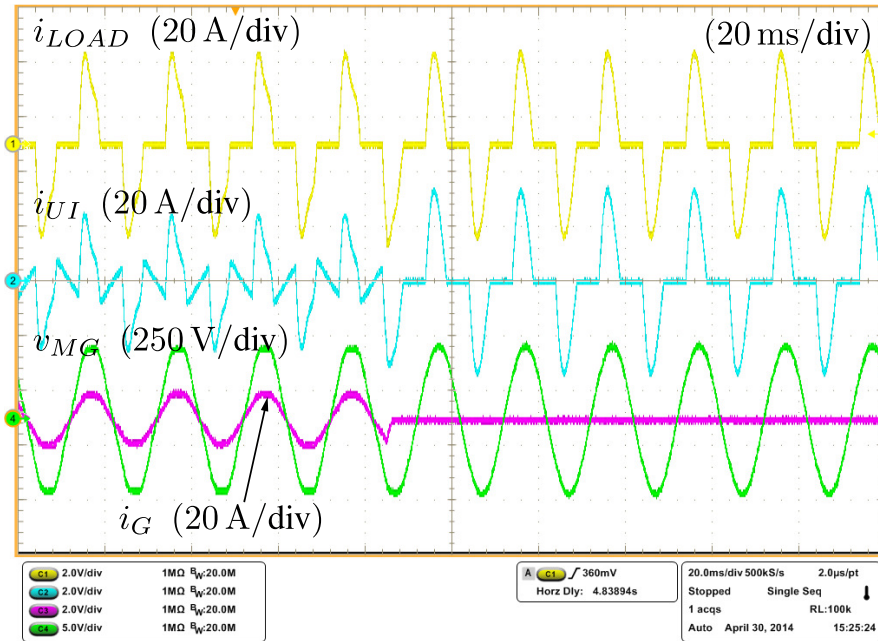


Figure 5-19: Transition to islanded operation.

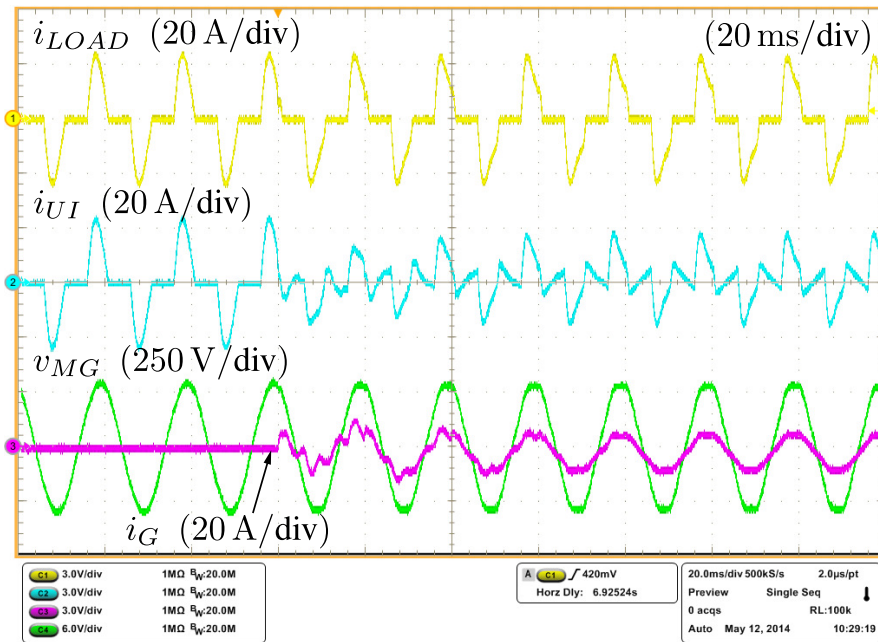


Figure 5-20: Transition to grid connected operation.

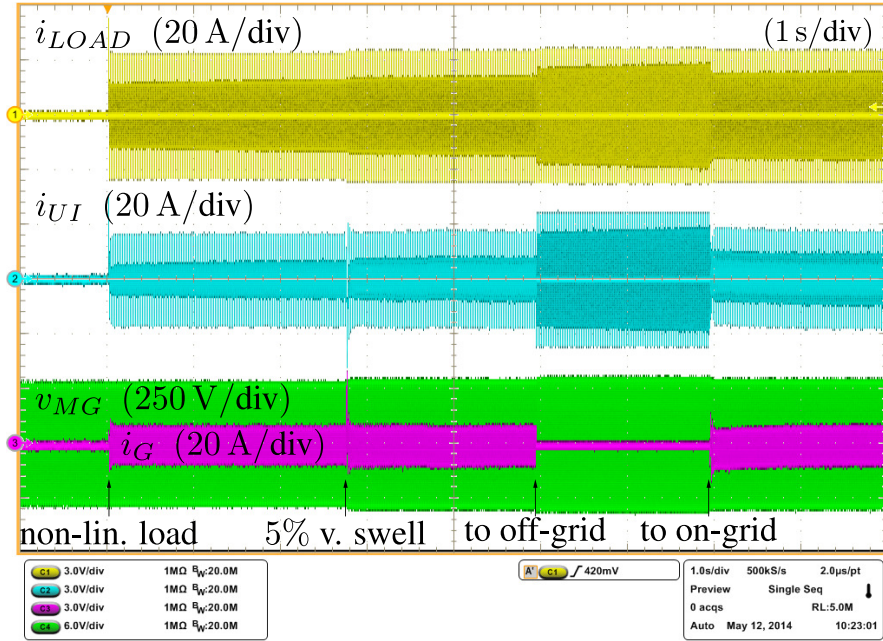


Figure 5-21: System behavior along the entire sequence of events.

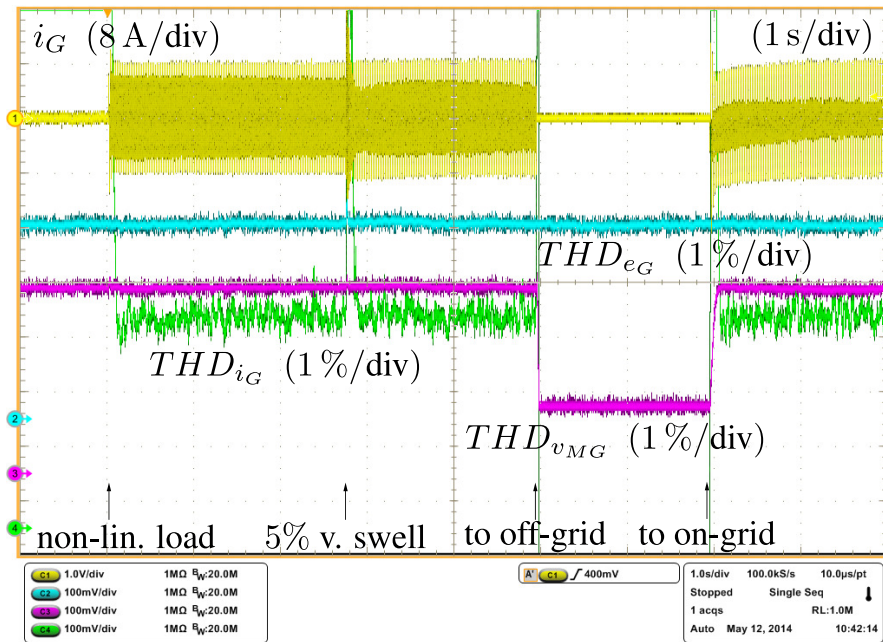


Figure 5-22: Measured THD along the entire sequence of events.

Experimental Results

An experimental realization of the case study displayed in Fig. 5-15 has been developed to verify the actual behavior of the final system. This paragraph reports the acquired results; in particular, circuit operation has been investigated in the following operating conditions.

Islanded operation. A programmable electronic load absorbing 2.0 kW with crest factor $CF = 2$ is connected to the setup. Fig. 5-23 shows grid voltage e_G , UI voltage v_{MG} , and the current absorbed by the local load i_{LOAD} in steady-state conditions. We notice that the UI manages to feed the local load with an adequate voltage quality v_{UI} ($THD_{v_{MG}} = 2.6\%$) and to synchronize with the grid voltage for a smooth and prompt transition to grid connected operation.

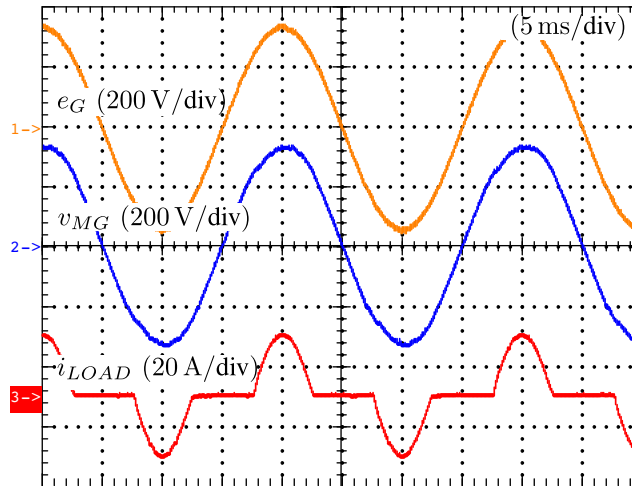


Figure 5-23: Islanded operation with non-linear load.

Grid connected operation. Fig. 5-24 shows system response at the connection of a non-linear load during grid connected operation with zero grid reference current. In these conditions, an ideal operation would require a constant zero current flow at PCC. Due to the finite response time of grid current regulator Z_i , the behavior shows a small transient of grid current i_G following the connection. The steady-state behavior reached during grid connected operation while the current reference I_G^* is equal to $7.5 A_{rms}$ is shown in Fig. 5-25. Acquired waveforms of main grid voltage e_G , UI voltage v_{MG} , current exchanged with

the main grid i_G , and current i_{UI} provided by the UI are reported. A good correspondence can be noticed with real-time simulation results (see Fig. 5-17). The same measurement is performed also with 5% of third harmonic present in grid voltage v_G . As expected in this situation, the grid current is correspondingly distorted due to the proportional relation between grid voltage and grid current. The acquired results are reported in Fig. 5-26, while the steady-state amplitudes and total harmonic distortion levels are reported in Table 5.2.

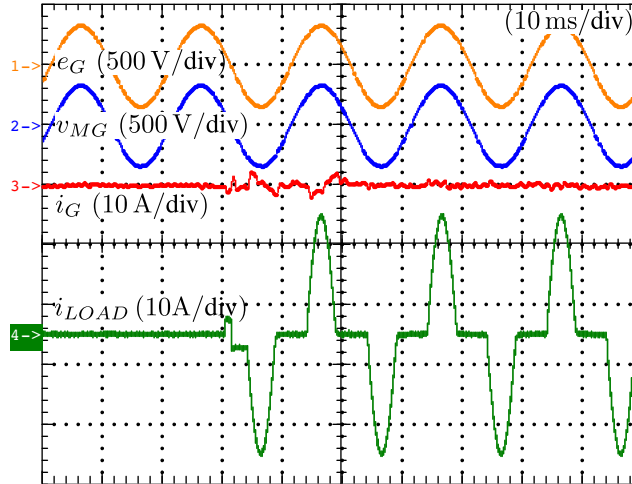


Figure 5-24: Connection of non-linear load during grid connected operation.

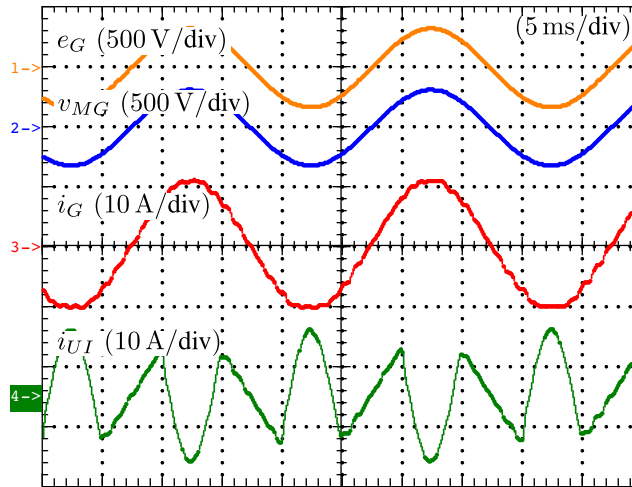


Figure 5-25: Grid connected operation with non-linear load; grid voltage THD: 0.25%.

Transition from islanded to grid connected operation. Fig. 5-27 displays the long term behavior during a transition to grid connected operation. In particular, grid voltage e_G , UI

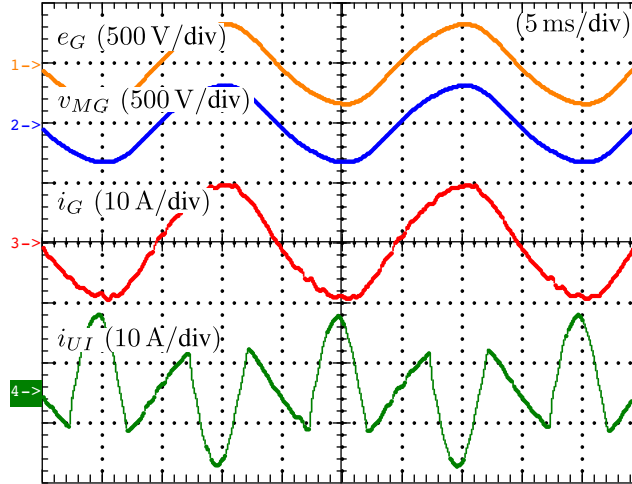


Figure 5-26: Grid connected operation with non-linear load; grid voltage with 5% of 3-th harmonic.

Table 5.2: Distortion measurements in steady-state from the prototype of Fig. 5-15⁽¹⁾

| | $v_G^{\text{rms}} /$ THD_{v_G} | $i_G^{\text{rms}} /$ THD_{i_G} | $v_{UI}^{\text{rms}} /$ $THD_{v_{UI}}$ | $i_{UI}^{\text{rms}} /$ $THD_{i_{UI}}$ | $i_{LOAD}^{\text{rms}} /$ $THD_{i_{LOAD}}$ |
|---|-------------------------------------|-------------------------------------|---|---|---|
| Islanded, no load | 237/0.5 | 0/— | 237/0.2 | 0/— | 0/— |
| Islanded + load | 237/0.5 | 0/— | 236/2.6 | 10.2/61.9 | 10.2/61.9 |
| Grid conn. no load | 244/0.5 | 10.3/1.8 | 258/0.4 | 10.3/1.8 | 0/— |
| Grid conn. + load ⁽²⁾ | 232/0.6 | 7.5/2.8 | 223/0.7 | 4.45/360 | 10.2/61.9 |
| Grid conn. + load ⁽²⁾ + 5 % of 3-rd harm. | 233/4.6 | 6.7/7 | 224/4.5 | 3.85/230 | 10.2/61.9 |

⁽¹⁾ Voltages are measured in volts, currents in amperes, relative quantities in percentage units.

⁽²⁾ Programmable electronic load absorbing 2 kW of active power with crest factor of 2.

voltage v_{MG} , UI current i_{UI} , and grid current i_G are shown along the main phases of the connection process. First, it is possible to remark the absence of any inrush current across the connection instant, thanks to the adopted deadband-based connection technique; secondly, that the voltage provided by the UI is well synchronized with grid voltage, thus v_{MG} maintains smooth and with desired amplitude around the transition. The grid connection process completes when the deadband period is elapsed. Finally, the amplitude of i_G^* is changed progressively with a suitable slew-rate. A zoomed-in view around the connection

instant is reported in Fig. 5-28. In the considered case, deadband duration is set equal to 1 s, though shortest values may be chosen.

Transition from grid connected to islanded operation. In this case, a commercial, fully compliant, PV inverter is connected to the system to verify that the management strategy of the UI succeeds in ensuring a seamless operation of small photovoltaic systems also under intentional and non-intentional islanding transitions. In Fig. 5-31, the PV source

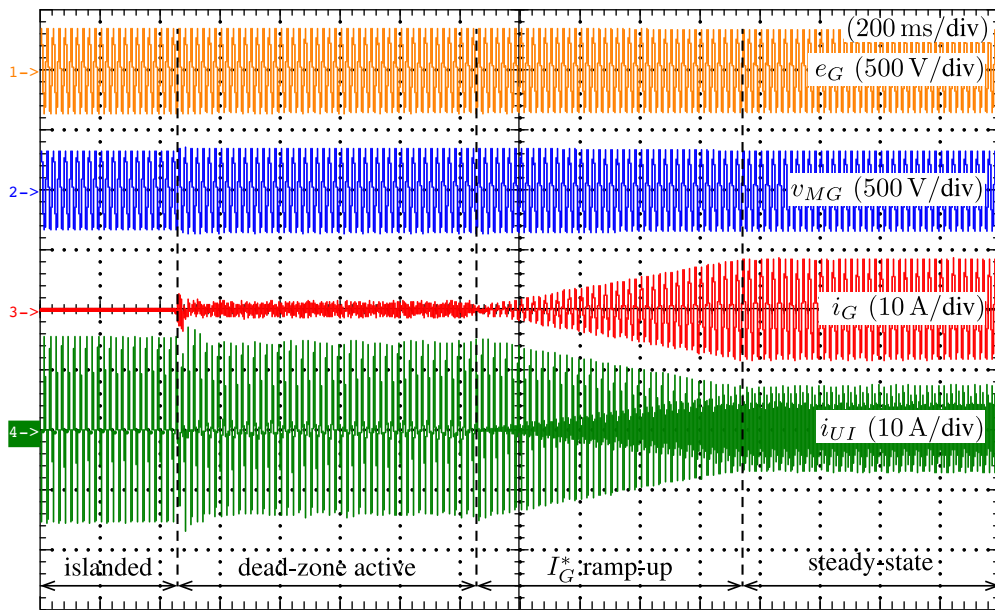


Figure 5-27: Transition from islanded to grid connected operation.

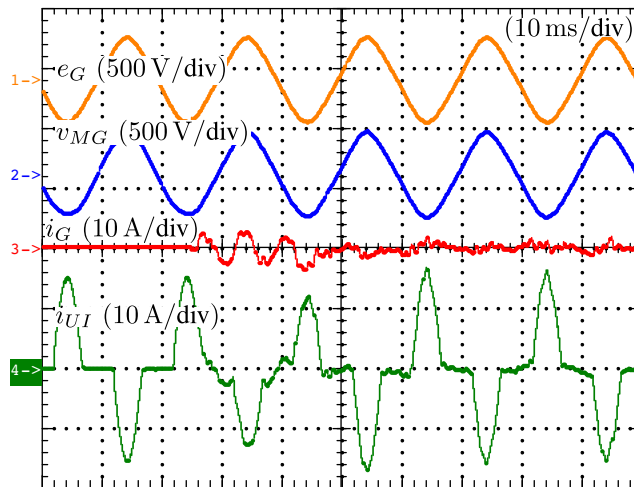


Figure 5-28: Zoomed-in view around the connection displayed in Fig. 5-27.

extracts approximately 0.4 kW from an array of photovoltaic panels and a programmable electronic load absorbs 1 kW with crest factor equal to 2. In this situation it is assumed that the UI undertakes an intentional islanding. The intentional islanding procedure commands the circuit breaker CB_2 to open and, simultaneously, sets the grid current reference to zero and activates the deadband control. After the circuit breaker CB_2 opens, the grid current controllers are reset to their initial condition till the arrival of a grid connection command. As can be observed in Fig. 5-31, the intentional islanding happens seamlessly: the voltage provided by the UI adapts smoothly, so that the PV does not notice the transition, maintaining an unperturbed operation along the event. Let's consider now the transition to islanded operation due to unpredictable events, namely, the non-intentional islanding. In this case, the local non-linear load absorbs 2 kW with current factor equal to 2, and the power injection from the PV inverter is nearly equal to 0.8 kW. Then, the circuit breaker CB_1 is opened and the microgrid loses the utility grid, undergoing a non-intentional islanding. In this condition, the UI automatically becomes the grid-forming device of the islanded microgrid, providing an adequate grid voltage for the islanded system. The acquired waveforms are reported in Fig. 5-29. The magnitude and frequency of voltage v_{MG} across the transition are reported in Fig. 5-30. Also in this case, it is possible to observe a seamless transition to islanded operation, which occurs unnoticed by the PV inverter.

An intentional transition to the islanded operation due to a detected anomalous voltage condition is reported in Fig. 5-31. Here, the grid voltage is made to steadily increase. When v_G exceeds the imposed voltage limit (equal to $245 V_{rms}$) the MC reacts by performing an intentional islanding transition with grid absent (see Fig. 5-12, Fig. 5-14, and Fig. 5-15). Therefore, the MC sets the grid power reference (p_G) to zero and bounds the PLL frequency around its nominal value (as per Fig. 5-14) before opening CB_2 ; thereupon the microgrid voltage returns to its nominal value, as shown in Fig. 5-32 because the reference E^* is set equal to the positive-sequence of a PCC voltage with nominal frequency ω and amplitude E .

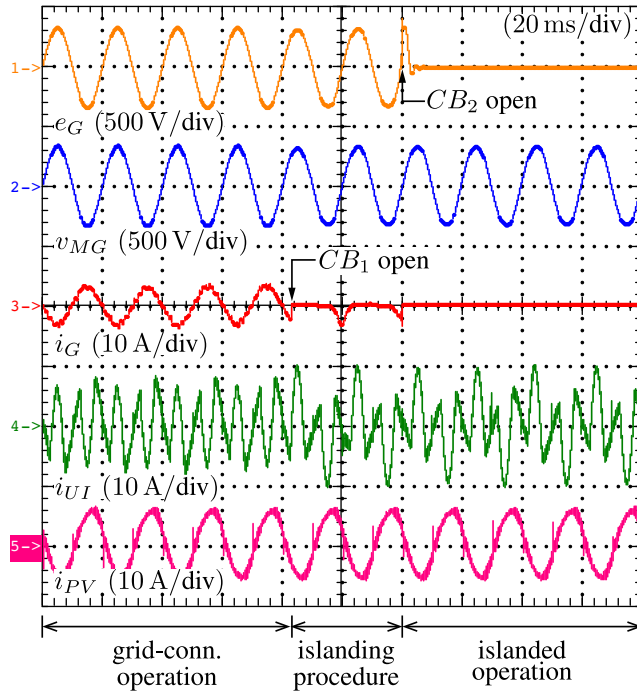


Figure 5-29: Non-intentional transition to islanded operation.

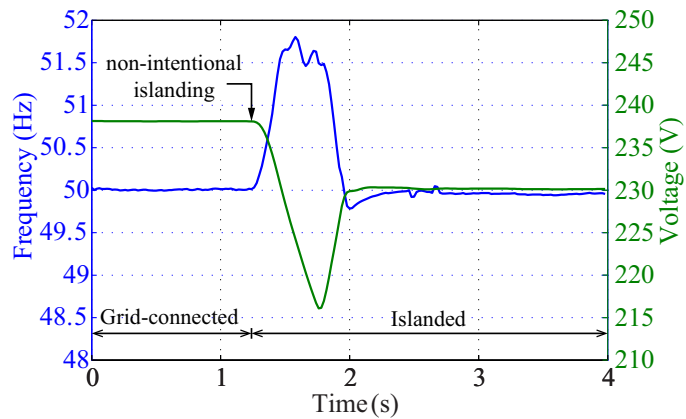


Figure 5-30: Amplitude and frequency of v_{MG} across the non-intentional transition shown in Fig. 5-29.

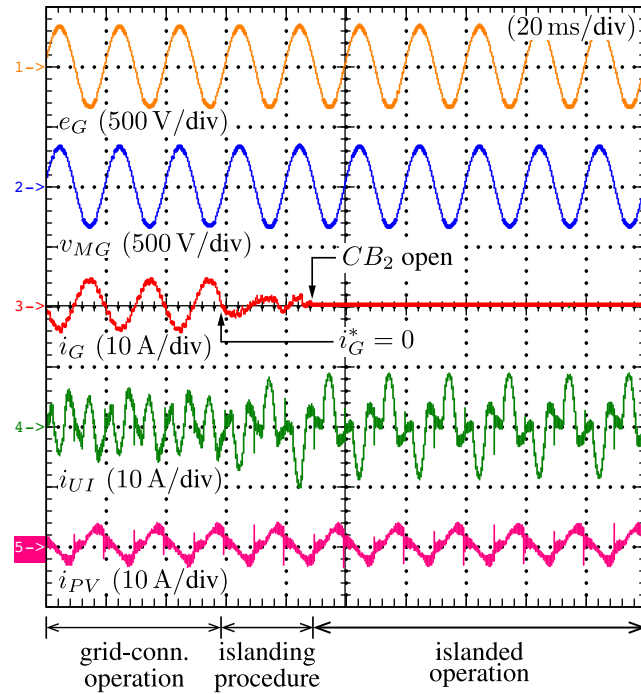


Figure 5-31: Intentional transition to islanded operation due to voltage out of range.

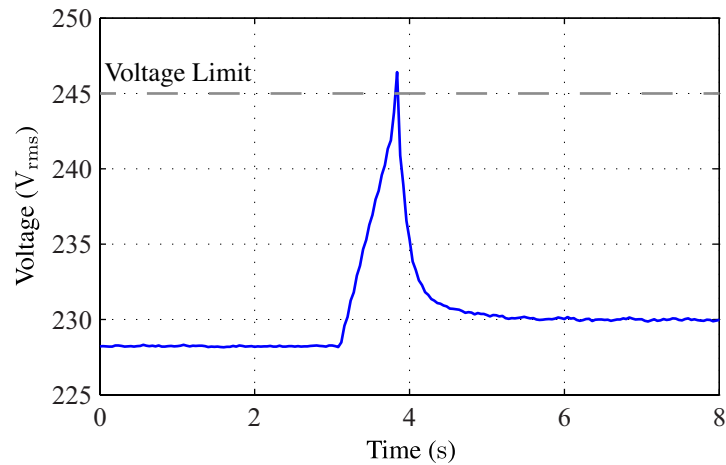


Figure 5-32: Amplitude of v_{MG} across an intentional islanding transition due to voltage out of range.

5.3 Summary

This chapter presents a master/slave architecture to coordinate the distributed energy resources in smart microgrids. The main elements of the architecture (namely, a *utility interface*—embedding the microgrid master controller—and the *energy gateways*) are introduced and a general control framework presented. A narrowband communication system is employed to the purpose of coordinating the constituting devices. By means of the UI and the EGs the architecture allows to decouple the needs for ensuring a high quality of the voltage provided to microgrid's loads, which is demanded to the UI, and the needs for attaining a synergistic operation of distributed energy resources, which is demanded to the EGs. The utility interface is considered in detail in the second part of the chapter, also proposing a possible implementation. Notably, with the UI, the proposed microgrid architecture can operate in both grid connected and islanded conditions, and seamlessly transit between the two operating modes.

Chapter 6

Controllers for Distributed Energy

Resources

The previous chapter introduces a particular kind of voltage-driven converter, called utility interface converter (see, specifically, Sec. 5.2), to interface a cluster of DERs to the main grid. In order to make a utility interface converter to perform as a voltage source with low output impedance a voltage control loop is needed, which can take advantage of a *high performance, inner current control loop*. A prompt current control can improve the dynamic response in sustaining fast load transients and compensating harmonic currents and, in addition, protects the converter from dangerous overload conditions. Beside that, wide bandwidth current control loops represent the backbone of a large variety of switching converter applications. According to grid connection standards, the currents generated by grid-tied converters, such as the EPPs of energy gateways, should follow given references with high accuracy and without being affected by voltage disturbances or uncertainties in the grid model, as remarked in Sec. 2.2.

This chapter focuses on the fundamental inner control loop for grid-tied inverters. Specifically, a couple of innovative current controllers [194, 195] are described in Sec. 6.1 and Sec. 6.2. The former is a fully digital, fixed frequency hysteresis current controller, integrating an algorithm that can attain the regulation of the switching frequency with a granularity of one half of a switching period. The latter is an oversampled dead-beat current controller with a regulation delay of one half of a modulation period and a large-signal

response improvement.

To the purpose of showing the advantages brought by the proposed controllers, the performances of the controllers measured on a laboratory prototype are reported in Sec. 6.3. In order to provide a benchmark, the results obtained from a conventional, oversampled proportional integral (PI) controller are included.

Reference Application Case. In this chapter, a single-phase, full bridge inverter is considered as the application case of reference. The converter's structure is schematically illustrated in Fig. 6-1, the converter's parameters are listed in Table 6.1. It is assumed that the switches are controlled so as to impose either $+V_{DC}$ or $-V_{DC}$ voltage at the converter's output (i.e., no three level modulation is considered). In addition, to the purpose of comparing the different solutions, a *common* control system and current sensing circuit are used. Details on this circuit are reported in Appendix A.

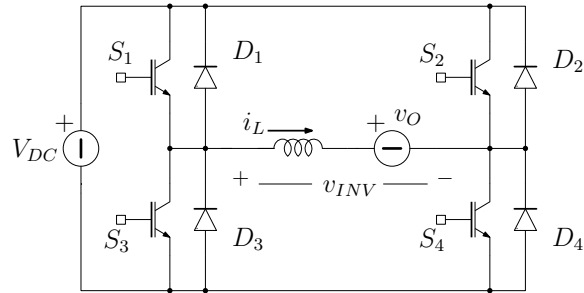


Figure 6-1: Simplified schematic of the considered full bridge inverter test bench.

Table 6.1: Converter parameters

| Parameter | Symbol | Value |
|----------------------------|-------------|----------------------|
| DC-link voltage | V_{DC} | 400 V |
| Switching frequency | f_{sw} | 20 kHz |
| Dead-time | T_D | 400 ns |
| Filter inductance | L | 1.2 mH |
| Series inductor resistance | ESR_L | 50 m Ω |
| Nominal power | S_o | 3 kVA |
| Nominal RMS output voltage | v_O^{rms} | 230 V _{rms} |
| Nominal output frequency | f_{vO} | 50 Hz |

6.1 Hysteresis Current Controller

The hysteresis current controller is the one that found the widest application thanks to its excellent dynamic characteristics. Its small- and large- signal responses are practically ideal, which guarantees minimum phase lag and residual reference tracking error. In current mode controlled DC-AC converters, the wide bandwidth current regulation is particularly effective in grid-tied, drive, and active filter applications. Even when the ultimate objective of the control system is to regulate a converter's output voltage, a fast inner current control loop is highly desirable, for protection purposes and/or to allow current limitation during large voltage reference or load transients.

On the other hand, the hysteresis controller operation always results in variable switching frequency, unless the voltage conversion ratio (or the inverter modulation index) and the current reference are both constant, which is seldom the case, at least in DC-AC converter applications.

Constant or limited switching frequency solutions, like those proposed in [111, 112, 196–198], are often sensitive to variations of system parameters (e.g., DC-link voltage, inductance value), to dead-times, and sampling delays. These factors, altogether, limit the practical effectiveness of the frequency regulation. Besides, these solutions employ additional analog hardware, which makes them relatively complex and sensitive to offsets, drifts, tolerances, and aging effects. For instance, operational amplifiers are needed in [199], whereas low latency comparators and/or digital to analog converters (DACs) are used in [196, 197] and [109, 111, 200–204]. Likewise, frequency-to-voltage converters are adopted in [205, 206]. Monolithic, highly effective implementations have also been proposed [207], which, however, offer no flexibility, being tailored to very specific applications.

In this section, an innovative digital current controller is presented that operates as a *virtual* analog hysteresis current controller, taking advantage of a high performance analog to digital converter (ADC) and of a field programmable gate array (FPGA) circuit implementation. It is designed as a non-linear current error filter and requires a considerable oversampling factor, compared to the natural, synchronous sampling of pulse-width-modulation

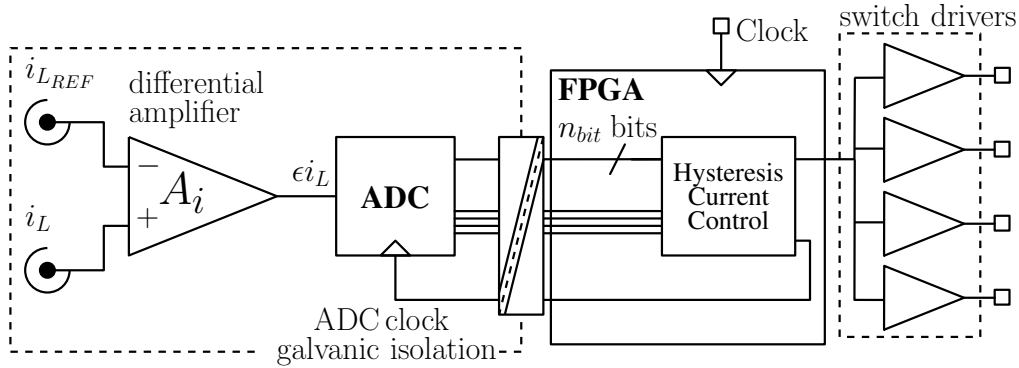


Figure 6-2: Current error acquisition and processing circuit structure.

(PWM) based current controllers. It overcomes the typical limitations of conventional hysteresis controllers, guaranteeing regulated switching frequency, with a few percent accuracy in the steady-state, together with minimum sensitivity to dead-times, sampling, and computation delays.

In the following, the algorithm operation and its design criteria are firstly explained. Successively, the effectiveness of the proposed solution is demonstrated by means of a 3 kVA, single-phase, full bridge inverter prototype (see Fig. 6-1).

6.1.1 Fixed Frequency Hysteresis Controller

The considered hysteresis controller, schematically represented in Fig. 6-2, operates on continuously acquired current error samples. The sampling period (T_{clock}) is N times smaller—with N even—than the desired switching period (T_s^*), which defines N as the *oversampling factor* of the controller. Samples are processed by a digital, FPGA synthesized circuit to generate the logic switching commands for the power converter. No other analog input signal or analog processing, either at the input or at the output, is required to operate the controller. Indeed, differently from several previous approaches, such as [109, 111, 198–200, 203, 204], the solution described here and originally proposed in [113, 194] is *fully* digital and has minimum component count. At the same time, it retains the flexibility of programmable logic hardware, which allows easy adaptation to different DC-DC and DC-AC converter topologies.

Fixed Frequency Hysteresis Current Control

Referring to Fig. 6-2 and Fig. 6-1 and considering *a single modulation period* of duration $T_s = 1/f_s$, the following current error dynamic equation can be written:

$$\frac{d\epsilon i_L(t)}{dt} = \frac{1}{L} (v_{INV}(t) - v_O(t)) - \frac{di_{LREF}(t)}{dt}, \quad (6.1)$$

where $\epsilon i_L(t) = i_L(t) - i_{LREF}(t)$ is the current error, $v_{INV}(t) = \pm V_{DC}$ is the inverter applied voltage and $t \in [0, T_s]$. Assuming that both the current reference i_{LREF} and the output voltage v_O are *slowly* varying during the modulation period, the expression of the current error slope can be written as:

$$s^\pm(t) \cong s^\pm(0) = \frac{\pm V_{DC} - v_O(0)}{L} - \left. \frac{di_{LREF}(t)}{dt} \right|_{t=0}, \quad (6.2)$$

where all variable quantities are assumed to be well approximated by their *initial* values (i.e., taken at $t = 0$, the beginning of the modulation period). Defining the instantaneous modulation index as:

$$m(t) = \frac{v_O(t) + L \frac{di_{LREF}(t)}{dt}}{V_{DC}}, \quad (6.3)$$

at any modulation period the current error slopes (6.2) can be re-written as:

$$s^\pm \cong s^\pm(0) = \frac{V_{DC}}{L} (\pm 1 - m(0)). \quad (6.4)$$

From (6.4), it is now immediate to prove that the current error peak amplitude or *threshold* (β^*) that determines the desired duration of the modulation period T_s^* is given by:

$$\beta^* = \frac{V_{DC} T_s^*}{4L} (1 - m^2(0)). \quad (6.5)$$

Equation (6.5) proves that, if constant switching frequency is desired, the current error threshold β^* has to be continuously adjusted, to compensate the modulation index variations determined by *non-constant* current reference and/or output voltage, as per (6.3). How this general principle is exploited in the controller is shown next.

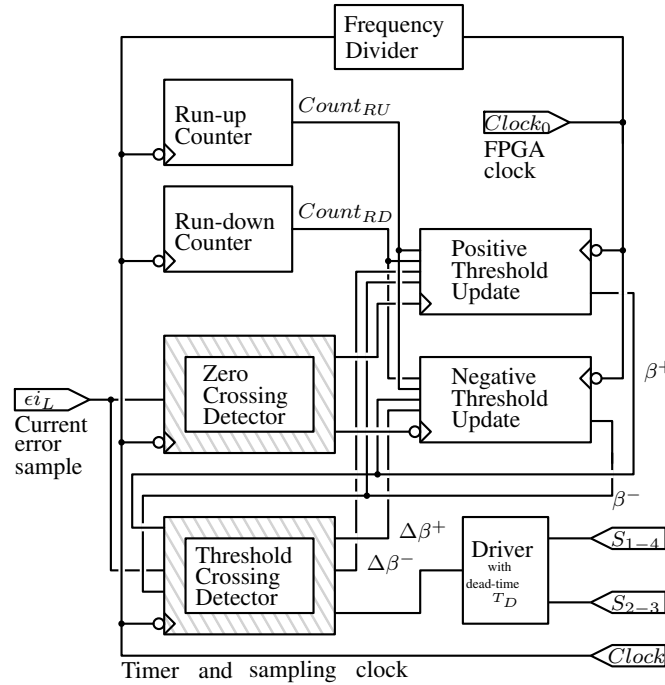


Figure 6-3: Simplified schematic diagram of the FPGA circuit organization with main control signals.

Principle of the Control Algorithm

The logic of the control algorithm can be explained referring to Fig. 6-3 and Fig. 6-4. The former shows the simplified internal organization of the FPGA circuit that implements the algorithm. The latter, instead, shows the current error signal evolution in a few control cycles around the generic k -th iteration of the algorithm, determined by a wrong hysteresis threshold positioning at instant $t_0 = (k-2)T_s^*/2$. To explain, as simply as possible, how the controller brings the current trajectory back to its ideal course, represented by the dashed line, Fig. 6-4 assumes that no switch dead-times or other error induced by data quantization affect the circuit operation.

As mentioned above, the purpose of the algorithm is to mimic an analog hysteresis controller. Besides, it is designed to synchronize the current error zero crossing instants with a predefined pulse sequence, the *synch pulses* displayed in Fig. 6-4, whose frequency is twice the desired converter switching frequency. To achieve that, at any sampling clock front, occurring N times in a T_s^* period, a new current error sample is acquired and processed in parallel by the two detection blocks of the FPGA circuit, highlighted in Fig. 6-3. Their

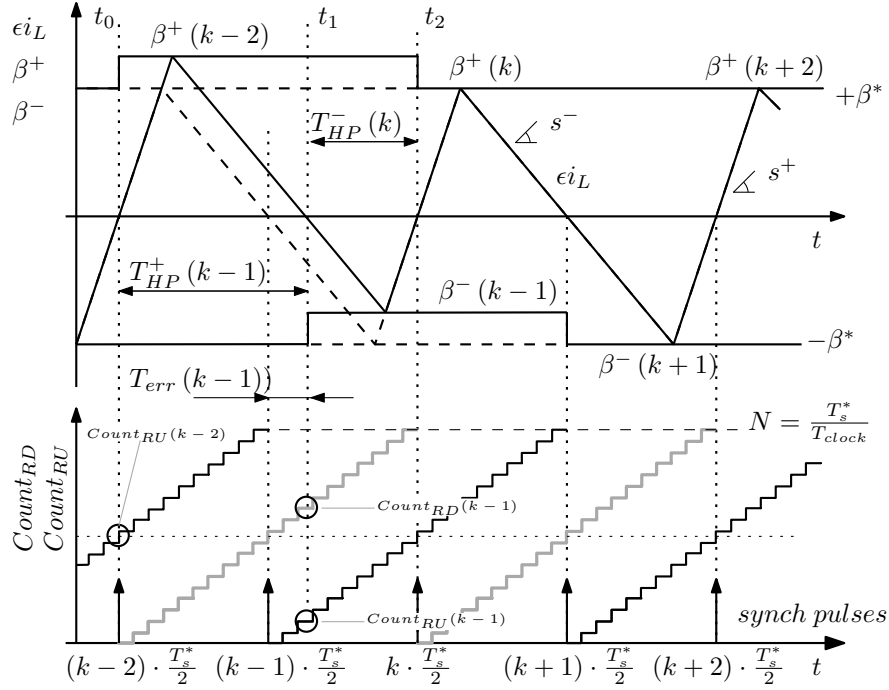


Figure 6-4: Internal variable evolution and control algorithm operation in ideal conditions (i.e., with no errors in threshold application). The sampling clock period is $T_{clock} = T_s^*/N$, where N is the oversampling ratio of the controller. Synchronization pulses occur at each counter's mid-count value, that is, with a period equal to $T_s^*/2$.

purpose is to verify if either a zero crossing or a threshold crossing condition has occurred. If neither has taken place, the circuit's state remains unaltered, and it just keeps waiting for a new sample. Otherwise, the appropriate sub-circuits are triggered, as explained in the following.

Zero crossing detection sub-circuit. If a zero crossing is detected, one of the two threshold update sub-circuits is triggered, depending on the current error slope. Indeed, a key feature of the proposed control strategy is the use of independently regulated positive and negative hysteresis thresholds. Differently from [109] and thanks to the FPGA hardware capabilities, at the time of current error zero crossing, *only the threshold the current error is directed to* is adjusted. As an example, in Fig. 6-4, at instant t_1 the zero crossing detector triggers the *negative* threshold update circuit. The sub-circuit calculates the new threshold

level according to the following equation:

$$\beta^-(k-1) = -\frac{T_s^* - 2T_{err}(k-1)}{T_s^*} \cdot \beta^*, \quad (6.6)$$

that can be derived immediately from simple geometrical considerations on the similarity of triangles. In (6.6), $T_{err}(k-1)$ represents the *synchronization error* of the last completed switching half period, that is the time distance between the zero crossing instant and the most recent synchronization pulse. In order to measure T_{err} , the threshold update circuit takes advantage of two timers, both with clock period equal to $T_{clock} = T_s^*/N$, respectively associated to the positive (Run Up, RU) and negative (Run Down, RD) slope zero crossings. The timers' setting is such that: *i*) they are reset when the target modulation period T_s^* has elapsed and *ii*) there is a half-period (i.e., $T_s^*/2$) delay between them. When the zero crossing condition occurs, both timers are read and the synchronization error is calculated, as an integer number of clock periods, according to the following relation:

$$\frac{T_{err}(k-1)}{T_{clock}} = Count_{RD}(k-1) - \frac{T_s^*}{2T_{clock}}, \quad (6.7)$$

where $Count_{RD}(k-1)$ is the reading of the timer at the $(k-1)$ -th algorithm iteration, indicated in Fig. 6-4. To finalize the calculation of (6.6), the threshold β^* , which is actually *unknown*, has to be determined as well. Because β^* experiences only negligible variations in a $T_s^*/2$ interval, the most recently adjusted value of the opposite current error threshold can be used to determine it. Indeed, again for the similarity of triangles, it results:

$$\beta^* = |\beta^+(k-2)| \cdot \frac{T_s^*}{2T_{HP}^+(k-1)}, \quad (6.8)$$

where $T_{HP}^+(k-1)$ represents the measured duration of the last completed switching half period, which corresponds to the time distance between two consecutive zero crossings of the current error.¹ To determine $T_{HP}^+(k-1)$, the timers are used once again. Indeed,

$$\frac{T_{HP}^+(k-1)}{T_{clock}} = Count_{RU}(k-1) - Count_{RU}(k-2), \quad (6.9)$$

¹The superscript $+$ of T_{HP}^+ indicates the positive phase of the current error.

where $Count_{RU}(\cdot)$ is the reading of the timer at the indicated algorithm iteration. Once $T_{HP}^+(k-1)$ is measured, substituting (6.8) into (6.6) yields the following final relation:

$$\beta^-(k-1) = -\frac{\frac{T_s^*}{2} - T_{err}(k-1)}{T_{HP}^+(k-1)} \cdot \beta^+(k-2). \quad (6.10)$$

As can be inferred from Fig. 6-4, (6.10) guarantees that the next current error zero crossing will be synchronized with the following *synch pulse* at instant $t_2 = kT_s^*/2$. A perfectly symmetrical expression is used by the other sub-circuit to calculate, at the next iteration, the adjusted value of the positive current error threshold $\beta^+(k)$ based on the run-up phase synchronization error [i.e., $T_{err}(k) \cong 0$] and the half period duration in the negative error phase [i.e., $T_{HP}^-(k)$]. When the algorithm reaches the steady-state, the current error zero crossings are in phase with the corresponding synchronization pulses and, therefore, the switching period matches the target value T_s^* . A remarkable advantage of (6.10) with respect to other frequency regulation strategies, like [201, 205], or others directly based on (6.5), is that it is completely insensitive to possible variations of system parameters (e.g., V_{DC} and L). Indeed, it totally relies on time interval measurements.

Threshold crossing detection sub-circuit. The threshold crossing sub-circuit is in charge of checking the relation between the current error sample and the hysteresis thresholds β^+ and β^- . When the current error sample crosses one of them, the appropriate switching action is commanded, so as to determine the current error slope reversal. At the same time, the measurement of the threshold error is initiated. Indeed, in the practical implementation, the current error slope reversal can be delayed with respect to the threshold crossing instant, basically due to the acquisition delay and to inverter dead-times, as shown in the insets of Fig. 6-5. The measurement of the threshold error is used by the threshold update circuits to correct the threshold level, as explained in the following.

Compensation of Controller's Non-Idealities

The above explained frequency regulation algorithm is exposed to different systematic and random error sources. The main ones are represented by:

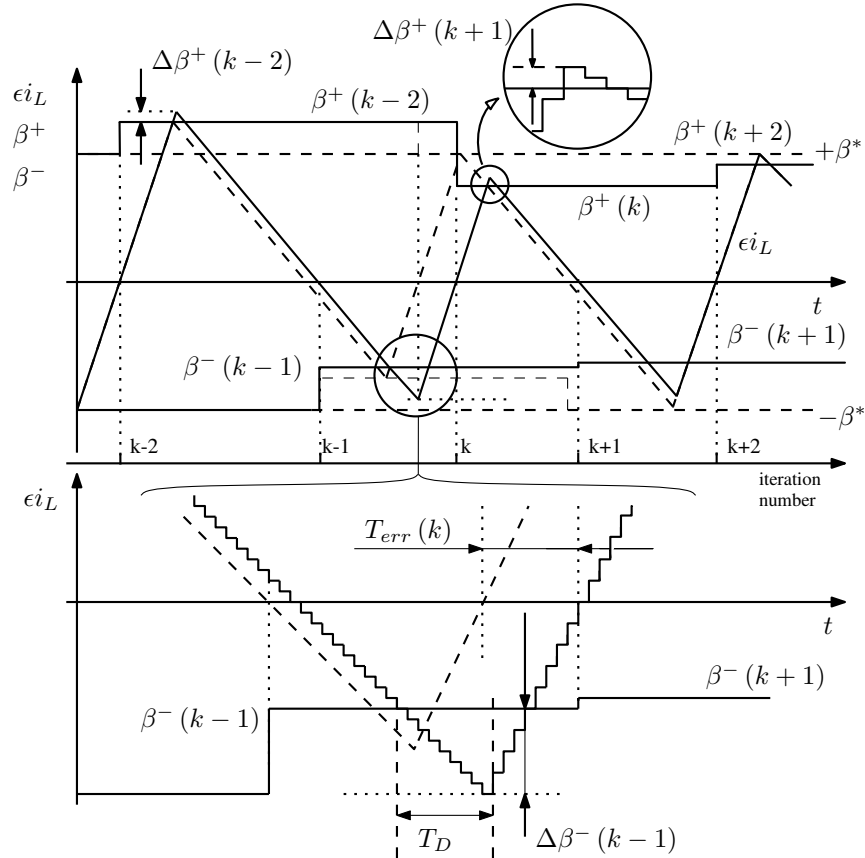


Figure 6-5: (a) Internal variable evolution and control algorithm operation in the presence of dead-times and quantization effects, determining applied threshold amplitude errors. (b) Detail of (a) where the dead-time induced threshold error is magnified.

1. analog to digital conversion (ADC) delay;
2. inverter dead-times;
3. finite counter resolution;
4. threshold saturation;
5. sampling noise.

These are examined in more detail in the following.

ADC delay and dead-times. The virtualization of the hysteresis comparator, replaced by a numerical comparison between the current error and hysteresis threshold values, introduces uncertainty in threshold crossing detection and a randomly variable delay in switch

commutations. Both effects are due to the quantization of the current error. A similar effect is caused by dead-times, which, however, determine a more systematic and much larger error. Altogether, these effects can be indicated as *threshold errors*. Their compensation is mandatory to achieve high quality switching frequency regulation and to keep zero average current error. To this purpose, when a threshold is crossed, the detector starts calculating and storing the difference between the new incoming current error samples and the last crossed threshold level, until it detects a *slope reversal*. The last measured difference represents the threshold error, indicated as $\Delta\beta^\pm(\cdot)$ in Fig. 6-5. From this standpoint, the digital implementation of the hysteresis controller is advantageous with respect to the analog one, where the threshold error due to dead-times has to be determined through interpolation [109] or approximated estimation [203]. The calculated error $\Delta\beta^\pm(\cdot)$ is then passed to the appropriate threshold update sub-circuit, which uses it, at its next activation, to correct the threshold level. As an example, the negative threshold adjustment algorithm, taking into account threshold errors, is modified as:

$$\beta^-(k-1) = -\frac{\frac{T_s^*}{2} - T_{err}(k-1)}{T_{HP}^+(k-1)} \cdot [\beta^+(k-2) + \Delta\beta^+(k-2)] - \Delta\beta^-(k-3). \quad (6.11)$$

A symmetrical expression applies to the positive threshold. Equation (6.11) is the one actually calculated by the threshold update circuit. Referring once again to Fig. 6-5, it is possible to see the different corrections, with respect to Fig. 6-4 (dashed trace), necessary to compensate for the same initial perturbation of the positive threshold. As can be seen, the presence of a dead-time (T_D) makes the first negative threshold adjustment ineffective in correcting the synchronization error. The threshold error $\Delta\beta^-(k-1)$ is generated that, in turn, generates the synchronization error $T_{err}(k)$. However, the measurement of $\Delta\beta^-(k-1)$ and $T_{err}(k)$ allows the algorithm to adjust the positive threshold $\beta^+(k)$ and, in the absence of random threshold errors, to get the synchronization error to zero at the following zero crossing, namely, the $(k+1)$ -th.

Because the last positive half period duration is still not equal to its reference value, at the $(k+1)$ -th zero crossing, the circuit will actually adjust the negative threshold once again, this time taking into account the dead-time induced error $\Delta\beta^-(k-1)$. As a result,

the negative threshold will be set to a less negative value, with respect to the ideal one, fully compensating the dead-time effect on the average current error. This asymmetrical threshold positioning allows the current error to keep zero average value, which cannot be guaranteed by setting $\beta^+(\cdot) = -\beta^-(\cdot)$. In that case, the regulation would be maintained at the expense of an average current error. Instead, keeping the current error zero crossings synchronized with the reference pulses, zero average current error is guaranteed *together* with frequency regulation. Finally, it is possible to notice how the disturbance (i.e., the wrong initial positive threshold value) is compensated in one and a half modulation period, after which the average current error and the frequency error are both back to zero (neglecting the effects of small random threshold errors).

Finite counter resolution. The choice of T_{clock} is crucial to the algorithm operation. Indeed, the algorithm time measurements (6.7) and (6.9) are obtained as integer multiples of this period, which also represents the uncertainty in the measurement of T_{HP}^\pm . As a result, the algorithm inherently generates limit cycle oscillations (LCOs), even in ideal conditions (no dead-times, no quantization or threshold errors). In order to limit the LCO amplitude, the ratio between the target switching period, T_s^* , and the clock period must not be set too low. Provided that $\beta^\pm(\cdot)$ is represented on more bits than the timing measurements, the minimum oscillation amplitude is easy to predict, using (6.8). It is given by the following relation:

$$\Delta\beta_{LCO} = \pm \frac{2T_{clock}}{T_s^*} \cdot \beta^* = \pm \frac{2}{N} \cdot \beta^*, \quad (6.12)$$

which can be used as a basic guideline to choose the maximum applicable T_{clock} . Because β^* and the switching period are proportional to each other, (6.12) proves that the best case cycle by cycle relative error on frequency regulation is $\pm 2/N$. In general, a certain amplification of the LCO amplitude can take place, due to threshold errors or other non-linear effects (e.g., saturations), especially when the inverter operates close to the maximum modulation index. Therefore, (6.12) gives just a best case estimation of the steady-state frequency regulation error. On the other hand, increasing the sampling rate and clock resolution beyond a maximum limit, which depends on the slope (6.4) of the current error and on the resolution of its numerical representation, results in multiple samples falling into

the same ADC bin. When this happens, there is no real advantage in further increasing the clock frequency; the uncertainty in zero or threshold crossing detections becomes higher than T_{clock} . A criterion to estimate the upper limit of the controller's clock frequency is given by:

$$f_{clock}^{max} = \frac{1}{T_{clock}^{min}} = \frac{V_{DC}}{L} \cdot \frac{2^{n_{bit}} \cdot K_{sense,i}}{FSR}, \quad (6.13)$$

where FSR is the ADC full scale range and $K_{sense,i}$ is the current sensor gain, so that the second term of the product represents the value in amperes of the ADC least significant bit (LSB). The meaning of (6.13) is that, when the modulation index is zero, the current error slope is such that one LSB is added for each clock period to the current error representation. As a result, zero or threshold crossing is detected with a single clock period uncertainty. Of course, when the modulation index differs from zero only the steeper (i.e., most critical) zero crossing or threshold crossing in each modulation period is be detected with minimum uncertainty. However, this is generally enough to ensure an excellent performance.

Threshold saturation. When the converter operates at high modulation index, the conduction interval of either S_1 - S_3 or S_2 - S_4 becomes relatively short. The FPGA circuit takes a definite amount of time, which is denoted as latency time (T_{lat}), to compute and adjust the current error threshold after each zero crossing of the current error. Therefore, if the run-up (or the run-down) phase becomes too short, positive (or negative) synchronization errors cannot be corrected rapidly enough, which generates undesired transients. In addition, if the run-up phase, or the run-down phase, becomes shorter than twice the dead-time T_D , the compensation is altogether impossible, as thresholds cannot invert their sign. Therefore, the algorithm can operate as described above only up to a maximum modulation index level, which is given by:

$$M_{max} = \min \left\{ 1 - 4 \frac{T_D}{T_s^*}, 1 - 4 \frac{T_{lat}}{T_s^*} \right\}, \quad (6.14)$$

where T_{lat} is equal to 550 ns in our hardware, determining a 0.956 maximum modulation index. To prevent undesired oscillations of thresholds when the modulation index tends to become higher than (6.14), a saturation strategy needs to be implemented. In our case, any

time the calculated threshold becomes lower than a predefined minimum a fixed threshold regime is entered; specifically, the last non-saturated threshold value is applied until the modulation index reduces and threshold calculation no longer results into too small values. Of course, frequency regulation is lost during saturation, but, thanks to the asymmetrical threshold positioning, average current control can be maintained.

Sampling noise. The current controller operates comparing current samples to thresholds and measuring zero crossing synchronization errors. Therefore, a good signal to noise ratio (SNR) in the current error sampling process is mandatory to achieve satisfactory performance. The circuit can be made somewhat tolerant to input injected noise by introducing hysteretic non-linearities in the zero crossing and threshold crossing detection sub-circuits and, sacrificing some bandwidth, by implementing an input digital denoising filter. Nevertheless, if the noise level is too high, the resulting jitter in the zero crossing and threshold crossing detections will rapidly deteriorate the performance. To estimate the controller robustness, simulations have been performed injecting white noise of increasing power at the ADC input. Doing so, it has been possible to verify that excellent frequency stabilization capabilities can be obtained as long as the ADC output SNR is above 60 dB or, in other words, the controller operates on at least 10 effective bits in the current error representation; in simulation, an average error below 1% has been achieved, with an adequate value of N . To guarantee this SNR level, care must be taken in the acquisition board design and layout. Analog filters can be used as well, but their frequency response needs to be carefully shaped, so as to avoid significant current error waveform distortion.

6.1.2 Small-Signal Behavior

Because of the non-linear nature of the controller, it is not possible to analytically derive any equivalent transfer function and verify these considerations by pencil and paper calculations. It is possible, however, to implement a *simulation model* that allows to test the controller response to small sinusoidal perturbations of the steady-state reference current. Based on that, the perturbation effect can be predicted and the controller's phase lag can be numerically estimated. The simulation model has been developed replicating, as precisely

Table 6.2: Hysteresis controller parameters

| Parameter | Symbol | Value |
|-------------------|-----------|--------|
| Oversampling rate | N | 100 - |
| Circuit latency | T_{lat} | 550 ns |

as possible, the operational characteristics of the controller implementation described in Sec. 6.1.1, including ADC and arithmetic quantization, computation delays, ADC latency, and sampling noise. This model is employed in Sec. 6.3 to verify the behavior of the current control technique.

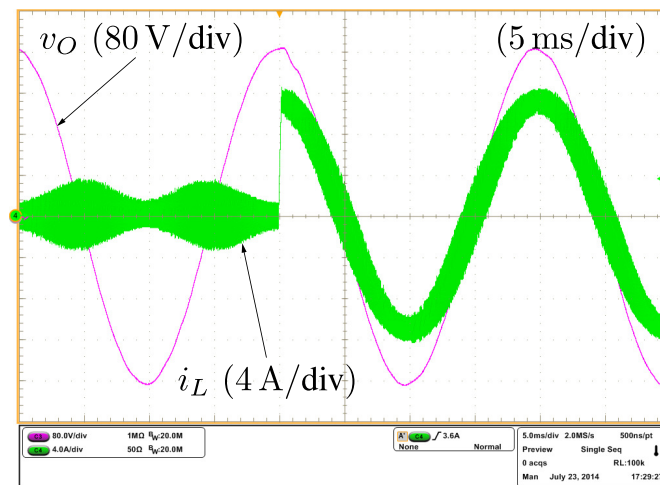
6.1.3 Experimental Test

Implementation Details

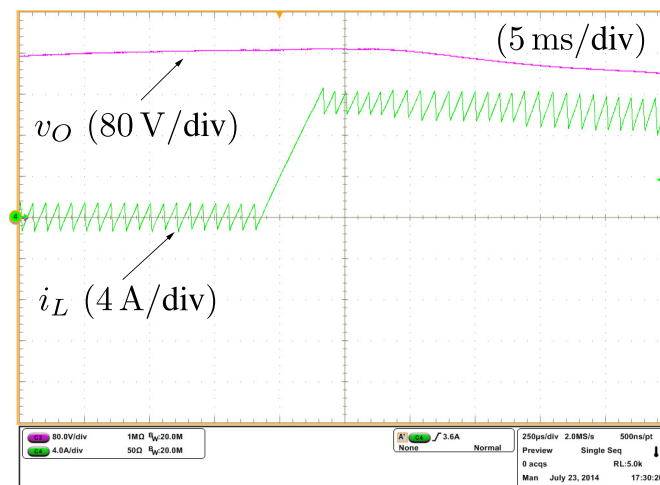
The circuit in Fig. 6-3 has been implemented in FPGA. The rising edges of a 2 MHz clock trigger the sequential execution of all the operations described in Sec. 6.1.1; this implies $N = 100$. The operations are executed within a time interval not longer than $T_{lat} = 550\text{ns}$. Concurrently in the same FPGA, an additional block clocked at 160 MHz continuously read the ADC circuit (see Appendix A) producing new samples with a throughput of 40 MHz. These samples are processed by a digital low pass filter and made available to the circuit of Fig. 6-3.

Results

The controller's response to current reference step variations is shown in Fig. 6-6 for an AC current reference signal, synchronized in phase with the imposed 50 Hz, 230 V_{rms} output voltage. As can be seen, the transient response is close to ideal, because the inverter keeps powering up the inductor for the exact time needed to track the new reference current [see Fig. 6-6(b)]. Then, it immediately resumes modulation with the correct steady-state duty cycle. As a result, the average converter current settles onto the new reference in the minimum time compatible with the available converter hardware.



(a) Reference step change.



(b) Zoomed-in view of (a).

Figure 6-6: AC step reference change.

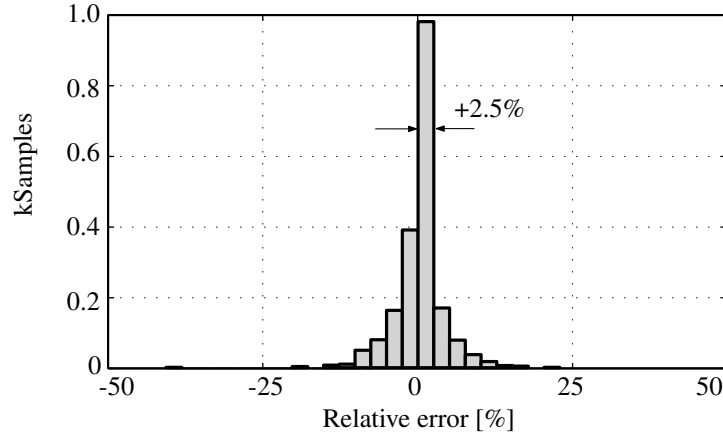


Figure 6-7: Statistical distribution of the relative switching frequency regulation error in $2 \cdot 10^3$ control cycles during the AC transient experiment of Fig. 6-6.

The resulting steady-state total harmonic distortion of the injected current is 1.47%. To illustrate the quality of frequency regulation, Fig. 6-7 shows the statistical distribution of 2000 instantaneous frequency error samples, recorded at each switching period during the AC transient experiment of Fig. 6-6. The samples are normalized to the target switching frequency value of Table 6.1. As can be seen, despite the transient, nearly 90% of the samples fall in a $\pm 5\%$ region around the target value.

6.2 Predictive Current Controller

Predictive current control has been long studied and often proposed as a high performance solution for a large variety of switch mode power supply applications. In the so-called *dead-beat* realization, originally presented in [95], a discrete time model of the controlled system is used to predict the current trajectory one or more sampling periods in advance, so as to determine the plant input (i.e., the duty-cycle) that makes the reference tracking error equal to zero in the same number of periods. The controller is characterized by a relatively low complexity, and, at the same time, by a very good dynamic performance [208].

On the other hand, the conventional implementations of dead-beat current controllers, [95, 99, 106, 208–214] are represented by software or firmware routines run by microcontrollers or digital signal processors (DSPs); these implementations typically rely on synchronous sampling and PWM processes, where the converter output current is sampled

once per modulation period. Due to the relatively slow computational speed of conventional digital control hardware, a full modulation period is normally assigned for updating the duty-cycle. As a result, two modulation periods (best case) are needed to reach the steady-state after any reference variation. When the current reference is not stepwise constant, but rather varies like, for example, a sinusoidal signal, the tracking delay results into a non-zero steady-state error. In an attempt to reduce such control delay, the use of state observers or reference estimators has been proposed [106, 210–212, 214], but this typically introduces additional sensitivity to parameter uncertainties and, in some cases, worsens the large-signal control performance.

In this section, an improved implementation of the dead-beat current controller is considered that is aimed at two purposes: *i*) the minimization of the small-signal response delay and *ii*) the optimization of the large-signal step response. The FPGA chip is employed to execute the control algorithm, the digital PWM, and the generation of switch control signals with dead-times. This organization reduces the control latency (i.e., the delay between the current sample acquisition and the duty-cycle update) to a negligible extent, allowing to perform the computations of the algorithm and duty-cycle update in the same control period. To achieve a faster response to large reference signal variations, a transient detection sub-circuit is also devised that, when triggered, overrides the dead-beat controller and operates duty-cycle corrections with minimum delay. This sub-circuit exploits the oversampling capability of the adopted ADC.

In the following, Sec. 6.2.1 explains the operation principle of the proposed controller and illustrates the provisions taken to compensate the systematic errors induced by the hardware non-ideal characteristics. The controller's small and large-signal responses are discussed in Sec. 6.2.2 and 6.2.3, respectively. Finally, in Sec. 6.2.4, the final controller's behaviour obtained from the experimental setup represented in Fig. 6-1 is shown.

6.2.1 Dead-Beat Controller

The principle of the proposed dead-beat current controller can be explained referring to the simple converter model shown in Fig. 6-8. The model assumes that the converter generates

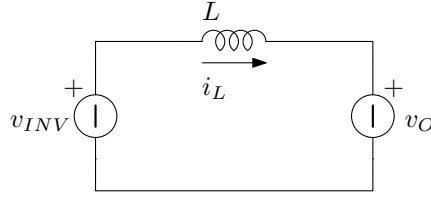


Figure 6-8: Converter equivalent circuit.

a PWM-controlled square wave signal v_{INV} that is filtered by a purely inductive output filter. It is worth noting that, although any inductor always presents some equivalent series resistance (ESR), the dynamic associated to the L/R ratio is typically much longer than the switching period. Because of that, the inductor current dynamics, in a switching period, are only marginally affected by the ESR and the assumption of an ideal inductor is generally well verified. The converter output voltage v_O is considered to be an exogenous input to the system, and can be both AC and DC. As a result, the scope of the discussion is not limited to DC-AC converter applications, but actually applies to any voltage source converter topology and application that is adequately modeled by the circuit in Fig. 6-8.

Principle of the Control Algorithm

The controller's logic organization can be explained referring to Fig. 6-9(a). A new current sample is read every M modulator clock periods ($M = 3$ in the figure), together with an output voltage v_O sample, for a total number of times Q during the modulation period, whose duration equals $2N$ clock periods. In other words, Q represents the *oversampling factor* of the controller. The current error at the k -th algorithm iteration, that is,

$$\epsilon i_L(kT_{sample}) = i_{LREF}(kT_{sample}) - i_L(kT_{sample}), \quad (6.15)$$

is then computed. The dead-beat controller is conceived to regulate the inverter *average* current, whose samples are naturally available at the instants indicated by arrows in Fig. 6-9(a), which correspond to the geometrical midpoints of the inverter voltage pulses (positive *and* negative). Accordingly, the control circuit is designed to select exactly those samples in the data stream generated by the ADC and to use them to adjust the duty-cycle, aiming at driving the reference tracking error to zero in a single *control* period. As a result, the

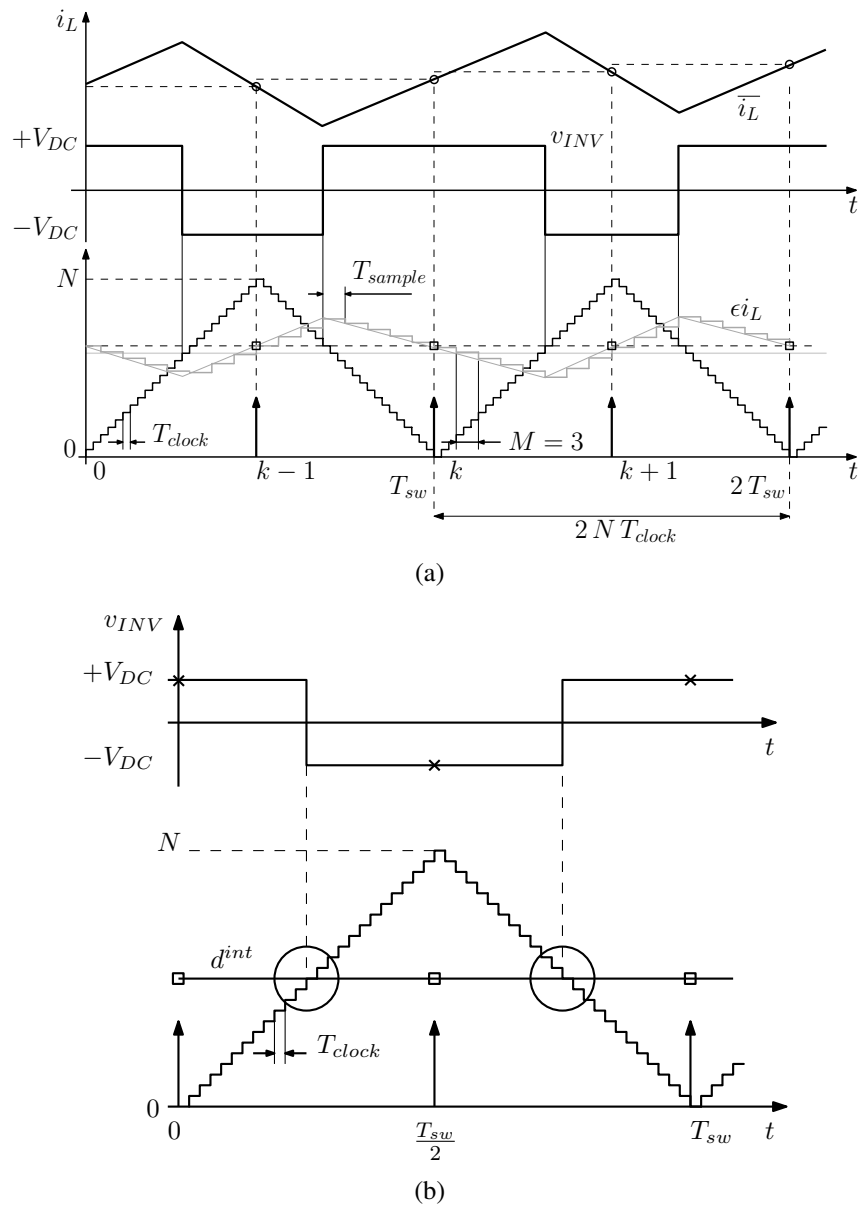


Figure 6-9: Dead-beat controller's operation principle: (a) the controller acquires $Q \geq 2$ samples per switching period, but only those taken in the clock periods marked by the arrows are used to update the duty-cycle. (b) Detail of the DPWM logic: the binary comparator treats the equality condition differently in the run-up and run-down phases so that, *in the steady-state*, a constant modulating signal generates perfectly symmetrical voltage pulses, centered on the sampling instants.

duty-cycle is updated *twice* in each modulation period. As will be shown in Sec. 6.2.3, the additional current error samples, available any time $Q > 2$, can be effectively exploited to improve the controller's large-signal dynamic response.

Considering Fig. 6-8 and Fig. 6-9(a), the following *average* current (\bar{i}_L) dynamic equation can be written:

$$\bar{i}_L(k+1) = \bar{i}_L(k) + d(k) \cdot \frac{V_{DC}}{2L f_{sw}} - (1-d(k)) \cdot \frac{V_{DC}}{2L f_{sw}} - \frac{v_O(k)}{2L f_{sw}}, \quad (6.16)$$

representing the zero order hold discrete time version of the inverter output current differential equation.² It is now possible to set $\bar{i}_L(k+1) = i_{LREF}(k)$ and to determine, as a result, the following duty-cycle update algorithm:

$$d(k) = \frac{L f_{sw}}{V_{DC}} \cdot \epsilon i_L(k) + \frac{v_O(k)}{2V_{DC}} + \frac{1}{2}. \quad (6.17)$$

The result of (6.17) is the input of the DPWM, whose counter operates according to the symmetrical pulse generation strategy shown in Fig. 6-9. As long as the converter's parameters appearing in (6.16) are *exactly* known, the reference tracking error is brought to zero in a single algorithm iteration.

It is worth noting that, in deriving (6.17), the algorithm calculation time is neglected completely, whereas it is accounted for with a full modulation period delay in the conventional controller formulations. Indeed, (6.17) determines the duty-cycle for the k -th control period, based on the most recently acquired average current and output voltage samples, belonging to the same k -th time interval. This is possible because the FPGA circuit is able to calculate (6.17) in a single clock cycle, which is, in any case, a negligible amount of time when compared to the switching—or even to the sampling—period. In case of a conventional software implementation, however, this might not be the case and the computation delay would have to be taken into account. In particular, the application of the proposed strategy could result into a not negligible duty-cycle limitation. In the case considered herein, instead, the modulating signal can be updated almost instantaneously, that is, as soon as new average current and output voltage samples are available.

²Please note that the indication of the sampling period T_{sample} has been omitted to simplify the notation.

It is also important to notice that (6.17) is correct as long as the current error sample is taken *exactly* at the midpoint of each inverter voltage pulse. This actually requires a suitable organization of the modulator, that is schematically represented in Fig. 6-9(b). As can be seen, the equality condition between the required duty-cycle numerical representation d^{int} , that is an integer number in the range $[0, N]$, and the DPWM counter is treated differently in the run-up and in the run-down phase. This asymmetry is essential to guarantee that, in the steady-state, the modulator generates symmetrical pulses and that the samples taken at the instants indicated by the arrows correspond exactly to the *average* value of the inverter current.

Limit Cycle Oscillations

The current control algorithm (6.17) is exposed to LCO phenomena, as any controller driving a digital pulse width modulator [215, 216]. These can be caused, primarily, by:

1. insufficient resolution in the DPWM;
2. incorrect choice of the controller oversampling ratio Q .

Each of these causes are discussed and the appropriate countermeasures presented in the following.

DPWM resolution. In a system like that of Fig. 6-8, the DPWM generates LCOs any time the duty-cycle required to achieve the $V \cdot s$ balance for inductor L does not match any of the physically realizable ones (corresponding to one of the possible counter values). As a result, the controller will *always* trigger some LCO. However, the LCO amplitude and frequency can be reduced to practically negligible levels, essentially increasing the DPWM resolution.

A simple criterion to determine the required DPWM resolution can be explained considering Fig. 6-9(a) once again. It is possible to see that the minimum applicable duty-cycle correction is equal to $1/N$. Varying the duty-cycle by such a minimum amount determines, after one half of a modulation period, an average current variation, whose amplitude can be

compared to the current error least significant bit value (q_{ADC}). Assuming *uniform* quantization and *unsigned* representation for the current samples, the following inequalities can be found:

$$\frac{1}{N} \leq k_\epsilon \cdot \frac{LSB_i}{2} \Leftrightarrow f_{clock} \geq \frac{V_{DC}}{L} \frac{2^{nbit}}{i_L^{MAX}}, \quad (6.18)$$

where i_L^{MAX} represents the full scale range (FSR) of the current sensor and $k_\epsilon = L f_{sw}/V_{DC}$ is here defined as the predictive current controller gain. Satisfying these conditions guarantees that enough resolution is available in the DPWM to make *all* LCOs so small in amplitude to have a negligible impact on the controller's performance. With the controller parameter values listed in Table 6.1, $V_{DC} = 400$ V and $L = 1.2$ mH, condition (6.18) requires a 27.31 MHz minimum clock frequency for the DPWM. For this reason, $f_{clock} = 28$ MHz has been considered in the controller implementation, yielding $N = 700$ when the switching frequency is set to 20 kHz.

Oversampling factor Q . With the proposed algorithm, LCOs can take place even in the presence of very high, ideally infinite, DPWM resolution, unless: *i*) the sampling process is synchronized with the modulator and *ii*) an even number of current error samples is taken in each modulation period. Only if these *necessary* conditions are met, in the steady-state all zero crossings of the current error signal are aligned with the average current sampling instants and, consequently, undesired transients are avoided.

Synchronization is ensured by the hardware organization of the controller, where the ADC sampling clock is directly derived from the DPWM clock. In addition, in order to get an even number of samples per switching period, the following design constraint must be satisfied:

$$Q = 2N/M = 2P \quad N, M, P, Q \in \mathbb{N}, N \geq M. \quad (6.19)$$

In other words, not any oversampling factor is compatible with a given DPWM resolution.

Systematic Errors

The described controller is capable of excellent steady-state performance in *ideal* conditions. In practice, however, the control action is negatively affected by switching dead

times, that are obviously unavoidable. Besides, the ADC latency and—to a much lesser extent—the FPGA calculation delay may induce further systematic control errors. Details on the compensation of these systematic errors are provided in the paper [195].

6.2.2 Small-Signal Behavior

If the above described modulator logic is adopted, then the algorithm (6.17) achieves an ideal one-step delayed dead-beat response to any step reference change. Indeed, by Z-transforming (6.17) the following *small-signal* discrete time transfer function can be defined:

$$R(z) = \frac{D(z)}{\epsilon I_L(z)} = \frac{L f_{sw}}{V_{DC}} = k_\epsilon, \quad (6.20)$$

where $\epsilon I_L(z)$ and $D(z)$ are the Z-transform of the current error and the duty-cycle sequence, respectively. Similarly, Z-transforming (6.16), under the assumption of exact system parameter identification, yields:

$$G(z) = \frac{\overline{I}_L(z)}{D(z)} = \frac{1}{k_\epsilon} \cdot \frac{z^{-1}}{1 - z^{-1}}. \quad (6.21)$$

Calculating now the unity feedback closed loop transfer function between the current reference sequence and the actual average current sequence it results:

$$W(z) = \frac{\overline{I}_L(z)}{I_{LREF}(z)} = \frac{R(z)G(z)}{1 + R(z)G(z)} = \frac{\frac{z^{-1}}{1 - z^{-1}}}{1 + \frac{z^{-1}}{1 - z^{-1}}} = z^{-1}. \quad (6.22)$$

Equation (6.22) proves that, in a small-signal sense, the algorithm (6.17) generates a current that is a single control period delayed replica of its reference.

It is worth noting that the implementation considered herein reduces the small-signal delay to the minimum achievable duration for a linear, PWM based controller, namely, to one half of the modulation period. This is exactly one quarter of what has been achieved in past implementations like, for example, [97, 209, 210].

A potential limitation for the predictive controller is represented by model mismatches or parametric uncertainties, extensively discussed in several papers, such as [97] or [209]. The same approach adopted in [97, 209] can be applied to the proposed controller to evalu-

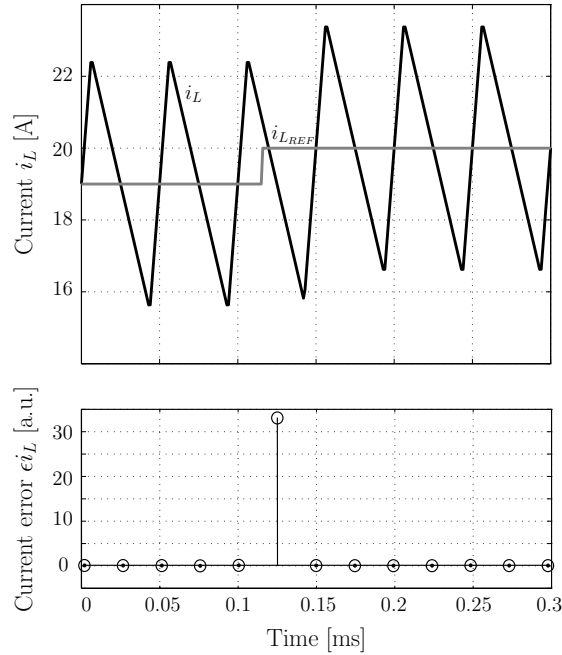


Figure 6-10: Small-signal step response in ideal conditions.

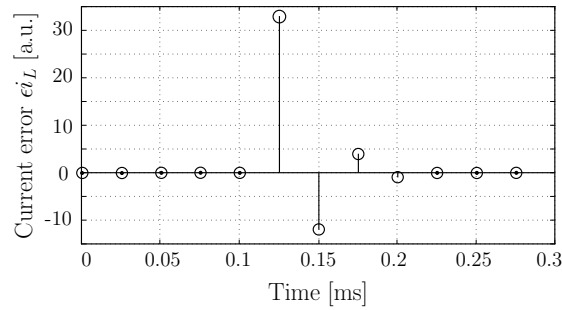


Figure 6-11: Small-signal step response as in Fig. 6-10, but with $\Delta L/L = +0.35$.

ate its sensitivity to parametric uncertainties. From (6.22), it is immediate to prove that the closed loop system eigenvalue is given by:

$$\lambda = \pm \frac{\Delta L}{L} = \pm \frac{\hat{L} - L}{L}, \quad (6.23)$$

where ΔL represents the absolute uncertainty on the value of inductor L , that is, the difference between its estimated value \hat{L} and its true value L . As can be seen, the eigenvalue lies within the unity circle any time the relative uncertainty is lower than 100%. Because the inductor variations, even in the presence of partial core saturation, are not likely to be so

large, the controller poses no real stability issues. However, experiments and simulations show that noticeably less ideal dynamic responses (with respect to Fig. 6-10) are obtained any time the parametric error is higher than $\pm 20\%$. An example of the effects of a $+35\%$ inductance estimation error in the controller is shown in Fig. 6-11. As can be seen, although the system is still asymptotically stable, the current error is no longer nulled in a single step; instead, a damped oscillation appears. Therefore, adequate inductance characterization and construction is required to get a consistently high performance from the proposed dead-beat controller.

6.2.3 Large-Signal Response Improvement

As shown in Sec. 6.2.1, the controller modifies the duty-cycle only at predefined instants, separated by time intervals of one half of a switching period. This not only affects the small-signal properties, but also the controller's dynamic response to *large-signal* reference step changes. If no provision is taken, the latter will be characterized, in the worst case, by one additional control period delay, which may represent a severe penalization in high performance applications where the current controller is expected to frequently experience fast current reference variations.

Oversampling the current error signal, in principle, may reduce the *large-signal* response delay, provided that the controller can exploit effectively the additional current samples. To this exact purpose, our control hardware is designed to allow high oversampling factors, that is, to allow the current error to be sampled much more than twice per modulation period. A schematic view of the control hardware and of the FPGA circuit is shown in Fig. 6-12 and Fig. 6-13, respectively. As can be seen, taking advantage of the additional available samples, a *large transient detection* sub-circuit that is aimed at monitoring the current error time derivative is added to the controller.

Any time the error rate of change becomes significantly larger, in absolute value, than the maximum current variation that is *physically possible* within a single sampling period interval, namely,

$$s_{MAX} = \frac{2V_{DC}}{L f_{sample}}, \quad (6.24)$$

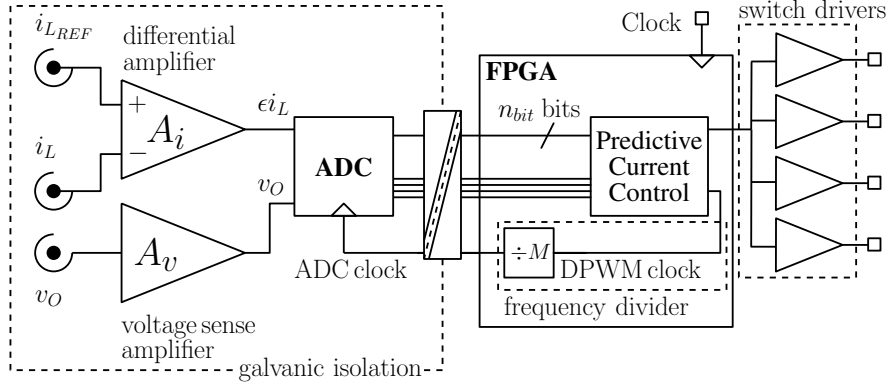


Figure 6-12: Current error acquisition and processing circuit structure of the dead-beat controller.

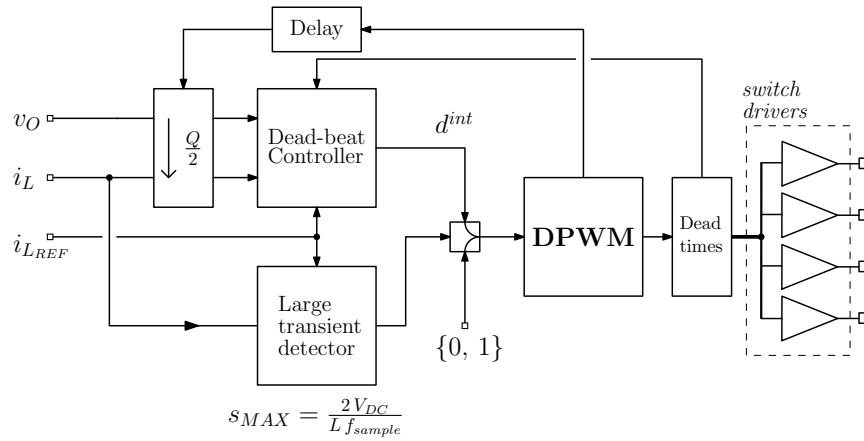
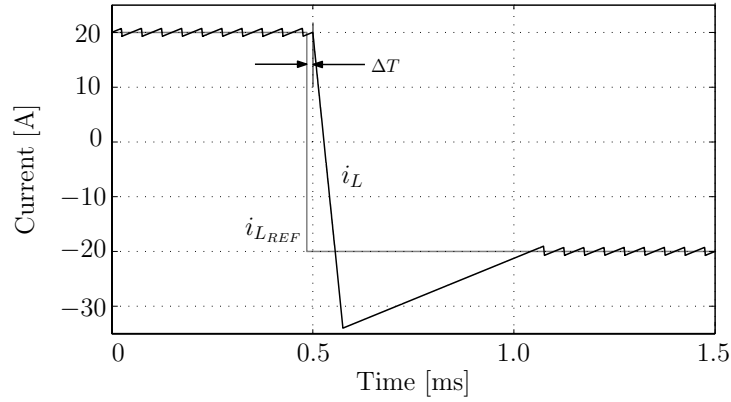


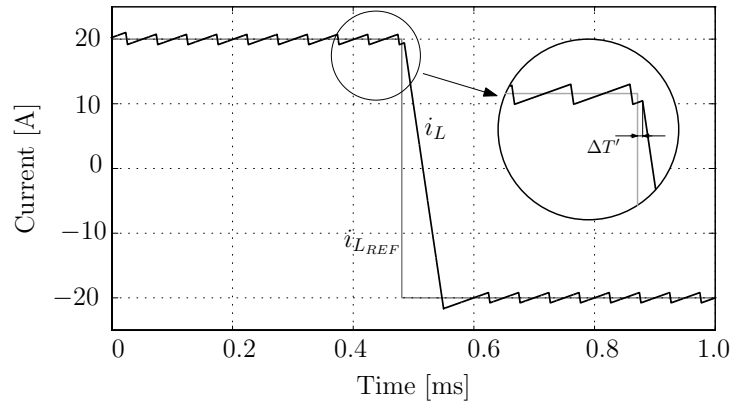
Figure 6-13: FPGA circuit with controller, modulator and transient detection sub-circuits.

the circuit overrides the dead-beat controller and modulator operation and imposes 0 or 100% duty-cycle, depending on the sign of the current error derivative. Please note that (6.24) is a highly selective triggering condition, scarcely prone to noise induced “false positives”. Indeed, the controller reacts only to those transients that would certainly drive the modulator to saturation at the following duty-cycle calculation. The maximum response delay is thus reduced to a single sampling period (plus the ADC latency). If the oversampling factor Q is relatively high, the reaction time can be much smaller than one half of a modulation period.

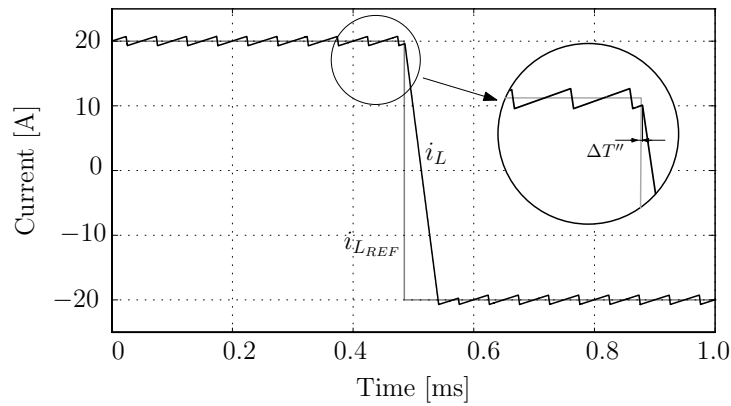
Once the current error is reduced so much that the current variation required to hit the reference in a control period is smaller than s_{MAX} , the dead-beat controller is resumed. Because the controller equation is instantaneous (i.e., no memory is kept of previous control



(a) Reference step change without transient detection sub-circuit



(b) Reference step change with transient detection sub-circuit and oversampling rate $Q = 10$



(c) Reference step change with transient detection sub-circuit and oversampling factor $Q = 50$

Figure 6-14: Controller large-signal step response during operation with a high modulation index, $m \geq 0.9$.

Table 6.3: Dead-beat controller parameters

| Parameter | Symbol | Value | |
|---------------------|-------------|-------|------|
| Clock frequency | f_{clock} | 28 | MHz |
| DPWM resolution | N | 700 | - |
| Oversampling rate | Q | 50 | - |
| Voltage sensor gain | A_v | 2.5 | mV/V |

cycles) no settling transient can be generated.

The improvement in the large-signal response determined by this control strategy is shown in Fig. 6-14, where the converter operation at a relatively high modulation index is displayed without [Fig. 6-14(a)] and with [Fig. 6-14(b) and 6-14(c)] the transient detection sub-circuit. As can be seen in Fig. 6-14(a), without the sub-circuit the current reference variation is detected with a certain delay, indicated by ΔT . In addition, because the modulation index is high, an undershoot is generated. Indeed, without oversampling, the controller acquires just three current error samples during the transition. In this particular case, the samples happen to be placed so that no correction is applied to the duty-cycle until the current has gone well below the desired set-point. Thanks to oversampling ($Q = 10$), in Fig. 6-14(b) the response delay is significantly reduced, together with the undershoot effect. Finally, in Fig. 6-14(c), that considers a higher oversampling factor ($Q = 50$), both the delay and the undershoot are practically eliminated. It is worth noting, however, that undershoot (as well as overshoot) effects are not easily observed at lower modulation indexes, even if the detection sub-circuit is not activated. Indeed, for a low current rate of change, a relatively large number of samples is taken during any transient, so that the conventional sampling strategy is typically able to prevent severe controller saturation. The response delay instead, cannot be avoided. Therefore, the transient detector provides the most significant practical benefits exactly in the minimization of the response delay. With the controller parameter values listed in Table 6.3, the step response delay in large-signal conditions is expected to be, in any case, lower than $1.5 \mu\text{s}$, a very low value that is experimentally verified in the following section.

6.2.4 Experimental Test

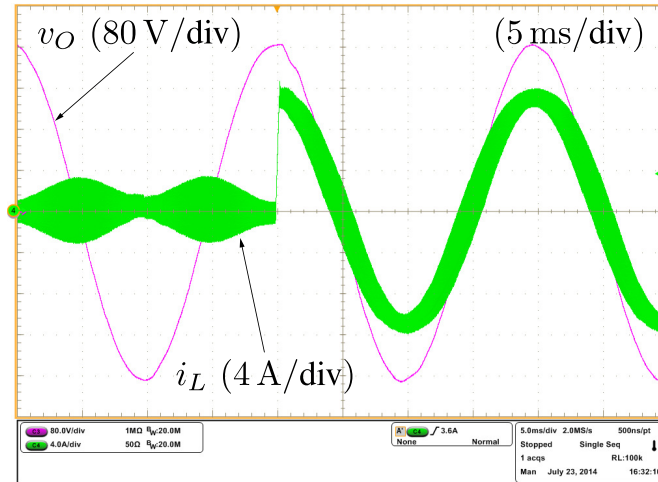
Implementation Details

The FPGA implementation circuit comprises two different clock domains, this allows to optimize power consumption and relax synthesis constraints whenever possible. The fastest domain operates on a 60 MHz clock, and includes the calculator of equation (6.17), the ADC read sub-circuit and the transient detector sub-circuit. Differently from the calculator, which operates *on demand*, the ADC read circuit is continuously working in the background, so as to make transient detection possible. Calculations are always executed in a single master clock cycle. Accordingly, the observed worst case duty-cycle update delay is equal to two clock periods (i.e., $\cong 33$ ns), the first one being used to transfer the samples from the ADC to the calculator and the second one to perform the calculation of (6.17). Such a delay represents a negligible fraction of the 50 μ s modulation period, and would still be negligible even if significantly higher modulation frequencies (up to a few hundred kHz) are considered.

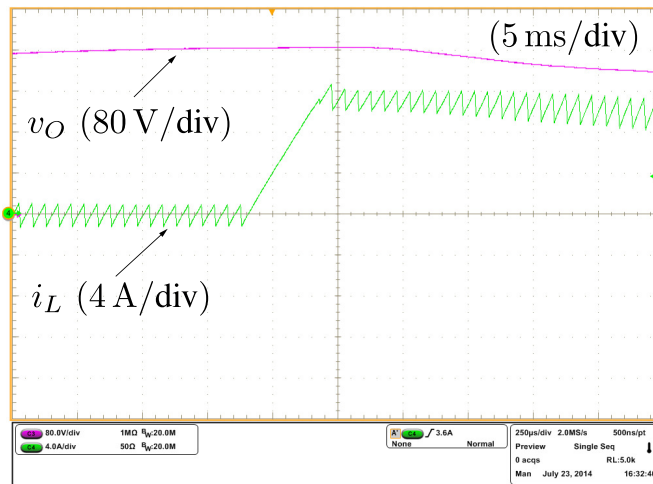
The DPWM is implemented in a different, 28 MHz clock domain and represents the heart of the circuit. Its clock is used to derive the ADC clock, which is one of the outputs of the FPGA chip. Setting $M = 28$, a 1 MHz sampling frequency (i.e., $Q = 50$) has been obtained. The other FPGA outputs are the inverter switch gate signals, once again generated by the modulator sub-circuit. In addition, the DPWM unit generates all the internal synchronization signals, like the data request signal, used to activate the control equation calculator at the desired instants.

Results

The controller's response to current reference step variations is shown in Fig. 6-15 for an AC current reference signal synchronized in phase with the imposed 50 Hz, 230 V_{rms} output voltage. Similarly to what observed in Sec. 6.1.3 for the case of the hysteresis controller, the transient response is close to ideal, notably, the current variation has maximum speed, with no unnecessary switching and no undesired settling transient taking place [see Fig. 6-15(b)]. Therefore, the average converter current settles onto the new reference in the



(a) Reference step change.



(b) Zoomed-in view of (a).

Figure 6-15: AC reference change.

minimum time compatible with the available converter hardware.

In Fig. 6-16 the controller’s response to a reference step variation is shown. Thanks to the oversampled implementation and to the transient detection algorithm, the controller can react well before the expected duty-cycle update instant, differently from what a conventional implementation would do, which yields a negligible large-signal response delay. This is clearly visible in Fig. 6-16(a), where the current inverts its slope immediately after the reference signal has changed. A clean response with no overshoots and no visible limit cycle effects is hence obtained, which confirms the simulation result of Fig. 6-14(c).

For better highlighting the improvement with respect to a more conventional imple-

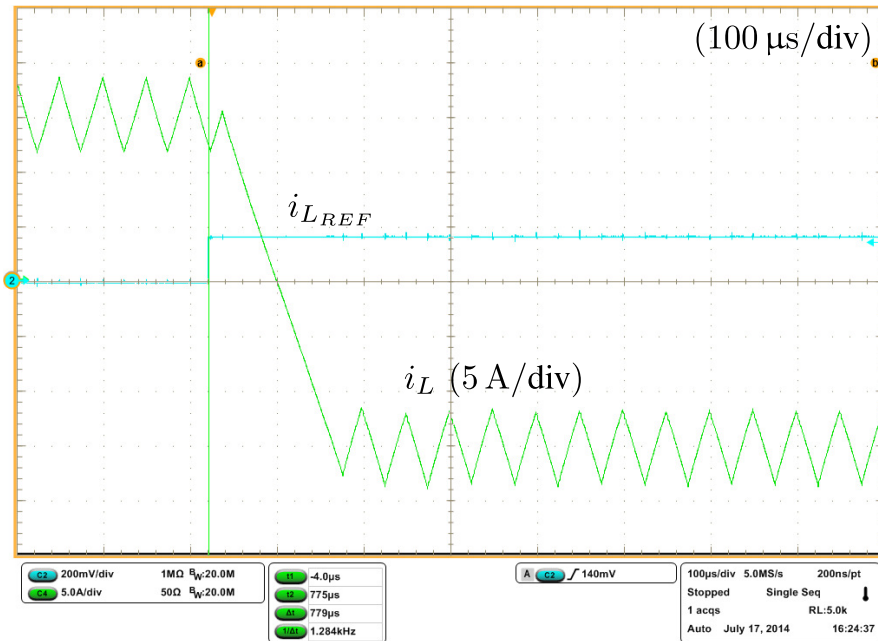
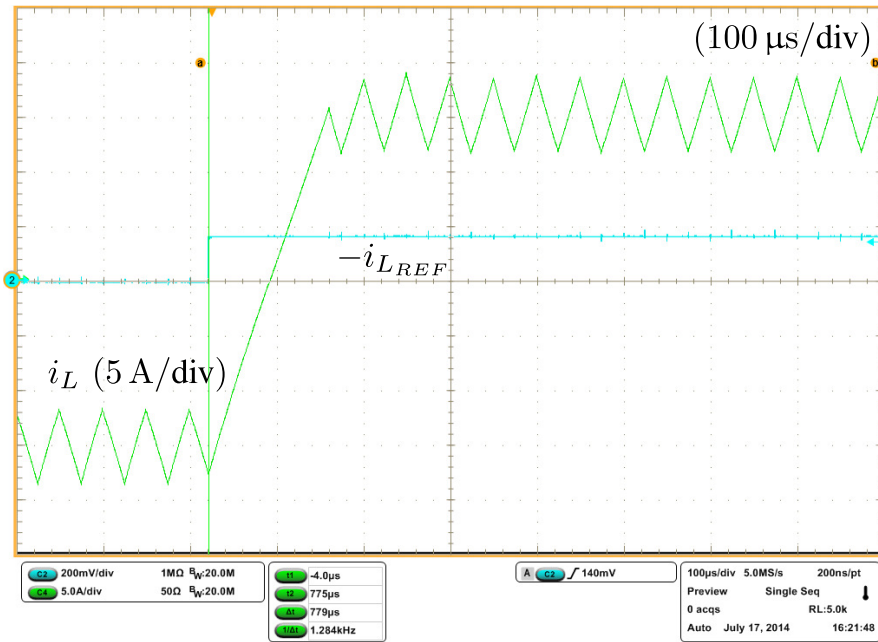


Figure 6-16: Experimental DC step responses of the proposed current controller to a step reference variation from -15 A to $+15\text{ A}$ and vice-versa. (a) with the transient detection circuit enabled; (b) without transient detection. Traces are: inductor current i_L (5 A/div) and reference current signal i_{LREF} (200 mV/div). Time-base: $100\ \mu\text{s/div}$.

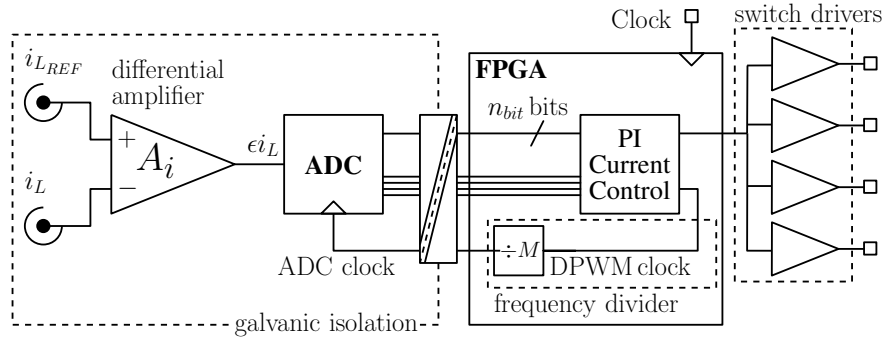


Figure 6-17: Current error acquisition and processing circuit structure of the oversampled PI controller.

mentation, Fig. 6-16(b) shows the step response when the transient detection algorithm is disabled. In this case, the current does not change its trajectory until the next duty-cycle adjustment is triggered by the DPWM, which determines, in this particular example, a $18 \mu\text{s}$ additional response delay. As mentioned before, because the modulation index is low (specifically, it is close to zero), no undershoot takes place, even if the transient detector is disabled.

6.3 Comparison

In this section the proposed oversampled current controllers are compared with a more conventional solution, represented by the oversampled proportional-integral (PI) current controller. This comparison aims at quantifying the advantages and disadvantages characterizing the different approaches and at highlighting the improvements brought by the proposed solutions described in Sec. 6.1 and Sec. 6.2.

6.3.1 The Conventional Oversampled PI Current controller

The hardware configuration of the controller is schematically shown in Fig. 6-17. As can be seen, the current error is sampled and subsequently processed at the occurrence of a clock pulse, derived from the DPWM clock that defines the time resolution of the modulation period. The typical signals for this type of controller are illustrated in Fig. 6-18, where the considered symmetrical DPWM implementation is displayed.

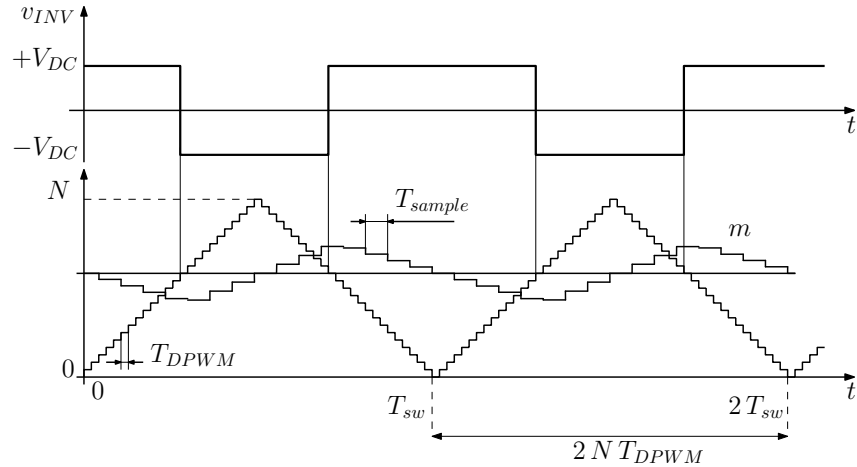


Figure 6-18: Digital pulse width modulator operation with a multi-sampled proportional integral (PI) current controller. The modulating signal m is the PI controller output, $T_{DPWM} = 1/f_{DPWM}$ and $T_{sw} = 1/f_{sw}$.

As usual, the DPWM clock frequency is an integer multiple of the switching frequency, so that each modulation period is divided into $2N$ DPWM clock periods, with:

$$N = \frac{1}{2 T_{DPWM} f_{sw}} = \frac{f_{DPWM}}{2 f_{sw}}. \quad (6.25)$$

The current error is acquired every M DPWM clock cycles with M chosen among the integer sub-multiples of N , that is, $N/M = P$, $P \in \mathbb{N}$. As a result, the oversampling factor Q of the controller can be defined as:

$$Q = 2 \frac{N}{M}. \quad (6.26)$$

As well known, closing a control loop around a DPWM may cause the occurrence of LCOs, even when oversampling is not considered [215]. A detailed analysis of this phenomenon for oversampled voltage regulation loops in buck converters is presented in [217]. Even if the considered controller is aimed at regulating the converter current, the same problem can obviously be expected to take place. In order to minimize its impact on the converter's performance the following criterion has been applied: supposing a one LSB wide duty-cycle oscillation is taking place, this can be considered to have negligible consequence if it generates an average current variation, in a switching period, that is lower

than half the zero bin of the current error sample numerical representation. Basically, this happens when:

$$f_{DPWM} \geq \frac{2^{nbit+1} V_{DC}}{L i_L^{MAX}}, \quad (6.27)$$

where i_L^{MAX} represents the full scale range in *ampere* of the current sensor. Clearly, (6.27) does not represent a necessary nor a sufficient condition to prevent LCOs, because larger duty-cycle variations can be generated, depending on the control system non-linearities, but also on the presence of noise. Adopting (6.27) as a design criterion guarantees that enough resolution is available in the DPWM to prevent the most common LCO condition, that is the non-existence of a stable DC operating point for the modulator, from perturbing the current controller significantly. In general, this makes the impact of the LCO on the regulated current practically negligible.

The PI controller gains can be easily selected imposing the desired crossover frequency and phase margin. Exploiting oversampling, the small-signal delay of the DPWM with symmetrical, triangular carrier reduces by a factor Q with respect to its natural implementation where, as known, it exactly corresponds to a $T_{sw}/2$ ZOH delay [218]. As a result, the current loop bandwidth can be pushed closer to its theoretical limit, determined by the converter output impedance.

It is easy to prove that the closed loop transfer function between the current reference and the inverter output current is given by the following expression:

$$W_{IPI}(s) = \frac{I_L(s)}{I_{LREF}(s)} = \frac{\frac{G_{PWM}(s)}{Z_O(s)} H(s)}{1 + \frac{G_{PWM}(s)}{Z_O(s)} H(s)}, \quad (6.28)$$

where

$$\begin{aligned} G_{PWM}(s) &= k_{i,sense} \frac{2 V_{DC}}{N} \cdot e^{-\frac{T_{sw}}{2Q}}; \\ Z_O(s) &= \frac{1}{sC} // Z_G(s) + sL + ESR_L \cong sL; \\ H(s) &= K_P + \frac{K_I}{s}. \end{aligned} \quad (6.29)$$

Equation (6.28) is important to estimate the equivalent small-signal delay of the closed loop current controller. Please note that the approximation $Z_O(s) \cong sL$ only holds around the controller's crossover frequency and is *not considered* in the analysis of the small-signal performance, but just to design the PI controller.

6.3.2 Experimental Results

The PI controller has been designed for a 3 kHz bandwidth and 60° minimum phase margin. The oversampling factor has been set to $Q = 20$; the same factor has been used for the predictive controller as well. Instead, for the hysteresis controller, the oversampling factor has been chosen four times higher to guarantee a sufficiently tight control of the converter switching frequency.

Small-Signal Response Test

One of the expected outcomes of the comparison presented in this section is the estimation of the small-signal response characteristics of each of the considered current controllers. For the linear controllers, an analytical solution to the problem, albeit under some simplifying assumptions, is reported in Sec. 6.3.1 and Sec. 6.2.2. For the non-linear controller of Sec. 6.1, instead, only numerical simulation and experimental measurements can give an estimation of the achievable phase lag, as mentioned in Sec. 6.1.2.

Experimental measurements have been performed for the three controllers and compared to analytical or, for the hysteresis controller, simulation results. The tests have been performed injecting a small sinusoidal perturbation signal into the current control loop and measuring the output current. The perturbation amplitude was set equal to 5% of the considered DC reference current. Then, Discrete Fourier Transform (DFT) has been calculated on the output current samples in a sufficiently large time span, so as to determine the phase and amplitude of the injected perturbation effect with adequate resolution and precision. In all experiments, the converter output voltage has been externally controlled to a constant DC level so as to achieve constant modulation index operation. The modulation index,

defined as:

$$m(t) = \frac{v_O(t)}{V_{DC}}, \quad (6.30)$$

has been set to the value corresponding to the peak of the expected average sinusoidal output voltage, equal to about 0.82. The results are presented in Fig. 6-19.

It is interesting to observe how experiments confirm the analytical results for the linear controllers, and the hypothesis on the hysteresis controller dynamic performance. In absolute terms, all the controllers guarantee a high performance level. In the considered bandwidth, extending from 10 Hz to 3.0 kHz, the amplitude response is practically flat (the measured maximum deviation is lower than 3 dB) while the phase shift is minimum for the hysteresis controller (equal to -3° at 3.0 kHz) and maximum for the PI controller (equal to -49° at 3.0 kHz).

Large-Signal Response Test

In this case, the controllers have been compared by considering their settling transients after a step change of the constant reference current. The obtained experimental results are shown in Fig. 6-20 and Fig. 6-21. In particular, Fig. 6-20(a) and Fig. 6-20(b) show the measured responses to a change in the reference current from 0 A to 10 A and from 10 A to 0 A, respectively, when the converter output is connected to a voltage source imposing $v_O = 280$ V. The relatively high, positive output voltage causes the positive current slope to be much lower than the negative one; the latter case allows to highlight how the best responsiveness is offered by the hysteresis and the predictive controllers, while the worse one is given by the PI controller. In all the cases, the reference step change is detected with minimum delay, specifically in a single sampling period. Consistent results are obtained in grid-tied operation as well; Fig. 6-21 shows the response to 180° phase steps in a 50 Hz sinusoidal reference current. A different test consisted in tracking a 50 Hz, 10 A peak amplitude, sinusoidal reference signal and measuring the resulting THD, considering harmonic components up to order 40. During the test, the grid voltage was intentionally polluted with third, fifth, seventh and eleventh harmonics, for a total THD equal to 3%. Table 6.4 reports the most relevant results of the performed experiments in the three cases.

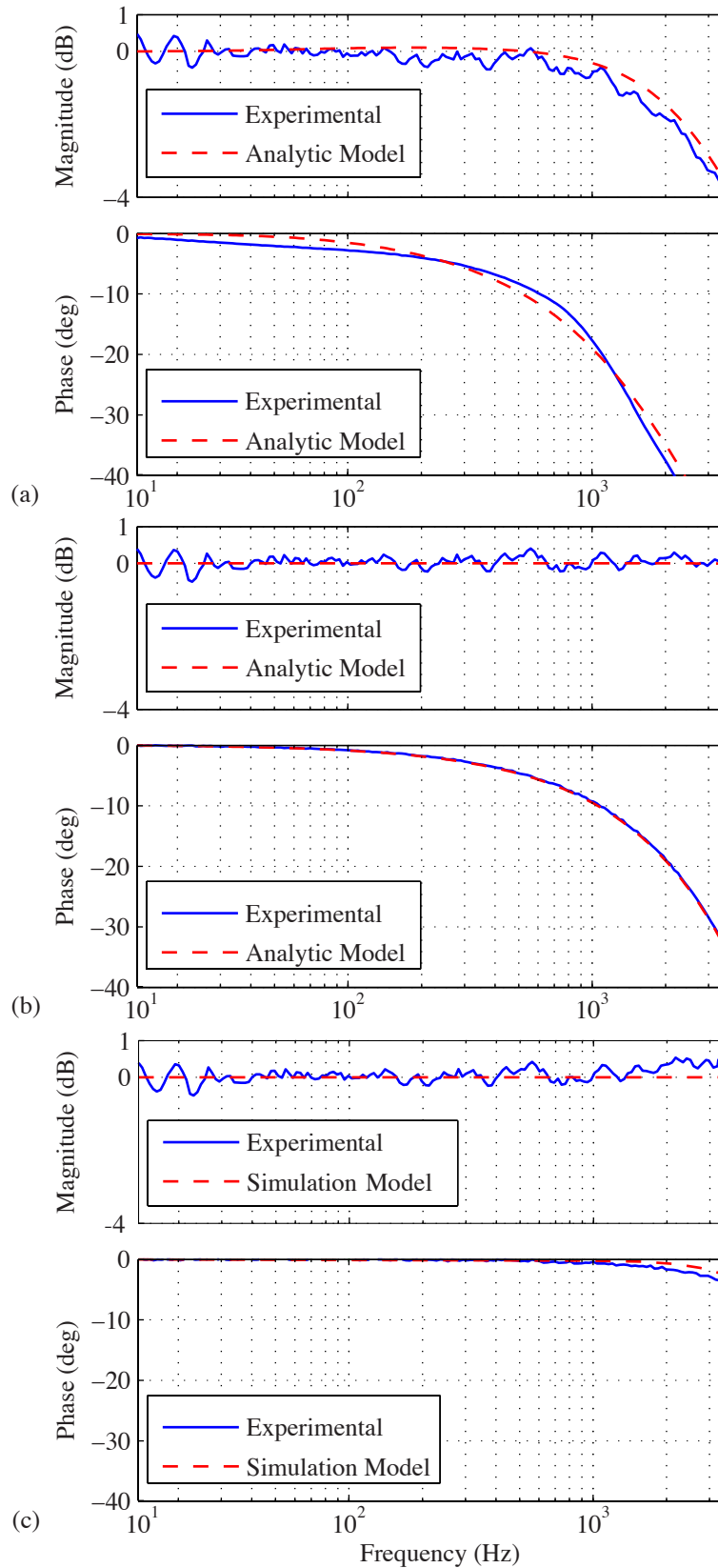


Figure 6-19: Bode plots from the analysis (dashed) and experiments (solid) of: (a) PI, (b) dead-beat, (c) hysteresis. The analysis is replaced by numerical simulation in case (c).

Table 6.4: Experimental results for the current controllers

| | PI | Predictive | Hysteresis |
|-----------------------|-------------|-------------------|-------------------|
| Phase shift @ 0.5 kHz | -8° | -5° | -0° |
| Phase shift @ 1.0 kHz | -18° | -10° | -1° |
| Phase shift @ 2.0 kHz | -37° | -19° | -2° |
| Phase shift @ 3.0 kHz | -49° | -28° | -3° |
| THD of 50Hz sinusoid | 1.52% | 0.82% | 1.47% |

As far as the measured total harmonic distortion of the inverter current is concerned, it is possible to notice that: *i*) all the controllers guarantee low distortion levels, which implies a good rejection of disturbances coming from the grid voltage, *ii*) by comparing the measured THDs, the predictive controller performs better than the other two controllers and that the PI controller shows the highest distortion. Fact *ii*) happens because the wide small-signal bandwidth of the predictive and the hysteresis controllers allows to better reject grid voltage disturbances with respect to the PI controller, whereas the low frequency harmonics disturb the instantaneous switching frequency control of the hysteresis controller and make it perform worse than the predictive one in terms of current THD.

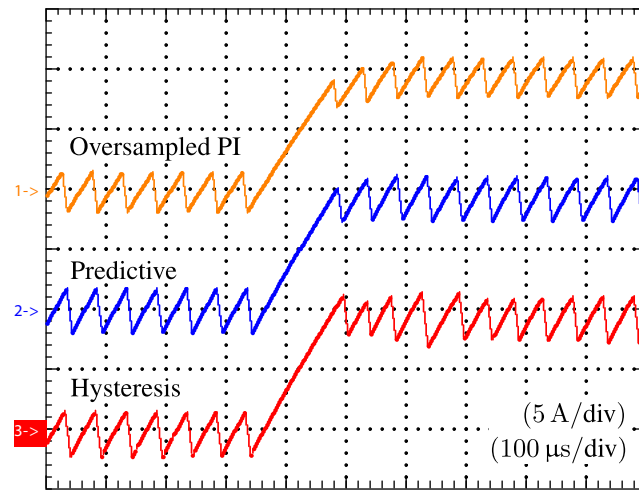
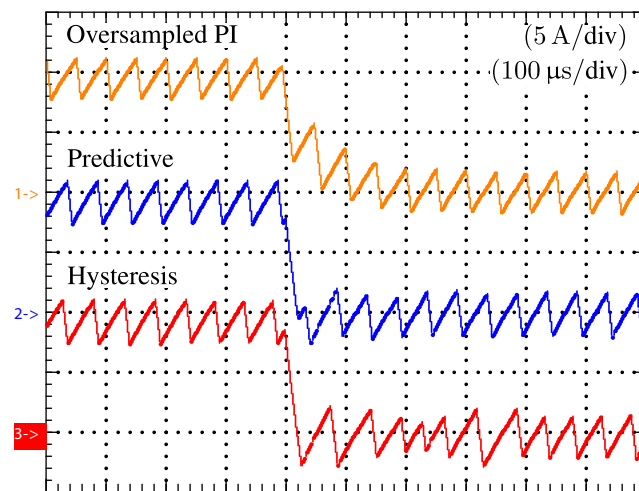
(a) Positive step of the reference current ($v_O = 280$ V)(b) Negative step of the reference current ($v_O = 280$ V)

Figure 6-20: Experimental measurement of the considered controllers' large-signal step responses.

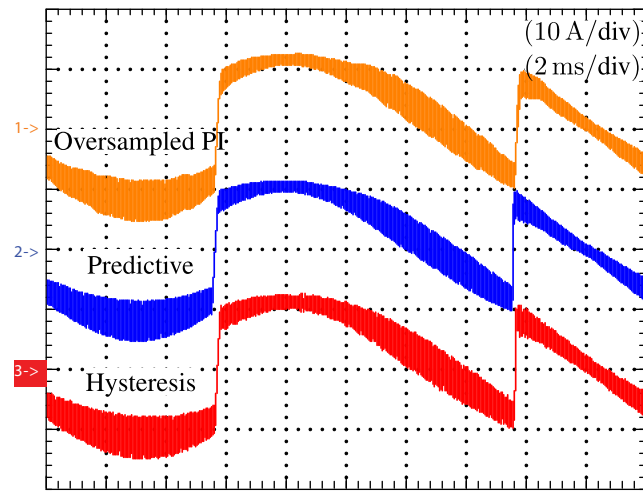


Figure 6-21: Experimental measurement of the considered controllers' large-signal step responses: 180° phase steps of a sinusoidal reference current during grid-tied operation ($V_G = 230 V_{\text{RMS}}$, $f_1 = 50 \text{ Hz}$).

6.4 Summary

In this chapter, a couple of digital, high performance, current controllers that perfectly fit the requirements of grid-tied converters are presented. In particular these controllers fit the needs of utility interface converters, as explained in details in [192].

The first controller is a fixed-frequency hysteresis current controller. Its operation results into an almost constant switching frequency in steady-state, while retaining the wide small-signal bandwidth and minimum large-signal response delay that are typical of non-linear controllers. The second controller is a minimum delay version of the dead-beat current controller. With this technique the small-signal response delay is reduced to one quarter of a switching period; the large-signal response delay is reduced to a single sampling period, plus the ADC latency.

The performances of the proposed current controllers are demonstrated by means of a laboratory prototype and compared with a more conventional controller, precisely, the oversampled PI regulator. The comparison shows that all the considered controllers attain high performance levels. In the considered bandwidth—spanning the frequency range [10Hz, 3.0 kHz]—the amplitude response is practically flat while the phase shift is minimum for the hysteresis controller (equal to -3° at 3.0 kHz) and maximum for the PI controller (equal to -49° at 3.0 kHz). Reference step changes are detected with both minimum delay and rise time for the hysteresis and deadbeat controllers, while the response of the PI regulator is, consistently with its small-signal bandwidth, significantly slower. As discussed in [192], the results attained with the reported studies provide insights on how to select the most appropriate controller for particular applications, such as the one relevant to utility interface converters.

Chapter 7

The Power-Based Control

This chapter describes a *model-free* control algorithm, called *power-based control*, where a master controller drives all distributed units to pursue the goals of secondary and tertiary control (see Table 2.2 in Ch. 2). In particular, the algorithm aims at regulating the power injection of controllable DERs (i.e., UI and EGs) so that the following objectives are simultaneously fulfilled:

- power flow at the PCC of the microgrid follows a pre-assigned profile;
- voltage magnitudes at the point of connection of controllable DERs are below a given threshold.

The former is an extremely valuable feature for a microgrid clustering renewable sources because it enables dispatchability. The latter allows to manage distribution network congestion during periods of peak production, so that to limit the stress to electrical infrastructures. To the purpose, each active unit is committed to contribute to microgrid power needs in proportion of its *power capability*, leading to a uniform utilization of DERs and thermal stress in EPPs.

It is shown that, when integrated into the master/slave architecture described in Ch. 5, the final microgrid can benefit of favorable features in terms of stability, robustness to grid parameter variations, dynamic response, and implementation requirements.

7.1 Microgrid Architecture and Control

Let's refer to the master/slave microgrid architecture introduced in Ch. 5, Fig. 5-1 and Fig. 5-2. It comprises a utility interface (UI), N energy gateways (EGs), and a set of passive nodes. As explained in Sec. 5.2, the UI permanently performs as a voltage source, and behaves as grid-supporting unit in grid-connected operation and as grid-forming unit in islanded operation. The EGs are always controlled as current sources. An ICT infrastructure provides the communication link between the UI, located at the PCC and hosting the microgrid master controller (MC), and the EGs, spread over the grid and performing as slave units.

To regulate the PCC power flow, the power-based control uses the principles described in Sec. 5.1. Specifically, in the power-based control the interaction among the MC and the EGs takes place in two phases. In the first phase, MC *gathers* from each EG a data packet that conveys the information of its local energy availability; in the second phase, MC *broadcasts* to *all* the EGs a common control packet that is finally translated by each EG into a particular power reference.¹ Power references are derived by EGs taking into account constraints on power availability and the maximum voltage magnitude (V^{\max}) at the point of connection. Fig. 7-1 highlights the two phases.

The following sections describe the operation of the power-based control algorithm in more details.

7.2 Data Collection

At the beginning of the $(\ell + 1)$ -th cycle, that is, at time instant ℓT , the MC determines the total active power $p_{MG}(\ell)$ and reactive power $q_{MG}(\ell)$ absorbed by the microgrid at PCC.² This power is equal to the sum of the power drawn from the mains (i.e., p_G, q_G) and the power delivered by the UI (i.e., p_{UI}, q_{UI}). Moreover, for $n \in \{1, \dots, N\}$, the *local controller* of the n -th EG (i.e., EG_n) sends the following data to the MC:

¹It is worth remarking that to broadcast a single, unique, reference to *all* the controllable units represents an advantageous feature of the approach, because it limits the workload to the communication infrastructure.

²For convenience, quantities are denoted simply by indicating the relevant control cycle, therefore, for example, by using $p_{MG}(\ell)$ in place of $p_{MG}(\ell T)$.

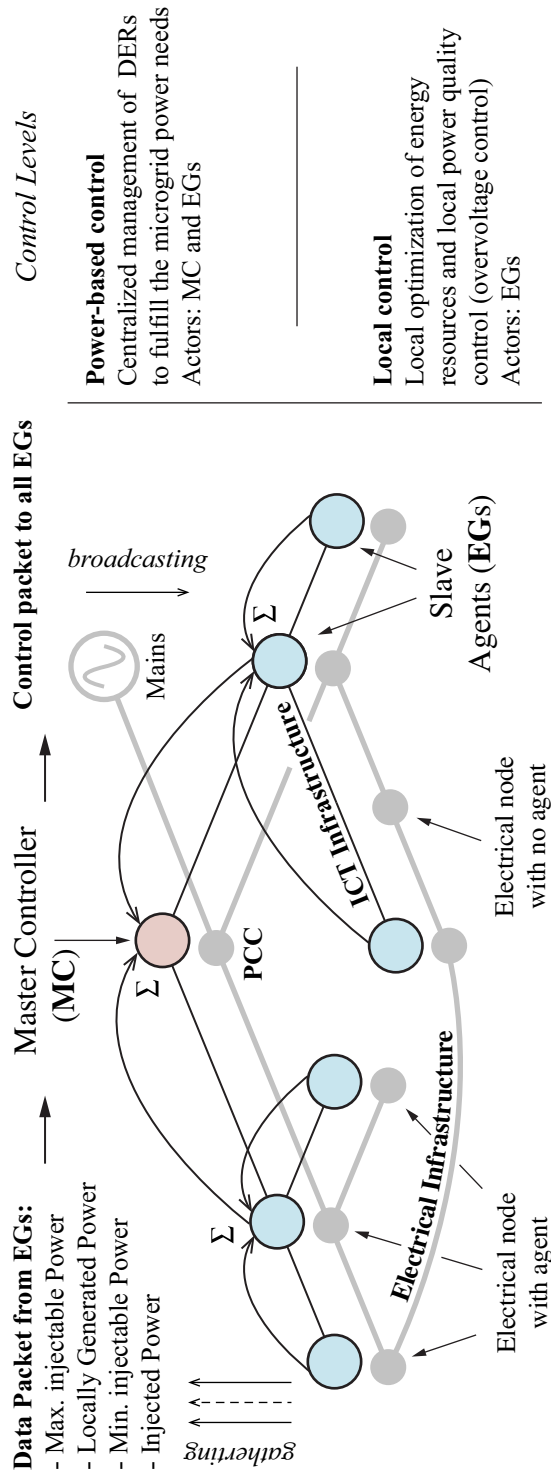


Figure 7-1: Master/slave microgrid architecture with power-based control.

- the active power $p_n(\ell)$ and the reactive power $q_n(\ell)$ generated during the ℓ -th control cycle;
- the estimated active power $\hat{p}_n(\ell + 1)$ that will be generated by the local renewable source in the current control cycle, namely, during the time interval $(\ell T, (\ell + 1)T)$;³
- the estimated minimum active power $\hat{p}_n^{\min}(\ell + 1)$ and maximum active power $\hat{p}_n^{\max}(\ell + 1)$ that the EG can inject during the current control cycle by taking into account all the local constraints, including the maximum power that can be delivered ($\hat{p}_{S_n}^{\text{out}}$) or absorbed ($\hat{p}_{S_n}^{\text{in}}$) by the local energy storage unit; in particular:

– if $|\underline{v}_n(\ell)| < V^{\max}$ (i.e., no voltage violations), then:

$$\begin{cases} \hat{p}_n^{\min}(\ell + 1) = \hat{p}_n(\ell + 1) - \hat{p}_{S_n}^{\text{in}}(\ell + 1) \\ \hat{p}_n^{\max}(\ell + 1) = \hat{p}_n(\ell + 1) + \hat{p}_{S_n}^{\text{out}}(\ell + 1) \end{cases}, \quad (7.1)$$

during *grid-connected* operation, and

$$\begin{cases} \hat{p}_n^{\min}(\ell + 1) = -\hat{p}_{S_n}^{\text{in}}(\ell + 1) \\ \hat{p}_n^{\max}(\ell + 1) = \hat{p}_n(\ell + 1) + \hat{p}_{S_n}^{\text{out}}(\ell + 1) \end{cases}, \quad (7.2)$$

during *islanded* operation;

- if $|\underline{v}_n(\ell)| \geq V^{\max}$, which corresponds to an overvoltage condition at the point of connection of the n -th EG, then \hat{p}_n^{\min} , \hat{p}_n^{\max} and \hat{p}_n are set equal to $p_n(\ell)$, that is:

$$\hat{p}_n^{\min}(\ell + 1) = \hat{p}_n^{\max}(\ell + 1) = \hat{p}_n(\ell + 1) := p_n(\ell). \quad (7.3)$$

- the rated apparent power $\hat{a}_n(\ell + 1)$ of the EPP of the EG inverter and its temporary overloading capability $\hat{a}_n^{\text{over}}(\ell + 1)$.

In a basic implementation, the estimated quantities for cycle $\ell + 1$ are simply considered equal to the values at control cycle ℓ . In more advanced implementations, during grid-connected operation it is possible to take advantage of additional information (e.g., node

³This estimate can be done on the basis of the status of the adopted renewable source (e.g., irradiation measurements for photovoltaic modules).

voltage statistics, weather forecasts) to learn how to conveniently define, on a long-term basis, the parameters $\hat{p}_{S_n}^{\text{out}}$ and $\hat{p}_{S_n}^{\text{in}}$, for example, in order to maximize the local energy production.

It is worth remarking how definitions (7.1) and (7.2) given for the estimated minimum active power \hat{p}_n^{min} reflect different control priorities in grid-connected and islanded operation. Indeed, during grid-connected operation it is more advantageous to extract all the power available from renewables (e.g., by operating PV sources at their maximum power point), whereas during islanded operation it is of paramount importance to guarantee the active power balance for the islanded system. In this light, \hat{p}_n^{min} is set equal to $\hat{p}_n - \hat{p}_{S_n}^{\text{in}}$ in grid-connected mode, so that each EG would produce at least the power available from the local source, independently from the state of charge of the local energy storage, whereas equal to $-\hat{p}_{S_n}^{\text{in}}$ during islanded mode, to allow EGs to provide non-positive active power injection when generation exceeds absorption.

7.3 Preprocessing

Concurrently with the operation of EGs, on the basis of the collected data the *master controller* determines:

- the total active and reactive power delivered by EGs along cycle ℓ :

$$p_{n,tot}(\ell) = \sum_{n=1}^N p_n(\ell) , \quad (7.4)$$

$$q_{n,tot}(\ell) = \sum_{n=1}^N q_n(\ell) ; \quad (7.5)$$

- the total active and reactive power absorbed within the microgrid along cycle ℓ by non-controllable units (i.e., non-controllable loads and DERs):

$$p_{l,tot}(\ell) = p_{MG}(\ell) + p_{n,tot}(\ell) , \quad (7.6)$$

$$q_{l,tot}(\ell) = q_{MG}(\ell) + q_{n,tot}(\ell) ; \quad (7.7)$$

which takes into account comprehensively the overall electrical load and the losses on the power lines.

- the estimated active power $\hat{p}_{l,tot}(\ell + 1)$ and reactive power $\hat{q}_{l,tot}(\ell + 1)$ that will be absorbed by microgrid loads in the next control cycle $\ell + 1$ and the reference for the total power $p_{n,tot}^*(\ell + 1)$, $q_{n,tot}^*(\ell + 1)$ to be delivered by EGs:

$$\begin{aligned} \hat{p}_{l,tot}(\ell + 1) &= p_{l,tot}(\ell) \\ p_{n,tot}^*(\ell + 1) &= \hat{p}_{l,tot}(\ell + 1) - p_{MG}^*(\ell + 1) \end{aligned} \quad , \quad (7.8)$$

$$\begin{aligned} \hat{q}_{l,tot}(\ell + 1) &= q_{l,tot}(\ell) \\ q_{n,tot}^*(\ell + 1) &= \hat{q}_{l,tot}(\ell + 1) - q_{MG}^*(\ell + 1) \end{aligned} \quad , \quad (7.9)$$

where $p_{MG}^*(\ell + 1)$ and $q_{MG}^*(\ell + 1)$ represent the assigned reference power flow for the microgrid for the next control cycle;

- the estimated total active power generated by EGs in cycle $\ell + 1$ and the corresponding upper and lower limits:

$$\hat{p}_{n,tot}(\ell + 1) = \sum_{n=1}^N \hat{p}_n(\ell + 1) \quad , \quad (7.10)$$

$$\hat{p}_{n,tot}^{\min}(\ell + 1) = \sum_{n=1}^N \hat{p}_n^{\min}(\ell + 1) \quad , \quad (7.11)$$

$$\hat{p}_{n,tot}^{\max}(\ell + 1) = \sum_{n=1}^N \hat{p}_n^{\max}(\ell + 1) \quad ; \quad (7.12)$$

- the estimated maximum reactive power that the active nodes can deliver in normal operation or in overloading condition in cycle $\ell + 1$:

$$\begin{aligned} \hat{q}_n^{\max}(\ell + 1) &= \sqrt{\hat{a}_n^2(\ell + 1) - \hat{p}_n^2(\ell + 1)} \\ \hat{q}_{n,tot}^{\max}(\ell + 1) &= \sum_{n=1}^N \hat{q}_n^{\max}(\ell + 1) \end{aligned} \quad , \quad (7.13)$$

$$\begin{aligned}\hat{q}_n^{\text{over}}(\ell+1) &= \sqrt{\hat{a}_n^{\text{over}2}(\ell+1) - \hat{p}_n^2(\ell+1)} \\ \hat{q}_n^{\text{over}}(\ell+1) &= \sum_{n=1}^N \hat{q}_n^{\text{over}}(\ell+1)\end{aligned}\quad (7.14)$$

Based on the global status of controllable DERs (i.e., EGs) obtained above, the MC regulates the power flow at the PCC to track the references p_{MG}^* , q_{MG}^* , given a pre-assigned power absorption profile from the main grid p_G^* , q_G^* . Accordingly, the power exchange at the terminals of the UI are:

$$\hat{p}_{UI}(\ell+1) = p_{MG}^*(\ell+1) - p_G^*(\ell+1), \quad (7.15)$$

$$\hat{q}_{UI}(\ell+1) = q_{MG}^*(\ell+1) - q_G^*(\ell+1). \quad (7.16)$$

While references p_G^* , q_G^* , that are actuated by the UI [219], are either set according to the negotiation on energy exchange with the DSO taking place in the tertiary control layer (see, e.g., Sec. 2.5.3 and [71]) or set to zero during the islanded operating mode, references p_{MG}^* , q_{MG}^* are locally adjusted by the MC according to the energy state of the UI, like, for example, in [39].

7.4 Setpoint Computation

The estimated quantities (7.8)-(7.14) are the input data for the control algorithm that drives the distributed EGs. In order to actuate it, the MC generates two control variables α_p and α_q (both ranging in the interval $[0, 2]$) that are finally *broadcasted* to all the EGs, namely, *applied to the whole microgrid*. Once new control coefficients are available, each EG autonomously compute its own set-point of power to be exchanged with the grid (p_n^* , q_n^*).

The following subsections describe how control variables α_p and α_q and set-points p_n^* and q_n^* are calculated, respectively, by the MC and the EGs.

7.4.1 Active Power Control

The active power is controlled by variable α_p , which is set by the MC depending on the operation mode. Four operating modes can be distinguished:

- 1) $p_{n,tot}^*(\ell + 1) < \hat{p}_{n,tot}^{\min}(\ell + 1)$ in this case, the loads are expected to absorb a total active power lower than the minimum power the active nodes can deliver. As a result, the MC sets:

$$\alpha_p = 0, \quad (7.17)$$

and each EG sets its active power reference $p_n^*(\ell + 1)$ at the minimum allowed value:

$$p_n^*(\ell + 1) = \hat{p}_n^{\min}(\ell + 1). \quad (7.18)$$

The power balance can temporarily be ensured by diverting the power in excess to the UI, which stores it in its energy storage device, as described in [38]. Of course, this situation can be sustained for a limited time, then loads and/or generators must be readjusted (e.g., MPPT's must be de-tuned so as to extract less power) to restore equilibrium.

- 2) $\hat{p}_{n,tot}^{\min}(\ell + 1) \leq p_{n,tot}^*(\ell + 1) < \hat{p}_{n,tot}(\ell + 1)$ the expected load power is lower than the generated power but the excess of generation can be temporarily diverted into distributed storage units. In this case, the UI does not contribute to power balance, and the MC sets the value of α_p as:

$$\alpha_p = \frac{p_{n,tot}^*(\ell + 1) - \hat{p}_{n,tot}^{\min}(\ell + 1)}{\hat{p}_{n,tot}(\ell + 1) - \hat{p}_{n,tot}^{\min}(\ell + 1)}, \quad 0 \leq \alpha_p < 1. \quad (7.19)$$

Correspondingly, each active node sets its active power reference as:

$$p_n^*(\ell + 1) = \hat{p}_n^{\min}(\ell + 1) + \alpha_p (\hat{p}_n(\ell + 1) - \hat{p}_n^{\min}(\ell + 1)). \quad (7.20)$$

- 3) $\hat{p}_{n,tot}(\ell + 1) \leq p_{n,tot}^*(\ell + 1) < \hat{p}_{n,tot}^{\max}(\ell + 1)$ the expected load power is higher than generated power but the difference can be supported, temporarily, by distributed energy storage. In this case, the UI does not contribute to power balance, and the MC sets the value of α_p as:

$$\alpha_p = 1 + \frac{p_{n,tot}^*(\ell + 1) - \hat{p}_{n,tot}(\ell + 1)}{\hat{p}_{n,tot}^{\max}(\ell + 1) - \hat{p}_{n,tot}(\ell + 1)}, \quad 1 \leq \alpha_p < 2. \quad (7.21)$$

Correspondingly, each active node sets its active power reference as:

$$p_n^*(\ell + 1) = \hat{p}_n(\ell + 1) + (\alpha_p - 1)(\hat{p}_n^{\max}(\ell + 1) - \hat{p}_n(\ell + 1)) . \quad (7.22)$$

- 4) $p_{n,tot}^*(\ell + 1) \geq \hat{p}_{n,tot}^{\max}(\ell + 1)$ the loads are expected to absorb a total power which is greater than the maximum power the active nodes can deliver. In this case the MC sets:

$$\alpha_p = 2 . \quad (7.23)$$

Correspondingly, each active node sets its active power reference as:

$$p_n^*(\ell + 1) = \hat{p}_n^{\max}(\ell + 1) . \quad (7.24)$$

The power balance can temporarily be ensured at the expense of the energy stored in the UI. After some time, of course, some of the loads and/or generators will have to be readjusted to restore the equilibrium.

By considering (7.18), (7.20), (7.22), (7.24), the control law for EGs written in a compact form is:

$$\begin{aligned} p_n^* &= \hat{p}_n^{\min}(\ell + 1) + \\ &+ (\hat{p}_n(\ell + 1) - \hat{p}_n^{\min}(\ell + 1)) \cdot \min(\alpha_p, 1) + \\ &+ (\hat{p}_n^{\max}(\ell + 1) - \hat{p}_n(\ell + 1)) \cdot \max(\alpha_p - 1, 0) . \end{aligned} \quad (7.25)$$

The control principle behind (7.25) is to make EGs to contribute to the power needs of the microgrid—measured at the microgrid’s PCC—in proportion of their *capability* of deliver or absorb power, thus allowing to obtain a uniform exploitation of available resources, without preventing EGs to pursue local objectives.

Voltage Magnitude Control

In order to maintain the voltage magnitudes at active nodes below a given threshold V^{\max} , for $n \in \{1, \dots, N\}$, EG_n applies a voltage control which is based only on local measure-

ments of the voltage magnitude. Precisely, EG_n continuously measures $|\underline{v}_n|$ and, in case an overvoltage occurs at some time instant \bar{t} , it adjusts the power injection according to the following rule:

$$\dot{p}_n(t) = -k_I (|\underline{v}_n(t)| - V^{\max}), \quad (7.26)$$

for $t \geq \bar{t}$, where $p_n(\bar{t}) = p_n^*$. In this case EG_n keeps applying the *purely local voltage control* described in (7.26) as long as the injected power p_n is lower than the power reference calculated as per (7.25) by using the received α_p and the *actual* [i.e., those indicated in (7.1) or (7.2)] parameters \hat{p}_n , \hat{p}_n^{\min} , and \hat{p}_n^{\max} .

The rationale behind this local control law is the following. If the node at which EG_n is connected is experiencing an overvoltage it means that node n cannot accept the power EG_n is injecting; accordingly, EG_n starts to decrease p_n as described in (7.26), relying on the fact that in a mainly resistive scenario, by decreasing the active power injection at grid nodes, the corresponding voltage magnitudes decrease as well. The effectiveness of this choice is discussed further in Sec. 7.5; whereas, a more formal analysis of the control scheme is provided in Sec. 7.6.

Observe also that, if there exists \tilde{t} such that $|\underline{v}(\tilde{t})| = V^{\max}$, then the power $p_n(\tilde{t})$ represents the power that the node where EG_n is connected can receive without experiencing overvoltages. In general, it might happen that, during the overvoltage condition, $\hat{p}_n((\ell + 1)T) < \hat{p}_n^{\min}(\ell + 1)$; in this case the overproduction $\hat{p}_n^{\min}(\ell + 1) - \hat{p}_n((\ell + 1)T)$ is assumed to be curtailed.

7.4.2 Reactive Power Control

The reactive power is controlled by variable α_q , which is set by the MC depending on the operation mode. There are two operation modes:

- 1) $q_{n,tot}^*(\ell + 1) \leq \hat{q}_{n,tot}^{\max}(\ell + 1)$ load requirements can be met by distributed EGs. In this case the MC sets:

$$\alpha_q = \frac{q_{n,tot}^*(\ell + 1)}{\hat{q}_{n,tot}^{\max}(\ell + 1)}, \quad 0 \leq \alpha_q \leq 1. \quad (7.27)$$

Correspondingly, each active node sets its reactive power reference as:

$$q_n^*(\ell + 1) = \alpha_q \cdot \hat{q}_n^{\max}(\ell + 1) . \quad (7.28)$$

- 2) $q_{n,tot}^*(\ell + 1) > \hat{q}_{n,tot}^{\max}(\ell + 1)$ loads requirement can only be met by overloading the EGs. In this case the MC sets:

$$\alpha_q = 1 + \frac{q_{n,tot}^*(\ell + 1) - \hat{q}_{n,tot}^{\max}(\ell + 1)}{\hat{q}_{n,tot}^{\text{over}}(\ell + 1) - \hat{q}_{n,tot}^{\max}(\ell + 1)} , \quad 1 < \alpha_q \leq 2 . \quad (7.29)$$

Correspondingly, each active node sets its reactive power reference as:

$$q_n^*(\ell + 1) = \hat{q}_n^{\max}(\ell + 1) + (\alpha_q - 1) (\hat{q}_n^{\text{over}}(\ell + 1) - \hat{q}_n^{\max}(\ell + 1)) . \quad (7.30)$$

7.4.3 Grid-Connected Mode: Active and Reactive Power Control

The strategy described above allows to control the microgrid's power absorption p_{MG} in both grid connected and islanded mode of operation. The different definition given in (7.2) and (7.1) is meant to guarantee the regulation of the power absorbed by the microgrid while operating islanded and the complete extraction of the power potentially available from renewables while operating grid connected.

Now, it is worth remarking that while operating connected to the mains the above control strategy can also be used to obtain a conventional grid-connected operation, where DERs simply inject the locally generated power in compliance with grid standards. This is obtained by the MC by setting $\alpha_p = 1$, so that the total power generated by DERs is injected into the grid. Local power needs (e.g., to restore the state of charge of the ES at the nominal value) continue to be taken into account by EGs, by correcting the estimates of generated power $\hat{p}_n(\ell + 1)$. In any case, the power balance is ensured by the utility grid.

As far as reactive power compensation is concerned, the UI first decides its contribution q_{UI} for the next control cycle. Then, it adjusts the total reactive power requested to the EGs

according to the equation:

$$q_{n,tot}^* (\ell + 1) = \hat{q}_{l,tot} (\ell) - q_{UI} (\ell + 1) . \quad (7.31)$$

Both for active and reactive power, the UI can also distribute the references differently in the three phases to compensate load unbalance, as described in [220].

7.5 Remarks on Voltage Control

To the end of controlling voltage profiles, the use of reactive power capabilities of DERs, which does not virtually involve additional costs, has been shown to be an effective and advantageous solution in medium-voltage (MV) networks [148, 221], where interconnection impedances are mainly inductive (i.e., characterized by low R/X ratios). However, this approach is not adequate in low-voltage networks, where, instead, interconnection impedances are typically resistive (i.e., R/X ratios are high) [222, 223]. Indeed, in networks with high R/X ratios, the reactive power injection that would be needed to counteract voltage rises caused by excessive active power injections may be so intense to lead to detrimental effects on the electrical infrastructure (e.g., overload of MV/LV transformer and distribution cables) and affect EPPs' reliability [224]. Therefore, approaches based on active power control, like the one in (7.26), fit better in high R/X networks, with the main drawback of the potential reduction in the overall power production, which, though, can be alleviated or even eliminated with small local accumulation.

About the effectiveness in counteracting overvoltages and undervoltage at grid nodes, in general, it is worth observing the following facts. One of the advantages given by distributed generation (with devices installed, ideally, at the consumers' premises) is to have active power generation closer to loads, namely, to the point where the power is consumed. This helps in compensating the voltage drops that would be naturally present due to the active power absorption by loads [44]. In addition, the control proposed herein coordinate the power injection by DERs (specifically, by EGs) so that it can adapt to the need of the microgrid's loads and to share the load among the generators in a fair way (specifically,

according to their power availability). This contributes in sustaining the grid voltage to avoid *undervoltage* conditions. On the other hand, *overvoltages* are an intrinsic issue of distributed generation in low-voltage grids. Indeed, overvoltages may occur due to congestion of distribution lines during periods of peak production from renewables, or can rise due to an excessive power injection by one or more distributed resources (e.g., in response to a remote control signal, like the one here referred to as α_p). These particular aspects, instead, are dealt with the local overvoltage control technique (7.26).

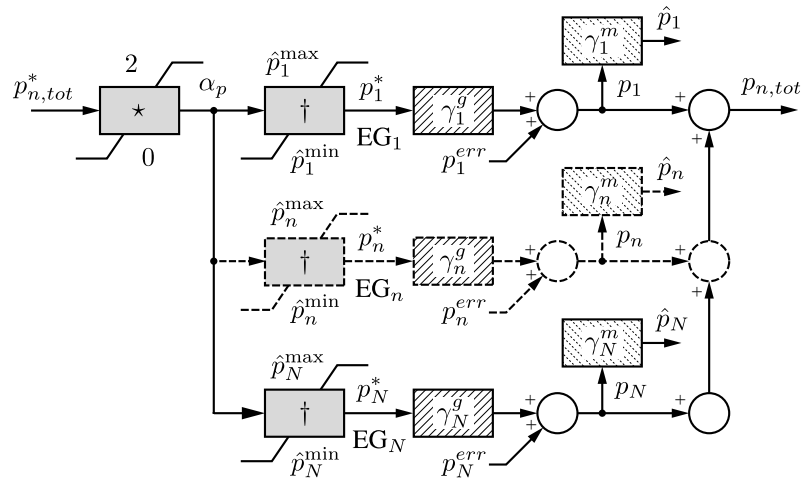
7.6 Control Analysis

In the devised control structure, an EG in overvoltage mode behaves as a non-controllable source, which does not respond to coefficient α_p ; such an EG can be considered as a load absorbing negative power. In addition, due to (7.3) and how the coefficient is calculated in (7.17), (7.19), (7.21), and (7.23), EGs in overvoltage mode do not affect the value of α_p . Therefore, the stability of the control system can be studied in two phases. The first considers the situation with no overvoltage occurrences; this allows to analyze the main operations of the power-based control, also taking into account the non-idealities of realistic application cases. The second phase considers a complete model of the system, including, specifically, the description of the distribution grid topology; this allows to analyze how the overvoltage control affects the dynamics of the system.

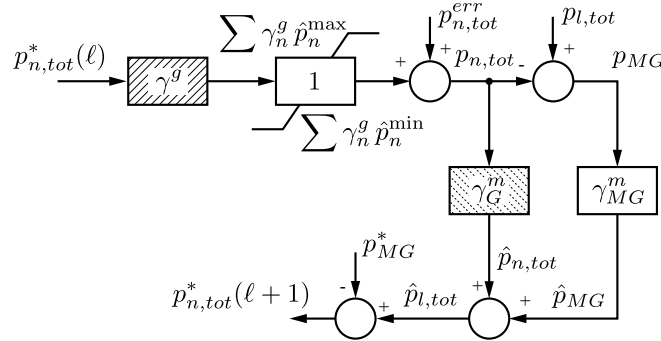
7.6.1 Power-Based Principle Analysis

A simplified block diagram representing the main operations of the power-based control for what concerns active power balance is shown in Fig. 7-2.⁴ Gain errors and off-set errors are included to take into account the main non-idealities of a realistic application case. In general, gain errors affect the loop gain of the feedback system and have to be considered to assess system stability, whereas off-set errors have to be taken into account to analyze its steady-state accuracy in regulating the controlled quantities. In Fig. 7-2(a), variables γ_n^g and p_n^{err} represent the gain and off-set errors made by EG_n in producing the assigned

⁴A corresponding scheme can be derived for reactive power control.



(a) Generation of power commands.



(b) Calculation of power references.

Figure 7-2: Simplified model of the power-based control. Symbol \star represents one of the equations (7.17), (7.19), (7.21), or (7.23); symbol \dagger represents one of the equations (7.18), (7.20), (7.22), or (7.24).

power reference p_n^* ; γ_n^m and γ_{MG}^m represent the gain errors of measurement instruments, while off-set errors in measurements are, for now, neglected. On the base of Fig. 7-2(a), the simplified model of Fig. 7-2(b) can be drawn, that is used for the analysis of the power-based control stability.

By employing the block diagram of Fig. 7-2(b) it is possible to derive the discrete time transfer function between the total absorbed power $p_{l,tot}$ and the reference $p_{n,tot}^*$. By neglecting the reference input p_{MG}^* , since it varies very slowly, as mentioned in the last paragraph of Sec. 7.3, it results:

$$p_{n,tot}^*(z) = \frac{\gamma_{MG}^m}{z + \gamma^g (\gamma_G^m - \gamma_{MG}^m)} p_{l,tot}(z). \quad (7.32)$$

Equation (7.32) shows that, if the system is ideal (i.e., γ_n^g , γ_n^m , γ_{MG}^m are equal to one and p_n^{err} is equal to zero) then the power reference EGs are committed to is going to track the total absorbed power in the microgrid, with one control cycle delay; secondly, that the stability condition for active power reference generation, in general, can be expressed as: $|\gamma^g (\gamma_G^m - \gamma_{MG}^m)| < 1$, which can easily be met by any commercial power meter. This proves a stable control operation for the operating modes 2) and 3) referred to in Sec. 7.4.1.

The diagrams in Fig. 7-2 also highlight that, if the power requested by the load exceeds the total power capability of EGs, the coefficient α_p seamlessly saturates to its upper limit, so that each EG continuously delivers the maximum power that is locally available (p_n^{\max}). When the opposite situation occurs, i.e., the minimum injectable power from EGs is higher than the load power, the coefficient α_p is automatically saturated at its lower limit and each EG continuously delivers the minimum power (p_n^{\min}). Because the control system operates on a cycle by cycle basis, with no memory of the grid state during previous cycles, a stable control operation is guaranteed, as well, for the operating modes 1) and 4) referred to in Sec. 7.4.1.

For what concerns the regulation accuracy of the power flow at the PCC, let's first observe that:

$$p_{MG}(\ell) = p_{l,tot}(\ell) - \gamma^g \hat{p}_{n,tot}^*(\ell) - p_{n,tot}^{err}(\ell), \quad (7.33)$$

where p_{MG} is shared among the UI (p_{UI}) and the mains (p_{GRID}) [equations (7.15)-(7.16)]

according to the negotiation on energy exchange with the DSO taking place in the tertiary control layer. From (7.33), the power flow at the PCC is equal to the power reference p_{MG} minus the error introduced by EGs. This error can be canceled by the MC, for example, by employing a local integrative regulator to properly modulate the power term p_{MG} [28]. Similarly, the fluctuations in local power production can be modeled as exogenous inputs, that only affect the limits \hat{p}_n^{\min} and \hat{p}_n^{\max} and do not impair the stability of the system. The limits are acquired and processed by the MC at each control cycle, allowing to accordingly update the control commands to EGs, so as to account for the actual generation profile. Finally, although temporary mismatches (i.e., lasting few line cycles) among the effectively generated power and its estimate can have an effect on the injected power, this can be limited by a proper design of EG hardware. In any case, DC-link voltage deviations caused by abrupt changes in operating conditions, which may affect primarily voltage-driven inverters [13], are attenuated in the considered EG structure thanks to the adopted approach current-driven [14].

7.6.2 System Analysis

To the purpose of investigating the stability of the proposed control scheme, let's consider a power system where power injections from distributed EGs are driven by the power-based control with the automatic overvoltage limitation (7.26). At the generic m -th node an EG and a load, absorbing a constant active power (P_{Lm}), can be connected. The load may represent also a non-controllable source, in this case $P_{Lm} < 0$. The voltage phasor at the m -th node is indicated as v_m .

In this situation, microgrid nodes can be grouped as follows:

- \mathcal{L} is the set of L passive nodes injecting or absorbing the total power that is produced or consumed locally. These can be modeled as constant power sources injecting:

$$p_m^{\mathcal{L}} = -P_{Lm}, \quad (7.34)$$

- \mathcal{K} is the set of k active nodes, not affected by overvoltage conditions, injecting or ab-

sorbing power under the guidance of the power-based control. These can be modeled as controlled power sources injecting:

$$p_m^{\mathcal{K}} - P_{Lm} = P_m^{\mathcal{K}}(\alpha_p, \hat{p}_m^{\min}, \hat{p}_m, \hat{p}_m^{\max}) - p_{Lm}, \quad (7.35)$$

- \mathcal{H} is the set of h active nodes where an overvoltage condition persists. For these nodes the active power injection is locally calculated to control the maximum measured node voltage amplitude. These nodes behave as controlled power sources with the control law:

$$p_m^{\mathcal{H}} - P_{Lm} = -\frac{k_I}{s} (|\underline{v}_m| - V^{\max}) - P_{Lm}, \quad (7.36)$$

- node 0, at the PCC, is characterized by a fixed nominal voltage $\underline{v}_0 = V_N e^{j0}$. The power absorption at this node guarantees the power balance of the system.

For the stability analysis, it is convenient to linearize the relation between voltage magnitudes and power injections at grid nodes. By employing the results attained in [49], voltage magnitudes at grid nodes may be modeled with the following approximated and linearized expression:

$$|\underline{v}| = V_0 \mathbf{1} + \frac{1}{V_0} \Re(e^{j\theta} \mathbf{X} \mathbf{a}^T) + \frac{d(V_0)}{V_0^2}. \quad (7.37)$$

In (7.37), \underline{v} is the vector of node voltages, V_0 is the voltage amplitude around which the model is linearized, \mathbf{X} is a symmetric and positive semidefinite matrix, $\mathbf{1}$ is a column vector with all ones, \mathbf{a}^T is the transpose of the complex power vector $\mathbf{a} = \mathbf{p} + j\mathbf{q}$ of node power injections, θ is the phase of the grid impedance per unit of length, $d(V_0)/V_0^2$ is a bounded function when $V_0 \rightarrow \infty$. \mathbf{X} carries the information on the grid topology and the interconnecting impedances. To ease the exploitation of symmetries, it is assumed in the following that nodes are arranged as $\mathbf{x} = (x_0, x_1^{\mathcal{L}}, x_2^{\mathcal{L}}, \dots, x_l^{\mathcal{K}}, x_1^{\mathcal{K}}, x_2^{\mathcal{K}}, \dots, x_k^{\mathcal{K}}, x_1^{\mathcal{H}}, x_2^{\mathcal{H}}, \dots, x_h^{\mathcal{H}})^T = (x_0, \mathbf{x}^{\mathcal{L}}, \mathbf{x}^{\mathcal{K}}, \mathbf{x}^{\mathcal{H}})^T$, where x is a generic electrical quantity.

Focusing on active power flows, neglecting the term $d(V_0)/V_0^2$, and assuming $\theta = 0$ (exploiting the LV networks' property of showing high R/X ratios), equation (7.37) may

be rewritten as:

$$|\underline{v}| = V_0 \mathbf{1} + \frac{1}{V_0} \mathbf{X} \mathbf{p}. \quad (7.38)$$

For what concerns the elements of vector \mathbf{p} in the situation described above, the power absorption at node 0 can be modeled as the difference between the total absorbed and generated power within the microgrid:

$$p_0 = \sum_{n=1}^l p_n^{\mathcal{L}} - \sum_{n=1}^k p_n^{\mathcal{K}} - \sum_{n=1}^h p_n^{\mathcal{H}}. \quad (7.39)$$

The power generation of nodes in \mathcal{K} is proportional to microgrid's power needs, considering the local power generation constant, because it depends on relatively slowly varying phenomena (e.g., weather condition and the state of charge of local energy storage). Indicating with values $m_1, \dots, m_k \in \mathbb{R}^+$, $m_n < 1$, the proportionality factors of the power contribution from the nodes in \mathcal{K} , it is possible to write:

$$p_n^{\mathcal{K}} = m_n \left(p_0 + \sum_{n=1}^k p_n^{\mathcal{K}} \right). \quad (7.40)$$

Finally, power generation of nodes in \mathcal{H} behaves with the control law (7.36):

$$p_n^{\mathcal{H}} = -\frac{k_I}{s} (|\underline{v}_n| - V_0), \quad (7.41)$$

where V_0 should assume in this case the value of the maximum voltage V^{\max} .

Therefore, for a specific configuration of absorption and generation, the total injected power at grid nodes can be represented as in (7.44).

Stability Analysis

The analysis is now focused on power absorption at non-passive nodes. In the following, vectors referring to this set of nodes are denoted with a tilde accent (e.g., $\tilde{\mathbf{x}}$). Considering, $\tilde{\mathbf{p}} = (\mathbf{p}_0, \mathbf{p}^{\mathcal{K}}, \mathbf{p}^{\mathcal{H}})^T$, we can observe that:

$$\tilde{\mathbf{p}} = \mathbf{A} \tilde{\mathbf{p}} + \mathbf{B} \mathbf{p}^{\mathcal{L}} + \frac{1}{s} \mathbf{C} (|\tilde{\underline{v}}| - |\tilde{v}_0|), \quad (7.42)$$

$$\mathbf{p} = \begin{bmatrix} 0 & 1 & \cdots & 1 & 1 & \cdots & 1 & 1 & \cdots & 1 \\ 0 & 0 & \cdots & 0 & 0 & \cdots & 0 & 0 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 0 & 0 & \cdots & 0 & 0 & \cdots & 0 \\ m_1 & 0 & \cdots & 0 & m_1 & \cdots & m_1 & 0 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ m_k & 0 & \cdots & 0 & m_k & \cdots & m_k & 0 & \cdots & 0 \\ 0 & 0 & \cdots & 0 & 0 & \cdots & 0 & 0 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 0 & 0 & \cdots & 0 & 0 & \cdots & 0 \end{bmatrix} \begin{bmatrix} p_0 \\ p_1^{\mathcal{L}} \\ \vdots \\ p_l^{\mathcal{L}} \\ p_1^{\mathcal{K}} \\ \vdots \\ p_k^{\mathcal{K}} \\ p_1^{\mathcal{H}} \\ \vdots \\ p_h^{\mathcal{H}} \end{bmatrix} \tag{7.44}$$

$$- \begin{bmatrix} 0 & 0 & \cdots & 0 & 0 & \cdots & 0 & 0 & \cdots & 0 \\ 0 & 0 & \cdots & 0 & 0 & \cdots & 0 & 0 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 0 & 0 & \cdots & 0 & 0 & \cdots & 0 \\ 0 & 0 & \cdots & 0 & 0 & \cdots & 0 & 0 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 0 & 0 & \cdots & 0 & 0 & \cdots & 0 \\ 0 & 0 & \cdots & 0 & 0 & \cdots & 0 & \frac{k_I}{s} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 0 & 0 & \cdots & 0 & 0 & \cdots & \frac{k_I}{s} \end{bmatrix} \begin{bmatrix} 0 \\ |v_1^{\mathcal{L}}| - V_0 \\ \vdots \\ |v_l^{\mathcal{L}}| - V_0 \\ |v_1^{\mathcal{K}}| - V_0 \\ \vdots \\ |v_k^{\mathcal{K}}| - V_0 \\ |v_1^{\mathcal{H}}| - V_0 \\ \vdots \\ |v_h^{\mathcal{H}}| - V_0 \end{bmatrix} - \begin{bmatrix} 0 \\ P_{L1} \\ \vdots \\ P_{Ll} \\ P_{Ll+1} \\ \vdots \\ P_{Ll+k+1} \\ P_{Ll+k+2} \\ \vdots \\ P_{Ln} \end{bmatrix}$$

where $\mathbf{p}^{\mathcal{L}}$ is the total load in the microgrid and:

$$\mathbf{A} = \begin{bmatrix} 0 & -\mathbf{1}_{\mathbf{k}}^T & -\mathbf{1}_{\mathbf{h}}^T \\ m & m\mathbf{1}_{\mathbf{k}}^T & \mathbf{O}_{\mathbf{kh}} \\ \mathbf{0}_{\mathbf{h}} & \mathbf{O}_{\mathbf{hk}} & \mathbf{O}_{\mathbf{hh}} \end{bmatrix} \quad \mathbf{B} = \begin{bmatrix} 1 \\ \mathbf{0}_{\mathbf{k}} \\ \mathbf{0}_{\mathbf{h}} \end{bmatrix} \quad \mathbf{C} = \begin{bmatrix} 0 & \mathbf{0}_{\mathbf{k}} & \mathbf{0}_{\mathbf{h}} \\ \mathbf{0}_{\mathbf{k}} & \mathbf{O}_{\mathbf{hk}} & \mathbf{O}_{\mathbf{hk}} \\ \mathbf{0}_{\mathbf{h}} & \mathbf{O}_{\mathbf{hk}} & -k_I I_{\mathbf{h}} \end{bmatrix}. \quad (7.43)$$

In (7.43), $\mathbf{1}_i$ denotes the $i \times 1$ column vector with all ones, $\mathbf{m} \in \mathbb{R}^{k \times 1}$, and $\mathbf{O}_{ij} \in \mathbb{R}^{i \times j}$ denotes the matrix with all zeros.

From (7.42) it is possible to write $\tilde{\mathbf{p}}$ as:

$$\tilde{\mathbf{p}} = (\mathbf{I} - \mathbf{A})^{-1} \mathbf{B} \mathbf{p}^{\mathcal{L}} + \frac{1}{s} (\mathbf{I} - \mathbf{A})^{-1} \mathbf{C} (|\tilde{\mathbf{v}}| - |\tilde{\mathbf{v}}_0|), \quad (7.45)$$

and, finally, using (7.45) in (7.38) for nodes $\{0, \mathcal{K}, \mathcal{H}\}$:

$$\begin{aligned} s (|\tilde{\mathbf{v}}| - |\tilde{\mathbf{v}}_0|) &= \frac{1}{V_0} \tilde{\mathbf{X}} (\mathbf{I} - \mathbf{A})^{-1} \mathbf{C} (|\tilde{\mathbf{v}}| - |\tilde{\mathbf{v}}_0|) + \\ &\quad \frac{s}{V_0} \tilde{\mathbf{X}} (\mathbf{I} - \mathbf{A})^{-1} \mathbf{B} \mathbf{p}^{\mathcal{L}}, \end{aligned} \quad (7.46)$$

which represents the state equation of the linearized system with state matrix:

$$1/V_0 \tilde{\mathbf{X}} (\mathbf{I} - \mathbf{A})^{-1} \mathbf{C}. \quad (7.47)$$

7.7 Application Example

The proposed power-based control technique has been tested for different network topologies and operating conditions, both static and dynamic, in grid-connected and islanded mode. To clearly illustrate the control features and also allow a viable laboratory implementation for comparison purposes, let's consider the simple test case shown in Fig. 7-3. It comprises two EGs, one load, and the UI.

The considered power system is low-voltage and the parameters of the adopted power electronic interfaces, PV sources, and storage units are those of commercial devices suited for residential applications. Distribution grid parameters are reported in Table 7.1, while

Table 7.1: Distribution grid parameters

| Parameter | Symbol | Value | |
|------------------------|------------------------|----------------|----------|
| Grid voltage | V_G | 230 | V |
| Grid frequency | f_G | 50 | Hz |
| Max. voltage deviation | $\Delta v_{\%}^{\max}$ | 4.0 | % |
| B_1 impedance | Z_{B1} | $0.17 + j0.04$ | Ω |
| B_2 impedance | Z_{B2} | $0.26 + j0.06$ | Ω |
| B_3 impedance | Z_{B3} | $0.70 + j0.16$ | Ω |
| Load power factor | PF | 0.95 | - |

Table 7.2: First energy gateway parameters (EG #1)

| Parameter | Symbol | Value | |
|---------------------------|-----------------------------|-------|-----|
| EG power rating | a_{EG1} | 4.2 | kVA |
| EG overload power rating | a_{EG1}^{over} | 4.6 | kVA |
| EG nominal efficiency | η_{EG1} | 0.95 | - |
| PV nominal power rating | P_{PV1} | 4.0 | kW |
| ES capacity | E_{ES1} | 3.6 | kWh |
| ES max discharging power | $p_{S1}^{\text{out}(\max)}$ | 2.0 | kW |
| ES max recharging power | $p_{S1}^{\text{in}(\max)}$ | 1.0 | kW |
| ES charging efficiency | $\eta_{ES1,Rec}$ | 0.92 | - |
| ES discharging efficiency | $\eta_{ES,Disc}$ | 0.92 | - |

Table 7.3: Second energy gateway parameters (EG #2)

| Parameter | Symbol | Value | |
|---------------------------|-----------------------------|-------|-----|
| EG power rating | a_{EG2} | 5.0 | kVA |
| EG overload power rating | a_{EG2}^{over} | 5.4 | kVA |
| EG nominal efficiency | η_{EG2} | 0.95 | - |
| PV nominal power rating | P_{PV2} | 4.0 | kW |
| ES capacity | E_{ES2} | 5.4 | kWh |
| ES max discharging power | $p_{S2}^{\text{out}(\max)}$ | 3.0 | kW |
| ES max recharging power | $p_{S2}^{\text{in}(\max)}$ | 1.5 | kW |
| ES charging efficiency | $\eta_{ES2,Rec}$ | 0.92 | - |
| ES discharging efficiency | $\eta_{ES,Disc}$ | 0.92 | - |

is automatically curtailed or, in case of ES availability, stored locally.

Active Power Profiles

Fig. 7-4, Fig. 7-5, and Fig. 7-6 show the behavior of the measured active power flows for the considered cases in response to given generation and absorption profiles.

In *Case A*, Fig. 7-4, EG_1 and EG_2 exchange with the grid only the active power produced by the PV sources, without taking into account any overvoltage constraint at grid nodes. Then, the power drawn from the PCC is equal to the total power absorbed by the load (plus losses) minus the total power generated by the PV sources. Consequently, the power flow at the PCC shows the same variability of generation and absorption profiles.

In *Case B*, Fig. 7-5, the power-based control is active. For what concerns the active power injection, when voltage magnitudes of active nodes are within nominal values, the active power flow behaviors in *Case B* and *Case A* are identical. A different situation is established for reactive power. Indeed, the power-based control instructs the EGs to completely compensate the net reactive power produced within the microgrid, thus causing a constant zero reactive power exchange at the PCC. Further details are given with the discussion of Table 7.4.

In *Case C*, Fig. 7-6, it is shown the effect on microgrid operation of the integration of ES. ES enables an efficient control of the active power injection from EGs. In fact, the active power injection from EGs is now driven by the needs of the loads through the supervision of the master controller. This reflects on the active power exchanged at the PCC, which appears smoother than in *Case A* and *Case B*, thanks to the inherent *peak shaving* capability of the microgrid.

Finally, a comparison between *Case B* and *Case C* show the effect of the overvoltage limitation by dynamic active power control, that causes the reduction in EG_2 power generation, needed to fulfill the imposed grid voltage magnitude constraint (see Table 7.2, parameter $\Delta v_0^{\%(\max)}$).

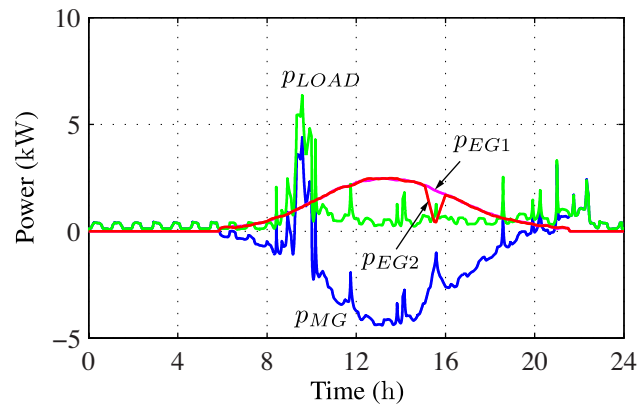


Figure 7-4: Active power profiles without power-based control (*Case A*).

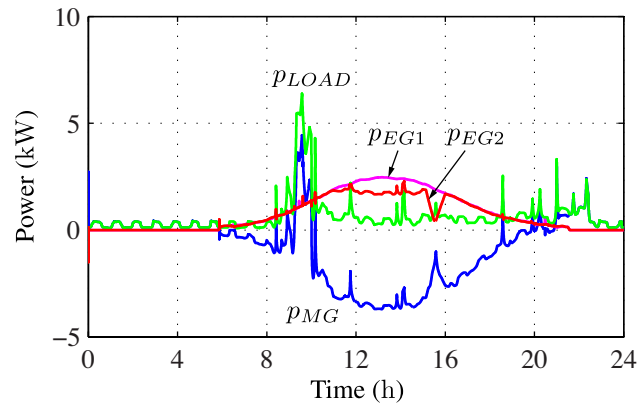


Figure 7-5: Active power profiles with power-based control (*Case B*).

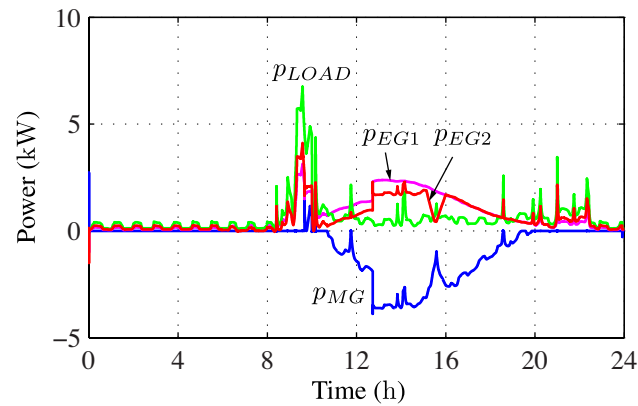


Figure 7-6: Active power profiles with power-based control and energy storage (*Case C*). Note how the peak in power demand, at 9:00 hours, is eliminated.

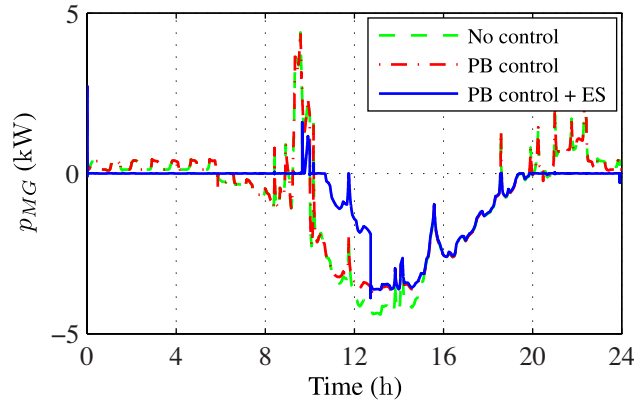


Figure 7-7: Active power at PCC.

Power Flow at PCC

Fig. 7-7 shows the behavior of the active power flow through the PCC for the considered cases. As noticed in the previous paragraph, the lower variance of the power flow at PCC happens when the power-based control is active and EGs are equipped with energy storage units. In Fig. 7-7, the fluctuations in load power absorption during intervals $[0, 8]$ h and $[20, 24]$ h are completely absorbed by EGs thanks to the available energy storage. Similarly, the peak of absorption occurring at 9 h is properly redistributed among EGs (see Fig. 7-6) and effectively reduced at the PCC.

Distributed ES also contributes to partially absorb the overproduction from PV sources, in the interval $[10, 13]$ h, until the completion of recharge cycle.

Distribution Losses

Fig. 7-8 shows the obtained distribution losses for the considered cases. The proposed power-based control formulation inherently compensates unwanted reactive power flows within the grid in a distributed fashion. This is known to be beneficial in terms of distribution losses [225]. Besides, the distributed energy storage, relevant for *Case C*, enables the active power control, and thus further improves the loss count by reducing circulating currents. The resulting effect on distribution losses can be noticed in interval $[10, 12]$ h of Fig. 7-8, where distribution losses in *Case C* are significantly lower than those measured in *Case A* and *Case B*.

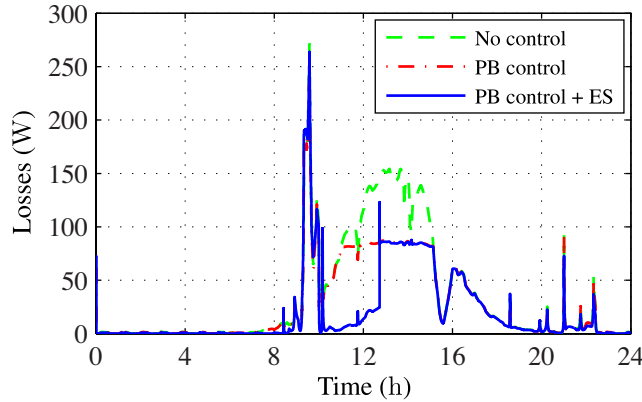


Figure 7-8: Distribution power losses over the grid.

Voltage Deviations at Grid Nodes

As discussed in Sec. 7.5, low-voltage distribution lines are mainly resistive, therefore, the active power flow significantly affects voltage amplitudes at grid nodes. Indeed, during periods of peak production from renewables, undesirable voltage deviations from nominal values can be registered due to abnormal active power injection. In the considered simulation setup, overvoltage conditions are automatically detected and managed locally by the active nodes by regulating dynamically the active power injected into the grid, as per (7.26).

Fig. 7-9 shows the voltage deviation at the point of connection of EG_2 . This node is more affected by these phenomena because it is the farthest from the PCC. In particular, the figure shows how the overvoltage control feature integrated into the control scheme allows an accurate and precise limitation of voltage magnitude at critical nodes. In the considered case, the power that cannot be injected into the grid due to overvoltage limitations is stored in the local accumulators, if compatible with the corresponding state of charge, otherwise the generation is curtailed by acting on the power point tracker, as, for example, in [219, 226].

Indeed, to meet the $\Delta v_{\%}^{\max}$ constraint can necessarily lead to a reduced power production from renewables in grids where the distribution lines have high R/X ratios. Fig. 7-10 reports the profile of the total maximum power that can be ideally extracted from PV sources and the actual total power production obtained in *Case B* and *Case C*. Since the power injection is limited during an overvoltage condition, the power in excess is totally

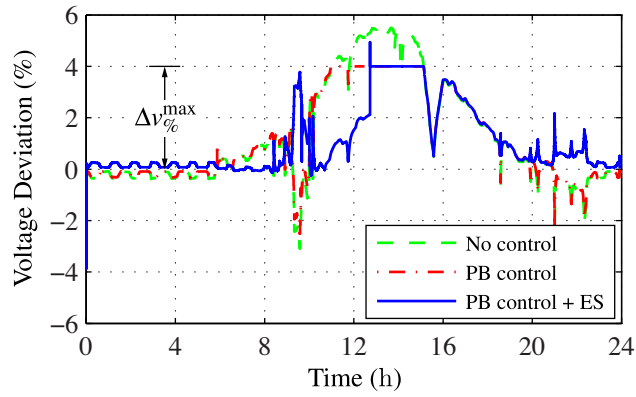


Figure 7-9: Voltage deviation at EG_2 node.

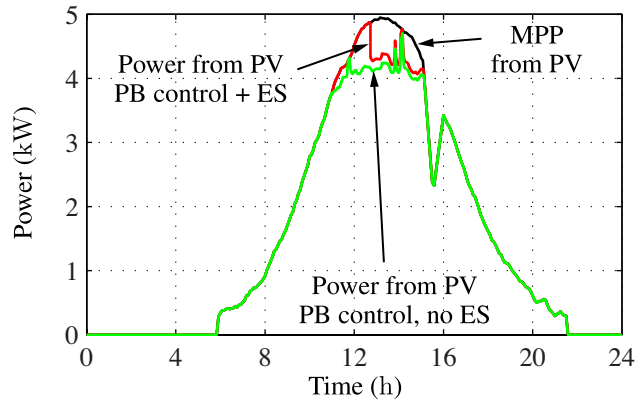


Figure 7-10: Total power production from PV sources.

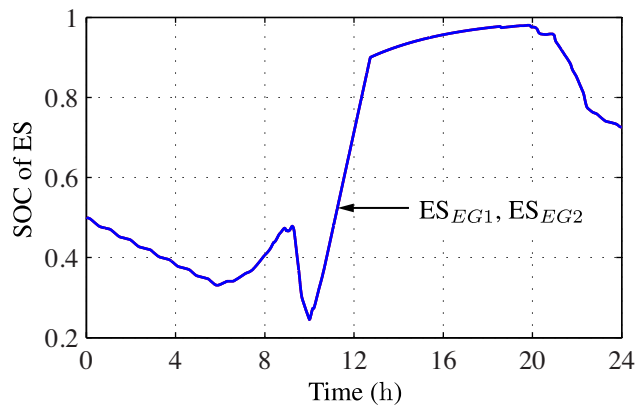


Figure 7-11: State of charge of energy storage devices (*Case C*).

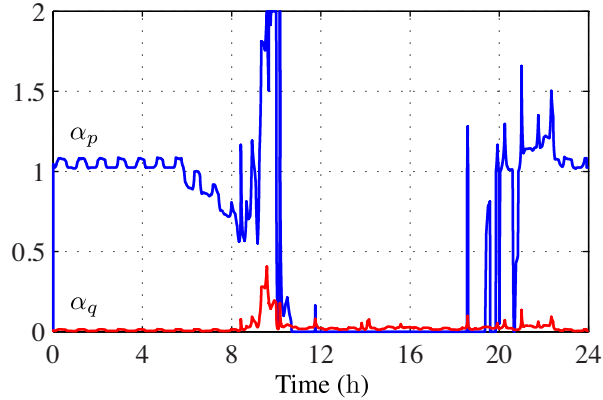


Figure 7-12: Behavior of coefficients α_p and α_q (*Case C*).

curtailed in *Case C*, whereas, in *Case B*, it is curtailed for only the portion that cannot be stored in the local ES. Fig. 7-11 shows the corresponding SOC of the ES of the two energy gateways; due to the proportional contribution from the EGs, SOC behaviors are similar.

The behavior of coefficients α_p and α_q along the considered simulation scenario is reported in Fig. 7-12, just for *Case C*. In *Case B* similar behaviors are obtained for what concerns the coefficient α_q , while the coefficient α_p assumes only the values corresponding to the operating modes 1) and 4) of Sec. 7.4.1, due to the absence of storage devices. In this last case, the power output from EGs are steadily equal to the maximum power that can be generated locally while complying with the overvoltage constraint $\Delta v_{\%}^{\max}$.

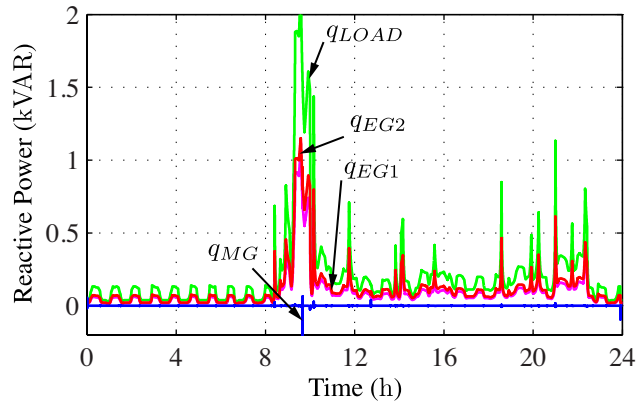
Performance Indexes

In order to emphasize the main results illustrated so far, Table 7.4 reports some performance indexes applied to the considered application example. In particular, the total produced energy, the energy dissipated in distribution lines, the overvoltage measured at grid nodes, and the power factor measured at the PCC are reported. The following aspects are remarked.

- The measured distribution losses in *Case B* are reduced by 20% with respect to *Case A*. A further reduction by 25% can be achieved with the integration of energy storage devices at active nodes (*Case C*). The maximum registered overvoltage stays within the programmed 4% limit (see Table 7.1) when the corresponding control functionality is active, notably, in *Case B* and *Case C*. On the other hand, if no provisions are taken, *Case A* reveals a maximum reached overvoltage of 5.5%.

Table 7.4: Performance indexes computed at microgrid PCC

| Parameter | Case A | Case B | Case C |
|--------------------------------|------------|------------|-----------------|
| | No Control | PB Control | PB control + ES |
| Produced Energy (kWh) | 36.5 | 34.1 | 34.2 |
| Distribution Loss (kWh) | 0.83 | 0.65 | 0.47 |
| v_{EG1} max overvoltage (%) | 1.4 | 1.2 | 1.2 |
| v_{LOAD} max overvoltage (%) | 2.4 | 1.8 | 1.8 |
| v_{EG2} max overvoltage (%) | 5.5 | 4.0 | 4.0 |

**Figure 7-13:** Reactive power contributions from EG_1 , EG_2 , and the PCC, together with the absorbed load power.

- In the considered application example, the power-based control accomplishes the full compensation of the reactive power produced by the loads, achieving a unity power factor measured at the PCC. Fig. 7-13 shows the obtained share of reactive power between EG_1 , EG_2 , and the PCC, together with the reactive power absorbed by the load.
- Thanks to the effective management of the generated and stored energy performed by the proposed control scheme, a reduction of only 6 % in the total produced energy can be noticed in spite of the stringent overvoltage limitation of 4 % with respect to the nominal value V_G .

7.8 Summary

In this chapter an algorithm, called power-based control, suitable to be integrated in the master/slave architecture (see Fig. 5-2) to control distributed energy resources in low-voltage microgrids is presented and analyzed. The control technique only requires non-time-critical power data to be transferred from the active nodes to a centralized controller through a narrowband communication link; the centralized controller, in turn, broadcasts active and reactive power set-points for all the active nodes, thus fitting the control framework introduced in Ch. 5. As opposed to the approaches discussed in Sec. 4.2, the control algorithm does not require specific knowledge on the controlled plant (e.g., grid parameters, grid topology), constituting, therefore, a *model-free* approach for the control of DERs in microgrids.

In summary, the power-based control shows the following features:

- no need of plant's models;
- no need of measures from passive nodes;
- no circulation currents among generators;
- light calculation and communication requirements;
- prompt regulation of the power flow at the interface between the microgrid and the mains;
- regularization of voltage profiles along distribution lines.

Chapter 8

Test Case

This chapter reports the experimental results concerning the operation of the proposed master/slave architecture, described in Ch. 5, with the power-based control, described in Ch. 7. Firstly the microgrid testbed that has been implemented and used to produce the experimental data is described. In the considered prototype, the utility interface, described in Sec. 5.2, regulates the current at the microgrid's PCC, whereas the controllable distributed energy resources, namely, the energy gateways, introduced in Sec. 5.1, contribute to the power needs of the microgrid according to their availability of generating power. In the second part, the experimental results are discussed, considering: power sharing with the power-based control, connection to the main grid, management of overvoltage conditions, transition to the islanded operation.

8.1 Microgrid Laboratory Testbed

To demonstrate the operation of the proposed concepts, the laboratory-scale testbed described in Fig. 8-1 has been implemented. The testbed has been employed to validate the most critical aspects of the proposed control algorithms and techniques, presented in [81, 113, 180, 192, 194, 195, 227–231]. The final testbed appears as in Fig. 8-2 and Fig. 8-3.

In the following, the proposed master/slave architecture [81] with the power-based control [228] is specifically addressed by means of the microgrid prototype schematically shown in Fig. 8-4, which displays a particular configuration of the laboratory testbed of

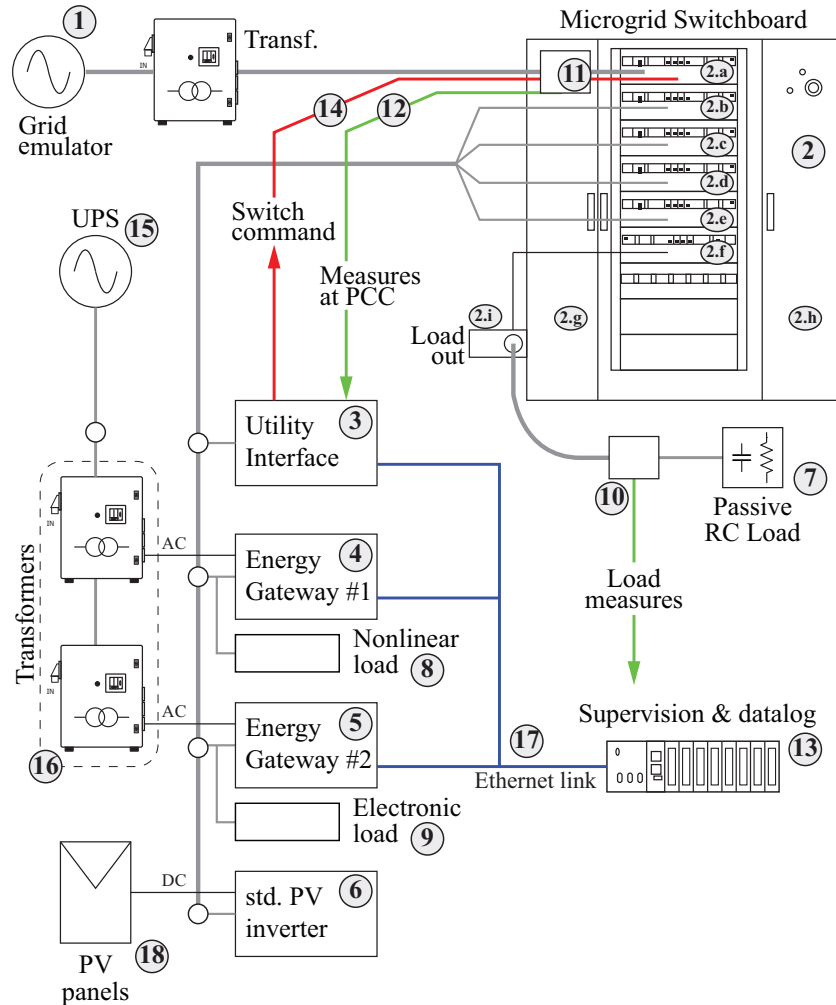


Figure 8-1: Diagram of the experimental testbed—**1.** 80 kVA grid emulator; **2.** Microgrid switchboard with: 2.a grid emulator channel, 2.b first source channel, 2.c second source channel, 2.d third source channel, 2.e fourth source channel, 2.f load channel, 2.g switchboard input panel, 2.h switchboard connection panel, 2.i load plug; **3** Utility Interface; **4.** Energy gateway #1; **5.** Energy gateway #2; **6.** Standard photovoltaic inverter; **7.** Passive *RC* load; **8.** Non-linear load; **9.** Electronic load; **10.** V-I meter; **11.** V-I meter, wide bandwidth; **12.** Digital communication channel for acquisition of measurements at the PCC; **13.** Supervision and data-log unit (cRIO-9082); **14.** UI-driven grid connection switch command; **15.** Three-phase UPS 10 kW; **16.** Isolation transformers; **17.** Ethernet communication link; **18.** PV panels (400 V, 3 kW).

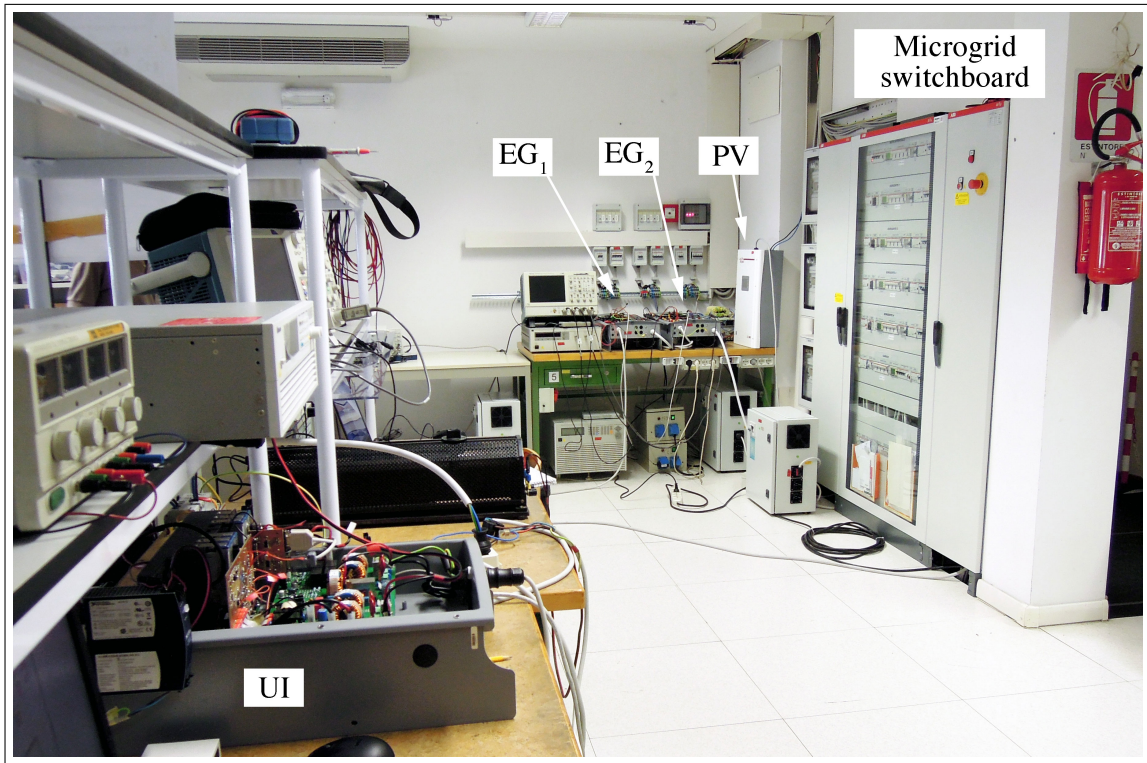


Figure 8-2: Photo of the implemented microgrid testbed (more details in Fig. 8-3).

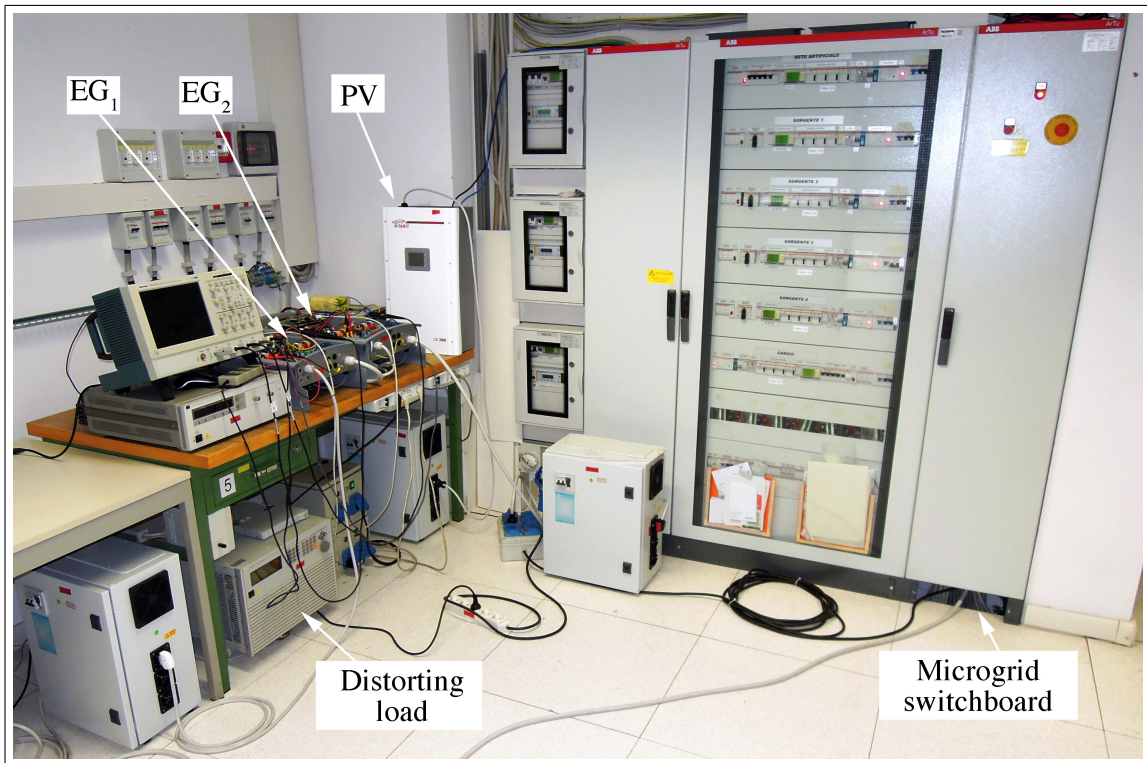


Figure 8-3: Photo of the implemented microgrid testbed (details of Fig. 8-2).

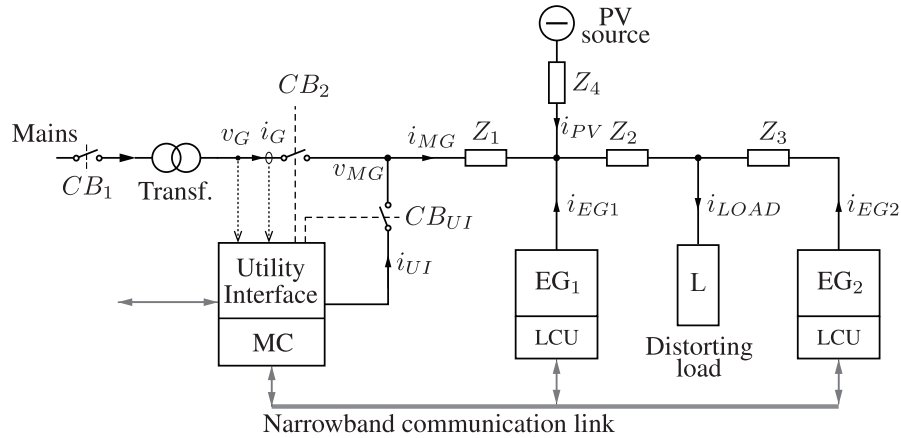


Figure 8-4: Schematic of the laboratory microgrid prototype.

Fig. 8-1. In the prototype, the mains are emulated by an 80 kVA three-phase bidirectional AC/AC power supply, the UI (see Sec. 5.2) and the two EG are implemented by employing commercial 3 kVA inverters, properly modified. The distribution grid topology and interconnection of electrical sources and loads are provided by a custom switchboard, which allows flexible configuration of microgrid topologies by giving access to various sections of low-voltage distribution cables.

National Instruments Reconfigurable Input/Output (RIO) platforms are employed for control, monitoring, and emulation purposes. The UI is controlled by a cRIO system, while each EG is controlled by a GPIC system; further details on the adopted prototyping framework are reported in Sec. 3.2.1. A TCP/IP Ethernet network using the National Instruments Publish-Subscribe Protocol (NI-PSP) provides the information exchange among the UI and the EG units. The main parameters of the prototype are listed in Table 8.1. The control techniques have been implemented by taking advantage of the developing methodology and prototyping approach presented in Ch. 3 and proposed in [232].

8.2 Experimental Results

The microgrid laboratory prototype described above has been employed to validate experimentally the master/slave architecture with the power-based control. The microgrid architecture has been tested in several operating conditions, both grid connected and islanded.

Table 8.1: Parameters of the laboratory microgrid prototype

| Parameter | Description | Value | |
|--|---------------------------|-----------|--|
| V_G | Grid voltage | 230 | V |
| V^{\max} | Maximum microgrid voltage | 240 | V |
| P_L | Load power | 4 | kW |
| f_0 | Grid frequency | 50 | Hz |
| L_G | Tran. inductance | 600 | μH |
| Z_1 | B1 impedance | 0.3+j0.07 | Ω |
| Z_2 | B2 impedance | 0.3+j0.07 | Ω |
| Z_3 | B3 impedance | 0.22+j0.0 | Ω |
| Z_4 | B4 impedance | 0.22+j0.0 | Ω |
| L_G | Transformer inductance | 600 | μH |
| k_I | OV control parameter | 500 | $\frac{\text{W}}{\text{s} \cdot \text{V}}$ |
| $\hat{p}_{G1}^{\min}, \hat{p}_{G2}^{\min}$ | Min gen. power | 0, 0 | kW |
| $\hat{p}_{G1}^{\max}, \hat{p}_{G2}^{\max}$ | Max gen. power | 0.8, 3 | kW |
| a_1, a_2 | Power rating | 3, 3 | kVA |

The most interesting measured behaviors are reported in the following.

8.2.1 Load Step During Islanded Operation

Fig. 8-5 shows a load step variation from 0 kW to 2 kW during islanded operation, where the dynamic response of UI and power-based control can be appreciated. Control references are set so that the power needs of the load are completely fed by EGs. Therefore, before the transition the UI performs as a grid forming device with a zero injected power. Differently, at the connection of the load, the UI provides a fast response in supplying its power demand, while, after the transition, the power-based control gradually redistributes the load among the EGs. In steady-state, the load power is completely supplied by the EGs in proportion of their local power availability. This proves that the power-based control automatically manages different saturation limits and dynamics of EGs.

8.2.2 Connection Process

Fig. 8-6 represents the microgrid connection process. After the UI synchronizes the microgrid voltage v_{MG} with the voltage of the mains v_G , the microgrid can safely connect to

the grid through the electromechanical breaker CB_2 (see Fig. 8-4). Once the connection is completed, the grid current is gradually adjusted to the desired set-point, guaranteeing a soft transition. Notice, indeed, that no critical transient occurs in voltage or current.

8.2.3 Load Step During Grid Connected Operation

Fig. 8-7 and Fig. 8-8 show the load step variation from 0 kW to 2 kW and from 2 kW to 4 kW, respectively, during grid-connected mode. Fig. 8-7 shows a well regulated grid current, with negligible perturbations. Fig. 8-8, instead, shows a similar dynamic behavior of Fig. 8-5; however, in the steady-state the active power provided by the EGs is not enough to supply the load demand. Consequently, the EGs are lead to smoothly reach their maximum generation capability; because the grid current reference is set to zero, the power balance is ensured by the UI. This proves that the power-based control automatically manages different saturation limits of EGs.

8.2.4 Transition to the Islanded Operation

Fig. 8-9 and Fig. 8-10 show the intentional and non-intentional islanding procedure, respectively. In the first one, the master controller is actually driving the transition (e.g., due to a scheduled maintenance) and sets the grid reference current to zero before performing the disconnection. In the second one, instead, the transition occurs without prior information to the master controller (i.e., CB_1 opens suddenly); therefore, UI must first detect the islanded condition and, subsequently, initiate the islanded mode (CB_2 opens), such sequence of operation implies a longer and more critical transition to the islanded operation. Still, both islanding processes are free of undesired transients.

8.2.5 Management of Overvoltage Conditions

The considered experiment emulates the situation where the master controller requires a step change in the power delivered by EGs. Initially, the microgrid fulfills its power needs autonomously, so that $p_{MG} = 0$ kW. Power injections from the EGs are approximately $p_{EG1} = 0.42$ kW and $p_{EG2} = 1.59$ kW; the power requested by the load is approximately

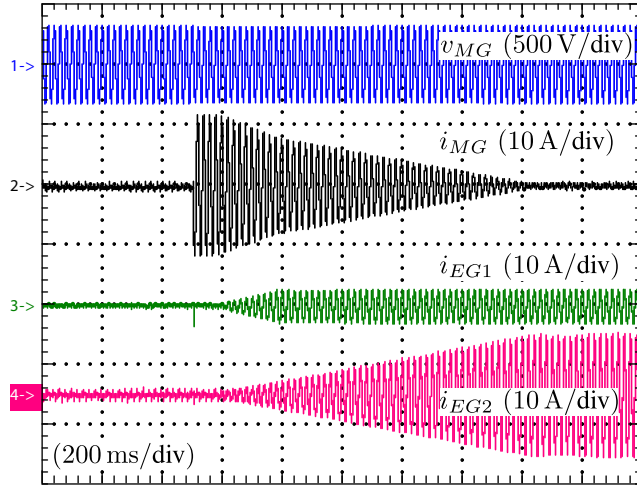


Figure 8-5: Load step (0 to 2 kW) during islanded operation

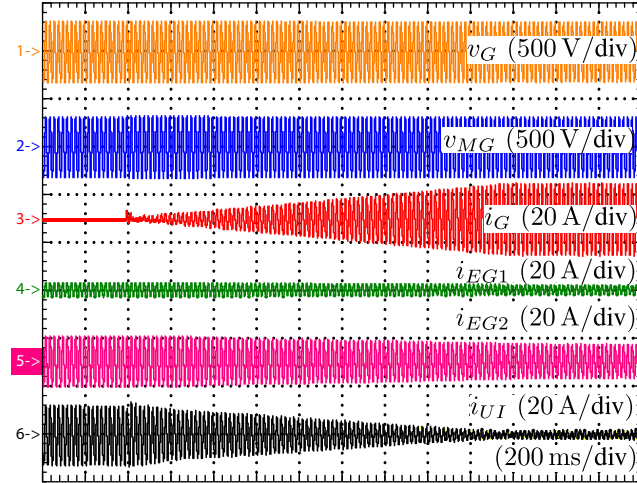


Figure 8-6: Process of connection to the mains

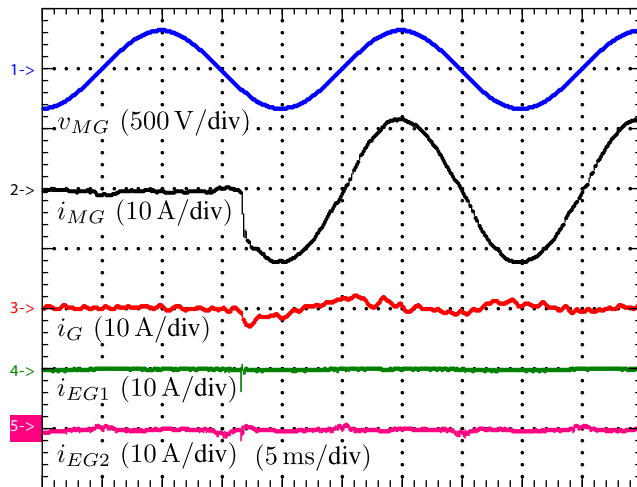


Figure 8-7: Load step (0 to 2 kW) during grid-connected operation

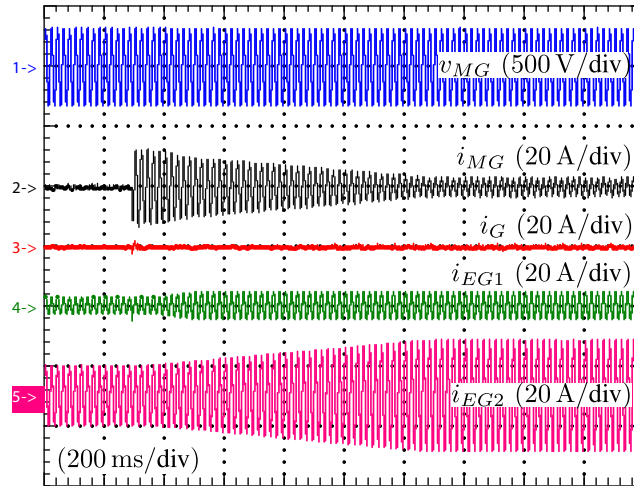


Figure 8-8: Load step (2 to 4 kW) during grid-connected operation

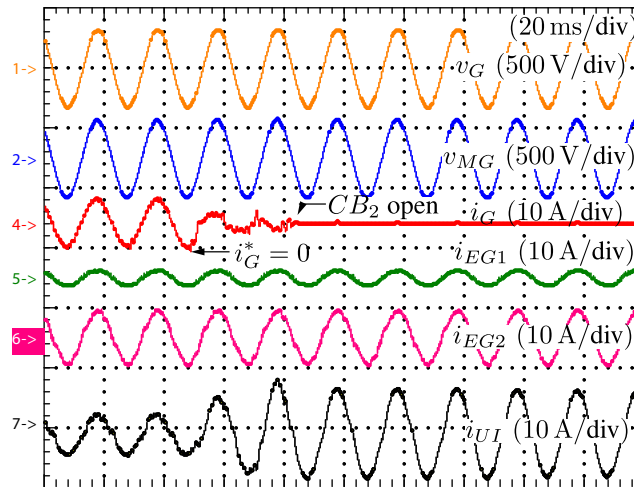


Figure 8-9: Intentional transition to islanded operation

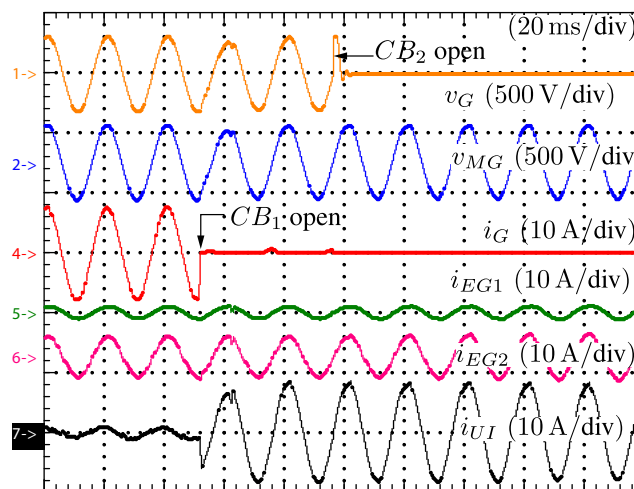


Figure 8-10: Non-intentional transition to islanded operation

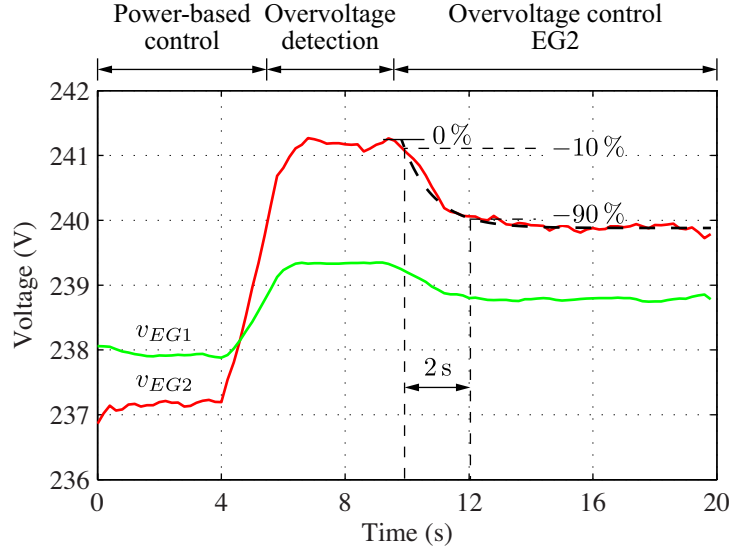


Figure 8-11: Experimental result. The dashed line represents the ideal first order behavior of the expected response of v_{EG2} .

$p_{LOAD} = 2 \text{ kW}$ and is shared among EG_1 and EG_2 in proportion to EGs availability (see Table 8.1), according to the power-based control.

At $t = 4 \text{ s}$ it is assumed that the power requested at the PCC from the MC changes to -1.5 kW . At this time power references would be equal to: $p_{EG1} = 0.74 \text{ kW}$ and $p_{EG2} = 2.76 \text{ kW}$. These are the power references calculated locally by the EGs, on the basis of the power-based control, and actuated. The increased generation from EGs rises the voltage along the distribution network, causing the occurrence of an overvoltage condition at the point of connection of EG_2 . In particular, V_{EG2} transcends the maximum voltage limit $V^{\max} = 240 \text{ V}$ and triggers the overvoltage control for EG_2 . The local overvoltage control makes the power injection from EG_2 decrease, so as to limit the measured output voltage V_{EG2} below V^{\max} . Concurrently, the power injection from EG_1 increases to provide the power that cannot be delivered by EG_2 , due to the voltage limitation. Finally, in the transient, EG_1 reaches the maximum value \hat{p}_{EG1}^{\max} , whereas EG_2 generates the active power that, in the considered situation, corresponds to a measured output voltage equal to the maximum value V^{\max} . In steady-state, the following power injections are obtained: $p_{GRID} = -1.2 \text{ kW}$, $p_{EG1} = 0.8 \text{ kW}$, $p_{EG2} = 2.4 \text{ kW}$, and $p_{LOAD} = 2 \text{ kW}$.

The dynamics shown in the experimental results can be verified by using (7.46). In the

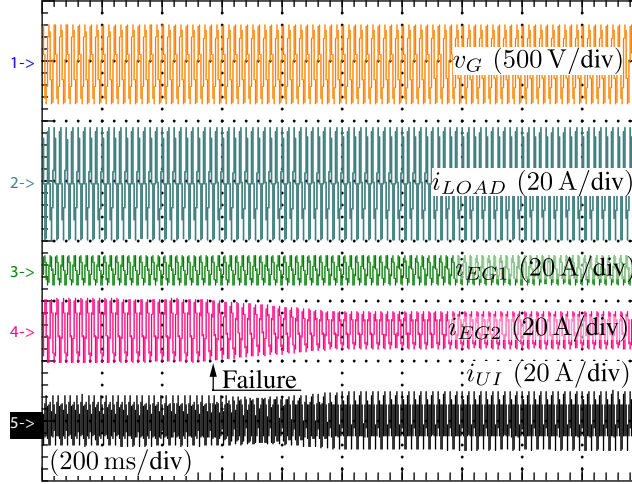


Figure 8-12: Communication failure.

considered case, matrices \mathbf{A} , \mathbf{C} and $\tilde{\mathbf{X}}$ are:

$$\mathbf{A} = \begin{bmatrix} 0 & -1 & -1 \\ 1 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix}, \quad \mathbf{C} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -k_I \end{bmatrix}, \quad \tilde{\mathbf{X}} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0.3 & 0.3 \\ 0 & 0.3 & 0.82 \end{bmatrix}. \quad (8.1)$$

Calculating the eigenvalues of $1/U_0 \tilde{\mathbf{X}} (\mathbf{I} - \mathbf{A})^{-1} \mathbf{C}$, it results: $500 \cdot [0, 0, -0.0022]$. These values correspond to a pole with time constant equal to 0.9 s. Correspondingly, the expected *rise time* needed to V_{EG2} to undergo a transient from 10% to 90% of the final total variation should be $2.2 \cdot 0.9 \text{ s} \simeq 2 \text{ s}$, which is in very good accordance with Fig. 8-11.

8.2.6 Communication Failure

Fig. 8-12 shows a communication failure occurring between MC and EG_2 during islanded operation. Before the communication link fails, the EGs are coordinated by the MC. After the failure, EG_1 keeps running regularly (driven by MC) whereas EG_2 changes its power reference from power-based control mode to local optimization mode. In this case, the UI ensures the power balancing, up to the instant when the communication is restored or loads and generators readjusted. It is worth remarking here how a communication failure does not jeopardize the system, which is instead able to ride through the abnormal event smoothly and without triggering any irregular behavior.

8.3 Summary

This chapter provides the experimental evaluation of the master/slave microgrid architecture with the power-based control algorithm. To that purpose, a laboratory microgrid prototype that integrates all the main features of the control architecture and algorithm is considered. In particular, the behavior of the following components is taken into account: the master controller, the slave controllers, the current controllers of EGs, the current, voltage, and grid current controller of the UI, the communication system, the management of islanding operation together with the needed hardware components, the fault protection system.

The microgrid prototype has been employed to evaluate the effectiveness of the most critical functionalities of the whole system. It is shown that:

- the power-based control can regulate the power flow at microgrid's PCC accurately and with fast dynamics;
- the UI smoothly manages transitions between the grid connected and islanded operation, which can occur unnoticed within the microgrid;
- the current requested to the mains is well filtered by the UI, even in case of connection/disconnection of loads, and also at the connection of the microgrid with the mains;
- overvoltage conditions at the nodes of the microgrids can be effectively managed by the power-based control.

Chapter 9

Conclusions

The evolution of the electric energy sector toward the smart grid model is a necessary step to attain electric power systems that are suitable for the future needs of society. This evolution, made of renewable sources, ICT, automation, and power electronics, concerns electric power systems comprehensively, including domains such as generation, distribution, transmission, customer, service provider, markets, operations. The electrical domain that may undergo the greatest changes is the low-voltage one, where, smart microgrids—namely, controllable power systems that aggregate loads and energy resources—are expected to autonomously fulfill local energy needs as well as make available to the upper level system their flexibility in managing surplus energy resources.

In some European countries (e.g., Germany, Italy) a significant adoption of renewable sources took place. The main challenges linked with an increasing penetration of distributed energy resources (DERs) in low-voltage grids could therefore be highlighted; these challenges are typically due to production peaks and fluctuations, harmonic and reactive currents, risks of unintentional islanding. A wide adoption of energy resources interfaced both to the grid and to an ICT infrastructure by means of electronic power converters will also take place in the next years. This, on the one hand, will endow low-voltage grids with superior flexibility in managing energy, on the other hand, will pose new control requirements to an efficient operation of the new, additional resources. These control issues have never directly concerned low-voltage grids before, hence, specific solutions and investigations on how to manage grid-connected devices are required.

The above scenario outlines the scope of this dissertation. In particular, the aim of the work presented herein is to identify and investigate a microgrid architecture that endows a section of a low-voltage grid with the features of a smart microgrid, by properly controlling the available DERs. With that aim, a master/slave architecture is proposed where DERs are interfaced to the grid by means of conventional current-driven electronic power processors (EPP) and the microgrid is interfaced to the utility via a voltage-driven EPP. EPP-interfaced DERs play as slave units, called energy gateways (EGs), while the EPP interfacing the microgrid to the utility, called utility interface (UI), plays the role of master unit and hosts a centralized microgrid controller, called master controller (MC). Innovative, high-performance current controllers with low implementation complexity are proposed to serve as inner current controllers for EPPs. For both measurement and control, power data only are used, and processed according to the Conservative Power Theory (CPT), which offers a meaningful and computationally efficient approach to manage power quantities referring to different grid nodes. The master/slave organization allows the microgrid to operate islanded from the mains and to decouple local (e.g., maximization of generation from renewables) and global (e.g., control of the power flow at the PCC) control objectives, with limited communication and computation requirements. Within this architecture, a model-free algorithm, the so called power-based control, is proposed to coordinate the contribution of injected power from UI and EGs to the purpose of regulating the power flow at the PCC and, simultaneously, limiting voltage magnitudes along distribution lines. The control of EGs is made by means of a couple of control coefficients, one for active power, the other for reactive power, that are computed by the MC on the basis of information collected from EGs and measurements made at microgrid's PCC. The power-based control ensures, in the steady state, an accurate, proportional active and reactive power sharing among EGs with respect to locally available power, with a minimum impact on the communication infrastructure. The individual devices of the architecture as well as the whole microgrid architecture have been tested by employing conventional simulations, real-time simulations, and laboratory prototypes.

Appendix A

Current Sensor Board

Ch. 6 reports the study on a couple of novel digital current controllers. The implementation of the controllers is made on the control platform described in this appendix.

The control algorithms described in Ch. 6 are synthesized into the FPGA chip (a Xilinx Spartan-6 LX45) available within the general purpose inverter control board from National Instruments that is referred to in Ch. 3. The control board is coupled to a custom acquisition daughter board (current sensor board) embedding the current sensor and featuring a 12-bit, 65 MS/s peak, analog to digital converter (AD9226). The performance that can be obtained with the presented controllers are influenced by the quality of the current measurement, therefore, in this appendix more details about the employed control and measurement system are reported.

A diagram of the sensor board is reported in Fig. A-1, the top view and bottom view of the final implementation are also reported, respectively, in Fig. A-2 and Fig. A-3.

The sensor board comprises the following components.

- Shunt resistor $25\text{ m}\Omega$, acts as current transducer.
- Differential amplifier INA2128, employed to buffer the transduced signal and reject the common mode noise that may appear due to converter's commutations.
- Fully differential amplifier AD8137, employed to feed the ADC with the transduced signal, it produces a differential signal that makes an optimized use of the ADC's dynamic range and drives its input as a low impedance source.

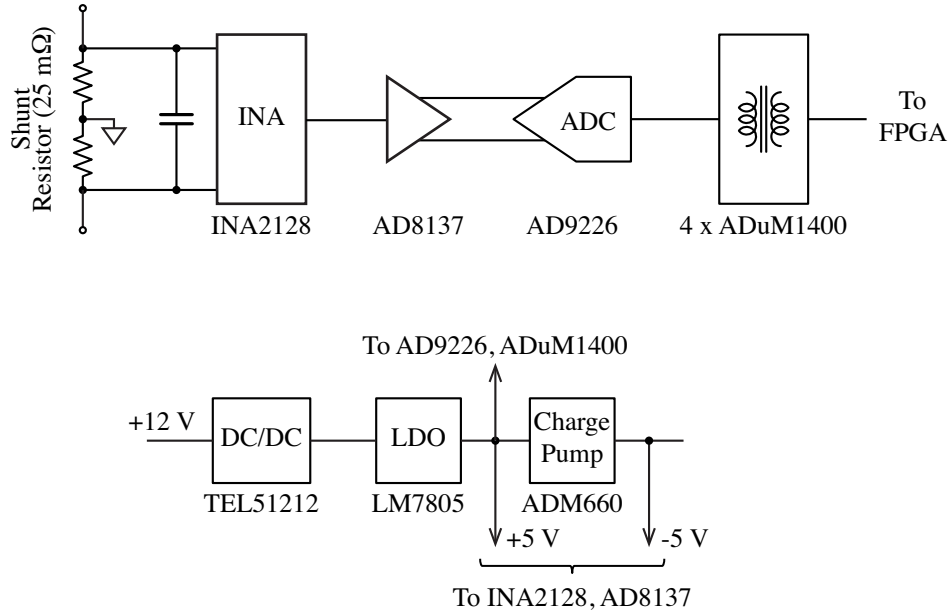


Figure A-1: Simplified circuit diagram of the current sensor board.

Table A.1: Current Sensor Board Parameters

| Parameter | Symbol | Value | |
|-------------------------------|-----------------|-------|---------|
| AD converter resolution | n_{bit} | 12 | bit |
| AD converter full-scale range | FSR | 2.0 | V |
| AD converter latency | Δt_{AD} | 0.2 | μs |
| Current sensor gain | $K_{sense,i}$ | 25 | mV/A |
| Arithmetic resolution | n_{bit}^{ALU} | 16 | bit |
| Current sensor FSR | i_L^{MAX} | 50 | A |

- Analog to digital converter AD9226, converts the analog signal to the digital domain with low latency and high sample rate.
- Magnetically isolated digital gates, isolate the computing unit (FPGA) from the grid-tied sensor circuit.

The main parameters of the current sensor board are reported in Table A.1.

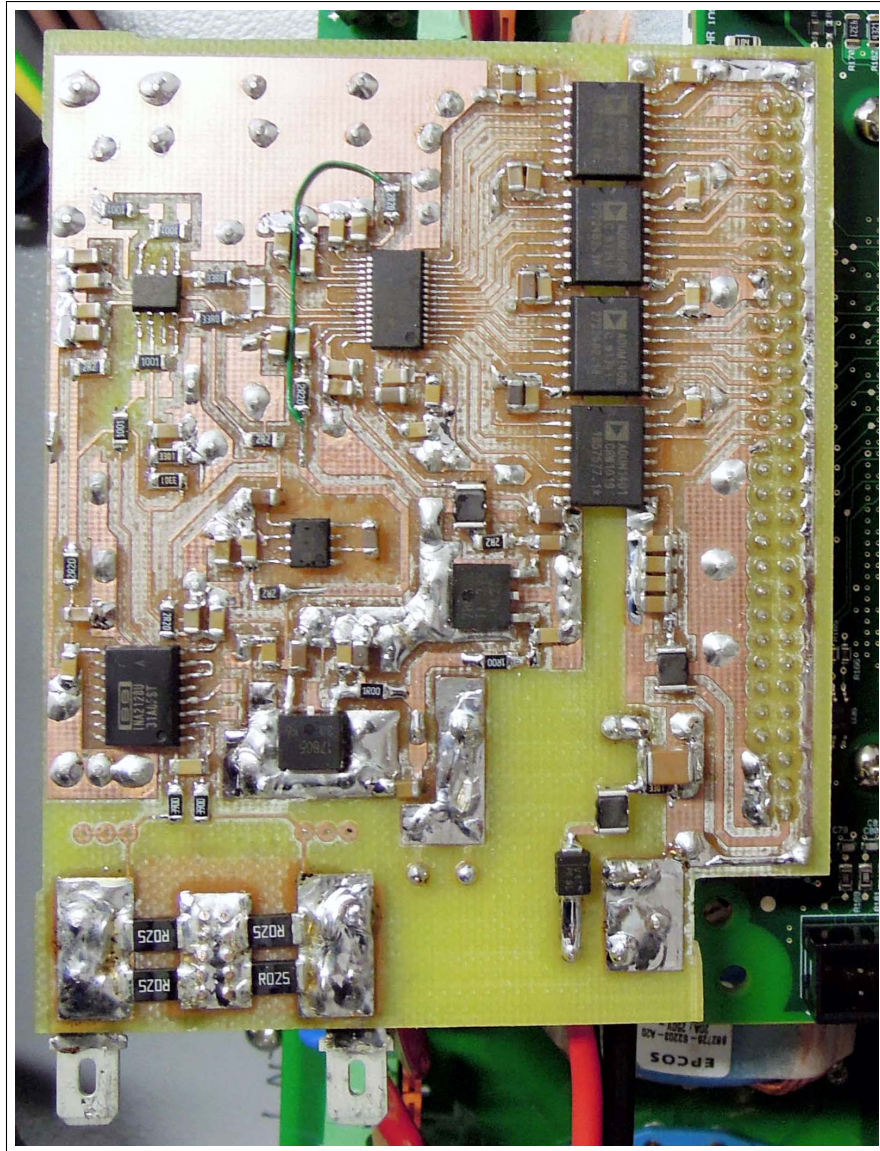


Figure A-2: Current sensor board (top view).

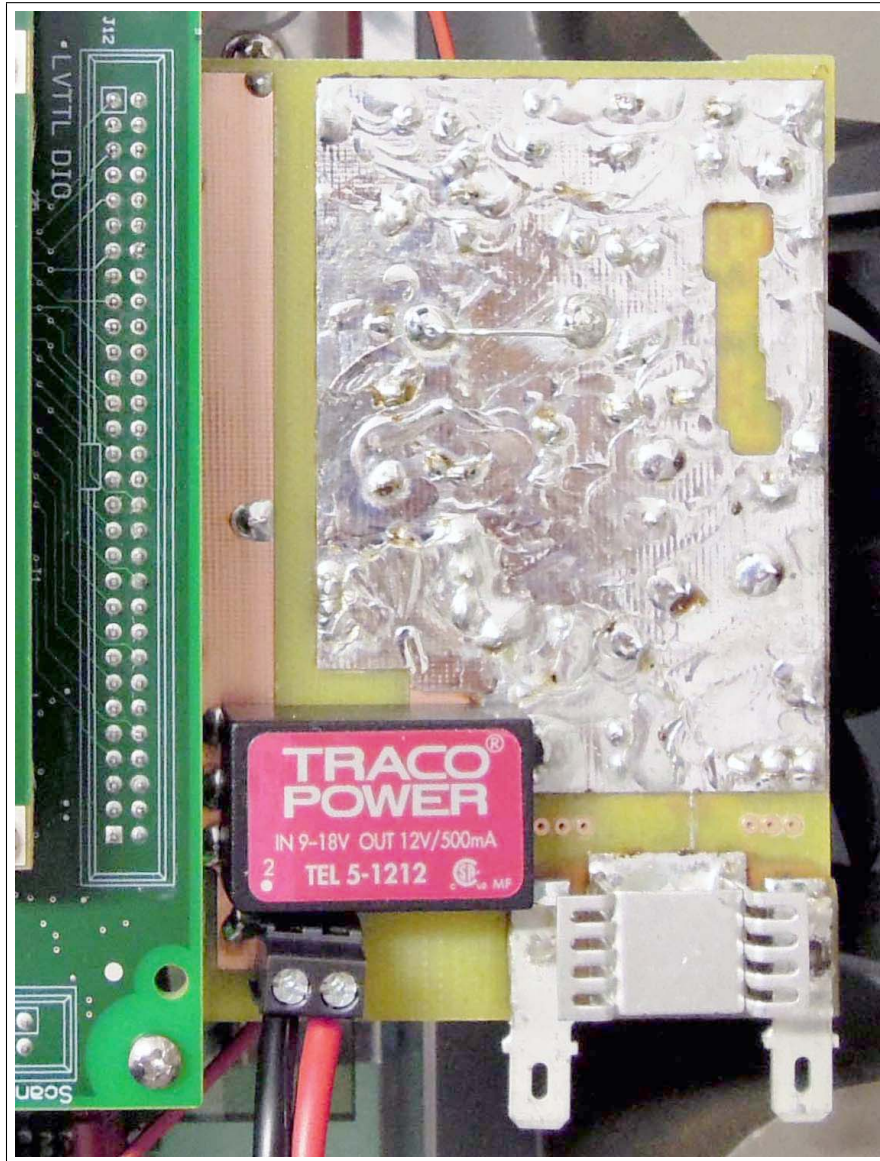


Figure A-3: Current sensor board (bottom view).

Bibliography

- [1] *Energy and Climate Change–World Energy Outlook Special Briefing for COP21*. International Energy Agency, 2015.
- [2] “Global Market Outlook/2015-2019,” European Photovoltaic Industry Association, Tech. Rep., 2015.
- [3] H. Wirth, “Recent Facts about Photovoltaics in Germany,” Fraunhofer, Tech. Rep., 2015.
- [4] D. Tan, “Emerging System Applications and Technological Trends in Power Electronics,” *IEEE Power Electronics Magazine*, vol. 2, no. 2, pp. 38–47, June 2015.
- [5] D. Boroyevich, I. Cvetkovic, R. Burgos, and D. Dong, “Integrid: A Future Electronic Energy Network?” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 3, pp. 127–138, September 2013.
- [6] O. Augé, “TOSA concept: a full electric large capacity urban bus system,” in *Keynote at 17th European Conference on Power Electronics and Applications (EPE ECCE-Europe)*, 2015.
- [7] C. Abbey, D. Cornforth, N. Hatziaargyriou, K. Hirose, A. Kwasinski, E. Kyriakides, G. Platt, L. Reyes, and S. Suryanarayanan, “Powering Through the Storm: Microgrids Operation for More Efficient Disaster Recovery,” *IEEE Power and Energy Magazine*, vol. 12, no. 3, pp. 67–76, May 2014.
- [8] P. Tenti, H. Paredes, and P. Mattavelli, “Conservative Power Theory, a Framework to Approach Control and Accountability Issues in Smart Microgrids,” *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 664–673, March 2011.
- [9] A. M. Bouzid, J. M. Guerrero, A. Cheriti, M. Bouhamida, P. Sicard, and M. Benghanem, “A survey on control of electric power distributed generation systems for microgrid applications,” *Renewable and Sustainable Energy Reviews*, vol. 44, no. 0, pp. 751–766, 2015.
- [10] A. Timbus, M. Liserre, R. Teodorescu, P. Rodriguez, and F. Blaabjerg, “Evaluation of current controllers for distributed power generation systems,” *IEEE Transactions on Power Electronics*, vol. 24, no. 3, pp. 654–664, 2009.

- [11] J. Xu, T. Tang, and S. Xie, "Evaluations of current control in weak grid case for grid-connected lcl-filtered inverter," *IET Power Electronics*, vol. 6, no. 2, pp. 227–234, 2013.
- [12] J. Wang, N. Chang, X. Feng, and A. Monti, "Design of a Generalized Control Algorithm for Parallel Inverters for Smooth Microgrid Transition Operation," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 8, pp. 4900–4914, Aug 2015.
- [13] W. Du, Q. Jiang, M. J. Erickson, and R. H. Lasseter, "Voltage-source control of pv inverter in a certs microgrid," *IEEE Transactions on Power Delivery*, pp. 1–1, 2014.
- [14] M. Erickson, T. Jahns, and R. Lasseter, "Comparison of PV Inverter Controller Configurations for CERTS Microgrid Applications of pv inverter controller configurations for certs microgrid applications," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2011, pp. 659–666.
- [15] F. Huerta, D. Pizarro, S. Cobreces, F. J. Rodriguez, C. Giron, and A. Rodriguez, "LQG Servo Controller for the Current Control of LCL Grid-Connected Voltage-Source Converters," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 11, pp. 4272–4284, 2012.
- [16] J. He and Y. W. Li, "Hybrid Voltage and Current Control Approach for DG-Grid Interfacing Converters With LCL filters," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 5, pp. 1797–1809, 2013.
- [17] D. Dong, T. Thacker, R. Burgos, D. Boroyevich, F. Wang, and B. Giewont, "Control design and experimental verification of a multi-function single-phase bidirectional pwm converter for renewable energy systems," in *13th European Conference on Power Electronics and Applications (EPE'09)*, Conference Proceedings, pp. 1–10.
- [18] J. Dannehl, C. Wessels, and F. W. Fuchs, "Limitations of Voltage-Oriented PI Current Control of Grid-Connected PWM Rectifiers With LCL Filters," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 2, pp. 380–388, 2009.
- [19] X. Zhang, J. W. Spencer, and J. M. Guerrero, "Small-Signal Modeling of Digitally Controlled Grid-Connected Inverters With LCL Filters," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 9, pp. 3752–3765, 2013.
- [20] S. Buso, S. Fasolo, and P. Mattavelli, "Uninterruptible power supply multiloop control employing digital predictive voltage and current regulators," *IEEE Transactions on Industry Applications*, vol. 37, no. 6, pp. 1846–1854, 2001.
- [21] J. He, Y. W. Li, and F. Blaabjerg, "Flexible Microgrid Power Quality Enhancement Using Adaptive Hybrid Voltage and Current Controller," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 6, pp. 2784–2794, June 2014.
- [22] D. Ahmadi and J. Wang, "Online Selective Harmonic Compensation and Power Generation With Distributed Energy Resources," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3738–3747, 2014.

- [23] J. He, Y. W. Li, F. Blaabjerg, and X. Wang, "Active Harmonic Filtering Using Current-Controlled, Grid-Connected DG Units With Closed-Loop Power Control," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 642–653, 2014.
- [24] J. Xu, S. Xie, and T. Tang, "Active Damping-Based Control for Grid-Connected LCL Filtered Inverter With Injected Grid Current Feedback Only," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 9, pp. 4746–4758, 2014.
- [25] A. Bueno, J. M. Aller, J. A. Restrepo, R. Harley, and T. G. Habetler, "Harmonic and Unbalance Compensation Based on Direct Power Control for Electric Railway Systems," *IEEE Transactions on Power Electronics*, vol. 28, no. 12, pp. 5823–5831, 2013.
- [26] J. He, Y. W. Li, D. Bosnjak, and B. Harris, "Investigation and Active Damping of Multiple Resonances in a Parallel-Inverter-Based Microgrid," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 234–246, 2013.
- [27] Y. W. Li and J. He, "Distribution System Harmonic Compensation Methods: An Overview of DG-Interfacing Inverters," *IEEE Industrial Electronics Magazine*, vol. 8, no. 4, pp. 18–31, Dec 2014.
- [28] A. Micallef, M. Apap, C. Spiteri-Staines, J. M. Guerrero, and J. C. Vasquez, "Reactive Power Sharing and Voltage Harmonic Distortion Compensation of Droop Controlled Single Phase Islanded Microgrids," *IEEE Transactions on Smart Grid*, vol. 5, no. 3, pp. 1149–1158, 2014.
- [29] X. Wang, F. Blaabjerg, M. Liserre, Z. Chen, J. He, and Y. Li, "An Active Damper for Stabilizing Power-Electronics-Based AC Systems," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3318–3329, 2014.
- [30] X. Wang, F. Blaabjerg, and Z. Chen, "Autonomous Control of Inverter-Interfaced Distributed Generation Units for Harmonic Current Filtering and Resonance Damping in an Islanded Microgrid," *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 452–461, Jan 2014.
- [31] A. Costabeber, P. Tenti, T. Caldognetto, and E. Verri Liberado, "Selective compensation of reactive, unbalance, and distortion power in smart grids by synergistic control of distributed switching power interfaces," in *15th European Conference on Power Electronics and Applications (EPE)*, Sept. 2013, Conference Proceedings, pp. 1–9.
- [32] U. Borup, F. Blaabjerg, and P. N. Enjeti, "Sharing of Nonlinear Load in Parallel-Connected Three-Phase Converters," *IEEE Transactions on Industry Applications*, vol. 37, no. 6, pp. 1817–1823, 2001.
- [33] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. Timbus, "Overview of Control and Grid Synchronization for Distributed Power Generation Systems," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1398–1409, Oct 2006.

- [34] D. Dong, B. Wen, D. Boroyevich, P. Mattavelli, and Y. Xue, "Analysis of Phase-Locked Loop Low-Frequency Stability in Three-Phase Grid-Connected Power Converters Considering Impedance Interactions," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 310–321, Jan 2015.
- [35] R. Sgarbossa, S. Lissandron, P. Mattavelli, R. Turri, and A. Cerretti, "Analysis of ΔP - ΔQ area of uncontrolled islanding in low voltage grids with PV generators," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2014, pp. 5667–5674.
- [36] H. Laaksonen, "Advanced Islanding Detection Functionality for Future Electricity Distribution Networks," *IEEE Transactions on Power Delivery*, vol. 28, no. 4, pp. 2056–2064, Oct 2013.
- [37] M. A. Abusara, J. M. Guerrero, and S. M. Sharkh, "Line-Interactive UPS for Microgrids," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 3, pp. 1292–1300, 2014.
- [38] K. Jong-Yul, J. Jin-Hong, K. Seul-Ki, C. Changhee, P. June Ho, K. Hak-Man, and N. Kee-Young, "Cooperative Control Strategy of Energy Storage System and Microsources for Stabilizing the Microgrid during Islanded Operation," *IEEE Transactions on Power Electronics*, vol. 25, no. 12, pp. 3037–3048, 2010.
- [39] K. Jong-Yul, K. Seul-Ki, and J. Jin-Hong, "Coordinated state-of-charge control strategy for microgrid during islanded operation," in *Power Electronics for Distributed Generation Systems (PEDG), 2012 3rd IEEE International Symposium on*, Conference Proceedings, pp. 133–139.
- [40] P. Mahat, J. Escribano Jimenez, E. Rodriguez Moldes, S. Haug, I. Szczesny, K. Pollestad, and L. Totu, "A Micro-Grid Battery Storage Management," in *IEEE Power and Energy Society General Meeting (PES)*, July 2013, pp. 1–5.
- [41] C. Gavriluta, I. Candela, J. Rocabert, I. Etxeberria-Otadui, and P. Rodriguez, "Storage system requirements for grid supporting PV-power plants," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2014, pp. 5323–5330.
- [42] K. De Brabandere, B. Bolsens, J. Van den Keybus, A. Woyte, J. Driesen, and R. Belmans, "A Voltage and Frequency Droop Control Method for Parallel Inverters," *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1107–1115, 2007.
- [43] P. Tenti, A. Costabeber, F. Sichirollo, and P. Mattavelli, "Minimum loss control of low-voltage residential microgrids," in *38th Annual Conference on IEEE Industrial Electronics Society (IECON'12)*, Conference Proceedings, pp. 5650–5656.
- [44] P. Tenti, A. Costabeber, P. Mattavelli, and D. Trombetti, "Distribution Loss Minimization by Token Ring Control of Power Electronic Interfaces in Residential Microgrids," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 10, pp. 3817–3826, Oct 2012.

- [45] L. Zhang, K. Sun, H. Hu, and Y. Xing, "A System-Level Control Strategy of Photovoltaic Grid-Tied Generation Systems for European Efficiency Enhancement," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3445–3453, 2014.
- [46] T. B. Lazzarin, G. A. T. Bauer, and I. Barbi, "A Control Strategy for Parallel Operation of Single-Phase Voltage Source Inverters: Analysis, Design and Experimental Results," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 6, pp. 2194–2204, 2013.
- [47] G. Yajuan, J. C. Vasquez, and J. M. Guerrero, "A simple autonomous current-sharing control strategy for fast dynamic response of parallel inverters in islanded microgrids," in *IEEE International Energy Conference (ENERGYCON)*, 2014, Conference Proceedings, pp. 182–188.
- [48] M. Prodanovic and T. Green, "High-Quality Power Generation Through Distributed Control of a Power Park Microgrid," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1471–1482, Oct 2006.
- [49] S. Bolognani and S. Zampieri, "A Distributed Control Strategy for Reactive Power Compensation in Smart Microgrids," *IEEE Transactions on Automatic Control*, vol. 58, no. 11, pp. 2818–2833, 2013.
- [50] R. Majumder, "Aspect of voltage stability and reactive power support in active distribution," *IET Generation, Transmission & Distribution*, vol. 8, no. 3, pp. 442–450, 2014.
- [51] P. Basak, S. Chowdhury, S. Halder nee Dey, and S. P. Chowdhury, "A literature review on integration of distributed energy resources in the perspective of control, protection and stability of microgrid," *Renewable and Sustainable Energy Reviews*, vol. 16, no. 8, pp. 5545–5556, 2012.
- [52] M. Falahi, K. Butler-Purry, and M. Ehsani, "Dynamic Reactive Power Control of Islanded Microgrids," *IEEE Transactions on Power Systems*, vol. 28, no. 4, pp. 3649–3657, 2013.
- [53] A. Milczarek, M. Malinowski, and J. Guerrero, "Reactive Power Management in Islanded Microgrid—Proportional Power Sharing in Hierarchical Droop Control," *IEEE Transactions on Smart Grid*, vol. 6, no. 4, pp. 1631–1638, July 2015.
- [54] L. Junqi, D. Obradovic, and A. Monti, "Decentralized LQG control with online set-point adaptation for parallel power converter systems," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2010, Conference Proceedings, pp. 3174–3179.
- [55] N. Jelani, M. Molinas, and S. Bolognani, "Reactive Power Ancillary Service by Constant Power Loads in Distributed AC Systems," *IEEE Transactions on Power Delivery*, vol. 28, no. 2, pp. 920–927, April 2013.

- [56] C.-H. Lo and N. Ansari, "Alleviating Solar Energy Congestion in the Distribution Grid via Smart Metering Communications," *IEEE Transactions on Parallel and Distributed Systems*, vol. 23, no. 9, pp. 1607–1620, 2012.
- [57] G. Mokhtari, A. Ghosh, G. Nourbakhsh, and G. Ledwich, "Smart Robust Resources Control in LV Network to Deal With Voltage Rise Issue," *IEEE Transactions on Sustainable Energy*, vol. 4, no. 4, pp. 1043–1050, 2013.
- [58] I. J. Balaguer, Q. Lei, S. Yang, U. Supatti, and F. Z. Peng, "Control for Grid-Connected and Intentional Islanding Operations of Distributed Power Generation," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 1, pp. 147–157, 2011.
- [59] Z. Liu, J. Liu, and Y. Zhao, "A Unified Control Strategy for Three-Phase Inverter in Distributed Generation," *IEEE Transactions on Power Electronics*, vol. 29, no. 3, pp. 1176–1191, 2014.
- [60] Z. Liu and J. Liu, "Indirect current control based seamless transfer of three-phase inverter in distributed generation," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3368–3383, 2014.
- [61] R. Tirumala, N. Mohan, and C. Henze, "Seamless transfer of grid-connected PWM inverters between utility-interactive and stand-alone modes," in *Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, vol. 2, 2002, pp. 1081–1086 vol.2.
- [62] Z. Yao, L. Xiao, and Y. Yan, "Seamless Transfer of Single-Phase Grid-Interactive Inverters Between Grid-Connected and Stand-Alone Modes," *IEEE Transactions on Power Electronics*, vol. 25, no. 6, pp. 1597–1603, June 2010.
- [63] J. Vasquez, J. Guerrero, A. Luna, P. Rodriguez, and R. Teodorescu, "Adaptive Droop Control Applied to Voltage-Source Inverters Operating in Grid-Connected and Islanded Modes," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 10, pp. 4088–4096, Oct 2009.
- [64] T. Vandoorn, B. Meersman, J. De Kooning, and L. Vandeveld, "Transition From Islanded to Grid-Connected Mode of Microgrids With Voltage-Based Droop Control," *IEEE Transactions on Power Systems*, vol. 28, no. 3, pp. 2545–2553, Aug 2013.
- [65] A. Micallef, M. Apap, C. Spiteri-Staines, and J. Guerrero, "Single-Phase Microgrid With Seamless Transition Capabilities Between Modes of Operation," *IEEE Transactions on Smart Grid*, vol. PP, no. 99, pp. 1–1, 2015.
- [66] Q.-C. Zhong, P.-L. Nguyen, Z. Ma, and W. Sheng, "Self-Synchronized Synchronverters: Inverters Without a Dedicated Synchronization Unit," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 617–630, 2014.
- [67] E. Alegria, T. Brown, E. Minear, and R. H. Lasseter, "CERTS Microgrid Demonstration With Large-Scale Energy Storage and Renewable Generation," *IEEE Transactions on Smart Grid*, vol. 5, no. 2, pp. 937–943, 2014.

- [68] M. Chandorkar, D. Divan, and R. Adapa, "Control of parallel connected inverters in standalone AC supply systems," *IEEE Transactions on Industry Applications*, vol. 29, no. 1, pp. 136–143, Jan 1993.
- [69] J. M. Guerrero, M. Chandorkar, T.-L. Lee, and P. C. Loh, "Advanced Control Architectures for Intelligent Microgrids - Part I: Decentralized and Hierarchical Control," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1254–1262, 2013.
- [70] W. Dan, T. Fen, T. Dragicevic, J. C. Vasquez, and J. M. Guerrero, "Coordinated primary and secondary control with frequency-bus-signaling for distributed generation and storage in islanded microgrids," in *39th Annual Conference of the IEEE Industrial Electronics Society (IECON'13)*, Conference Proceedings, pp. 7140–7145.
- [71] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. de Vicuna, and M. Castilla, "Hierarchical Control of Droop-Controlled AC and DC Microgrids - A General Approach Toward Standardization," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 1, pp. 158–172, 2011.
- [72] X. Lu, J. M. Guerrero, K. Sun, J. C. Vasquez, R. Teodorescu, and L. Huang, "Hierarchical Control of Parallel AC-DC Converter Interfaces for Hybrid Microgrids," *IEEE Transactions on Smart Grid*, vol. 5, no. 2, pp. 683–692, 2014.
- [73] N. Ullah, T. Thiringer, and D. Karlsson, "Voltage and Transient Stability Support by Wind Farms Complying With the E.ON Netz Grid Code," *IEEE Transactions on Power Systems*, vol. 22, no. 4, pp. 1647–1656, Nov 2007.
- [74] Q.-C. Zhong, "Robust Droop Controller for Accurate Proportional Load Sharing Among Inverters Operated in Parallel," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1281–1290, April 2013.
- [75] A. Bidram, A. Davoudi, F. L. Lewis, and J. M. Guerrero, "Distributed Cooperative Secondary Control of Microgrids Using Feedback Linearization," *IEEE Transactions on Power Systems*, vol. 28, no. 3, pp. 3462–3470, 2013.
- [76] T. L. Vandoorn, J. D. M. De Kooning, B. Meersman, and L. Vandeveldel, "Review of primary control strategies for islanded microgrids with power-electronic interfaces," *Renewable and Sustainable Energy Reviews*, vol. 19, pp. 613–628, 2013.
- [77] J. M. Guerrero, L. Hang, and J. Uceda, "Control of distributed uninterruptible power supply systems," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 8, pp. 2845–2859, 2008.
- [78] F. Pinhabel Marafão, D. Iglesias Brandão, A. Costabeber, and H. Morales Paredes, "Multi-task control strategy for grid-tied inverters based on conservative power theory," *IET Renewable Power Generation*, vol. 9, no. 2, pp. 154–165, 2015.
- [79] D. Dong, T. Thacker, I. Cvetkovic, R. Burgos, D. Boroyevich, F. Wang, and G. Skutt, "Modes of Operation and System-Level Control of Single-Phase Bidirectional PWM

- Converter for Microgrid Systems,” *IEEE Transactions on Smart Grid*, vol. 3, no. 1, pp. 93–104, March 2012.
- [80] A. Bidram and A. Davoudi, “Hierarchical Structure of Microgrids Control System,” *IEEE Transactions on Smart Grid*, vol. 3, no. 4, pp. 1963–1976, 2012.
- [81] T. Caldognetto and P. Tenti, “Microgrids Operation Based on Master-Slave Cooperative Control,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 4, pp. 1081–1088, 2014.
- [82] T. H. Qing-Chang Zhong, *Control of Power Inverters in Renewable Energy and Smart Grid Integration*. Wiley-IEEE Press, 2013.
- [83] R. Teodorescu, F. Blaabjerg, M. Liserre, and P. Loh, “Proportional-resonant controllers and filters for grid-connected voltage-source converters,” *IEE Proceedings Electric Power Applications*, vol. 153, no. 5, pp. 750–762, September 2006.
- [84] G. Weiss, Q. C. Zhong, T. C. Green, and J. Liang, “ H^∞ repetitive control of DC-AC converters in microgrids,” *IEEE Transactions on Power Electronics*, vol. 19, no. 1, pp. 219–230, 2004.
- [85] G. Escobar, P. Mattavelli, M. Hernandez-Gomez, and P. R. Martinez-Rodriguez, “Filters With Linear-Phase Properties for Repetitive Feedback,” *IEEE Transactions on Industrial Electronics*, vol. 61, no. 1, pp. 405–413, 2014.
- [86] T. Hornik and Q.-C. Zhong, “A Current-Control Strategy for Voltage-Source Inverters in Microgrids Based on H^∞ and Repetitive Control,” *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 943–952, March 2011.
- [87] D. Dong, T. Thacker, R. Burgos, F. Wang, and D. Boroyevich, “On Zero Steady-State Error Voltage Control of Single-Phase PWM Inverters With Different Load Types,” *Power Electronics, IEEE Transactions on*, vol. 26, no. 11, pp. 3285–3297, Nov 2011.
- [88] Y. Yang, K. Zhou, H. Wang, F. Blaabjerg, D. Wang, and B. Zhang, “Frequency Adaptive Selective Harmonic Control for Grid-Connected Inverters,” *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 3912–3924, July 2015.
- [89] L. He, K. Zhang, J. Xiong, and S. Fan, “A Repetitive Control Scheme for Harmonic Suppression of Circulating Current in Modular Multilevel Converters,” *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 471–481, Jan 2015.
- [90] Q.-C. Zhong and T. Hornik, “Cascaded Current-Voltage Control to Improve the Power Quality for a Grid-Connected Inverter With a Local Load,” *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1344–1355, 2013.
- [91] T. Hornik and Q.-C. Zhong, “ H^∞ repetitive voltage control of grid-connected inverters with a frequency adaptive mechanism,” *IET Power Electronics*, vol. 3, no. 6, pp. 925–935, Nov 2010.

- [92] S. Alepuz, S. Busquets-Monge, J. Bordonau, J. Gago, D. Gonzalez, and J. Balcells, "Interfacing Renewable Energy Sources to the Utility Grid Using a Three-Level Inverter," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1504–1511, Oct 2006.
- [93] J. Burl, *Linear Optimal Control: H^2 and H^∞ Methods*. Addison Wesley Longman, 1999.
- [94] P. Cortes, M. Kazmierkowski, R. Kennel, D. Quevedo, and J. Rodriguez, "Predictive Control in Power Electronics and Drives," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 12, pp. 4312–4324, Dec 2008.
- [95] K. P. Gokhale, A. Kawamura, and R. Hoft, "Dead Beat Microprocessor Control of PWM Inverter for Sinusoidal Output Waveform Synthesis," *IEEE Transactions on Industry Applications*, vol. IA-23, no. 5, pp. 901–910, Sept 1987.
- [96] T. Kawabata, T. Miyashita, and Y. Yamamoto, "Dead beat control of three phase PWM inverter," *IEEE Transactions on Power Electronics*, vol. 5, no. 1, pp. 21–28, Jan 1990.
- [97] L. Malesani, P. Mattavelli, and S. Buso, "Robust dead-beat current control for PWM rectifiers and active filters," *IEEE Transactions on Industry Applications*, vol. 35, no. 3, pp. 613–620, May 1999.
- [98] S. Kouro, P. Cortes, R. Vargas, U. Ammann, and J. Rodriguez, "Model Predictive Control—A Simple and Powerful Method to Control Power Converters," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, pp. 1826–1838, June 2009.
- [99] J. Rodriguez, J. Pontt, C. Silva, P. Correa, P. Lezana, P. Cortes, and U. Ammann, "Predictive Current Control of a Voltage Source Inverter," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 1, pp. 495–503, Feb 2007.
- [100] P. Cortes, J. Rodriguez, D. Quevedo, and C. Silva, "Predictive Current Control Strategy With Imposed Load Current Spectrum," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 612–618, March 2008.
- [101] P. Acuna, L. Moran, M. Rivera, J. Dixon, and J. Rodriguez, "Improved Active Power Filter Performance for Renewable Power Generation Systems," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 687–694, Feb 2014.
- [102] R. M. K. Kennel, M. Kazmierkowski, and J. Rodriguez, "Predictive Control - A Simple and Powerful Method to Control Power Converters and Drives," Sept. 2014, IEEE ECCE 2014 Tutorial.
- [103] S. Buso and P. Mattavelli, *Digital Control in Power Electronics*, 2nd ed. Morgan & Claypool, 2015.

- [104] P. Cortes, S. Kouro, B. La Rocca, R. Vargas, J. Rodriguez, J. Leon, S. Vazquez, and L. Franquelo, "Guidelines for weighting factors design in Model Predictive Control of power converters and drives," in *IEEE International Conference on Industrial Technology (ICIT)*, Feb 2009, pp. 1–7.
- [105] A. Kawamura, T. Haneyoshi, and R. Hoft, "Deadbeat controlled PWM inverter with parameter estimation using only voltage sensor," *IEEE Transactions on Power Electronics*, vol. 3, no. 2, pp. 118–125, Apr 1988.
- [106] Y.-R. Mohamed and E. El-Saadany, "An Improved Deadbeat Current Control Scheme With a Novel Adaptive Self-Tuning Load Model for a Three-Phase PWM Voltage-Source Inverter," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 2, pp. 747–759, April 2007.
- [107] L. Malesani and P. Tenti, "A novel hysteresis control method for current-controlled voltage-source PWM inverters with constant modulation frequency," *IEEE Transactions on Industry Applications*, vol. 26, no. 1, pp. 88–92, Jan 1990.
- [108] L. Malesani, P. Mattavelli, and P. Tomasin, "Improved constant-frequency hysteresis current control of VSI inverters with simple feedforward bandwidth prediction," *IEEE Transactions on Industry Applications*, vol. 33, no. 5, pp. 1194–1202, Sep 1997.
- [109] S. Buso, S. Fasolo, L. Malesani, and P. Mattavelli, "A dead-beat adaptive hysteresis current control," *IEEE Transactions on Industry Applications*, vol. 36, no. 4, pp. 1174–1180, 2000.
- [110] D. Zmood and D. Holmes, "A generalised approach to the modulation of current source inverters," in *IEEE Power Electronics Specialists Conference (PESC)*, vol. 1, May 1998, pp. 739–745 vol.1.
- [111] Q. Yao and D. Holmes, "A simple, novel method for variable-hysteresis-band current control of a three phase inverter with constant switching frequency," in *IEEE Industry Applications Society Annual Meeting*, Oct 1993, pp. 1122–1129 vol.2.
- [112] F. Wu, F. Feng, L. Luo, J. Duan, and L. Sun, "Sampling Period Online Adjusting-Based Hysteresis Current Control Without Band With Constant Switching Frequency," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 270–277, Jan 2015.
- [113] S. Buso and T. Caldognetto, "A non-linear wide bandwidth digital current controller for DC-DC and DC-AC converters," in *Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Oct 2014, pp. 1090–1096.
- [114] J. Rocabert, A. Luna, F. Blaabjerg, and P. Rodríguez, "Control of Power Converters in AC Microgrids," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4734–4749, 2012.

- [115] M. Monfared, S. Golestan, and J. M. Guerrero, "Analysis, Design, and Experimental Verification of a Synchronous Reference Frame Voltage Control for Single-Phase Inverters," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 1, pp. 258–269, 2014.
- [116] J.-F. Chen and C.-L. Chu, "Combination Voltage-Controlled and Current-Controlled PWM Inverters for UPS Parallel Operation," *IEEE Transactions on Power Electronics*, vol. 10, no. 5, pp. 547–558, Sep 1995.
- [117] L. Zeng and L. Jinjun, "A control strategy for seamless transfer and smoothing power fluctuation of microgrid," in *7th International Power Electronics and Motion Control Conference (IPEMC'12)*, vol. 1, Conference Proceedings, pp. 136–140.
- [118] "Reference technical rules for the connection of active and passive users to the lv electrical utilities," *CEI 0-21*, pp. 1–146, 2012.
- [119] Y. Wang, P. Zhang, W. Li, W. Xiao, and A. Abdollahi, "Online Overvoltage Prevention Control of Photovoltaic Generators in Microgrids," *IEEE Transactions on Smart Grid*, vol. 3, no. 4, pp. 2071–2078, Dec 2012.
- [120] A. R. Bergen and V. Vittal, *Power Systems Analysis*, 2nd ed. Prentice Hall, 2000.
- [121] F. Gao and M. Iravani, "A Control Strategy for a Distributed Generation Unit in Grid-Connected and Autonomous Modes of Operation," *IEEE Transactions on Power Delivery*, vol. 23, no. 2, pp. 850–859, April 2008.
- [122] M. Ashabani and Y.-R. Mohamed, "Novel Comprehensive Control Framework for Incorporating VSCs to Smart Power Grids Using Bidirectional Synchronous-VSC," *IEEE Transactions on Power Systems*, vol. 29, no. 2, pp. 943–957, March 2014.
- [123] B. Shoeiby, R. Davoodnezhad, D. Holmes, and B. McGrath, "A New Current Control Droop Strategy for VSI-Based Islanded Microgrids," in *International Power Electronics Conference (IPEC)*, May 2014, pp. 1482–1489.
- [124] —, "Voltage-Frequency Control of an Islanded Microgrid using the Intrinsic Droop Characteristics of Resonant Current Regulators," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2014, pp. 68–75.
- [125] —, "A Resonant Current Regulator Based Microgrid Control Strategy with Smooth Transition Between Islanded and Grid-Connected Modes," in *IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, June 2014, pp. 1–8.
- [126] J. M. Guerrero, J. Matas, L. Garcia De Vicuna, M. Castilla, and J. Miret, "Wireless-Control Strategy for Parallel Operation of Distributed-Generation Inverters," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1461–1470, Oct 2006.

- [127] M.-B. Ghorbal, W. Ghzaiel, I. Slama-Belkhodja, and J. Guerrero, "Online Detection and Estimation of Grid Impedance Variation for Distributed Power Generation," in *IEEE Mediterranean Electrotechnical Conference (MELECON)*, March 2012, pp. 555–560.
- [128] A. Riccobono, S. Naqvi, A. Monti, T. Caldognetto, J. Siegers, and E. Santi, "Online wideband identification of single-phase AC power grid impedances using an existing grid-tied power electronic inverter," in *IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Jun. 2015, pp. 1–8.
- [129] J. Guerrero, L. Garcia De Vicuna, J. Matas, M. Castilla, and J. Miret, "Output Impedance Design of Parallel-Connected UPS Inverters With Wireless Load-Sharing Control," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 4, pp. 1126–1135, Aug 2005.
- [130] J. Guerrero, J. Matas, L. G. de Vicuna, M. Castilla, and J. Miret, "Decentralized Control for Parallel Operation of Distributed Generation Inverters Using Resistive Output Impedance," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 2, pp. 994–1004, April 2007.
- [131] N. Watson, T. Scott, and S. Hirsch, "Implications for Distribution Networks of High Penetration of Compact Fluorescent Lamps," *IEEE Transactions on Power Delivery*, vol. 24, no. 3, pp. 1521–1528, July 2009.
- [132] D. Salles, C. Jiang, W. Xu, W. Freitas, and H. Mazin, "Assessing the Collective Harmonic Impact of Modern Residential Loads—Part I: Methodology," *IEEE Transactions on Power Delivery*, vol. 27, no. 4, pp. 1937–1946, Oct 2012.
- [133] C. Jiang, D. Salles, W. Xu, and W. Freitas, "Assessing the Collective Harmonic Impact of Modern Residential Loads—2014;Part II: Applications," *IEEE Transactions on Power Delivery*, vol. 27, no. 4, pp. 1947–1955, Oct 2012.
- [134] "IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems," *IEEE Std 519-2014 (Revision of IEEE Std 519-1992)*, pp. 1–29, June 2014.
- [135] D. Thomas, "Conducted emissions in distribution systems (1 kHz-1 MHz)," *IEEE Electromagnetic Compatibility Magazine*, vol. 2, no. 2, pp. 101–104, Second 2013.
- [136] J. Enslin and P. J. Heskes, "Harmonic Interaction Between a Large Number of Distributed Power Inverters and the Distribution Network," *IEEE Transactions on Power Electronics*, vol. 19, no. 6, pp. 1586–1593, Nov 2004.
- [137] S. Munir and Y. W. Li, "Residential Distribution System Harmonic Compensation Using PV Interfacing Inverter," *IEEE Transactions on Smart Grid*, vol. 4, no. 2, pp. 816–827, June 2013.

- [138] H. Akagi, "Control Strategy and Site Selection of a Shunt Active Filter for Damping of Harmonic Propagation in Power Distribution Systems," *IEEE Transactions on Power Delivery*, vol. 12, no. 1, pp. 354–363, Jan 1997.
- [139] V. Vorperian, *Fast Analytical Techniques for Electrical and Electronic Circuits*. Cambridge University Press, 2002.
- [140] J. He, Y. W. Li, and M. Munir, "A Flexible Harmonic Control Approach Through Voltage-Controlled DG–Grid Interfacing Converters," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 1, pp. 444–455, Jan 2012.
- [141] H. Han, X. Hou, J. Yang, J. Wu, M. Su, and J. Guerrero, "Review of Power Sharing Control Strategies for Islanding Operation of AC Microgrids," *IEEE Transactions on Smart Grid*, vol. 7, no. 1, pp. 200–215, Jan 2016.
- [142] K. Siri, C. Lee, and T.-F. Wu, "Current Distribution Control For Parallel Connected Converters: Part I," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 28, no. 3, pp. 829–840, Jul 1992.
- [143] A. Roslan, K. Ahmed, S. Finney, and B. Williams, "Improved Instantaneous Average Current-Sharing Control Scheme for Parallel-Connected Inverter Considering Line Impedance Impact in Microgrid Networks," *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 702–716, March 2011.
- [144] X. Sun, Y.-S. Lee, and D. Xu, "Modeling, analysis, and implementation of parallel multi-inverter systems with instantaneous average-current-sharing scheme," *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 844–856, May 2003.
- [145] J. W. Simpson-Porco, F. Dörfler, and F. Bullo, "Synchronization and power sharing for droop-controlled inverters in islanded microgrids," *Automatica*, vol. 49, no. 9, pp. 2603 – 2611, 2013.
- [146] A. Bidram, F. Lewis, and A. Davoudi, "Distributed Control Systems for Small-Scale Power Networks: Using Multiagent Cooperative Control Theory," *IEEE Control Systems*, vol. 34, no. 6, pp. 56–77, Dec 2014.
- [147] J. Simpson-Porco, Q. Shafiee, F. Dorfler, J. Vasquez, J. Guerrero, and F. Bullo, "Secondary Frequency and Voltage Control of Islanded Microgrids via Distributed Averaging," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 11, pp. 7025–7038, Nov 2015.
- [148] S. Lissandron and P. Mattavelli, "A controller for the smooth transition from grid-connected to autonomous operation mode," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2014, pp. 4298–4305.
- [149] A. Engler and N. Soutanis, "Droop control in LV-grids," in *International Conference on Future Power Systems*, Nov 2005, pp. 6 pp.–6.

- [150] Q.-C. Zhong, “Robust Droop Controller for Accurate Proportional Load Sharing Among Inverters Operated in Parallel,” *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1281–1290, April 2013.
- [151] E. Crisostomi, M. Liu, M. Raugi, and R. Shorten, “Plug-and-Play Distributed Algorithms for Optimized Power Generation in a Microgrid,” *IEEE Transactions on Smart Grid*, vol. 5, no. 4, pp. 2145–2154, July 2014.
- [152] A. Borghetti, M. Bosetti, S. Grillo, S. Massucco, C. Nucci, M. Paolone, and F. Silvestro, “Short-Term Scheduling and Control of Active Distribution Systems With High Penetration of Renewable Resources,” *IEEE Systems Journal*, vol. 4, no. 3, pp. 313–322, Sept 2010.
- [153] Y. Levron, J. Guerrero, and Y. Beck, “Optimal Power Flow in Microgrids With Energy Storage,” *IEEE Transactions on Power Systems*, vol. 28, no. 3, pp. 3226–3234, Aug 2013.
- [154] K. Turitsyn, P. Sulc, S. Backhaus, and M. Chertkov, “Local Control of Reactive Power by Distributed Photovoltaic Generators,” in *First IEEE International Conference on Smart Grid Communications (SmartGridComm)*, Oct 2010, pp. 79–84.
- [155] ———, “Options for Control of Reactive Power by Distributed Photovoltaic Generators,” *Proceedings of the IEEE*, vol. 99, no. 6, pp. 1063–1073, June 2011.
- [156] J. Rocabert, G. Azevedo, I. Candela, R. Teoderescu, P. Rodriguez, and I. Etxebarria-Otadui, “Microgrid connection management based on an intelligent connection agent,” in *36th Annual Conference on IEEE Industrial Electronics Society (IECON)*, Nov 2010, pp. 3028–3033.
- [157] M. Hanif, V. Khadkikar, and P. Kanjiya, “Control and SRF-q based resynchronization of a master DG for microgrids,” in *6th IEEE Power India International Conference (PIICON)*, Dec 2014, pp. 1–6.
- [158] G. Azevedo, F. Bradaschia, M. Cavalcanti, F. Neves, J. Rocabert, and P. Rodriguez, “Safe transient operation of microgrids based on master-slave configuration,” in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2011, pp. 2191–2195.
- [159] A. Bellini, S. Bifaretti, and F. Giannini, “A Robust Synchronization Method for Centralized Microgrids,” *IEEE Transactions on Industry Applications*, vol. 51, no. 2, pp. 1602–1609, March 2015.
- [160] A. Micallef, M. Apap, C. Spiteri-Staines, and J. Guerrero, “Single-Phase Microgrid With Seamless Transition Capabilities Between Modes of Operation,” *IEEE Transactions on Smart Grid*, vol. 6, no. 6, pp. 2736–2745, Nov 2015.
- [161] N. Hoffmann and F. W. Fuchs, “Minimal Invasive Equivalent Grid Impedance Estimation in Inductive-Resistive Power Networks Using Extended Kalman Filter,” *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 631–641, 2014.

- [162] A. Khamis, H. Shareef, E. Bizkevelci, and T. Khatib, "A review of islanding detection techniques for renewable distributed generation systems," *Renewable and Sustainable Energy Reviews*, vol. 28, pp. 483 – 493, 2013.
- [163] S. McArthur, E. Davidson, V. Catterson, A. Dimeas, N. Hatziargyriou, F. Ponci, and T. Funabashi, "Multi-Agent Systems for Power Engineering Applications–Part I: Concepts, Approaches, and Technical Challenges," *IEEE Transactions on Power Systems*, vol. 22, no. 4, pp. 1743–1752, Nov 2007.
- [164] N. Hatziargyriou, *Microgrids: Architectures and Control*. Wiley-IEEE Press, 2014.
- [165] A. Monti, R. Liu, A. Deshmukh, F. Ponci, and R. Dougal, "Towards a new fully-flexible control approach for distributed Power Electronics Building Block systems," in *34th Annual Conference of IEEE Industrial Electronics (IECON)*, Nov 2008, pp. 2955–2961.
- [166] L. Meng, A. Luna, E. Diaz, B. Sun, T. Dragicevic, M. Savaghebi, J. Vasquez, J. Guerrero, and M. Graells, "Flexible System Integration and Advanced Hierarchical Control Architectures in the Microgrid Research Laboratory of Aalborg University," *IEEE Transactions on Industry Applications*, 2015.
- [167] Y. Yan, Y. Qian, H. Sharif, and D. Tipper, "A survey on smart grid communication infrastructures: Motivations, requirements and challenges," *Communications Surveys Tutorials, IEEE*, vol. 15, no. 1, pp. 5–20, First 2013.
- [168] C. Buccella, C. Cecati, and H. Latafat, "Digital Control of Power Converters - A Survey," *IEEE Transactions on Industrial Informatics*, vol. 8, no. 3, pp. 437–447, 2012.
- [169] T. Strasser, F. Andren, J. Kathan, C. Cecati, C. Buccella, P. Siano, P. Leitao, G. Zhabelova, V. Vyatkin, P. Vrba, and V. Marik, "A Review of Architectures and Concepts for Intelligence in Future Electric Energy Systems," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 4, pp. 2424–2438, 2015.
- [170] F. Blaabjerg, K. Ma, and Y. Yang, "Power electronics for renewable energy systems - status and trends," in *8th International Conference on Integrated Power Systems (CIPS'14)*, Conference Proceedings, pp. 1–11.
- [171] (2015, November) FOX G20 - Linux Embedded Single Board Computer. [Online]. Available: <http://www.acmesystems.it/FOXG20>
- [172] (2015, November) National Instruments Single Board RIO - General Purpose Inverter Controller. [Online]. Available: <http://www.ni.com/singleboard/gpic/>
- [173] (2015, November) Smart fusion customizable System on Chip. [Online]. Available: <http://www.actel.com/products/smartfusion/>

- [174] M. Vekić, S. Grabić, D. Majstorović, I. Čelanović, N. Čelanović, and V. Katić, “Ultra-low Latency HIL Platform for Rapid Development of Complex Power Electronics Systems,” *IEEE Trans. on Power Electronics*, vol. 27, no. 11, pp. 4436–4444, 2012.
- [175] B. Lu, X. Wu, H. Figueroa, and A. Monti, “A Low-Cost Real-Time Hardware-in-the-Loop Testing Approach of Power Electronics Controls,” *IEEE Trans. on Industrial Electronics*, vol. 54, no. 2, pp. 919–931, 2007.
- [176] J. Wang, Y. Song, W. Li, J. Guo, and A. Monti, “Development of a Universal Platform for Hardware In-the-Loop Testing of Microgrids,” *IEEE Transactions on Industrial Informatics*, vol. 10, no. 4, pp. 2154–2165, 2014.
- [177] (2013, November) National Instruments Compact RIO – High performance reconfigurable controller. [Online]. Available: <http://www.ni.com/compactrio/>
- [178] C. Graf, J. Maas, T. Schulte, and J. Weise-Emden, “Real-time HIL-simulation of Power Electronics,” in *Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE*, 2008, pp. 2829–2834.
- [179] A. Hasanzadeh, C. S. Edrington, N. Stroupe, and T. Bevis, “Real-Time Emulation of a High-Speed Microturbine Permanent-Magnet Synchronous Generator Using Multiplatform Hardware-in-the-Loop Realization,” *IEEE Transactions on Industrial Electronics*, vol. 61, no. 6, pp. 3109–3118, 2014.
- [180] T. Caldognetto, P. Tenti, A. Costabeber, and P. Mattavelli, “Improving Microgrid Performance by Cooperative Control of Distributed Energy Sources,” *IEEE Transactions on Industry Applications*, vol. 50, no. 6, pp. 3921–3930, 2014.
- [181] P. Tenti, A. Costabeber, T. Caldognetto, and P. Mattavelli, “Cooperative control of smart micro-grids based on conservative power commands,” *Przegląd Elektrotechniczny*, vol. 89, no. 6, pp. 32–40, 2013.
- [182] A. Costabeber, T. Erseghe, P. Tenti, S. Tomasin, and P. Mattavelli, “Optimization of micro-grid operation by dynamic grid mapping and token ring control,” in *Proceedings of the 2011-14th European Conference on Power Electronics and Applications (EPE'11)*, Conference Proceedings, pp. 1–10.
- [183] A. Costabeber, “Advanced Control of Power Converters for Efficient Use of Distributed Energy Resources in Future Smart Microgrids,” Ph.D. dissertation, Ph.D. School in Information Engineering—Information Science and Technology, 2012.
- [184] P. Tenti, A. Costabeber, D. Trombetti, and P. Mattavelli, “Plug and Play Operation of Distributed Energy Resources in Micro-Grids,” in *IEEE International Telecommunications Energy Conference (INTELEC)*, June 2010, pp. 1–6.
- [185] A. Costabeber, T. Erseghe, P. Tenti, S. Tomasin, and P. Mattavelli, “Optimization of Micro-Grid Operation by Dynamic Grid Mapping and Token Ring Control,” in *IEEE European Conference on Power Electronics and Applications (EPE)*, Aug 2011, pp. 1–10.

- [186] D. Dardari, A. Conti, U. Ferner, A. Giorgetti, and M. Win, "Ranging With Ultrawide Bandwidth Signals in Multipath Environments," *Proceedings of the IEEE*, vol. 97, no. 2, pp. 404–426, Feb 2009.
- [187] A. Angioni, A. Sadu, F. Ponci, A. Monti, D. Patel, F. Williams, D. Della Giustina, and A. Dede, "Coordinated voltage control in distribution grids with LTE based communication infrastructure," in *IEEE 15th International Conference on Environment and Electrical Engineering (EEEIC)*, June 2015, pp. 2090–2095.
- [188] B. Kroposki, R. Lasseter, T. Ise, S. Morozumi, S. Papathanassiou, and N. Hatziaargyriou, "Making microgrids work," *IEEE Power and Energy Magazine*, vol. 6, no. 3, pp. 40–53, 2008.
- [189] D. E. Olivares, A. Mehrizi-Sani, A. H. Etemadi, C. A. Canizares, R. Iravani, M. Kazerani, A. H. Hajimiragha, O. Gomis-Bellmunt, M. Saeedifard, R. Palma-Behnke, G. A. Jimenez-Estevez, and N. D. Hatziaargyriou, "Trends in Microgrid Control," *IEEE Transactions on Smart Grid*, vol. 5, no. 4, pp. 1905–1919, 2014.
- [190] R. Abe, H. Taoka, and D. McQuilkin, "Digital Grid: Communicative Electrical Grids of the Future," *IEEE Transactions on Smart Grid*, vol. 2, no. 2, pp. 399–410, June 2011.
- [191] K. Hyosung, Y. Taesik, and C. Sewan, "Indirect Current Control Algorithm for Utility Interactive Inverters in Distributed Generation Systems," *IEEE Transactions on Power Electronics*, vol. 23, no. 3, pp. 1342–1347, 2008.
- [192] S. Buso, T. Caldognetto, and D. I. Brandao, "Comparison of oversampled current controllers for microgrid utility interface converters," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2015, pp. 6888–6895.
- [193] S. Chen, Y. M. Lai, S. C. Tan, and C. K. Tse, "Analysis and design of repetitive controller for harmonic elimination in PWM voltage source inverter systems," *IET Power Electronics*, vol. 1, no. 4, p. 497, 2008.
- [194] S. Buso and T. Caldognetto, "A Nonlinear Wide-Bandwidth Digital Current Controller for DC-DC and DC-AC Converters," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 12, pp. 7687–7695, Dec 2015.
- [195] S. Buso, T. Caldognetto, and D. Brandao, "Dead-Beat Current Controller for Voltage Source Converters with Improved Large Signal Response," *IEEE Transactions on Industry Applications*, 2015.
- [196] W.-T. Yan, K. Au, C.-m. Ho, and H.-H. Chung, "Fixed-Frequency Boundary Control of Buck Converter With Second-Order Switching Surface," *IEEE Transactions on Power Electronics*, vol. 24, no. 9, pp. 2193–2201, Sept 2009.
- [197] S. Maity and Y. Suraj, "Analysis and Modeling of an FFHC-Controlled DC-DC Buck Converter Suitable for Wide Range of Operating Conditions," *IEEE Transactions on Power Electronics*, vol. 27, no. 12, pp. 4914–4924, Dec 2012.

- [198] B. Bose, "An adaptive hysteresis-band current control technique of a voltage-fed PWM inverter for machine drive system," *IEEE Transactions on Industrial Electronics*, vol. 37, no. 5, pp. 402–408, Oct 1990.
- [199] R. Ramos, D. Biel, E. Fossas, and F. Guinjoan, "A fixed-frequency quasi-sliding control algorithm: application to power inverters design by means of FPGA implementation," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 344–355, Jan 2003.
- [200] K. Rahman, M. Khan, M. Choudhury, and M. Rahman, "Variable-band hysteresis current controllers for PWM voltage-source inverters," *IEEE Transactions on Power Electronics*, vol. 12, no. 6, pp. 964–970, Nov 1997.
- [201] C.-m. Ho, V. Cheung, and H.-H. Chung, "Constant-Frequency Hysteresis Current Control of Grid-Connected VSI Without Bandwidth Control," *IEEE Transactions on Power Electronics*, vol. 24, no. 11, pp. 2484–2495, Nov 2009.
- [202] J.-C. Olivier, J.-C. Le Claire, and L. Loron, "An Efficient Switching Frequency Limitation Process Applied to a High Dynamic Voltage Supply," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 153–162, Jan 2008.
- [203] D. Holmes, R. Davoodnezhad, and B. McGrath, "An Improved Three-Phase Variable-Band Hysteresis Current Regulator," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 441–450, Jan 2013.
- [204] F. Liu and A. Maswood, "A Novel Variable Hysteresis Band Current Control of Three-Phase Three-Level Unity PF Rectifier With Constant Switching Frequency," *IEEE Transactions on Power Electronics*, vol. 21, no. 6, pp. 1727–1734, Nov 2006.
- [205] D. Grant, "Frequency control of hysteretic power converter by adjusting hysteresis levels," Feb. 19 2002, US Patent 6,348,780.
- [206] A. Mihalka, "Fixed frequency hysteretic regulator," Apr. 26 2005, US Patent 6,885,175.
- [207] F. Su, W.-H. Ki, and C. ying Tsui, "Ultra Fast Fixed-Frequency Hysteretic Buck Converter With Maximum Charging Current Control and Adaptive Delay Compensation for DVS Applications," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 815–822, April 2008.
- [208] H. Young, M. Perez, J. Rodriguez, and H. Abu-Rub, "Assessing Finite-Control-Set Model Predictive Control: A Comparison with a Linear Current Controller in Two-Level Voltage Source Inverters," *IEEE Industrial Electronics Magazine*, vol. 8, no. 1, pp. 44–52, March 2014.
- [209] G. Bode, P. Loh, M. Newman, and D. Holmes, "An improved robust predictive current regulation algorithm," in *The Fifth International Conference on Power Electronics and Drive Systems (PEDS)*, vol. 2, Nov 2003, pp. 1058–1063 Vol.2.

- [210] P. Mattavelli, "An improved deadbeat control for UPS using disturbance observers," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, pp. 206–212, Feb 2005.
- [211] Q. Zeng and L. Chang, "An Advanced SVPWM-Based Predictive Current Controller for Three-Phase Inverters in Distributed Generation Systems," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 3, pp. 1235–1246, March 2008.
- [212] J. Guzinski and H. Abu-Rub, "Speed Sensorless Induction Motor Drive With Predictive Current Controller," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 2, pp. 699–709, Feb 2013.
- [213] L. Malesani, P. Mattavelli, and S. Buso, "Robust dead-beat current control for PWM rectifiers and active filters," in *The 1998 IEEE Industry Applications Conference. Thirty-Third IAS Annual Meeting.*, vol. 2, Oct 1998, pp. 1377–1384 vol.2.
- [214] M. Oettmeier, C. Heising, V. Staudt, and A. Steimel, "Dead-Beat Control Algorithm for Single-Phase 50-kW AC Railway Grid Representation," *IEEE Transactions on Industrial Electronics*, vol. 25, no. 5, pp. 1184–1192, May 2010.
- [215] A. Peterchev and S. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," in *IEEE 32nd Annual Power Electronics Specialists Conference (PESC)*, vol. 2, 2001, pp. 465–471 vol.2.
- [216] H. Peng, A. Prodic, E. Alarcon, and D. Maksimovic, "Modeling of Quantization Effects in Digitally Controlled DC-DC Converters," *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 208–215, Jan 2007.
- [217] M. Bradley, E. Alarcon, and O. Feely, "Design-Oriented Analysis of Quantization-Induced Limit Cycles in a Multiple-Sampled Digitally Controlled Buck Converter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 4, pp. 1192–1205, April 2014.
- [218] L. Corradini and P. Mattavelli, "Modeling of Multisampled Pulse Width Modulators for Digitally Controlled DC-DC Converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 1839–1847, July 2008.
- [219] H. Mahmood, D. Michaelson, and J. Jiang, "A Power Management Strategy for PV/Battery Hybrid Systems in Islanded Microgrids," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 4, pp. 870–882, Dec 2014.
- [220] T. Caldognetto, P. Tenti, P. Mattavelli, S. Buso, and D. I. Brandao, "Cooperative Compensation of Unwanted Current Terms in Low-Voltage Microgrids by Distributed Power-Based Control," in *IEEE Power Electronics Society-Southern Power Electronics Conference*, November 2015.
- [221] P. Carvalho, P. F. Correia, and L. Ferreira, "Distributed Reactive Power Generation Control for Voltage Rise Mitigation in Distribution Networks," *IEEE Transactions on Power Systems*, vol. 23, no. 2, pp. 766–772, May 2008.

- [222] R. Tonkoski, L. Lopes, and T. El-Fouly, “Coordinated Active Power Curtailment of Grid Connected PV Inverters for Overvoltage Prevention,” *IEEE Transactions on Sustainable Energy*, vol. 2, no. 2, pp. 139–147, April 2011.
- [223] M. Kabir, Y. Mishra, G. Ledwich, Z. Dong, and K. Wong, “Coordinated Control of Grid-Connected Photovoltaic Reactive Power and Battery Energy Storage Systems to Improve the Voltage Profile of a Residential Distribution Feeder,” *IEEE Transactions on Industrial Informatics*, vol. 10, no. 2, pp. 967–977, May 2014.
- [224] A. Anurag, Y. Yang, and F. Blaabjerg, “Thermal Performance and Reliability Analysis of Single-Phase PV Inverters with Reactive Power Injection Outside Feed-In Operating Hours,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. in press, 2015.
- [225] T. Stetz, F. Marten, and M. Braun, “Improved Low Voltage Grid-Integration of Photovoltaic Systems in Germany,” *IEEE Transactions on Sustainable Energy*, vol. 4, no. 2, pp. 534–542, 2013.
- [226] A. Ahmed, L. Ran, S. Moon, and J.-H. Park, “A Fast PV Power Tracking Control Algorithm With Reduced Power Mode,” *IEEE Transactions on Energy Conversion*, vol. 28, no. 3, pp. 565–575, 2013.
- [227] T. Caldognetto, S. Buso, and P. Mattavelli, “Digital Controller Development Methodology Based on Real-Time Simulations with LabVIEW FPGA Hardware-Software Toolset,” *Electronics Journal*, vol. 17, no. 2, pp. 110–117, 2013.
- [228] T. Caldognetto, S. Buso, P. Tenti, and D. Brandao, “Power-Based Control of Low-Voltage Microgrids,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2015.
- [229] S. Buso, T. Caldognetto, and D. Iglesias Brandao, “Oversampled dead-beat current controller for voltage source converters,” in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2015, pp. 1493–1500.
- [230] T. Caldognetto, S. Buso, P. Tenti, and D. I. Brandao, “Experimental verification of an active microgrid with distributed power-based control,” in *17th European Conference on Power Electronics and Applications (EPE, ECCE-Europe)*, Sept 2015, pp. 1–8.
- [231] ———, “A dynamic overvoltage limiting technique for low-voltage microgrids,” in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2015, pp. 2321–2327.
- [232] S. Buso and T. Caldognetto, “Rapid Prototyping of Digital Controllers for Microgrid Inverters,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 2, pp. 440–450, June 2015.