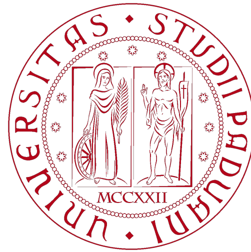

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Total Ionizing Dose Degradation Mechanisms in Nanometer-scale Microelectronic Technologies

Coordinator: Prof. Andrea Neviani
Supervisor: Prof. Alessandro Paccagnella
Co-Supervisor (University of Padova): Prof. Simone Gerardin
Co-Supervisor (Vanderbilt University): Prof. Daniel M. Fleetwood

Ph.D. Student: Stefano Bonaldo

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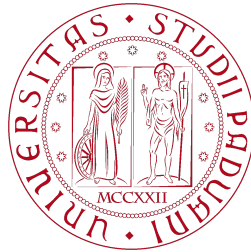

UNIVERSITÀ DEGLI STUDI DI PADOVA

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Corso di Dottorato in Ingegneria dell'Informazione

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Effetti e Meccanismi di Dose Totale in Transistors su Scala Nanometrica

Coordinatore: Ch.mo Prof. Andrea Neviani

Supervisore: Ch.mo Prof. Alessandro Paccagnella

Co-Supervisore (Università di Padova): Ch.mo Prof. Simone Gerardin

Co-Supervisore (Vanderbilt University): Ch.mo Prof. Daniel M. Fleetwood

Dottorando: Stefano Bonaldo

Anno Accademico 2018/2019

"Still examine it by a few experiments.
Nothing is too wonderful to be true,
if it be consistent with the laws of nature;
and in such things as these,
experiment is the best test of such consistency."

[MICHAEL FARADAY]

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Terminology

ASIC - Application Specific Integrated Circuit

CB - Conduction Band

CP - Charge Pumping

CTRW - Continuous Time Random Walk

DD - Displacement Damage

DFT - Density Functional Theory

DUT - Device Under Test

ESD - ElectroStatic Discharge

ELT - Enclosed Layout Transistor

GAA - Gate-All-Around

LHC - Large Hadron Collider

LET - Linear Energy Transfer

LLD - Lightly Doped Region

NWE - Narrow-Width Effect

RINCE - Radiation-Induced Narrow Channel Effect

RISCE - Radiation-Induced Short Channel Effect

RT - Room Temperature

RTN - Random Telegraph Noise

SEE - Single Event Effect

SCE - Short Channel Effect

SRB - Strain-Relaxed Buffer layer

STI - Shallow Trench Isolation

TCAD - Technology Computer-Aided Design

TID - Total Ionizing Dose

VB - Valence Band

VBO - Valence Band Offset

Abstract

(ENGLISH VERSION)

Total ionizing radiation may affect the electrical response of the electronic systems, inducing a variation of their nominal electrical characteristics and degrading their performance. The study of the radiation effects in microelectronic devices is essential in the space, avionic, and ground level applications affected by artificial and/or natural radiation environments, where the reliability is one of the most important requirements. In this thesis work, I investigate the total ionizing dose (TID) degradation mechanisms in several modern nanometer-scale technology nodes. The analysis of the TID mechanisms is focused on the evaluation of measurable effects affecting the electrical response of the devices and on the identification of the microscopical nature of the radiation-induced defects. Several transistors, based on MOSFET and FinFET structures of different manufacturers, have been tested under ionizing radiation at several temperatures, bias configurations, annealing conditions, and transistor dimensions. Technologies dedicated to high energy physics experiments have been tested at ultra-high doses, never explored thus far. Several different techniques, as DC static characterization, charge pumping and low frequency noise measurements as well as Technology Computer-Aided Design simulations, were used to identify location, density and energy levels of the radiation-induced defects. The experimental measurements presented in this work provide a unique and comprehensive set of data, pointing out the strong influence of the scaling down to the TID-induced phenomena in deeply scaled microelectronic transistors. TID mechanisms have been studied following the technological evolution of the devices at various nodes: 150 nm Si-based MOSFET, 65 nm Si-based MOSFET, 28 nm Si-based MOSFET with HfO_2 gate dielectric, 16 nm InGaAs-based FinFET with HfO_2/Al_2O_3 gate dielectrics and, at last, a new laboratory grade InGaAs MOSFET with Al_2O_3 gate dielectric. All results confirm the high TID tolerance of the thin gate oxide of nanoscaled technologies, due to the reduced charge trapping in the gate dielectric. However, the aggressive downsizing of devices has led to new TID-induced effects related to other thick oxides and modern production processes, e.g., shallow trench insulations oxides, spacer dielectrics, and halo implantations. In the case of compound semiconductors, I have observed how defects are associated to the properties at the interface between III-V materials and high-k dielectrics. New TID mechanisms appear, showing their dependence on irradiation/annealing bias condition, channel length, and channel width.

(VERSIONE IN ITALIANO)

Le radiazioni ionizzanti possono influenzare la risposta elettrica dei sistemi elettronici, inducendo una variazione della risposta elettrica nominale e degradandone le loro prestazioni. Lo studio degli effetti delle radiazioni nei dispositivi microelettronici è essenziale nelle applicazioni spaziali, avioniche e al suolo colpite da sorgenti artificiali e/o naturali, in cui l'affidabilità è uno dei requisiti più importanti. In questo lavoro di tesi, ho studiato i meccanismi di degrado indotti da dose ionizzante (TID) per diversi nodi tecnologici avanzati su scala nanometrica. L'analisi dei meccanismi da TID è focalizzata sulla valutazione degli effetti che influiscono sulla risposta elettrica dei dispositivi e sull'identificazione della natura microscopica dei difetti indotti da radiazione. Diversi transistor, basati su strutture MOSFET e FinFET di diversi produttori, sono stati testati con radiazioni ionizzanti a diverse temperature, configurazioni di polarizzazione, condizioni di annealing e dimensioni dei transistor. Le tecnologie dedicate agli esperimenti di fisica delle alte energie sono state testate a dosi ultra alte finora mai esplorate. Diverse tecniche, come la caratterizzazione statica in DC, il charge pumping e le misure di rumore 1/f a bassa frequenza, così come le simulazioni TCAD, sono state utilizzate per identificare la posizione, la densità e i livelli energetici dei difetti indotti da radiazioni. Le misure sperimentali presentate in questo lavoro forniscono un insieme unico e completo di dati che sottolineano la forte influenza della riduzione della dimensione sui meccanismi di danno da TID nei transistor moderni. I meccanismi TID sono stati studiati seguendo l'evoluzione tecnologica dei dispositivi in vari nodi: MOSFET in Si a 150 nm, MOSFET in Si a 65 nm, MOSFET in Si a 28 nm con dielettrico di gate in HfO_2, FinFET in InGaAs a 16 nm con dielettrico di gate in HfO_2/Al_2O_3 e, infine, un nuovo MOSFET in InGaAs ancora in fase sperimentale con dielettrico di gate in Al_2O_3. I risultati dei test di radiazione su dispositivi in Si confermano l'elevata tolleranza del dielettrico di gate a effetti da TID, grazie all'impiego di ossidi di gate estremamente sottili, che intrappolano modeste quantità di carica indotte dalla radiazione. Tuttavia, la miniaturizzazione dei dispositivi ha portato a nuovi fenomeni di degrado da TID associati a ossidi spessi e a processi di produzione moderni, come ad esempio agli ossidi di isolamento di campo STI, ai dielettrici di spacer e agli impianti di halo. Con la introduzione dei dispositivi basati su materiali III-V, ho osservato come gli effetti da TID siano nuovamente associati al dielettrico di gate in seguito all'elevata densità di difetti all'interfaccia dei materiali III-V con i dielettrici high-k di gate. In questo lavoro di tesi, i meccanismi da TID di ogni nodo tecnologico sono analizzati e discussi, dimostrando come ogni nodo tecnologico sia caratterizzato da differenti sensibilità dipendenti dalla condizione di polarizzazione, dalla lunghezza di canale e dalla larghezza di canale.

Introduction

Electronic circuits are used in several application fields where different degrees of radiation tolerance may be required [1–4]. The amount of radiation that semiconductor devices encounter during their lifecycle strongly depends on the radiation environment [3, 5, 6]. Typical applications within aggressive radiation environments are space and avionic systems, high energy physics experiments, nuclear power plants, medical diagnostic imaging and therapy, industrial imaging and material processing. When operated in these environments, solid-state devices may be directly struck by photons, electrons, protons, neutrons or heavier particles, inducing an alteration of their electrical response, which can cause a temporarily or a permanently malfunction of the electronic system [2–4]. Remarkably, even the terrestrial environment where everyday life takes place has become not exempt from radiation issues: chip downscaling and the massive use of electronics have made our society more vulnerable to the effects of terrestrial neutrons and radioactive contaminants in the chip and packaging materials.

One famous catastrophic event induced by ionizing radiation was the failure of the communication satellite Telstar 1 in 1962. A malfunction in the satellite control system was caused by the Total-Ionizing-Dose (TID) degradation of some bipolar junction transistors (BJTs) [7]. This unpredicted failure happened after an abrupt increase of radiation levels in the Van Allen belts due to high altitude nuclear tests from USA and USSR [8, 9].

The severity of the radiation-induced effects depends on the type of the device and on the energy and type of the incident particle [10, 11]. Different effects and relevant physical mechanisms may contribute to the degradation of the device performance, and they can be classified in three main categories: Total Ionizing Dose (TID) [12–14], Displacement Damage (DD) [15–17], and Single Event Effects (SEEs) [18–22]. TID and DD mechanisms are the results of a large number of micro-scale contributions elicited by the penetrating particles, whose effects add up over time. On the other side, a SEE occurs whenever an ionizing particle passes through a sensitive part of the device, generating a single and detectable effect into the device.

This work is focused on the TID mechanisms in modern semiconductor Field-Effect Transistors (FETs), i.e., MOSFETs and FinFETs [23–27]. TID effects are induced by

the Coulomb interaction between the device materials and the ionizing particles, which generate charges that can be collected and trapped in some sensitive part of the device. These charges are typically stuck in the insulator materials, and cause parametric shifts in the transistor electrical response [12–14]. The research on the basic degradation mechanisms is of great interest and essential to ensure the reliability of the electronic devices. An extensive knowledge of the TID mechanisms allows to develop rad-hard circuits and design techniques to improve the tolerance of electronic circuits working in some specific applications, limiting failures and costs [28]. However, the continuous scaling down of the device dimensions combined with the introduction of new structures and materials [29–31] in the fabrication processes have led to new TID mechanisms and effects, that need to be continuously explored along with the scaling down of the technology nodes.

In this thesis work, I investigate the total ionizing dose (TID) degradation mechanisms in several modern nanometer-scale technology nodes. The parametric shift in the electrical response of the devices and the microscopic nature of the radiation-induced defects are investigated in several transistors of different manufacturers. The TID response of the devices are tested at several temperatures, bias configurations, annealing conditions and for several transistor dimensions. The type, location, density and energy levels of the radiation-induced defects are investigated through DC static characterizations, charge pumping, and low frequency noise measurements. The purpose of this study is to assess the qualitative response of the tested devices, trying to understand the TID mechanisms, and not to qualify them. This work provides a unique and comprehensive set of data, pointing out the strong influence of the scaling down on the TID-induced phenomena in modern microelectronics. Experimental results confirm the high TID tolerance of the extremely thin gate oxide of nanoscale technologies. However, the device scaling down has given rise to new TID-induced effects related to other thick oxides and specific fabrication production processes, e.g., shallow trench insulations oxides, spacer dielectrics, and halo implantations, while new defects appear associated to the properties of interface between III-V materials and high-k dielectrics. Each of the thesis chapters presents and discusses the TID mechanisms of a technological node, following the technological evolution of the devices: namely, 150 nm Si-based MOSFET; 65 nm Si-based MOSFET; 28 nm Si-based MOSFET with HfO_2 gate dielectric; 16 nm Si-based FinFET with HfO_2/Al_2O_3 gate dielectric; and a new laboratory-grade InGaAs MOSFET with Al_2O_3 gate dielectric.

In order to fully interpret the experimental results, and thus to be able to predict the device responses in a variety of radiation environments, Chapter 1 presents the state-of-the-art knowledge about TID mechanisms. The radiation induced effects related to the gate oxide are analyzed in terms of generation, transport, and trapping of radiation-induced charges in the oxides and along the oxide/semiconductor interface. New recent findings are discussed to underline the importance of TID degradation phenomena related to charge trapping in the shallow trench insolation and spacer dielectrics.

In Chapter 2, I present the TID results of 150 nm Si MOSFET technology, which has

been qualified for space applications up to 125 krad(SiO_2). I show the degradation of core and I/O transistors with different channel dimensions due to the radiation-induced defects related to the STI and gate oxides. The comparison between I/O and core transistors evidences the strong influence of the dielectric thicknesses to the TID sensitivity. At the end of the chapter, I also present the TID response of an operational amplifier designed by using 150 nm MOSFETs, in order to evaluate how the single transistor degradation can affect a more complex electronic system.

Chapter 3 shows the TID response of 65 nm Si MOSFET technology up to ultra-high doses (1 Grad(SiO_2)) for high energy physics applications. The very thin oxide thickness makes these devices insensitive to the effects of charge buildup in the gate oxide. Their TID response is dominated by the charge trapping into STI and new experimental evidence points out high density of trapped charges within the spacer oxides, used for the fabrication of the lightly doped regions. Through charge pumping measurements, I investigate the density of interface traps under the spacers, identifying a new interesting distribution of interface traps, whose generation is strongly influenced by the applied bias during the irradiation. Experimental results are finally combined with Technology Computer-Aided Design (TCAD) simulations to support the interpretation of the charge buildup mechanism related to the spacer dielectrics.

Chapter 4 analyzes the TID effects in 28 nm Si MOSFET technology at ultra-high doses (1 Grad(SiO_2)) for high energy physics applications. The TID degradation depends strongly on the channel width and channel length. Surprisingly, the channel length characteristics are the opposite of those previously found in 65 nm MOSFETs: the shortest channel device is the most tolerant to TID. By comparing the experimental responses with Technology Computer-Aided Design simulations, I demonstrate that this new channel-length effect is due to the presence of the halo implantations, introduced in the fabrication process to overcome the problem of the threshold voltage drop in short channel devices. Finally, I discuss the TID degradation at several doses, as different mechanisms can dominate the TID response depending on the quantity of cumulated dose.

In Chapter 5, I show the TID response of III-V material devices, in particular the 16 nm InGaAs FinFET technology. The high TID-induced degradation of these devices is related to the charge trapping in the defects of the HfO_2/Al_2O_3 gate dielectric. Therefore I investigate the microscopic nature, densities and energies of defects through an extensive experimental characterization using DC static measurements, hysteresis responses, and $1/f$ low frequency noise from cryogenic to high temperatures. The results are interpreted by using Density Functional Theory (DFT) simulations, pointing out the important role of oxygen vacancies in Al_2O_3 and HfO_2 dielectrics in the radiation-induced charge trapping.

In Chapter 6, I discuss about TID mechanisms in a laboratory-grade InGaAs MOSFETs. These devices are produced on InP substrate with Al_2O_3 high-k gate stack. TID effects visible in the DC static characteristics are dominated by net positive charge trapping in the gate oxide, border traps, and interface traps. Hysteresis and I_d-V_{gs} measurements

from cryogenic to high temperatures confirm that positive charge trapping derives from oxygen vacancies in Al_2O_3, while acceptor defects responsible for the hysteresis are most likely dangling Al bonds in the near-interfacial Al_2O_3.

Finally, Chapter 7 summarizes all the results obtained.

Chapter 1

Basic Mechanism of the TID in MOSFET Devices

Total ionizing radiation may affect the electrical response of MOSFET devices, inducing a variation in their nominal electrical response and degrading their performance. The Total Ionizing Dose (TID) effects are based on the ionization of the device materials, generating charge that can be collected in some sensitive regions of the device. Insulators are the most sensitive materials. Indeed, ionizing radiation can induce significant charge buildup in the dielectrics and at the dielectric/semiconductor interfaces, leading to performance degradation or even to its complete failure.

In this chapter, I summarize the main concepts about the TID basic mechanisms in MOSFETs, as discussed in several books [32, 33] and articles [14, 34–36]. The analysis starts in the Section 1.1 with the description of phenomenas of electron-hole pair generation, hole transport, charge trapping and interface trap buildup in SiO_2 gate dielectrics. Then, in the Section 1.2, I describe the results of recent works [37–39] about the effects of the scaling down of the technology nodes. The reduced thickness of the gate stack has improved the sensitivity of the radiation effects related to the gate dielectric. However, the new insulator materials and layout structures of modern fabrication processes have led to TID degradation mechanisms related to other thick oxides, as the Shallow Trench Isolation (STI) and the spacers.

1.1 Basic TID mechanism in gate oxides

The TID is a cumulative effect based on the Coulomb interaction between the incident particle/photon and the electrons of the lattice of the material. In accordance with the International System of Units (SI), the Gray (Gy) is the unit of measure for the ionizing radiation dose, which is defined as the absorption of one joule of radiation energy by one kilogram of matter. An equivalent unit is the rad (1 rad = 0.01 Gy), which is typically used in the space community, as well as in this work. In general, the definition of dose D

is:

$$D = \frac{dE}{dm}\bigg|_e \qquad \left[\frac{\text{MeV}}{\text{g}}\right] \tag{1.1}$$

where the subscript e underlines that the energy is absorbed due to the electron interaction. The TID mainly depends on the type and the energy of the impinging particle or photon, as well as on the density of the material.

In this work, most of the radiation exposures are carried out through X-ray irradiators composed by a tungsten tube with peak energy deposition at 10 keV. On the basis of photon energy and target material, photons can interact with the matter through three main processes: photoelectric effect, Compton scattering and pair production [40, 41]. As shown in Figure 1.1, at 10 keV, the X-ray photons interact with silicon ($Z_{Si} = 14$) and silicon dioxide ($Z_O = 8$) materials mainly through photoelectric effect [42]. The phenomena of photoelectric effect is shown in Figure 1.2. The incident photon is completely absorbed by the target atom, which in turn releases an electron. Once the electron is released, an electron-hole (e-h) pair is generated. Meantime, another electron on an external orbit drops in the vacated state, causing the emission of a low-energy photon. The emitted electron can in turn directly ionize the surrounding material, generating e-h pairs along its path. The e-h pairs generation is the key element for the TID-induced damage. Typically, during an X-ray exposure, most of e-h pairs are induced by ionizing electrons generated by the interaction between photons and atoms rather than the photon itself.

When a MOS device is irradiated with ionizing radiation, electron-hole (e-h) pairs are generated in the dielectrics [12, 14, 34, 43, 44]. Electrons that escape initial recombination

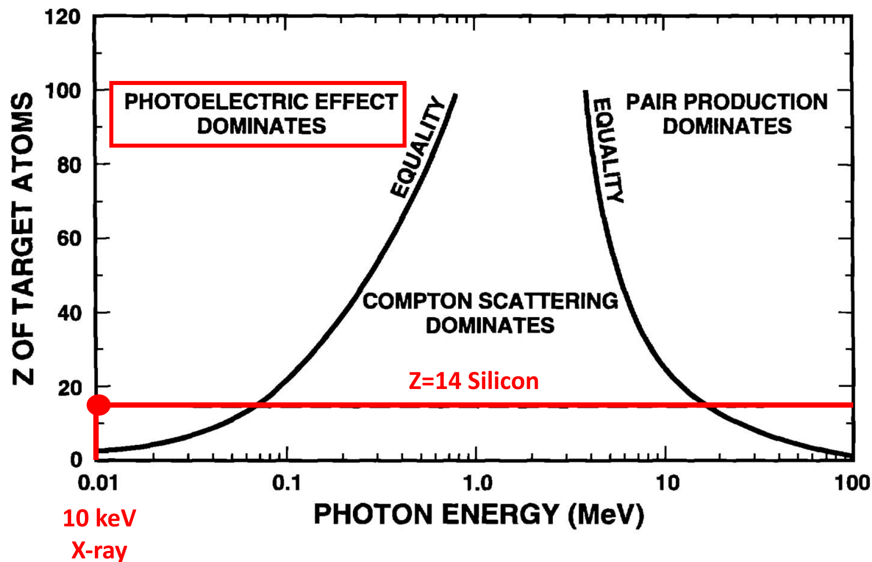


Figure 1.1: Relative weight of the main three photon-matter interaction processes at different energies of incident photon into several materials. The plot highlights in red that X-ray photons at 10 keV interact with matter through photoelectric effect. (After [40])

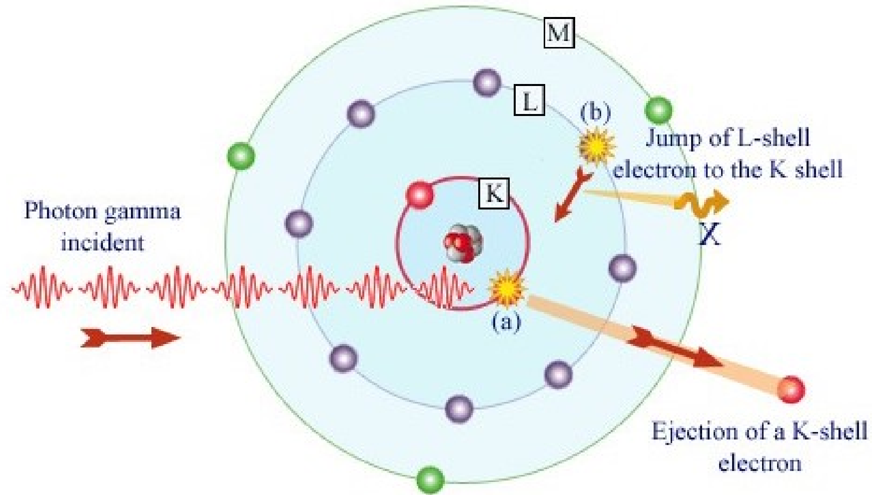


Figure 1.2: Schematic representation of the photoelectric effect.

are typically swept out of an oxide under bias in picoseconds [45]. Holes (positive charge) in SiO_2 have lower effective mobility than electrons and they are trapped in the insulator material. Trapped charges in the oxide can change the electrical properties of the device, degrading its performance. The analysis of the TID effects is here focused on the TID mechanism related to the gate oxide, but it can typically be extended to other dielectric layers used in the semiconductor devices. Figure 1.3 shows the energy band diagram of a Si nMOSFET with SiO_2 gate dielectric. The device is irradiated with ionizing radiation with positive voltage at the gate terminal. The TID degradation in the gate oxide follow these stages:

1. Ionization of the insulator with generation of e-h pairs.
2. Partial recombination of e-h pairs.
3. Hopping transport of holes through localized states.
4. Deep hole trapping and border traps.
5. Proton (H^+) release and formation of interface traps.

Each of these steps is now analyzed in detail.

1.1.1 Ionization of the insulator with generation of e-h pairs

When a X-ray photon impinges the device, it ionizes the semiconductor and insulator atoms, generating e-h pairs (step (1) of Figure 1.3). The energy needed to generate an e-h pair in SiO_2 is ~17 eV [46]. As long as the energies of the electrons and holes generated are higher than the minimum energy required to create an electron-hole pair, they can in turn generate additional e-h pairs. In this way, a single incident photon can induced a

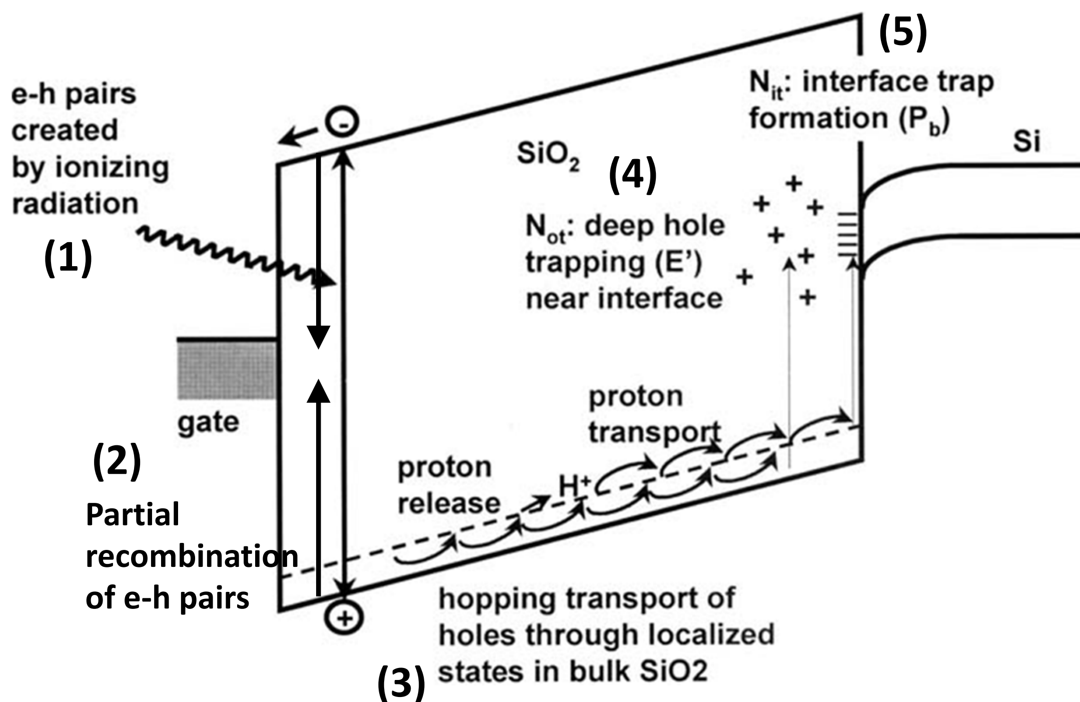


Figure 1.3: Illustration of the TID damage. The main processes of the TID mechanism related to the gate oxide are shown through the band diagram of a nMOSFET biased with positive voltage at gate. (After [41])

shower of e-h pairs. The charge pair volume density per rad is about 8.1 x10^{12} pairs/cm^3 [12].

Immediately after the generation of e-h pairs, the positive field applied at the gate drifts most of electrons out of the gate oxide within picoseconds. This rapid phenomena is possible thanks to the high mobility of electrons in SiO_2. On the contrary, the effective mobility of the holes in SiO_2 is extremely low, several orders of magnitude lower than the electron one [43, 47, 48]. Therefore, holes become trapped in the gate oxide [45, 49].

1.1.2 Partial recombination of e-h pairs

Within the time of picoseconds needed for electrons to leave the oxide, some electrons recombine with the holes. The fraction of e-h pairs escaping recombination is called the electron-hole yield or charge yield. The amount of initial recombination is highly dependent on the magnitude of the electric field through the oxide and on the energy and type of incident particle/photon [43].

The influence of the electric field to the charge yield is shown in Figure 1.4 for low-energy protons, alpha particles, gamma rays (Co-60), and X-rays [41, 50]. For all radiation types, the charge yield increases by increasing the electric field, as the probability that a hole will recombine with an electron decreases. The energy and type of the incident particle

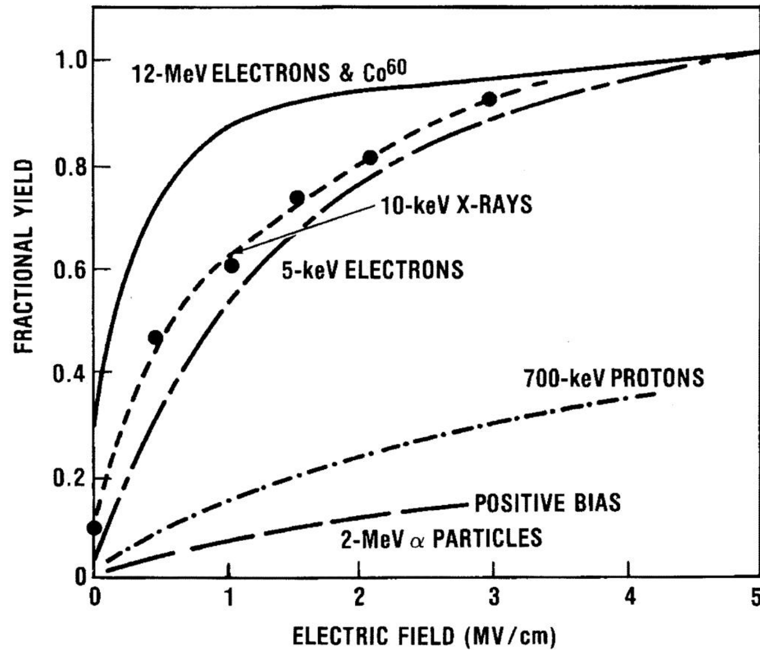


Figure 1.4: Charge yield as a function of applied field for different types of incident particles or photons. (From [12])

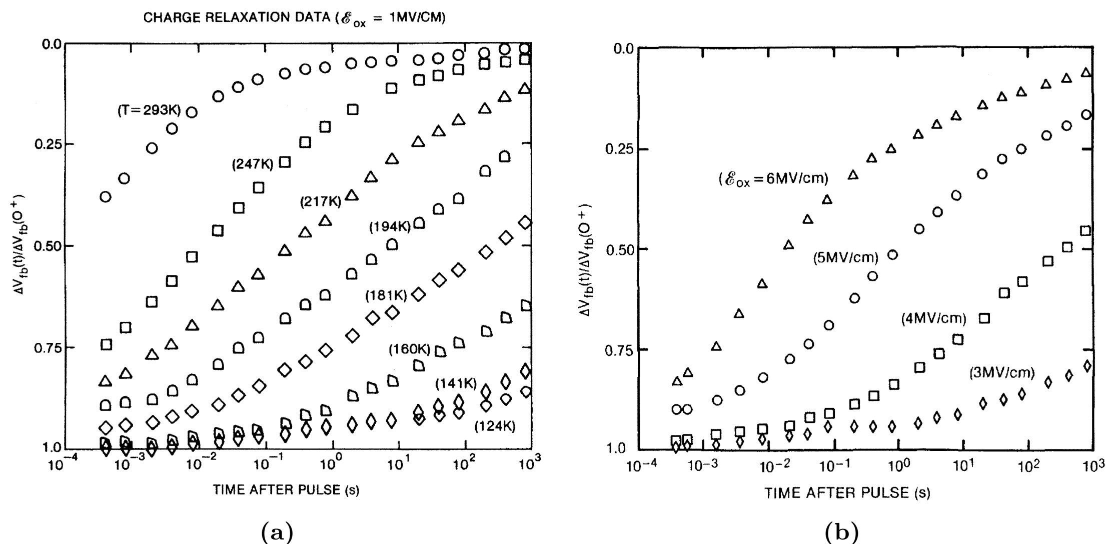
determine its ionization power. Radiation with high ionization power form dense columns of charge with high densities of e-h pairs. High densities of e-h pairs limit the average spacing between generated e-h pairs, consequently promoting the recombination (high recombination rates). On the other hand, weakly ionizing particles generate relatively isolated e-h pairs, decreasing the recombination likelihood (low recombination rates) [43]. For this reason, two models have been defined to study the recombination and the charge yield: the geminate model and the columnar model. In the geminate model, the average separation between e-h pairs is much greater than the thermalization distance needed for the e-h recombination. In this way, the recombination is treated singularly in each e-h pair, while interactions with other e-h pairs are neglected [51, 52]. In the columnar model, the separation between pairs is much less than thermalization distance (5 nm) [51]. High numbers of electrons are nearby the generated holes and the probability of recombination is consequently much greater compared to the geminate case [53].

1.1.3 Hopping transport of holes through localized states

The generated holes in the oxide are drifted slowly by the electric field, depending on its direction and magnitude. Accordingly to Figure 1.3, the applied positive field at the gate drifts the trapped holes toward the SiO_2/Si channel interface. The hole transport follows the Continuous Time Random Walk (CTRW) hopping transport mechanism [41, 54, 55]. In the CTRW mechanism, the transport happens through small polaron

hopping of holes between localized shallow trap states characterized by a random spatial distribution with average separation of about 1 nm. The term polaron refers to the situation where a charged carrier interacts strongly with the surrounding medium, creating a lattice distortion in its immediate vicinity [54]. As a hole moves through SiO_2, a distortion of the local potential field of the SiO_2 is induced by its charge. This local distortion increases the trap depth at the localized site, which tends to confine the hole to its immediate vicinity. Therefore, the hole tends to trap itself at the localized site.

Polaron hopping makes hole transport dispersive, as hole transport occurs over many decades in time after a radiation pulse. Hole transport depends on temperature and magnitude of electrical field [41, 54, 55]. Figure 1.5 highlights the influence of temperature and electric field on the hole transport [12]. The variation of the flatband voltage in a MOS structure is plotted as a function of the time needed to remove the effect of the radiation-induced trapped charge after a fast irradiation pulse. The gate oxide is irradiated with a 12 MeV electron pulse of 4 μs [12]. The fast pulse was neccessary to minimize the time between the end of the generation/recombination process and the measurements. In Figure 1.5(a), the variation of the flatband voltage is measured at different temperatures under an electrical field of 1 MV/cm, while, in Figure 1.5(b), the variation of the flatband voltage is measured at different electrical field at 79 K. Finally, Figure 1.7, the flatband voltage shift is plotted as a function of the scaled time $t/t_{1/2}$ [12]. The time $t_{1/2}$ is defined as the time needed to the flat-band voltage to recovery of 50%. The entire transport process covers 14 decades in time, and all the curves approximately overlap one to each others, indicating the universality and dispersion of the transport. The solid line is an analytical fit of the CTRW model (with α shape parameter = 0.25) [12].



(a) (b)

Figure 1.5: (a) Normalized flatband voltage recovery of MOS structure (t_{ox} = 96.5 nm) after a pulsed irradiation with 12 MeV electrons. (a) Irradiations at different temperatures with 1 MV/cm of electric field in the oxide. (b) Irradiations at different electric fields at 79 K. (From [12])

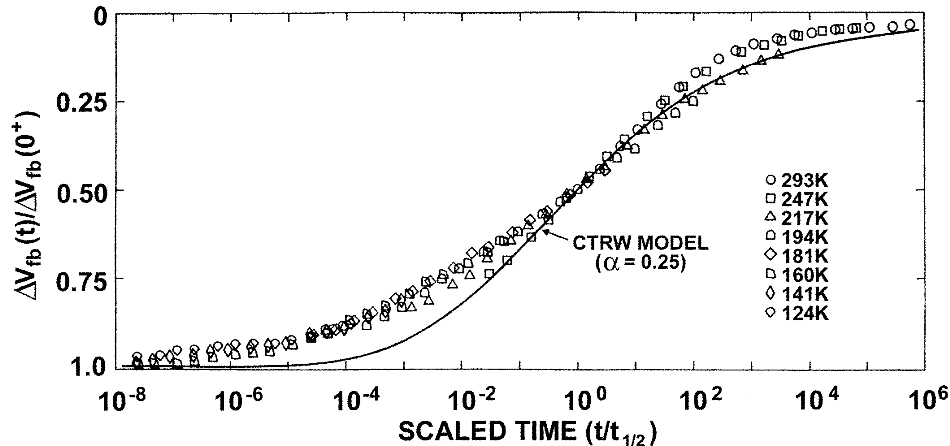


Figure 1.6: The normalized flatband recovery results shown in Figure 1.5(a) are re-scaled in time to half of the recovery time. The plot highlights the universal response with respect to temperature. Solid curve is retrieved by the CTRW model with $\alpha = 0.25$. (From [12])

Trapped holes in the gate oxide can be neutralized by two mechanisms: tunneling of electrons from the silicon into oxide traps, and thermal emission of electrons from the oxide valence band into oxide traps [56–58]. The dominant phenomena for the charge neutralization depends on the spatial and energy distributions of the oxide traps. Typically, oxide traps close to the SiO_2/Si interface are neutralized through electron tunneling. On the other hand, neutralization by thermal emission occurs when the energy levels of the oxide traps are close to the oxide valence band [58]. Other parameters, as temperature and applied electric field, can strongly affect the rate of neutralization.

1.1.4 Deep hole trapping and border traps

With the application of a positive gate bias, holes are drifted towards the SiO_2/Si interface. The SiO_2/Si interface is characterized by a large number of defects, as excess of Si atoms and oxygen vacancies, caused by the atomic mismatch of different type of materials and out-diffusion of oxygen atoms from the SiO_2 [59]. In particular, oxygen vacancies can act as hole trapping defects, called E' centers.

In defects caused by an oxygen vacancy, the localized atomic structure is formed by a strained and weak Si-Si bond, as shown in Figure 1.7 and in (a) of Figure 1.8. As soon as a radiation-induced hole reaches the strained Si-Si site, it can break the Si-Si bond by recombining with one of the two electrons shared between the Si atoms [59, 60]. When the strained bond is broken and the remaining electron of the Si-Si bond is shared between the two Si atoms, a E'_δ center is generated [59, 60]. The result is a structure composed by a positive trapped charge Si, as shown in (b) of Figure 1.8. However, if the remaining electron is associated with just one of the two Si atoms, the site become a dipole, which is asymmetric and positively charged. This site is called E'_γ center and it is formed by

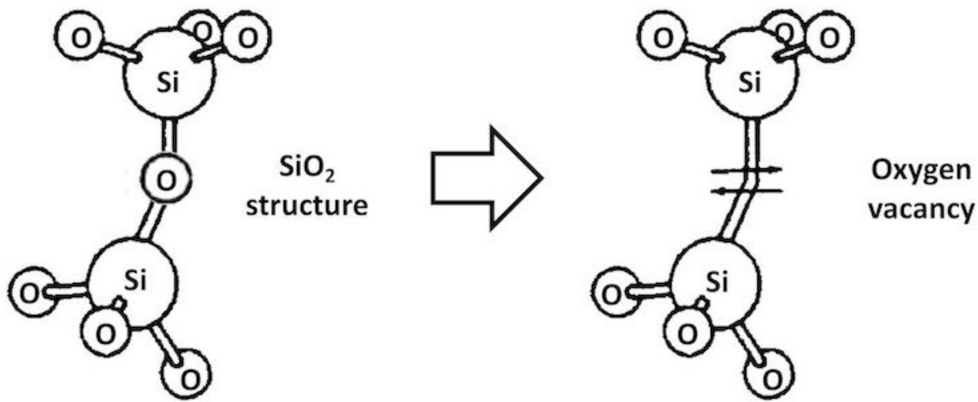


Figure 1.7: (a) Typical atomic structure of SiO_2 material layer. (b) Oxygen vacancy is a missing oxygen atoms in the SiO_2 material layer, responsible for the E' defects.

the positively charged Si atom and by the neutral Si atom with unpaired spin [59, 60]. In both E'$_\delta$ and E'$_\gamma$ centers, the result is the generation of a positive trapped charge.

Positive charges trapped in the E' centers can undergo a neutralization (annealing) process. The neutralization requires both the unpaired spin and the net positive charge

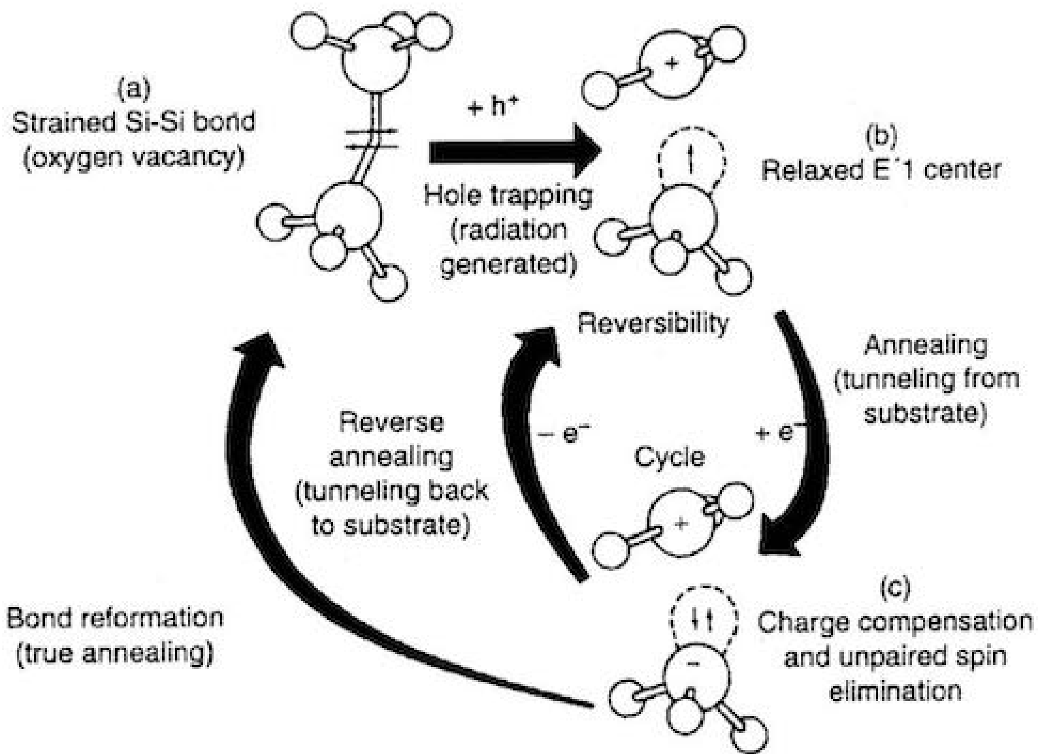


Figure 1.8: Generation and annealing of oxide trapped charge through an E' center. (From [60])

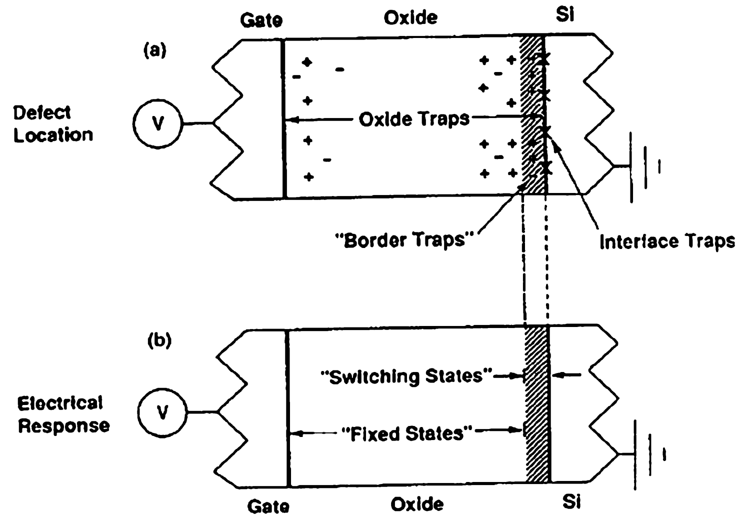


Figure 1.9: Schematic illustration of defects in MOS devices: oxide traps, border traps, and interface traps. (From [61])

to be removed at the same time. An electron can tunnel from the close Si substrate to the E' center, where it fills the half-filled orbital, neutralizes the positive net charge and eliminates the unpaired spin [59, 60] (see (c) of Figure 1.8). If the tunnelled electron recombines with the positively charged Si atom, the Si-Si bond is again established and the annealing is permanent, (c) → (a) of Figure 1.8. On the other hand, as the lattice has relaxed considerably more about the positively charged Si atom, the positively charged Si atom is typically a less attractive site from an energy standpoint than the neutral Si atom. Therefore, the tunnelled electron may be captured by the neutral Si atom, compensating electrically the positively charged neighboring Si. In this case, the bond between the two Si atoms is not reformed, and the extra electron can tunnel back out of the oxide, leaving again a net positive charge in particular when a negative bias is applied. This effect is called reverse annealing, (c) → (b) of Figure 1.8.

The neutralization likelihood of a trapped charge in the oxide through an electron coming from the silicon bulk depends on the distance between the oxide trap and the interface. Oxide traps relatively far from the interface have a very small probability to be reached by an electron injected from the Si substrate [57]. Therefore, the charge trapped in far E' centers is annealed by relatively long times through tunnelling electrons and/or by thermal emission [58]. This more stable traps are responsible for positive charge buildup in the gate oxide and TID degradation of the DC response, as shown in (1) and (2) of Figure 1.10. On the other side, if a trap is located close to the SiO_2/Si interface, it can exchange electrons with the Si substrate in relatively short times, depending on the applied electric field [62]. The E' centers located in the gate dielectric in the proximity of the SiO_2/Si interface are defined as border traps, as shown in Figure 1.9 [61, 63]. Border traps stay typically within 3 nm from the interface with emission and capture times in the range

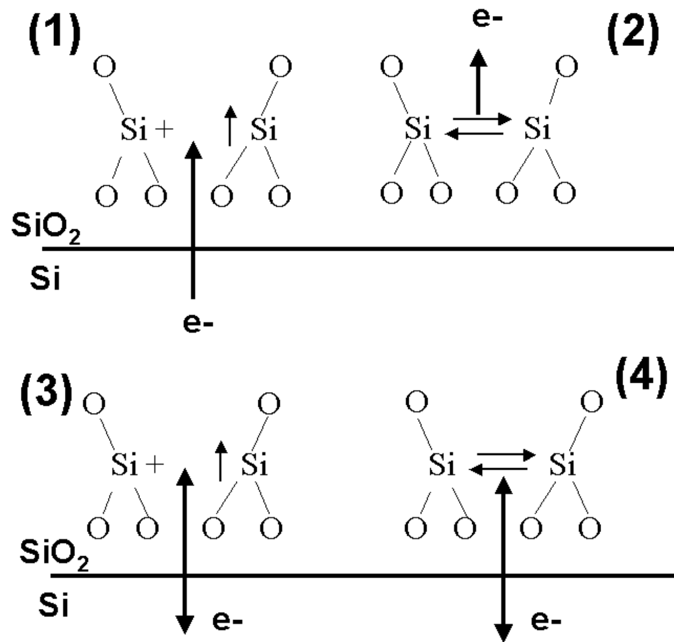


Figure 1.10: Schematic illustrations of the emission and capture of electrons in a E' center contributing to hole trapping 1), 2) and noise 3), 4). 1) An electron from the Si neutralizes the E' center. 2) An electron from a weak ≡Si-Si≡ defect is emitted, generating a positively charged E' defect shown in 1). 3) Noise due to electron exchange between the Si and a positively charged E' center. 4) Noise due to electron exchange between the Si and a weak ≡Si-Si≡ defect. (From [62])

between 0.01 s and 1 s and, due to their relatively low emission/capture times, they are responsible for hysteresis and low frequency $1/f$ noise, as shown in (3) and (4) of Figure 1.10 [62, 64].

1.1.5 Proton (H^+) release and formation of interface traps

Another major class of defects responsible for the TID degradation are interface traps. Interface traps is rapresented by located exactly at the interface between the oxide and the Si substrate layer. Similar to border traps, they also exchange charge with the Si channel, however, at difference from border traps, the capture and emission of charge in/out interface defects are possible with no barrier of carriers in the Si channel. The nature of interface traps is primarily dangling bond defects, called P_b centers [65]. These imperfections along the SiO_2/Si interface have a large impact on the carrier mobility and on the recombination rates of carriers in the channel. In Si MOS transistors with SiO_2 dielectric, the most important and abundant of these P_b centers is the P_{b0} defect, while marginal effects are typically due to a second defect type called P_{b1} [65]. Figure 1.11 shows a schematic illustration of P_{b0} and P_{b1} interface defects in (111), (110), and (100) Si substrates [66].

The process leading to the formation of interface traps follows the one of oxide

trapped charge through the e-h pair generation, recombination, and transport of holes in the gate oxide. The final step toward the generation of the radiation-induced interface traps is the formation of dangling bonds, whose formation depends mainly on two reactions. The first reaction is between the radiation-induced trapped holes and hydrogen containing oxide defects (D'H), which releases protons (H^+) [67]. Near and above room temperature, most interface traps are created by H^+ [68]. Thus, the creation of a P_b center primarily relies on the presence of H^+ near the interface [69]. A second potential sources of H^+ are the dopant-H complexes in the Si bulk [70]. Hole interactions with these hydrogen complexes can lead to the generation of H^+ that drift toward the interface under negative gate biases [70]. H^+ diffusing or driven by the electric field to the SiO_2 interface can interact with the hydrogens of the H-passivated dangling bonds (D) [67]. The formation of an interface dangling bond is summarized by the following reaction:

$$SiH + H^+ \Rightarrow D^+ + H_2 \tag{1.2}$$

The D^+ is the resulting dangling bond defect responsible for a P_b center.

In Si MOSFETs with SiO_2 gate dielectric, interface traps have an amphoteric behaviour. The P_b defects characterized by an energy level lower than the Si midgap are mostly donor-like, while defects in the upper part of Si midgap are acceptor-like [71–73]. As shown in Figure 1.12 the trap status of a P_b center depends on the position of the Fermi

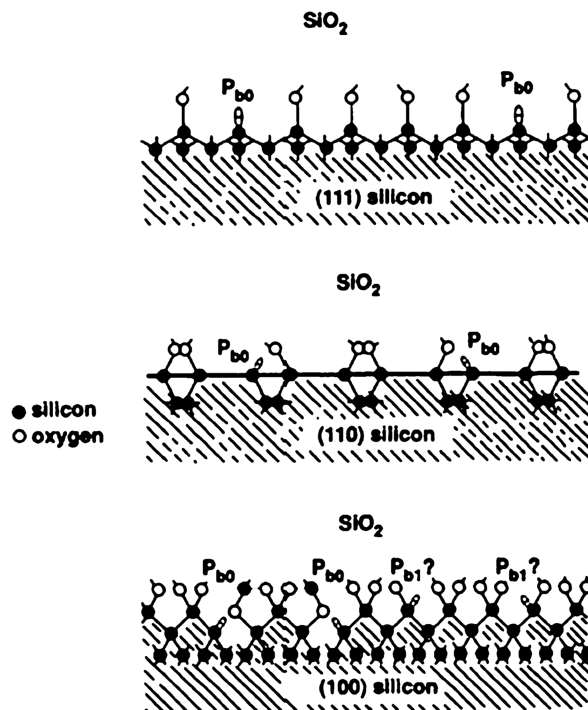


Figure 1.11: Illustration of the P_{b0} and P_{b1} interface trap defects on (111), (110), and (100) Si substrate. (From [66])

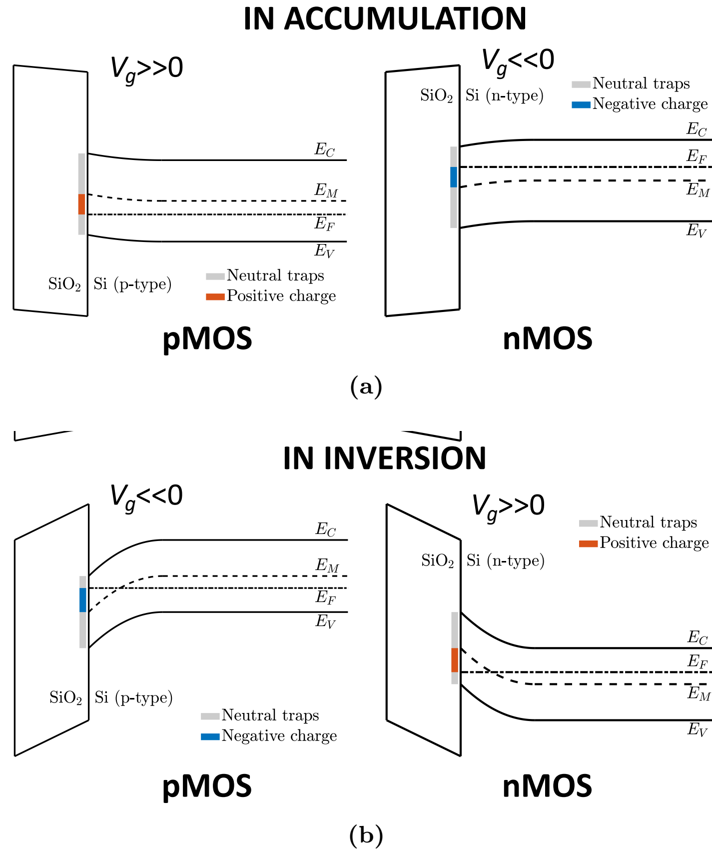


Figure 1.12: Energetic band diagram of MOS devices. The sign of the net trapped charge at the interface depends on the Fermi level position at the channel surface. (a) Off-state with channel in accumulation and (b) on-state with channel in inversion. (After [74])

level with respect to its energy level. Donor-like defects are neutral when they sit below the Fermi level, and they release an electron, consequently becoming positive, when they sit above the Fermi level. On the other side, acceptor-like defects are neutral above the Fermi level and they capture an electron, consequently becoming negative, when below the Fermi level [71–73]. Therefore, as shown in Figure 1.12, the sign of the net charge trapped at the interface depends on the applied gate bias, which control the Fermi level position at the surface. For example, in a nMOSFETs biased in inversion with $V_{gs} \gg 0$, the interface traps are negatively charged, while in pMOSFETs biased in inversion with $V_{gs} \ll 0$, interface traps are positively charged.

1.2 Gate-oxide related effects on the electrical response of MOSFETs

Radiation induces charge trapping in oxide, border, and interface traps [63]. The most efficient way to highlight the impact of each trap type is to measure the DC static I_d-V_{gs} response in linear region. Figure 1.13 shows schematically the typical I_d-V_{gs} curves of n-

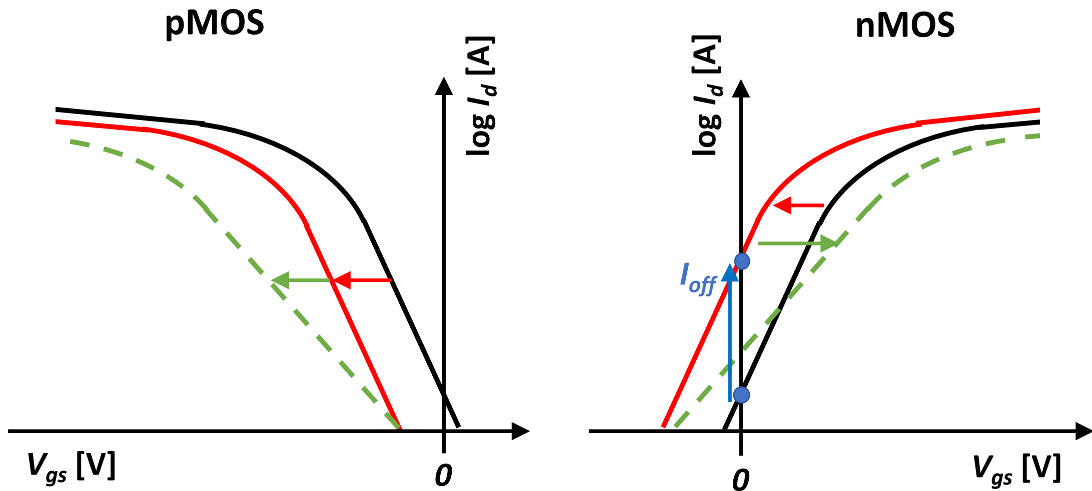


Figure 1.13: Illustration of the TID effects on the I_d-V_{gs} of MOS devices. The threshold voltage, sub-threshold and leakage current are evidenced. In black pre-rad devices, in red the effects of charges in the oxide (typically during irradiation) and in green the effects of interface traps.

and p-channel MOSFETs. The black curves indicate the response before the irradiation. In Si MOSFETs with SiO_2 gate dielectric, radiation generates hole (positive charge) trapping in the gate oxide. The effect of oxide trapped charge is shown by the red curves, which evidence a parallel shift of the I_d-V_{gs} [12, 13, 34]. In nMOSFETs, this shift leads to a reduction in threshold voltage and an increase in the off-state current I_{off} and in the maximum drain current I_{on-lin} at linear regime. In p-channel MOSFETs, the threshold voltage increases negatively, while I_{off} and I_{on-lin} currents are reduced. The threshold voltage shift induced by positive trapped charges in the oxide can be calculated by the following equation:

$$\Delta V_{ot} = \frac{t_{ox}}{k_{ox}\epsilon_0} q \Delta N_{ot} \tag{1.3}$$

where k_{ox} is the thickness of the gate oxide, k_{ox} is the dielectric constant of gate oxide and ϵ_0 is the permittivity of free space [75].

Interface traps have different effects on the responses of p-channel and n-channel transistors, due to their amphoteric nature [73]. The charge status of interface traps depends on the applied bias, which can trap or detrap the charge at the interface as the channel is swept from accumulation to inversion by the gate voltage. At midgap, interface-traps are neutral [73, 76] and do not impact the I_d-V_{gs} curve. Out of the midgap voltage, interface states influence the I_d-V_{gs} characteristics by stretching the curves in the subthreshold region. This is illustrated in Figure 1.13 by the green curves, showing the stretch-out towards more negative values for pMOSFETs, and the stretch-out towards more positive values for nMOSFETs. The different sign in the trapped charge induces substantial differences in the overall radiation response of pMOSFETs and nMOSFET.

In pMOSFETs, interface traps are predominantly positive, causing negative threshold-voltage shifts, while for an n-channel transistor interface traps are predominantly negative, causing positive threshold-voltage shifts [12, 13, 34]. In nMOSFETs, the negative charge trapped in the interface traps can compensate partially or completely the effects of the oxide trapped holes. When the effects of the negative charge dominates, a rebound effect is typically visible in the threshold voltage.

Border traps can also change charge state as the DC bias at gate is varied. In DC measurements, it is difficult to distinguish the effects of interface and border traps. The key difference between the interface and border traps is the rate at which the charge is exchanged between the trap and the substrate. Border traps are able to capture and emit electrons at slow time rates, typically $\lesssim$ 100 Hz [64]. On the contrary, the time rates of interface traps is typically $\gtrsim$ 1 kHz [61, 63]. In general, during an experimental measurement of the I_d-V_{gs} response, the border traps can contribute to hysteresis, subthreshold stretchout, and threshold voltage shift, depending on their emission/capture times compared to the measurement time. Traps with emission/capture rates slower than the total time for a V_{gs} sweep are able to contribute just to hysteresis and threshold voltage shift, but not to the subthreshold stretchout. On the contrary, border traps with emission/capture rates faster than the total time for a V_{gs} sweep are able to increase the subthreshold stretchout. Other measurement techniques, like C-V characteristics and low frequency 1/f noise, are typically used to investigate the effects of border traps, as it will be further discussed by presenting the experimental results in the next chapters [62].

1.3 Total ionizing dose vs. scaling down of the CMOS technology node

In the past decades, the scaling down of technology nodes was driven by the Moore's law [30, 31]. With the shrink of the SiO_2 gate layers to thickness close to 1 nm, the TID effects related to the gate oxide have become increasingly less problematic in electronic devices for both digital and analog applications [12, 13, 34, 36]. The relation between the gate oxide thickness and the radiation-induced charge trapping is shown in Figure 1.14 [77, 78], which plots the flatband voltage shift per unit dose of several MOS capacitors fabricated with different gate oxide thickness. In general, for thicknesses > 10 nm, the flatband voltage shift per unit dose decreases with a trend proportional to t_{ox}^2 [79]. For thicknesses < 10 nm, the decrease in hole trapping is much more rapid than the expected t_{ox}^2 dependence visible in thick oxide capacitors [36, 77, 78]. This abrupt decrease in the hole trapping is related to the tunnelling electrons, which neutralize the trapped holes located within the $\sim$ 3 nm of either the metal/oxide or oxide/semiconductor interfaces.

The relation between the gate oxide thickness and the radiation-induced generation of interface traps follows a similar trend of the gate oxide charge. Figure 1.15 reports the density of interface traps per unit dose as a function of the oxide thickness in several MOS

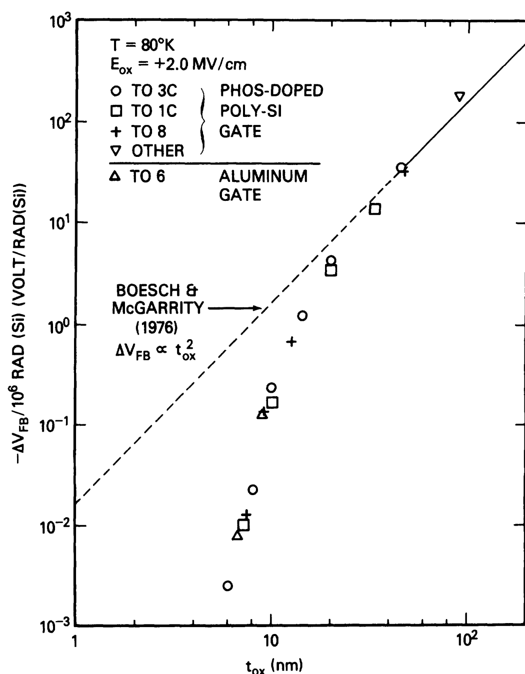


Figure 1.14: Flatband voltage shift per unit dose as a function of gate oxide thickness in MOS capacitors irradiated at 80 K with a Co-60 γ-rays. The dashed curve indicates the assumption of t_{ox}^2 dependence [79] for thick gate oxides. (From [77])

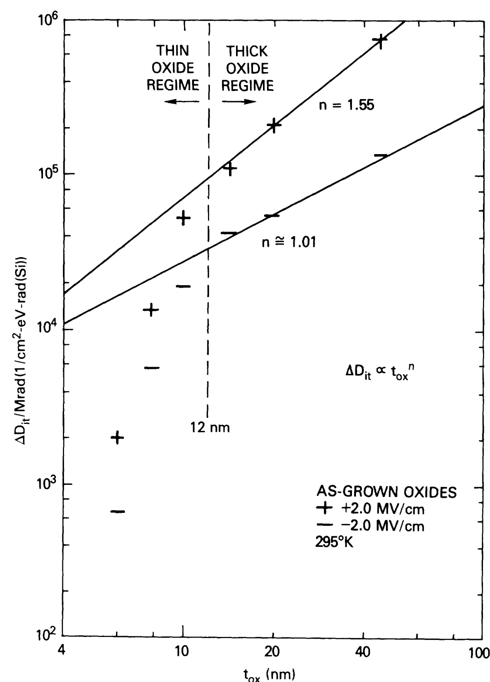


Figure 1.15: Density of interface traps per unit dose and energy D_{it} as a function of gate oxide thickness in MOS capacitors irradiated with Co-60 gamma rays in two different irradiation electric fields of $\pm$ 2 MV/cm. The values of D_{it} were estimated via the AC conductance method at 1 kHz. (From [80])

capacitors [80]. Similarly to the oxide charges, an abrupt reduction in the interface-trap density is visible at ultra-thin oxides < 10 nm. Tunnelling electrons from the metal/oxide or oxide/semiconductor interfaces neutralize the trapped hole in the oxide, avoiding the release of H^+ responsible for the interface traps buildup [68, 80–82]. Moreover, Figure 1.15 evidences higher densities of interface traps when the MOS is irradiated under positive bias than negative bias. This bias dependance is in agreements with the generation and release of H^+, which under positive bias are drifted toward the gate SiO_2/Si interface, where they can depassivate the Si-H bonds and generate interface traps [80].

The reduction of the TID effects related to gate oxide has a strong benefit the radiation response of MOSFET devices of modern technological nodes [36, 83]. However, TID effects have become less predictable with the advent of high-k gate materials and of alternative semiconductor materials and structures used by modern semiconductor industries [36]. Indeed, the gate oxide is not the unique insulator layer in modern MOSFETs. Recent works [37–39, 84] have pointed out other TID mechanisms related to other two dielectrics: the shallow trench isolation and the spacers.

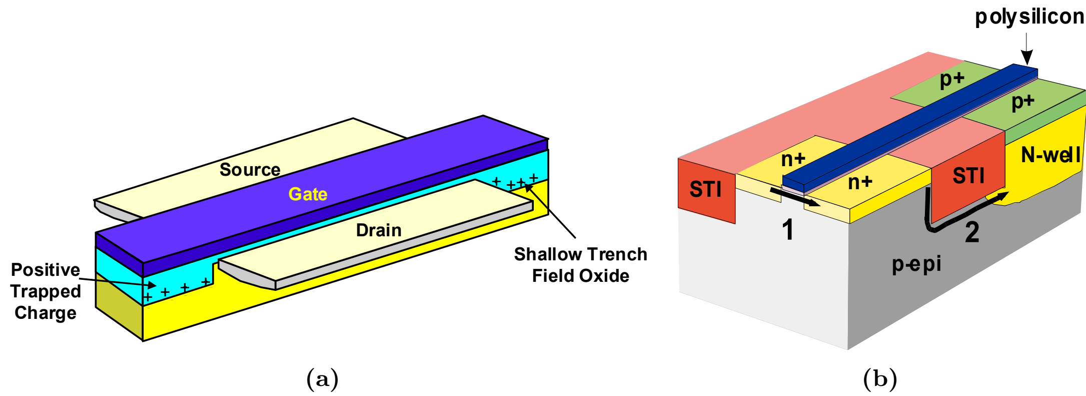


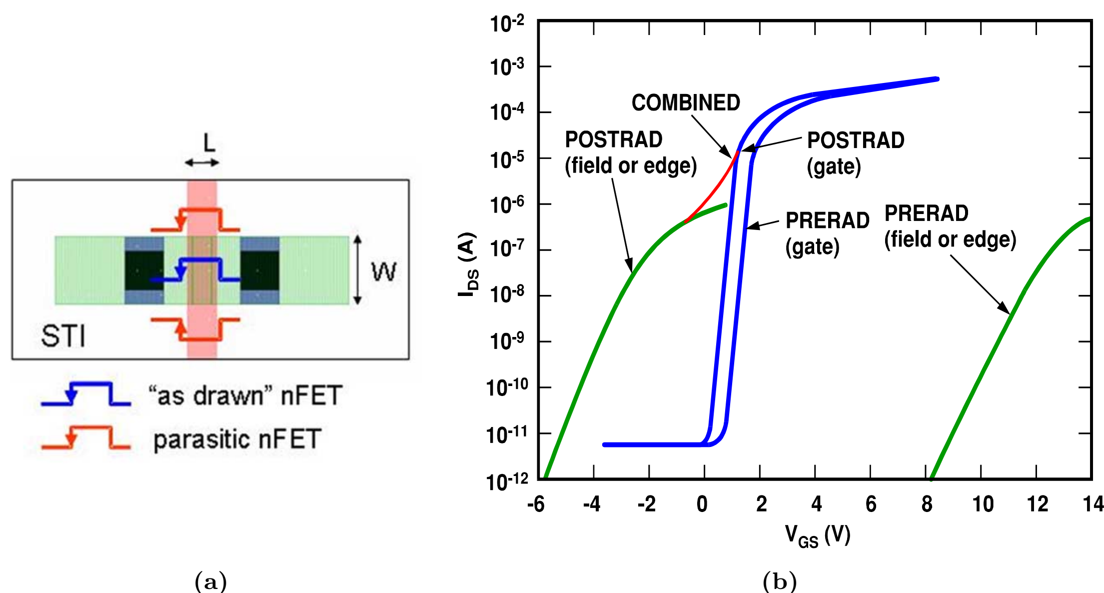
Figure 1.16: (a) Schematic representation of a transistor with STI. (b) The arrows indicate two possible leakage paths in technology nodes using STI. The first leakage path is at the edge of the gate-oxide transistor between the source and drain. The second leakage path occurs between the n-type source and drain regions of a nMOSFET and the n-well of an adjacent pMOSFET. (From [85] and [34])

1.3.1 STI-related effects (RINCE)

Shallow Trench Isolation (STI) oxides have been introduced since the 250 nm MOSFET node to replace their predecessors LOCOS [85]. STI are trenches of low quality SiO_2, which surround the device to prevent electric leakage currents between adjacent semiconductor components. STI oxides are much thicker than gate oxides. Typical field-oxide STI thicknesses are in the range of 100 nm to 1000 nm [85]. Unlike gate oxides that are typically grown by thermal oxidation, STI oxides are produced using a wide variety of deposition techniques, which are poorly controlled and are considerably different compared to those used for the gate oxides.

Radiation-induced degradation related to STI is caused by positive charge buildup in the STI oxides, as shown in Figure 1.16(a). Positive charge in the STI can significantly affect the radiation hardness of nanoscale transistors through two main degradation effects: increased radiation-induced standby currents and threshold voltage shifts in narrow-channel transistors, also called Radiation-Induced Narrow-Channel Effect (RINCE).

The causes of increased standby current are leakage paths created by the radiation-induced positive charge buildup in STI [38, 39, 74, 86]. The basic mechanisms for all STI-induced leakage phenomena are the same. Positive charge in STI oxides inverts the adjacent p-type Si regions, forming an inverted layer around the STI sidewalls. As the surface inverts, conducting paths are generated, markedly increasing the leakage current. As shown in Figure 1.16(b), these leakage paths include: 1) drain-to-source leakage in a single n-channel MOSFET, 2) source-to-well leakage between two different devices, and 3) drain-to-source leakage between two different devices (not shown in the Figure 1.16(b)) [34, 85]. These leakage paths will cause an increase in static power supply current of an IC with radiation. As the radiation-induced charge buildup in the STI oxides is predominantly



(a) (b)

Figure 1.17: (a) The STI-related effects are modelled with the n-channel MOSFET with two lateral parasitic n-channel transistors (From [13]). (b) Representative example of I_d-V_{gs} curves for a gate-oxide transistor and for its parasitic field-oxide transistor before and after the irradiation. The radiation-induces charge buildup in the STI oxide, shift the threshold voltage of the parasitic field-oxide transistors with a consequent increase in leakage current at $V_{gs} = 0$ V. (From [34]).

positive, its effect is usually most important for n-channel transistors [34, 38, 39].

In the drain-to-source leakage, the sidewalls of the trench oxide create a lateral leakage path which becomes the dominant contributor to off-state leakage current in n-channel MOSFETs [85]. As represented in Figure 1.17(a), the STI oxides (or field oxides) forms two parasitic field-oxide transistors in parallel with the main gate-oxide transistor [13]. At the edges of the gate transistor, the gate polysilicon extends over the field-oxide region, as shown in Figure 1.16(a). A parasitic field-oxide transistor consists of the gate polysilicon, a portion of the field oxide, and the source and drain of the gate transistor. The effect of the excess leakage current from a parasitic field-oxide transistor on the total drain current gate of the transistor is illustrated in Figure 1.17(b) ([34]). The plot reports the drain-to-source current I_{ds} versus the gate-to-source voltage V_{gs} for a n-channel MOSFET. The I_{ds} is shown for the parasitic field-oxide transistors and for the gate-oxide transistor before and after the irradiation. Because of the large thickness of the field oxide, the prerad threshold voltage of the parasitic field-oxide transistor is relatively large. During the irradiation, positive charge is trapped in the STI, causing a large negative threshold voltage shift of the parasitic field-oxide transistor. If the threshold voltage of the parasitic field-oxide transistor shifts enough to negative values (see Figure 1.17(b)), it can contribute to increase the off-state leakage current at $V_{gs} = 0$ V, preventing the gate oxide transistor to be completely turned off.

Figure 1.18 reports an example of experimental evidences about the catastrophic effects of charge buildup in the STI oxides. The plot shows the I_d-V_{gs} response of a nMOS-

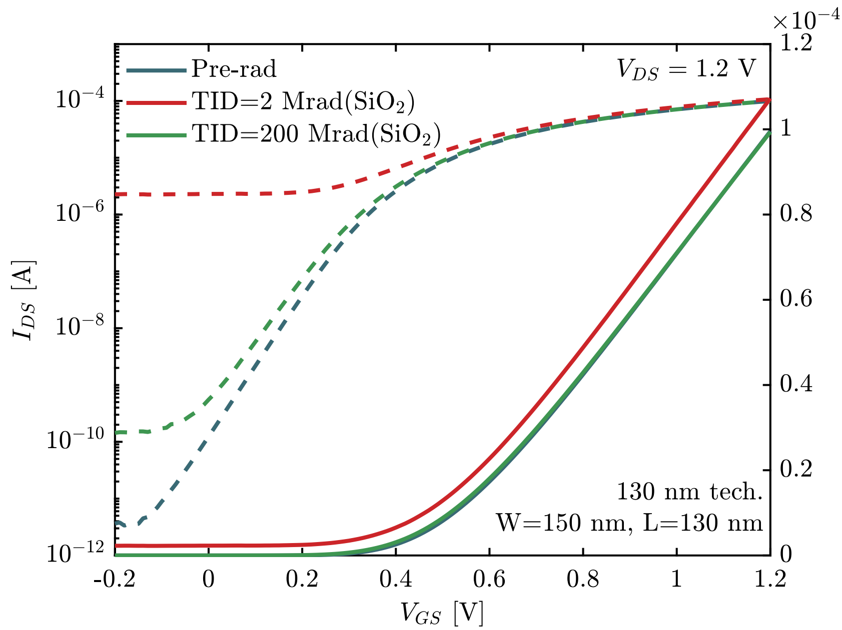


Figure 1.18: I_d-V_{gs} response at $V_{ds} = 1.2$ V of a nMOSFET produced in the 130 nm technology node. The device was irradiated with X-rays up to 200 Mrad(SiO_2). The dashed curves show the curves in logarithmic scale (left axis) while the solid curves refer to the characteristics in linear scale (right axis). (From [74])

FET built in the 130 nm technology node, irradiated with x-rays up to 200 Mrad(SiO_2) [74]. The characteristics are measured before the exposure, at 2 Mrad(SiO_2) and at 200 Mrad(SiO_2). At 2 Mrad(SiO_2), the drain-to-source leakage current increases of about six order of magnitude with an almost constant leakage current in the range -0.2 V $\lesssim V_{gs} \gtrsim$

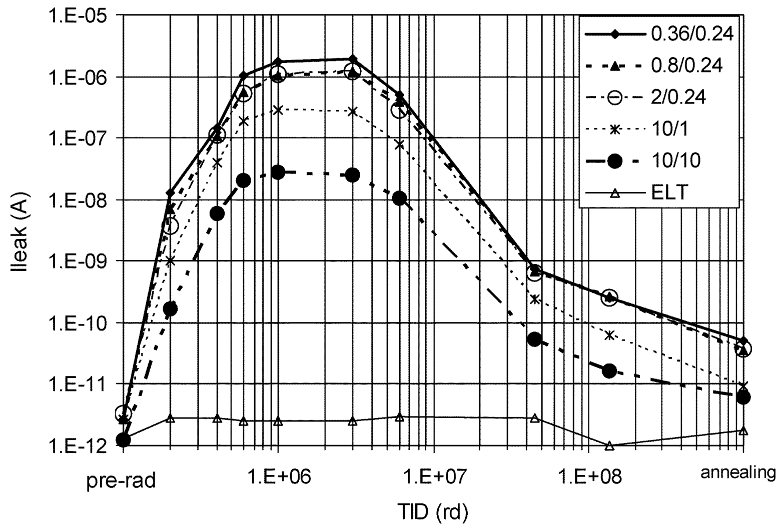


Figure 1.19: Leakage current (I_d at $V_{gs} = 0$ V) as a function of cumulated dose for nMOSFETs fabricated in a 130 nm commercial node. Devices were irradiated with X-rays up to 136 Mrad(SiO_2) and then annealed at 100 °C. (From [38])

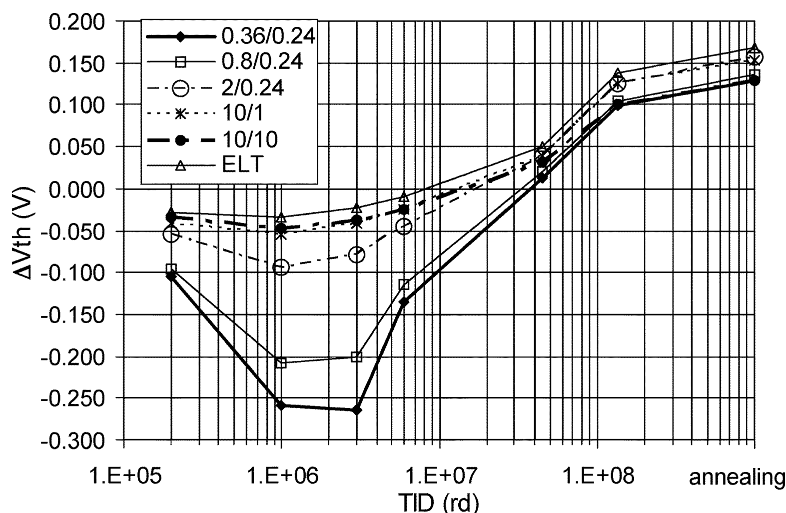


Figure 1.20: Threshold voltage shift as a function of cumulated dose for nMOSFETs fabricated in a 130 nm commercial node. Devices were irradiated with X-rays up to 136 Mrad(SiO_2) and then annealed at 100 °C. (From [38])

0.1 V. The insensitivity of the leakage current to V_{gs} indicates that the charge responsible for the inversion of the parasitic channels is probably extending in the lower part of the STI sidewalls, far from the STI-gate corner, where the gate control is weak or completely absent [86, 87]. At 200 Mrad(SiO_2), the leakage current decreases to the pre-rad values with a slight increase in the subthreshold stretchout. These two effects suggest generation of interface traps along the STI sidewalls. Indeed, interface traps can trap negative charge, which compensates the effect of the positive trapped charge in the STI oxides. The recover of the leakage is clearly visible in Figure 1.19 at ultra-high doses. Figure 1.19 plots the leakage current as a function of the dose for several nMOSFETs with different channel dimensions. The rebound of the leakage current occurs around 2 Mrad(SiO_2), when the generation of positive charge saturates and the formation of negative charge trapped at the interface makes it more difficult for the new positive charge to reverse the parasitic channels. Finally, Figure 1.19 highlights that the STI-induced leakage current is slightly dependant on the channel width, while it is completely suppressed in transistors designed with rad-hard solutions, i. e. the enclosed layout transistors (ELT) [38, 74]. The formation of the leakage current is a complex mechanisms that involves both oxide- and interface-trapped charge and depends on the quality of the STI oxides and on the applied bias during the irradiation, making quite difficult the prediction of its impact in the electronic circuits.

In addition to leakage-current, charge trapping in the STI of highly scaled technologies can lead to significantly larger-than-expected voltage shifts in narrow-channel devices [37, 38, 74]. This effect is named Radiation-Induced Narrow Channel Effect (RINCE) [37] and it affect the TID response of nMOSFETs and mostly pMOSFETs. The dependance of RINCE with the channel width is visible from the experimental data shown in Figure

1.22. The plot reports the threshold voltage shift as a function of the cumulated dose for nMOSFETs with different channel width in the 130 nm node. Narrow-channel transistors degrade more than large-channel transistors, while the ELT transistor is insensitive to RINCE effects. In narrow transistors, the two lateral STI are close to each others and the electrical field generated by the positive trapped charge in the STI can influence also the central part of the channel. Therefore, in narrow nMOSFETs, the positive charge in the STI contributes to invert the p-type substrate, inducing a decrease of the threshold voltage with cumulated dose [37]. At ≈ 2 Mrad(SiO_2), a rebound of the threshold voltage occurs due to the generation of interface traps along the gate oxide and the STI sidewalls, which compensate the positive charge, similarly to the rebound phenomena seen in the leakage current of Figure 1.19. At doses $\gtrsim$ 100 Mrad(SiO_2), the negative charge in interface traps dominates the TID response and the threshold voltage is shifted toward positive values.

On the contrary, in narrow-channel pMOSFETs, positive charge in the STI can contribute to accumulate the n-type substrate, shifting the threshold voltage toward higher values [37]. Figure 1.21 summarizes the variation of the maximum drain current, the threshold voltage shift and the maximum transconductance degradation of nMOSFETs and pMOSFETs designed in the 130 nm node. Devices with identical channel length

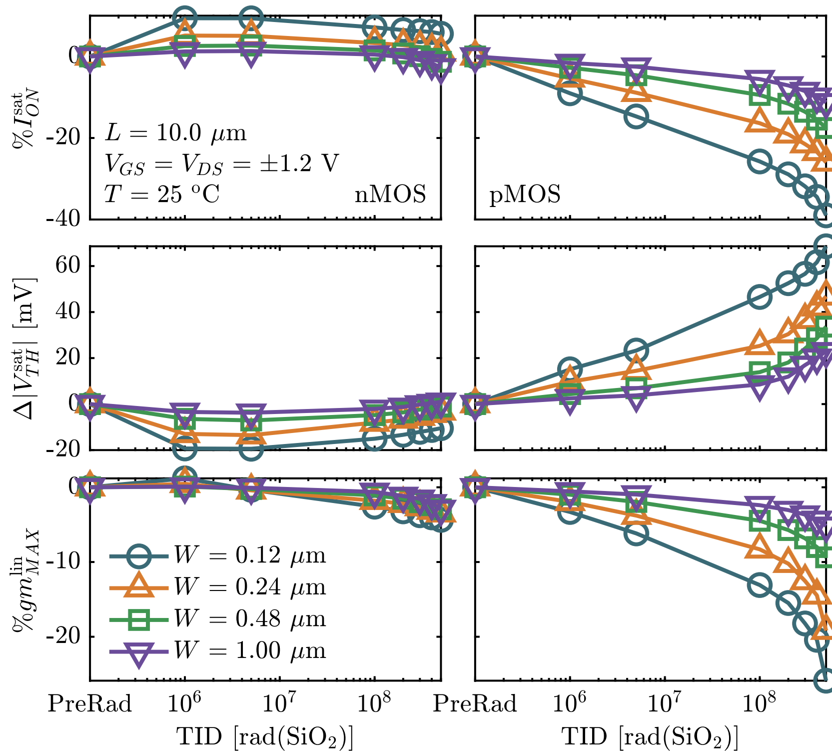


Figure 1.21: Degradation of the maximum drain current, threshold voltage shift and maximum trasconductance degradation of nMOSFETs and pMOSFETs with different channel width and identical channel length of 10 μm. Devices were measured in linear region (V_{ds} ¡ $V_{gs} - V_{th}$). In both pMOSFETs and nMOSFETs, the TID degradation is channel-width dependent with worst-case in narrow-channel transitors. (From [74])

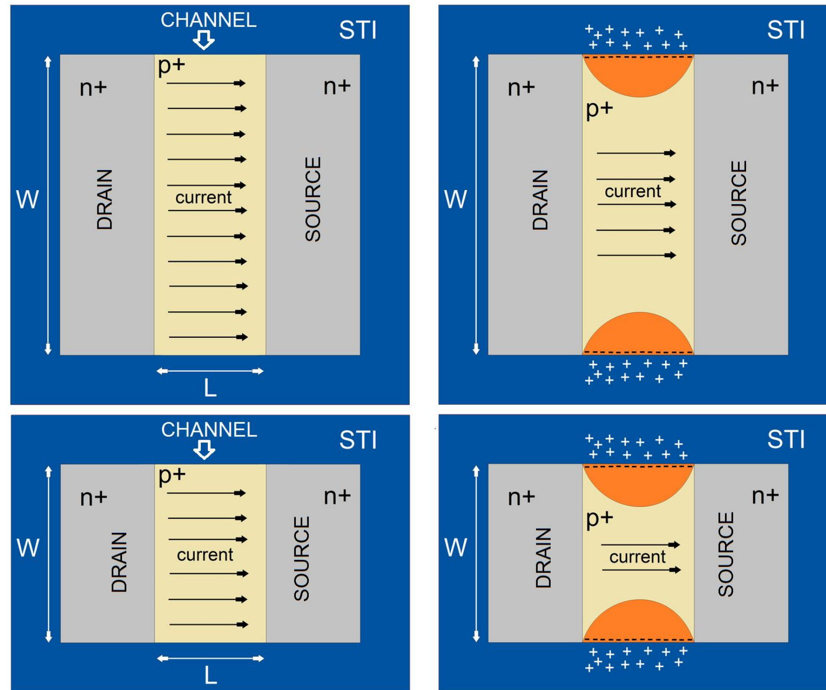


Figure 1.22: Schematic representation of the radiation induced narrow channel effects (RINCE). The electric field generated by the charge trapped in the STI depletes the lateral regions close to the STI sidewalls, reducing the effective channel width and mostly degrading the current flow of the narrow-channel transistor. (From [74])

($L = 10\ \mu$m) were irradiated through X-ray exposures. Worst-case degradation is in pMOSFETs devices, which exhibit a strong channel-width dependent degradation. The narrowest device is the most sensitive. The TID response is dominated by a collapse of the drain current in linear region caused by a large degradation of trasconductance and by a positive threshold voltage shift. The large degradation of the transconductance is typical in narrow transistors affected by RINCE [37, 39, 88, 89]. Indeed, the transconductance of a transistor is proportional to the effective channel width. Radiation-induced positive charge in STI oxides depletes the lateral Si-channel regions close to the STI sidewalls, consequently reducing the effective channel width. The reduction of the effective channel width is rappresented in Figure 1.22, which reproduces the top view of a narrow and a large pMOSFET working in inversion region (on-state). After the irradiation, the lateral regions close to the STI sidewalls are depleted by the positive charge in the STI, mostly degrading the current flow of the narrow-channel transistor [37, 74].

1.3.2 Spacer related effects (RISCE)

The TID degradation mechanism related to spacer oxide has been reported recently by few works [37, 84, 90] and the research on its degradation mechanism started to be investigated in the last few years. The recent miniaturization of devices to nanometer scale has

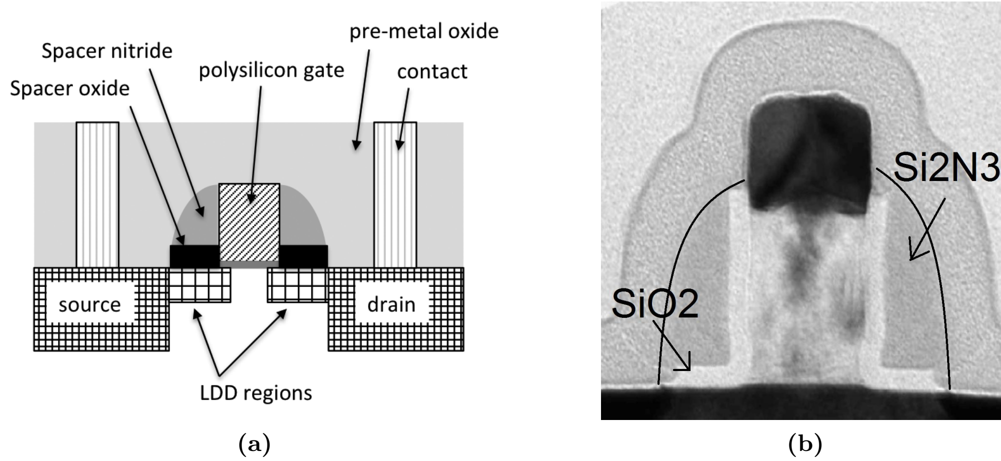


Figure 1.23: (a) Schematic rappresentation of the fabrication process of a MOSFET with spacers used for the implantation of LDDs. (From [37]). (b) Transmission electron microscopy image of a 65 nm MOSFET technology node, showing the significant volume of the spacer dielectrics. (After [90])

led to the use of the Lightly Doped Drain regions (LDDs) [91], used to decrease the impact of hot carriers, to eliminate punchthrough and to moderate threshold voltage dependence on channel length. Figure 1.23(a) shows a schematic view of a modern manufacturing process technology using LDD regions. During the fabrication process, a moderate doping implantation covering the full drain/source area is first applied to produce a shallower and more lightly doped region. Spacer are then grown around the gate polysilicon, and source/drain regions are implanted. The spacers prevent the high doping implants of the source/drain regions to reach the proximity of the channel, allowing the formation of LDD regions characterized by a lower doping than drain/source implantations. As shown in the transmission electron microscopy picture of Figure 1.23(b), spacers are usually formed by a layer of 10-20 nm-thick SiO_2 covered by a thicker Si_3N_4 layer [91, 92]. Both SiO_2 and Si_3N_4 layers are grown through low-pressure chemical vapor deposition, which typically leaves an high percent of hydrogen content in the Si_3N_4 [93].

Spacer-related phenomena has been studied mainly in the 65 nm Si MOSFET technology [37, 74]. One of the first clue of a possible impact of spacers to the TID transistor response was the discovery of a channel-length dependence in the degradation of the drain current of irradiated devices biased in the linear region [37]. Figure 1.24 shows the percentage degradation of the maximum drain current I_{on-lin} as a function of cumulated dose in nMOSFETs and pMOSFETs designed with enclosed layout, which avoids any STI-related effect by design. Devices are irradiated with X-rays up to ultra-high doses. A relevant I_{on-lin} decrease is observed during irradiation of both nMOSFETs and pMOSFETs with worst-case performance degradation for short-channel devices. The short-channel effect is mainly visible in pMOSFETs and it is almost negligible for gate lengths above 1 μm. This channel-length dependent phenomena has been named Radiation-Induced Short Channel

Effect (RISCE) [37].

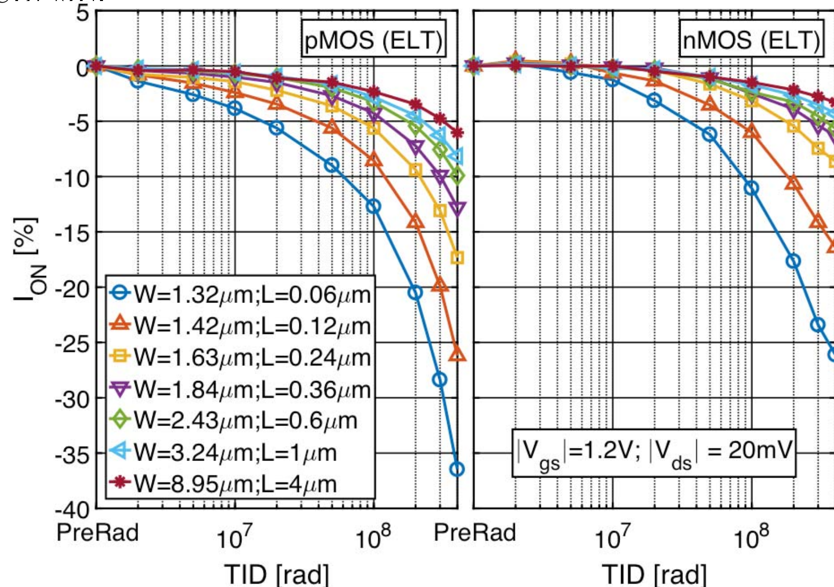


Figure 1.24: Degradation of the current I_{on-lin}, defined as the drain current at $|V_{gs}| = 1.2$ V in linear region ($|V_{ds}| = 20$ mV) for pMOSFETs and nMOSFETs fabricated as ELTs. Transistors were irradiated with X-rays in the "diode"-bias configuration up to 400 Mrad(SiO_2). (From [90])

Further research demonstrate that the channel-length dependence is particularly dominant after high temperature annealing. Figure 1.25 reports the degradation of the maximum drain current for transistors of different lengths irradiated up to 400 Mrad(SiO_2) and then annealed at 100 °C for 100 h. The width of these transistors is 20 μm, large enough to avoid any effect related to charge buildup in the STI. The longest transistor with $L = 10$ μm has a very small degradation, less than 5% during irradiation and high-temperature annealing, proving the extreme robustness of the thin gate oxide. Worst-case TID degradation is found in the shortest pMOSFET, which shows a collapse of the maximum drain current during the high temperature annealing, almost 60% after the 100 h at 100 °C. Figure 1.25 highlights also that the RISCE dominates at ultra-high doses, as the degradation is almost negligible (< 5%) at doses lower than 10 Mrad (SiO2).

Figure 1.26 highlights the causes of such a large degradation in the short channel device [74]. The I_d-V_{gs} in linear region ($|V_{ds}| = 20$ mV) is measured before irradiation, and after exposure and annealing of 100 h at 100 °C. The measurements were carried out in two different modes: nominal (solid lines) and reversed (dashed lines). In nominal mode, the I_d-V_{gs} is measured with V_{ds} = -20 mV, while, in reversed mode, the I_d-V_{gs} is measured with V_{ds} = 20 mV, which means that the drain terminal is switched with the source one. Here, the nominal and reversed curves overlap, indicating a symmetric response of the transistor. After irradiation, the decrease of the maximum drain current I_{on-lin} is caused by the increase of the series resistance of the transistor with slight threshold voltage shift and negligible variation of the subthreshold stretcout. After annealing, the decrease of the I_{on-lin} current is due to an extremely large shift of the threshold voltage together with an

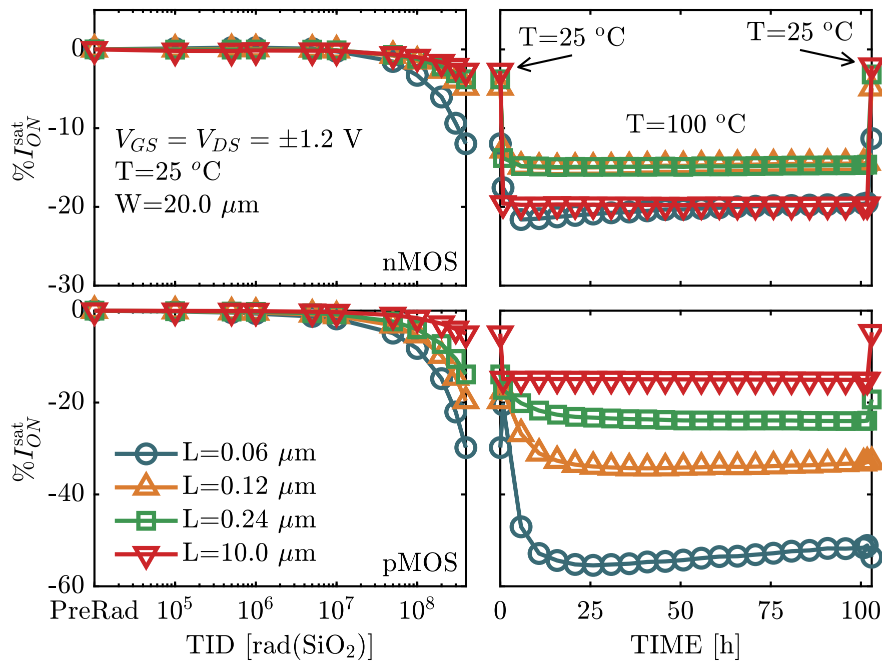


Figure 1.25: Comparison of the TID degradation of transistors with different channel length and same width $W = 20$ μm. The degradation of the drain current at $|V_{gs}| = 1.2$ V in linear region ($|V_{ds}| = 20$ mV) is plotted for pMOSFETs (top row) and nMOSFETs (bottom row) fabricated as ELTs. Transistors were irradiated with X-rays in the "diode"-bias configuration up to 400 Mrad(SiO_2) and then annealed for 100 h at 100 °C. All measurements during the annealing test were carried out at 100 °C, except the first and the last points, which were measured at room temperature. (From [74])

increase of the subthreshold stretchout. [37, 74]

The increase of the series resistance R_{sd} during irradiation is visible in Figure 1.27. The plot reports the R_{sd} normalized by channel width as a function of cumulated dose in nMOSFETs and pMOSFETs irradiated at two different temperatures. Indeed, consistently with the large degradation of the drain current of pMOSFETs in linear region, the worst-case increase of R_{sd} is visible in pMOSFETs. The measurements demonstrate that the increase of R_{sd} is insensitive to the channel length. However, the effects of R_{sd} are more visible in short-channel transistors, which are characterized by larger voltage drops due to the their higher drain current compared to long-channel ones. The increase of R_{sd} in pMOSFETs is caused by the buildup of positive charge in the spacers during irradiation. High density of positive charge in spacer dielectrics can reduce the number of majority carriers in the underlaying lightly p-doped regions of the LDDs. This effect does not affect nMOSFETs, as positive charge in the spacer contributes to increase the number of carriers in the n-doped LDDs [37, 74].

Annealing tests performed at high temperature display an enhanced positive shift of the threshold voltage in short-channel pMOSFETs. Figure 1.28 shows the I_d-V_{gs} in the saturation region ($|V_{ds}|$ = 1.2 V) of the shortest pMOSFET before irradiation, after exposure and annealing of 100 h at 100 °C. The short transistor exhibits a large positive degradation of the threshold voltage. Moreover, the DC response is strongly asymmetric with larger V_{th} shift in nominal mode than in reversed mode. This asymmetry is noticeable only in the saturation region, whereas, in the linear region, the nominal and reversed responses overlap (see Figure 1.26). Both radiation-induced threshold voltage shift and

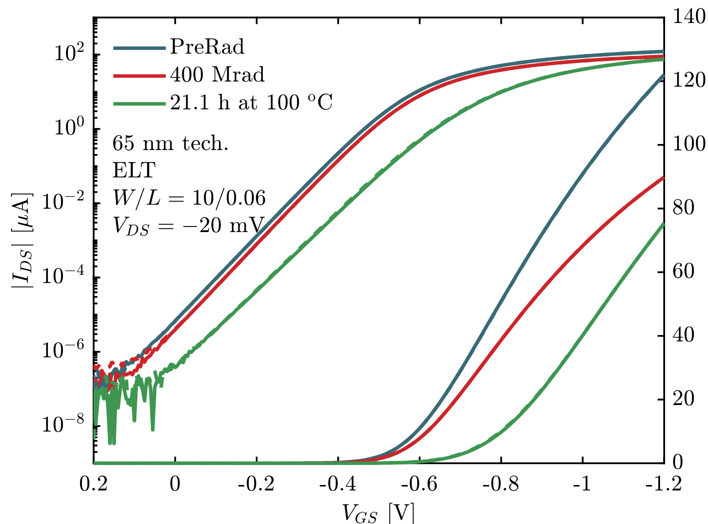


Figure 1.26: The $|I_d| - |V_{gs}|$ in linear region $|V_{ds}|$ = 20 mV for a short-channel ELT pMOSFET with L = 60 nm. The transistor was irradiated with X-rays in the "diode"-bias configuration up to 400 Mrad(SiO_2) and then annealed for 100 h at 100 °C. Measurements were carried out in nominal mode (NOM, solid lines) with V_{ds} = -20 mV and in reversed mode (REV, dashed lines) with V_{ds} = 20 mV, where the drain terminal is switched with the source one. (From [74])

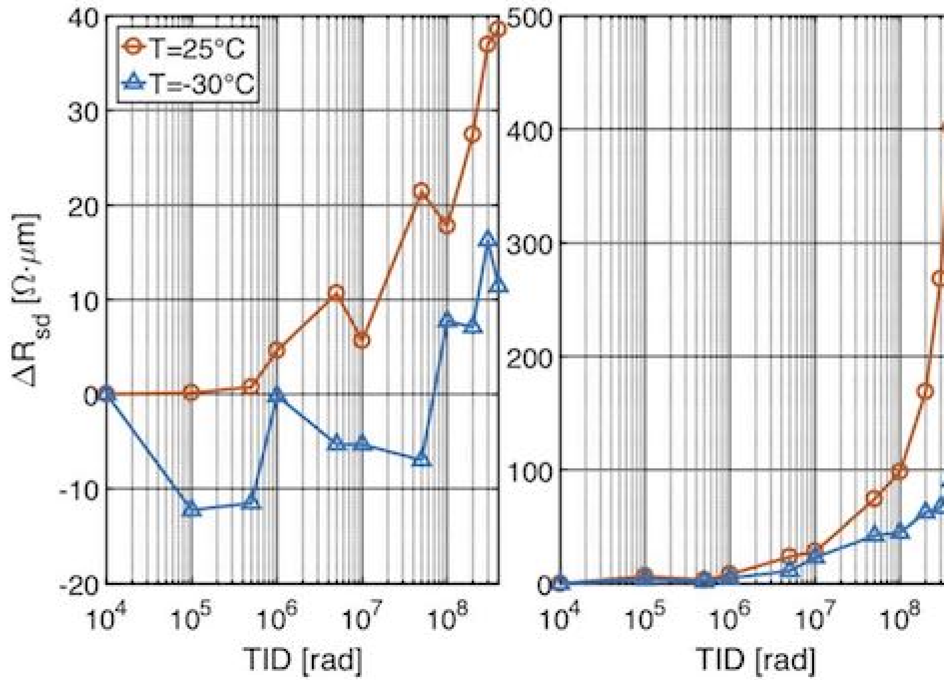


Figure 1.27: The series resistance R_{sd} normalized by the channel width as a function of cumulated dose in nMOSFETs and pMOSFETs irradiated at two different temperatures. Transistors were irradiated with X-rays up to 400 Mrad(SiO_2). Channel width of all transistors was 20 μm, sufficient large to avoid RINCE. (From [90])

asymmetry are activated only at high temperatures and only when the shortest device is annealed in the "diode"-bias condition ($|V_{gs}| = |V_{ds}| = 1.2$ V), that means when a lateral source-to-drain field is applied during the annealing.

In summary, devices affected by RISCE are typically characterized by the following TID-induced effects:

- Increase of the series resistance during the irradiation, regardless of the applied bias and of channel length dimension.
- Large threshold voltage shifts in short channel devices, enhanced by high temperature and high electrical field in the gate oxide.
- Asymmetric I_d-V_{gs} response visible only in saturation region, when the device is irradiated and/or annealed with high drain-to-source bias ("diode"-bias condition).

Recently, in some literature studies [37, 90], the RISCE has been explained with a model, where radiation-induced charge buildups in the spacer oxide and its interface. The proposed model is represented in Figure 1.29, which explains the evolution of the RISCE mechanism through the following stages:

- (a). Ionizing radiation induces hole trapping and release of H^+ in the spacers. Holes

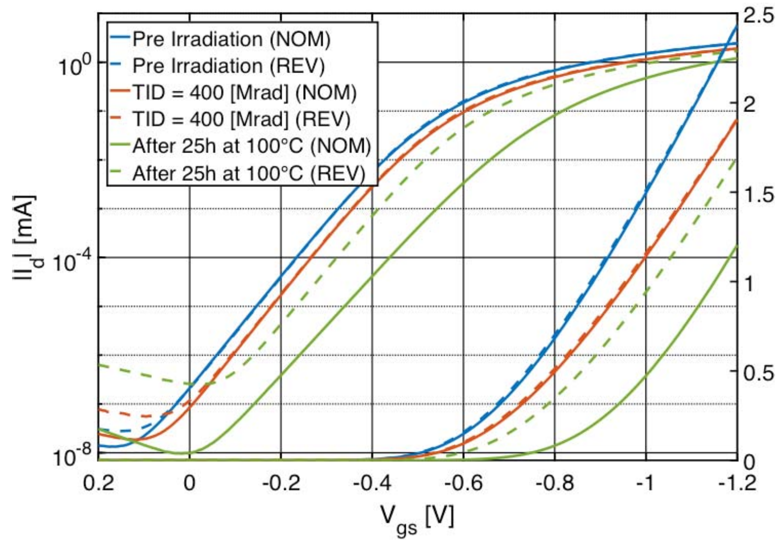
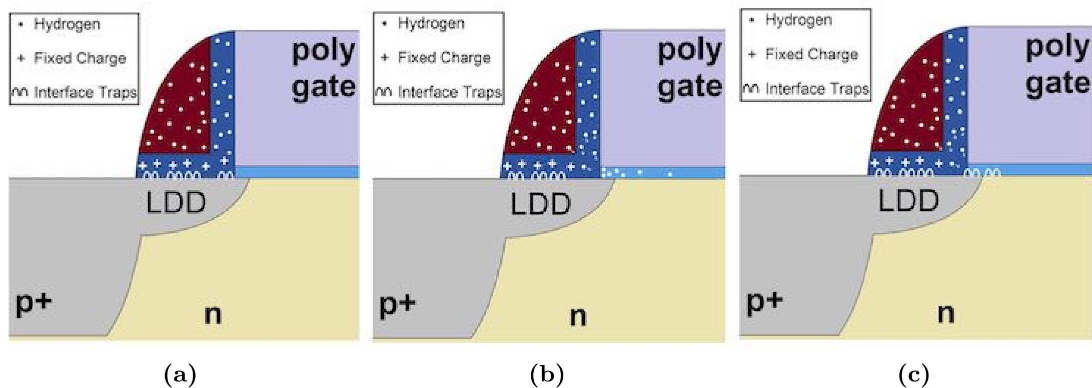


Figure 1.28: The $|I_d| - |V_{gs}|$ in saturation region $|V_{ds}| = 1.2$ V for a short-channel ELT pMOSFET with $L = 60$ nm. Transistors were irradiated with X-rays in the "diode"-bias configuration up to 400 Mrad(SiO_2) and then annealed for 25 h at 100 °C. Measurements were carried out in nominal mode (NOM, solid lines) with V_{ds} = -20 mV and in reversed mode (REV, dashed lines) with V_{ds} = 20 mV, where the drain terminal is switched with the source one. A strong asymmetry between NOM and REV curves is visible. (From [90])

and H^+ can affect the the density of majority carriers in the low-doped LDDs, consequently increasing the series resistance of the p-channel MOSFETs.

- (b). Under high temperature, the hole and H^+ transport is enhanced. At high gate bias, hole and H^+ are drifted from the spacers to the gate oxide.



(a) (b) (c)

Figure 1.29: Schematic representation of the evolution of the spacer-related mechanism. (a) Radiation generates trapped positive charge in the spacers, increasing the series resistance in the LDD regions. (b) H^+ are released in the spacers and are drifted in the thin gate oxide, depending on temperature and electric field. (c) H^+ reach the SiO_2/Si interface at the gate corner generating localized interface traps. (From [74])

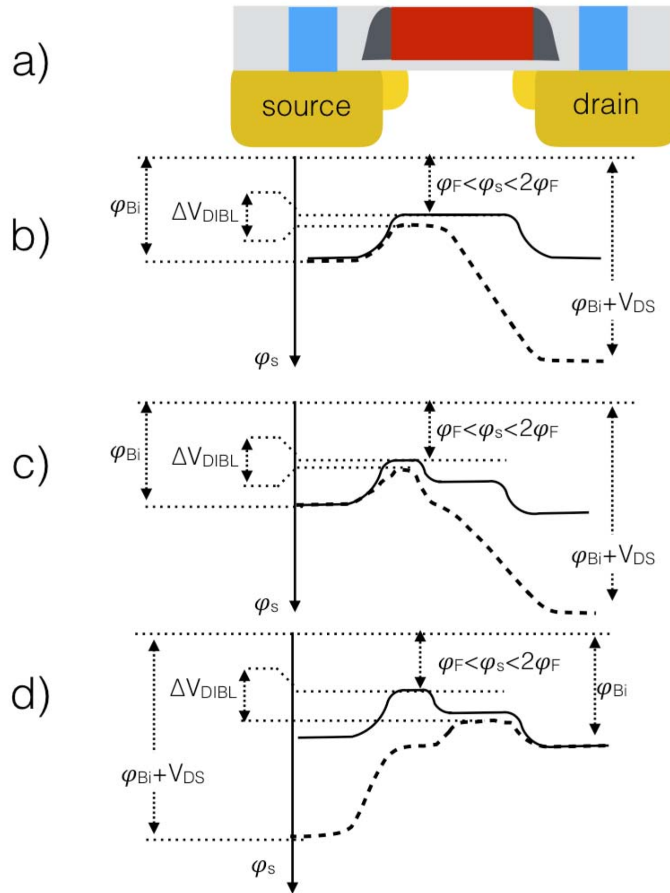


Figure 1.30: Schematic representation of the potential barrier in the NOM and REV bias modes in a MOSFET, before and after high temperature annealing. (From [90])

- (c). If $|V_{ds}| \gg 0$ bias is applied, H^+ are drifted from one spacer into the gate oxide. H^+ de-passivate Si-H bonds along the SiO_2/Si interface, creating a large density of interface traps at the source side (in pMOSFETs) and at the drain side (in nMOSFETs), which cause the asymmetric large threshold voltage shift.

This model has been supported by DC characteristics and low frequency $1/f$ noise measurements presented in [90] and it will be fully validated by the charge pumping measurements and TCAD Sentaurus simulations, reported in the third chapter and in [94].

The strong asymmetric DC response measured in saturation region of pMOSFETs can be understood through the drain induced barrier lowering (DIBL) with a peak density of interface traps localized close to source region [90]. Figure 1.30 schematically represents the surface potential ϕ_S of a pMOSFET biased in inversion. (b) shows to the surface potential after irradiation, while (c) and (d) refer to surface potential after annealing measured in nominal (c) and reverse (d) configurations. The V_{DIBL}, measured in mV/V, is defined as the gate voltage shift V_{gs} induced by a large drain voltage change V_{ds} for the same drain current in weak inversion. Solid lines indicate the ϕ_S in the linear region ($V_{ds} =$

-20 mV), while dashed lines indicate the ϕ_S in the saturation region (V_{ds} = -1.2 V). Before and after irradiation, ϕ_S is uniform along the channel, and the nominal V_{DIBL} is equal to reversed V_{DIBL}. After the annealing at high source-to-drain bias, the H^+ are drifted in the gate oxide from the source spacer and interface traps are generated with a peak density close to the source region. These traps are populated by positive charge and a larger gate voltage is now necessary to invert the channel region close to the source, although the channel region close to the drain is already in strong inversion. In this condition, the $|V_{th}|$ of the transistor is larger than before annealing. As shown in Figure 1.30(c), high bias at the drain terminal marginally influences the maximum value of ϕ_S with a consequent small V_{DIBL}. However, if the same voltage is applied to the source (d), it lowers the surface potential at the source side and the maximum ϕ_S is determined by the barrier close to the drain with a consequent increase of the V_{DIBL}. From the data of Figure 1.30, it results that the effect of the asymmetry appears only in the saturation region, while, in the linear region, the transistor remains symmetric.

The spacers-related effects on the radiation response of MOS transistors have only been studied recently. Further insights about the spacer mechanism will be given in the third chapter through the discussion of new experimental results, which were obtained during this thesis work and have been recently published in [90, 94].

Chapter 2

150 nm Si CMOS technology

In space applications, integrated circuits (ICs) must overcome environmental hazards and at the same time keep their performance requirements [1]. Even if commercial devices are available in nodes lower than 10 nm, the electronics for space still use older technologies, like the 150 nm CMOS technology node analyzed in this chapter, whose production process is more established than novel technologies [28]. In this chapter, the TID response of a 150 nm Si CMOS technology produced by LFoundy, Italy, within a collaboration with Sitael, Italy, is studied and analyzed through a qualification campaign up to 125 krad(SiO_2).

As explained in the previous chapter, ionizing radiations affect the reliability of ICs by generating trapped charges in the insulator materials, causing parametric shifts of transistor responses [12, 13, 34]. Trapped charges in the gate oxides of MOSFETs induce threshold voltage shifts, transconductance degradations, and drive current variations [34]. In the last years, the shrink of the gate oxide thickness of MOSFETs has improved the TID sensitivity [12, 46, 95]. Indeed, the buildup of positive trapped charge scales with the dielectric thickness [46, 78] also thanks to the increased likelihood of charge neutralization through tunneling of electrons injected from the adjacent semiconductor materials [78]. However, the furthermore scaling down of the devices has brought new degradation mechanisms related to other thick oxides.

Several recent works [37, 39] about TID effects of modern devices designed in the 180 nm node or lower report stronger radiation-induced degradation in narrow-channel transistors. As explained in Section 1.3.1, this channel-width dependent effect is called RINCE [37]. RINCE is related to charge trapping in the STI oxide and its oxide/semiconductor interface [38], which induces parametric shifts in the I-V curves of narrow n- and p-channel MOSFETs [37, 96, 97]. Moreover, positive charge buildup in the STI oxide can increase the leakage currents of n-channel MOSFETs regardless of the channel width, due to the activation of the lateral parasitic transistors [37, 98]. Finally, recent studies [97, 99] demonstrate that the TID response of 90 nm and 28 nm CMOS technology starts to be influenced by the halo implantations. The influence of the halo implantations on the TID response will be extensively analyzed in the 28 nm Si CMOS technology in the fourth chapter, but their

influence is here introduced to explain some minor dependance of the TID to the channel length. Indeed, halo implantations can increase the overall bulk doping of short-channel transistors, which results more TID tolerant than long-channel transistors [97].

With the experimental test presented in this chapter, I bring new insights about the TID radiation-induced mechanism affecting the 150 nm MOSFET technology. nMOSFETs and pMOSFETs are characterized by DC static measurements, evidencing different TID sensitivity depending on channel dimension and on the type of transistors (core or I/O). Core transistors exhibit higher TID tolerance than I/O transistors, probably due to the scaled dimensions of the gate oxide thickness combined with the higher doping profiles and different fabrication processes adopted in the core transistors. The degradation is channel-width dependent, confirming the strong influence of this technology to the trapped charges in the STI oxides. Moreover, experimental measurements evidence a new channel-length dependence of the TID degradation, which is related to the use of halo implantations.

2.1 Devices and experiments

2.1.1 Device description

Devices under test are fabricated in bulk 150 nm CMOS technology based on SiO_2 gate dielectrics, fabricated by LFoundry, Avezzano, Italy. nMOSFETs and pMOSFETs are provided on Si wafers in a customized array structure, containing several types and several geometries of transistors with no ESD protections. As shown in Table 2.1, four types of transistors are tested: I/O 5V, I/O 3.3V, core HS 1.8V (high speed), and core LL 1.8V (low leakage). Each array structure contains 12 different geometries of channel width (0.32 μm $<$ W $<$ 10 μm) and channel length (0.15 μm $<$ L $<$ 10 μm). In this work, I focus

MOSFET types	#1 Narrow/Short W/L [µm]	#2 Narrow/Long W/L [µm]	#3 Large/Long W/L [µm]
I/O 5V nMOSFET	0.8 / 0.8	0.8 / 10	10 / 10
I/O 5V pMOSFET	0.8 / 0.6	0.8 / 10	10 / 10
I/O 3.3V nMOSFET	0.8 / 0.35	0.8 / 10	10 / 10
I/O 3.3V pMOSFET	0.8 / 0.35	0.8 / 10	10 / 10
core HS 1.8V nMOSFET	0.32 / 0.15	0.32 / 10	10 / 10
core HS 1.8V pMOSFET	0.32 / 0.15	0.32 / 10	10 / 10
core LL 1.8V nMOSFET	0.32 / 0.15	0.32 / 10	10 / 10
core LL 1.8V pMOSFET	0.32 / 0.15	0.32 / 10	10 / 10

Table 2.1: Types and dimensions of the MOSFETs under test divided in three groups: narrow and short, narrow and long, and large and long.

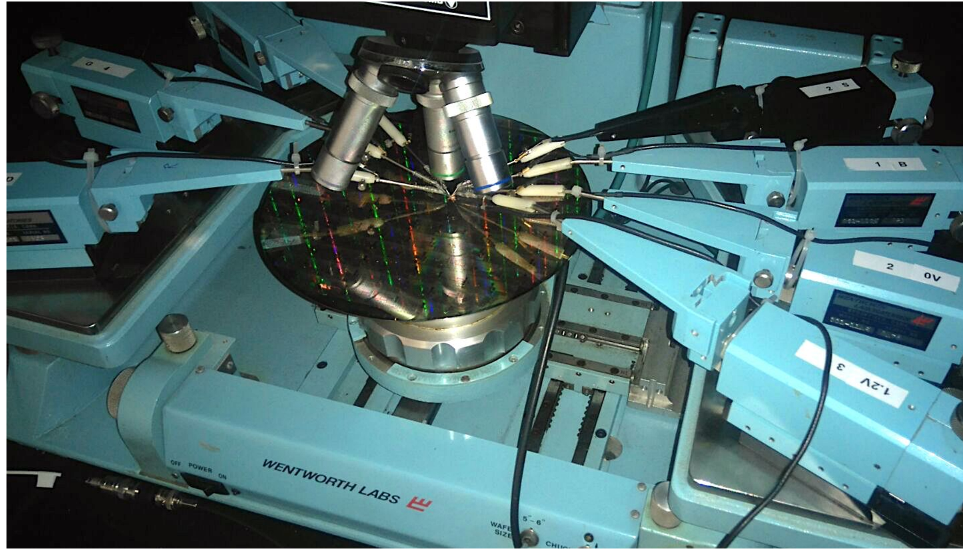


Figure 2.1: Photo of the manual probe station used for the irradiation test.

the analysis on three significative channel dimensions (see Table 2.1): narrow and short, narrow and long, and large and long. Transistors of the same type share gate, source and bulk terminals, while separated drain terminals are dedicated to each transistors. Transistors are measured on wafer through a manual probe station (see Figure 2.1).

2.1.2 Irradiation conditions and measurements details

I irradiated the devices up to 125 krad(SiO_2) at room temperature at the University of Padova using an X-ray irradiator composed by a tungsten tube with peak energy deposition at 10 keV [100]. The X-ray spectra emitted from the tube was filtered by a 150 μm Al foil in order to remove the low-energy component (< 8 keV). The dose rate wass set to 36 krad(SiO_2)/hour within the ESCC 22900 standard rate [101], for a total exposure time of about 4 hours.

The devices under test were biased and measured with the help of a wafer prober inside the irradiation cabinet. After the exposure, I performed two different annealing tests at room temperature and high temperatures. Due to the constraints of wafer-level measurements, annealing time was shortened with respect to the ESCC 22900 standard durations used with packaged devices [101]. In particular, the devices were first annealed at room temperature for 24 hours and then at 100 °C for other 24 hours through a thermal chuck. Accordingly to previous studies [38, 39, 98, 102] in Si-based MOSFETs, worst-case DC biases were applied during irradiation and post-exposure annealing: "on"-bias configuration for nMOSFETs ($|V_{gs}| = V_{dd}$+10% and $|V_{ds}| = 0$ V) and "off"-bias configuration for pMOSFETs ($|V_{gs}| = 0$ V and $|V_{ds}| = 0$ V). Devices of two different wafer lots were measured, showing lot-to-lot variation less than 8%. At least two different devices of each type were evaluated for all experimental conditions with typical results shown below. The

DC responses of the transistors were evaluated by measuring the main DC parameters with a semiconductor parameter analyzer (HP 4156) before the exposure, at several irradiation steps and after the annealing tests.

2.2 Experimental results

2.2.1 TID effects on nMOSFETs and pMOSFETs

Figure 2.2 reports the I_d-V_{gs} in logarithmic and in linear scales for I/O 5V MOSFETs with narrow and long channel (W = 0.8 μm and L = 10 μm). Transistors are measured in linear region ($|V_{ds}|$ = 0.1 V) at several irradiation steps up to 125 krad(SiO_2). The largest degradation is found in the n-channel MOSFET, which exhibits increased leakage off current I_{off} and negative shift of threshold voltage V_{th}. At 125 krad(SiO_2), the transistor response is dominated by an extremely high I_{off}, comparable to the drain current in linear region, while the maximum drain current at $|V_{gs}|$ = 5 V increases of 28%, due to the negative shift of V_{th}. After the exposure, transistors are annealed for 24 hours at room temperature and at 100 °C. Room temperature annealing causes negligible effects, while high temperature annealing induces large recovery of I_{off} and an almost complete recovery of V_{th}. On the contrary, the p-channel MOSFET has modest degradation compared to the n-channel one. The V_{th} of pMOSFET slightly increases with the cumulated dose and the transconductance g_m slightly decreases, causing an overall variation of the maximum drain current of -3% at 125 krad(SiO_2). During room temperature annealing, the transistor response is stable, while the high temperature annealing induces an additional slight degradation of both V_{th} and g_m.

Figure 2.3 reports the I_d-V_{gs} in logarithmic and linear scales for core HS MOSFETs with narrow and long channel (W = 0.32 μm and L = 10 μm). Transistors are measured at room temperature in the linear region ($|V_{ds}|$ = 0.1 V) at several irradiation steps up to 125 krad(SiO_2) and after 24 hours of annealing at room temperature. The high sensitivity to ESD discharges of core transistors combined with the numerous operations needed to carry out the high temperature annealing tests have limited the annealing measurements just to room temperature, and not to high temperature. nMOSFET shows negative V_{th} shift and g_m degradation, which cause an increase of the maximum drain current of 7% at 125 krad(SiO_2). Modest variation of leakage current is detected in the core nMOSFETs with an increase of I_{off} of less than one order of magnitude. During room temperature annealing, the nMOSFET response is almost unchanged. Core pMOSFET results the most tolerant device with $<$ 1% of variation of the maximum drain current after 125 krad(SiO_2).

Figure 2.4 compares the TID sensitivity of four different types of MOSFETs: I/O 5V, I/O 3.3V, core HS 1.8V and core LL 1.8V. The variation of the threshold voltage $\Delta|V_{th}|$ is plotted as a function of the dose for narrow and long channel transistors (W = 0.32 μm and L = 10 μm). The worst-case response is found in I/O 5V transistors, while core 1.8 V transistors exhibit the best TID tolerance. The I/O 5V transistor shows

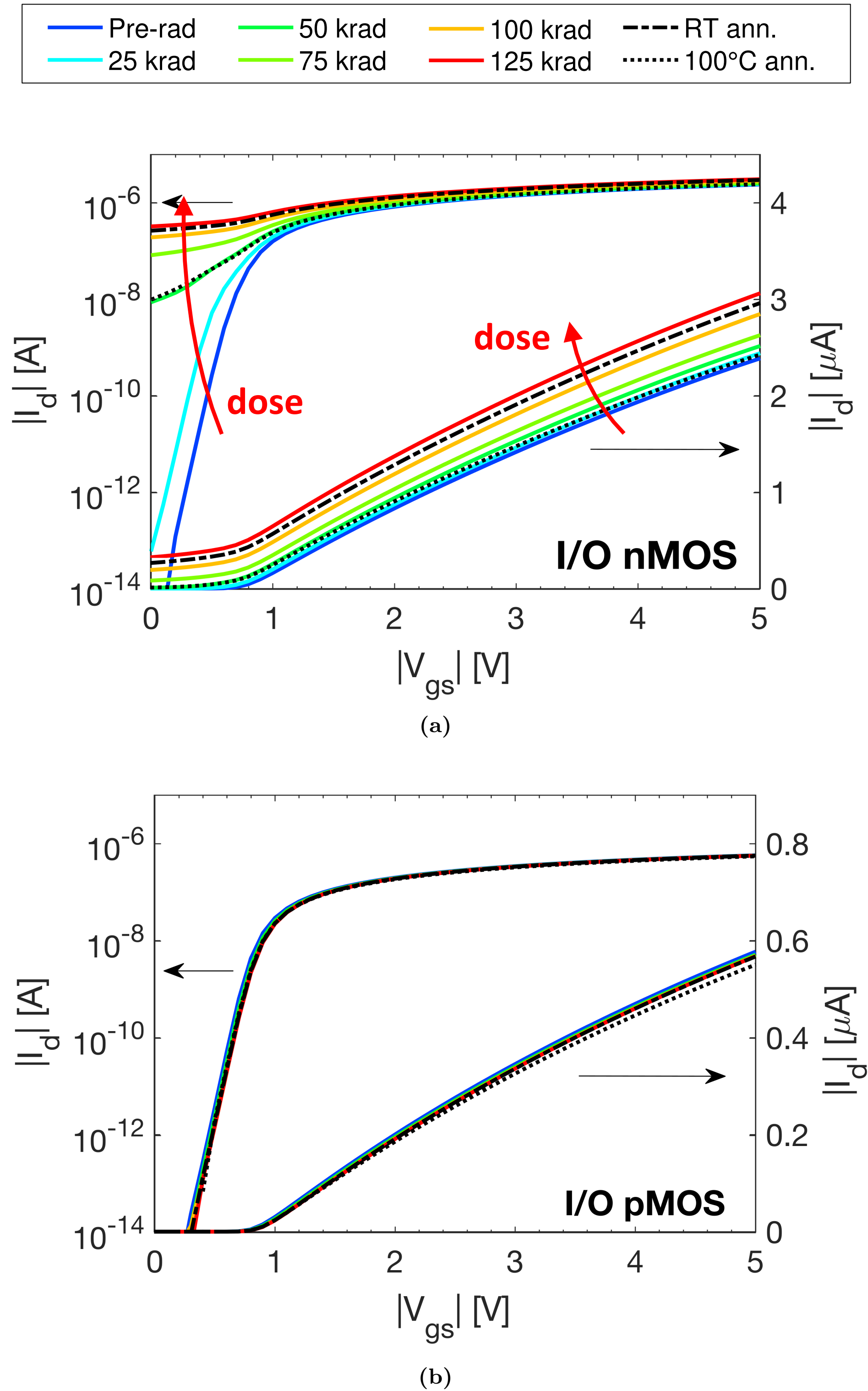
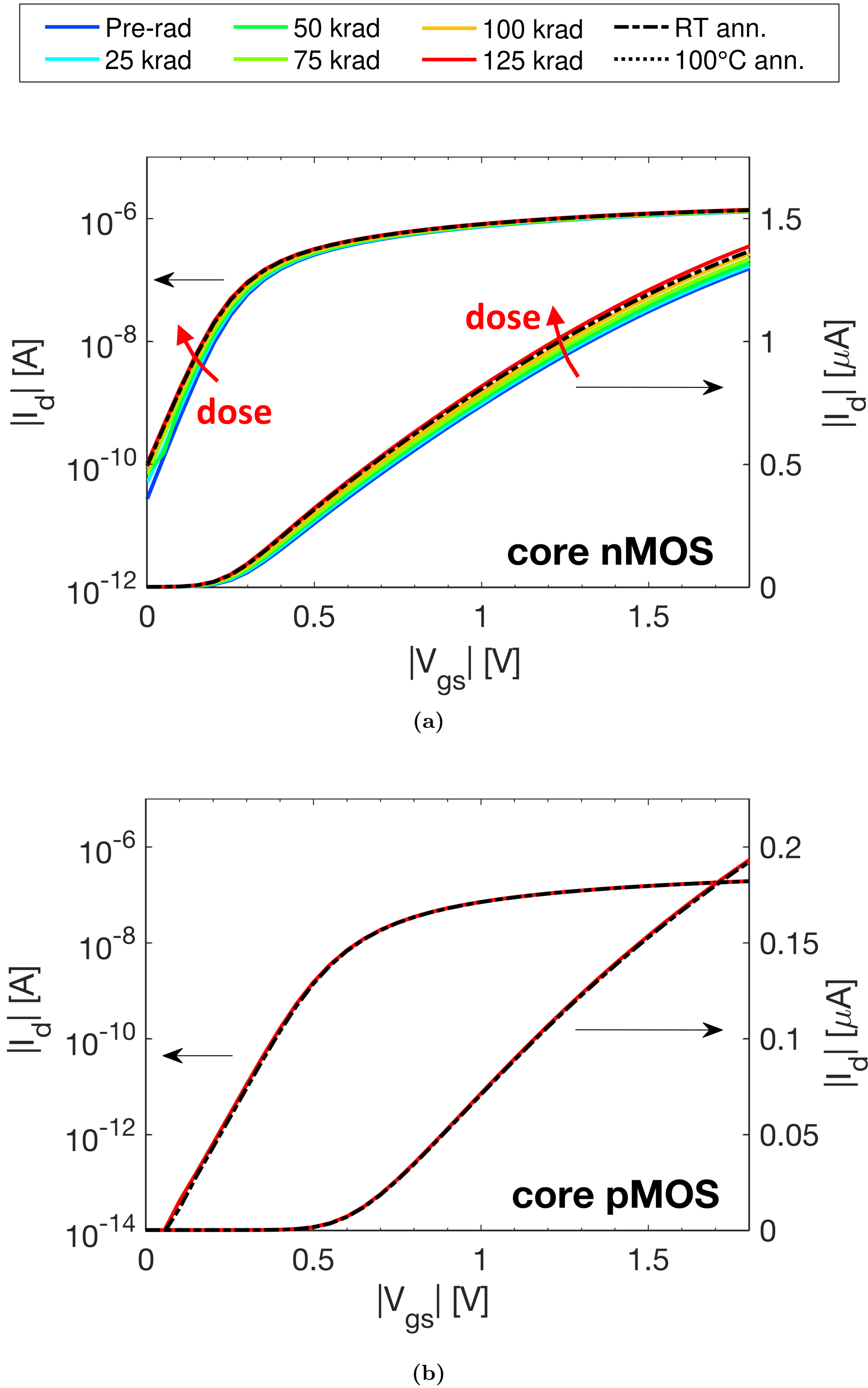


Figure 2.2: $I_d - V_{gs}$ responses at room temperature of long and narrow channel of I/O 5V MOSFETs biased in the linear regime ($|V_{ds}| = 0.1$ V) with $W = 0.8$ μm and $L = 10$ μm. Transistors were irradiated up to 125 krad(SiO_2), annealed at room temperature for 24 hours, and finally annealed at 100 °C for 24 hours. (a) nMOSFET and (b) pMOSFET.



(a)

(b)

Figure 2.3: $I_d - V_{gs}$ responses at room temperature of long and narrow channel of core HS 1.8V MOSFETs biased in the linear regime ($|V_{ds}| = 0.1$ V) with $W = 0.8$ μm and $L = 10$ μm. Transistors were irradiated up to 125 krad(SiO_2), annealed at room temperature for 24 hours, and finally annealed at 100 °C for 24 hours. (a) nMOSFET and (b) pMOSFET.

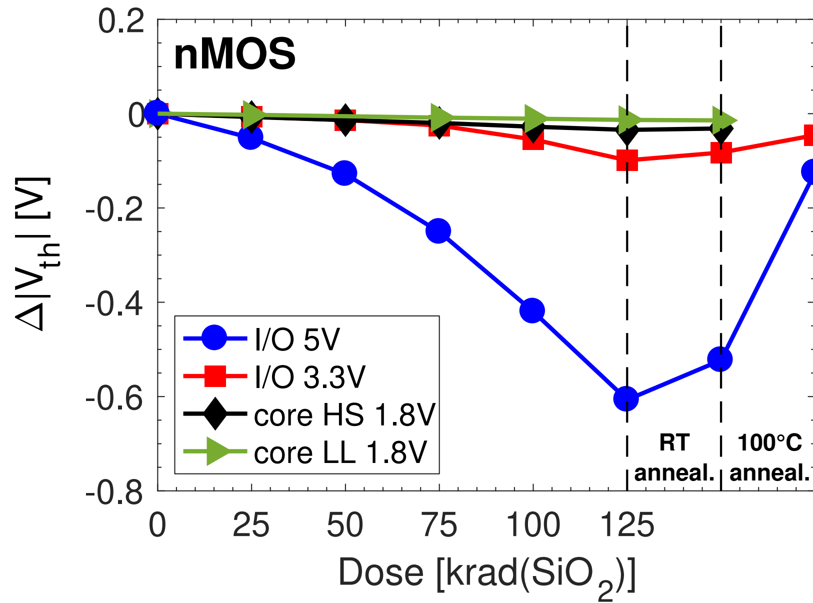
a $\Delta|V_{th}|$ shift of -0.6 V vs. -0.1 V of I/O 3.3V and <-0.05 V of core transistors. Room temperature annealing causes only marginal parametric shifts, while high temperature annealing induces large recovery of V_{th} for I/O 5V and I/O 3.3V transistors.

Figure 2.5 shows the leakage current I_{off} as function of dose in different types of nMOSFETs, irradiated up to 125 krad(SiO_2). The I_{off} current is defined as the drain current when the device is biased at $|V_{gs}| = 0$ V. Before the exposure, the leakage currents of all transistor are around 1 x10^{-14} A, with exception of core HS devices, which show a higher $|I_{off}|$ of 1 x10^{-11} A. The different pre-rad leakage currents between HS and LL core transistors can be due to different doping density of the bulk and of halo implantations. Indeed, LL transistors require increased bulk/halo doping to improve the leakage current at the expense of the channel control and speed, which on the contrary are essential parameters in HS devices. The high bulk/halo doping of LL devices is also in agreement with the higher V_{th} of LL core devices if compared to the HS devices. Indeed, pre-rad $|V_{th}|$ is 0.6 V for narrow and long LL nMOSFETs and 0.35 V for the same dimension HS transistors.

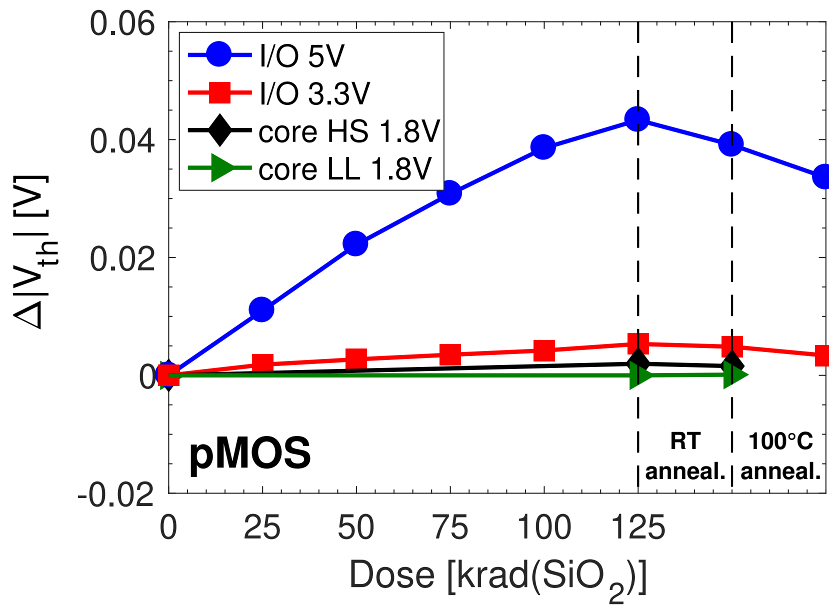
As shown in Figure 2.5, when transistors are exposed to ionizing radiation, I/O transistors exhibit the largest increase of the I_{off} with worst-case in the 5V nMOSFETs with I_off increasing from 1 x10^{-14} A to 3 x10^{-7} A. On the contrary, LL and HS core nMOFETs show modest increase of the leakage current with an increment of less than one order of magnitude after 125 krad(SiO_2). Room temperature annealing has minor effects on the leakage current, while high temperature annealing in-duces a recovery of I_{off} of about two orders of magnitude in I/O transistors.

2.2.2 TID response of I/O transistors

Figure 2.6 highlights the influence of the channel dimensions on the TID sensitivity of I/O nMOSFETs. The $\Delta|I_{on-lin}|$, $\Delta|V_{th}|$ ad $\Delta|g_m|$ are plotted as function of dose up to 125 krad(SiO_2) for three different channel sizes of transistors. The worst-case response is found in narrow and long channel transistors, which exhibit an increase of the maximum drain current of 30% vs. 10% and 2% of narrow and short transistors and large and long transistors, respectively. The small degradation of the large devices indicates modest charge trapping in the gate oxide and along its interface with the Si bulk [12, 13, 34]. In narrow devices, the large increase of the $|I_{on-lin}|$ is caused by negative V_{th} shift and increased g_m. The channel-width dependence combined with the large increase of the I_{off} current indicate charge buildup in the STI oxides [37, 39]. Indeed, when the device is in off condition ($V_{gs} < V_{th}$), positive charge in the STI inverts the lateral regions of the channel close to the STI sidewalls, causing an increase of the leakage current [37, 98]. When the channel is in inversion ($V_{gs} > V_{th}$), the positive charges in the STI improve the conductivity of the lateral regions, increasing the gm and the V_{th} (RINCE) [37, 38]. Room temperature induces a slight recover of the parametric shift, due to recombination of trapped charges in the STI oxides. The largest recovery is visible during the high temperature annealing with



(a)



(b)

Figure 2.4: Radiation-induced threshold voltage shift at room temperature of different types of MOSFETs in the linear regime ($|V_{ds}| = 0.1$ V) irradiated up to 125 krad(SiO_2). (a) nMOSFETs and (b) pMOSFETs with narrow and long channel ($W/L = 0.8/10$ μm for I/O transistors, and $W/L = 0.32/10$ μm for core transistors).

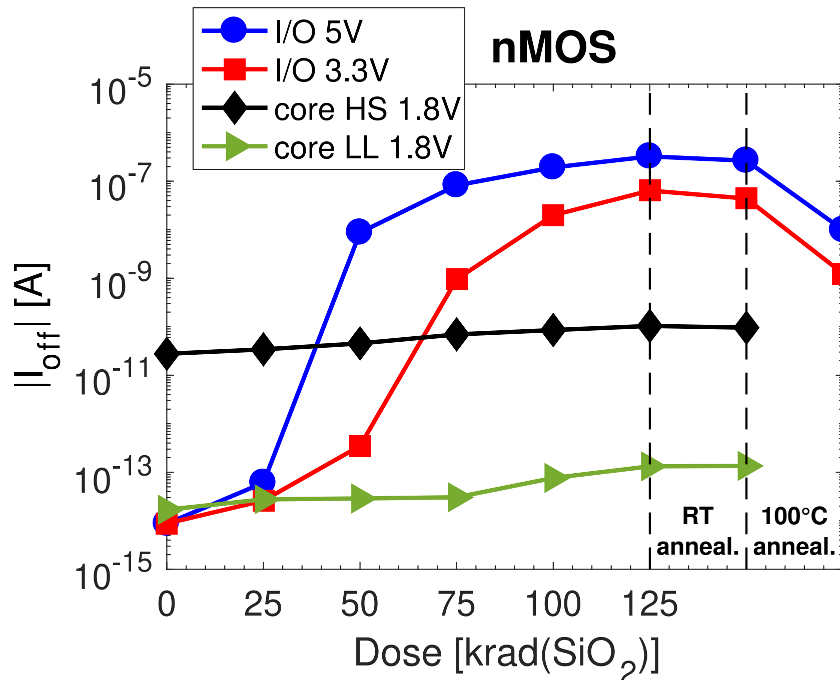
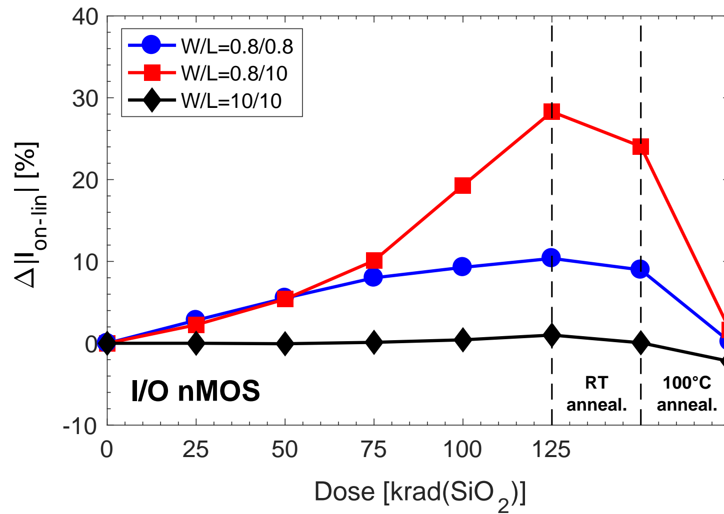


Figure 2.5: Radiation-induced leakage current at room temperature of different types of MOSFETs irradiated up to 125 krad(SiO_2). The I_off is defined as the drain current at $|V_{gs}| = 0$ V at $|V_{ds}| = 0.1$ V. (a) nMOSFETs and (b) pMOSFETs with narrow and long channel, $W/L = 0.8/10$ μm for I/O transistors, and $W/L = 0.32/10$ μm for core transistors.

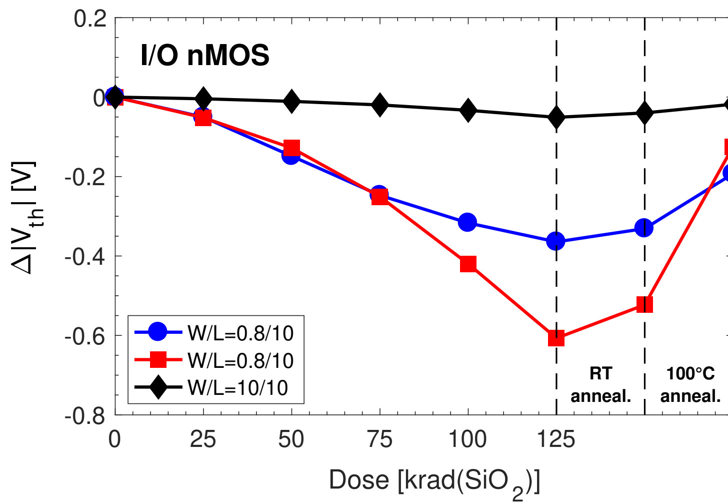
recovery of gm and V_{th} in all transistors. The largest transistors exhibit slight positive $\Delta|V_{th}|$, indicating generation of interface traps at the SiO_2/Si channel interface along the gate oxide.

Interestingly, short channel nMOSFETs exhibit higher TID tolerance than long channel ones with improved V_{th} and g_m. This channel-length dependence is probably related to the halo implantations, as similarly studied in 28 nm pMOSFETs [97]. In short channel devices, the halo implantations increase the overall bulk doping. Higher bulk doping requires larger amount of charge to alter the carrier distribution [97, 99], consequently mitigating the radiation-induced effects in short channel transistors.

Figure 2.7 reports the influence of the channel dimensions on the TID sensitivity of I/O pMOSFETs. Similarly to I/O nMOSFETs in Figure 2.6, the $\Delta|I_{on-lin}|$, $\Delta|V_{th}|$ ad $\Delta|g_m|$ are plotted as function of dose up to 125 krad(SiO_2) for three different channel sizes. In I/O pMOSFETs, the radiation-induced degradation in pMOSFETs is smaller than in nMOSFETs, but the TID effects are still channel width dependent. Narrow pMOSFETs exhibit the largest decreased $|g_m|$ and increased $|V_{th}|$, indicating charge buildup in the STI oxides. Large transistors show small degradation of $|V_{th}|$ and $|g_m|$, indicating negligible buildup of defects in the gate oxide and along the SiO_2/Si gate interface. The negligible effects of interface traps is also visible in Figure 2.8, which reports the subthreshold swing



(a)



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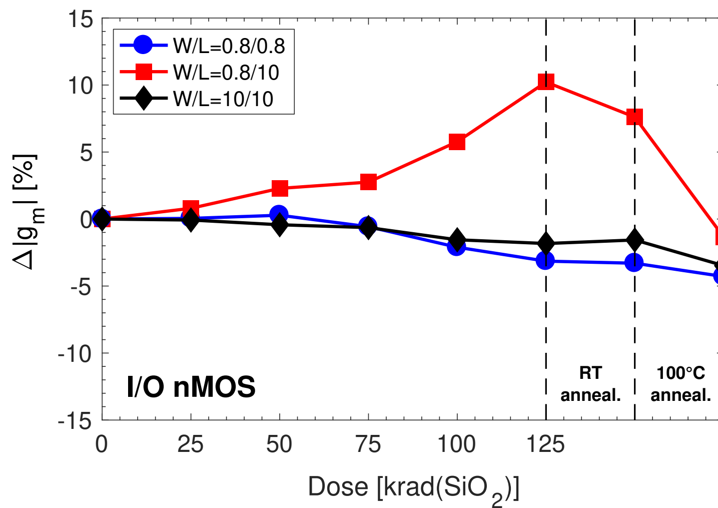


(c)

Figure 2.6: Channel dimension dependence of the I/O 5V nMOSFETs. Transistors were irradiated up to 125 krad(SiO_2), annealed at room temperature for 24 hours, and then annealed at 100 °C for 24 hours. All measurements are carried out at room temperature in linear regime ($|V_{ds}| = 0.1$ V). (a) Degradation of the maximum drain current $\Delta|I_{on-lin}|$, (b) threshold voltage shift $\Delta|V_{th}|$, and (c) transconductance degradation $\Delta|g_m|$.

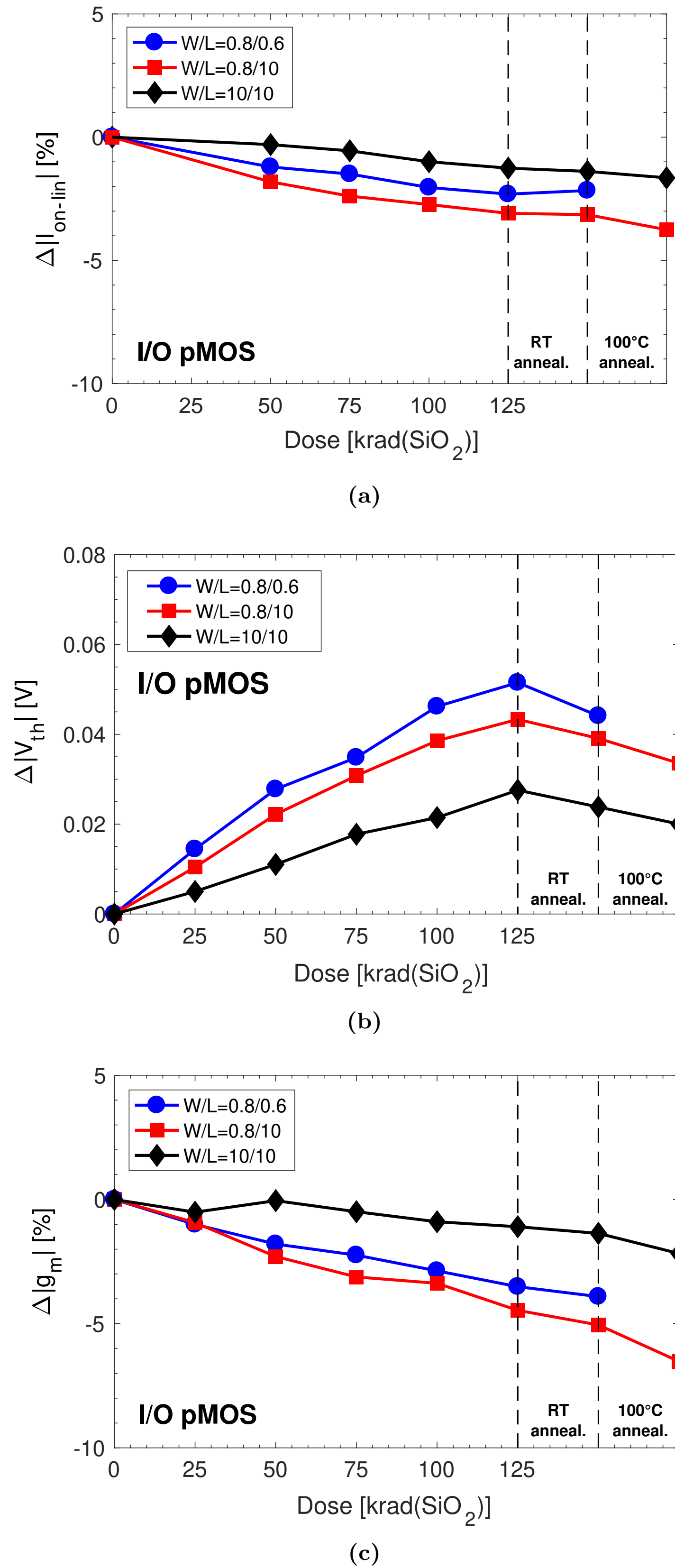


Figure 2.7: Channel dimension dependence of the I/O 5V pMOSFETs. Transistors were irradiated up to 125 krad(SiO_2), annealed at room temperature for 24 hours, and then annealed at 100 °C for 24 hours. All measurements are carried out at room temperature in linear regime ($|V_{ds}| = 0.1$ V). (a) Degradation of the maximum drain current $\Delta|I_{on-lin}|$, (b) threshold voltage shift $\Delta|V_{th}|$, and (c) transconductance degradation $\Delta|g_m|$.

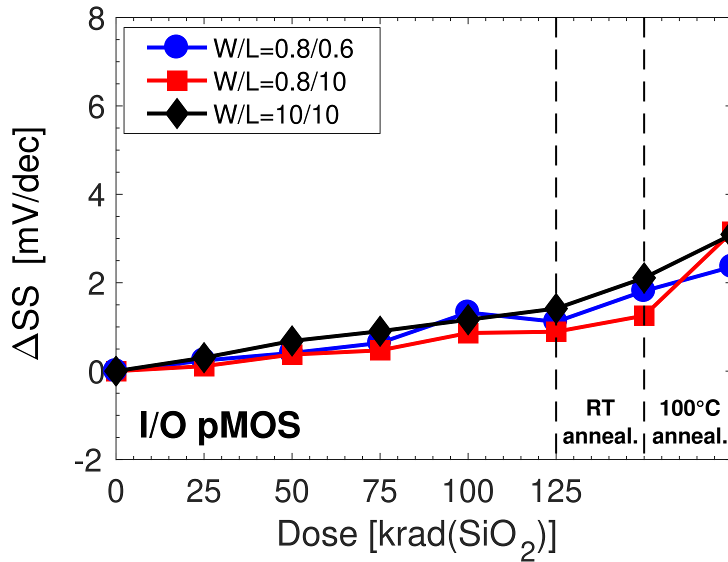


Figure 2.8: Subthreshold swing in the linear regime ($|V_{ds}| = 0.1$ V) for I/O 5V pMOSFETs irradiated up to 125 krad(SiO_2), annealed at room temperature for 24 hours and finally annealed at 100 °C for 24 hours.

variation ΔSS as a function of dose in I/O pMOSFETs. After 125 krad(SiO_2), the ΔSS is lower than 2 mV/dec, independently of the channel dimension, proving very low density of interface traps along the gate oxide [76]. The analysis of the SS is limited to pMOSFETs, as in nMOSFETs the sub-threshold region is dominated by the drain-to-source leakage current induced by the STI.

Figure 2.9 shows leakage current as a function of the dose for different channel dimensions of I/O nMOSFETs and pMOSFETs. The extreme degradation of the I_{off} visible between 25 krad(SiO_2) and 50 krad(SiO_2) indicates the total cumulated dose necessary to invert the lateral regions close to the STI sidewalls, independently of the channel dimension. At 125 krad(SiO_2), the I_{off} increases from about 10^{-14} A to 10^{-6} A. Room temperature and high temperature annealing induce a decrease of I_{off} of about two orders of magnitude, due to partial recombination of the positive trapped holes in the STI oxides.

2.2.3 TID response of core transistors

Figure 2.10 shows the influence of the channel dimensions on the TID sensitivity of core nMOSFETs. Small degradation of the large devices indicated modest charge trapping in the gate oxide and along its interface with the Si bulk. The channel dimension dependence is similar to the one of I/O transistors, as the worst-case response is found in narrow and long channel transistors. However, the magnitude of the radiation-induced degradation is much lower than I/O transistors. This lower sensitivity to TID effects can be due to higher doping profiles and different fabrication processes used in the core transistors.

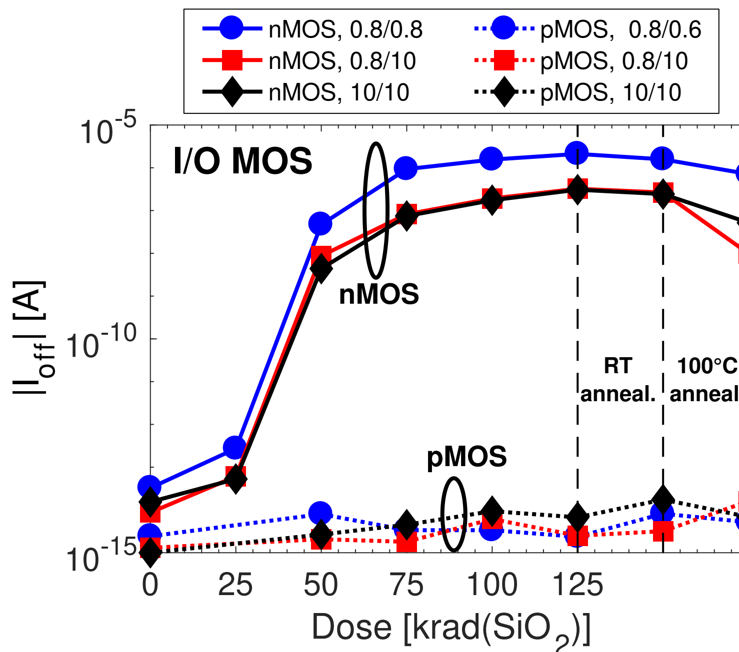


Figure 2.9: Radiation-induced leakage current at room temperature of I/O 5V nMOSFETs and pMOSFETs irradiated up to 125 krad(SiO_2). After the exposure, transistors were annealed for 24 hours at room temperature and for 24 hours at 100 °C. The I_off is defined as the drain current at $|V_{gs}| = 0$ V at $|V_{ds}| = 0.1$ V.

On the other side, the channel length dependence of core devices is more evident than I/O ones, due to the higher doping of halo implantations, necessary to reduce the leakage current of the reduced channel length of core devices. Room temperature induces a slight recovery of the parametric shift, due to recombination of trapped charges in the STI oxides.

Figure 2.11 reports the influence of the channel dimensions on the TID sensitivity of core pMOSFETs. Results are very similar to I/O pMOSFETs, but with lower TID degradation.

2.3 Discussion

Experimental results on 150 nm MOSFET highlight the high sensitivity of the TID response to channel width, channel length, and type of transistors. The slight degradation of the V_{th}, g_m and SS of the largest devices suggests modest charge buildup in gate oxide and its interface in all transistors. The TID effects of 150 nm MOSFETs are dominated by charge buildup in SiO_2 of STI, degrading narrow transistors (RINCE) [37], consistent with previous works on 180 nm, 130 nm and 65 nm technology nodes [37, 39]. nMOSFETs with narrow channel exhibit large negative V_{th} shifts and increased I_{off} currents. During the high temperature annealing, the almost complete recovery of V_{th} of narrow transistors indicates neutralization of positive trapped charges in the STI. The neutralization is probably limited to the upper region of the STI oxide close to the gate corner, as the I_{off}

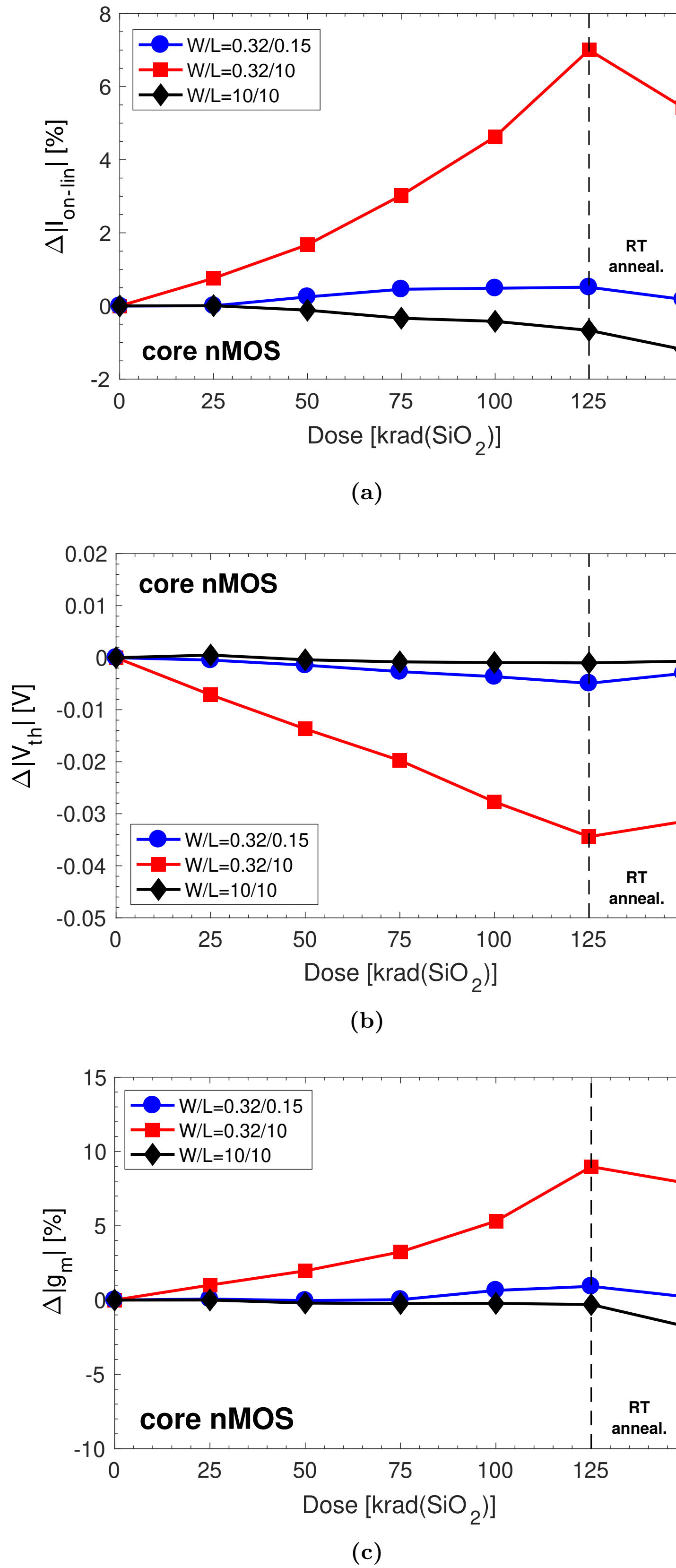


Figure 2.10: Channel dimension dependence of the core HS 1.8V nMOSFETs. Transistors were irradiated up to 125 krad(SiO_2) and annealed at room temperature for 24 hours. All measurements are carried out at room temperature in linear regime ($|V_{ds}| = 0.1$ V). (a) Degradation of the maximum drain current $\Delta|I_{on-lin}|$, (b) threshold voltage shift $\Delta|V_{th}|$, and (c) transconductance degradation $\Delta|g_m|$.

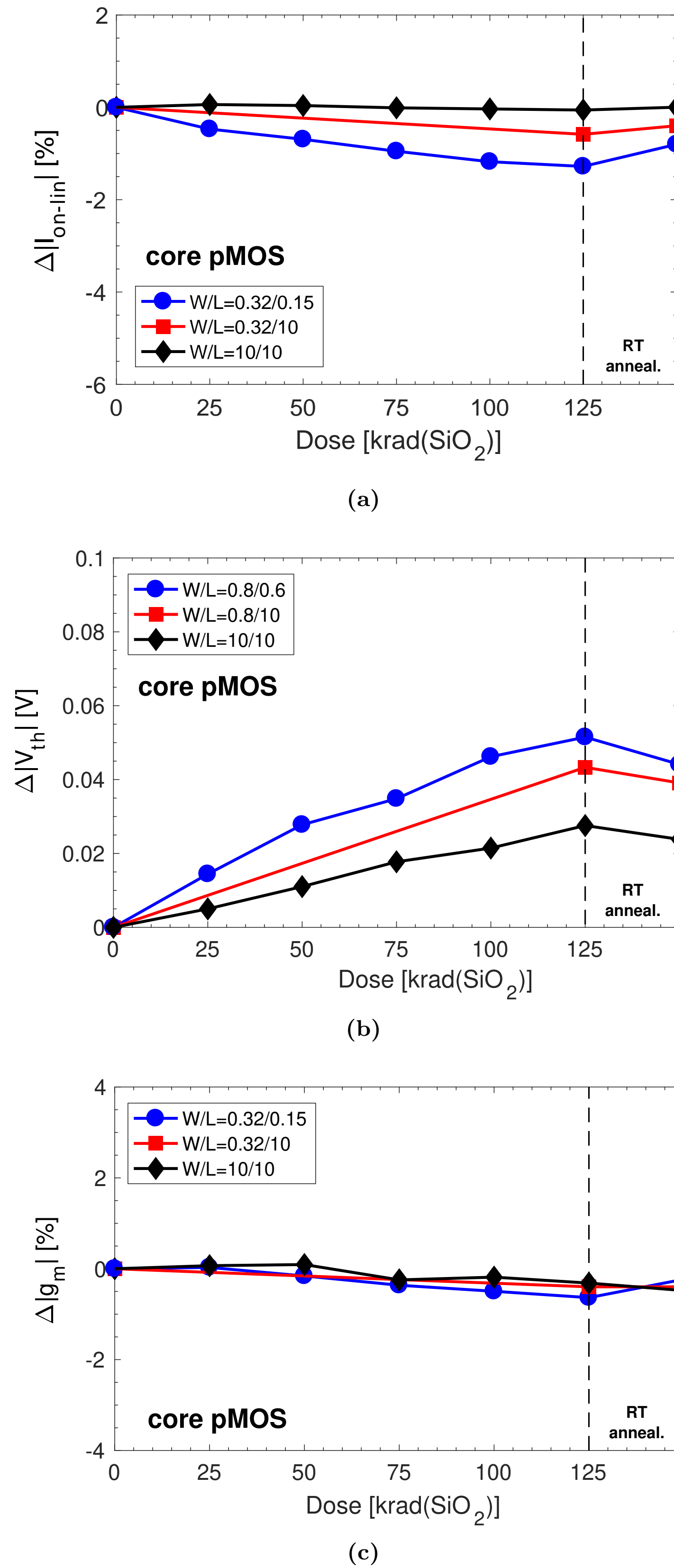


Figure 2.11: Channel dimension dependence of the core HS 1.8V pMOSFETs. Transistors were irradiated up to 125 krad(SiO_2) and annealed at room temperature for 24 hours. All measurements are carried out at room temperature in linear regime ($|V_{ds}| = 0.1$ V). (a) Degradation of the maximum drain current $\Delta|I_{on-lin}|$, (b) threshold voltage shift $\Delta|V_{th}|$, and (c) transconductance degradation $\Delta|g_m|$.

current do not completely recover such as the V_{th}. This is consistent with a model where the electrical field applied to the nMOSFET gate during the high temperature annealing ($V_{gs} = V_{dd}$ in nMOSFETs) drift holes and H^+ of the upper corner of the STI toward the SiO_2/Si interface [39, 87]. At the SiO_2/Si interface of the corner of the STI, holes can recombine with tunneling electrons and H^+ can depassivate Si-H bondings, generating new interface traps, negatively charged.

Another interesting results is the channel length dependence of the TID degradation of nMOSFETs. Short channel nMOSFETs show lower TID sensitivity than long channel transistors. This effect can be related to the halo implantations, which increase the average bulk doping in the channel region. Transistors with larger doping concentration are less affected by radiation, because larger amount of charge are required to alter the carrier distribution. The influence of halo implantations are even more visible in core LL nMOSFETs, probably characterized by large halo doping to decrease the leakage current.

On the other side, the response of pMOSFETs are also dominated by charge buildup in the STI, but pMOSFETs are more radiation tolerant than nMOSFETs. The higher tolerance of pMOSFETs can be related to the limited charge yield related to the low electrical field applied to the gate during the irradiation [103]. The ground bias of pMOSFET generates low densities of positive trapped charges in the gate oxide and in the oxide at the corner with the STI, leading to limited TID effects.

Finally, the TID sensitivity is clearly higher in the I/O transistors than core transistors. This difference is associated to the reduced thickness of gate oxide combined with the higher doping profiles and different fabrication processes adopted in the core transistors.

2.4 TID response of an op-amp designed in 150 nm 3V technology

The following irradiation tests aim to understand how the degradation of transistors can influence more complex circuits. We report in this section the TID response of an operational amplifier (op-amp) designed with the use of I/O 3.3V transistors. The available input and output terminals of the op-amp are shown in Figure 2.12. The op-amp has an operating voltage (V_{dd}) of 3.3 V and a reference current (I_{bias}) of 10 μA, while the output is activated by 3.3 V at the enable port (en). Several dies from the same wafers are irradiated at room temperature up to 125 krad(SiO_2) with the op-amps connected in buffer configuration. In buffer configuration, the op-amp output is short-circuited to the inverting input, while the not-inverting input is connected to a function generator. The irradiations are carried with several waveforms applied to the input of the buffer: 0.3 V DC, 1.6 V DC, 3 V DC, sine with 1.6 V peak-to-peak amplitude or sine with 3.2 V peak-to-peak amplitude. The sine waveforms have a base voltage of 1.6 V and frequency of 100 kHz. At several irradiation steps, the offset voltage and the off supply current are measured by using the connections shown in Figure 2.12.

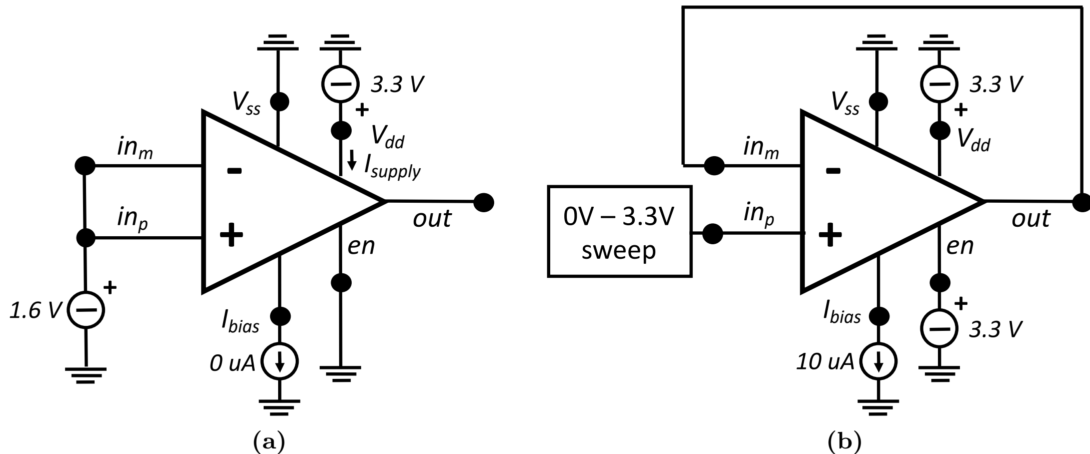
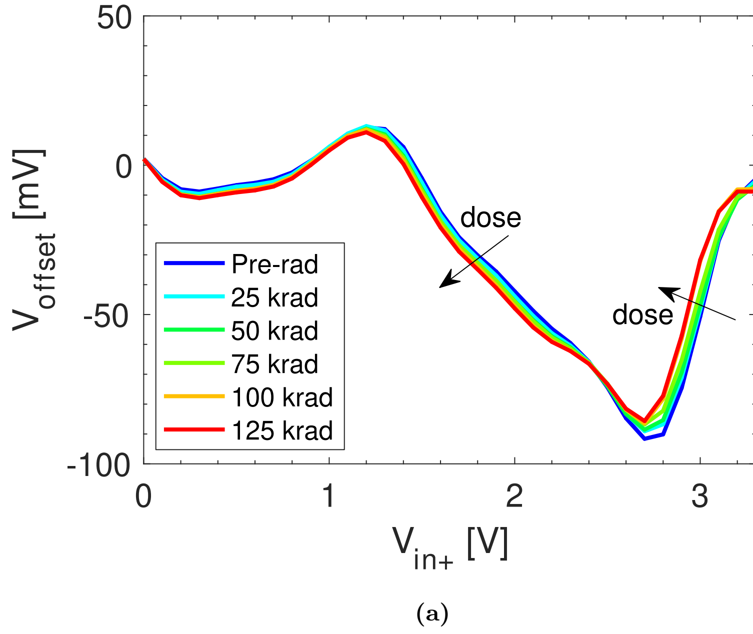


Figure 2.12: Electrical connections used to measure the (a) power supply leakage test and (b) the offset voltage.

The offset voltage test is carried out by connecting the op-amp in the buffer configuration and by reading the output voltage, when a DC signal is swept from 0 V to 3.3 V in the not-inverting terminal (see Figure 2.12(a)). The offset voltage $V_{off-set}$ is calculated as the difference between the output voltage and the voltage at the not-inverting terminal ($V_{offset} = V_{out} - V_{in+}$). Figure 2.13(a) shows the $V_{off-set}$ as a function of V_{in+} at several doses, when op-amps are irradiated in the 0.3 V DC configuration. Figure 2.13(b) shows the variation of the V_{offset} at $V_{in+} = 1.6$ V at different input waveforms applied to the input during the irradiations. The variation of the op-amp offset is negligible, regardless of the waveform applied to the input during the irradiation, with less than 10 mV of ΔV_{offset}.

The off leakage test is carried out by measuring the supply current at the V_{dd} terminal when the op-amp is in off state ($en = 0$ V) and inputs are short circuited to 1.6 V, as shown in Figure 2.12(b). Figure 2.14 plots the supply leakage current as a function of the dose, when op-amps are irradiated with several input waveforms. The leakage current of the op-amp increases with the dose. Before the exposure, the leakage current is around 4 x10^{-11} A and it increases of about two order of magnitude after 125 krad(SiO_2). The increase of the leakage is mostly due to the increase of the I_{off} of the I/O 3.3 V nMOSFETs. The magnitude of the damage depends slightly on the input waveform. Worst-case is found when the not-inverted input is connected to low voltage (0.3 DC, or also *sine* $A = 1.6$ V). Indeed, as shown in previous work, the charge yield and the charge transport in the gate and STI oxides depends on the bias condition during the irradiation, which can influence the TID response of the transistors.



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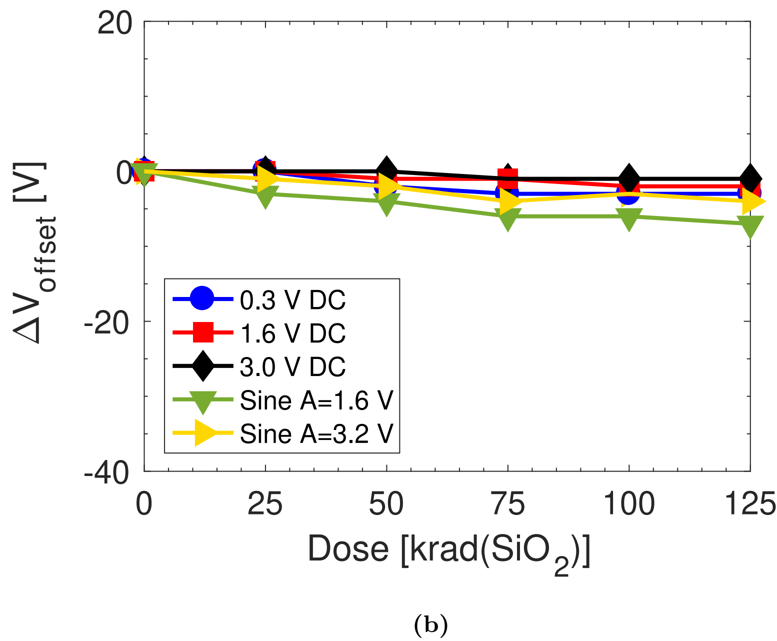
(a)



(b)

Figure 2.13: Offset voltage of the operational amplifier measured with the connections shown incFigure 2.12(b) The operational amplifier was exposed up to 125 krad(SiO_2). (a) Offset voltage as a function of dose for 0.3 V DC condition. (b) Degradation of the offset voltage output at V_{in+} = 1.6 V for different bias input during the irradiation.

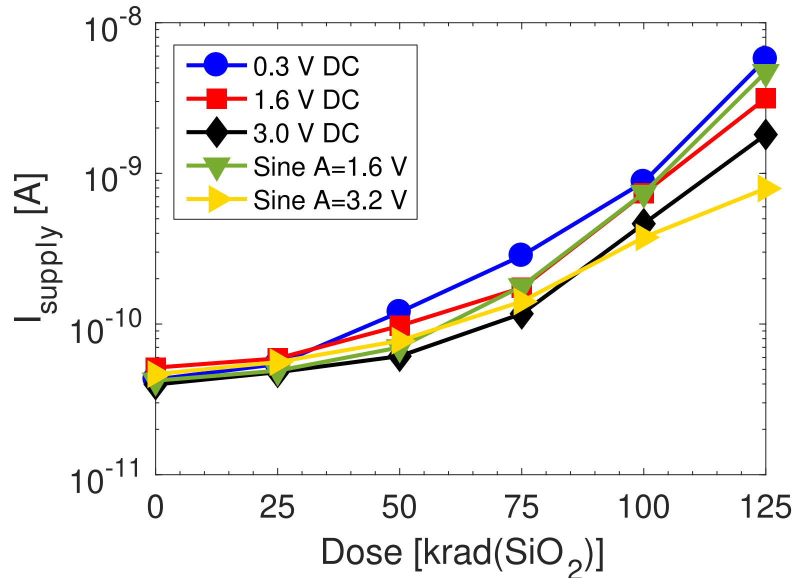


Figure 2.14: Leakage supply current of the operational amplifier exposed up to 125 krad(SiO_2), measured with the connections shown in Figure 2.12(a). Each curve refers to different bias conditions during the irradiation.

2.5 Conclusions

The TID sensitivity of 150 nm MOSFETs depends on channel dimension and type of transistor (nMOSFET or pMOSFET, I/O or core). The radiation-induced degradation is dominated by positive charge buildup in the STI. The most sensitive transistors are the narrow and long I/O nMOSFETs, which show large negative shift of the threshold voltage and extremely high leakage currents. Core transistors are more tolerant than I/O transistors, due to the scaled thickness of gate dielectric combined with the higher doping profiles and different fabrication processes adopted in the production of I/O and core transistors. Moreover, a channel-length dependence is clearly visible in the TID response of nMOSFETs. Short nMOSFETs exhibit less TID sensitivity than long channel transistors, due to increased average bulk doping caused by the halo implantations. On the other side, pMOSFETs show modest parametric shifts because of large e-h recombination at low electrical fields. Finally, an operational amplifier designed by 3.3 I/O transistors is irradiated and characterized up to 125 krad(SiO_2), in order to understand how the degradation of transistors can influence more complex circuits. The leakage current of the op-amp in off operation increases more than two order of magnitude, in agreement with the measured increase of leakage cur-rents of 3.3V I/O nMOSFETs, while the offset voltage degrades of less than 10 mV, in agreement to the modest V_{th} shift of the 3.3V transistors.

Chapter 3

65 nm Si CMOS technology

The 65 nm lithographic node was introduced in the commercial market in 2007. At the European Laboratory for Particle Physics (CERN), a commercial 65 nm CMOS technology has been selected for the development of application specific integrated circuits (ASICs). Most of ASICs used in the LHC detectors are designed in the older 250 nm CMOS technology, which is not able to satisfy the requirements of high speeds and larger bandwidth for the read-out electronic of the trackers. Indeed, the planned 10x luminosity increase of the LHC at CERN will require electronics in the 65 nm technology able to withstand ultra-high doses of up to 1 Grad(SiO_2) over 10 years of operation.

The TID response of modern CMOS technologies was evaluated up to 1 Grad(SiO_2), in recent works [37, 89], including the influence of irradiation on transistor variability [104] and the influence of the dose rate [105]. Typically, the thin SiO_2 gate oxide of modern transistors is insensitive to radiation-induced charge buildup in the gate dielectric [28]. However, as introduced in Sections 1.3.1 and 1.3.2, transistor performance is degraded by radiation-induced effects in thick dielectrics used during manufacturing, such as the shallow trench isolation (STI) and spacer dielectrics (Figure 3.1) [37, 38]. Radiation-induced degradation mechanisms related to charge trapping in the STI have been extensively characterized in the past by various studies [37, 87, 106]. The positive charge buildup in the STI can lead to the opening of parasitic drain-source leakage paths in nMOSFETs, and to degradation of the on-current of narrow-channel pMOSFETs [96].

On the contrary, TID issues related to the spacers have been just recently identified [84, 90] and are currently under investigation. In 65 nm MOSFETs, the LDD spacers are made by Si_3N_4 over a thick layer of SiO_2, as shown in Figure 3.1. The previous study on this devices [37] showed that a large drive current degradation affects the shortest MOSFET when irradiated at ultra-high doses. This effect is called Radiation-Induced Short-Channel Effect (RISCE) [37, 90] (see Section 1.3.2). The worst TID response was found in pMOSFETs, where the positive charge buildup in the spacer dielectrics triggers an increase of the series resistance. Additionally, a large threshold voltage shift in short-channel pMOSFETs was reported during high temperature annealing for devices biased in

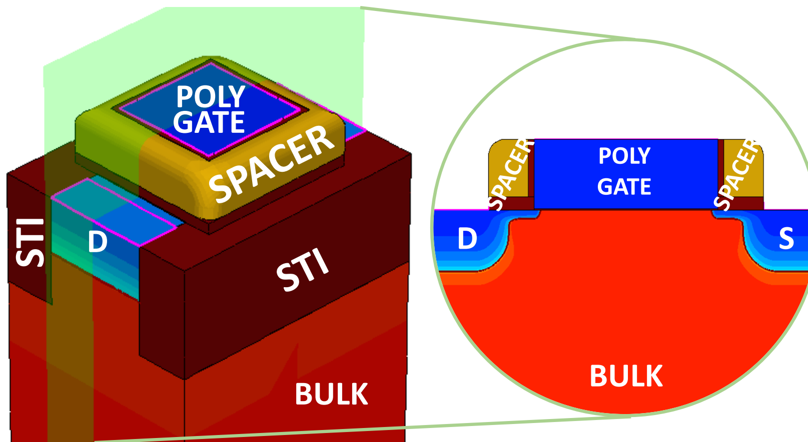


Figure 3.1: Schematic 3D view of modern CMOS devices with STI and spacer dielectrics. Yellow = Si_3N_4, brown = SiO_2, red = n-doped Si, blue = p-doped Si.

the "diode" configuration ($|V_{gs}| = 1.2$ V and $|V_{ds}| = 1.2$ V). This effect was far less evident when switching the role of source and drain terminals, and such asymmetry was associated with a non-uniform spatial density of defects along the channel. Further investigations by $1/f$ noise and charge pumping (CP) measurements confirmed that the transistors irradiated and annealed in the "diode" mode are characterized by a higher interface trap density at the source than at the drain [90]. However, the spatial profile of interface traps was not clearly characterized and discussed.

In this chapter, I focus on the investigation of the spacer charge buildup and on the spatial distribution of interface traps along the gate SiO_2/Si interface. The defects are studied during irradiation and after high temperature annealing under two different bias conditions, "on" and "diode", showing the large influence of the bias on the generation of the interface traps. Finally, experimental results are discussed and compared with the result of 3D Technology Computer-Aided Design (TCAD) simulations.

The work presented in this chapter has been carried out in collaboration with: CERN, Geneva, Switzerland; University of Udine, Udine, Italy; University of Salento, Lecce, Italy; and University of Vanderbilt, Nashville, USA.

Most of the results and figures presented in this chapter have been published and/or submitted in the following peer-reviewed publications:

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and H+ transport on the total-ionizing-dose response of 65 nm MOSFETs irradiated to ultrahigh doses," in *IEEE Transactions on Nuclear Science*, vol. 65, no. 1, pp. 164-174, Jan. 2018. **Winner of the Outstanding Paper Award: 2017 IEEE Nuclear and Space Radiation Effects Conference - NSREC, New Orleans, LA, USA, July 2017.**

Moreover, the results have been presented at the following international conferences:

- Radiation Effects on Components and Systems - RADECS 2018, Gothenburg, Sweden, 16th-21th September 2018, oral presentation about "Charge Buildup and Spatial Distribution of Interface Traps in 65 nm pMOSFETs Irradiated to Ultra-high Doses".
- Nuclear and Space Radiation Effects Conference - NSREC 2018, New Orleans, USA, 17th-21th July 2017, oral presentation about "Influence of LDD spacers and H+ transport on the total-ionizing-dose response of 65 nm MOSFETs irradiated to ultrahigh doses".

3.1 Devices and experiments

3.1.1 Device description

The Devices Under Test (DUTs) were manufactured in a 65 nm bulk CMOS process using a SiO_2 gate oxide with a nominal operating voltage of 1.2 V. The chip and the transistor structure are shown in Figure 3.2. For this experiment, I used the "Charge Pumping 1" column, containing Enclosed Layout (ELT) pMOSFETs with the same gate width W of 10 μm and three different lengths L of 60, 240 and 480 nm. Transistors had separate gate, bulk, source and drain contacts, with no electrostatic discharge protection. A custom probe card and a switching matrix were used to bias and measure the transistors at the same time during the exposure.

3.1.2 Irradiation conditions and measurements details

Irradiations were performed at the University of Padova using an X-ray irradiator composed of a tungsten tube with peak energy deposition at 10 keV [100]. To reach doses up to 400 Mrad(SiO_2), the dose rate was set to 5.12 Mrad(SiO_2)/h. Each irradiation test was performed at room temperature on an array of MOSFETs comprised of three transistors with channel lengths of 60, 240, and 480 nm. After the 400 Mrad(SiO_2) exposure, devices were annealed at 100 °C for 24 hours. During irradiation and the annealing, all pMOSFETs of the array were biased in one of the following conditions: "diode" ($|V_{gs}| =$ 1.2 V and $|V_{ds}| =$ 1.2 V) or "on" ($|V_{gs}| =$ 1.2 V and $|V_{ds}| =$ 0 V).

Ten different chips from the same wafer were tested; at least two devices of each type were evaluated for all experimental conditions, with typical results shown below. The static characteristics of the transistors were measured with a semiconductor parameter analyzer

(HP 4156) at different irradiation steps and after annealing. The switching matrix allowed the connection of the gate terminal of each transistor to a pulse generator (HP 8110) for CP measurements [107, 108]. A pulse signal with 50% duty cycle was applied to the gate. Source and drain terminals were biased at -0.1 V or left floating, depending on the type of measurement, while the bulk terminal was at 0 V. All CP measurements reported in this work were performed by sweeping the amplitude (fixed base technique [108]). The high level V_{gH} of the gate pulse signal was constant at 1.2 V, and the low level V_{gL} was swept down from 0.4 V to -0.8 V. The frequency of the pulse signal was 1 MHz with 100 ns of rise-fall time. The CP current is calculated by subtracting the bulk current at low gate frequency (f = 1 kHz) from that at high frequency (f = 1 MHz) to remove the leakage component [109].

3.2 Experimental results

In the following section, the I_{on-lin} and I_{on-sat} currents are defined, respectively, as the drain-to-source currents in the linear region ($|V_{ds}|$ = 0.1 V), and in the saturation region ($|V_{ds}|$ = 1.2 V), when the channel is in strong inversion at $|V_{gs}|$ = 1.2 V. Similar notation is used for the threshold voltage V_{th-lin} and V_{th-sat}. Finally, the curves labelled with REV (reversed) are measured by reversing the role of the source and drain terminals.

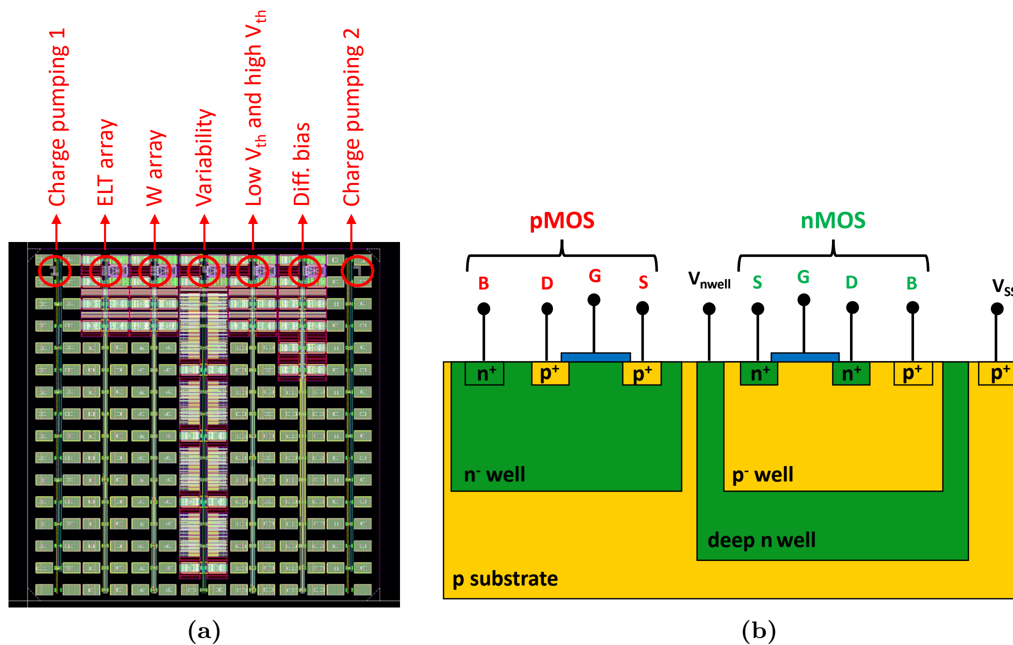


Figure 3.2: (a) Die layout with different columns of transistor arrays for several purposes. (b) Schematic representation of the transistors under test.

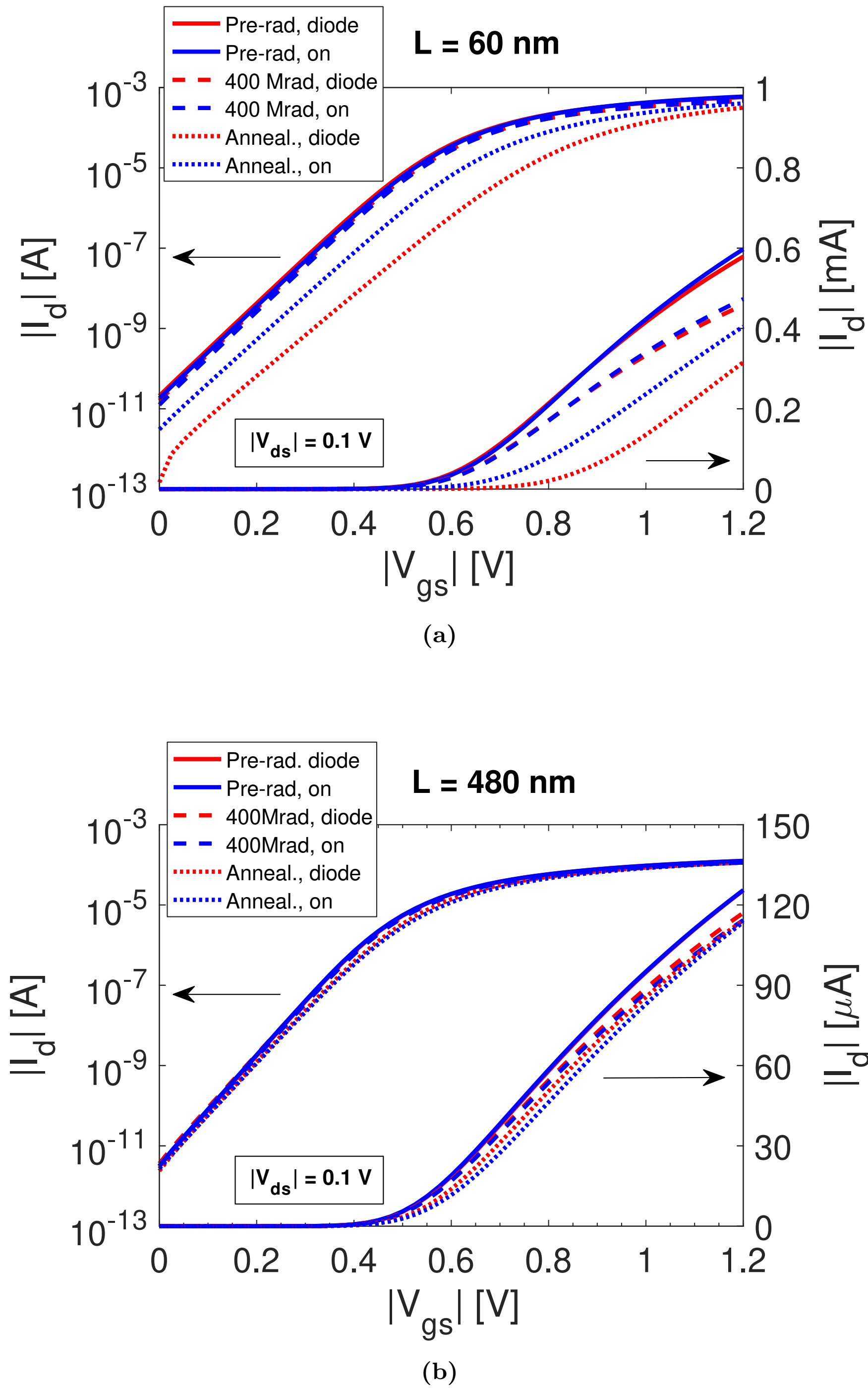


Figure 3.3: $|I_d| - |V_{gs}|$ of pMOSFETs in the linear region ($|V_{ds}| = 0.1$ V). Transistors were irradiated to 400 Mrad(SiO_2) and annealed at 100 °C for 24 hours in "diode" and "on" configurations. (a) $L = 60$ nm. (b) $L = 480$ nm. The left sets of curves and y-axis labels are in logarithmic scale, and the right sets and y-axis labels are in linear scale. (From [94])

3.2.1 Static DC measurements

Figure 3.3 plots the $|I_d| - |V_{gs}|$ characteristics of the 60 and 480 nm pMOSFETs, irradiated up to 400 Mrad(SiO_2), and then annealed for 24 hours at 100 °C in the "diode" or "on" bias configurations. The measurements were carried out in the linear region with $|V_{ds}| = 0.1$ V. The radiation-induced degradation is channel-length dependent with worst-case in the short channel transistor. The results are consistent with RISCE effects described in [84] and [90]. After 400 Mrad(SiO_2), the degradation is attributed to the increase of the series resistance in both "on" and "diode" configurations. In the linear region of operation, the voltage drop due to the series resistance (proportional to the drain current) more significantly affects the shortest device because it has the highest I_{on-lin} current. After the annealing, the shortest transistor also exhibits a significant V_{th} shift and a slight subthreshold swing (SS) increase.

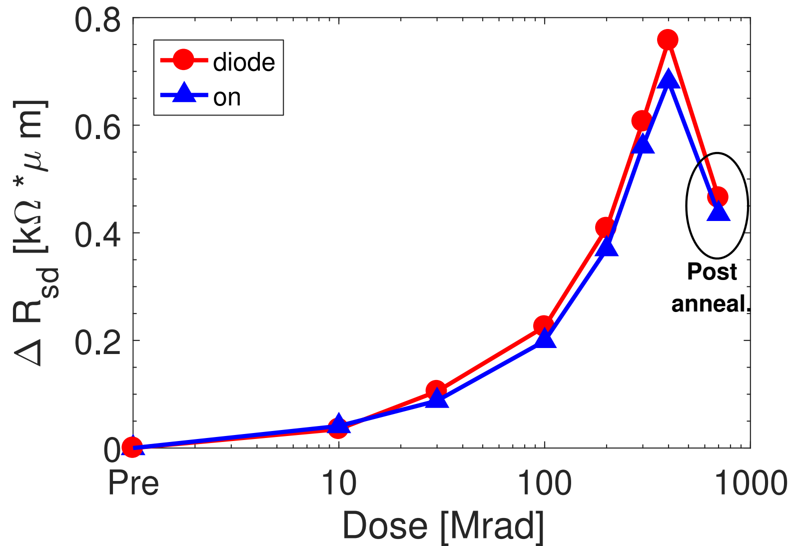


Figure 3.4: Average degradation of the series resistance of pMOSFETs irradiated up to 400 Mrad(SiO_2) and then annealed at 100 °C for 24 hours in the "diode" and "on" configurations. (From [94])

The worst-case is found for the "diode" configuration, which exhibits a percentage decrease $\Delta|I_{on-lin}|$ of -46% vs. -32% for the "on" configuration. Using the technique described in [110], the series resistance R_{sd} was found to be independent on the channel length. The average degradation ΔR_{sd} between different channel-lengths is shown in Figure 3.4, which reports the variation of the series resistance normalized by the channel width as a function of the cumulative dose. The ΔR_{sd} was measured during the exposure up to 400 Mrad(SiO_2) and after high temperature annealing. The series resistance increases with dose for both the "on" and "diode" bias conditions. Before the annealing, the ΔR_{sd} is about 0.7 $k\Omega \cdot \mu m$, equivalent to 70 Ω for these pMOSFETs with $W = 10$ μm. After 24

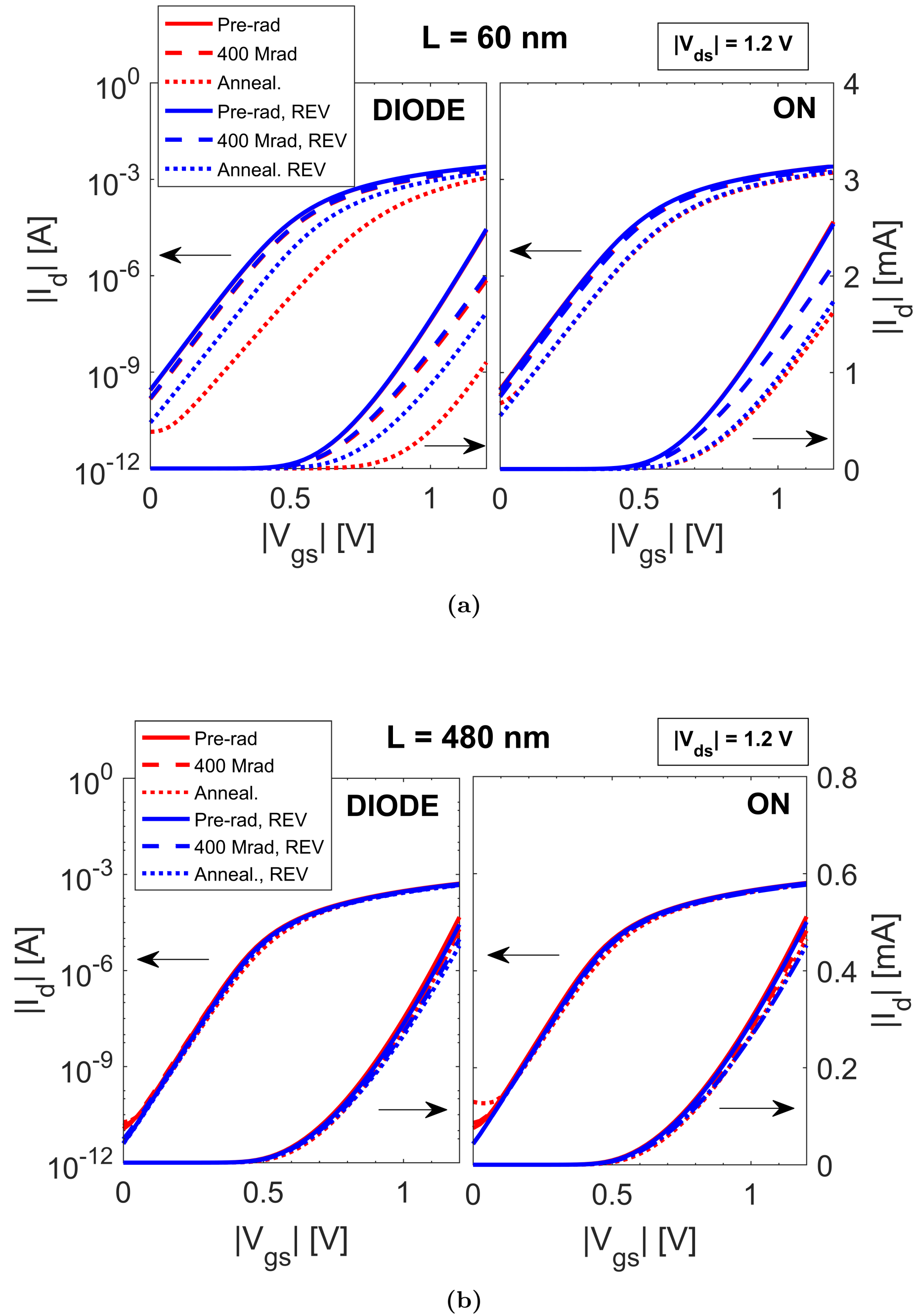
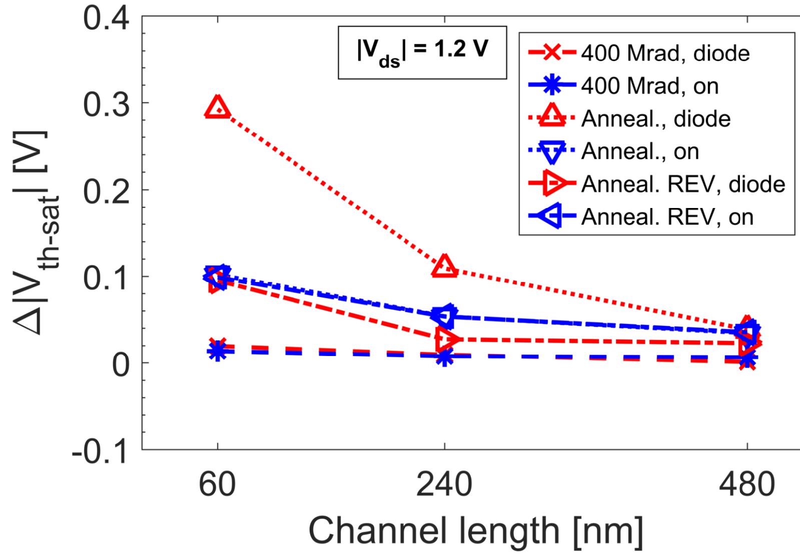
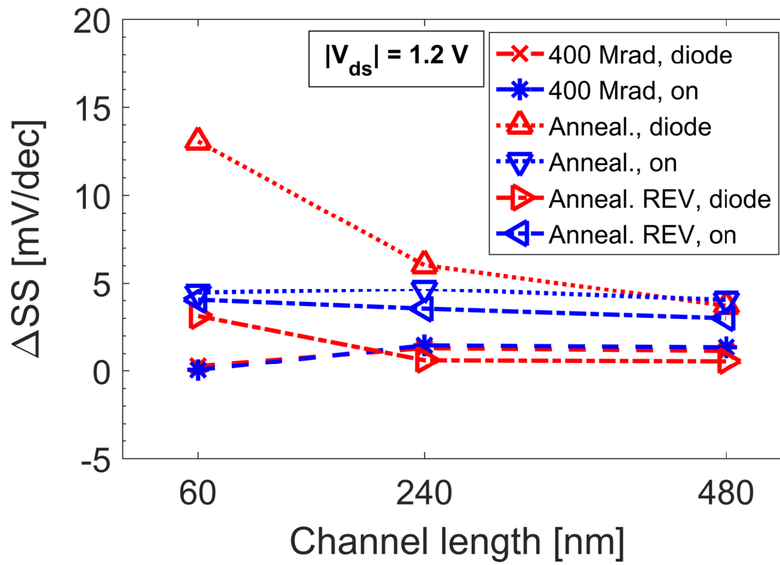


Figure 3.5: (a) $|I_d| - |V_{gs}|$ characteristics of pMOSFETs in the saturation region ($|V_{ds}| = 1.2$ V), irradiated up to 400 Mrad(SiO_2) and annealed at 100 °C for 24 hours in "diode" and "on" configurations. (a) $L = 60$ nm. (b) $L = 480$ nm. (From [94])



(a)



(b)

Figure 3.6: TID response in the saturation region ($|V_{ds}|$ = 1.2 V) of pMOSFETs irradiated up to 400 Mrad(SiO_2) and annealed at 100 °C for 24 hours in "diode" and "on" configurations. (a) Threshold voltage shift. (b) Subthreshold swing variation. (From [94])

hours of annealing at 100 °C, the series resistance decreases in both "on" and the "diode" conditions, exhibiting a ΔR_{sd} of about 0.45 k$\Omega \cdot \mu$m.

Figure 3.5 shows the TID response of short and long pMOSFETs measured in the saturation region ($|V_{gs}| = 1.2$ V), before exposure, after 400 Mrad(SiO_2), and after 24 hours of annealing at 100 °C in the "diode" and "on" configurations. The measurements are carried out in direct and reverse (REV) modes. After high temperature annealing, devices biased in either the "on" or the "diode" configuration significantly differ in response. The shortest channel transistor annealed in the "diode" condition exhibits a different $|I_d| - |V_{gs}|$ curve when source and drain terminals are reversed. This asymmetric response between direct and reverse measurements is not visible in transistors exposed and annealed in the "on" condition [90]. Large transistors show a lower TID sensitivity, and are characterized by a typical symmetric $|I_d| - |V_{gs}|$ response.

Figure 3.6(a) summarizes the radiation-induced shift of the threshold voltage V_{th-sat} as a function of the channel length at 400 Mrad(SiO_2) and after annealing in both "diode" and "on" bias configurations. The plot shows that, after 400 Mrad(SiO_2) irradiation, all transistors, independently of L, exhibit a negligible V_{th-sat} shift (< 15 mV). After annealing, the V_{th-sat} shift is much larger and channel-length dependent. The shortest transistor in the "diode" configuration is the worst-case, with a $\Delta|V_{th-sat}|$ of 290 mV ("diode" bias) and 100 mV ("on" bias). In contrast, the longest channel transistor exhibits similar $\Delta|V_{th-sat}|$ shifts - around 35 mV - when irradiated and annealed in the "diode" and "on" configurations. Interestingly, when the short transistor is "on"-biased, $|I_d| - |V_{gs}|$ characteristics are the same when the roles of the drain and source are reversed (REV), while in the "diode" configuration the transistor exhibits an asymmetrical DC characteristic and very different values of $\Delta|V_{th-sat}|$. A similar response is found for the variation of the SS measured in saturation ($|V_{ds}| = 1.2$ V), as shown in Figure 3.6(b).

3.2.2 Charge pumping results

The charge pumping technique has been used in [111–113] to characterize the spatial density of interface traps in the lateral regions of the SiO_2/Si gate interface. Our CP measurements follow a similar approach, and have been carried out under the conditions described in the previous section. Figure 3.7 shows the charge pumping current in the smallest pMOSFET before exposure, at 400 Mrad(SiO_2), and after 24 hours of annealing at 100 °C. The irradiation and annealing were carried out in the "diode" configuration. The red curves indicate the "source" charge pumping currents (I_{cp-S}), obtained with the source biased at -0.1 V and the drain floating. The blue curves show the "drain" charge pumping currents (I_{cp-D}), with the drain biased at -0.1 V and the source floating. When either the source or drain is disconnected, the interface traps in the extensions left floating are not pumped and do not contribute to CP current at $V_{gL} > 0.18$ V. At $V_{gL} <$ -0.18 V, the gate pulse starts to pump the channel region until the maximum current I_{cp-max} is reached at $V_{gL} =$ -0.8 V, where both extensions and the entire channel are pumped. The

noisy CP curves for the pre-irradiation characteristics at V_{gL} > -0.18 V are due to the very small CP current (of the order of 1 pA), which is comparable to the leakage current through the gate oxide.

Figure 3.8 shows a qualitative representation of the spatial profiles of $V_{fb}(x)$ and $V_{th}(x)$, which determine the gate voltage necessary to locally accumulate and invert the underlying Si at position x. The effective pumped region depends on the lower level of the pulse, V_{gL}. In these devices, I define the CP current at V_{gL} = -0.18 V as the LDD extension CP current, in particular as I_{D-LDD} (Drain side), when the source is floating, and as I_{S-LDD} (Source side), when the drain is floating. The maximum I_{cp} current at V_{gL}=-0.8 V is defined as I_{cp-max}, as it is due to the pumping of the interface traps of the entire channel plus the LDD extensions.

From Figure 3.7, the I_{cp-ch} increases with dose from the initial value of 60 pA for a fresh sample to 200 pA after 400 Mrad(SiO_2) and 900 pA after the annealing. The I_{cp} in the source extension increases during the exposure and after annealing, whereas I_{cp} in the drain extension increases with dose but abruptly decreases after annealing. These results show that interface traps in the channel and LDD extension regions can respond quite differently to post-irradiation annealing, as discussed below.

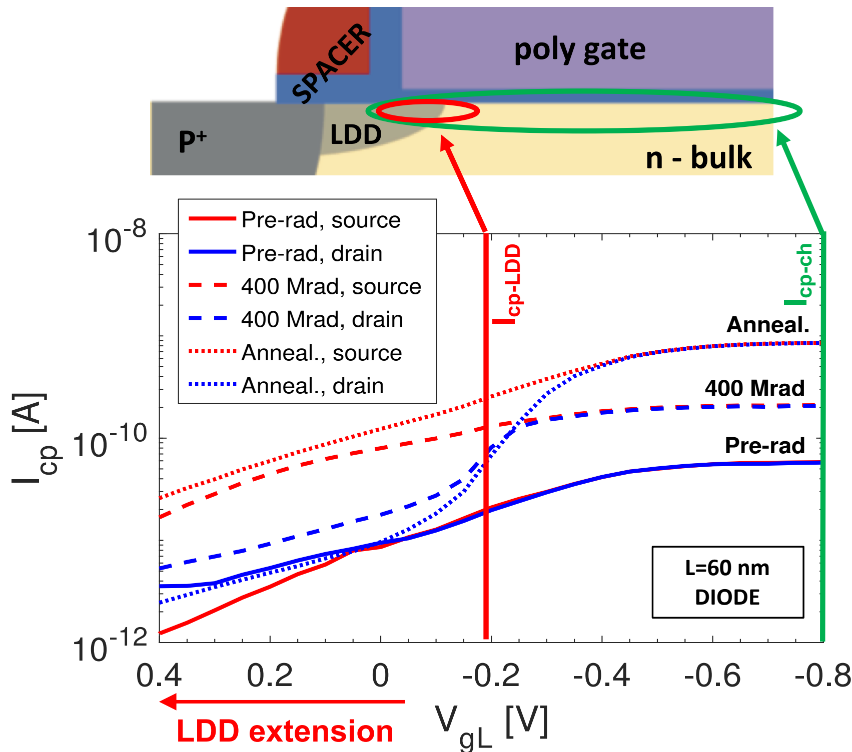


Figure 3.7: CP currents for the shortest pMOSFET before the exposure, after 400 Mrad(SiO_2), and after high temperature annealing in the "diode" configuration. The CP measurements were measured at room temperature in two different modes: (drain) drain at -0.1 V and source floating, (source) source at -0.1 V and drain floating. (From [94])

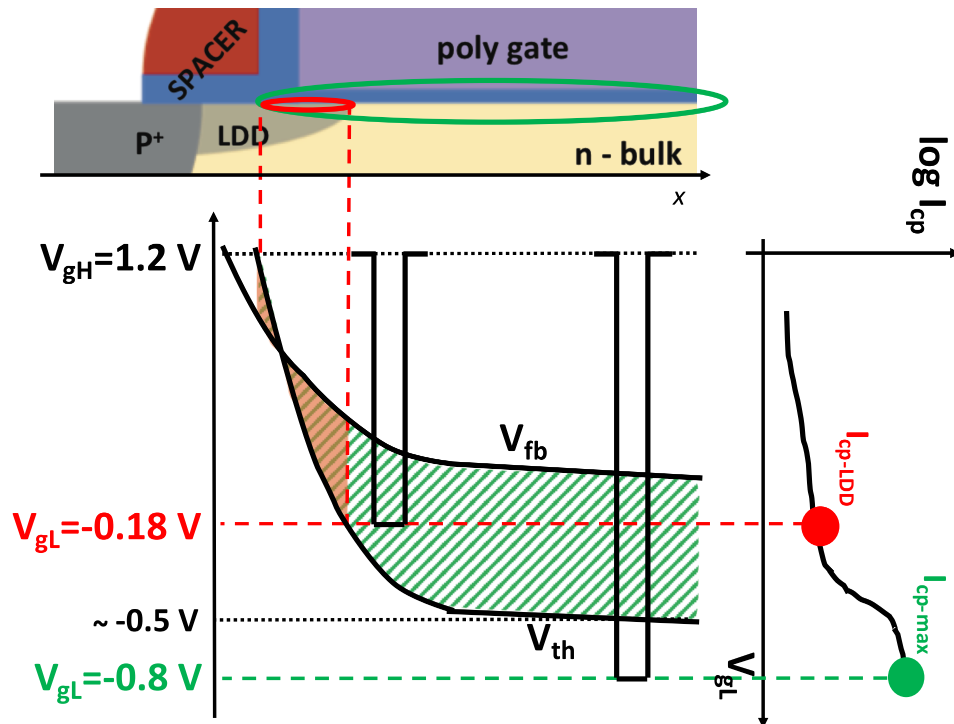
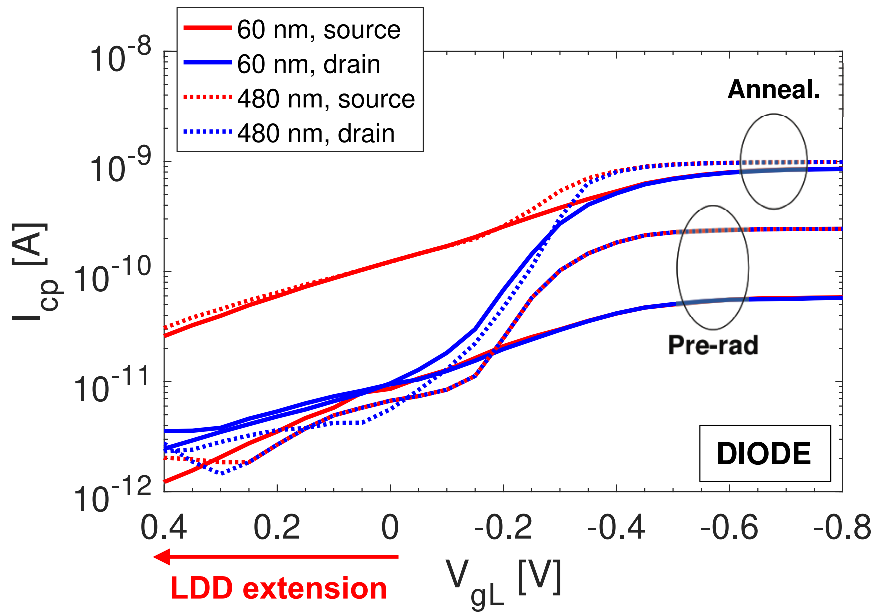


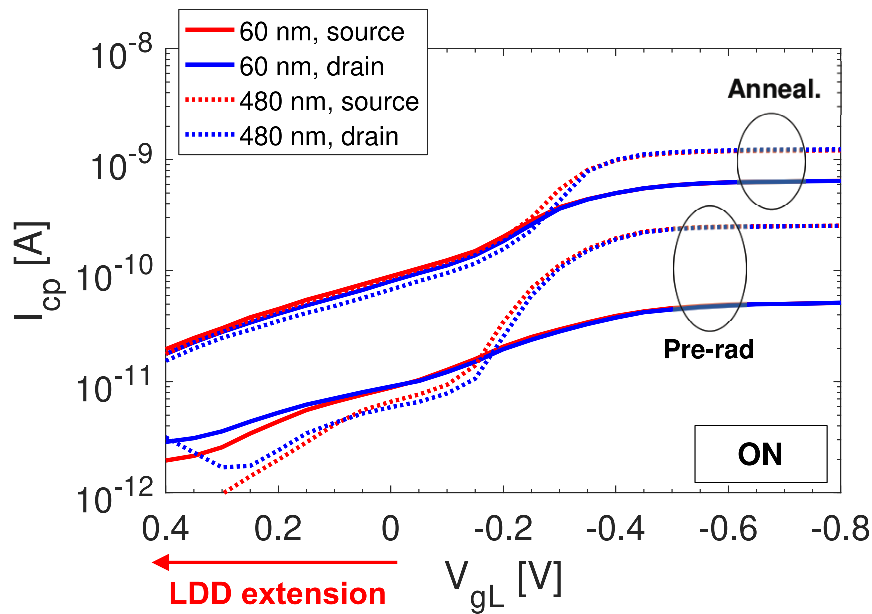
Figure 3.8: Qualitative representation of the spatial profiles of $V_{fb}(x)$ and $V_{th}(x)$. The pumped region depends on V_{gH} and V_{gL}, that continuously bring the local pumped Si area from accumulation to inversion. For 65 nm pMOSFETs, the CP pulses with V_{gL} = -0.18 V and V_{gL} = -0.8 V pump traps in the LDD lateral region and in the entire channel, respectively. (From [94])

Figure 3.9 shows the charge pumping current as a function of the pulse low level V_{gL} in pMOSFETs with different channel lengths. The plots show the CP characteristics before irradiation and after 24 hours of annealing at 100 °C in (a) "diode" and (b) in the "on" bias configurations. Currents are not normalized to the gate size. Hence, longer channel transistors have a larger signal at V_{gL} < -0.6 V where interface traps in the whole channel contribute to the signal. In contrast, for small amplitude pulses, when V_{gL} > -0.18 V, only interface traps in the extension implants and under the LDD spacers contribute to the CP current [111]. In this range the CP current of fresh transistors is not channel-length dependent, as the lateral LDD fabrication process is equal in all transistors irrespective of their length.

In fresh devices, the source and drain CP currents overlap for all V_{gL}. However, when the pMOSFETs are annealed, the shapes of the source and drain CP currents depend on the bias conditions during the exposure/annealing. In the "diode" configuration (a), I_{cp-S} and I_{cp-D} have different shapes after the annealing. For V_{gL} > -0.18 V, the I_{cp-S} increases up to I_{S-LDD} = 300 pA, while the I_{cp-D} is constant around the pre-irradiation values with I_{D-LDD} of about 40 pA. In contrast, in the "on" bias configuration (b), I_{cp-S} and I_{cp-D} overlap for all V_{gL}, both before irradiation and after annealing.



(a)



(b)

Figure 3.9: CP currents on pMOSFETs before the irradiation and after 400 Mrad(SiO_2) plus annealing at 100 °C for 24 hours. The CP measurements were carried out at room temperature in two different modes: (drain) drain at -0.1 V and source floating, (source) source at -0.1 V and drain floating. The bias condition during the irradiation and annealing were (a) in "diode" configuration and (b) in "on" configuration. (From [94])

3.2.3 Spatial density of interface traps

Figure 3.10 shows the estimated interface trap density in the LDD extension regions, obtained from the measurement of I_{S-LDD} and I_{D-LDD} using the technique described in [112]. The technique allows one to estimate the lateral pumped region from the measured CP current for the specified geometries under the hypothesis of uniform interface-trap distribution before irradiation, in the energy range of interest [112]. Under this hypothesis, at V_{gL} = 0.18 V, I estimate a lateral pumped region of about 18 nm from the gate oxide edge under the LDD spacers. Although the density in the LDD regions before exposure and after irradiation plus annealing does not depend on the channel length; however, it is affected by the bias configuration applied during annealing. In the "diode" configuration, the interface-trap generation is higher in the source LDD extension (almost 1 x10^{12} cm^{-2}) than in the drain extension (2 x10^{11} cm^{-2}). In contrast, in the "on" configuration, the interface trap density distribution after annealing is symmetric between the source and drain, almost 7 x10^{11} cm^{-2} in both source and drain LDDs.

An estimate of the interface-trap density inside the channel can be obtained via standard techniques [107, 108] by considering that I_{CP-ch} = I_{cp-max} - I_{CP-LDD}, where I_{CP} max is the maximum CP current at V_{gL} = -0.8 V and I_{CP-LDD} is the CP current at V_{gL} = 0.18 V. Figure 3.11 shows the average density N_{it-ch} in the channel as a function of channel length. Pre-irradiation CP measurements show a constant density of 3 x10^{10} cm^{-2}, regardless of channel length. After irradiation to 400 Mrad(SiO_2), the average density inside the channel increases up to 6 x10^{10} cm^{-2}, with twice-as-large density in the smallest pMOSFET irradiated in the "diode" bias configuration. After high temperature annealing, the channel density of interface traps is channel-length dependent - more strongly in the "diode" configuration. The trap density increases most noticeably in the shortest pMOSFET, which exhibits N_{it-ch} of 7 x10^{11} cm^{-2} in the "diode" configuration and 3 x10^{11} cm^{-2} in the "on" configuration, while large pMOSFETs exhibit N_{it-ch} of about 1.2 x10^{11} cm^{-2}.

3.3 Discussion

The measurements presented above significantly extend the discussions of RISCE from those in [37] and [90]. I now discuss the buildup of fixed charge in the spacers and the spatial distribution of interface traps under the "diode" and "on" bias configurations. As discussed in [90], the Ion degradation of pMOSFETs during irradiation is caused by an increase in series resistance. The radiation-induced accumulation of trapped positive charge in the spacer dielectrics above the LDD region is responsible for this degradation and, as shown in Figure 3.4, is largely independent of whether "on" or "diode" bias is applied during irradiation.

The degradation of "diode"-biased transistors is in agreement with a model where the interface trap activation is due to electric field-driven drift of H^+ ions. The electric

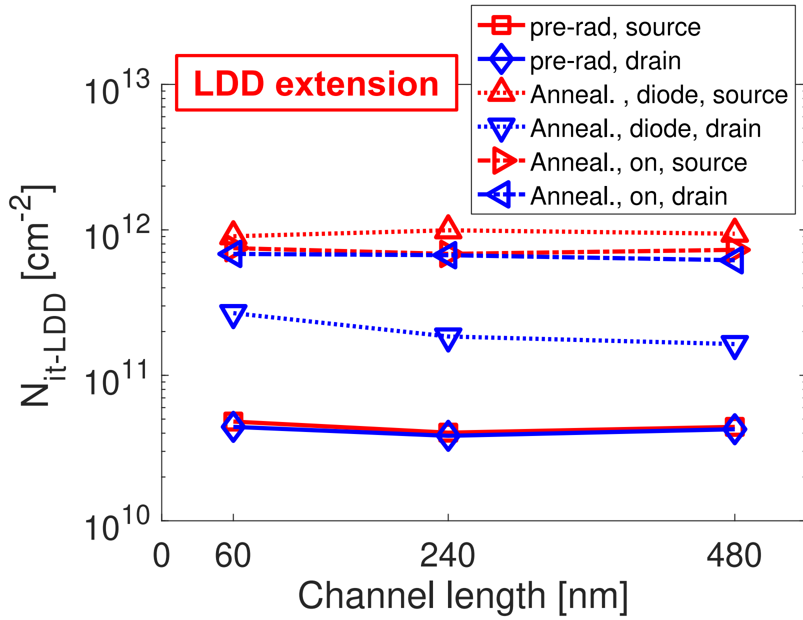


Figure 3.10: Density of interface traps in the LDD spacer extensions in pMOSFETs before irradiation, after 400 Mrad(SiO_2), and after 24 hours of annealing at 100 °C. (From [94])

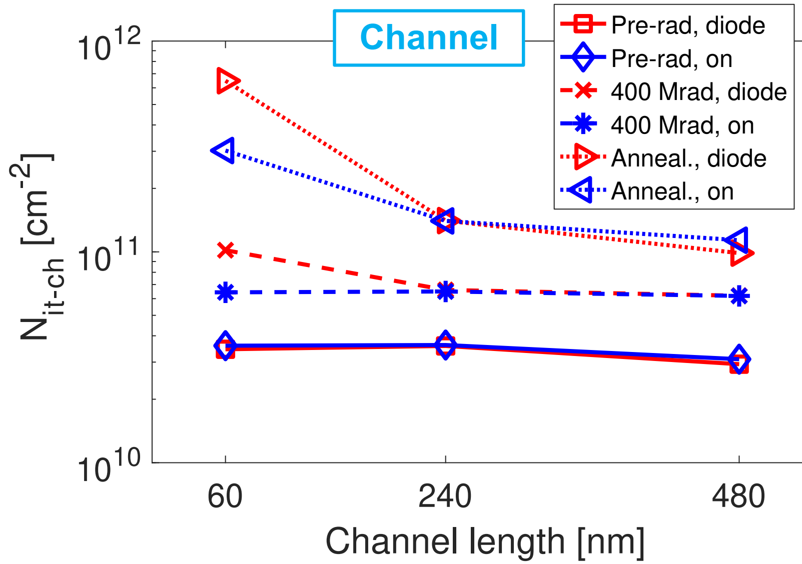


Figure 3.11: Density of interface traps in the channel in pMOSFETs before irradiation, after 400 Mrad(SiO_2), and after 24 hours of annealing at 100 °C. (From [94])

field favors the drift the H^+ ions from the source spacer to the SiO_2/Si interface close to LDD/gate oxide edge. Because of the lateral electric field, charged hydrogen can also reach the channel interface under the gate oxide. This effect is suggested by Figure 3.11, where the interface trap density in the channel region is strongly channel-length dependent. In short-channel transistors the drift of H^+ ions from the source spacer can more efficiently reach a larger fraction of the gate oxide interface, explaining both the asymmetry and the channel-length dependence of the parametric shift (V_{th}, SS) of Figure 3.6.

In the "on" mode, the interface trap density in the LDD extensions is symmetric (see Figure 3.10), suggesting similar degradation in both source and drain LDD extensions. The SS shift visible in Figure 3.6 is uniform with channel length, indicating an equal interface trap density in the channels of all transistors. The low trap-density N_{it-ch} and the high-trap density N_{it-LDD} at both source and drain LDDs suggest that the H^+ are drifted from both drain and source spacers to the LDD/gate oxide edge, but the absence of any lateral source-to-drain voltage limits H^+ transport only into the LDD extensions and not inside the channel (Figure 3.7). The slight length dependence visible in Figure 3.11 on N_{it-ch} can be due to a partial pumping of the lateral high-density traps of the LDD extensions, causing an overestimation of the N_{it-ch} of the shortest pMOSFET.

In Figure 3.7, the drain CP current for V_{gL} > -0.18 V increases after 400 Mrad(SiO_2) and decreases to pre-irradiation values after annealing at 100 °C in the "diode" configuration, while the source CP current continues to increase during annealing. This difference in response most likely occurs because the source-to-gate electric field is large and positive during annealing (V_{sg} = 1.2 V), but the drain-to-gate electric field is nearly zero (V_{dg} = 0 V). When the applied electric field is large and positive, radiation-induced interface trap densities tend to be stable and/or increasing during 100 °C annealing [28, 114, 115]. However, when the electric field is low, and especially when densities of hydrogen are high, as one expects for the spacers, significant reductions in interface trap densities can occur during elevated temperature annealing [67, 116, 117]. Thus, it is the asymmetry in gate-source and gate-drain electric fields that leads to the differences in interface trap responses in Figure 3.7. In both "diode" and "on" configurations, high temperature annealing also leads to a partial recovery of the series resistance (Figure 3.5), which can be explained by thermally-activated de-trapping of holes in the spacer oxides [90].

3.4 TCAD simulations

In this section, the experimental interpretation and the degradation models in "on" and "diode" configurations are supported by 3D TCAD Sentaurus simulations. The spacer dielectrics are designed as a thick 60 nm layer of Si_2N_3 over 20 nm of SiO_2. The radiation damage is simulated by inserting a uniform spatial density of positive charges in the spacers and by several spatial interface trap distributions.

The manufacturer does not provide any information about the fabrication process,

such as doping concentrations and materials. For this reason, the simulated device structures were designed on the basis of publicly available information and agreement with the experimental characterization of the as-processed devices.

3.4.1 Positive charge buildup in the spacers

The radiation effects during the exposure are simulated in Figure 3.12, which shows the hole density distribution under the source LDD extension of pMOSFET biased in linear region. Similar results are visible at the drain side. The simulated as-processed structure does not contain any defects, whereas the irradiated device is simulated by inserting a uniform spatial density of positive charges in the spacers (Q_{sp} = 6 x10^{18} cm^{-3}); this value was tuned by a comparison between simulations and experimental measurements. Simulations confirm that positive trapped charges deplete the Si regions under the spacers, decreasing the density of the majority carriers and increasing the Si resistivity of the LDD extensions.

Figure 3.13(a) compares the simulated $|I_d| - |V_{gs}|$ with the experimental measurements in the linear region ($|V_{ds}| = 0.1$ V). Similarly to Figure 3.12, irradiated devices have a uniform spatial density of positive charges in both drain and source LDD spacers (Q_{sp} = 6 x10^{18} cm^{-3}). The simulated $|I_d| - |V_{gs}|$ curves agree with experimental measurements,

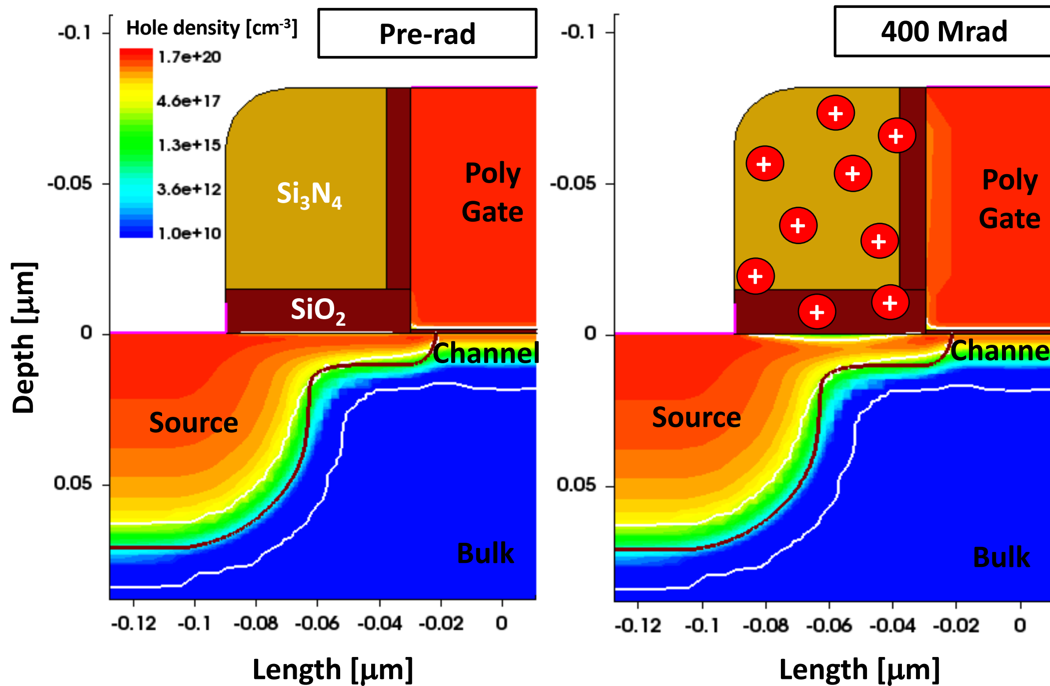


Figure 3.12: Hole density along a cut plane in the channel direction of pMOSFET with $L = 60$ nm and $W = 10$ um biased at $|V_{gs}| = 1.2$ V and $|V_{ds}| = 0.1$ V. The irradiated device is simulated by inserting a uniform density of positive charges of 6 x10^{18} cm^{-3} in the spacer dielectrics. (From [94])

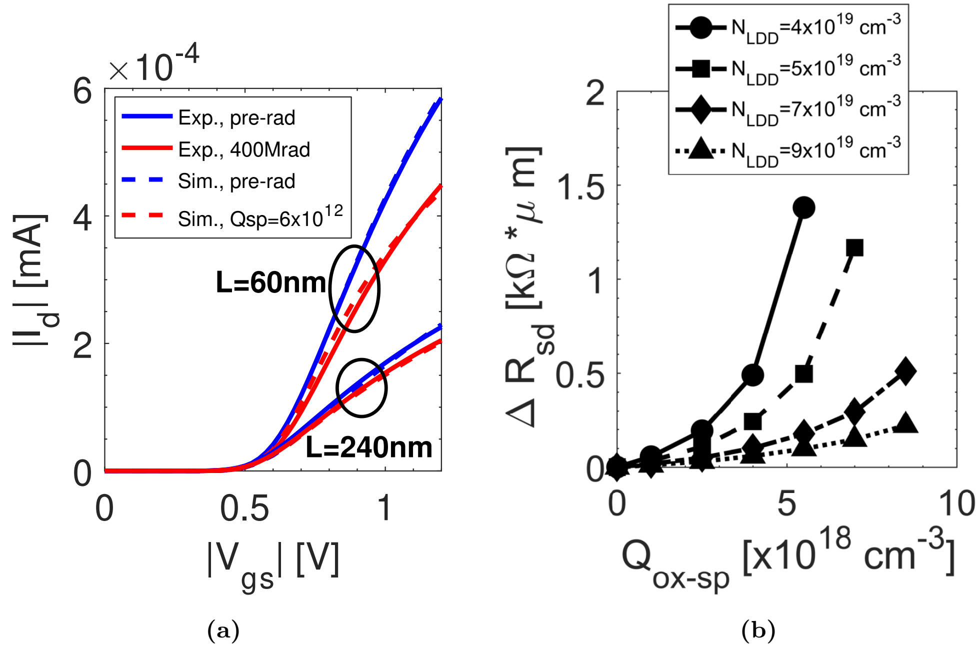


Figure 3.13: (a) Simulated $|I_d| - |V_{gs}|$ compared with the experimental results for pMOSFETs with $L = 60$ nm and $L = 240$ nm in the linear region ($|V_{ds}| = 0.1$ V). The irradiation damage is simulated by a uniform charge density of 6 x10^{18} cm^{-3} in the spacer dielectrics. (b) Simulated variation of the R_{sd} as a function of the charge density in the spacers at different LDD doping concentration; peak values N_{LDD} are indicated in the legend. (From [94])

confirming that the degradation of series resistance is insensitive to the channel length. The quality of fit is similar in both the linear and subthreshold regime (not shown in the figure). However, its effect on the $|I_d| - |V_{gs}|$ characteristics is worse in short-channel transistors due to their higher drain currents.

Figure 3.13(b) shows the series resistance derived from simulations as a function of trapped charge density in the spacers. The N_{LDD} identifies the peak value of p-type dopants implanted in the LDD regions. The series resistance increases with charge density in the spacer dielectrics and depends on the characteristics of the LDD implants, e.g., the LDD doping. Increased doping levels effectively reduce radiation-induced degradation, similarly to what is observed in [97]. However, such a change in LDD doping also renders the device more susceptible to hot carrier effects, thus reducing the efficacy of the LDDs in their primary function.

3.4.2 Influence of the bias

I previously discussed the experimental results for transport in the spacer regions during high temperature annealing. Indeed, the H^+ ions drift is driven by the electric field, depending on the applied bias condition. Simulations in Figure 3.14 show the electrostatic potential in the “on” and “diode” configurations, while the black arrows indicate the

electric field direction. Figure 3.15 provides further insight into the lateral electrical field intensity $|E_x|$ along a cutline in the middle of the gate oxide thickness (at y = -0.8 nm of Figure 3.14).

In the "diode" configuration, the electric field in the source spacer drives the H^+ ions towards the gate electrode. Ions reaching the gate oxide from the source spacer are then subjected to further field-driven transport and reach farther regions of the gate-substrate interface. At the drain side, the electrostatic potential drives the H^+ far from the SiO_2/Si interface, preventing the interface trap activation under the drain LDD extension. The experimental worst-case response of the shortest transistor is hence well explained by the high lateral electric field E_x in the gate oxide.

In the "on" mode, the electrostatic potential is symmetric between source and drain and no lateral field E_x appears in the gate oxide. The electric field is confined within the LDD spacers, and no field drives the H^+ ions in the gate oxide, in agreement with the experimental observations of high N_{it-LDD} and low N_{it-ch}.

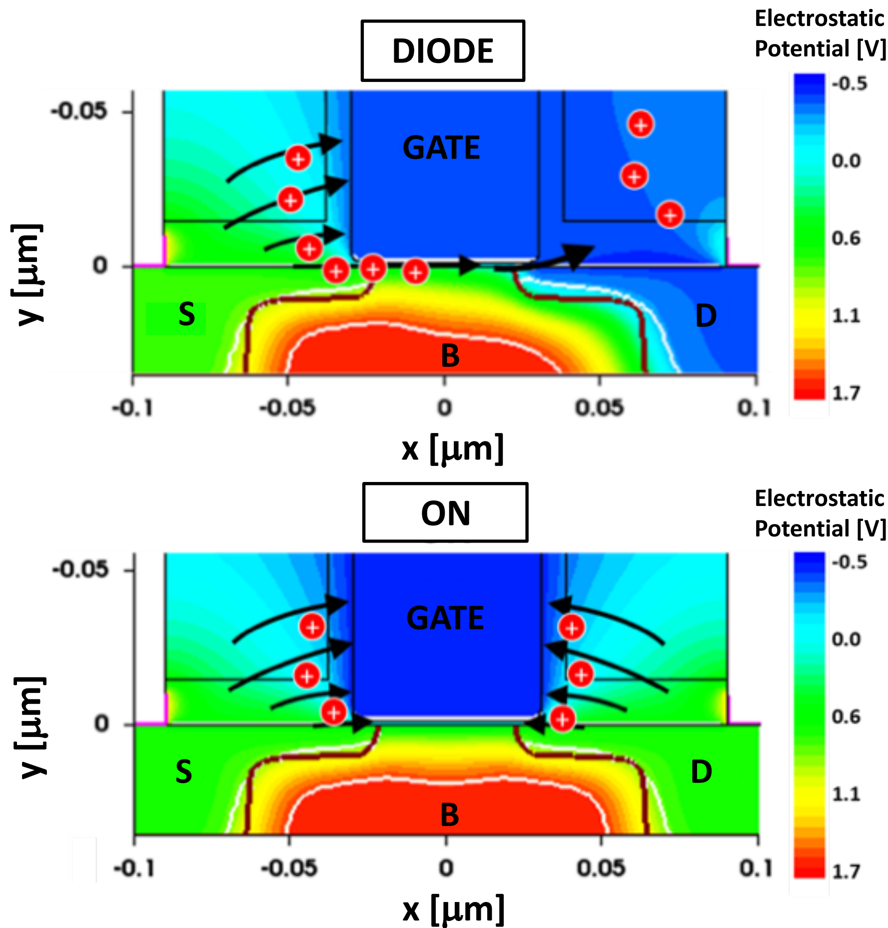


Figure 3.14: Simulations of the electrostatic potential inside a pMOSFET with L = 60 nm, biased in "diode" and "on" mode. The black arrows indicate the direction of the H^+ transport. (From [94])

3.4.3 Asymmetric interface trap distribution

In [90], the different response between direct and reverse characteristics of "diode"-biased transistors was well explained by the analysis of the drain-induced barrier lowering, DIBL, which suggested a higher density of defects close to the source region. Further support for this interpretation is provided by the TCAD simulations. The approximation I chose for a non-uniform distribution of interface traps along the channel is a step function, as illustrated in Figure 3.16(a) for the shortest pMOSFET with L = 60 nm. The step function is defined by a high density level N_{it-LDD} of 3.6 x10^{12} cm^{-2} and a low density level N_{it-ch} of 6 x10^{11} cm^{-2}. Both acceptor and donor defects are energetically distributed with a Gaussian shape, similar to [118]. The position x_{step} of the step function is varied from 0 nm to 60 nm, while the threshold voltage is extrapolated in the direct and reverse configurations at several step positions.

The plot on the top of Figure 3.16(b) shows the normal threshold shift $\Delta|V_{th}|$ and reverse threshold shift $\Delta|V_{th-REV}|$ in the saturation region ($|V_{ds}|$ = 1.2 V). The shift is calculated with respect to the threshold voltage of a defect-free device. The normal $\Delta|V_{th}|$ increases when the density-step position moves toward the drain, due to the increase of the average interface trap density along the channel. However, when terminals are reversed, the threshold shift is smaller: at x_{step} = 18 nm, $\Delta|V_{th}|$ = 0.22 V vs. $\Delta|V_{th-REV}|$ = 0.06 V. The bottom of Figure 3.16(b) shows normalized V_{th}, calculated as $(\Delta|V_{th-REV}| -$

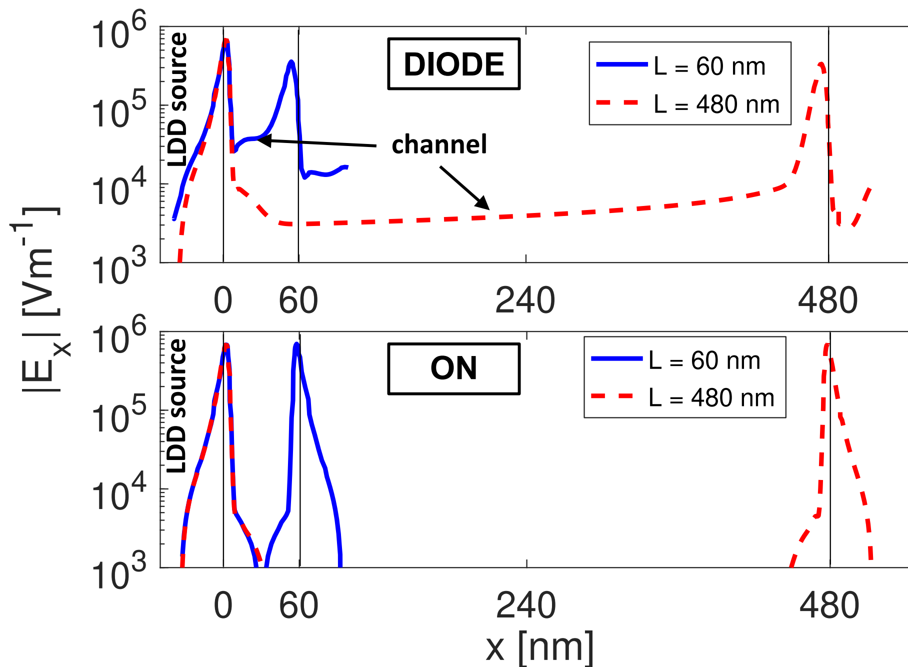


Figure 3.15: A cut plane along the middle of the gate oxide thickness highlights the lateral electric field E_x under the spacers and along the channel. The $x = 0$ nm line identifies the edge of the gate oxide at the source side. (From [94])

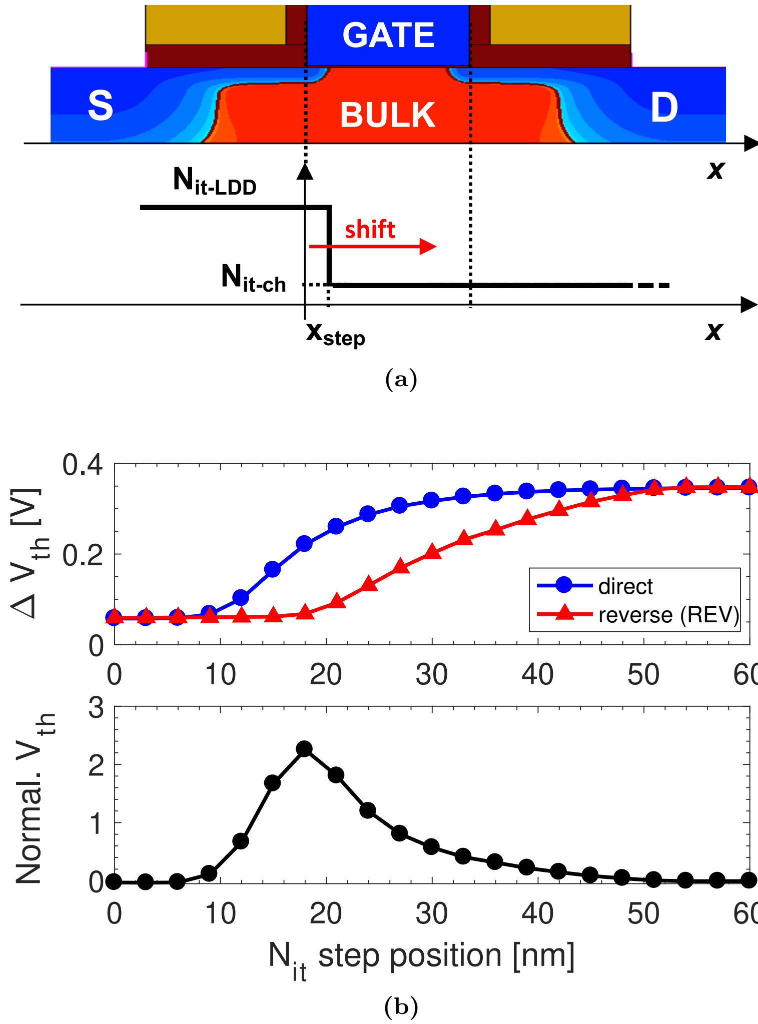


Figure 3.16: (a) The interface trap distribution defined during the TCAD simulations. A density-step function of interface traps is spatially shifted from source to drain in pMOSFET with $L = 60$ nm. (b) The $\Delta|V_{th}|$ is calculated by simulations with the step function distribution in normal and reverse mode. (From [94])

$\Delta|V_{th}|)/\Delta|V_{th}|(x_{step} = 0)$, as a function of x_{step}. The largest difference between direct and reverse modes is found at $x_{step} = 20$ nm, slightly before the midpoint of the channel, when the high interface trap density extends into the channel region at the source side. This asymmetry in the measured threshold voltage agrees with the experimental results of Figure 3.6(a).

In Figure 3.17 the simulated and experimental saturation ($|V_{ds}| = 1.2$ V) transfer characteristics are compared for the $L = 60$ nm pMOSFET with the step function position at $x_{step} = 18$ nm. The slight difference in the pre-irradiation characteristics is most likely due to the approximate structure geometries and doping profiles. The general agreement of the ΔV_{th-sat} between simulations and experimental results confirms that, after irradiation and annealing in the "diode" bias mode, the active interface traps in short-channel transistors are primarily concentrated in the LDD source region as well as in the first 10-20

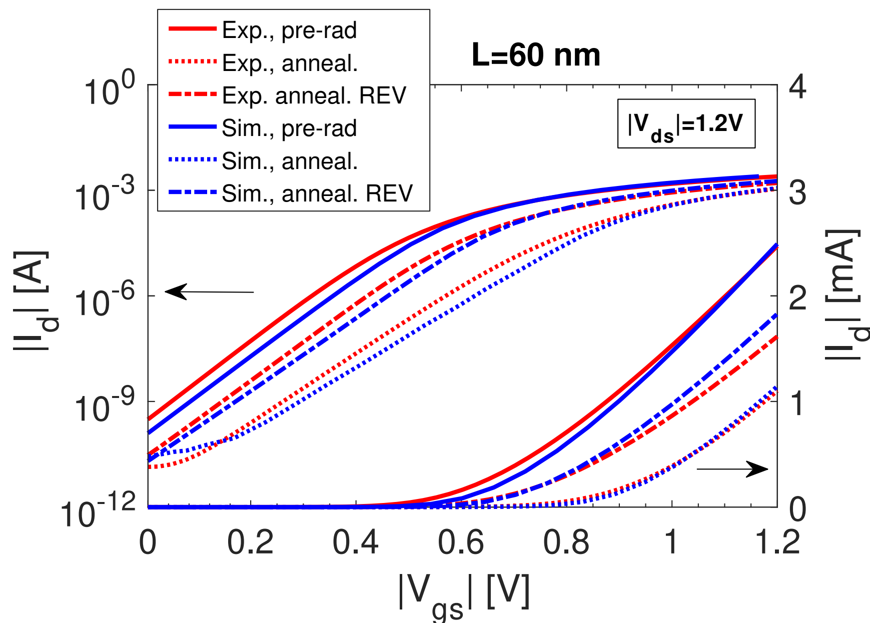


Figure 3.17: Simulated $|I_d| - |V_{gs}|$ compared to the experimental results for pMOSFETs with $L = 60$ nm in saturation region ($|V_{ds}| = 1.2$ V). In simulations, the radiation damage is simulated by a step density function with $x_{step} = 18$ nm, $N_{it-LDD} = 3.6$ x10^{12} cm^{-2} and low level $N_{it-ch} = 6$ x10^{11} cm^{-2}. A clear change in subthreshold swing is observed after irradiation and annealing, consistent with a significant increase in interface-trap density. (From [94])

nm of channel close to the source. Regardless of the quality of the match between the simulated and experimental ΔV_{th-sat}, the SS in the simulation data is slightly larger than in experiments in both direct and reverse (REV) configurations. This mismatch likely occurs because only interface traps are incorporated in the simulation. However, border traps [61, 119] are also present in the real devices. Both types of defects contribute to threshold voltage shifts. However, interface traps more strongly affect subthreshold stretchout than border traps [61, 76, 90, 119], thereby accounting for the greater SS in Figure 3.17 than Figure 3.3.

Finally, it is worth mentioning that a source-drain asymmetry is also observed in nMOSFETs irradiated and annealed in the "diode" mode. In these devices, in contrast to the pMOSFETs, the worst-case ΔV_{th-sat} shift is measured in the reverse (REV) measurements. Because of the opposite voltage polarity in the n-channel transistors, H^+ drifts towards the channel from the drain spacer oxides; hence, in these devices the higher density of interface traps is localized close to the drain. This and other observations in nMOSFETs presented here and in [90] deserve further study.

3.5 Conclusions

The degradation of 65 nm pMOSFETs irradiated at ultra-high doses is dominated by radiation-induced short-channel effects. During irradiation, trapped holes and H^+

are generated in the spacer dielectrics, depleting LDD extensions and increasing the series resistance, independently of the applied bias configuration and of the channel length. During high temperature annealing, the degradation is dominated by interface-trap buildup, which is quite sensitive to the applied source-to-drain bias and is channel-length dependent. Combining experimental results with 3D TCAD simulations, I confirm that, in "diode"-biased transistors, the electric field in the source spacer transports H^+ close to the SiO_2/Si interface, depassivating Si-H bonds and generating a high density of interface traps under the source spacer alone. Worst-case is found in short-channel transistors, where, because of the lateral source-to-drain electric field, H^+ ions reach into the gate oxide and a large density of active interface traps is found also in the channel. In contrast, in "on"-biased transistors the electric field is symmetric and hydrogen drift is limited to the LDD extensions only. In this case, the interface trap generation in the channel is strongly reduced. When devices are annealed in the "diode"-bias condition, interface trap densities increase in the source region as a result of the large positive electric field, and decrease in the drain region as a result of the very low electric field, coupled with a relatively high concentration of hydrogen in the spacer.

Chapter 4

28 nm Si CMOS technology with high-k dielectrics

In this chapter, the TID response of a 28 nm Si commercial CMOS technology is evaluated up to ultra-high doses. This work was carried out within the Scaltech28 experiment developed by the National Institute for Nuclear Physics (INFN), Italy. The application is intended for the future High-Energy Physics (HEP) experiments at the European Laboratory for Particle Physics (CERN), Switzerland. The future plan is to upgrade the 65 nm Si CMOS technology analyzed in the previous chapter with a commercial 28 nm Si CMOS technology, whose higher performance will allow higher granularity and bandwidth of the tracking systems at the Large Hadron Collider (LHC) experiments, like at A Toroidal LHC ApparatuS (ATLAS) and at Compact Muon Solenoid (CMS) [120, 121]. Similar to 65 nm Si CMOS, the future high luminosity of the LHC require chips able to withstand ultra-high dose levels, up to 1 Grad(SiO_2) over 10 years of operation.

Previous chapter and recent works [37, 90, 94, 96, 105] studied the TID response of SiO_2-based 65 nm CMOS technology up to 1 Grad(SiO_2). In these devices, the radiation-induced degradation was stronger in narrow-channel transistors due to the RINCE [37], which is related to charge buildup in STI oxide and its interface [39]. RINCE increases the leakage currents due to the activation of parasitic transistors in n-channel MOSFETs and induces a parametric drift in narrow n and p-channel MOSFETs.

In addition, the scaling limits of SiO_2 [78] have required the introduction of high-k dielectric materials [122]. Consequently, the research interests of the HEP community have moved towards the evaluation of the high-k gate oxide response at ultra-high radiation levels. In recent studies [88, 89, 123, 124], HfO_2-based MOSFETs were investigated up 1 Grad(SiO_2), but additional work is still needed to characterize the sensitivity of HfO_2-based MOSFETs exposed to ultra-high doses.

Finally, in sub-micron technology nodes, halo implantations are extensively used to reduce Short Channel Effects (SCEs) [125]. Halo implantations in Ge-based MOSFETs use a high doping level. When such devices are irradiated up to 1 Mrad(SiO_2), they exhibit an

increase in the off leakage, enhanced interface-trap buildup and greater $1/f$ noise [126, 127]. The influence of the halo on radiation-induced effects in Si-based MOSFETs was studied in some publications. Most of the studies [99, 128] were focused on the development of analytical models that describe the increase in the off-state leakage current in nMOSFETs, considering the charge buildup in the STI and the process variation of the doping profile along the sidewall regions of STI. It has been found that the high variability on the radiation-induced leakage current in nMOSFETs is caused by the statistical variation of the doping implantation process in the regions close to the STI [86]. In particular, a study [99] showed through simulations that the radiation-induced leakage current decreases in 90-nm nMOSFETs, when the doping along the STI sidewalls is increased. Similar results were also obtained in a recent work [87], where radiation-induced STI effects were modelled as a function of the halo implants. In this case, it was demonstrated that the higher doping of halo implantation reduces the magnitude of the radiation-induced off-state leakage currents in nMOSFETs. Therefore, the radiation sensitivity of nMOSFETs can be largely affected by variations in the doping of halo implantation.

In this chapter, I evaluate the radiation-induced effects on 28 nm MOSFETs with high-k oxides at ultra-high doses. By DC and low-frequency noise measurements I obtained insight into TID degradation mechanisms at ultra-high doses for both nMOSFETs and pMOSFETs. Dependences on channel width, channel length and irradiation bias are investigated and discussed, with a primary focus on the mechanisms responsible for the higher TID tolerance of short channel devices. Indeed, new experimental evidences point out a new effect, related to the strong influence of the halo implantation on the TID response of MOSFETs.

The work presented in this chapter has been carried out within the Scaltech28 experiment funded by the National Institute for Nuclear Physics - INFN, in a collaboration with: CERN, Geneva, Switzerland; University of Milano, Milano, Italy; École polytechnique fédérale de Lausanne, Lausanne, Switzerland; and University of Vanderbilt, Nashville, USA.

Most of the results and figures presented in this chapter have been published and/or submitted in the following peer-reviewed publications:

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- [129] S. Bonaldo, S. Mattiazzo, C. Enz, A. Baschirotto, D. M. Fleetwood, A. Paccagnella, and S. Gerardin, "TID Mechanisms and Low-frequency Noise in 28 nm MOSFETs Irradiated to Ultra-high Doses," in *IEEE Transactions on Nuclear Science*. (Accepted for RADECS 2019 conference, Montpellier, France, and currently submitted

for publication in IEEE Transanctions on Nuclear Science).

Moreover, the results have been presented at the following international conferences:

- Nuclear and Space Radiation Effects Conference - NSREC 2018, Kona, Hawaii, USA, 17th-20th July 2018, poster presentation about "Influence of Halo Implantations on the Total Ionizing Dose Response of 28-nm pMOSFETs Irradiated to Ultrahigh Doses". (I was the presenting author)
- Radiation Effects on Components and Systems - RADECS 2019, Montpellier, France, 16th-20th September 2019, oral presentation about "TID Mechanisms and Low-frequency Noise in 28 nm MOSFETs Irradiated to Ultra-high Doses". (I was the presenting author)

4.1 Devices and experiments

4.1.1 Device description

Devices under test are manufactured on Si substrates in a commercial 28 nm bulk CMOS process. A schematic representation of the transistor layout is shown in Figure 4.1 for both nMOSFETs and pMOSFETs. The gate stack is formed by a layer of HfO_2 over a thin layer of SiO_2, with an equivalent oxide thickness of ∼1.1 nm. Transistors are provided in an array structure of pMOSFETs and nMOSFETs with several channel widths (100 nm $\leq W \leq 3$ μm) and channel lengths (30 nm $\leq L \leq 1$ μm). Available channel dimensions are listed in Figure 4.2, while a digital picture of a die containing the array of transistors is shown in Figure 4.3. Even if results are presented for several channel length and channel width, I will mainly focus the discussion of the results by comparing three representative channel geometries: W/L = 100 nm/30 nm (narrowest and shortest), W/L = 100 nm/1 μm (narrowest and longest) and W/L= 1 μm/1 μm (largest and longest).

The transistors had separated drain and gate contacts, while they shared the source and bulk contacts. The gate terminals were protected by ESD protections designed in a two-diodes configuration. A customized probe-card allowed to bias 10 different transistors at the same time during the exposure, while a switching matrix selected the transistors to connect to the measurement system.

4.1.2 The halo implantations

The continuing downscaling of the technology node has led to new limitations and issues in the working principle of modern CMOS transistors. One of the main problem is related to the punch-through effect, caused by the reduced length of the channel of the smallest devices. Indeed, when the effective channel length L_{eff} becomes comparable to the source/drain junction depletion width, the potential distribution along the channel depends on both normal and lateral electric fields. At high V_{ds}, reduced the channel

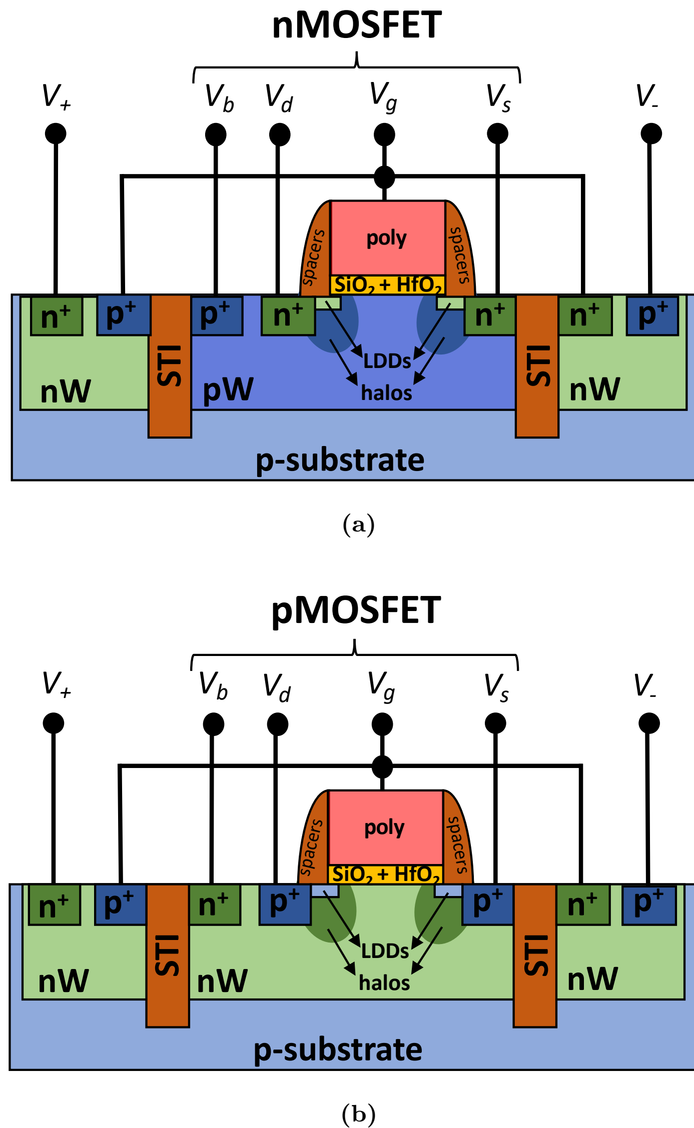


Figure 4.1: Schematic representation of the transistor layout of the 28 nm MOSFETs under test. (a) nMOSFET and (b) pMOSFETs. (From [129])

length causes increased leakage currents, degradation of the subthreshold characteristics and decreased threshold voltage V_{th}. In extremely scaled devices, the L_{eff} is further reduced and the transistor response can collapse due to the ultra-high drain currents and due to lost of gate control on channel carriers. In order to suppress the punch-through effect, modern CMOS technologies employ the halo implantations [130], which are implanted with the same dopant type of the bulk at low energy and at large incident angle to allow the implanted dopants to penetrate underneath the edge of the spacers and of the gate stack. In this way, halos prevent very low L_{eff} by limiting the expansion of the drain depletion region into the channel area when the device works in saturation regime [131, 132].

In Figure 4.4, I represented schematically the 28 nm MOSFET structure. The

28 nm CMOS technology
nMOSFET/pMOSFET

Transistor	W [nm]	L [nm]
#1	100	30
#2	100	80
#3	100	200
#4	100	600
#5	100	1000
#6	500	1000
#7	1000	1000
#8	3000	600
#9	3000	200
#10	3000	30
#11	1000	30
#12	500	30

Figure 4.2: Dimensions of the MOSFETs available for the irradiation test of the 28 nm CMOS technology.

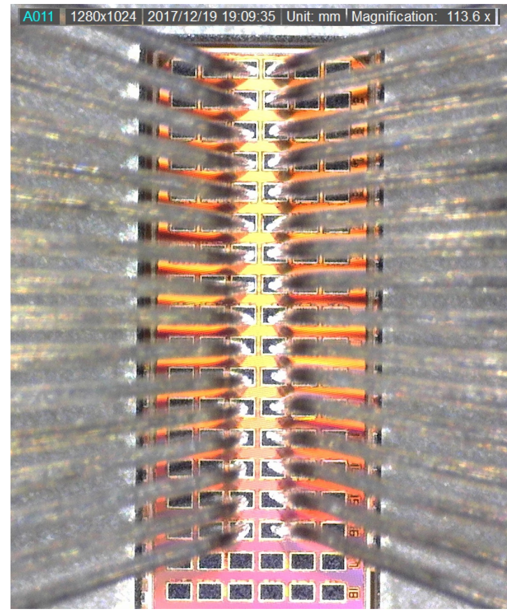


Figure 4.3: Digital photo at 113x magnification of the probe card tips over the pads of transistors in the array structure.

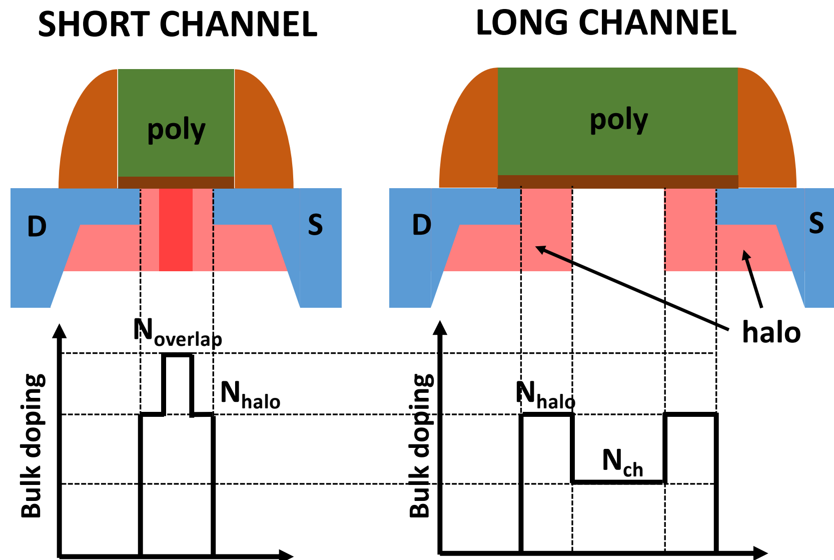


Figure 4.4: 28 nm MOSFET structure with non-uniform doping distribution of the bulk due to the halo implantations. In short-channel transistor the drain halo can overlap with the source one, whereas in long channel transistor halos are confined in the lateral regions of the channel. (From [97])

bulk doping along the channel is not uniform due to the halo implantations and the doping profile depends on the channel length. In short channel transistors the drain halo implantation can overlap with the source one [133], causing an increase in the overall channel doping. In the shortest channel transistors, the overlap of halos can induce a

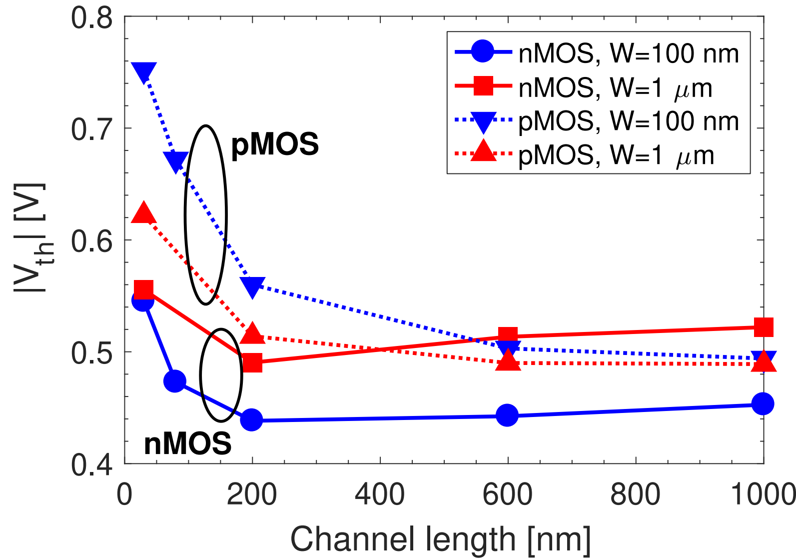


Figure 4.5: The threshold voltage $|V_{th}|$ of fresh MOSFETs under test are plotted as a function of the channel length for different channel width. Measurements are carried out at room temperature in linear region ($|V_{ds}| = 0.1$ V). (After [97])

doping peak in the center of the channel, which increases abruptly the threshold voltage of the short transistors [134]. The rise of the threshold voltage with decreasing channel-length is called Reverse Short Channel Effect (RSCE) [135], and characterizes scaled CMOS technologies with high halo doping concentration.

Figure 4.5 shows the threshold voltage $|V_{th}|$ of nMOSFETs and pMOFETs before the exposure. The $|V_{th}|$ is plotted as a function of the channel-length for transistors with channel-width $W = 100$ nm and 3 μm. The trend of the $|V_{th}|$ vs. L is characterized by an evident RSCE, indicating highly doped halo implantations and low substrate concentration, which cause the increase of the V_{th} in short-channel transistors. The abrupt increase of the V_{th} for $L < 100$ nm suggests that the drain halo starts to overlap the source one when L is reduced below 100 nm. The RSCE is particularly evident in the pMOSFETs with $W = 100$ nm, where the $|V_{th}|$ difference between the longest and the shortest channel devices is ≈ 0.25 V, while in nMOSFETs this $|V_{th}|$ difference is ≈ 0.1 V in nMOSFETs with $W = 100$ nm.

The dependence of V_{th} with transistor width is caused by the gate fringing field in the channel corner edge with the STI. Depending on the transistor type, production process and STI design different effects can arise: the Narrow-Width Effect (NWE) and the Reverse-Narrow-Width Effect (RNWE) [136].

4.1.3 Irradiation conditions and measurements details

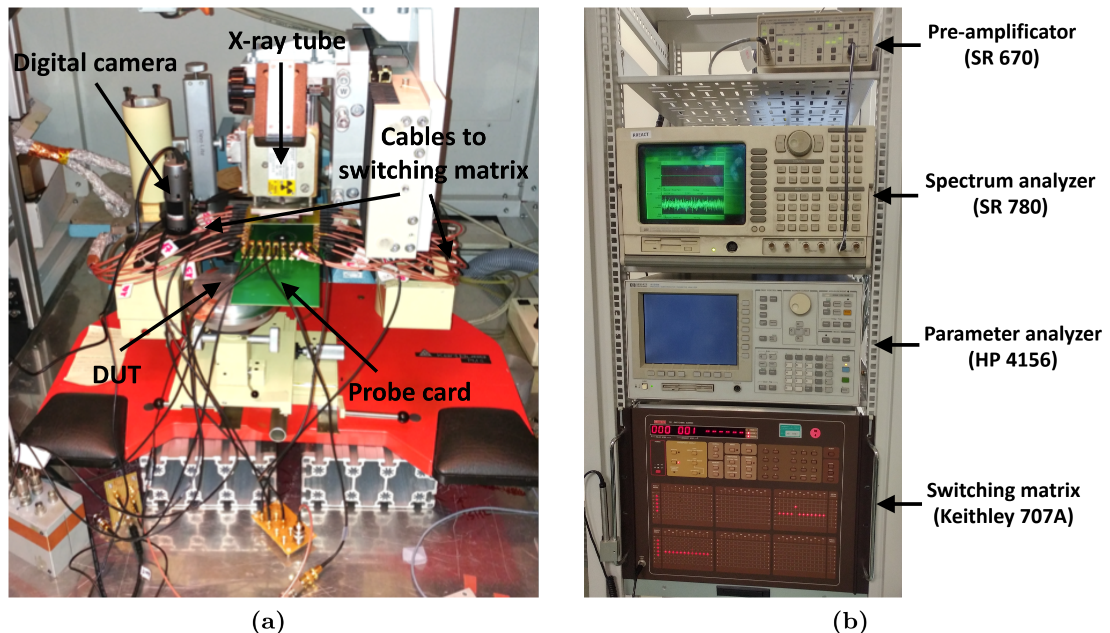
The irradiation tests were performed at the University of Padova using an X-ray irradiator composed by a tungsten tube with peak energy deposition at 10 keV. In order

to reach ultra-high doses up to 1 Grad(SiO_2), the dose rate was set to 5.12 Mrad/h(SiO_2) [100], allowing devices to reach 1 Grad(SiO_2) doses in about 8 days of exposure. Figure 4.6 shows the irradiation setup with probe card station, x-ray tube and instruments used during the evaluation of 28 nm transistors. Immediately after the exposure, annealing tests were carried out by heating up the dies to 100 °C for 24 hours by mean of a controlled heating ceramic resistor. During the irradiation and the annealing, all transistors of the array structure were biased in one of the following configurations: "diode" ($|V_{gs}|$ = 1 V, $|V_{ds}|$ = 1 V), "on" ($|V_{gs}|$ =1 V, $|V_{ds}|$ = 0 V) or "off" ($|V_{gs}|$ = 0 V, $|V_{ds}|$ = 0 V).

The measurements presented in this thesis work were performed on more than 40 samples up to different cumulated dose. At least two different devices of each type were evaluated for all experimental conditions, with typical results shown below. The DC responses of the transistors were measured in the linear region with $|V_{ds}|$ = 0.1 V with a semiconductor parameter analyzer (HP4156). Low frequency $1/f$ noise measurements were carried out at room temperature by the use of a pre-amplifier (SR 570) and a spectrum analyzer (SR 780). The low-frequency noise [137] was measured in a frequency span between 0.5 Hz and 1 kHz at $|V_{ds}|$ = 0.1 V and at several values of $V_{gt} = V_{gs} - V_{th}$.

4.2 Experimental results

In the following section, the TID responses of MOSFETs are reported by measuring the DC static characteristics and extracting the main parameters: maximum drain current



(a) (b)

Figure 4.6: Experimental setup for the evaluation of the TID response of the 28 nm transistors. (a) Probe card station inside the X-ray facility. (b) Instruments used for the measurements of the DC static response and of low frequency $1/f$ noise.

variation (ΔI_{on-lin}), threshold voltage shift (ΔV_{th}), degradation of the transconductance (Δg_m) and subthreshold swing variation (ΔSS). The I_{on-lin} current is defined as the drain-to-source current in linear region ($|V_{ds}| = 0.1$ V) when the channel is in strong inversion at $|V_{gs}| = 1$ V. The threshold voltage V_{th} is extracted by the linear region (ELR) method [138], as the gate voltage axis intercept of the linear extrapolation of the $I_d - V_{gs}$ characteristics at its maximum first derivative point. Nominally identical devices irradiated and annealed under similar conditions show DC characteristics that typically vary by less than ± 10%.

4.2.1 TID Response: $I_d - V_{gs}$

Figure 4.7 reports the $I_d - V_{gs}$ characteristics at $|V_{ds}| = 0.1$ V of nMOSFETs with three different channel sizes: (a) W/L = 100/30 nm, (b) W/L = 100/1000 nm and (c) W/L = 1000/1000 nm. The transistors were irradiated at room temperature up to 1 Grad(SiO_2) and then annealed at 100 °C for 24 hours. Both during the exposure and the annealing, the transistors were biased in the "diode" configuration.

In all nMOSFETs, the leakage current degrades with the dose, with an increase of ≈ 2 order of magnitude after 1 Grad(SiO_2). A rebound [14] of the V_{th} occurs around 100 Mrad(SiO_2). Below 100 Mrad(SiO_2), $|V_{th}|$ decreases with dose, negligible variation is measured in g_m, and very low SS variation is observed. Above 100 Mrad(SiO_2), $|V_{th}|$ shifts back to more positive values, with large g_m and SS degradation. The larger TID sensitivity is found in narrow and long channel tranisistors, while the best TID tolerance is found in the long and large transistor, indicating the influence of the channel dimension to the TID mechanism. The black dash-dotted lines indicate the TID responses of the transistors after 24 hours at 100 °C. After high temperature annealing, the TID response of nMOSFETs recovers almost completely, from $|\Delta I_{on-lin}|$ = -15% at 1 Grad(SiO_2) to $|\Delta I_{on-lin}|$ = -4% after annealing, while pMOSFETs show partial recovery of the DC response, from $|\Delta I_{on-lin}|$ = -80% at 1 Grad(SiO_2) to$|\Delta I_{on-lin}|$= -36% after annealing.

Similarly to Figure 4.7, Figure 4.8 shows the $I_d - V_{gs}$ at $|V_{ds}| = 0.1$ V of pMOSFETs with the three different channel sizes, irradiated and annealed in the "diode" configuration. pMOSFETs show higher TID sensitivity than nMOSFETs. After irradiation to 1 Grad(SiO2), the degradation of the maximum drain current in the narrow and long transistors is -80% in pMOSFETs vs. -15% in nMOSFETs. All tested pMOSFETs exhibit a continuous decrease of the maximum drain current current with cumulated dose, while the threshold voltage shifts to lower values. In pMOSFETs, the influence of the channel dimension is evident and clear. The pMOSFET with long and wide channel (c) reveals the highest TID tolerance, showing a $\Delta|I_{on-lin}|$ variation of -15% at 1 Grad(SiO_2). The worst TID degradation is found in the narrow and long channel transistor (b), which exhibits a $\Delta|I_{on-lin}|$ decrease of -78% at 1 Grad(SiO_2). While the shortest and narrowest pMOSFET (a) has a $\Delta|I_{on-lin}|$ degradation of -40%, which is half of the large and narrow channel transistor. The subthreshold swing (SS) increases slightly with dose; $\Delta SS < 10$

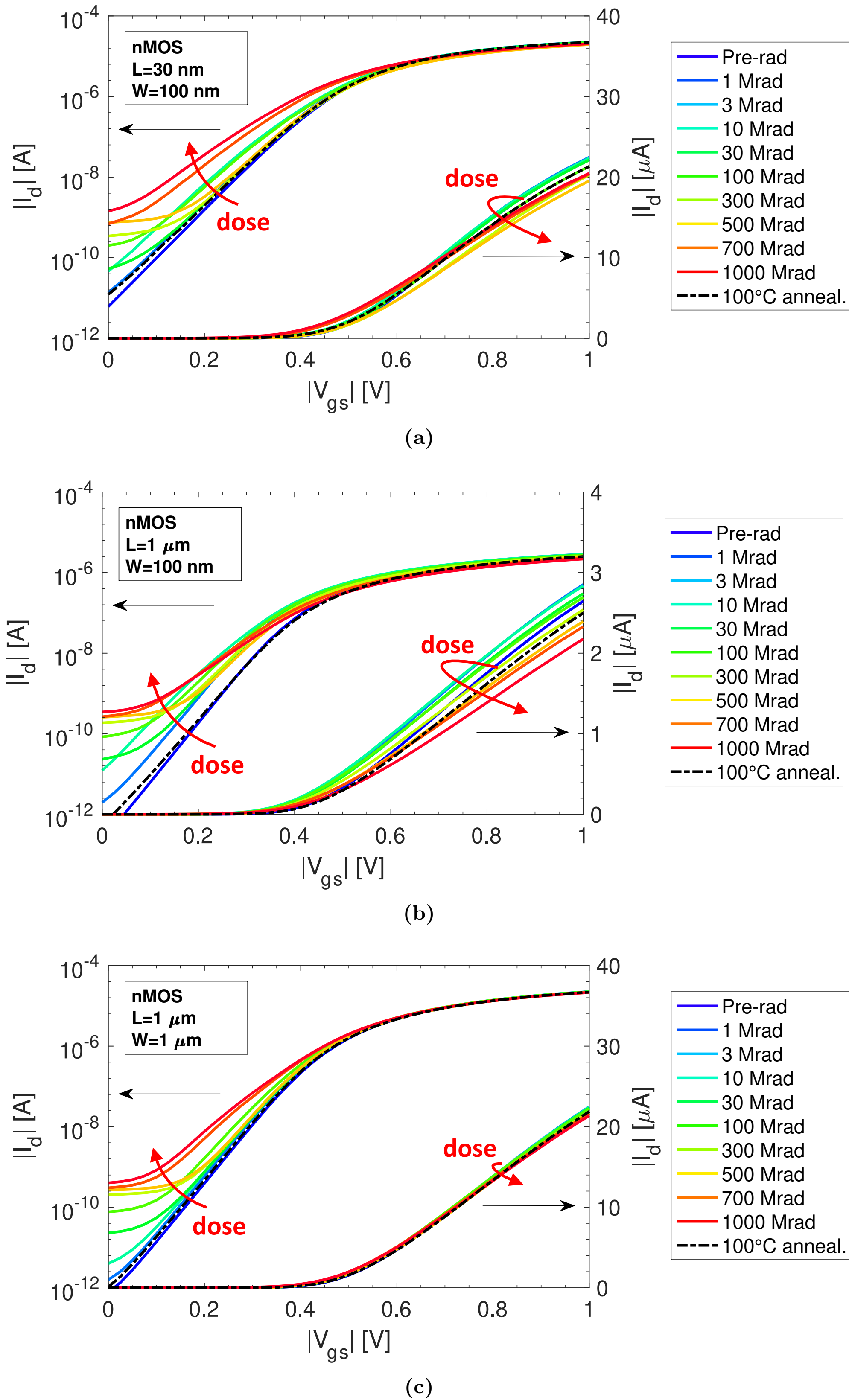


Figure 4.7: Degradation of the $I_d - V_{gs}$ in linear region ($|V_{ds}| = 0.1$ V) of nMOSFETs irradiated at room temperature up to 1 Grad(SiO_2) and then annealed for 24 hours at 100 °C in the "diode" configuration. (a) W = 100 nm, L = 30 nm. (b) W = 100 nm, L = 1000 nm. (c) W = 1000 nm, L = 1000 nm.

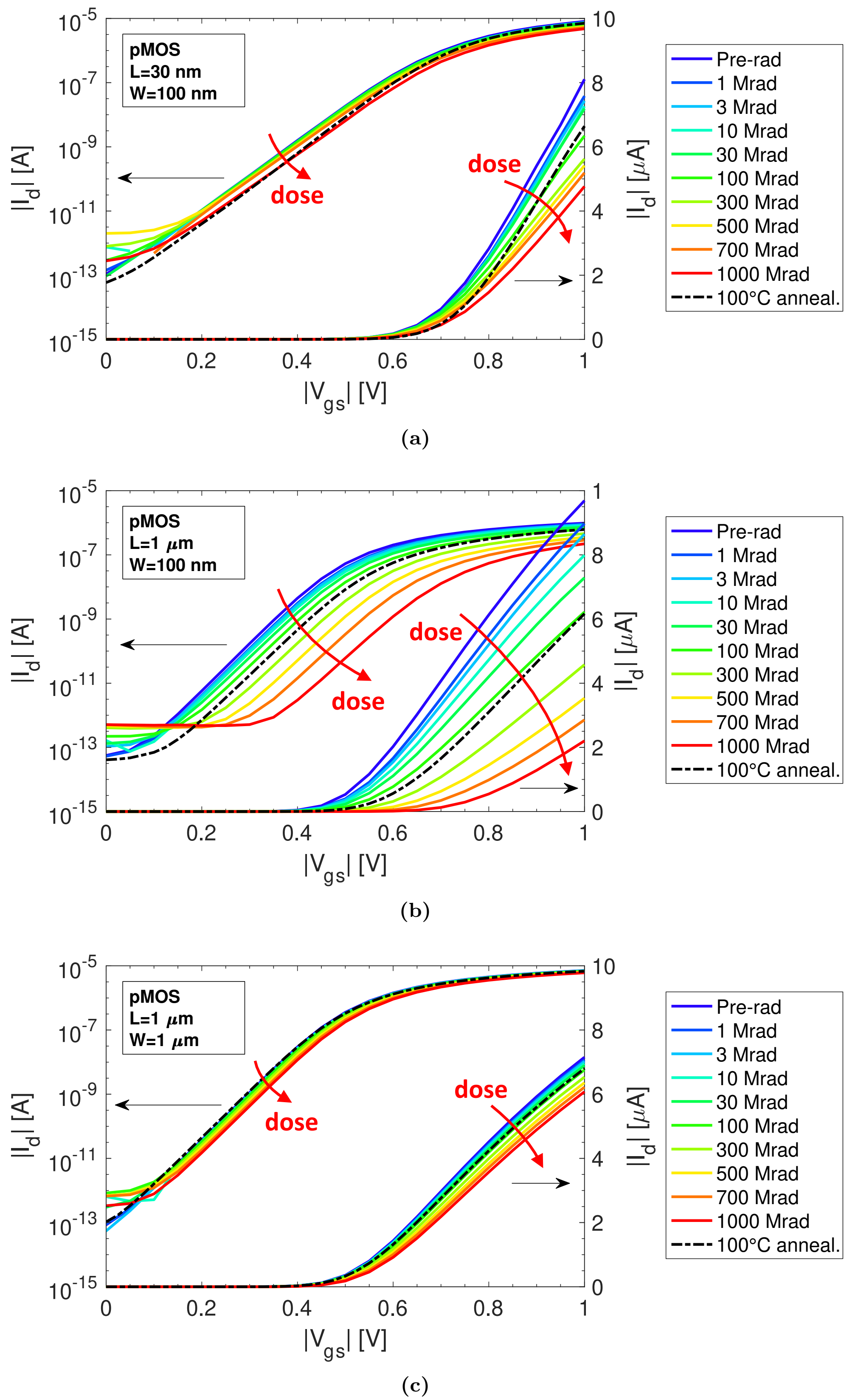


Figure 4.8: Degradation of the $I_d - V_{gs}$ in linear region ($|V_{ds}| = 0.1$ V) of pMOSFETs irradiated at room temperature up to 1 Grad(SiO_2) and then annealed for 24 hours at 100 °C in the "diode" configuration. (a) $W = 100$ nm, $L = 30$ nm. (b) $W = 100$ nm, $L = 1000$ nm. (c) $W = 1000$ nm, $L = 1000$ nm.

mV/dec after 1 Grad(SiO_2). The off-state drain leakage current of all pMOSFETs slightly increases, about one order of magnitude after 1 Grad(SiO_2). After high temperature annealing, transistors with narrow channel show a visible recovery.

The influence of the channel dimension on TID response is extremely evident in the pMOSFETs. Figure 4.9 summarizes the main parameter degradation of pMOSFETs of different gate areas. Similarly to Figure 4.8, the transistors were irradiated at room temperature up to 1 Grad(SiO_2) and then annealed at 100 °C for 24 hours in the "diode" configuration. The degradation of the $\Delta|I_{on-lin}|$ evidences that the narrowest transistors (W = 100 nm) are the most sensitive to TID. Narrow and long transistors with $L \geq$

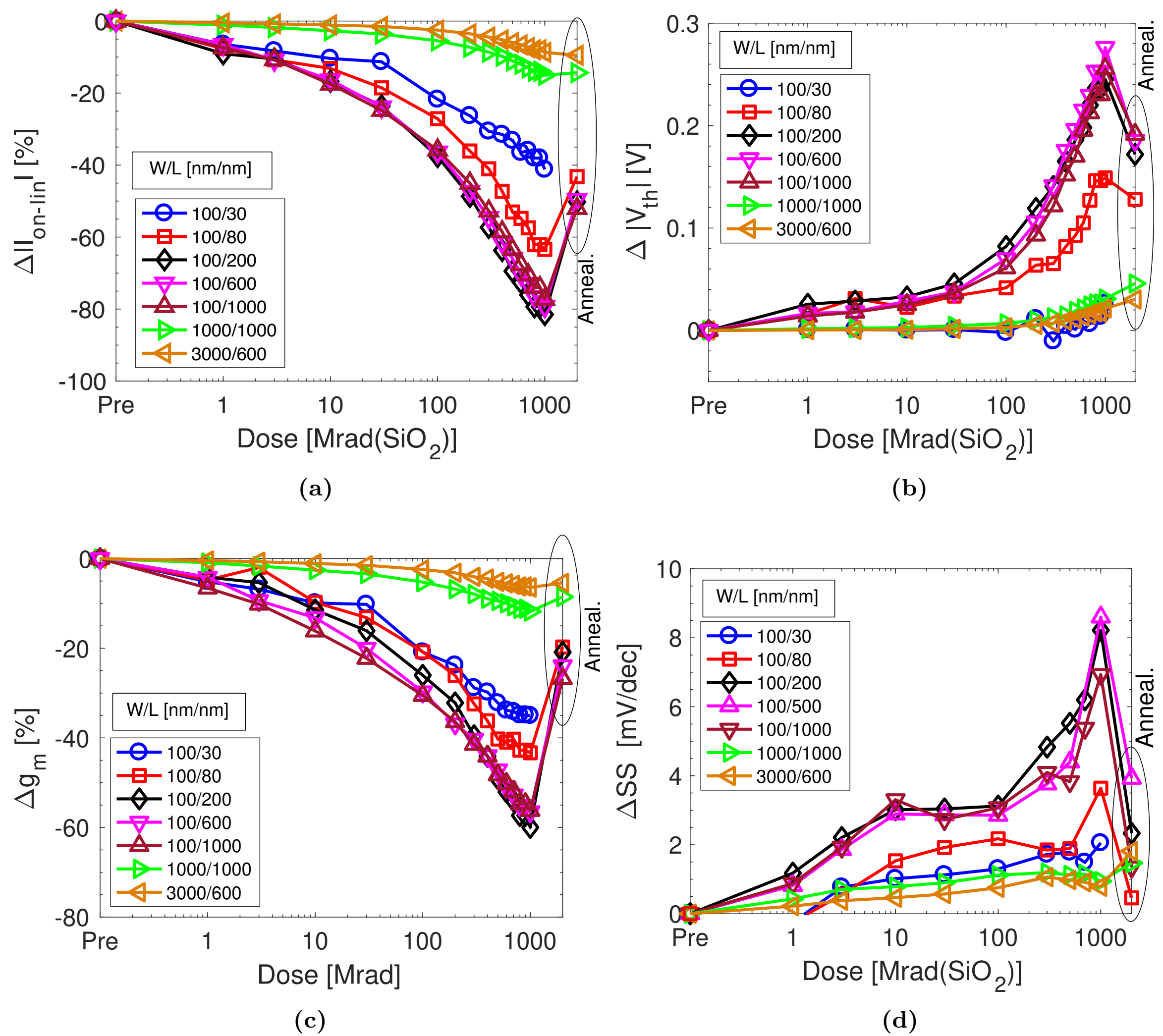


Figure 4.9: Summary of the main parameters degradation of pMOSFETs irradiated up to 1 Grad(SiO2) and then annealed at 100 °C for 24 hours in the "diode" configuration. All measurements were carried out in linear region ($|V_{ds}|$ = 0.1 V) and at room temperature. (a) Maximum drain current variation $\Delta|I_{on-lin}|$. (b) Threshold voltage $\Delta|V_{th}|$. (c) Transconductance Δg_m. (d) Subthreshold swing ΔSS. (From [97])

200 nm degrade almost equally, $\Delta|I_{on-lin}|$ is about -78% after 1 Grad(SiO_2). Instead, narrow and short transistors with $L < 100$ nm exhibit a channel-length dependence, with the shortest transistor (L = 30 nm) having the smallest degradation. Focusing on this channel length dependence of narrow transistors, after 1 Grad(SiO_2), pMOSFETs with L = 30 nm, 80 nm and 100 nm exhibit respectively a $\Delta|I_{on-lin}|$ degradation of -40%, -63% and -82%. The length-dependent effect is visible at high doses, since 10 Mrad(SiO_2), and is dominant at ultra-high doses over 100 Mrad(SiO_2).

As visible in Figure 4.9(b) and Figure 4.9(c), the decrease of the maximum drain current I_{on-lin} is caused by a degradation of both V_{th} and g_m. The channel-length dependence of the degradation of $\Delta|I_{on-lin}|$ is visible also on the Δg_m and in particular on the $\Delta|V_{th}|$. The pMOSFETs exhibit a $\Delta|V_{th}|$ degradation of -20 mV, -140 mV and -280 mV respectively on transistors with L = 30 nm, 80 nm and 200 nm. Finally, Figure 4.9(d) shows the variation of the subthreshold slope as a function of the dose. The ΔSS is almost negligible, less than 9 mV/dec after an exposure of 1 Grad(SiO_2). The worst case is the narrowest channel transistors with ΔSS of about 9 mV/dec, whereas all other channel geometries exhibit a ΔSS of less than 2 mV/dec.

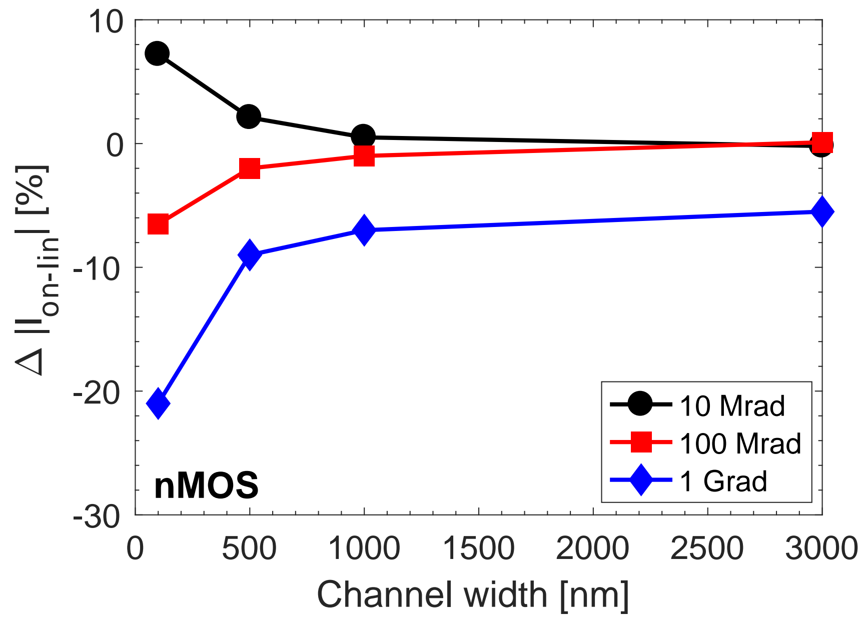
As the TID degradations in transistors with $L \geq 200$ nm are similar to each other, in the next pages I mainly focus on the results of three representative geometries: W/L = 100 nm/30 nm (narrowest and shortest), W/L = 100 nm/1 μm (narrowest and longest) and W/L = 1 μm/1 μm (largest and longest).

4.2.2 Channel-width dependence

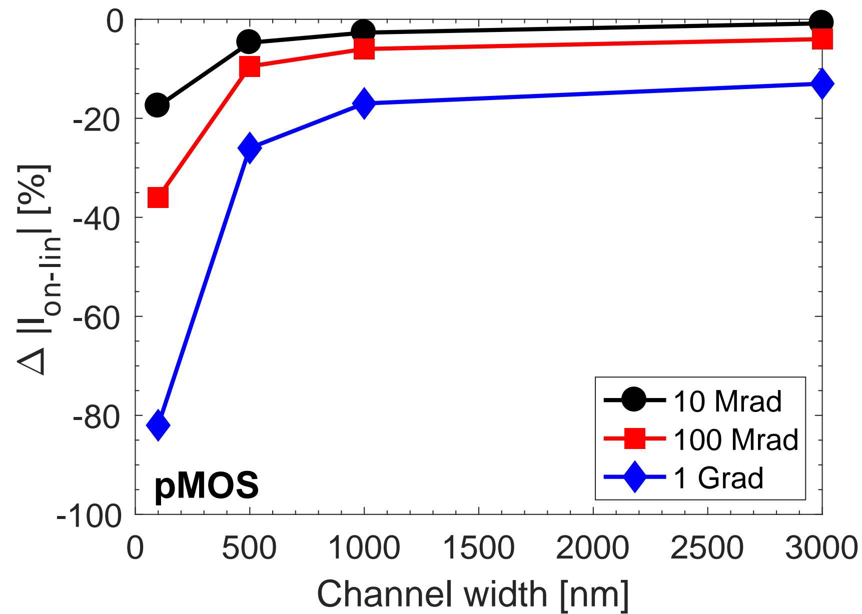
Figure 4.10 shows the TID degradation of the $\Delta|I_{on-lin}|$ as a function of channel width in MOSFETs. Only long channel transistors are taken into account to minimize short channel effects with L = 1 μm (except one device with W/L = 3000 nm/500 nm). Transistors of different widths were measured up to 1 Grad(SiO_2) in the “diode” condition. The I_{on-lin} current is defined as the drain current at $|V_{gs}|$ = 1 V and $|V_{ds}|$ = 0.1 V.

In Figure 4.10(a), nMOSFETs irradiated at 10 Mrad(SiO_2) show positive and channel-width dependent shift of the $\Delta|I_{on-lin}|$, due to positive charge buildup in the STI [37]. The worst-case $\Delta|I_{on-lin}|$ is found in the narrowest transistor with an increase of 9%, while the $\Delta|I_{on-lin}|$ of the largest device is negligible, < 1%, indicating no effects related to the gate oxide. At 100 Mrad(SiO_2), the $\Delta|I_{on-lin}|$ for the narrowest nMOSFET decreases to -6%, while the degradation of the largest nMOSFET changes less than 1%. The negligible effect on the largest nMOSFET still suggests negligible charge buildup in the gate oxide, while the negative $\Delta|I_{on-lin}|$ values for the narrowest device suggest negative charge buildup in the interface traps of the STI sidewalls. At 1 Grad(SiO_2), the degradation is strongly channel-width dependent. The largest nMOSFET exhibits a negative $\Delta|I_{on-lin}|$ degradation, indicating interface trap buildup along the gate oxide and/or Si channel interface.

In Figure 4.10(b), pMOSFETs are much more sensitive to TID effects than nMOS-



(a)



(b)

Figure 4.10: Degradation of the drain current as a function of channel width W in MOSFETs irradiated up to 1 Grad(SiO_2) in the "diode" bias condition. Transistors have long channel with L = 1 μm (except W/L = 3000 nm/500 nm). The I_on current is defined as the drain current when $|V_{gs}|$ = 1 V and $|V_{ds}|$ = 0.1 V. (a) nMOSFETs and (b) pMOSFETs. (From [129])

FETs. $\Delta|I_{on-lin}|$ values for pMOSFETs are negative for all devices at all doses, consistent with the previous works [88, 89]. The narrowest pMOSFET exhibits the worst-case TID response due to positive charge buildup in the STI [37], while the degradation of the largest transistors is negligible. The increased degradation of largest pMOSFET with dose suggests positive charge buildup in the gate oxide and/or Si channel interface.

4.2.3 Channel-length dependence

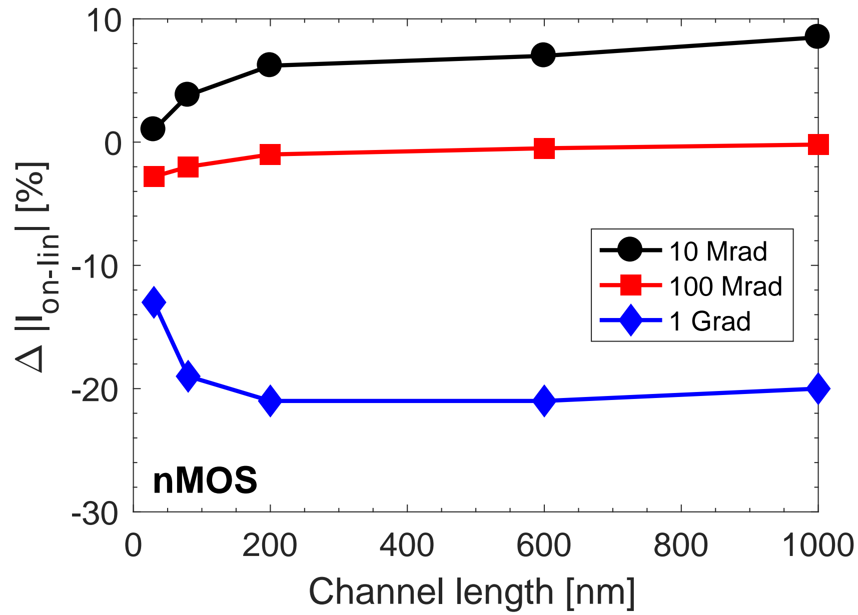
The channel-length dependence is one of the most interesting result. Figure 4.11 shows the degradation of the $\Delta|I_{on-lin}|$ as a function of channel length for MOSFETs with narrow channel $W = 100$ nm irradiated up to 1 Grad(SiO_2) in the "diode" condition. In nMOSFETs irradiated up to 10 Mrad(SiO_2), $\Delta|I_{on-lin}|$ is channel length dependent. The worst-case is found in the longest device, with $\Delta|I_{on-lin}| = 9\%$, while the degradation of the shortest device is negligible, <1%. At 100 Mrad(SiO_2), $\Delta|I_{on-lin}|$ of the nMOSFETs decreases by less than 2%, regardless of channel length. Above 100 Mrad(SiO_2), the degradation of the $\Delta|I_{on-lin}|$ is negative and shows a clear channel-length dependence. The shortest transistor exhibits the most tolerant response, with $\Delta|I_{on-lin}| = 12\%$, vs. $\Delta|I_{on-lin}| = 20\%$ of the longest channel device.

In pMOSFETs, $\Delta|I_{on-lin}|$ is always negative and channel-length dependent, which increases with increasing dose. Short channel pMOSFETs exhibit higher TID tolerance than longer channel devices. At 1 Grad(SiO_2), the $\Delta|I_{on-lin}|$ of the shortest transistor degrades of -40%, while the longest channel transistor degrades of -80%. However, p-channel transistors with $L > 100$ nm do not show any channel-length dependence, showing a constant degradation around -80%. This short-channel effect is visible only in narrow channel transistors at both very high doses (10 Mrad(SiO_2)) and ultra-high doses (> 100 rad(SiO_2)) and will soon be related to the influence of halo implantations, as explained in the next pages.

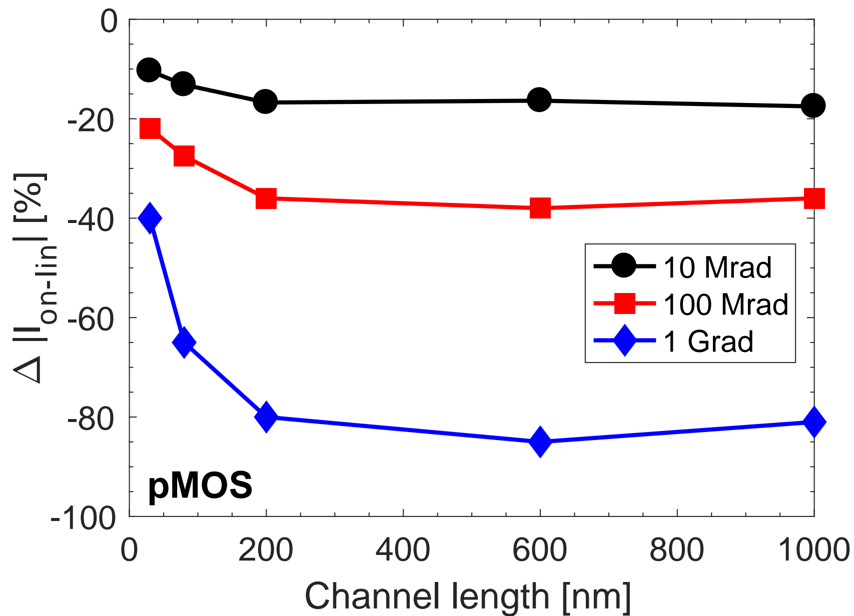
4.2.4 DC response: nMOSFETs vs. pMOSFETs

Figure 4.12 shows the radiation-induced degradation of the main DC parameters: (a) threshold voltage, (b) transconductance, and (c) leakage current. All devices were irradiated up to 1 Grad(SiO_2) and annealed for 24 h at 100 °C in the "diode" condition. In agreement with the values of I_{on-lin} in Figures 4.10 and 4.11, the TID parametric shifts in both nMOSFETs and pMOSFETs depend on channel width and channel length.

In nMOSFETs irradiated up to 100 Mrad(SiO_2), the worst-case V_{th} shift is found in the narrowest and longest transistor, which shows a decrease of $|V_{th}|$ due to positive charge buildup in the STI. The degradation of g_m is less than 5% for all nMOSFETs. Leakage current increases with increasing dose, due to the activation of the parasitic transistor close to the STI sidewalls [37]. The channel-length dependence of the I_{off} current is similar to trends shown in Figure 4.11. Shorter-channel transistors exhibit lower degradation of



(a)



(b)

Figure 4.11: Degradation of the drain current as a function of channel length L in MOSFETs irradiated up to 1 Grad(SiO_2) in the "diode" bias condition. Transistors have narrow channel with W = 100 nm. The I_{on-lin} current is defined as the drain current when $|V_{gs}|$ = 1 V and $|V_{ds}|$ = 0.1 V. (a) nMOSFETs and (b) pMOSFETs. (From [129])

I_{off} than longer devices, with I_{off} ratios of 2 x10^3 vs. 2 x10^4, respectively. Above 100 Mrad(SiO_2), $|V_{th}|$ turns around and increases significantly, leading to a positive $\Delta|V_{th}|$ shift when the dose approaches 1 Grad(SiO_2). The increase of V_{th}, combined with the significant decrease of the gm at doses > 100 Mrad(SiO_2), indicate generation of interface traps in the gate oxide and/or in the STI sidewalls. Consistent with this interpretation, the insensitivity of g_m with channel length and the rebound of V_{th} at doses larger than 100 Mrad(SiO_2) are also more consistent with interface-trap buildup than electrostatic effects of charge trapping in STI.

In pMOSFETs, the channel length and channel width dependence of the TID degradation are also clearly evident. The highest sensitivity is found in the narrowest and longest channel devices, which show $\Delta|V_{th}| = 250$ mV vs. $\Delta|V_{th}| = 40$ mV of narrowest and shortest transistor at 1 Grad(SiO_2). The large degradation of the g_m in narrow transistors is mostly due to the reduction of the effective width of the transistors. As shown in [37], positive trapped charge in the STI can deplete the lateral region of the transistors, reducing its effective channel width. Finally, the increase of the leakage current in pMOSFETs, about one order of magnitude at 1 Grad(SiO_2), is significantly less than for nMOSFETs. The increase of the leakage current in pMOSFETs is most likely due to the peripheral drain to substrate junction leakage current. This current is associated with surface generation at the intersection of the depletion region and the STI sidewalls, where a high density of interface traps is located [139].

4.2.5 Bias condition dependence

Figure 4.13 shows how the TID response depends on bias. The V_{th} shift, the g_m degradation, and the subthreshold swing SS are plotted as a function of dose for pMOSFETs and nMOSFETs with $W/L = 100$ nm/1 μm. Transistors were irradiated up to 500 Mrad(SiO_2) in "off", "on" and "diode" conditions. The "off" condition shows the highest TID tolerance in both nMOSFETs and pMOSFETs. At 500 Mrad(SiO_2), pMOSFETs irradiated in the "off" condition show ΔV_{th} of 90 mV vs. 180 mV for devices irradiated in the "diode" condition. The difference between the "diode" and "on"-biased transistors is negligible, showing the insensitivity of the TID response of these devices to lateral drain-to-source electric fields. The degradation of the transconductance of nMOSFETs is significant after 100 Mrad(SiO_2) due to increased carrier scattering induced by the buildup of interface traps along the gate oxide and the STI sidewalls. The SS variation in nMOSFETs increases abruptly after 100 Mrad(SiO_2), indicating large generation of interface traps. "OFF"-biased nMOSFETs show lower increases of SS. In pMOSFETs, the variation of the SS is nearly insensitive to the bias condition, and is small compared to the nMOSFETs. At a dose of 1 Grad(SiO_2), ΔSS is 7 mV/dec for "on"-biased pMOSFETs and 38 mV/dec for "on"-biased nMOSFETs. In contrast, changes in V_{th} and g_m depend on the bias condition, with highest TID tolerance observed for "off"-biased pMOSFETs. In case of the pMOSFETs, the g_m degradation is not due to carrier scattering, but it is

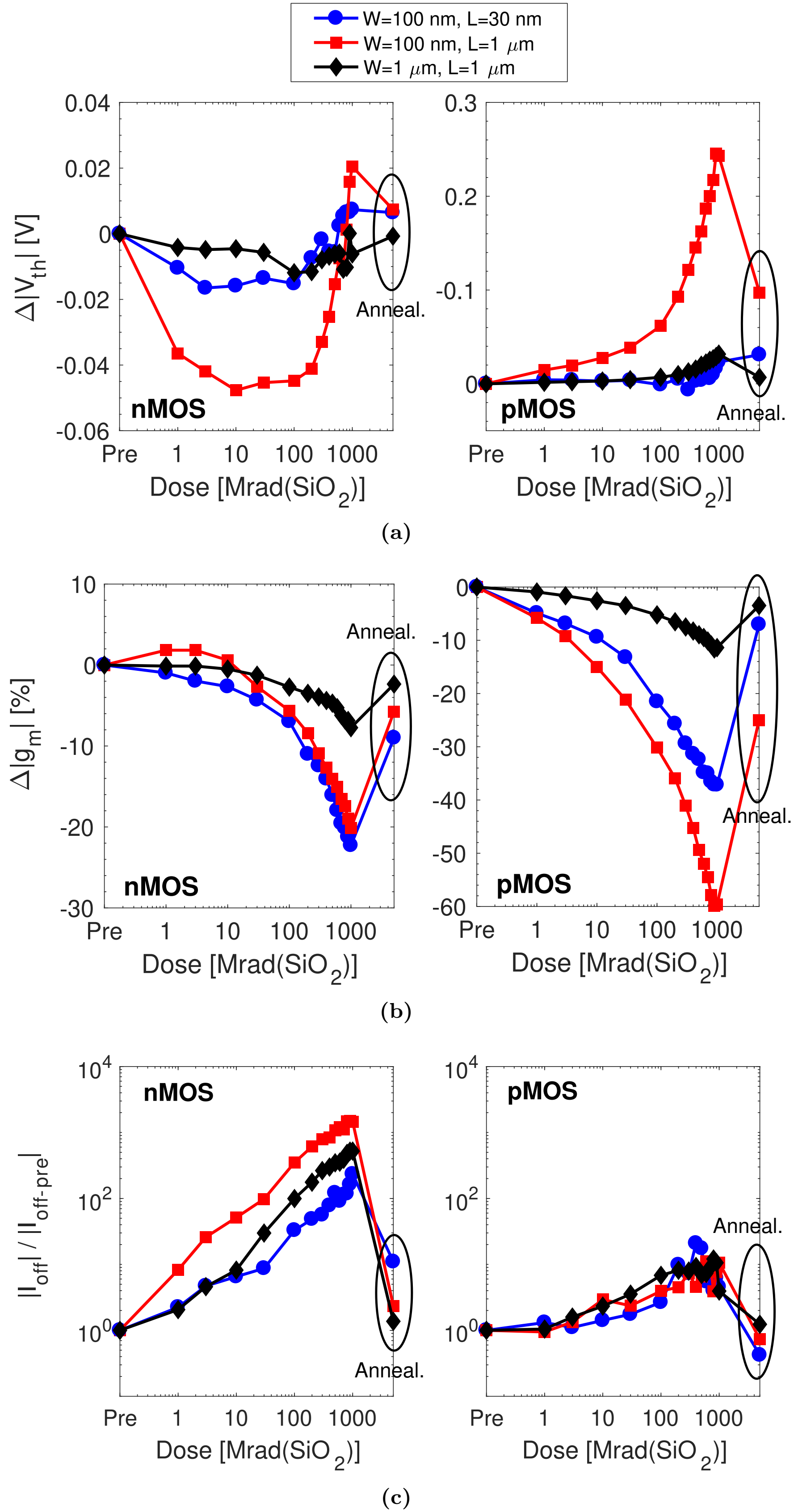


Figure 4.12: TID sensitivity to gate length and width. The plots show the main DC parametric shifts at RT in nMOSFETs and pMOSFETs of different channel widths and lengths in the linear region ($|V_{ds}| = 0.1$ V). All transistors were irradiated up to 1 Grad(SiO_2) and then annealed for 24 h at 100 °C in the "diode"-bias condition. (a) Threshold voltage $\Delta|V_{th}|$, (b) transconductance $\Delta|g_m|$, and (c) leakage current increase $|I_{off}|/|I_{off-pre}|$. (From [129])

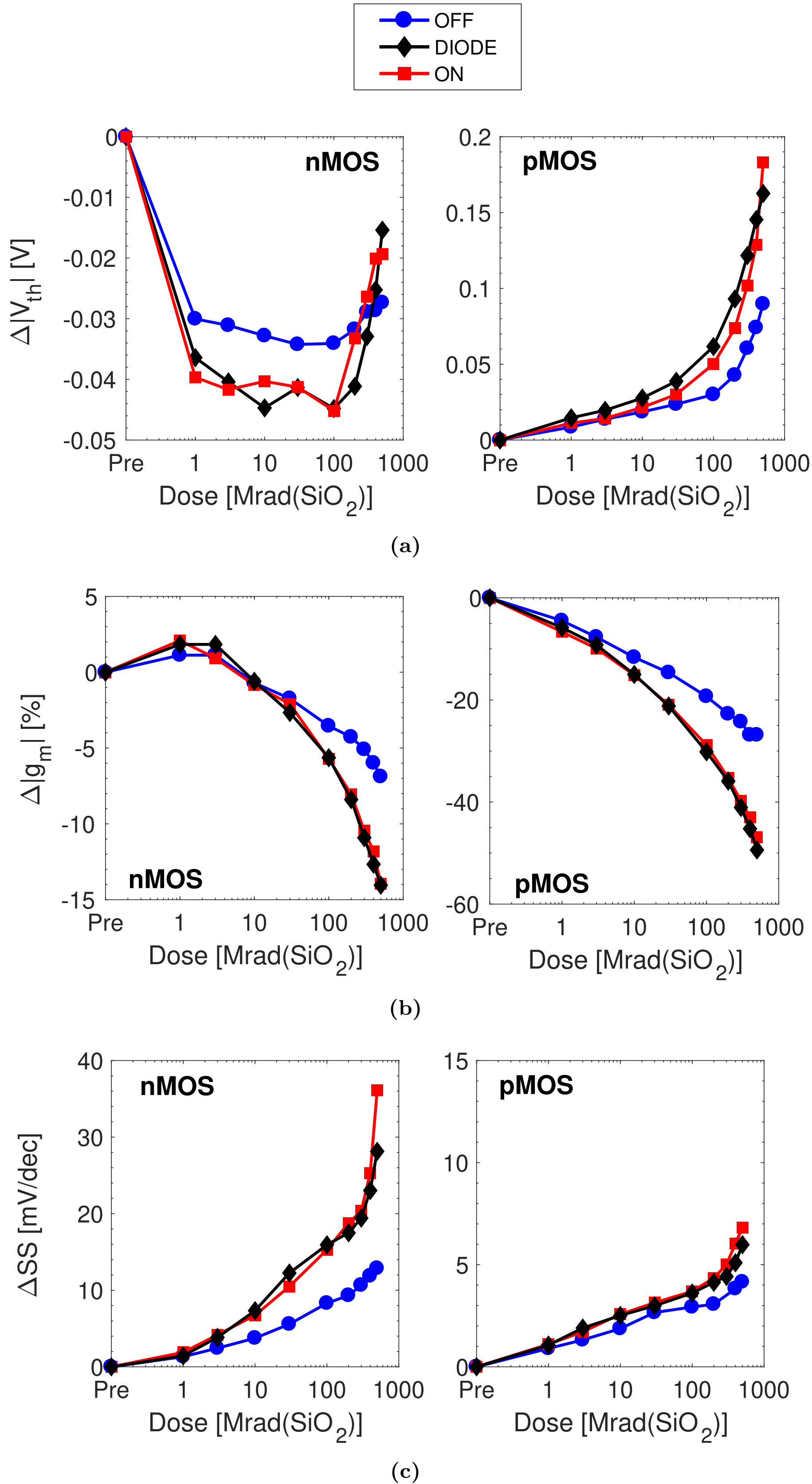


Figure 4.13: TID sensitivity to bias condition during irradiation. The plots show the main DC parametric shifts at RT in nMOSFETs and pMOSFETs in the linear region ($|V_{ds}| = 0.1$ V). All transistors were irradiated up to 1 Grad(SiO_2) in the "off", "diode", or "on" condition. (a) Threshold voltage $\Delta|V_{th}|$, (b) transconductance $\Delta|g_m|$, and (c) subthrehosld swing increase ΔSS. (From [129])

mainly due to the reduction of the effective channel width, induced by the trapped positive charges in the STI.

4.2.6 High temperature annealing

Figure 4.14 reports the degradation of the I_on during the exposure up to 500 Mrad(SiO_2) and during the 24 hours of annealing at 100 °C in the "diode" bias mode. The first and last measurements reported in the annealing plot were carried out at room temperature, whereas the others in the red span were carried out at 100 °C. The large difference between the first and the second points in the annealing plot is mainly related to the effects of high temperature, which generally causes a reduction of the threshold voltage and of the carrier mobility.

The annealing evolution is very fast during the first hour at high temperature. After 24 hours at 100 °C, narrow transistors recovers part of the degradation caused by the exposure. The highest recovery of the response is found in the narrowest (W = 100 nm) and long ($L >$ 100 nm) transistors, which exhibit a $\Delta|I_{on-lin}|$ of about -70% after the exposure and a $\Delta|I_{on-lin}|$ of -40% after the annealing. The $\Delta|I_{on-lin}|$ of shortest channel transistors degrade of -30% after the exposure and recovers up to -18% after the annealing. In these devices the recovery of the TID response is mainly due to a large improvement of the transconductance. On the contrary, the TID response of wide transistors after the annealing is almost negligible or, even, of the opposite sign, such as for pMOSFETs with W = 3000 nm.

4.2.7 Low frequency noise measurements

Low-frequency noise was measured at several gate voltages to evaluate the noise response of the MOSFETs, and to obtain insights into the TID induced defects [62, 140]. The low-frequency noise of MOS devices has been shown to be due primarily to carrier number fluctuations [137, 141, 142].

Low frequency noise measurements is carried out in current by monitoring the fluctuations of the drain current at several gate voltages. In order to limit the electromagnetic interference of the external environment, like the 50 Hz of the power line, the drain bias is applied by a pre-amplifier working with batteries. Figure 4.15 shows the low-frequency noise of nMOSFETs and pMOSFETs at several values of L, before exposure, at 30 Mrad(SiO_2), and at 500 Mrad(SiO_2). The noise magnitude scales inversely with gate area [137], and increases with dose. nMOSFETs exhibit the typical $\sim 1/f$ low frequency dependence, regardless of V_{gs}, dose and channel dimension. pMOSFETs show larger noise magnitudes than nMOSFETs, and $S_{id} - f$ slopes depend on channel length, consistent with trends in radiation-induced charge trapping. The noise magnitudes and frequency dependences for the shortest-channel transistors vary from device to device. Most shorter-channel devices exhibit Lorentzian noise, characterized by $\sim 1/f^2$ slopes at low frequency

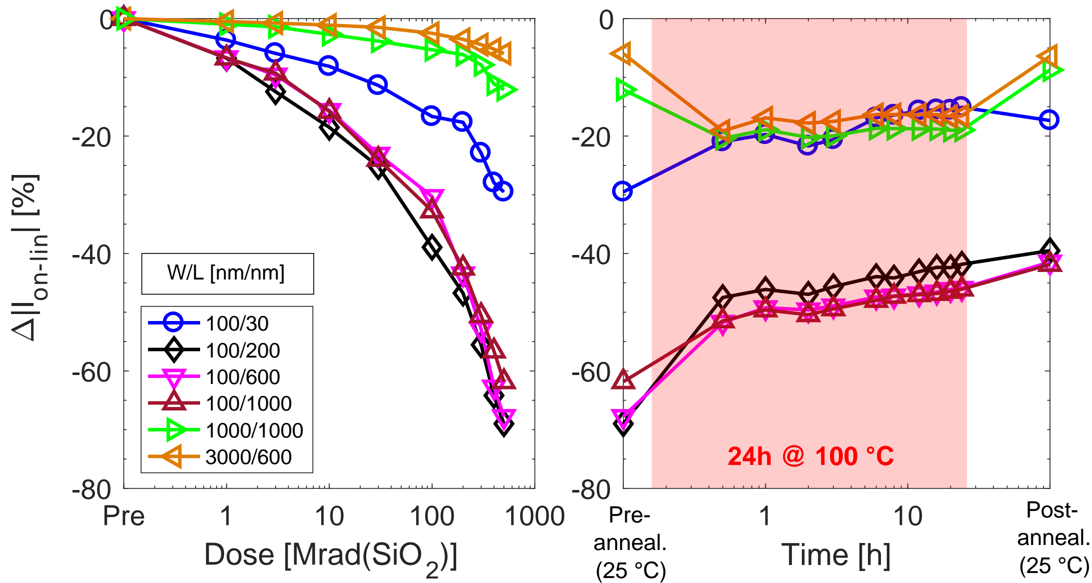
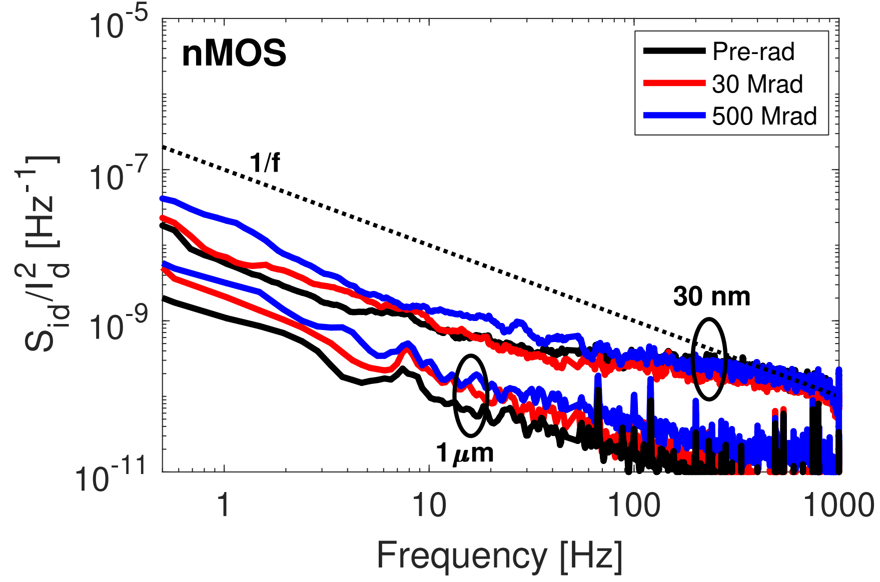


Figure 4.14: The I_{on-lin} variation ($|V_{ds}| = 0.1$ V) of pMOSFETs irradiated up to 500 Mrad(SiO_2) and then annealed at 100 °C for 24 hours in the "diode" configuration. Measurements in the red space were carried out at 100 °C, whereas the others in the white background were carried out at room temperature. (From [97])

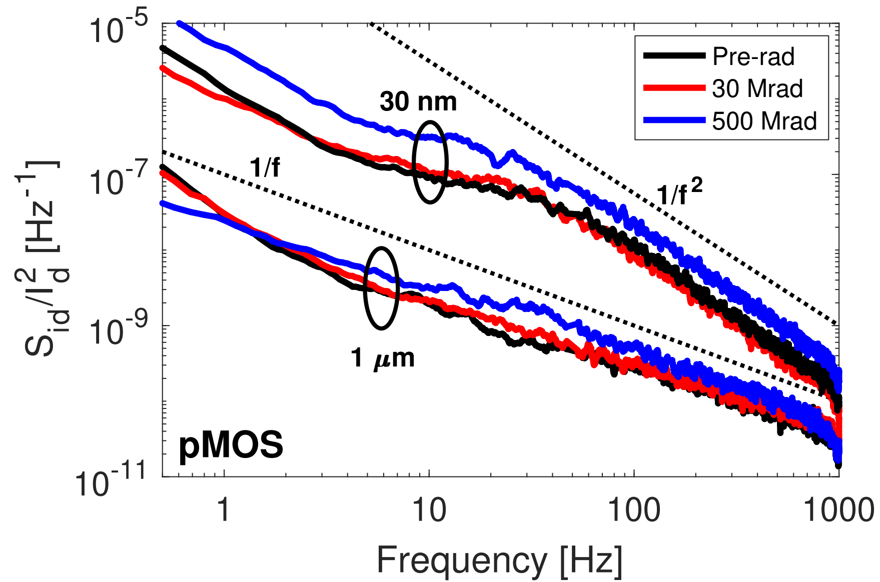
[62, 140], as shown in Figure 4.15, while longer-channel pMOSFETs are typically characterized by $\sim 1/f$ noise.

Figure 4.16 plots the drain current as a function of time, normalized by the average (I_{d0}) for the shortest channel pMOSFETs of Figure 4.15(a). Consistent with the multiple Lorentzian shapes, the signal in time is dominated by Random Telegraph Noise (RTN) [140, 143]. RTN is visible only in the small devices, due to the alternate capture and emission of carriers at individual defect sites, which generate discrete switching in the device channel resistance. Figure 4.16 shows two dominating traps with different amplitudes and emission/capture times. These are related to Lorentzian power spectra with corner frequencies $f_c < 1$ Hz and $f_c \approx 30$ Hz. At 500 Mrad(SiO_2), amplitudes of the RTN slightly increase, and the emission/capture time of the slower defect decreases from $\tau_c/\tau_e = 3.2$ s/2.1 s before irradiation to $\tau_c/\tau_e = 1.3$ s/1.1 s after exposure. In contrast, the faster defect has similar emission/capture times, $\tau_c/\tau_e = 18$ ms/120 ms before the irradiation and $\tau_c/\tau_e = 14$ ms/113 ms after the exposure. Hence, irradiation only modestly affects these pre-existing defects in the as-processed devices.

The measurement of low frequency noise at several gate voltages can provide further details about the effective defect-energy distribution [137, 141, 142, 144]. The low



(a)



(b)

Figure 4.15: Low-frequency noise magnitude for nMOSFETs and pMOSFETs with W = 100 nm irradiated up to 500 Mrad(SiO_2) in the "diode"-bias condition. The noise is measured at $|V_{ds}|$ = 0.1 V and $|V_{gs}|$ = 0.9 V at room temperature. (a) nMOSFETs and (b) pMOSFETs. (From [129])

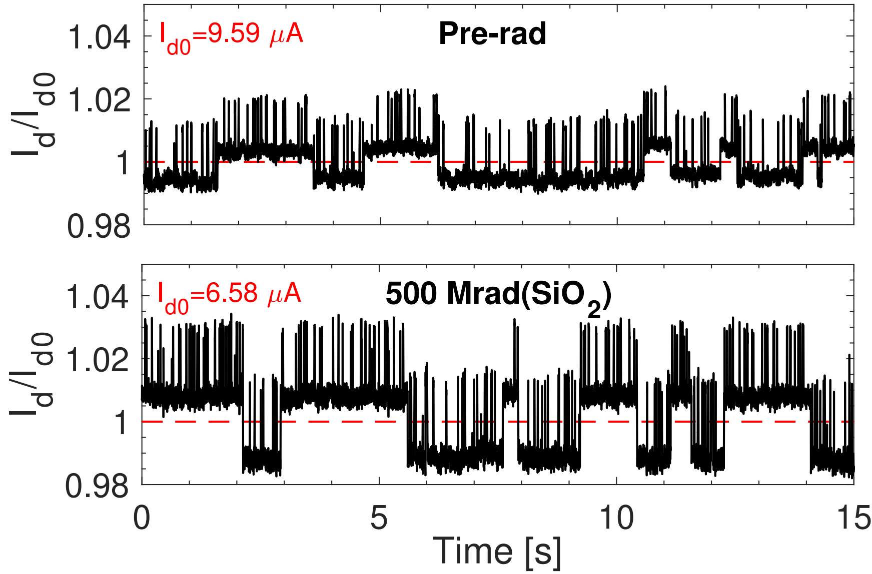


Figure 4.16: Normalized random telegraph noise before irradiation and after 500 Mrad(SiO_2) for the smallest pMOSFET with $L = 30$ nm shown in Figure 4.15. (From [129])

frequency noise can be paramaterized through the expression [142, 144, 145]:

$$S_{vd}(f, V_{ds}, V_{gs}) = \frac{(KV_{ds}^2)}{(f^\alpha(|V_{gs} - V_{th}|)^\beta)} \tag{4.1}$$

where S_{vd} is the excess drain-voltage noise power spectral density, f is the frequency, K is the normalized noise magnitude, $\alpha = \delta \log S_{vd}/\delta \log f$, and $\beta = \delta \log S_{vd}/\delta \log |V_{gs} - V_{th}|$. In the linear region of device response, the drain-voltage noise power spectral density S_{vd} is related to the drain-current noise power spectral density S_{id} by the relation:

$$S_{vd} = R_{ch}^2 S_{id} = \frac{V_{ds}^2}{{I_d s}^2} S_{id} \tag{4.2}$$

So Eq. (4.3) can be rewritten equivalently as:

$$\frac{S_{id}}{I_{ds}^2}(f, V_{gs}) = \frac{K}{f^\alpha(|V_{gs} - V_{th}|)^\beta} \tag{4.3}$$

When traps contributing to noise are distributed uniformly in space throughout the gate oxide and in energy in the Si band gap, the low frequency noise is characterized by $\alpha \approx 1$ and $\beta \approx 2$ [62, 137, 141, 142]. In contrast, significant deviations from $\alpha \approx 1$ and $\beta \approx 2$ are evidence of non-uniform defect-energy distributions in energy and/or space [137, 142, 144, 145]. When contact noise and noise due to series resistance are negligible compared to the noise due to number fluctuations in the device channel, and when $\beta < 2$, the distribution of border traps is increasing toward the semiconductor conduction band for nMOSFETs or the valence band for pMOSFETs [142, 144]. Under these same

conditions but for $\beta > 2$, the distribution of border traps is increasing toward midgap [137, 142, 144].

In Figure 4.17 the noise magnitude at $f = 10$ Hz is plotted as a function of $|V_{gs} - V_{th}|$ for the shortest and longest devices, with $W = 100$ nm, irradiated in the "diode" bias condition. The noise magnitude increases with dose. In nMOSFETs the slope ($|\beta|$) of the $S_{vd} - V_{gt}$ curves is $\sim$2, indicating approximately uniformly distributed defects in space and energy at all doses [137]. In pMOSFETs, the increase of the noise magnitude is the highest. The shortest channel transistors are dominated by RTN, but longer-channel transistors exhibit $1/f$ noise with $|\beta| \approx 1$. This suggests that few defects are dominating the noise of the small devices, and that multiple defects are contributing to the noise, with no single defect dominating over others [137]. As often seen in pMOS devices, the defect energy-distribution increases strongly towards the valence band edge [137, 142, 144].

4.3 Discussion

Experimental results at ultra-high doses highlight the high sensitivity of the TID response of these devices to channel width, channel length, and bias conditions.

4.3.1 STI-related effects

The width-dependence of the degradation suggests that the charge trapping in the gate dielectric is not the dominating radiation-induced effect. Consistent with previous results in 65 nm and 28 nm technologies [37, 89, 123, 123], the degradation is larger in narrow transistors, due to enhanced charge buildup in shallow trench insulators (RINCE) [37]. In p-channel MOSFETs, the positive trapped charges in the STI oxide can buildup an electric field capable of depleting the lateral edges of the transistor channel. This reduces the effective channel width, concurrently decreasing the transconductance g_m and increasing the threshold voltage $|V_{th}|$ of the transistor [37]. On the contrary, in nMOSFETs the positive charge buildup in the STI induces a negative V_{th} shift of narrow transistors and inverts the lateral channel regions close to the STI, activating a lateral parasitic transistor and increasing the leakage current I_{off} [37, 38, 98]. Consequently, the width-dependent degradation found in 28 nm pMOSFETs can be related to the STI charge buildup, proving the sensitivity of 28 nm MOSFETs to the RINCE effects.

Moreover, the results show that the worst-case bias conditions are the "diode" and "on" modes, in which the gate-to-bulk voltage is maximized. This is in agreement with the simulations in [87], which demonstrated that the charge trapping generation in the STI oxide rises by increasing the gate-to-bulk electrical field. This result differs from the past literature about TID effects on pMOSFETs [34], where the worst-case bias condition for p-channel MOSFETs was the "off" state. This difference is attributed to the different nature of the radiation-induced damage. Older CMOS devices were usually dominated by the gate oxide charge buildup, which is maximized in the "off" bias condition. On

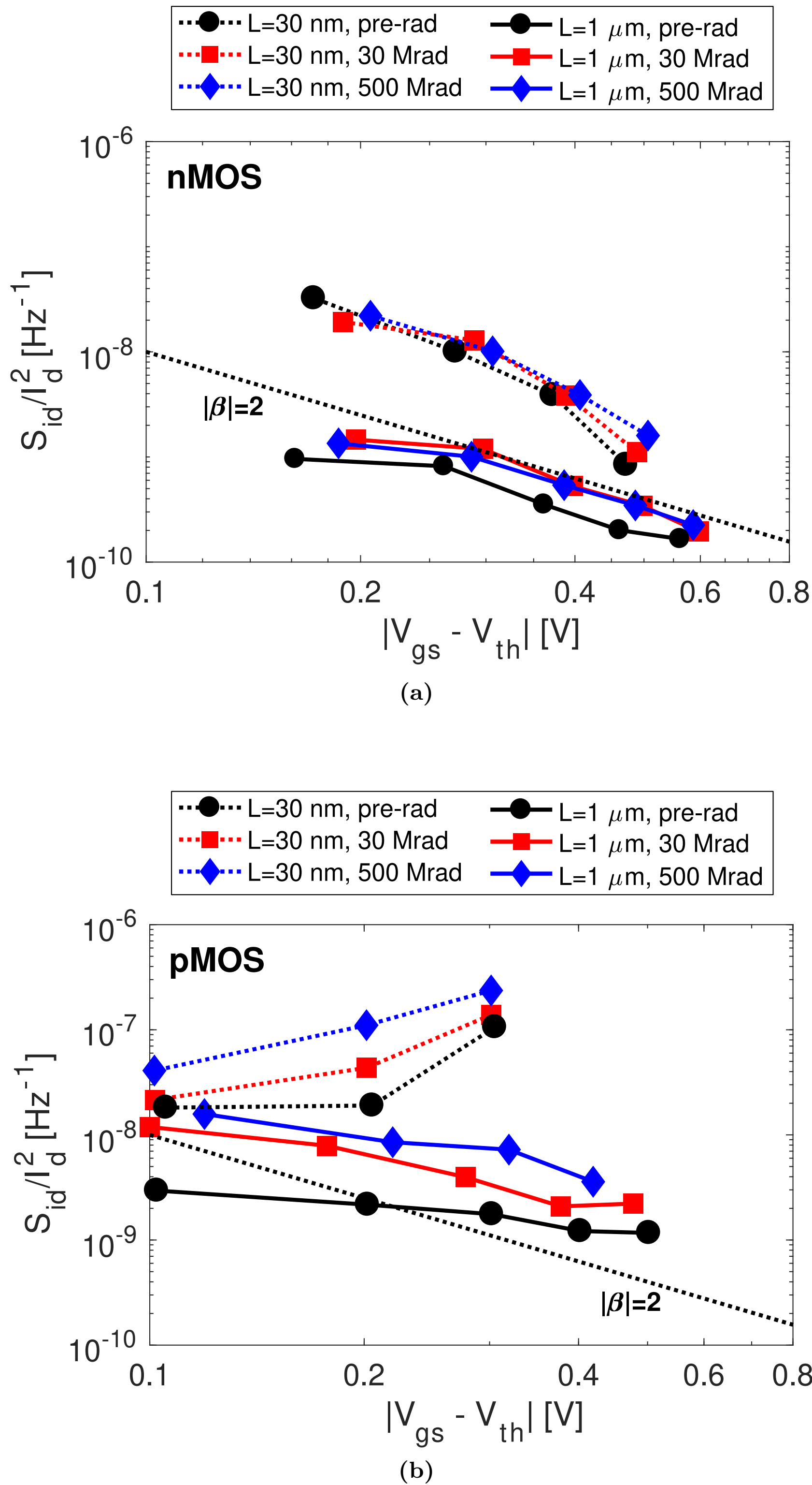


Figure 4.17: $1/f$ noise magnitudes at $f = 10$ Hz vs. $|V_{gs} - V_{th}|$ for (a) nMOSFETs and (b) pMOSFETs with $W = 100$ nm, and $L = 30$ nm or $L = 1$ μm. Transistors were irradiated in the "diode" condition with the noise measured before exposure, at 30 Mrad(SiO_2), and at 500 Mrad(SiO_2), for $|V_{ds}| = 0.1$ V. (From [129])

the contrary, 28 nm pMOSFETs are dominated by STI degradation, which tends to be maximized in the “diode” and “on” conditions.

The observed variation of the off-state leakage current in pMOSFETs is probably due to the peripheral drain to substrate junction leakage current. This current is associated to the surface generation at the intersection of the depletion region and the STI sidewalls, where a high density of interface traps is located [139]. The slight variation of the SS suggests that interface trap generation is limited to the STI sidewalls and does not extend along the gate oxide/bulk interface.

4.3.2 Halo influence

One of the most interesting result of this work is the observed length dependence, particularly evident in the pMOSFETs and opposite to the Radiation-Induced Short-Channel Effect (RISCE) affecting the 65 nm node [90]. The absence of the RISCE in both narrow and large transistors suggests an improvement of the robustness of the spacers in 28 nm technology, but it is not clear if it is due to the high-k materials or to the fabrication process.

One possible explanation of the decreased sensitivity at short gate lengths is the influence of the halo implantations used in modern CMOS processes [146]. Large implant doses and energies in the halo regions can induce a positive $|V_{th}|$ shift, known as V_{th} roll-off [122]. This effect is evident in short channel transistors, where the halo implantations can slightly overlap each other, increasing the average doping of the channel region. By analyzing the pre-rad $|V_{th}|$ of 28 nm pMOSFETs (Figure 4.5), the V_{th} roll-off is visible, and it increases abruptly on the MOSFETs with $L < 100$ nm, indicating that in these transistors the halo implantations increase the overall channel doping.

In recent studies based on device simulation [99, 128], it was demonstrated that the doping of the bulk regions close to the STI edge can drastically modify the TID tolerance of nMOSFETs. In nMOSFETs the positive trapped charges in the STI invert the lateral edges of the transistor channel, forming a parasitic n-channel FET [37]. An increase of the bulk doping in the regions close to the STI edge can lead to an improvement of the TID response of the nMOSFET, as the electrical field generated by the trapped charge in the STI is not able to invert the lateral channel regions. As a consequence, in the short channel nMOSFETs with overlapping halo implantations and high channel doping, the off-state leakage current and the V_{th} degradation decreases.

I think that these results can be applied to the pMOSFETs as well. On pMOSFETs the increase of the bulk doping in the regions close the STI edge can reduce the depleted lateral region responsible for RINCE. Consequently, the width reduction of the irradiated transistor is limited, leading to an increase of the TID tolerance of the pMOSFETs. Figure 4.18 shows a schematic top view of narrow pMOSFETs in the channel region. The green regions represent the STI oxides, filled by the buildup of positive trapped charges. The colour gradient in the yellow regions denotes the halo implantations, which almost overlap

in the short-channel transistors. The dark-blue areas are the regions which do not reach strong inversion due to the influence of the STI trapped charges and are responsible of the reduction of the effective transistor width.

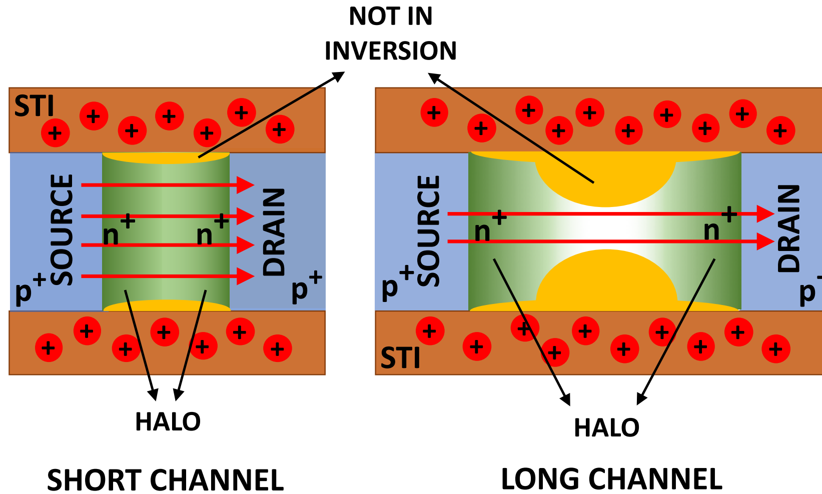


Figure 4.18: Schematic view of the influence of the halo regions on the TID response of short and long channel pMOSFETs. (From [97])

4.3.3 TID degradation mechanisms at high and ultra-high doses

The V_{th} rebound and the large V_{th} degradation at doses > 100 Mrad(SiO_2) visible in the response of nMOSFETs and pMOSFETs (see Figure 4.12) suggests two different mechanisms activated at high and ultra-high doses. Figure 4.19 shows the evolution of the TID degradation mechanisms related to the STI in the 28 nm technology for (a) nMOSFETs and (b) pMOSFETs. The TID-induced effects are analyzed in narrow transistors at high doses ($\sim$ 1-100 Mrad(SiO_2)) and ultra-high doses ($>$ 100 Mrad(SiO_2)). The halo implantations are represented with shaded colours, blue for nMOSFETs and green for pMOSFETs, indicating the doping level of the bulk, while the yellow colour indicates the non-inverted regions (i.e., the depleted regions) of the channel.

At doses of 1-100 Mrad(SiO_2), the large V_{th} shifts of narrow channel devices, the off-state leakage current increase of nMOSFETs, and the large $\Delta|g_m|$ in narrow pMOSFETs show that the TID response in both pMOSFETs and nMOSFETs is dominated by positive oxide-trap charge buildup in STI oxides [37, 39, 86, 123] (see Figure 4.19). The small variation of SS and of I_{on-lin} degradation in the largest device suggests negligible effects related to the gate oxide at doses $<$ 100 Mrad(SiO_2). The improved responses of shorter-channel transistors are related to halo implantations, as explained in the section above.

At ultra-high doses, TID effects differ for nMOSFETs and pMOSFETs. In nMOSFETs, the buildup of positive-charge in the STI increases the I_{off} current [87]. Increases of SS and g_m, along with the rebound of the V_{th}, indicate large generation of interface

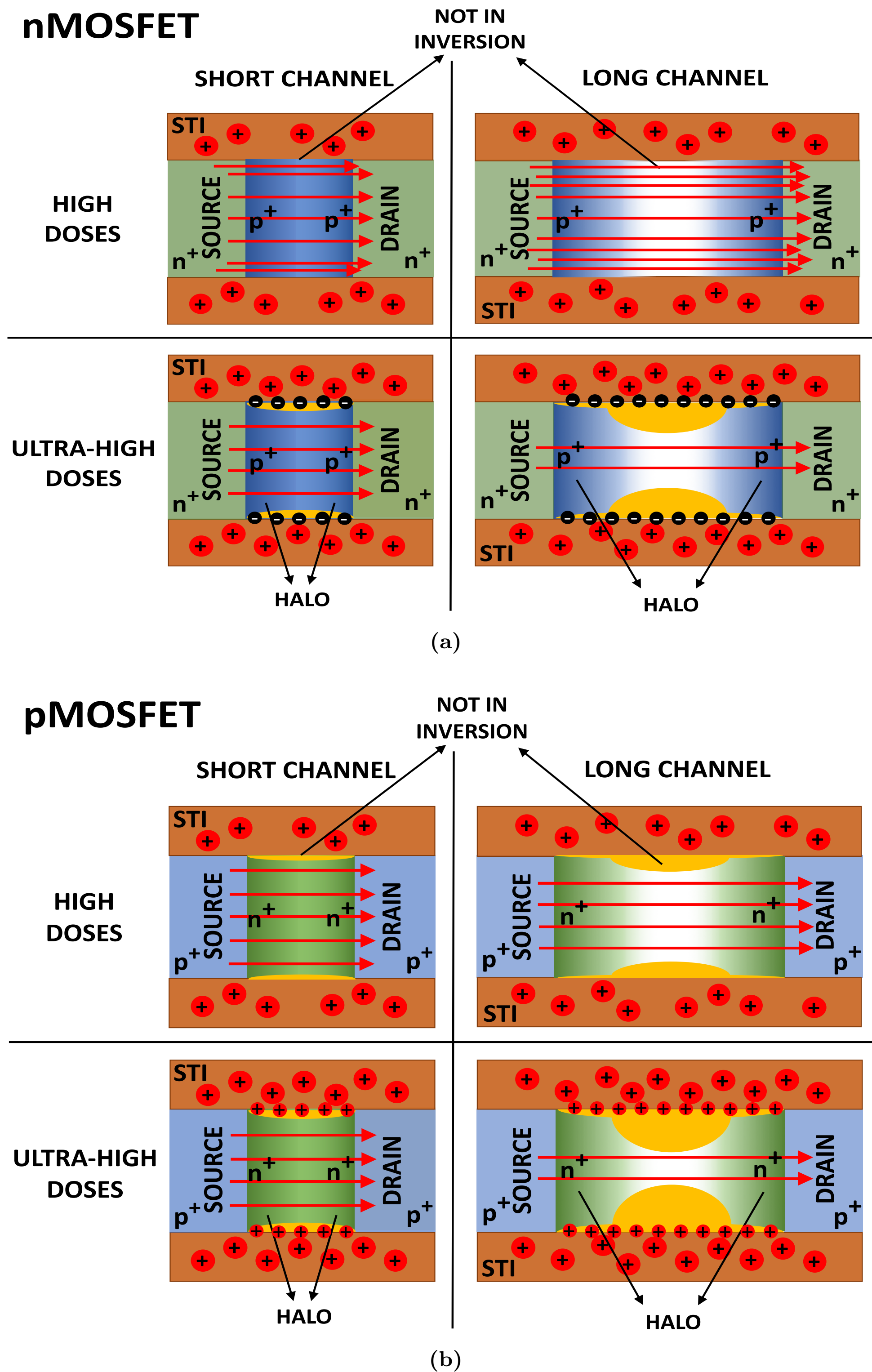


Figure 4.19: Top view of transistors along a horizontal cut-plane immediately below the gate oxide. The evolution of TID mechanisms are shown, related to STI charge buildup and the influence of the halo implantations in narrow MOSFETs biased in the linear region. The TID-induced effects are illustrated in long and short channel devices at high doses ($\sim$ 1-100 Mrad(SiO_2)) and ultra-high doses ($>$ 100 Mrad(SiO_2)). Red arrows represent the amount of flowing current, yellow colours identify the non-inverted regions of the channel, and the shaded colours indicate the bulk doping level, highlighting the halo implantations. (From [129])

traps at the gate dielectric to channel interface [14]. In addition, the results of Fig. 3(a) show a clear channel-width dependence of TID effects at ultra-high doses, with the worst negative $\Delta|I_{on-lin}|$ degradation in narrow devices. This indicates a high density of interface traps in the upper corner between STI and the gate oxide, which can partially deplete the lateral regions close to the STI, reducing the effective channel width and degrading the g_m of narrow nMOSFETs (see Figure 4.19(a)). In pMOSFETs at doses of 1-100 Mrad(SiO_2), the strong channel-width dependence and degradation of the g_m of narrow pMOSFETs indicate continuous positive charge buildup in the STI, most likely accompanied by interface-trap generation along the STI sidewalls. In the nMOSFETs, the high degradation in "on" and "diode" bias conditions is associated with the large generation of interface traps along the gate oxide and along the corner of the STI. This result is in agreement with a model where the interface trap activation is due to electric field-driven drift of H^+ ions; the electric field favors the drift the H_+ ions from the oxides to the SiO_2/Si interfaces. In both pMOSFETs and nMOSFETs, "0V"-biased transistors exhibit the least TID degradation due to enhanced electron-hole recombination in the STI at lower electric fields [147].

4.4 TCAD simulation on halo influence

In this paragraph, the experimental results are compared with Technology Computer-Aided Design (TCAD) Sentaurus simulations. As the the highest degradation is found in the pMOSFETs, only the 28 nm pMOSFETs are simulated. I have designed the simulations structure by adopting a 3D structure with halo implantations and STI. Simulations presented in this work aim to support the interpretation of the length dependence of TID effects and its relation to the halo implantations. The radiation damage is simulated by inserting a volumetric concentration of fixed positive charges in the STI oxides, allowing to study the TID effects during the irradiation.

4.4.1 Simulation approach and goals

The manufacturer does not provide any information about the fabrication process, such as doping concentrations and materials used into the production of the 28 nm transistors. For this reason, the simulated device structure was designed on the basis of publicly available information and agreement with the experimental characterization of the prerad devices. For example, the high-k gate dielectric thickness was estimated by the gate capacitance of a p-channel varactor. Supposing a thickness of the SiO_2 layer of about 0.7 nm, the thickness of the HfO_2 layer results 2 nm.

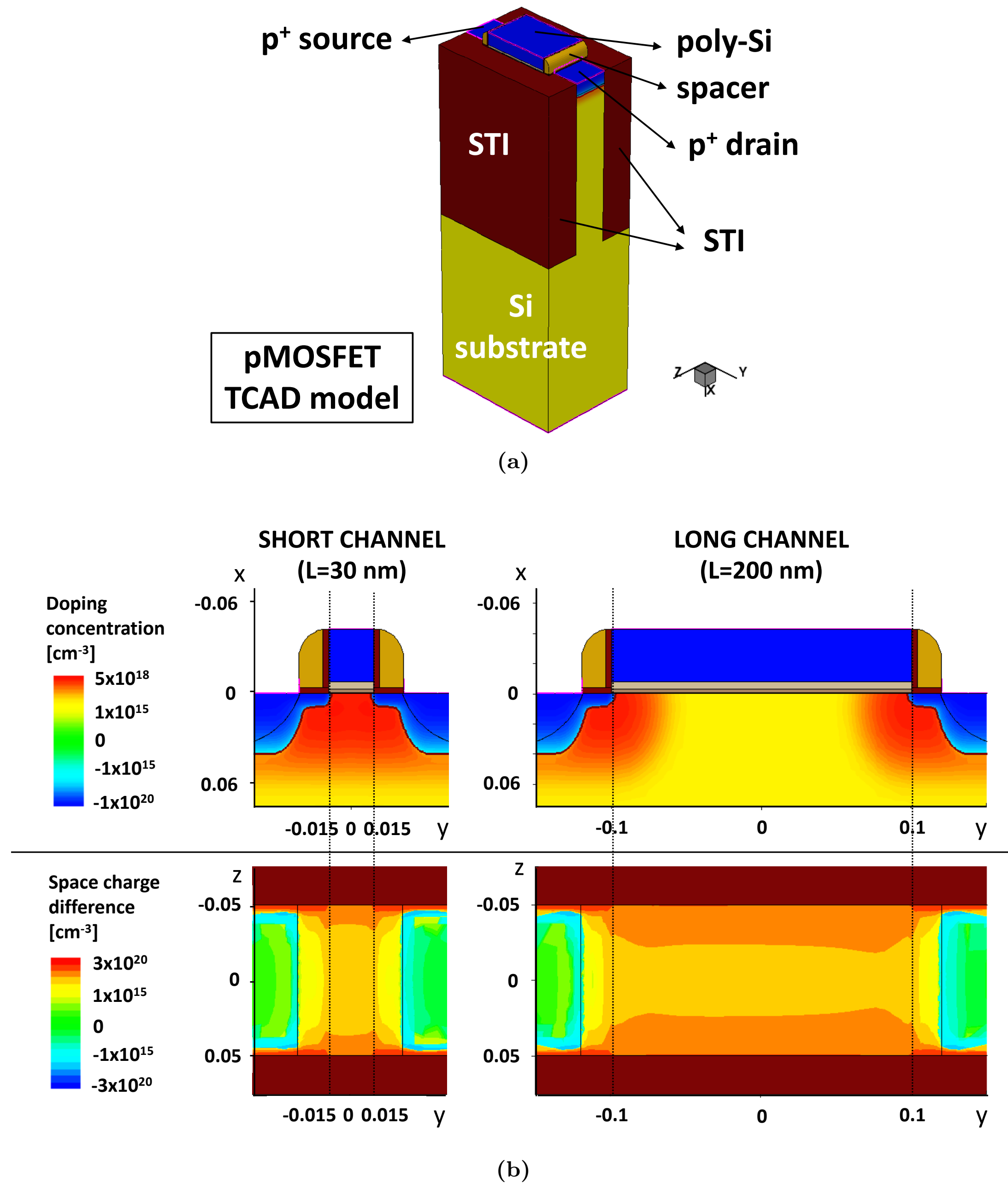


Figure 4.20: The 3D TCAD simulations of the 28 nm pMOSFETs. (a) The simulation are based on a 3D structure, implementing STI and halo regions. (b) In the first row, a cut plane at $z = 0$ μm shows the doping concentrations in short and long channel pMOSFETs. In the second row, cut plane at $x = 2$ nm shows the delta space charge density, calculated as the difference of the space charge density between pre-rad and irradiated devices in short and long channel pMOSFETs. (From [97])

4.4.2 Bulk doping influence

Figure 4.20(a) shows the simulated 3D structure of a pMOSFET with L = 200 nm. In the top part of Figure 4.20(b), a cut plane at $z = 0$ μm shows the doping concentration in the short channel and long channel pMOSFETs. The highly doped regions in red colour identify the halo implantations, which almost overlap each other in the short channel transistor with L = 30 nm. In the bottom part of Figure 4.20(b), the plots have been obtained at a horizontal cut plane at x = 0.002 μm, which is 2 nm beyond the SiO_2/Si interface. The transistors are simulated in linear region with $|V_{ds}|$ = 0.1 V and $|V_{gs}|$ = 1 V. The plots report the concentration difference of the space charges between a fresh device and an irradiated device. The irradiated device is simulated by inserting a uniform volumetric density of positive charges Q_{STI} = 3 x10^{18} cm^{-3} in the STI, equal to 8 x10^{12} cm^{-2} along the STI sidewalls, which is comparable to the charge densities of other previous works [128].

The decrease of the space charge regions close to the STI is larger in the long-channel pMOSFET than in the short-channel one. The smooth increase of the space charge difference visible close to y = -0.1 μm and y = 0.1 μm is due to the higher doping of halos. In the short channel transistor, the high doping of the halos reduces the space charge degradation along the entire channel. Simulations confirm that the degradation of the carrier concentration due to the STI fixed charges is reduced in short-channel transistors,

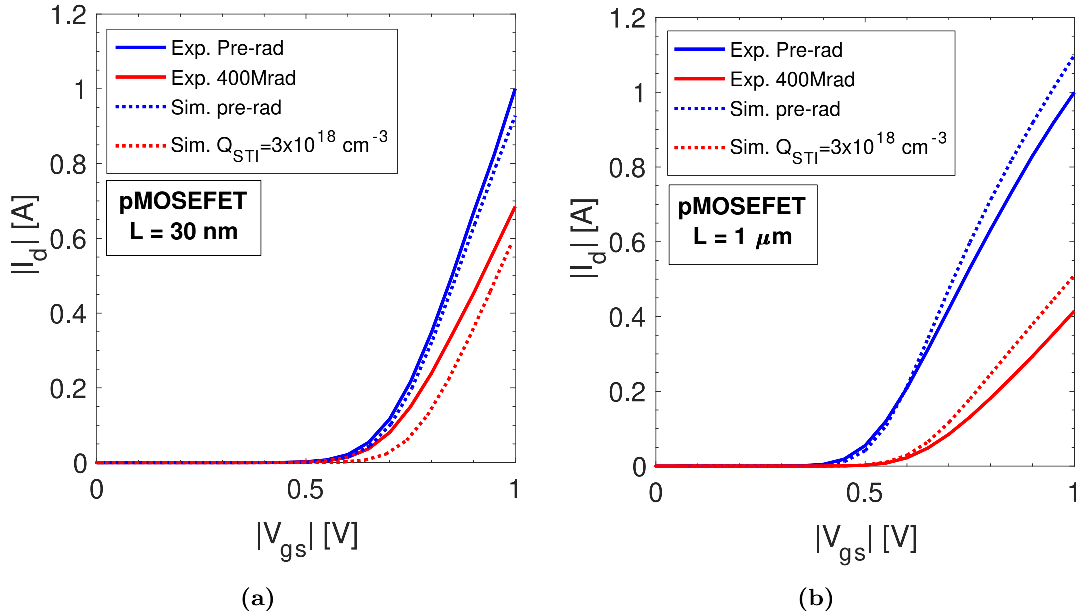


Figure 4.21: The simulated DC characteristics are compared to experimental measurements for $|V_{ds}|$ = 0.1 V before and after the exposure for pMOSFETs with W = 100 nm. (a) L = 30 nm and (b) L = 1 μm. Irradiated devices are simulated by inserting a uniform density of positive charges Q_{STI} = 3 x10^{18} cm^{-3} in the STI. (After [97])

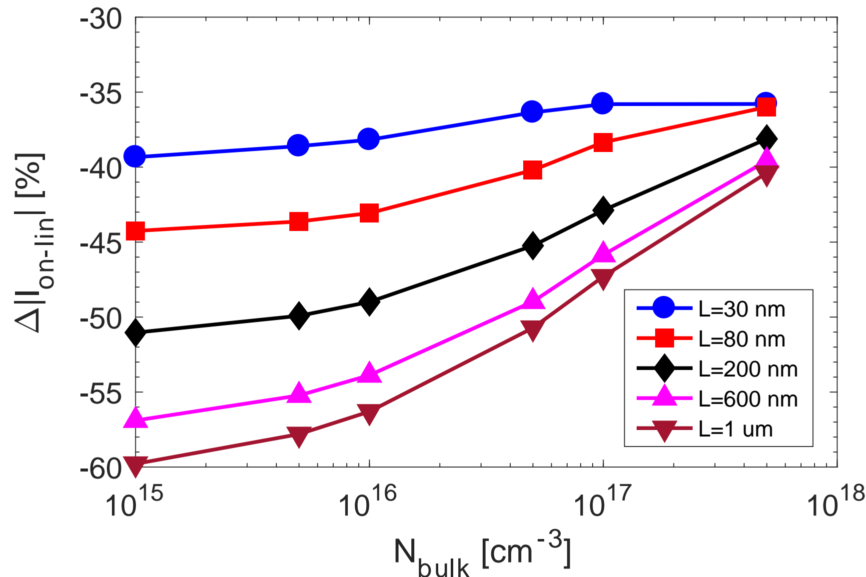


Figure 4.22: The degradation of the maximum drain current I_{on-lin} in linear region ($|V_{ds}|$ = 0.1 V) is simulated by TCAD. Irradiated devices are simulated by inserting a uniform density of positive charges (Q_{STI} = 3 x10^{18} cm^{-3}) in the STI. The $\Delta|I_{on-lin}|$ is plotted as a function of the bulk doping for different channel length transistors, while the doping of halo implantations is constant ($N_{halo-peak}$ = 3.2 x10^{18} cm^{-3}). (From [97])

where the channel doping is dominated by the high concentration of the halo implants.

Figure 4.21 compares the simulated $I_d - V_{gs}$ with the experimental values for the shortest and longest pMOSFETs with W = 100 nm. In the simulations, the fixed charge in the STI causes a degradation of the V_{th} and of the g_m, which is comparable to the experimental measurements.

Figure 4.22 shows the simulated degradation of the I_{on-lin} in pMOSFETs with different channel lengths at several bulk doping concentrations. The irradiated transistor is simulated by inserting a volumetric uniform density of positive charges of 3 x10^{18} cm^{-3} in the STI. Only the bulk doping is varied, whereas halo implantations are constant with $N_{halo-peak}$ = 3.2 x10^{18} cm^{-3}.

This plot clearly evidences the influence of the bulk doping on the transistor TID response. The TID effects in long channel transistors decrease by increasing the doping of the bulk. The pMOSFET with L = 1 μm exhibits a degradation of -60% when the bulk is doped at 10^{15} cm^{-3} and decreases to -40% when the bulk concentration is raised to 5 x10^{18} cm^{-3}. On the contrary, the TID degradation of short channel transistors is almost insensitive to the bulk doping concentration. At 10^{15} cm^{-3}, the $\Delta|I_{on-lin}|$ of pMOSFET with L = 30 nm is -39% and slightly decreases to -36% at 5 x10^{18} cm^{-3}.

This demonstrates that the increase of the bulk concentration improves the TID radiation response. In short channel transistors, the insensitivity of the TID response

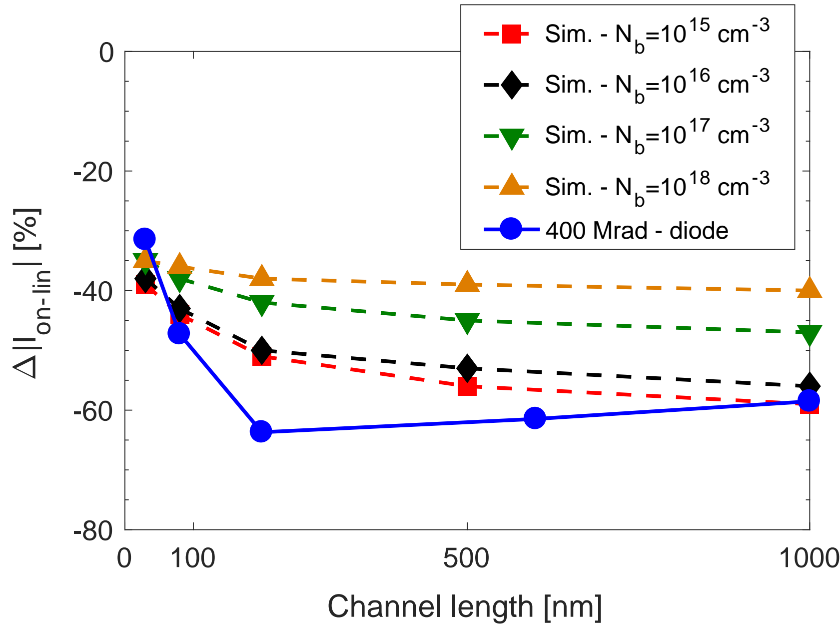


Figure 4.23: The experimental degradation of maximum drain current I_{on-lin} in linear region ($|V_{ds}| = 0.1$ V) at 400 Mrad(SiO_2) in the "diode" bias configuration is compared to simulations at different channel lengths. Irradiated devices are simulated by inserting a uniform density of positive charges ($Q_{STI} = 3$ x10^{18} cm^{-3}) in the STI. Simulations are carried out for different bulk concentrations, while the doping of halo implants is constant ($N_{halo-peak} = 3.2$ x10^{18} cm^{-3}). (From [97])

with bulk doping is due to the high doping of the halo implantations, which increase the overall concentration along the entire channel, independently from the bulk concentration.

Finally, Figure 4.23 evidences the channel-length dependence of the TID in simulations and experimental measurements. The plot compares the experimental and simulated $\Delta|I_{on-lin}|$ degradation as a function of the channel length. The simulated curves are obtained similarly to Figure 4.22. Here, the channel-length dependence of the $\Delta|I_{on-lin}|$ is clearly visible in the simulations and follows the experimental trend. The not perfect match between simulations and experimental values can be due to the differences in the STI edge profile, in the STI corner rounding, in the position and quantity of trapped charges. Moreover, when the bulk doping N_{bulk} is increased, the channel-length dependence is reduced and it disappears at $N_{bulk} \approx 10^{18}$ cm^{-3}, which is comparable to the peak doping of the halos $N_{halo-peak} = 3.2$ x10^{18} cm^{-3}.

In conclusion, TCAD simulations highlight the influence of the bulk doping on the transistor TID response. High doping regions in the bulk attenuate the effects induced by the charge buildup in the STI. This attenuation is larger in short-channel pMOSFETs due to the overlap of the halo regions.

4.5 Conclusions

At ultra-high doses, the TID response of 28 nm pMOSFETs and nMOSFETs depends on channel width, channel length, and bias condition. Worst-case shifts are observed for both nMOSFETs and pMOSFETs irradiated at high gate voltage, due to increased charge yield in each, and to interface-trap formation in nMOSFETs at higher doses. DC and low frequency noise measurements indicate that positive charge trapping in the STI oxide leads to enhanced degradation in narrow channel transistors. At doses up to 100 Mrad(SiO_2), the dominant degradation mechanism is trapping of positive charges in the STI. At ultra-high doses, the effects of interface traps along the gate oxide and STI sidewalls become more significant. Low-frequency noise measurements show the presence of RTN in small devices and increased noise with dose, due primarily to charge trapping in the gate dielectric. Moreover, short-channel transistors show lower radiation-induced degradation than long channel ones. Indeed, modern CMOS technologies employ the halo implantations, highly doped bulk regions close to the extensions. In short channel transistors, the source and drain halo implantations can overlap each other, increasing the overall doping in the channel region. TCAD simulations confirm the influence of the bulk doping concentration on the TID response. Higher bulk doping requires larger amount of charge to alter the carrier distribution, consequently mitigating the radiation-induced effects in short channel transistors. By combining the experimental measurements with simulations, I confirm that the channel-length dependence is associated with the halo implantations, which fortuitously increase the radiation tolerance of modern CMOS devices.

Chapter 5

16 nm InGaAs FinFET technology with high-k dielectrics

With the 16 nm technology node, the scaling limitations of SiO_2 have required the introduction of high-k dielectric materials [122], improved design structures and new channel materials. III-V compound semiconductors combined with the FinFET structure and high-k gate dielectrics are potentially promising structures for future high-speed applications [148]. Recently, indium gallium arsenide (InGaAs) has been used as an alternative channel material in n-type FETs due to its high electron mobility, with the possibility of co-integration with standard Si CMOS processing technology [27].

Recent works [149–151] have pointed out several possible issues for high-k dielectric-based InGaAs transistors when exposed to TID irradiation. InGaAs multi-fin capacitors with combined HfO_2 and Al_2O_3 gate stacks show higher sensitivity to total-ionizing-dose (TID) irradiation compared to Si MOS capacitors and Ge multi-fin capacitors [149]. Capacitance-voltage $C - V$ and capacitance-frequency $C - f$ measurements in InGaAs capacitors show high densities of interface and border traps and large densities of TID-induced trapped positive charge [149, 150]. In [151], TID effects in InGaAs FinFETs of several channel lengths with HfO_2 over Al_2O_3 gate dielectrics were evaluated at several bias conditions. Similar to InGaAs MOSFETs [150], a large negative threshold voltage shift was observed at doses below 500 krad(SiO_2) [151]. Worst-case responses were found with negative gate bias during irradiation and for short channel transistors [151]. These results provide early insight into TID-induced degradation, without detailed discussion of the location, microstructure, activation mechanism, and energetics of the defects responsible for radiation-induced charge trapping in these materials and devices.

In this chapter, I evaluate the TID response of InGaAs FinFETs, irradiated under positive, negative, and grounded bias and annealed at high temperature. Combining low-frequency noise measurements over a wide temperature range and density functional theory (DFT) calculations, I obtained insight into defects in InGaAs FinFETs with HfO_2/Al_2O_3 based gate stacks. Finally, the TID response of a second-generation lot of InGaAs FinFETs

with improved performance is compared to the previous first-generation one, in order to understand how the TID sensitivity changes with different transistor structure and materials.

The work presented in this chapter has been supported by: AFRL and AFOSR through the Hi-REV program, DTRA through its Basic Research program, Department of Defense's High Performance Computing Modernization Program, and by the McMinn endowment at Vanderbilt University.

Most of the results and figures presented in this chapter may have been published and/or submitted in the following peer-reviewed publications:

- [152] S. Bonaldo, S. E. Zhao, A. O'Hara, M. Gorchichko, E. X. Zhang, S. Gerardin, A. Paccagnella, N. Waldron, N. Collaert, V. Putcha, D. Linten, S. T. Pantelides, R. A. Reed, R. D. Schrimpf, and D. M. Fleetwood, "Total-ionizing-effects and low-frequency noise in 16-nm InGaAs FinFETs with HfO_2/Al_2O_3 dielectrics," in *IEEE Transactions on Nuclear Science*, vol. 67, no. 1, Jan. 2020. **Winner of the Best Student Paper Award: 2019 IEEE Nuclear and Space Radiation Effects Conference - NSREC, San Antonio, TX, USA, July 2019.** (Accepted).

- [153] S. E. Zhao, S. Bonaldo, P. Wang, E. X. Zhang, N. Waldron, N. Collaert, D. Linten, S. Gerardin, A. Paccagnella, R. D. Schrimpf, R. A. Reed, and D. M. Fleetwood, "Total ionizing dose effects on InGaAs FinFETs with improved gate stack," in *IEEE Transactions on Nuclear Science*, vol. 67, no. 1, Jan. 2020. (Accepted).

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Moreover, the results may have been presented at the following international conferences:

- Nuclear and Space Radiation Effects Conference - NSREC 2019, San Antonio, TX, USA, 8th-12th July 2019, oral presentation about "Total-ionizing-effects and low-frequency noise in 16-nm InGaAs FinFETs with HfO_2/Al_2O_3 dielectrics". (I was the presenting author)

- Nuclear and Space Radiation Effects Conference - NSREC 2019, San Antonio, TX, USA, 8th-12th July 2019, oral presentation about "Total ionizing dose effects on InGaAs FinFETs with improved gate stack".

- Radiation Effects on Components and Systems - RADECS 2018, Gothenburg, Sweden, 16th-21th September 2018, oral presentation about "Gate Bias and Length De-

pendences of Total-Ionizing-Dose Effects in InGaAs FinFETs on Bulk Si".

5.1 Experimental details

5.1.1 Test structures

Devices under test (DUTs) are manufactured in a development-stage 16-nm Si-bulk InGaAs FinFET process. Figure 5.1 shows the schematic structure of the InGaAs FinFETs. The high-k gate stack is formed by 2 nm of HfO_2 over 2 nm of Al_2O_3, with an equivalent oxide thickness of 1.5 nm. Transistors are designed with a single fin of n-type $In_{0.53}Ga_{0.47}As$, which allows the device to work in accumulation mode. The fin width is 16 nm and the height is 15 nm. Two different channel lengths (L) were tested, 50 nm and 1 μm. Transistors are bonded in a custom package allowing measurements to be performed at cryogenic temperatures with separate gate, source, and drain contacts and no ESD protection [154].

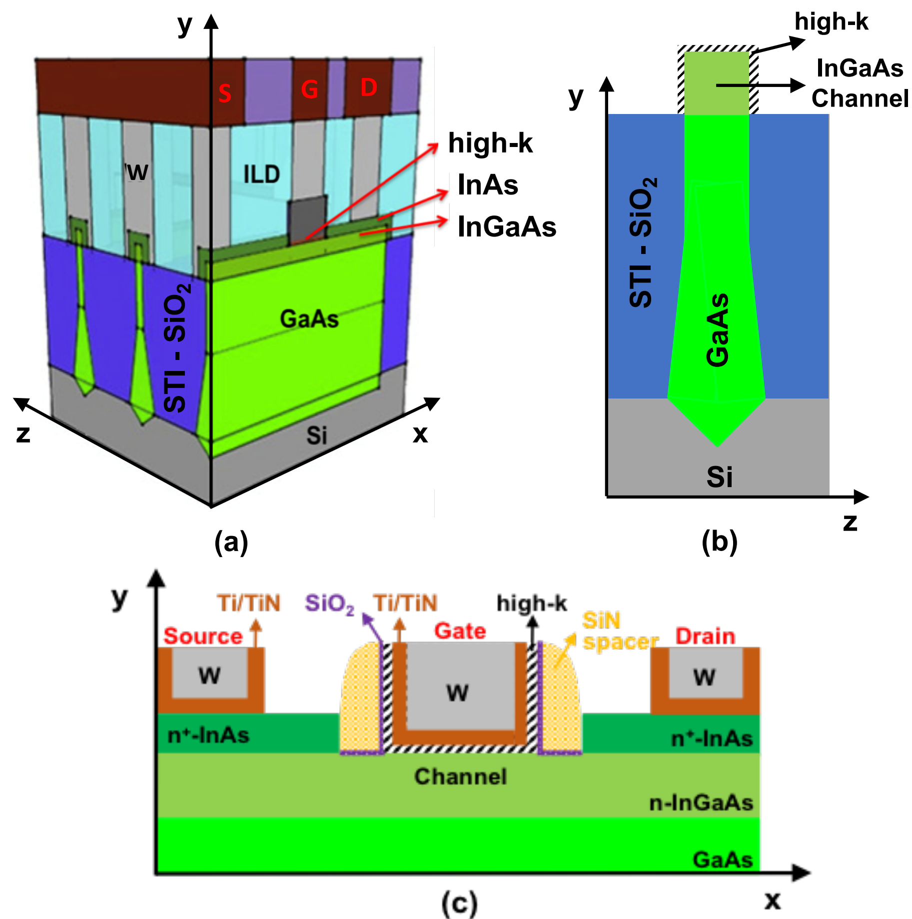


Figure 5.1: Schematic diagrams of InGaAs FinFETs: (a) 3D structure. (b) Cut-plane along channel width on the zy plane. (c) Cut-plane along channel length on the xy plane. (From [152])

5.1.2 Irradiation conditions and measurements details

Irradiations were performed at room temperature at Vanderbilt University using an ARACOR Model 4100 X-ray irradiator, composed of a tungsten tube with peak energy deposition at 10 keV [14]. The dose rate was 30.3 krad(SiO_2)/min; all doses and rates are referred to equilibrium doses in SiO_2 for consistency in calibration and to facilitate comparison with other work [14]. After exposure, devices were annealed at 400 K for 6 hours. Irradiation and annealing were performed for three different bias configurations: "-1V" (V_{gs} = -1 V, V_{ds} = 0 V), "0V" (V_{gs} = 0 V, V_{ds} = 0 V), and "+1V" (V_{gs} = 1 V, V_{ds} = 0 V). Measurements were performed on more than 10 devices. At least two devices of each type were evaluated for all experimental conditions. Nominally identical devices irradiated, annealed, and tested under similar conditions show DC parameter degradations that typically vary by less than ± 15%. Typical results are shown below. Transistor DC responses were measured with a semiconductor parameter analyzer at several temperatures before irradiation, after exposure, and after annealing. The threshold voltage V_{th} is calculated as $V_{gs-int} - V_{ds}/2$, where V_{gs-int} is in the linear region (V_{ds} = 50 mV), as the gate voltage axis intercept of the linear extrapolation of the $I_d - V_{gs}$ curve at the point of its maximum first derivative point. No significant differences in radiation response were observed for measurements performed under saturation conditions (V_{ds} = 1.1 V). The low-frequency (mostly $1/f$) noise is measured between 1 Hz and 400 Hz in the linear region (V_{ds} = 50 mV) at several temperatures and gate voltages, $V_{gt} = V_{gs} - V_{th}$.

5.2 Experimental results

5.2.1 DC static characterization

Figure 5.2 plots the $I_d - V_{gs}$ curves for InGaAs FinFETs with $L = 1$ μm, irradiated up to 500 krad(SiO_2), in the "+1V", "0V" and "-1V" bias conditions. After irradiation, devices show large negative shifts due to net positive oxide-trap charge. This significant increase of subthreshold stretchout indicates the generation of large densities of interface and border-traps [34, 63, 151]. The increase in subthreshold leakage current visible at V_{gs} = -1 V also indicates positive charge buildup in the shallow trench isolation [34, 35, 37–39]. The largest V_{th} shift is visible in the FinFET irradiated in the "-1V" condition. The changes in derivatives of the subthreshold slopes of the I_d-V_{gs} curves and in-creases of leakage current are due primarily to the non-uniform defect energy distribution of the transistors and the activation of a parasitic channel close to the STI oxides. In the "1V" condition, the leakage current at V_{gs} = -1 V increases by more than two orders of magnitude.

Figure 5.3 summarizes the radiation-induced shifts of the threshold voltage V_{th} with dose. In Figure 5.3(a), the V_{th} degradation is shown as a function of bias conditions for transistors irradiated to 500 krad(SiO_2) and annealed for 6 hours at 400 K. Worst-case is for "-1V"-biased transistors, which exhibit a ΔV_{th} shift of -280 mV vs. -196 mV for "+1V"-

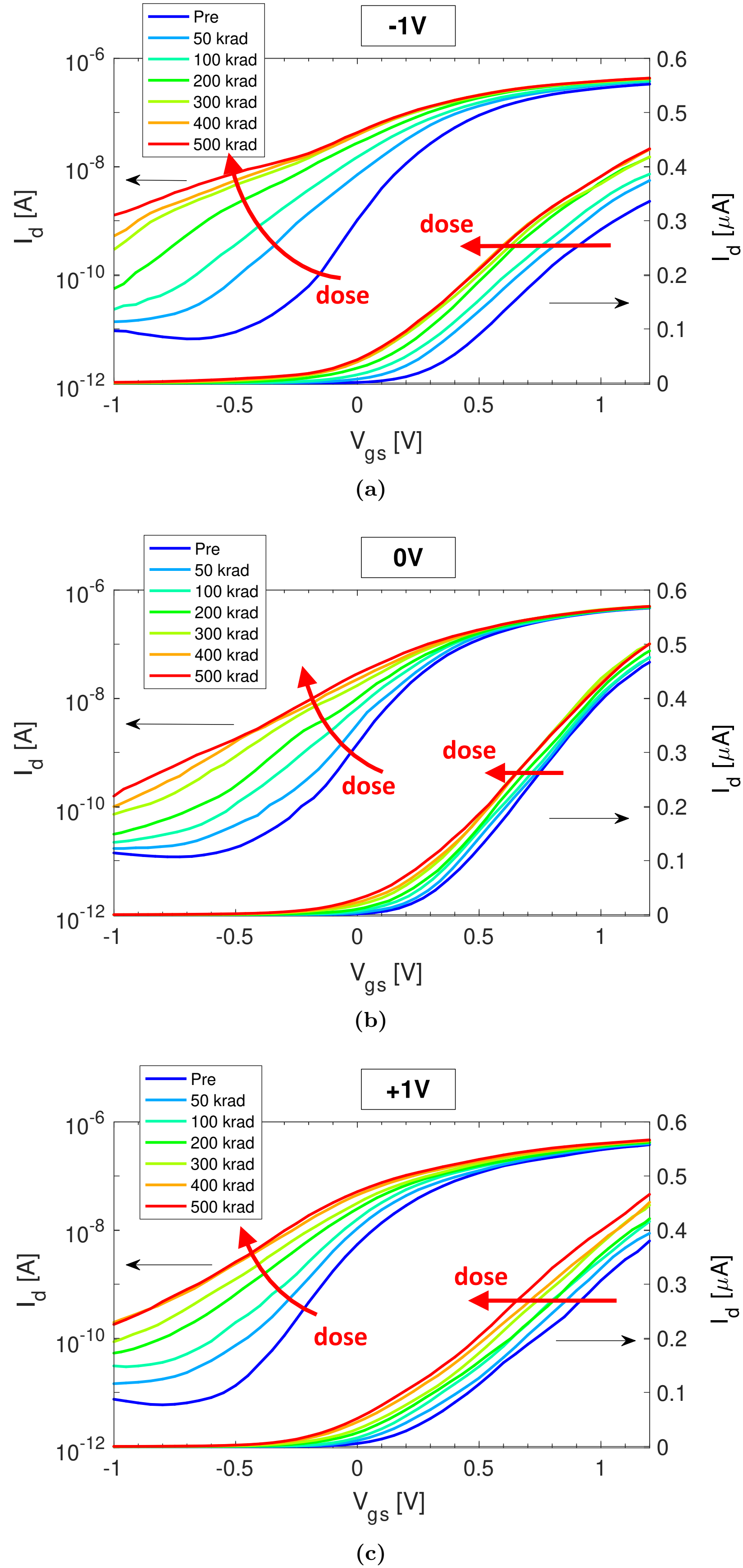
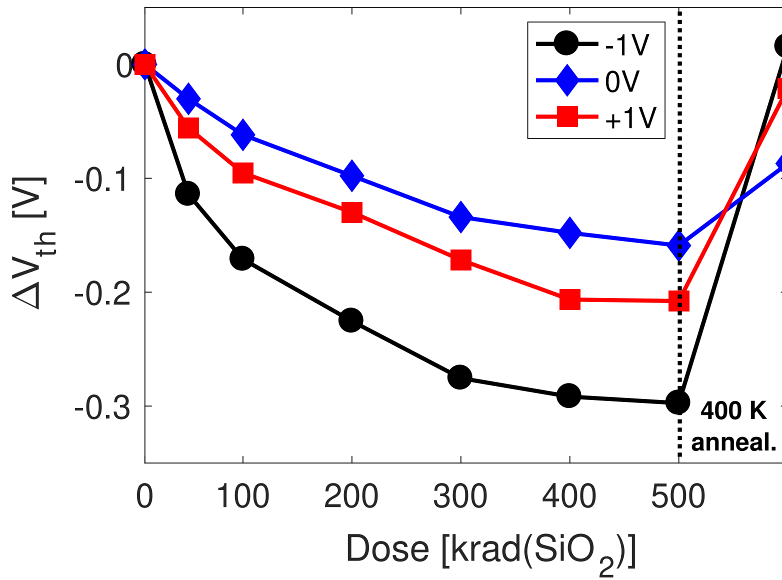
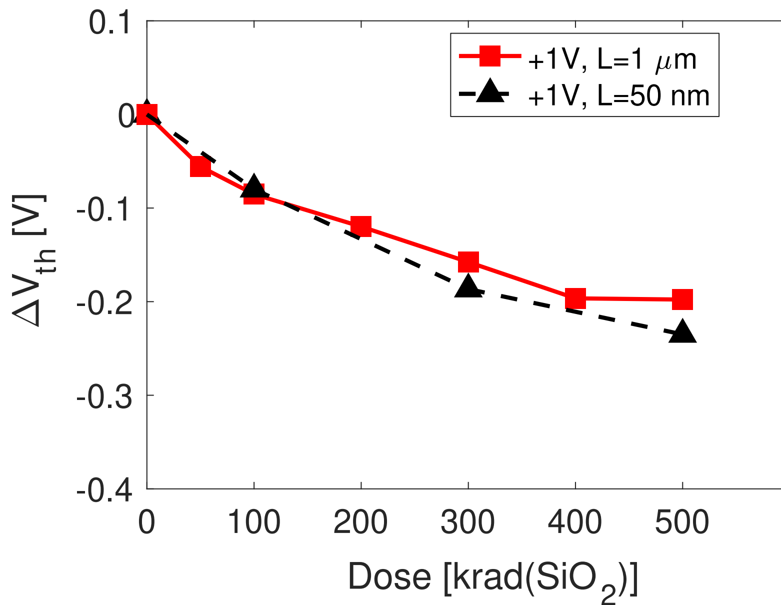


Figure 5.2: $I_d - V_{gs}$ response at different irradiation steps in the linear region of device operation (V_{ds} = 50 mV) for InGaAs FinFETs with $L = 1$ μm. Transistors were irradiated at room temperature in three different bias conditions: (a) "-1V", (b) "0V" and (c) "+1V". (After [152])



(a)



(b)

Figure 5.3: (a) V_{th} shifts for InGaAs FinFETs with $L = 1$ μm irradiated up to 500 krad(SiO_2) and annealed for 6 h at 400 K in "-1V", "0V" or "+1V" bias conditions. (b) V_{th} shifts for InGaAs FinFETs with different channel lengths irradiated up to 500 krad(SiO_2) in the "+1V" bias condition. (After [152])

bias and -150 mV for "0V"-bias. "0V"-biased transistors show the highest tolerance to TID effects, caused by the limited charge yield related to the low electric field applied into the gate oxide during the irradiation [103]. After high temperature annealing, the values of V_{th} of the transistors are more positive than initial values for the "-1V" condition [34]. Nearly complete recovery is observed for the other bias conditions, owing to neutralization of most radiation-induced trapped holes in the gate dielectric [34]. The modest recovery visible at "0V" is due to the reduced electric field during annealing, as compared with the "+1V"- and "-1V"-bias conditions. This limits the number of tunneling electrons from the channel and gate, respectively, reducing the likelihood that trapped positive charge in the gate dielectric is neutralized [35, 63, 78]. The V_{th} shifts of the shortest-channel transistor are similar to, or slightly worse than, V_{th} shifts of the longest-channel transistors.

To provide an order-of-magnitude estimate of the maximum possible contribution of charge trapping in the gate dielectric to the observed V_{th} shifts, I first assume for simplicity that the trapping efficiency of the oxide $f_{ot} \approx 1$ (100% trapping probability). With this assumption, the density of holes trapped in the gate stack can be estimated via [147, 155–157]:

$$N_{ox} = k_g f_y t_{stack} k_{DEF} D \tag{5.1}$$

where N_{ox} is the areal density of trapped holes projected to the InGaAs/Al_2O_3 interface, k_g is the charge generation efficiency in the dielectric layers, f_y is the probability that an electron-hole (e-h) pair escapes recombination, t_{stack} is the physical thickness of the gate dielectric, k_{DEF} is the dose enhancement factor, and D is the dose. For 10-keV X-rays at high electric fields, f_y is nearly ~ 1 [12, 14]. The combined dielectric thickness $t_{stack} \approx 4$ nm (2 nm HfO_2 + 2 nm Al_2O_3). For simplicity I assume $k_g \approx 9.2 \text{ x } 10^{12}$ $cm^{-3}rad(HfO_2)^{-1}$, consistent with [156]. I further assume dose enhancement from the nearby W layer of at least $\sim$ 4x, based on the results of [157]. Under these assumptions, at 500 krad(SiO_2) the maximum density of trapped holes N_{ox-max} is estimated to be $\sim 7 \text{ x} 10^{12}$ cm^{-2}. The corresponding maximum threshold voltage shift (ΔV_{th-max}) is:

$$\Delta V_{th-max} = \frac{N_{ox-max} q}{C_{ox}} = \frac{N_{ox-max} q t_{EOT}}{\epsilon_0 \epsilon_{SiO2}} \tag{5.2}$$

where t_{EOT} is the equivalent oxide thickness (EOT), q is the elementary charge, ϵ_0 is the vacuum permittivity, and ϵ_{SiO2} is the relative dielectric constant of SiO_2. By (2), $\Delta V_{th-max} \approx 600$ mV. The measured V_{th} shift in the "1V"-biased devices in Figure 5.3(a) is $\sim$ 300 mV at 500 krad(SiO_2), which is $\sim$ 50% lower than the estimated maximum possible shift. Because I do not expect the dielectric charge trapping to be 100% efficient, the observed V_{th} shifts are indeed consistent with the assumption that charge trapping in the dielectric is the primary contributing factor. Additional contributions may result from electrostatic effects of nearby trapped charge in the STI, especially for shorter-channel devices [37].

Figure 5.4 shows the I_{on-lin}/I_{off} ratios for InGaAs FinFETs irradiated under dif-

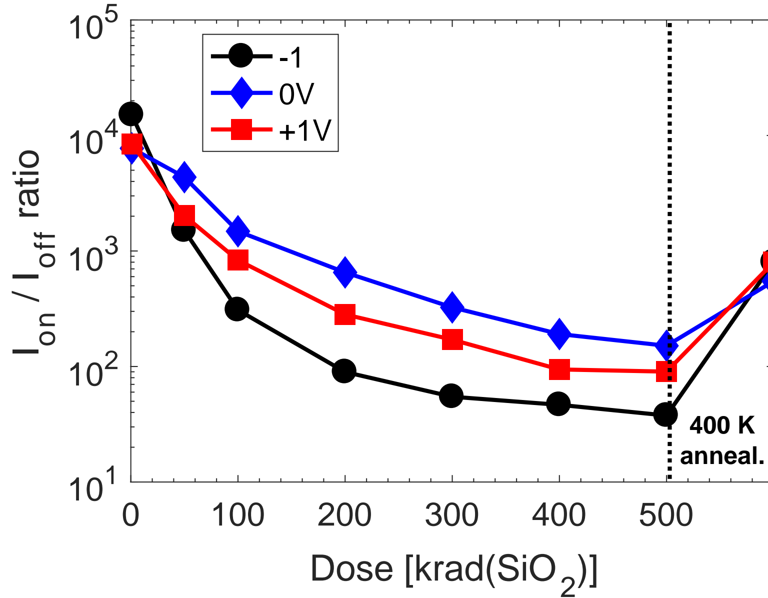


Figure 5.4: I_{on-lin}/I_{off} ratio for InGaAs FinFETs with L = 1 μm irradiated up to 500 krad(SiO_2) and annealed for 6 h at 400 K in "-1V", "0V" or "+1V" bias conditions. I_{on-lin} is defined as the drain current at V_{gs} = 1 V and V_{ds} = 50 mV, while I_{off} is defined as the drain current at V_{gs} = -0.4 V and V_{ds} = 50 mV. (From [152])

ferent bias conditions. I_{on-lin} is defined as the drain current at V_{gs} = 1 V and V_{ds} = 50 mV, while I_{off} is defined as the drain current at V_{gs} = -0.4 V and V_{ds} = 50 mV. Before exposure, transistors show an I_{on-lin}/I_{off} ratio of about 104. After 500 krad(SiO_2), I_{on-lin}/I_{off} ratios are primarily degraded by increases in leakage current and increases in $I_d - V_{gs}$ strechout. The worst-case ratio is in the "-1V"-biased transistors, which show an I_{on-lin}/I_{off} of 40 after 500 krad(SiO_2) vs. 100 in the "+1V" case and 200 in the "0V" case. After annealing, the recovery of the I_{on-lin}/I_{off} ratio is modest, compared to the ΔV_{th} recovery shown in 5.3(a). The small recovery of the I_{on-lin}/I_{off} ratio is likely due to more stable hole trapping in the near-by SiO_2 of the shallow trench isolation, increasing the leakage current and coupling electrostatically with the device channel [37, 38, 98].

5.2.2 $I_d - V_{gs}$ measurements: hysteresis effects

The hysteresis exhibited in the $I_d - V_{gs}$ curves was measured to study the slow charge trapping/detrapping response in the devices [63, 158]. The hysteresis is evaluated by performing two different V_{gs} sweeps of the $I_d - V_{gs}$ curves at a rate of $\sim$ 0.18 V/s. In the "BCK" (backward) mode sweep, the transistors are biased at V_{gs} = -1 V for 10 seconds and, then, V_{gs} is quickly swept from -1 V to 1.2 V. In contrast, for the "FWD" (forward) mode sweep, the transistors are biased at V_{gs} = 1.2 V for 10 seconds and, then, V_{gs} is quickly swept from 1.2 V to -1 V. Figure 5.5 compares the $I_d - V_{gs}$ curves in "BCK" and "FWD" modes before exposure, after 500 krad(SiO_2), and after 6 hours of annealing at 400

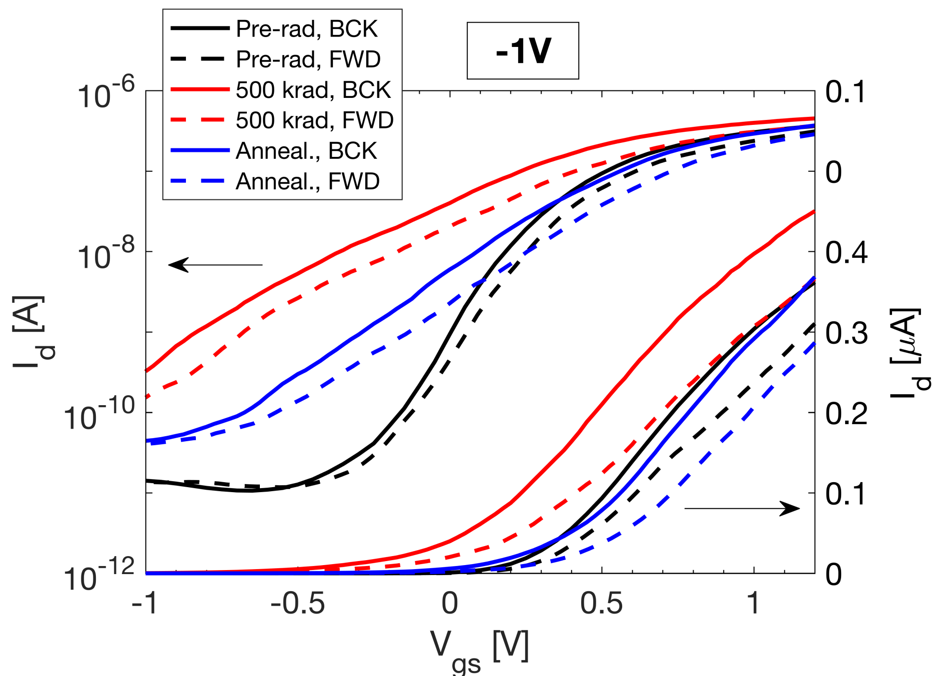


Figure 5.5: Hysteresis of the $I_d - V_{gs}$ curves for InGaAs FinFETs with $L = 1$ μm irradiated up to 500 krad(SiO_2) and annealed for 6 h at 400 K in the "-1V" bias condition. The "BCK" label refers to V_{gs} sweeps performed from -1 V to 1.2 V, while "FWD" labels refers to V_{gs} sweeps performed from 1.2 V to -1 V. (After [152])

K for "-1V"-biased InGaAs FinFETs. It has been verified that consecutive measurements alternatively in "BCK" and "FWD" modes overlap with each other, indicating a stable and reproducible process. Before exposure, after 500 krad(SiO_2), and after annealing, the "FWD" curves show larger V_{th} shifts than the "BCK" curves, due to the effects of slow border traps with capture/emission times on the order of few seconds [159]. The higher V_{th} values for the "FWD" responses and the greater stretchout than in the "BCK" curves indicate that the hysteresis is caused by electron traps [63, 159]. The long emission/capture times of these traps suggests that their spatial location is far from the Al_2O_3/InGaAs interface, probably close to the HfO_2/Al_2O_3 interface, where high densities of defects are expected due to the transition between the two different dielectric layers.

In Figure 5.6, the V_{th} hysteresis ($V_{th-FWD} - V_{th-BCK}$) is plotted at room temperature as a function of dose for InGaAs FinFETs irradiated under different bias conditions. The hysteresis increases with dose, suggesting increasing densities of slow traps with cumulative radiation [159]. Worst-case is found for the "-1V"-bias condition, consistent with Figures 5.2 and 5.3. For the "-1V"-bias condition, the hysteresis is 170 mV after 500 krad(SiO_2). The hysteresis is 105 mV and 130 mV for the "0V" and "+1V" bias conditions, respectively.

Figure 5.7 plots the V_{th} hysteresis ($V_{th-FWD} - V_{th-BCK}$) as a function of temperature for "-1V"-bias InGaAs FinFETs irradiated to 500 krad(SiO_2) and then annealed for 6 hours

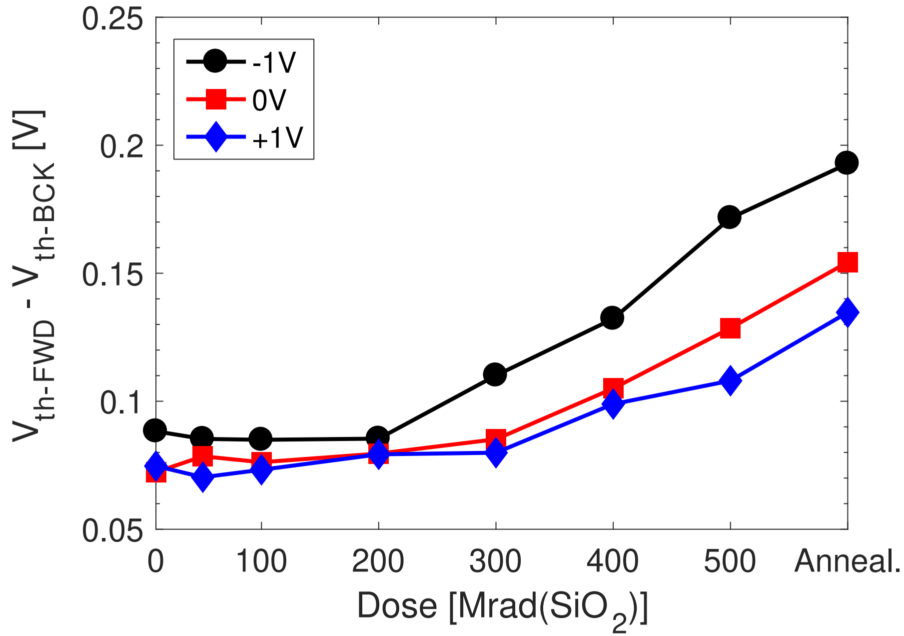


Figure 5.6: V_{th} hysteresis ($V_{th-FWD} - V_{th-BCK}$) at room temperature as a function of dose for InGaAs FinFETs with $L = 1$ μm irradiated up to 500 krad(SiO_2) and annealed for 6 h at 400 K in "-1V" "0V" or "+1V" bias conditions. (From [152])

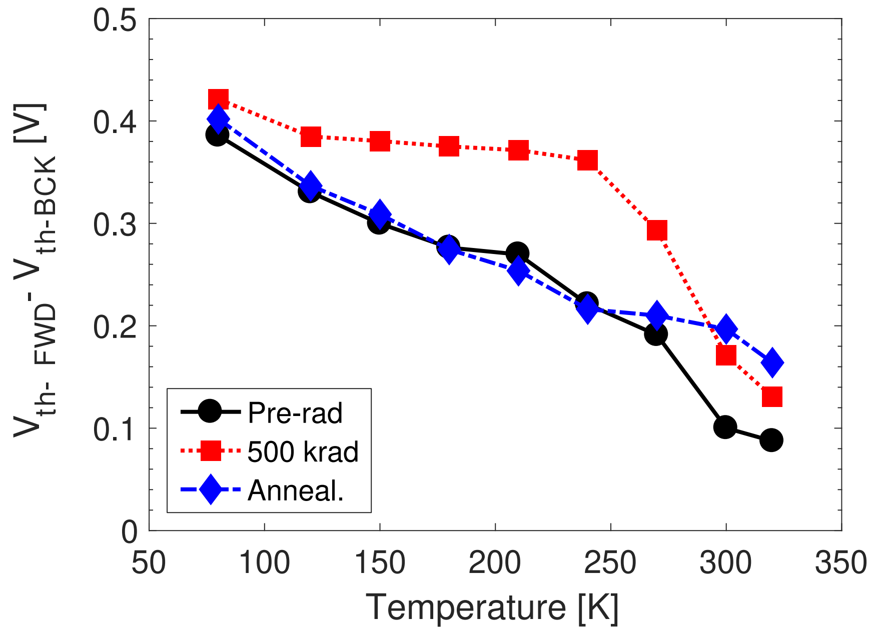


Figure 5.7: V_{th} hysteresis ($V_{th-FWD} - V_{th-BCK}$) as a function of temperature for InGaAs FinFETs with $L = 1$ μm irradiated up to 500 krad(SiO_2) and annealed for 6 h at 400 K in "-1V" bias conditions. (From [152])

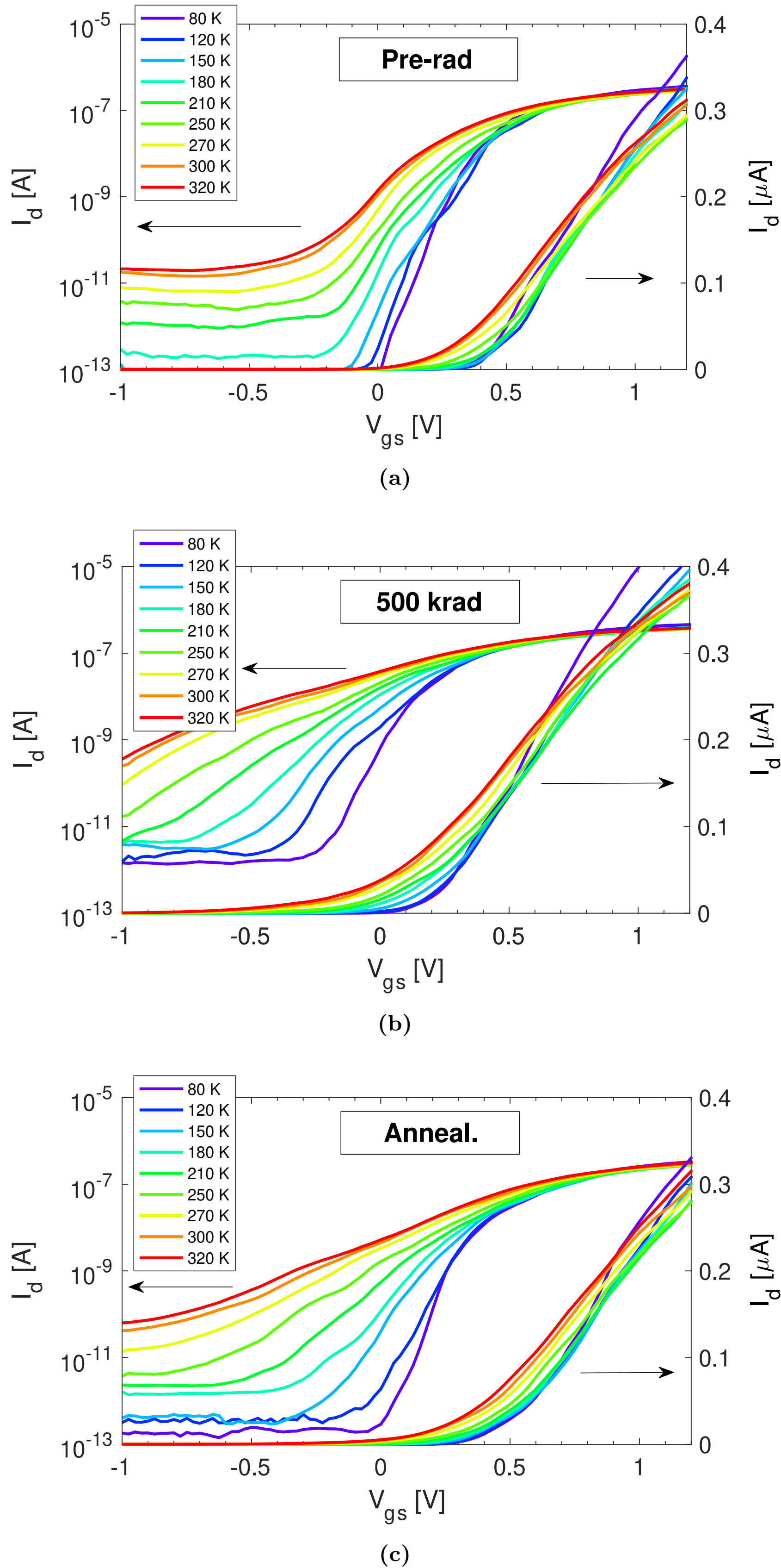
at 400 K. The hysteresis decreases with temperature, due to the enhanced rates at which charge can be exchanged with interface and border traps at elevated temperatures [12, 159]. After 500 krad(SiO_2), the V_{th} hysteresis decreases more slowly at lower temperatures, suggesting an enhanced role for tunneling (less sensitive to changes in temperature than thermally activated processes [160]) in the post-irradiation charge exchange than in the pre-irradiation charge exchange, and/or a peak in the border-trap density in the range of $\sim$ 150-200 K, as discussed below. After high temperature anneal-ing, the V_{th} hysteresis decreases almost to pre-irradiation values due to increasing trap neutralization.

5.2.3 DC response from 80 K to 320 K

The DC static response has been measured at temperatures ranging from 80 K to 320 K. Figure 5.8 shows $I_d - V_{gs}$ curves at different temperatures for a "-1V"-biased device (a) before exposure, (b) after 500 krad(SiO_2), and (c) after 6 h of annealing at 400 K. A parametric shift in temperature is detected in threshold voltage V_{th}, off-state current I_{off} (defined as the I_d at V_{gs} = -1 V) and subthreshold swing SS. In as-processed devices, the V_{th} strongly depends on temperature at $T > 200$ K, and is almost constant at lower temperatures. The transconductance decreases with temperature due to phonon scattering [161]. After 500 krad(SiO_2), transistors show increased subthreshold stretchout at all temperatures due to increases in interface and border trap densities. Increases in the base level of the leakage current are also observed, due to hole trapping in the STI ox-ides [37, 38, 98]. Finally, increased thermal generation of carriers in the depletion region is also seen as a result of in-creased radiation-induced defects, which can act as generation-recombination centers.

Figure 5.9 summarizes V_{th}, I_{off}, and SS as a function of temperature for "-1V"-biased InGaAs FinFETs before exposure, after 500 krad(SiO_2), and after 6 h at 400 K. After the irradiation, the value of V_{th} decreases by $\sim$-0.2 V at low temperature, and by $\sim$-0.3 V at high temperature. The increase of I_{off} at low temperature in irradiated devices is due to two different factors. At low temperature, I_{off} has lower sensitivity to temperature, as it is related to the activation of the STI-related parasitic channel. At high temperature, I_{off} is dominated by the large increase of the subthreshold stretchout. This increase in SS is consistent with the large negative shift of the V_{th} due to the buildup of interface and border traps in the gate oxide that occurs during annealing [34, 63].

That neither the hysteresis nor the SS recovers to pre-irradiation values (see Figures 5.8 and 5.9) confirms the relative stability of interface and border traps in these devices, as compared with the radiation-induced trapped positive charge [34, 63]. The lack of complete recovery in values of I_{off} indicates residual trapped positive charge in the sidewall regions of the STI and/or backside interface between the n-InGaAs channel and GaAs buffer layer.

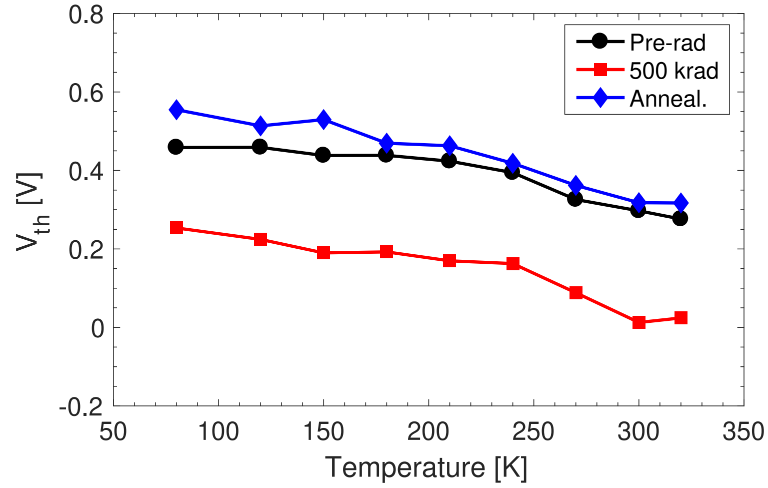


(a)

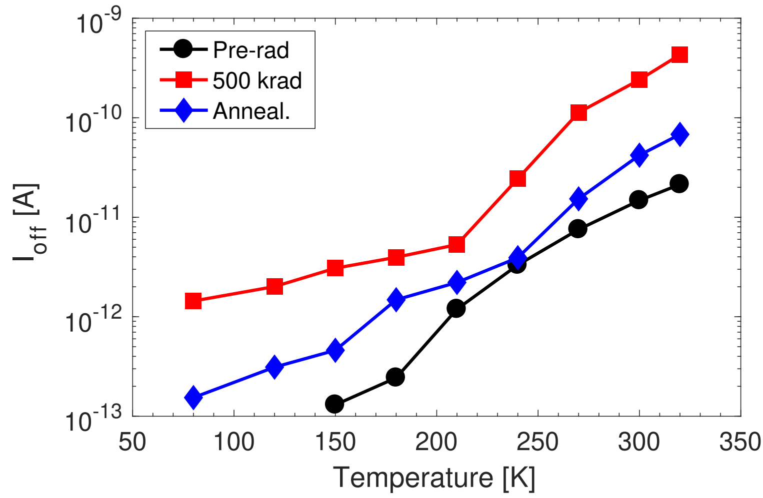
(b)

(c)

Figure 5.8: $I_d - V_{gs}$ curves vs. temperature in the linear region of operation (V_{ds} = 50 mV) for InGaAs FinFETs with $L = 1$ μm in the "-1V" bias condition: (a) Before irradiation, (b) after irradiation to 500 krad(SiO_2), and (c) after 6 h of annealing at 400 K. (From [152])



(a)



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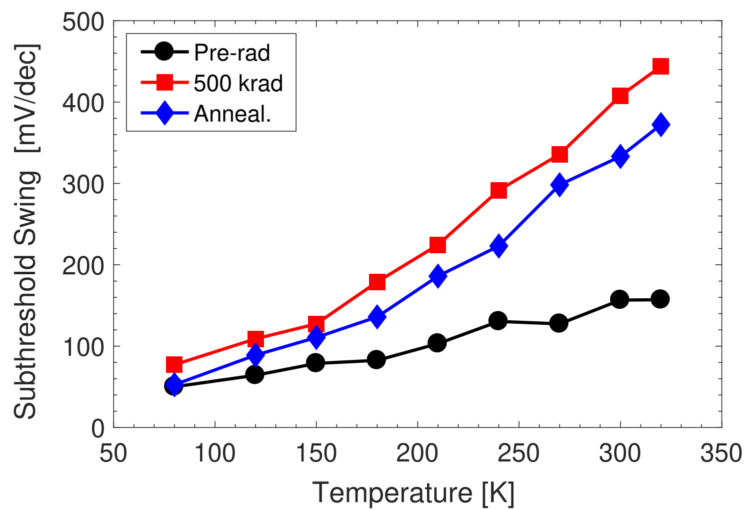
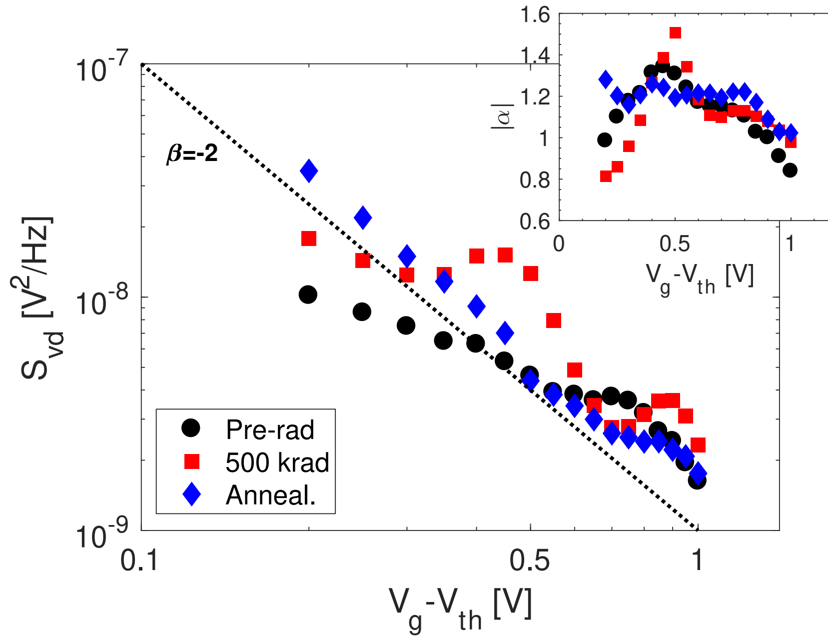
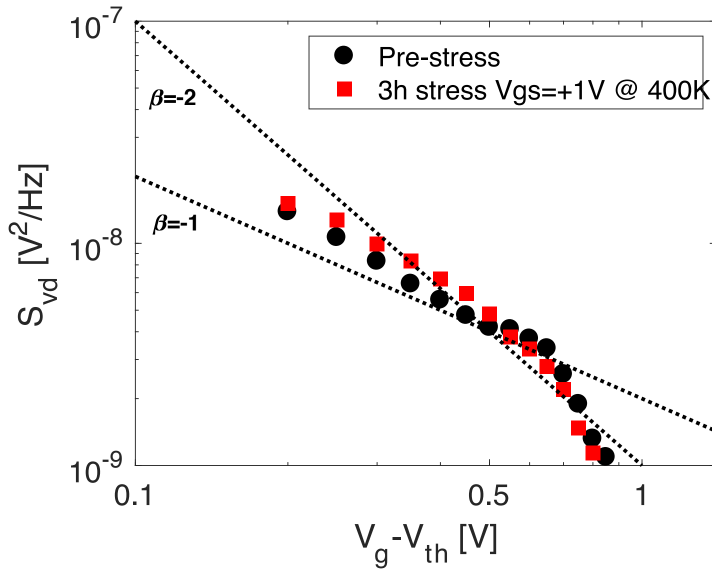


(c)

Figure 5.9: DC static parameters at several temperatures for InGaAs FinFETs with $L = 1$ μm irradiated up to 500 krad(SiO_2) and annealed for 6 h at 400 K in the "+1V" bias condition: (a) threshold voltage, (b) off-state current defined here as the Id at V_{gs} = -1 V, and (c) subthreshold swing. (From [152])



(a)



(b)

Figure 5.10: $1/f$ noise magnitude at 10 Hz as a function of $V_{gs} - V_{th}$ for (a) InGaAs FinFETs irradiated up to 500 krad(SiO_2) and annealed for 6 h at 400 K in the "+1V" bias condition, and (b) unirradiated devices baked at 3 h under similar bias conditions. The inset of (a) shows the experimental alpha values.(From [152])

5.2.4 Low frequency $1/f$ noise vs. V_{gs}

Low-frequency noise measurements are used to obtain insight into the densities, energies, and microscopic nature of the defects contributing to radiation-induced charge trapping [62, 137, 141, 141, 142, 144, 145, 162–168]. The dependence of the noise with applied gate voltage indicates the energy distribution of the defects [141, 142, 144, 145]. The excess drain-voltage noise power spectral density S_{vd} can be expressed as a function of V_{gs} and f by the following equation [169, 170]:

$$S_{vd}(f, V_{ds}, V_{gs}) = KV_{ds}^2 f^{-\alpha}(V_{gs} - V_{th})^{-\beta} \tag{5.3}$$

where K is a constant factor indicating the normalized noise magnitude, α represents the exponential factor indicating the dependence with frequency, and β is the exponential factor indicating the dependence with $V_{gt} = V_{gs} - V_{th}$; $S_{vd} \propto (V_{gs} - V_{th})^{-\beta}$ [170]. When the gate oxide defects are uniform in space and in energy along the InGaAs channel band gap, the β factor is $\approx$2 [169, 170]. Significant deviations from $\beta \approx 2$ indicate non-uniform distribution of the defects in energy and/or space. In n-channel devices, when $\beta < 2$, the effective density of border traps is increasing towards the conduction band [171]; when $\beta > 2$, the effective density of border traps is increasing toward midgap [142, 144, 145].

Figure 5.10 shows low-frequency noise magnitude at f = 10 Hz for several values of $V_{gt} = V_{gs} - V_{th}$ for InGaAs MOSFETs before and after 500 krad(SiO_2) irradiation in the "+1V" bias condition. The increase of the noise after irradiation indicates the generation of radiation-induced border traps. Before irradiation, the value of β is $\approx$1, indicating large densities of border traps close to conduction band [142, 144, 145]. After 500 krad(SiO_2), the noise magnitude S_{vd} increases, and the dependence of S_{vd} on $V_{gs} - V_{th}$ shows a peak at V_{gt} = 0.5 V. The peak at 0.5 V suggests a non-uniform density in energy, with maximum border-trap density at $V_{gs} - V_{th}$ = 0.5 V. After high temperature annealing, the noise magnitude decreases and the β factor is $\approx$ 2, indicating a reduction in total defect density and more uniform energy distribution of border traps [62, 137]. Figure 5.10(b) shows that baking as-processed devices at 400 K for $\sim$ 3 h does not significantly change the noise of these devices, confirming the relative stability of as-processed devices. Hence, the results of Figure 5.10 are consistent with trends in I_d-V_{gs} curves in Figures 5.2, 5.5, and 5.8.

5.2.5 Low frequency $1/f$ noise vs. temperature

In modern semiconductor devices, low-frequency noise is caused primarily by random thermally activated processes having a broad distribution of energies relative to kT. The Dutta-Horn model describes the relation of the $1/f^\alpha$ noise with frequency and temperature [162]:

$$\alpha(f, T) = 1 - \frac{1}{\ln(2\pi f \tau_0)}\left(\frac{\delta \ln S_{vd}(T)}{\delta \ln T} - 1\right) \tag{5.4}$$

where S_{vd} is the excess drain-voltage noise power spectral density, τ_0 is the characteristic

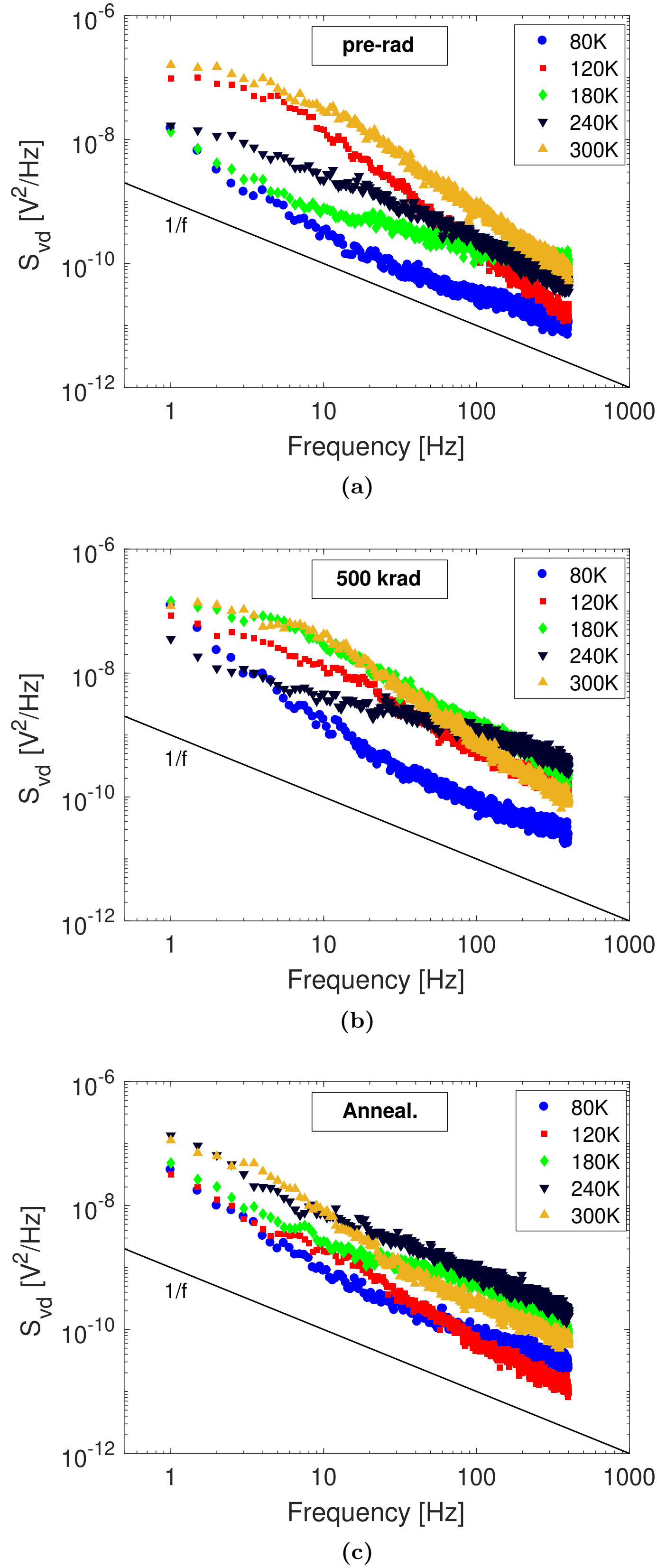


Figure 5.11: Low-frequency noise at several temperatures for InGaAs FinFETs with L = 50 nm at V_{ds} = 50 mV and V_{gt} = 0.5 V. The noise was measured (a) before the irradiation, (b) after exposure, and (c) after 6 h annealing at 400 K. The bias condition during the exposure and annealing was "+1V". (After [152])

time of the process leading to the noise. The defect-energy distribution $D(E_0)$ can be obtained from measurements of the S_{vd} vs. temperature by the relation:

$$D(E_0) \propto \frac{2\pi f}{kT} S_{vd}(f,T) \tag{5.5}$$

where the defect energy E_0 is related to the temperature and frequency by the expression:

$$E_0 \approx -kT \ln(2\pi f \tau_0) \tag{5.6}$$

In this work, the value of τ_0 is chosen to be 1.81 x10^{-15} s, consistent with previous work on Si MOS devices [160, 163].

Figure 5.11 shows the noise magnitude vs. frequency at several temperatures for an InGaAs FinFET irradiated to 500 krad(SiO_2) and annealed for 6 h at 400 K in the "+1V" bias condition. Before irradiation, the power spectra at 80 K, 180 K, and 240 K show the typical $\sim 1/f$ frequency dependence. In contrast, the frequency dependences at 120 K and 300 K have a slope of $\sim 1/f^2$ for $f > 8$ Hz and $< 1/f$ 1.0 for $f < 8$ Hz, i.e., a Lorentzian shape [137]. This indicates a single, dominant defect switching its charge state actively at a rate of ~8 Hz [137]. When the device is irradiated to 500 krad(SiO_2), the power spectrum at 180 K increases abruptly and the slope changes from $1/f$ to $1/f^2$, indicating the activation of a new dominant trap level.

In Figure 5.12, the noise is measured in the time domain at 180 K with the same bias condition as in Figure 5.11. After the exposure, large random telegraph noise (RTN) [172] is visible. This indicates the alternate capture and emission of carriers at an individual, prominent defect site, which generates discrete switching in the device channel resistance. At 500 krad(SiO_2), the emission/capture time is about 230 ms, consistent with the Lorentzian power spectrum at $T = 180$ K and corner frequency $f_c \approx 8$ Hz. After annealing, the strong RTN signal is not visible and the noise generally decreases at all temperatures, and recovers the $\sim 1/f$ shape of the power noise spectrum. This shows that the defect responsible for the RTN has been neutralized or removed by the elevated temperature annealing process.

The shape of the defect-energy distribution $D(E_0)$ is proportional to $S_{vd} \cdot f/T$, where E_0 is the energy barrier needed by the system to change the trap occupation [137, 162]. Figure 5.13 shows the f/T-normalized low-frequency noise as a function of the temperature at $f = 10$ Hz for "+1V" and "-1V" biased transistors. Pre-irradiation noise measurements show peaks at ~130 K and 300 K, corresponding to activation energies of ~0.25 eV and ~0.8 eV, respectively. As-processed devices may show both, one, or neither peak, consistent with the part-to-part variation in $I_d - V_{gs}$ curves discussed above. After irradiation, all tested devices for both "+1V" and "-1V" bias conditions exhibit a large increase of noise magnitude at T ≈180 K (~0.4 eV), which is the dominant defect contributing to the low-frequency noise of these devices. An additional peak is generated at ~300 K (~0.8 eV) for "-1V"-biased transistors. This peak is consistent with the change

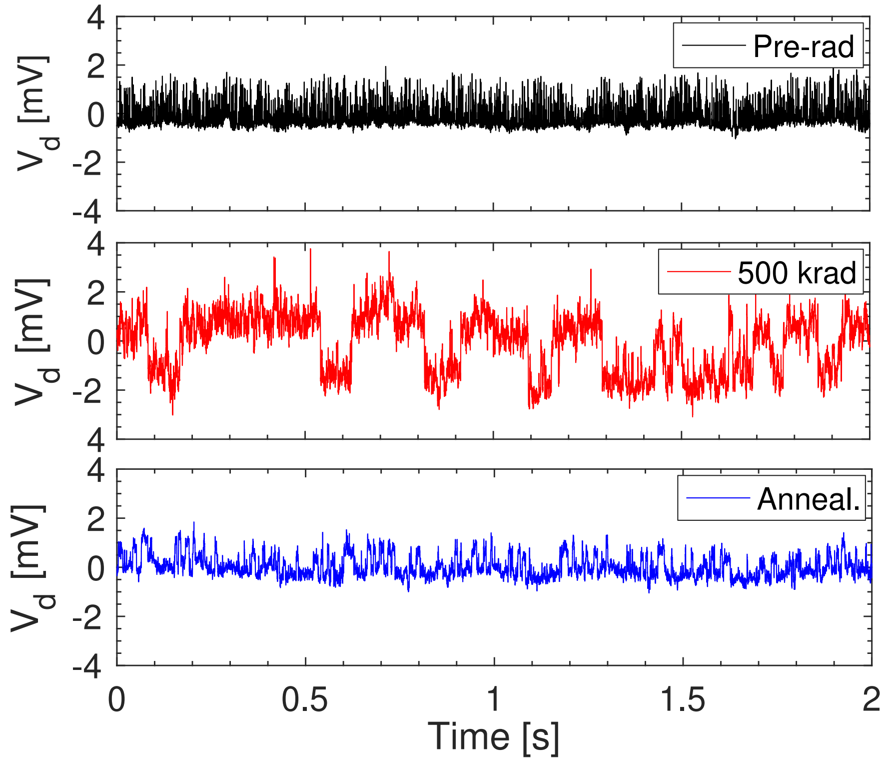


Figure 5.12: Random telegraph noise (RTN) at T = 180 K for a InGaAs FinFET, shown in 5.11, before exposure, after 500 krad(SiO_2) and after high temperature annealing in "+1V" bias condition. During the measurement, the transistor was biased at V_{gs} = 0.5 V and V_{ds} = 50 mV at 180 K. (From [152])

in slope in voltage dependence of the room temperature noise in Figure 5.10(a), as each of these parameters is affected by the changes in defect-energy distribution that occur at $\sim$ 300 K [137, 142, 144, 145]. After annealing, the peak at $\sim$180 K decreases significantly, and the peaks at 130 K and 300 K in the irradiated devices change in shape from pre-irradiation levels. These changes in peak size and/or shape are often characteristic of changes in both defect density and microstructure (e.g., configuration of nearest-neighbor atoms) [62, 137, 162].

Figure 5.14 compares the α parameter of experimental data of Figure 5.13(c) with α values derived from the Dutta-Horn model via Eq. (5.4). The α values from the Dutta-Horn model are in reasonable qualitative agreement with the experimental values, justifying the use of Dutta-Horn analysis to provide insight into the kinetics and microstructures of the defects responsible for the observed noise [173].

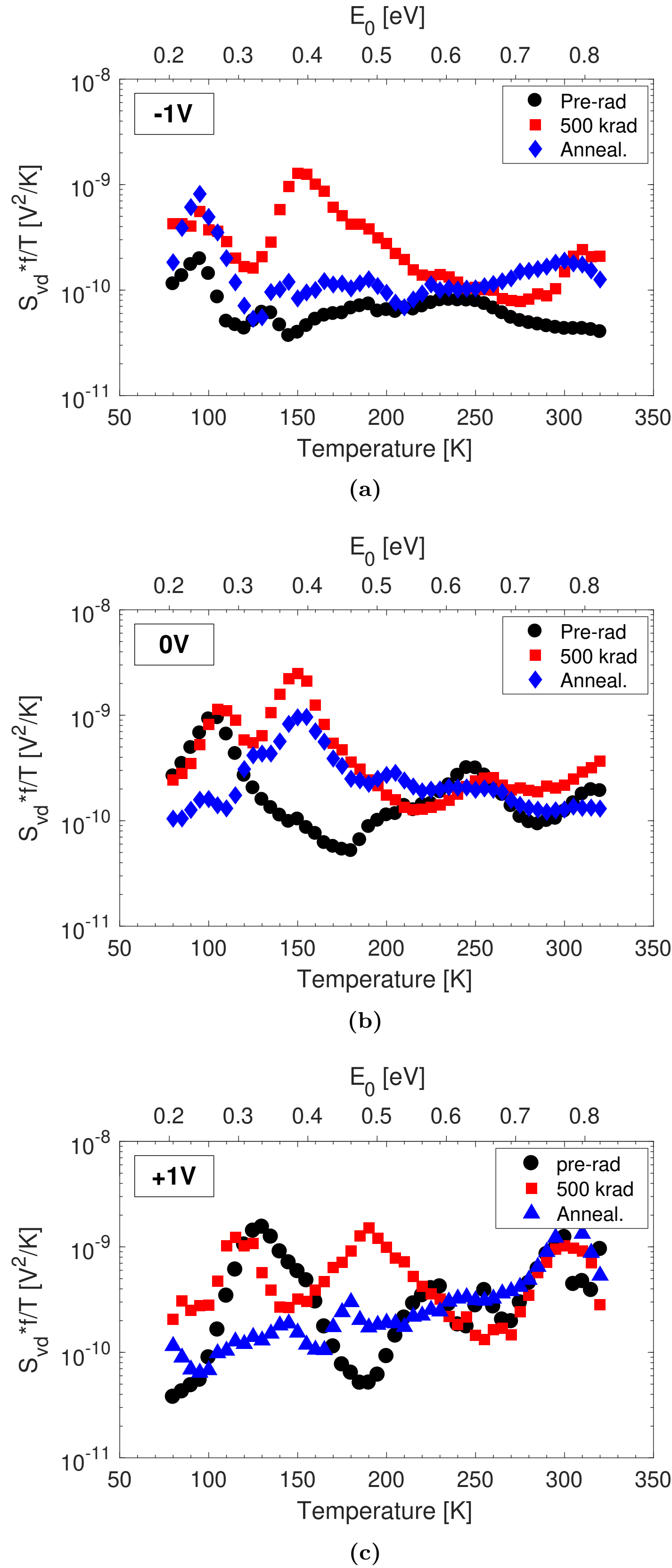
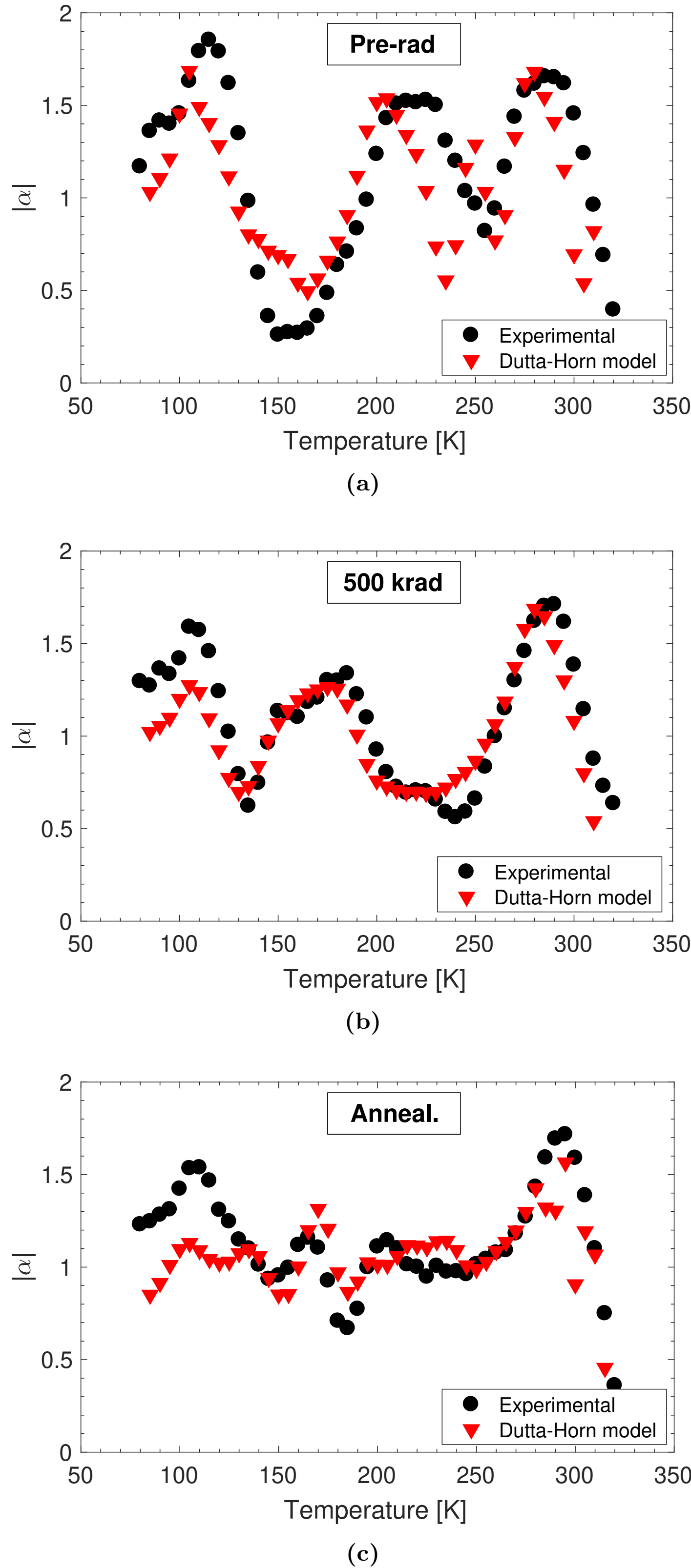


Figure 5.13: Normalized $1/f$ noise magnitude as a function of temperature for InGaAs FinFETs biased at V_{ds} = 0.1 V and V_{gt} = 0.5 V. The noise was measured at f = 10 Hz before irradiation, after exposure, and after 6 h annealing at 400 K. The bias condition during exposure and annealing was (a) "-1V", (b) "0V" and (c) "+1V". The energy scale on the upper x-axis is derived from the Dutta-Horn model of $1/f$ noise with τ_0 = 1.8 x10^{-15} s. (After [152])



(a)

(b)

(c)

Figure 5.14: Frequency dependence of the low-frequency noise for the InGaAs FinFET shown in 5.13(c). The transistor was irradiated up to 500 krad(SiO_2) and annealed for 6 h at 400 K in the "+1V" bias condition. The experimental values of α are compared with the values derived from the temperature dependence of the noise magnitude via Eq. (5.4): (a) Before exposure, (b) after 500 krad(SiO_2), and (c) after 6 h annealing at 400 K.

5.3 Defect microstructure

5.3.1 Calculation methods

To further explore the nature of the defects responsible for the observed threshold voltage and low-frequency noise measurements, DFT calculations were performed using the Vienna Ab initio Simulation Package (VASP) code [174, 175]. Calculations were performed using the project-augmented-wave pseudopotential method [176, 177] with a plane-wave-cutoff energy of 400 eV and the HSE06 range-separated hybrid functional for the exchange correlation functional [178, 179]. Defect microstructures were calculated in bulk unit cells with experimental lattice constants [180–183]. The HSE06 hybrid functional has been shown over a wide range of systems to not only produce DFT-based bandgaps in good agreement with experimental values, but also improved values for the position of defect levels [175, 184]. HfO_2 was modelled using the monoclinic phase. Al_2O_3 was modelled using the θ phase (rather than the α phase), because its lower density and average bond coordination is more similar to amorphous gate oxides [185]. In amorphous gate oxides, defect levels in the gap typically are distributed around the crystal level, due to variations in the local environment. To have a computationally-practical-sized supercell, $In_{0.53}Ga_{0.47}As$ was approximated as $In_{0.50}Ga_{0.50}As$ in a checkerboard pattern; this leads to negligible shifts in the band edge positions. GaAs and InGaAs were modelled with the cubic zinc-blende phase with InGaAs as a checkerboard pattern in a 2x2x2 supercell. As an approximation to $In_{0.53}Ga_{0.47}As$, our model has the ratio $In_{0.5}Ga_{0.5}As$. This leads to negligible shifts in the band edge positions. For calculation of the defect energies, I utilized supercells of the primitive cells with respective sizes of 2x2x2 for HfO_2, 1x4x2 for Al_2O_3, and 2x2x2 for GaAs. Brillouin zone integration was performed on k-point grids of 2x2x2, 2x2x2, and 4x4x4, respectively. For calculation of charged defects, I included electrostatic potential corrections due to finite supercell size [186]. The present results significantly extend previous studies of defects in HfO_2 and Al_2O_3 [169, 173, 175, 187–192].

To compare the calculated atomistic defect levels in the gate stack and strain-relaxed buffer layer to the Fermi level set by the n-type InGaAs channel, the relative band offsets between these materials is required. Alignment based on the ϵ_H $(+/-)$ energy level crossing point for an interstitial hydrogen often provides a reasonable approximation for a universal alignment point of the bands [193]. Calculated band offsets are illustrated in Figure 5.15, where the dotted red line indicates the Fermi energy level set by the conduction band in n-type InGaAs. For Al_2O_3/InGaAs, I obtained a valence band offset (VBO) of 3.71 eV. This compares favorably with experimental measurements and theoretical values for other phases of Al_2O_3 [187, 194–196]. The obtained VBO between HfO_2 and InGaAs is 3.39 eV. Experimentally, the reported HfO_2/InGaAs VBO can be quite variable [196–198], due to relative oxygen content at their interface [199]. I calculated GaAs/InGaAs VBO is 0.02 eV, slightly smaller than experimental values, due to neglecting strain effects, and consistent with the smaller band gap of InGaAs arising primarily from a lowering of the

CB [200, 201].

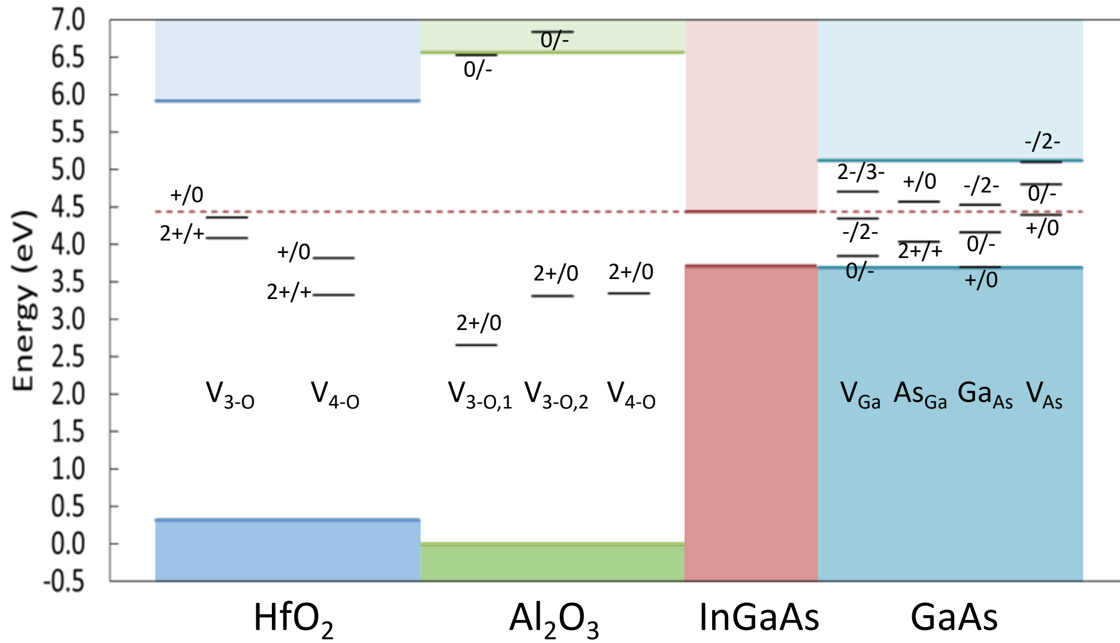


Figure 5.15: Calculated band alignment between HfO_2, Al_2O_3, InGaAs, and GaAs. Equilibrium defect levels are shown for two oxygen vacancy microstructures in HfO_2 (V_{3-O} and V_{4-O}), three oxygen vacancy microstructures in Al_2O_3 ($V_{3-O,1}$, $V_{3-O,2}$, and V_{4-O}), and the primary vacancies and antisites defects in GaAs. The conduction band level of InGaAs are extended as a guide to the eye. (From [152])

5.3.2 HfO_2 defects

In the HfO_2 structure, oxygen atoms can be either 3-fold coordinated or 4-fold coordinated to the Hf atoms [180]. This leads to two different oxygen vacancy microstructures to consider, which I label V_{3-O} and V_{4-O}. Both microstructures introduce $2+/+$ and $+/0$ donor levels that sit energetically below the InGaAs conduction band (Figure 5.15). These levels are initially neutral during pre-irradiation measurements. After irradiation, these levels can trap up to two holes [147]. This trapping is consistent with the observed negative V_{th} shifts during irradiation (Figures 5.2 and 5.3(a)) and subsequent recovery of V_{th} after annealing at 400 K (Figure 5.3(a)). Due to their physical distances from the InGaAs channel, these HfO_2-based defects are unlikely to account for the majority of the observed $1/f$ noise in the measured frequency span [137], as emission/capture times are out of the lowest frequency range of the experimental noise measurements. Thus, it is most likely that defects in the Al_2O_3 or GaAs layer which directly contact the InGaAs channel are responsible for the peaks in noise magnitude observed in Figure 5.13.

5.3.3 HfO_2 defects

Oxygen vacancies also are a common defect in Al_2O_3 dielectrics. In the θ-Al_2O_3 structural model presently used [181, 185], oxygen atoms are either 4-fold or 3-fold coordinated to the Al atoms with the 3-fold coordination possessing two symmetrically inequivalent sets of bond lengths. I, therefore, label the different oxygen vacancy microstructures as V_{4-O}, $V_{3-O,1}$, and $V_{3-O,2}$. The $V_{3-O,1}$ defect exhibits a localized $0/-$ acceptor level just below the Al_2O_3 band edge (Figure 5.15). After irradiation, trapped holes on the HfO_2 side of the HfO_2/Al_2O_3 interface can increase the capture probability (i.e., lower defect energetics) and cause this level to metastably trap an electron forming an interface dipole, similar to what is commonly observed in the SiO_2/Si interface [12, 34, 137]. Furthermore, again consistent with inferences for near-interfacial SiO_2 [62, 137], strain can cause an oxygen vacancy $0/-$ acceptor level to lower significantly in energy from the upper region of the oxide band gap to lie closer to mid gap. An electron trapped in such an acceptor level would be consistent with the middle noise peak ($\approx$0.40 eV) in Figure 5.13 that only appears after irradiation under all bias conditions. Furthermore, the almost complete ("-1V" and "+1V") or partial ("0V") decrease in magnitude after annealing is consistent with the level emptying and shifting slightly higher after release of trapped holes in HfO_2 as evidenced by the corresponding change in V_{th}. The $V_{3-O,2}$ vacancy also has a $0/-$ acceptor level which can localize an electron but nominally sits energetically slightly above the Al_2O_3 band edge. Like the $V_{3-O,1}$ acceptor level, this level may also be pulled down by strain. No stable $0/-$ acceptor level was found for the V_{4-O} microstructure.

The low-frequency noise measurements show two additional peaks around $\approx$0.25 eV and $\approx$0.8 eV present during both pre- and post-irradiation measurements. In our Al_2O_3 model, all three oxygen vacancy configurations possess occupied $2+/0$ donor states. For the $V_{3-O,2}$ and V_{4-O} vacancies, these levels are 1.13 eV and 1.09 eV below the InGaAs CB (Figure 5.15). Emission of electrons from this level to the Fermi energy near the InGaAs CB is consistent with the higher energy observed peak in low-frequency noise, but not the lowest energy peak.

5.3.4 GaAs defects

In the present devices, the FinFET structure sits on a GaAs strain-relaxed buffer layer (SRB) between the substrate and device (as shown in Figure 5.1). The as-grown GaAs can contain several native point defects, i.e. gallium vacancies (V_{Ga}), arsenic antisites (As_{Ga}), arsenic vacancies (V_{As}), and gallium antisites (Ga_{As}). Due to strain mismatch with both the underlying silicon substrate and the InGaAs channel, this region will likely contain dislocations and increased formation of the native point defects. Since the channel is fully in contact with the SRB and the full device stack comes into contact around the lower edges, these defects in the GaAs may also contribute to the observed peaks in the low-frequency noise.The calculated levels for these defects are summarized in Figure 5.15.

From the calculations, the most likely defect candidate levels for the peak at ≈0.25 eV is the electron capture by the nominally unoccupied V_{Ga} $2-/3-$ level which sits 0.27 eV above the InGaAs CB. Emission from the AsGa $2+/+$ level which sits 0.40 eV below the InGaAs CB is also plausible [202],[203]. This peak could also be caused by electron capture by the V_{As} at 0.36 eV above the InGaAs CB. However, Ga-site defects are generally more commonly observed than As-site defects in GaAs. GaAs defects are unlikely to account for the higher energy noise peak.

5.4 Discussion

Consistent with previous work on similar devices [151], InGaAs FinFETs in this work show negative threshold voltage shifts during irradiation, indicative of net positive oxide-trap charge buildup [150, 151]. From Figure 5.3(b), the degradation is almost insensitive to channel length, while it is sensitive to the bias applied during the irradiation (Figure 5.3(a)). Worst case degradation of V_{th} is in "-1V" and "+1V"-biased devices. The highest tolerance of "0V"-biased transistors is more likely due to the limited charge yield obtained by the low applied electrical field into the gate oxide [103]. In all devices, the increase of the leakage current with cumulative dose (Figure 5.4) is caused by the increase of $I_d - V_{gs}$ stretchout and by the positive charge buildup in the STI oxides, which depletes the lateral corner region close to the STI, consequently forming a parasitic channel path between the drain and source [37, 38, 98].

The relatively small decrease in transconductance during irradiation indicates modest increase of the carrier scattering, suggesting only small buildup of interface traps along the Al_2O_3/InGaAs interface. Hence, the large increases in $I_d - V_{gs}$ stretchout when devices are irradiated appear to be due to border traps [172]. This interpretation is consistent with the large increase in low-frequency noise with irradiation, which is also a signature of an increase in border-trap density [63, 137].

As shown in Figure 5.13, the low frequency noise measurements at several temperatures reveal the generation of a defect energy peak at activation energy around ≈0.5 eV in all devices, regardless of the bias condition. After high temperature annealing, the $I_d - V_{gs}$ shifts recover and this noise peak decreases in magnitude, indicating full or partial deactivation of these border traps. Interestingly, the highest V_{th} recovery during the annealing is measured in the "-1V"-biased transistors (Figure 5.3), which concurrently exhibits a complete recover of the energy peak at 0.5 eV. On the contrary, modest recovery of the V_{th} is measured in the "0V"-biased transistors, showing accordingly a slight decrease of the energy peak in Figure 5.13(b).

By combining DFT calculations with the experimental measurements, it is clear that different defects can contribute to the DC and noise measurements depending on their spatial position, defect nature, and energetics. Oxygen vacancies in HfO_2 dielectrics are responsible for the negative V_{th} shifts during irradiation (Figures 5.2 and 5.3) and

subsequent recovery of V_{th} after annealing at 400 K (Figure 5.3). Indeed, the donor levels of HfO_2 oxygen vacancies sit energetically below the InGaAs conduction band. These levels are initially neutral, and, during X-ray irradiation, net hole trapping occurs in the HfO_2, with the Al_2O_3 serving primarily as a tunnel barrier. Due to their distance from the InGaAs channel, the HfO_2-based defects are unable to account for the observed $1/f$ noise in the measured frequency span, and are considered very slow defects that can be also responsible of hysteresis in the $I_d - V_{gs}$ of Figures 5.5-5.7.

On the other side, defects in the Al_2O_3 layer are primarily responsible for the peaks in noise magnitude in Figure 5.13. As shown by the DFT calculation of Figure 5.15, O vacancies in Al_2O_3 induce deep acceptor levels. These defects can participate in the noise during the irradiation as their defect energetics can be lowered to near mid gap by the effects of hole trapping in the HfO_2 and by interfacial and irradiation-induced strain. Additional noise peaks often present during all three testing conditions (i.e., pre-irradiation, post-irradiation, and post-annealing) which can be attributed to Al_2O_3 O vacancy levels and GaAs defects.

5.5 Second-generation InGaAs FinFETs with improved performance

A second-generation of the InGaAs FInFET was developed and produced with an improved production process, aimed to increase the performance of the transistors. The TID response of the new InGaAs FinFETs with an improved gate stack was tested at different gate lengths with 10-keV X-rays under different gate biases. Their radiation responses are compared to those of first-generation [27] presented in the above sections, showing interesting changes on the TID sensitivity. Indeed, in second-generation devices the radiation-induced-hole trapping is markedly reduced with a larger ratio of electron trapping to hole trapping than in first-generation InGaAs FinFETs. The improvement of the radiation tolerance is attributed to modifications in the gate dielectric, removal of tungsten from the top of the gate stack, and changes to the buffer layer materials.

5.5.1 Changes on second-generation devices

The second-generation InGaAs FinFETs are fabricated by the same foundry and a comparison with the previous first-generation structure is shown in Figure 5.16. The following changes in the materials and layout have been carried out:

1. The epitaxial process has been improved by changing the buffer layer below the active fin from GaAs to $In_{0.3}Ga_{0.7}As$.

2. The gate dielectric stack has been changed from 2 nm HfO_2/2 nm Al_2O_3 to 3 nm HfO_2/1 nm Al_2O_3.

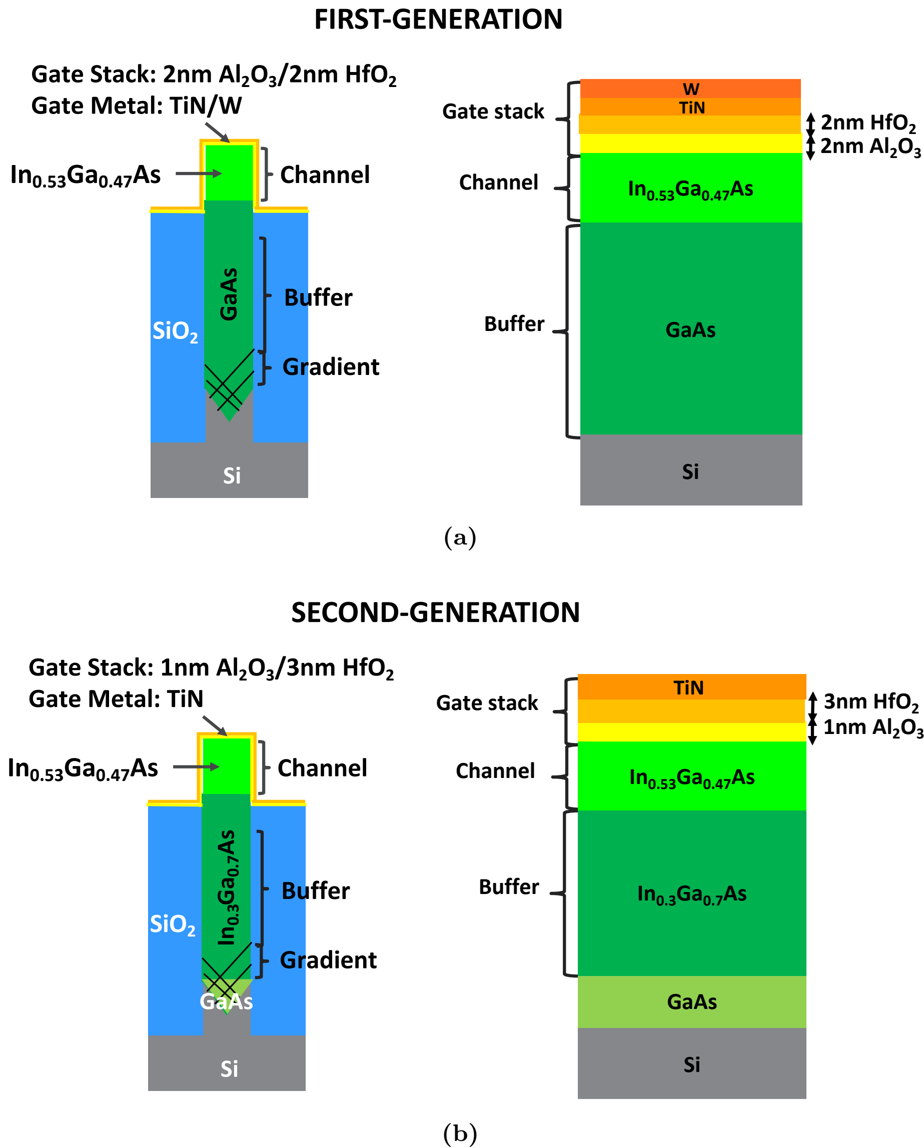


Figure 5.16: Schematic illustration of the InGaAs FinFET structures and of the material layers used in the (a) first-generation and (b) second-generation devices. (After [153])

3. The tungsten layer over the TiN has been removed in the second-generation devices.

The new lot is irradiated with identical conditions of first-generation lot with room temperature irradiations through 10-keV X-rays at a dose rate of 30.3 krad(SiO_2)/min. After the irradiation, the devices are annealed at room temperature for 1 hour. During the irradiations and annealing tests, the gate is biased at "+1V", "0V" and "-1V". Current-voltage (I_d-V_{gs}) responses are measured in the linear region with V_d = 50 mV using a semiconductor parameter analyzer (HP 4156). Tested devices have channel length ranging from 50 nm to 500 nm with fin width of 16 nm and fin height of 15 nm. The results about the radiation-induced parametric shifts are presented as the average of the TID response of a minimum of three devices, showing responses varying less than 15%.

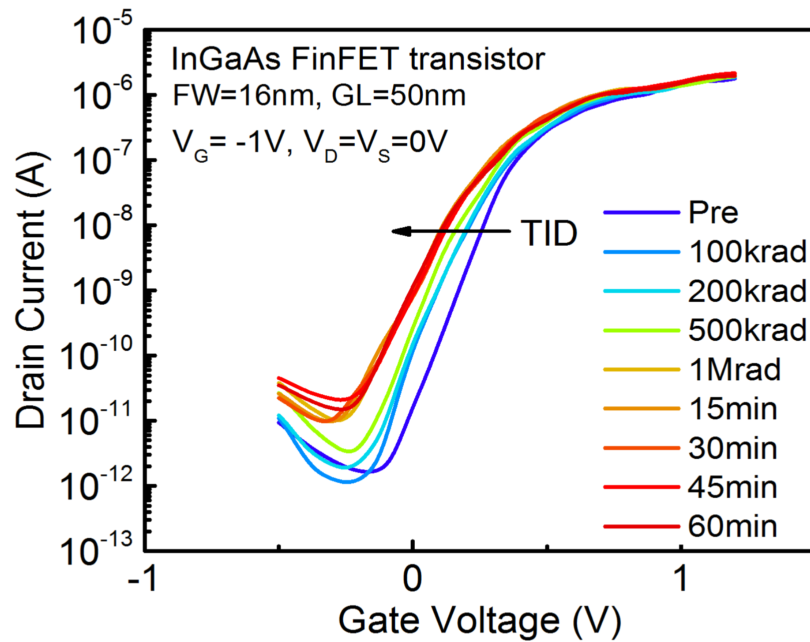


Figure 5.17: I_d-V_{gs} characteristic of second-generation InGaAs FinFET with gate length of 50 nm. The device was irradiated up to 1 Mrad(SiO_2) and annealed at room temperature up to 1 hour with the "-1V" bias condition. (From [153])

5.5.2 TID response of second-generation devices

Figure 5.17 shows the I_d-V_{gs} for the second-generation devices with channel length of 50 nm, irradiated and annealed in "-1V" bias conditions. Pre-rad devices exhibit improved performance respect to the first-generation devices, whose I_d-V_{gs} have been previously shown in Figure 5.2. The pre-rad leakage current is $\sim 10^{-12}$ A versus $\sim 10^{-9}$ A of first-generation devices. Consequently, the pre-rad ON/OFF ratio also improves with a ON/OFF ratio $\sim$ 100 times greater than first-generation devices. One possible reason of the improvement of the second-generation in the pre-rad performance is related to material change in the the buffer layer from GaAs to $In_{0.3}Ga_{0.7}As$, which has reduced the mismatch between the channel and the sub-fin region. During the irradiation, the I_d-V_{gs} shifts negatively with an increase of the leakage current and of the subthreshold stretchout, similar to the first-generation TID response showed in Figure 5.2. Qualitatively, the TID degradation of second-generation devices is similar to the first-generation ones, but by comparing Figures 5.17 and 5.2 the TID sensitivity of the second-generation devices is smaller than of first-generation devices.

In order to analyze the TID parametric shifts induced in the second-generation InGaAs FinFETs, Figure 5.18 shows the threshold voltage shift as a function of cumulated dose. The devices have a gate length of 90 nm and are irradiated and annealed in several bias conditions. The worst-case degradation is found in the "-1V" bias condition, which induces a V_{th} degradation of $\sim$ -900 mV after 1 Mrad(SiO_2). Surprisingly, the "+1V" is here the best case with almost a negligible degradation, less than -10 mV after

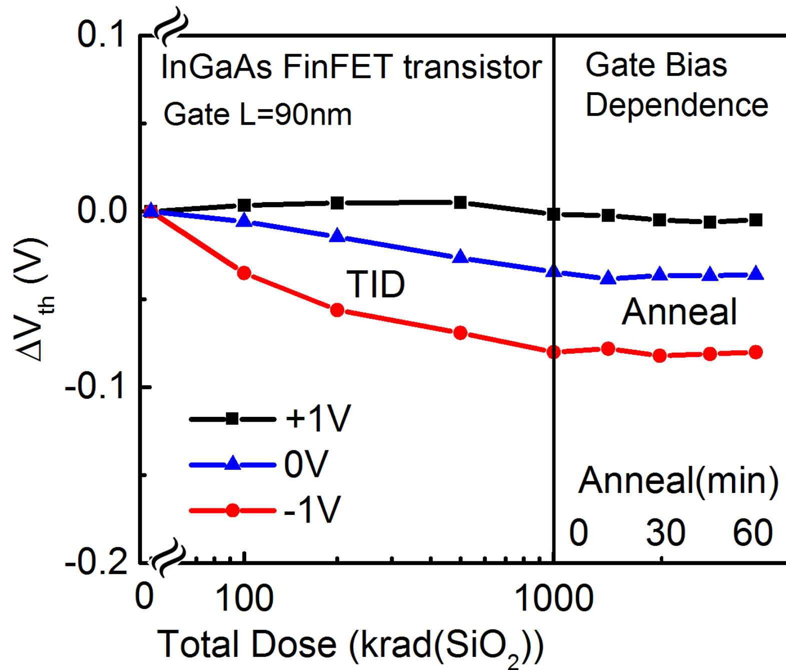


Figure 5.18: The V_{th} shift for second-generation InGaAs FinFETs with gate length of 90 nm. Devices were irradiated up to 1 Mrad(SiO_2) and annealed at room temperature up to 1 hour in the "-1V", "0V" and "+1V" bias conditions. (From [153])

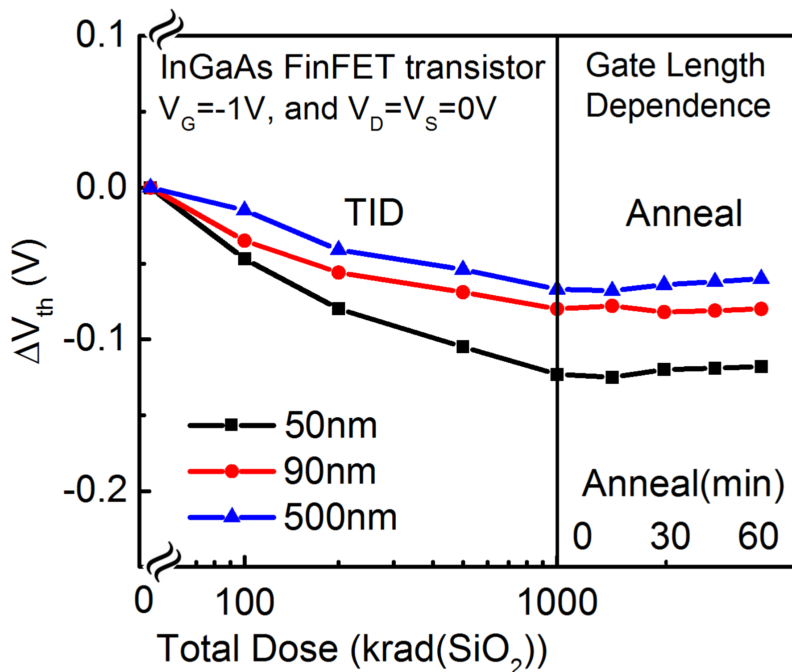


Figure 5.19: V_{th} shifts for second-generation InGaAs FinFETs with gate lengths varying from 50 nm to 500 nm. Devices were irradiated up to 1 Mrad(SiO_2) and annealed at room temperature up to 1 hour in the "-1V" bias condition. (From [153])

1 Mrad(SiO_2). In general, the V_{th} decreases with cumulated dose, indicating net positive charge trapping in the gate dielectric layers, and it remains approximately constant during the room temperature annealing.

During the "+1V" irradiations, since the tunneling probability depends exponentially on oxide thickness [12, 56], the reduction of the Al_2O_3 thickness facilitates electron tunneling into the HfO_2, consequently assisting the neutralization of radiation-induced trapped holes in HfO_2 [14, 204, 205]. Instead, during "-1V" bias irradiations, radiation-induced holes generated in the Al_2O_3 are drifted by the electrical field into the HfO_2 [169, 204, 205], increasing the TID effects related to positive trapped charges in the gate stack.

Figure 5.19 shows the V_{th} shifts for second-generation InGaAs FinFETs designed with several gate lengths, 50 nm, 90 nm, and 500 nm. The devices were irradiated up to 1 Mrad(SiO_2) and annealed at room temperature in the "-1V" bias condition. The V_{th} shifts increases by decreasing the channel length, indicating larger TID sensitivity in short channel transistors. The increased V_{th} shift in short channel devices indicates larger interface or border trap densities generated in short channel devices than long channel devices. This occurs because of the enhanced effects of radiation-induced charge trapping in the STI and/or SiO_2/Si_3N_4 spacers for short channel devices, relative to effects in longer channel devices, i.e., RISCE [37].

5.5.3 First-generation vs. second-generation TID responses

Figure 5.20 compares radiation-induced ΔV_{th} as a function of cumulated dose and annealing for first- and second-generation devices with channel length of 500 nm. Devices are irradiated and annealed in the "-1V" and "+1V" condition. At 500 krad(SiO_2), the ΔV_{th} in the "+1V" condition is $\sim$130 mV for first-generation devices and less than 10 mV for second-generation devices. Second-generation devices irradiated in the "-1V" shows typically a ΔV_{th} approximately 5-6 times larger than first-generation ones.

It is likely that a significant portion of the low TID sensitivity od second-generation TID response is related to the absence of tungsten over the TiN layer and to the reduced thickness of the Al_2O_3 layer in the gate stack. Therefore, based on previous experimental and computational studies [156, 157, 206], the tungsten in the gate stack enhances the cumulated dose delivered to the gate dielectric up to a factor of 3 or more. Finally, changes in the buffer layer from GaAs to $In_{0.3}Ga_{0.7}As$ and improvements in high-k deposition technologies likely also enhance the material quality and add to the above improvements in TID response.

5.6 Conclusions

The TID-induced degradation of the InGaAs FinFETs with HfO_2 and Al_2O_3 gate stack is dominated by hole trapping in the gate stack and in the shallow trench isolation,

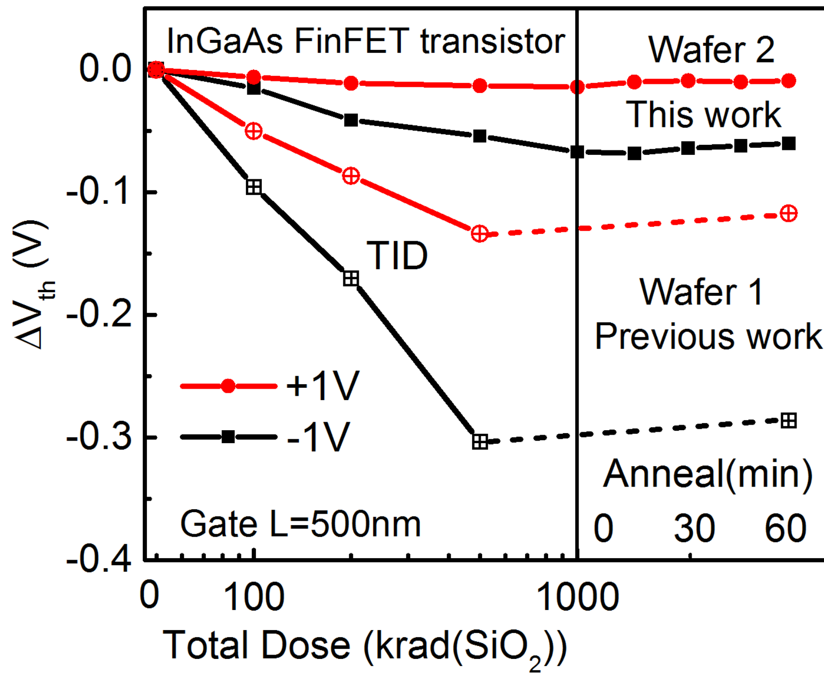


Figure 5.20: Comparison of the V_{th} shifts between from first-generation and second-generation InGaAs FinFETs as a function of dose and room temperature annealing time. Irradiation and annealing condition is "-1V" and "+1V". The devices have same geometry with gate length of 500 nm, fin width of 16 nm, and fin height of 16 nm. Dashed lines are used to indicate the final annealing results of first-generation devices, as they were irradiated only up to 500 krad(SiO_2). (From [153])

causing large negative V_{th} shifts, significant increases in subthreshold stretchout, and increases in leakage currents. I demonstrate through low-frequency noise measurements and DFT calculations that O vacancies in the HfO_2 are primarily responsible for the radiation-induced-hole trapping in the gate dielectric layers. Oxygen vacancies located in the Al_2O_3 layer contribute significantly to increased noise and sub-threshold stretchout. Additional contributions to the low-frequency noise and hysteresis may occur from other O vacancy levels and other point defects in the Al_2O_3 layer, as well as from defects in the GaAs SRB layer. These results illustrate the continuing sensitivity of devices based on III-V materials and high-k dielectrics to ionizing radiation, and emphasize the continuing need for process improvements in this important, developing technology.

A second-generation lot of InGaAs FinFETs with modifications into the gate dielectric and sub-fin buffer layers displays a significant improvement of the electrical performance with a higher radiation tolerance compared to previous first-generation InGaAs FinFETs. The removal of the tungsten in the second-generation lot from the gate stack reduces the dose enhancement. The worst-case bias condition is still observed for negative gate bias during irradiation, as a result of less compensation of hole trapping in the HfO_2 by electrons generated in the Al_2O_3. These results show that InGaAs FinFETs are becoming increasingly promising for future space applications of ultimately scaled MOS technologies.

Chapter 6

A Novel InGaAs MOSFET technology with high-k dielectrics

Indium gallium arsenide (InGaAs) has received increasing attention as channel material in n-type FETs, due to its improved electron mobility, leading to higher device performance for high-speed and low-voltage applications [27, 148]. The interest on the evaluation of the TID effects on InGaAs devices is increasing in the last years.

The recent works [149–151] and the data on InGaAs FinFETs discussed in the previous chapter highlight significant issues for high-k dielectric-based InGaAs transistors exposed to ionizing radiation. In [149], the sensitivity to TID of InGaAs multi-fin capacitors was shown to be higher than for Si MOS capacitors and Ge multi-fin capacitors. High densities of TID-induced trapped positive charge and border traps were measured by capacitance-voltage and capacitance-frequency measurements. In [151] and in previous chapter [153, 207], the InGaAs FinFETs with HfO_2-over-Al_2O_3 gate stack showed a large negative threshold-voltage shift below 500 krad(SiO_2), similar to the responses of planar InGaAs MOSFETs [150] and InGaAs Gate-All-Around (GAA) MOSFETs with Al_2O_3 gate dielectrics [208]. For planar InGaAs MOSFETs, worst-case response is found in the shortest gate-channel device with negative gate bias applied during irradiation [150].

In this chapter, I show the experimental results about the TID sensitivity of InGaAs-based MOSFETs. The MOSFETs in a new development-stage InGaAs fabrication process are irradiated and annealed at high temperature under several gate bias conditions. The TID response is characterized via DC static measurements for different channel dimensions, which are not highly scaled in order to focus the studies on the material and device structure quality. Negative gate bias during exposure is found to be worst-case for threshold-voltage shifts and ON/off ratios, due to enhanced hole trapping in the Al_2O_3 dielectric. Positive bias is worst-case for the subthreshold slope degradation, due to enhanced interface-trap buildup. Hysteresis and I_d-V_{gs} measurements from cryogenic to high temperatures show the important role of defects in the Al_2O_3 gate dielectric to the TID response. Analysis of the temperature dependence of V_{th} and SS suggests that rate at

which electrons leave the Al_2O_3 during a positive-to-negative gate-bias sweep is higher than the rate at which they enter during negative-to-positive gate-bias sweep. Finally, due to the large dimensions of the transistors, low-frequency noise measurements is dominated primarily by contact noise.

The work presented in this chapter has been supported by: AFRL and AFOSR through the Hi-REV program, DTRA through its Basic Research program, Department of Defense's High Performance Computing Modernization Program, and by the McMinn endowment at Vanderbilt University.

Most of the results and figures presented in this chapter have been published and/or submitted in the following peer-reviewed publications:

- [152] S. Bonaldo, E. X. Zhang, S. E. Zhao, V. Putcha, B. Parvais, D. Linten, S. Gerardin, A. Paccagnella, R. A. Reed, R. D. Schrimpf, and D. M. Fleetwood, "Total-ionizing-dose Effects in InGaAs MOSFETs with high-k Gate Dielectrics and InP Substrates," in *IEEE Transactions on Nuclear Science.* (Accepted for RADECS 2019 conference, Montpellier, France, and currently submitted for publication in IEEE Transactions on Nuclear Science).

Moreover, the results have been presented at the following international conferences:

- Radiation Effects on Components and Systems - RADECS 2019, Montpellier, France, 16th-20th September 2019, oral presentation about "Total-ionizing-dose Effects in InGaAs MOSFETs with high-k Gate Dielectrics and InP Substrates". (I was the presenting author)

6.1 Devices and experiments

6.1.1 Device description

The devices under test are manufactured in a InGaAs process, which can be used to fabricate MOSFETs and MOS-HEMTs with the same masks [209, 210]. The tested transistors have the MOSFET structure shown in Figure 6.1. These are development stage devices that are not highly scaled to enhance yield and facilitate characterization of the material and device quality. The $In_{0.53}Ga_{0.47}As$ channel layer is 10 nm thick and unintentionally n-doped, allowing the device to work in accumulation mode. The gate stack is formed by 10 nm of Al_2O_3, with an equivalent oxide thickness of $\sim$ 5 nm. The channel width (W) is 10 μm; several channel lengths (L) ranging from 5 μm to 50 μm are available. Transistors are bonded in a customized package [154] with separate gate, source, and drain and no ESD protection.

6.1.2 Irradiation conditions and measurements

Irradiations were performed at room temperature at Vanderbilt University using an ARACOR Model 4100 X-ray irradiator, composed of a tungsten tube with peak energy deposition at 10 keV [14]. The dose rate was 30.3 krad(SiO_2)/min. Devices are irradiated at room temperature (RT) and annealed at 373 K at biases of "+1V" (V_{gs}=-1 V, V_{ds}=0 V), "0V" (V_{gs}=0 V, V_{ds}=0 V) or "+1V" (V_{gs}=+1 V, V_{ds}=0 V). Transistor DC responses are measured with a semiconductor parameter analyzer at RT. Measurements were performed on more than 10 devices. At least two devices of each type were evaluated for all experimental conditions. Nominally identical devices that are irradiated, annealed, and tested under similar conditions show DC parameter degradations that typically vary by less than ±10%. Typical results are shown below.

The threshold voltage V_{th} is calculated as V_{gs-int} - $V_{ds}/2$, where V_{gs-int} is extracted in the linear region (V_{ds} = 50 mV) as the gate-voltage axis intercept of the linear extrapolation of the I_d-V_{gs} curve at the point of its maximum first derivative. I_d-V_{gs} hysteresis measurements were performed from 80 K to 320 K, enabling the estimation of the effective border-trap density [159, 211]. The low-frequency $1/f$ noise [137] was measured in a frequency span between 1 Hz and 400 Hz in the linear region (V_{ds} = 50 mV) at several values of $V_{gt} = V_{gs} - V_{th}$ and different temperatures.

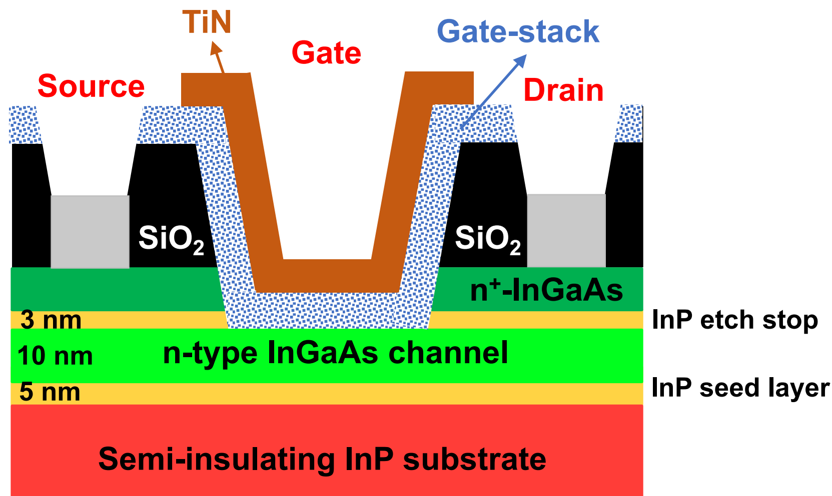


Figure 6.1: Schematic diagram of InGaAs MOSFETs in a cut-plane along the channel length. (From [152])

6.2 Experimental results

6.2.1 DC static characterization

Figure 6.2 plots I_d-V_{gs} curves for InGaAs MOSFETs, irradiated up to 2 Mrad(SiO_2) and annealed for 1 hour at 100 °C in the "-1V", "0V" and "+1V" bias conditions. The

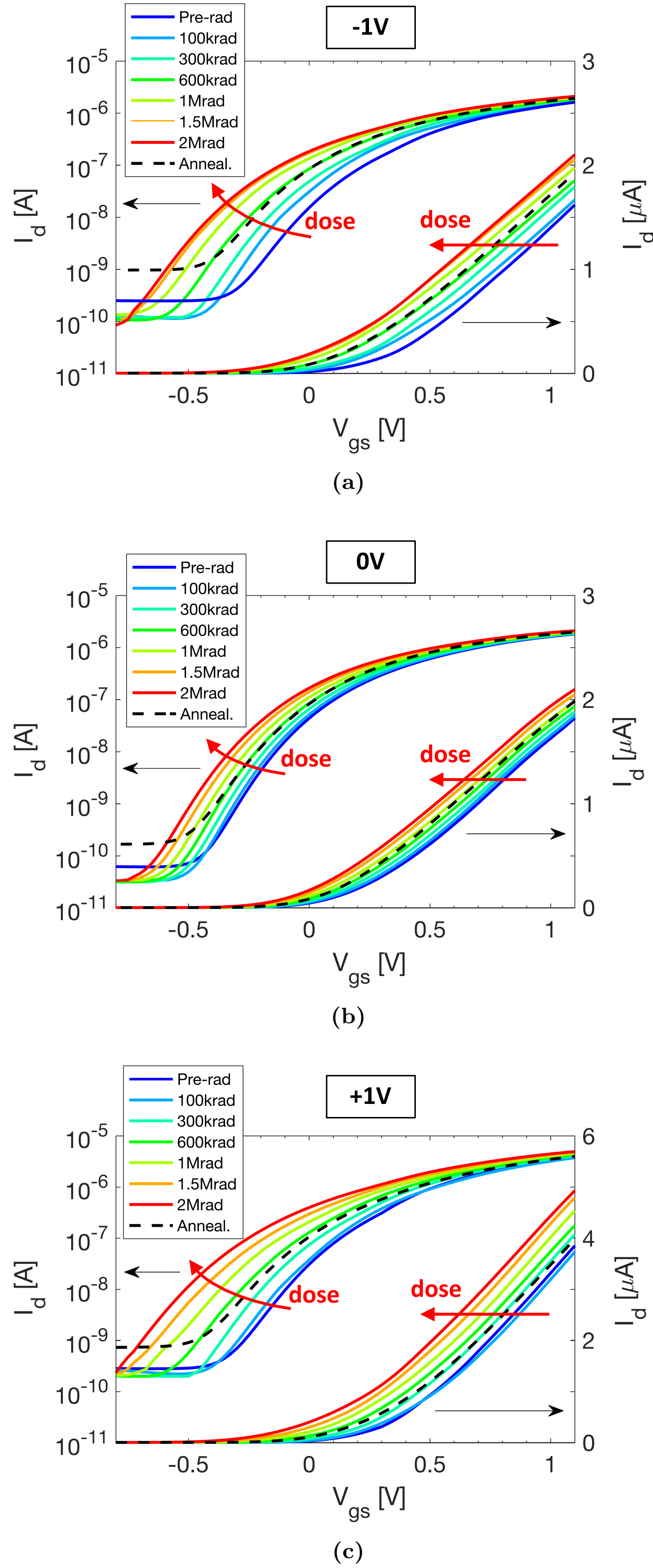


Figure 6.2: I_d-V_{gs} curves in the linear region (V_{ds} = 50 mV) for InGaAs MOSFETs with (a) and (b) L = 10 μm, and (c) L = 5 μm. Transistors were irradiated at room temperature up to 2 Mrad(SiO_2) and annealed for 1 hour at 100 °C in three different bias conditions: (a) "-1V" (b) "0V" and (c) "+1V". All measurements were carried out at room temperature. (After [152])

measurements were carried out at RT in the linear region with V_{ds} = 50 mV. After irradiation, devices show large negative shifts, indicating net positive oxide-trap charge buildup. Subthreshold stretchout occurs in all bias conditions due to increases in interface and border-trap densities [63, 151, 159, 211]. "+1V"-biased transistors show the most stretchout, e.g., 30 mV/dec vs. 10 mV/dec for "0V"-biased transistors. Drive current increases by 37% in the "-1V"-biased transistors, by 31% in "+1V"-biased transistors, and 19% in the "0V"-biased devices.

Note also in Figure 6.2 that the (fully) off-state leakage current at V_{gs} = 0.8 V decreases abruptly in the first few krad(SiO_2) of irradiation. The magnitude of this decrease in leakage varies from device-to-device, and occurs for most devices regardless of irradiation bias. This abrupt leakage decrease is caused most likely by the rapid neutralization of process-induced charged defects at the back-side interface between the semi-insulating InP layer and the InGaAs channel and/or in the shallow trench isolation oxides (STI) [37, 39, 212, 213]. After this fast charge neutralization, the leakage current is insensitive to dose.

After 1 hour annealing at 100 °C, devices partially recover, with positive shift of the V_{th}. The off-state leakage increases by about one order of magnitude, regardless of the applied bias. The largest recovery of the V_{th} occurs for "+1V"-biased transistors. This increase is mostly likely due to neutralization of trapped positive charges combined with interface-trap buildup, whose generation is enhanced under positive applied bias [149, 151]. The increase of the leakage current is probably related to the generation of additional interface traps at the gate-STI boundary [37, 39].

Figure 6.3 summarizes (a) the threshold voltage shift, (b) maximum transconductance degradation, and (c) variation of the subthreshold in MOSFETs as functions of dose, bias condition, and channel length. All devices were irradiated at RT to 2 Mrad(SiO_2) and annealed for 1 hour at 100 °C. At 2 Mrad(SiO_2), values of ΔV_{th} are -0.36 V, -0.25 V, and -0.17 V for irradiations at "-1V", "+1V" and "0V", respectively. Worst-case ΔV_{th} is for "-1V"-biased transistors, while the "0V" bias condition leads to the smallest shifts. The degradation of g_m is less than 10% in the "+1V" and "-1V" conditions, and negligible in the "0V" condition. The SS increases with dose. After 2 Mrad(SiO_2) irradiation, the largest ΔSS degradation is for the "+1V" irradiation, due to enhanced interface-trap buildup at the gate/dielectric interface [12, 14, 34].

Figure 6.3(d) shows changes of the I_{on}/I_{off} ratio (here defined as I_{on} at V_{gs} = 0.6 V and I_{off} at V_{gs} = 0.4 V) for transistors with different channel lengths. For InGaAs MOSFETs, the differences between L = 10 μm and L = 5 μm are negligible. After 2 Mrad(SiO_2), I_{on}/I_{off} = 800 for 50 μm devices and I_{on}/I_{off} = 200 for 10 μm devices.

6.2.2 I_d-V_{gs} measurements: hysteresis effects

The hysteresis in the I_d-V_{gs} curves is analyzed to study the slow charge trapping/detrapping response of the devices [63, 158] and estimate the effective density of

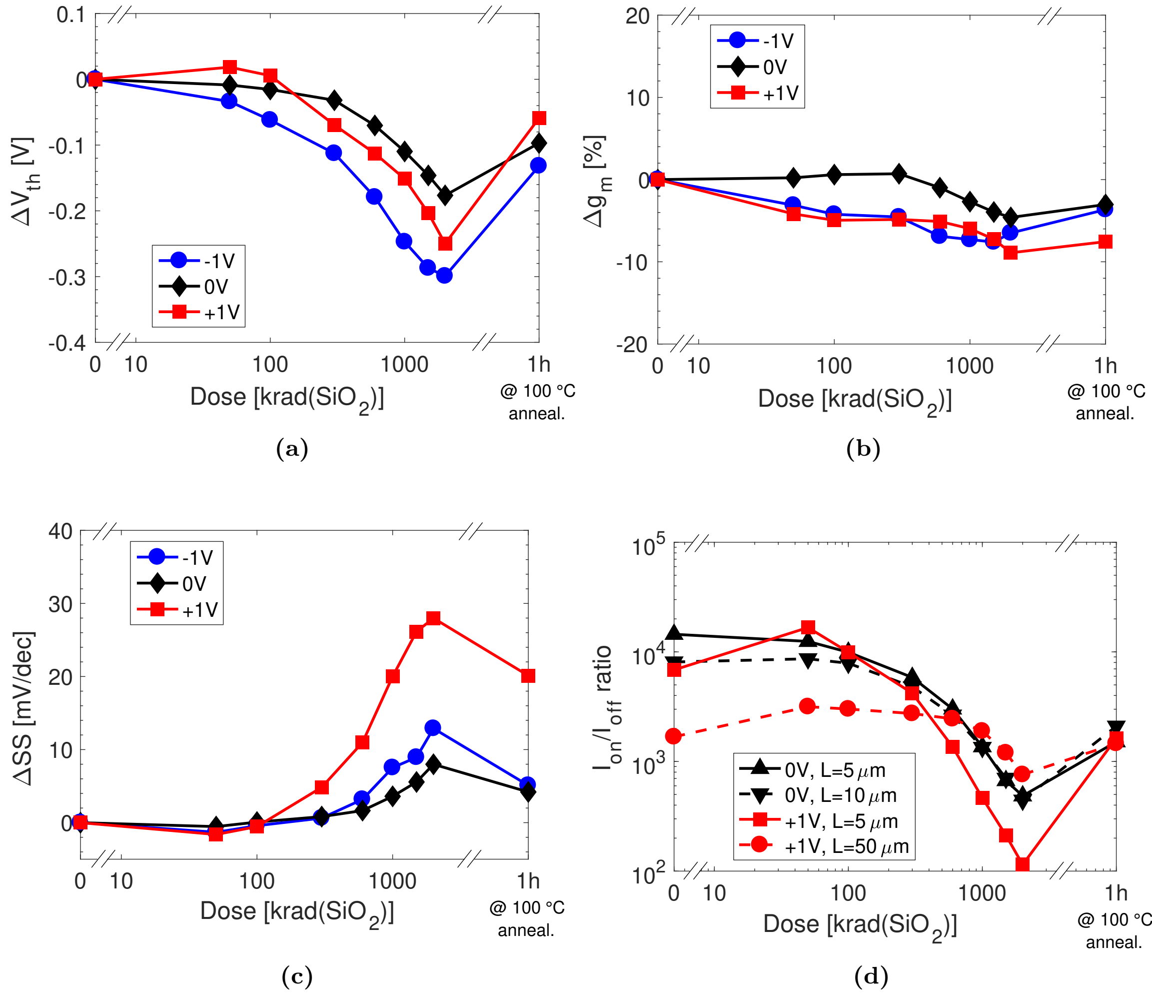


Figure 6.3: (a) Threshold voltage shifts, (b) maximum transconductance degradation, and (c) change in subthreshold swing for InGaAs MOSFETs irradiated and annealed in the "-1V", "0V" ($L = 10$ μm), and "+1V" (L = 5 μm) bias conditions. The SS is calculated in the subthreshold I_d range between 3 x10^{-9} A and 1 x10^{-8} A. (d) ON/off ratios for transistors with different channel lengths. (From [152])

slow border traps [159, 211]. The hysteresis is evaluated by performing two sweeps of the I_d-V_{gs} curves at a rate of $\sim$ 0.18 V/s. For the "BCK" (backward) mode sweep, transistors are biased at V_{gs} = -0.8 V for 10 s and then V_{gs} is quickly swept from -0.8 V to 1.1 V. For the "FWD" (forward) mode sweep, transistors are biased at V_{gs} = 1.1 V for 10 s, and V_{gs} is quickly swept from 1.1 V to -0.8 V.

Figure 6.4 shows I_d-V_{gs} curves in "BCK" and "FWD" modes before exposure, after 2 Mrad(SiO_2), and after 1 hour annealing at 100 °C for "+1V"-biased InGaAs MOSFETs. Consecutive measurements alternatively in "BCK" and "FWD" modes overlap, indicating a stable defect population. Before exposure, after 2 Mrad(SiO_2), and after annealing, the "FWD" curves show larger V_{th} shifts than the "BCK" curves, due to the effects of slow border traps with capture/emission times on the order of a few seconds [159]. The higher

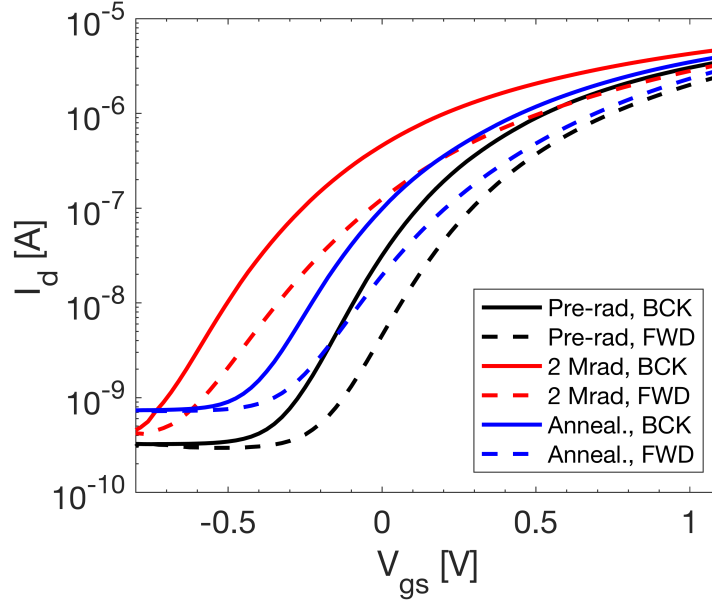


Figure 6.4: Hysteresis of the I_d-V_{gs} curves for InGaAs MOSFETs with $L = 5$ μm, irradiated up to 2 Mrad(SiO_2) and annealed for 1 hour at 100 °C in the "+1V" bias condition. The "BCK" label refers to V_{gs} sweeps performed from -0.8 V to 1.1 V; the "FWD" label refers to V_{gs} sweeps performed from 1.1 V to -0.8 V. (From [152])

V_{th} values for the "FWD" responses and the greater stretchout than in the "BCK" curves indicate that the hysteresis is caused by slow donor traps that are positively charged at low V_{gs} and/or slow acceptor traps that are negatively charged at high V_{gs} [63, 158].

In Figure 6.5, the V_{th} hysteresis ($V_{th-FWD} - V_{th-BCK}$) is plotted at room temperature as a function of dose for InGaAs MOSFETs irradiated under different bias conditions. On the right axis, the density of border traps N_{bt} is extrapolated in a first-order approximation by the relation [211]:

$$N_{bt} = \frac{\Delta V_H}{qC_{ox}} \tag{6.1}$$

where C_{ox} is the oxide capacitance ($C_{ox} = \epsilon_0 \epsilon_{SiO2}/t_{EOT}$) and ΔV_H is the hysteresis, defined as ΔV_H=$V_{th-FWD} - V_{th-BCK}$. The hysteresis increases with dose, as a result of increasing densities of slow traps with increasing dose [159]. Consistent with Figure 6.3(a), the worst-case hysteresis is found for the "-1V"-biased transistors, which exhibit an increase of the hysteresis from 180 mV to 345 mV after 2 Mrad(SiO_2), equivalent to an increase in the density of border traps N_{bt} from $\sim$ 8 x10^{11} cm^{-2} to $\sim$ 1.5 x10^{12} cm^{-2}. "0V"- and "+1V"-biased transistors are characterized by a hysteresis of 250 mV and 290 mV, respectively. During the annealing, the hysteresis decreases, indicating trap neutralization.

In Figure 6.6, the V_{th} hysteresis ($V_{th-FWD} - V_{th-BCK}$) and the density of border traps N_{bt} are plotted as a function of temperature for InGaAs MOSFETs irradiated at "+1V" bias to 2 Mrad(SiO_2) and annealed for 1 hour at 100 °C. On the right axis, the

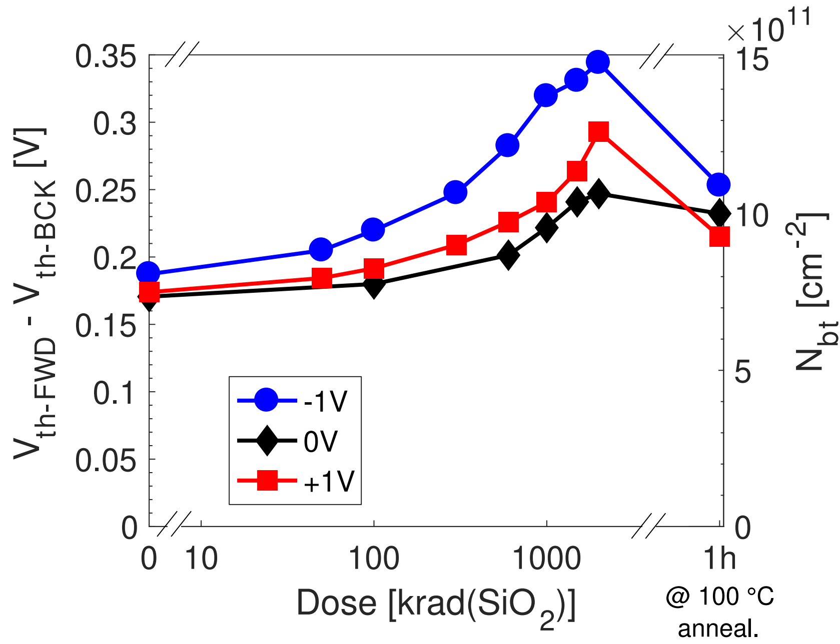


Figure 6.5: On left axis, the V_{th} hysteresis ($V_{th-FWD} - V_{th-BCK}$) and, on right axis, the effective density of border traps (N_{bt}) as a function of dose. Measurements were carried out at room temperature for InGaAs MOSFETs with $L = 5$ μm, irradiated up to 2 Mrad(SiO_2) and annealed for 1 hour at 100 °C under "-1V", "0V", or "1V" bias conditions. (From [152])

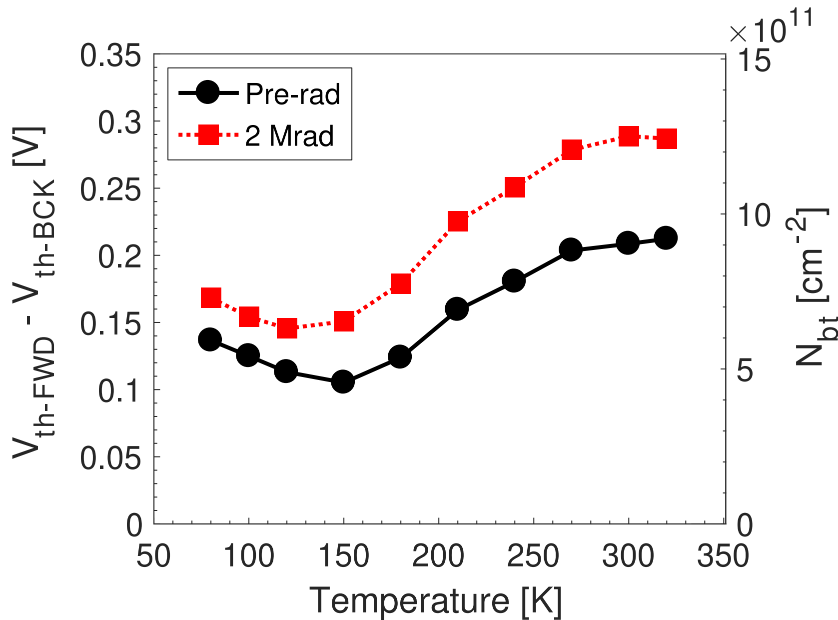


Figure 6.6: On the left axis, the V_{th} hysteresis ($V_{th-FWD} - V_{th-BCK}$) and, on the right axis, the effective density of border traps (N_{bt}) as a function of temperature. Measurements were carried out for InGaAs MOSFETs with $L = 5$ μm, before and after devices were irradiated to 2 Mrad(SiO_2) in the "+1V" bias condition. (From [152])

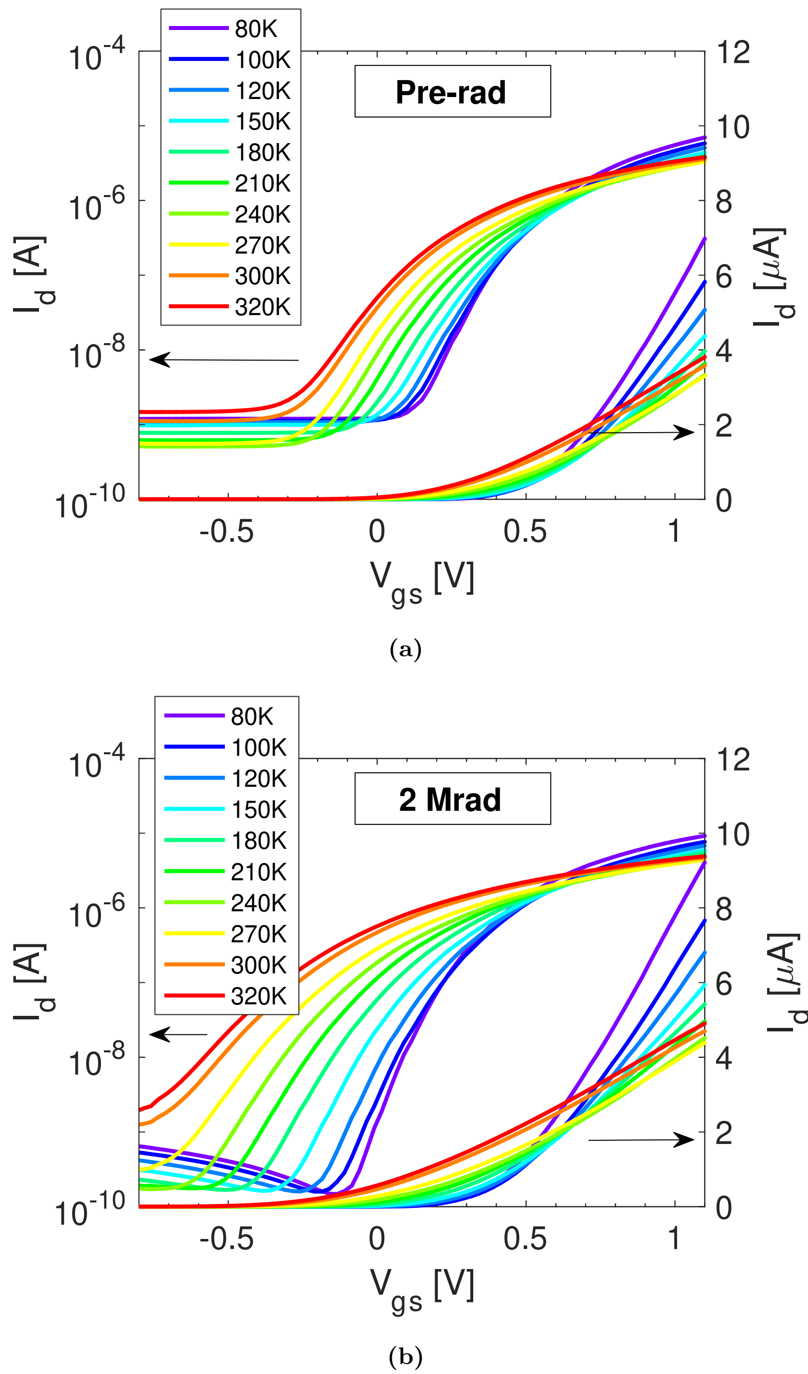
density of border traps N_{bt} is estimated via Eq. (6.1) The largest hysteresis is observed at high temperature after irradiation. The difference between the pre-irradiation and 2 Mrad(SiO_2) hysteresis is as low as $\sim$ 30 mV at 80 K and as large as $\sim$ 100 mV at 320 K. Although irradiation-induced defects add to the hysteresis, they do not significantly affect the temperature dependence. At low temperature ($T < 150$ K), the hysteresis decreases slightly with increasing temperature, most likely because charge can be exchanged with interface and border traps at higher rates when the temperature is raised [12, 159]. For 150 K $< T <$ 300 K, the hysteresis and effective density of border traps increases with temperature, suggesting an enhanced role for trap-assisted tunneling [57, 160].

6.2.3 DC response at cryogenic and high temperatures

Figure 6.7 shows I_d-V_{gs} curves in "BCK"-mode for values of T ranging from 80 K to 320 K for a "+1V"-biased device (a) before exposure and (b) after the device was irradiated to 2 Mrad(SiO_2). The off-state current generally increases with increasing temperature as a result of the thermal generation of carriers within the depletion region of the drain/bulk junction [161]. In Figure 6.7(b), the I_d-V_{gs} characteristics at 2 Mrad(SiO_2) show a large negative shift in V_{th} and increased SS at all temperatures, as compared with pre-irradiation values in Figure 6.7(a), due to radiation-induced buildup of trapped positive charges and border traps in the Al_2O_3 and traps at its interface with the InGaAs channel. After irradiation, the off-state leakage current decreases by about one order of magnitude, consistent with initial rapid neutralization of process-induced charged defects visible in Figure 6.2 [37, 39, 212–214].

Figure 6.8 shows values of (a) V_{th}, (b) g_m, and (c) SS as a function of temperature for these devices before exposure and at 2 Mrad(SiO_2). In Figure 6.8(a), V_{th} decreases monotonically with increasing temperature above $\sim$ 200 K. Above 200 K, the $V_{th} - T$ curve of as-processed devices is linear, with a slope of 2.5 mV/K for both "BCK" and "FWD" curves. This trend is similar to the response of Si-based MOSFETs, typically characterized by a slope between 2 and 4 mV/K depending on the density of the bulk doping [215, 216]. Below 200 K, the deviation from the linear trend is caused by changes in trap occupancy of pre-existing and radiation-induced defects, as well as the freeze-out of carriers due to the decrease of bulk acceptor concentration observed at cryogenic temperature [217, 218]. After irradiation, V_{th} decreases by $\sim$ -0.12 V at 80 K, and $\sim$ 0.31 V at 320 K.

Before irradiation, in Figures 6.8(b) and 6.8(c), values of g_m decrease and values of SS increase with increasing temperature due to enhanced phonon scattering [219] and the charging of process induced by interface traps. In both "BCK"- and "FWD"-modes, values of SS change significantly more with irradiation than do values of g_m. This strongly suggests that the additional increase in SS with irradiation above 150 K is due primarily to the charging of radiation-induced border traps. If it were instead due primarily to radiation-induced interface traps, one would have expected a much greater increase in g_m, since scattering rates are much higher from interface traps than from border traps



(a)

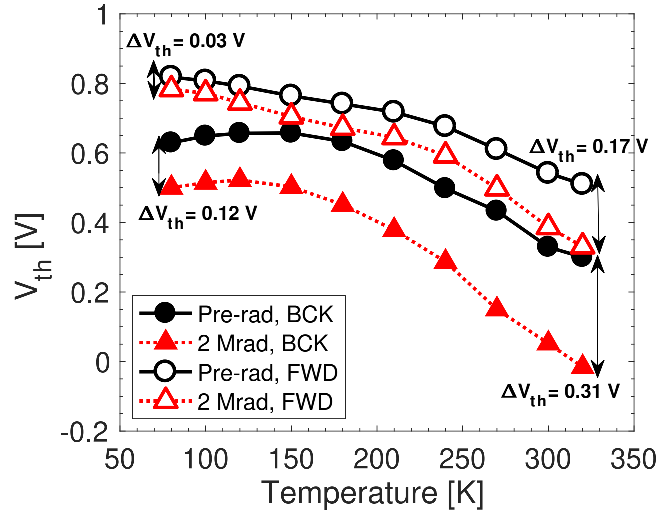
(b)

Figure 6.7: I_d-V_{gs} curves in "BCK"-mode vs. measurement temperature in the linear region of operation (V_{ds} = 50 mV) for InGaAs MOSFETs with L = 5 μm irradiated in the "+1V" bias condition: (a) before irradiation and (b) after irradiation to 2 Mrad(SiO_2). (From [152])

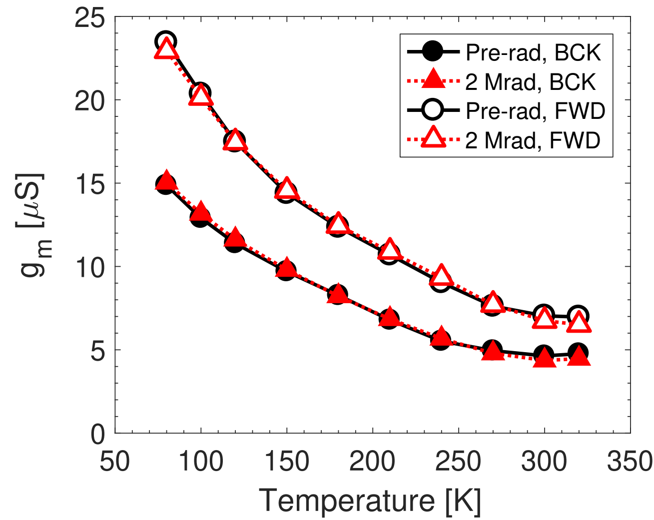
[63, 159, 211].

6.2.4 Low frequency noise at room temperature

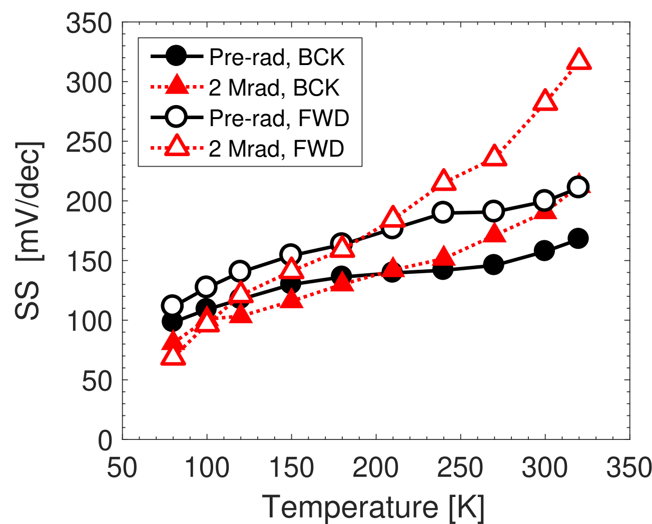
I carried out some low-frequency noise measurements at several gate voltages with the aim of investigating the energy distribution of border traps [137, 141, 142]. The excess



(a)



(b)



(c)

Figure 6.8: (a) Threshold voltage, (b) trasconductance, and (c) subthreshold swing in "BCK"- and "FWD"-modes as a function of temperature for InGaAs MOSFETs with $L = 5\ \mu$m irradiated up to 2 Mrad(SiO_2) in the "+1V" bias condition. The SS is calculated in the subthreshold I_d range between 2 x10^{-9} A and 5 x10^{-8} A. (From [152])

drain-voltage noise power spectral density S_{vd} can be expressed as a function of V_{gs} and f by the expression [137]:

$$S_{vd}(f, V_{ds}, V_{gs}) = KV_{ds}^2 f^{-\alpha}(V_{gs} - V_{th})^{-\beta} \tag{6.2}$$

where K is a constant factor indicating the normalized noise magnitude, α represents the exponential factor indicating the dependence with frequency, and β is the exponential factor indicating the dependence with $V_{gt} = V_{gs} - V_{th}$. It results that the excess drain-voltage noise power spectral density S_{vd} is proportional to $(V_{gs} - V_{th})^{-\beta}$ [137, 142]. When gate oxide defects are uniform in space and in energy within the range of the Si band gap, β is expected to be 2 [137, 142].

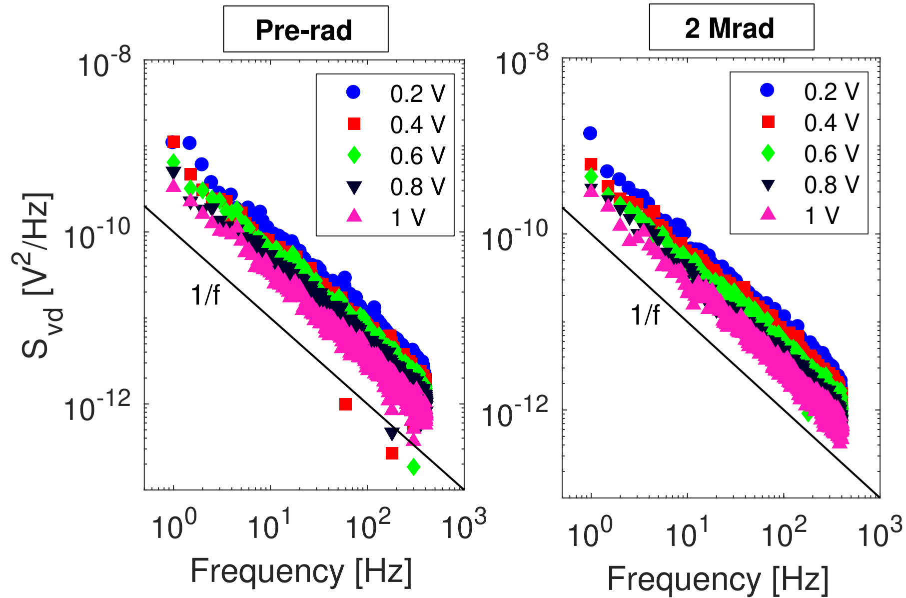
Figure 6.9(a) shows low-frequency noise at several values of $V_{gt} = V_{gs} - V_{th}$ for InGaAs MOSFETs before and after 2 Mrad(SiO_2) irradiation in the "+1V" bias condition. Before and after irradiation, the power spectrum shows the typical $\sim 1/f$ frequency dependence for all measured ranges of V_{gt}. Figure 6.9(b) plots the noise magnitude at $f = 10$ Hz as a function of the V_{gt} for two different devices irradiated in the "+1V" and "-1V" bias conditions. All measured noise of InGaAs MOSFETs is insensitive to dose, regardless of the bias condition. The value of applied gate voltage only modestly affects the noise; the slope ($|\beta|$) of the $S_{vd} - V_{gt}$ curves in is about ~ 0.4 at $V_{gt} < 0.5$ V and ~ 0.8 at $V_{gt} > 0.5$ V.

In FET devices, low-frequency noise is typically caused by random thermally activated processes related to trapping and detrapping process of electrons in the defects close to the oxide/semiconductor interface. Measurements of noise at several temperatures combined with the Dutta-Horn model [162] can give some insights into the defect-energy distribution, identifying the activation energy E_0 needed by the system to change the trap occupation [162]. The defect-energy distribution $D(E_0)$ can be obtained from measurements of the $S_{vd} - T$ through the relation:

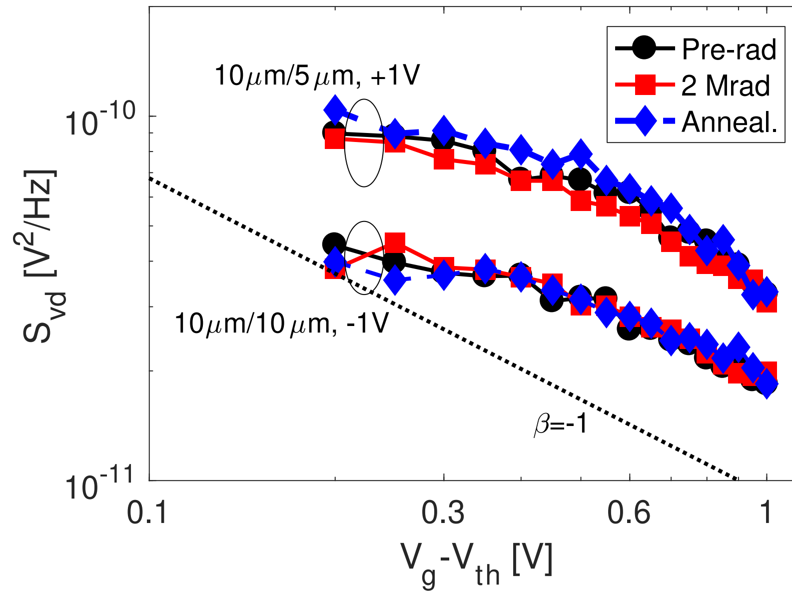
$$D(E_0) \propto \frac{2\pi f}{kT} S_{vd}(f, T) \tag{6.3}$$

Therefore, the defect-energy distribution $D(E_0)$ is proportional to excess drain-voltage noise power spectral density S_{vd} normalized by f/T. Figure 6.10 report the low-frequency noise normalized by f/T as a function of temperature. The noise refers to $f = 10$ Hz for InGaAs MOSFET irradiated in the "+1V"-bias condition. Figure 6.10 shows that the normalized S_{vd} is insensitive to temperature and does not evidence any peak formation in the noise spectrum.

The Dutta-Horn model has been used in several works to investigate the nature of defects in both Si- and InGaAs-based devices [137, 151, 166, 211]. When the Dutta-Horn model is valid, the $1/f^{\alpha}$ noise is related with frequency and temperature by the relation



(a)



(b)

Figure 6.9: (a) $1/f$ noise at several values of $V_{gt} = V_{gs} - V_{th}$ for InGaAs MOSFETs with $L = 5$ μm before and after irradiation in the "+1V" bias condition. Noise measurements were carried out at room temperature with $V_{ds} = 0.05$ V. (b) Noise magnitude at $f = 10$ Hz vs. V_{gt} for two different MOSFETs irradiated in the "+1V" and "-1V" conditions. Noise was measured at RT before irradiation, after exposure, and after 1 hour annealing at 100 °C. β is the slope of the $S_{vd} - V_{gt}$ curves.

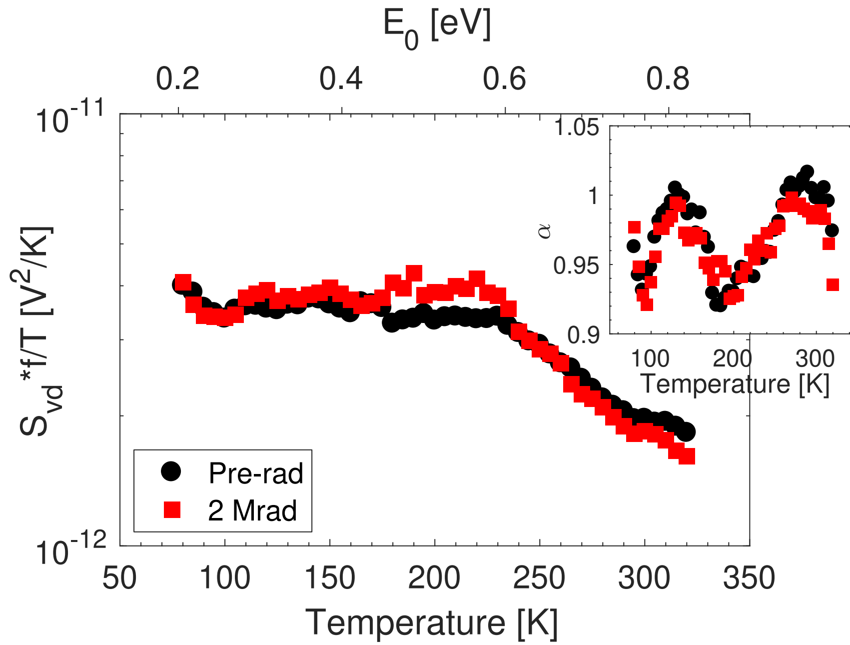


Figure 6.10: Normalized $1/f$ noise magnitude as a function of temperature for InGaAs MOSFETs biased at V_{ds} = 0.1 V and V_{gt} = 0.4 V. The noise was measured at f = 10 Hz before irradiation and after exposure to 2 Mrad(SiO_2) in the "+1V"-bias condition. The energy scale on the upper x-axis is derived from the Dutta-Horn model of $1/f$ noise with τ_0 = 1.8 x10^{-15} s, consistent with previous work on Si MOS devices [163]. The inset shows the experimental α as a function of temperature for the noise values of the main plot.

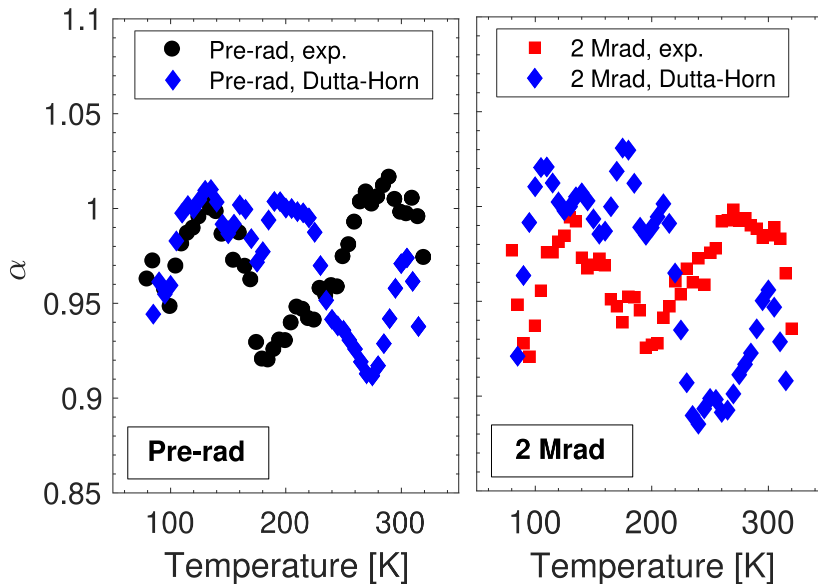


Figure 6.11: Alpha parameter for the InGaAs MOSFET shown in Figure 6.10. Transistor was irradiated up to 2 Mrad(SiO_2) in the "+1V" bias condition. Measured experimental α is compared with the one retrieved by the Dutta-Horn model: (a) before the exposure and (b) after 2 Mrad(SiO_2).

[141]:

$$\alpha(f,T) = 1 - \frac{1}{\ln(2\pi f \tau_0)} \left(\frac{\delta \ln S_{vd}(T)}{\delta \ln T} - 1 \right) \tag{6.4}$$

where τ_0 is the characteristic time of the process leading to the noise. Figure 6.11 compares the α parameter of experimental data shown in Figure 6.10 with the α values retrieved from the Dutta-Horn model via Eq. (6.3). The α values from the Dutta-Horn model are not in agreement with the experimental values, suggesting that low frequency noise in these devices is not dominated by effects of emission/capture of electrons in the border traps along the channel, but it is probably dominated by other noise sources like the contact noise.

6.3 Discussion

TID-induced degradation of InGaAs MOSFETs with 10 nm Al_2O_3 gate stacks is dominated by hole trapping in the gate stack, causing large negative V_{th} shifts, and significant increases in subthreshold stretchout. Negative charges trapped in the Al_2O_3 or in interface traps offset the net positive charges trapped in the Al_2O_3 dielectric, leading to higher TID tolerance in the "+1V" condition than in the "-1V" condition [12]. Hence, the worst-case TID response is observed for the "-1V"-bias condition, in which the electric field maximizes the hole trap-ping and minimizes the interface trap buildup at the oxide/channel interface. This result is consistent with previous studies on InGaAs FinFETs [151, 153, 207], planar devices [150], and GAA FETs [208]. In contrast, the largest subthreshold swing degradation is observed for "+1V"-irradiation bias, when interface-trap buildup is maximized, as a result of proton drift through the Al_2O_3 to the InGaAs/Al_2O_3 interface [12]. Transistors irradiated in the "0V" bias condition exhibit the least TID degradation due to enhanced electron-hole recombination at lower electric fields [14, 34, 147]. Only modest variations in TID response are observed as a function of channel length [90], but this will need to be further evaluated on devices with sub-μm length, for which radiation-induced short channel (RISCE) and narrow channel (RINCE) effects are more likely to be observed [37, 38, 90, 94].

The decrease of the V_{th} is consistent with radiation-induced hole trapping in oxygen vacancy defects, which are common in Al_2O_3 dielectrics [211, 220]. In HfO_2/Al_2O_3-based InGaAs FinFETs [211], 4-fold (V_{4-O}) or 3-fold ($V_{3-O,1}$, $V_{3-O,2}$) oxygen vacancies in bulk Al_2O_3 are characterized by 2+/0 donor traps, which energetically sit below the Fermi level [211]. Before irradiation, these defects are neutral. During exposure, these defects trap radiation-induced holes. Dangling Al bonds in the Al_2O_3 exhibit 0/- acceptor traps, with near midgap energy levels [187]. Such a defect can capture an electron under positive bias, and release the electron under negative bias. The capture probability and release rate will de-pend on distance to the interface [56, 63, 159] and detailed bonding configurations of nearby atoms [62, 221, 222], similar to what is observed in SiO_2. Hence, dangling Al bonds

may well account for most of the hysteresis observed in these devices.

The rate at which the values of V_{th} in Figure 6.8(a) decrease with the temperature depends on the emission and capture times of slow border traps [220, 223, 224]. The V_{th} decrease is most pronounced for devices swept in "BCK"-mode (negative to positive) sweep, and the increase in SS is most pronounced in the "FWD"-mode (positive to negative) sweep. Assuming these changes are associated with trap-assisted tunneling of electrons into and out of defects in the near-interfacial SiO_2, analogous to similar effects observed in Si MOS devices with SiO_2 and/or high-k dielectrics [60, 62, 137, 160, 221], these results imply that the rate at which these electrons leave the oxide (trap emission, sensed in the positive to negative sweep as increased SS during transport) is greater than the rate at which they enter (electron capture, sensed in the negative to positive sweep as decreased V_{th} before the trapping occurs). This further implies that capture and emission of electrons at border traps leads to reconfiguration and a change in energy of the defect, again consistent with effects observed in Si MOS devices with SiO_2 and/or high-k dielectrics [62, 142, 163, 222].

6.4 Conclusions

I have evaluated TID effects on development-stage In-GaAs MOSFETs with Al_2O_3 gate dielectrics. Irradiated devices show net positive charge buildup in the gate oxide and increases in interface and/or border-trap charge densities. Significant hysteresis is observed before and after irradiation. For all bias irradiation conditions, the TID effects are not significantly channel-length dependent in these large geometry devices. This result will need to be evaluated further for more highly scaled devices in future studies. The worst-case TID response is with the "-1V"-bias condition, in which the electric field maximizes the hole trapping and minimizes the interface trap buildup at the oxide/channel interface. Hysteresis and I_d-V_{gs} characteristics from cryogenic to high temperatures show large densities of border traps, pointing out the important role of defects in the Al_2O_3 gate dielectric to the TID response. Therefore, oxygen vacancies in the bulk Al_2O_3 primarily trap holes during irradiation. Dangling Al bonds near the interface can serve as acceptor defects, which can contribute to electron trapping and hysteresis. The rate at which electrons leave the Al_2O_3 during positive-to-negative gate-bias sweeps is higher than the rate at which they enter during negative-to-positive gate-bias sweeps. This result, as well as the temperature dependence of V_{th} and SS, strongly suggest that electron capture and emission have significantly different capture and emission times. The low-frequency noise is nearly constant with dose and do not show any peak formation in the spectrum of the $S_{vd} \cdot f/T - T$ during the irradiation, consistent with a significant contribution of contact noise.

Chapter 7

Conclusions

This thesis work explores the TID degradation mechanisms in several modern nanometer-scale technology nodes. By an extensive work of irradiation campaigns, I provide new insights about the influence of the technological scaling down to the TID effects of modern transistors. Toward this aim, devices produced from different manufacturers were irradiated with X-rays up to never-explored doses of 1 Grad(SiO_2) and, then, annealed at room and/or high temperatures. The parametric shifts in the electrical responses were measured by DC static characterizations, charge pumping and low frequency noise measurements, allowing to investigate the nature, locations, densities, and energetic levels of the TID-induced defects. The TID mechanisms were evaluated in five different technology nodes: 150 nm Si-based MOSFET, 65 nm Si-based MOSFET, 28 nm Si-based MOSFET with HfO_2 gate dielectric, 16 nm Si-based FinFET with HfO_2/Al_2O_3 gate dielectrics and

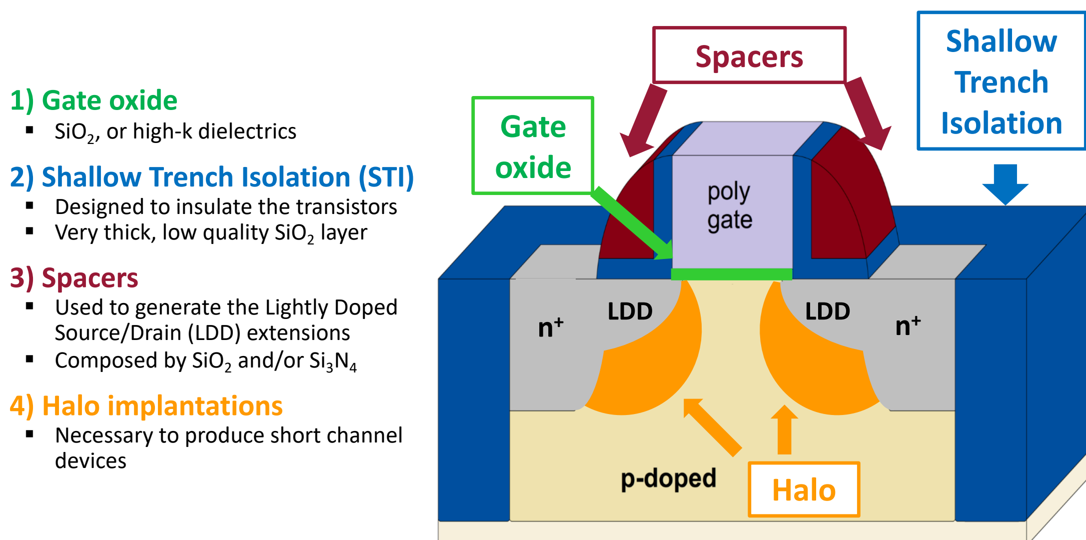


Figure 7.1: Schematic structure of a MOSFET summarizing the main elements that contribute to TID degradation. The TID effects in modern nanometer-scale transistors are influenced by: gate dielectric, shallow trench insulations oxides, spacer dielectrics, and halo implantations.

a new development-stage InGaAs MOSFET with Al_2O_3 gate dielectric.

The obtained experimental results show different dominating TID mechanisms, whose sensitivities depends on irradiation bias condition, channel length, and channel width. The density of trapped charge in the gate oxide is reduced thanks to the ultra-thin thickness of the gate dielectric of scaled technology nodes. However, with the further advance of the semiconductor industry, new TID-induced effects arise due to charge trapping in other thick oxides and to modern production processes. In Figure 7.1, the schematic representation evidences the main key elements which contribute to the TID degradation of modern transistors: gate stack, shallow trench isolation, spacers, and halo implantations.

Starting from the 150 nm Si-based MOSFETs, experimental results up to 125 krad(SiO_2) show that the worst TID degradation is in nMOSFETs, where a large negative shift of the threshold voltage and a very high leakage current indicate positive charge buildup in gate and STI oxides. The higher TID tolerance of core transistors than I/O transistors is due to the reduced thickness of the gate and STI oxides. Narrow transistors are the most TID tolerant. This channel-width dependance is related to the STI oxides and is know as Radiation-Induced Narrow Channel Effect (RINCE). A new channel-length dependance is also visible and it is most likely related to the halo implantations, which improve the TID tolerance of short transistors.

With the scaling down to the 65 nm Si MOSFET technology node, the charge trapping in the gate stack is negligible, thanks to the ultra-thin thickness of the gate dielectric. The TID degradation is dominated by the charge generation in the STI oxides, whose effects are suppressed in the enclosed layout transistors (ELTs). At ultra high-doses up to 1 Grad(SiO_2), a new Radiation-Induced Short-Channel Effect (RISCE) induces high degradation in short channel devices with charge buildup in spacer dielectrics and along

Technology nodes	Dominating TID effets			
	Gate stack	STI	Spacer	Halo
150 nm Si MOSFET	Medium	High	Low	Medium
65 nm Si MOSFET	Low	High	High	Low
28nm Si MOSFET with high-*k* gate	Low	High	Low	High
16 nm InGaAs FinFET with high-*k* gate	High	High	Medium	Not used
InGaAs MOSFET with high-*k* gate	High	Medium	Low	Not used

Figure 7.2: Dominating TID-induced degradation mechanisms are related to: gate dielectrics, shallow trench insulations (STI), spacers, and halo implantations. The table indicates how much each element influences the TID electrical response of each analyzed technological node.

its oxide/semiconductor interface. Through charge pumping measurements and TCAD simulations in p-channel ELTs, I prove that the density of radiation-induced interface traps is not uniform along the channel, and has a density peak close to the source region. The worst-case bias condition corresponds to high electric fields at drain and gate during the irradiation. Indeed, the applied electric field drives the radiation-induced protons from the source spacer to the source gate oxide corner, drifting them into the gate oxide dielectric, where they can generate high densities of interface traps close to the source region.

In 28 nm Si-based MOSFETs irradiated up to 1 Grad(SiO_2), the TID degradation of pMOSFETs depends again on the channel width (RINCE), featuring a new channel length dependence, opposite from the RISCE of 65 nm MOSFETs. Short-channel devices exhibit higher TID tolerance compared to long ones. Through DC static measurements and TCAD simulations, I show that this new effect is related to highly doped halo implantations. In short-channel devices, the drain halo can overlap the source one, consequently increasing the average bulk doping along the channel. Enhanced bulk doping attenuates the effects induced by charge buildup in the STI, improving the TID tolerance of short-channel transistors. At high doses ($\lesssim$ 100 Mrad(SiO_2)), the TID degradation mechanism is dominated by positive charge buildup in the STI, while, at ultra-high doses ($\gtrsim$ 1 Grad(SiO_2)), the TID degradation is dominated by interface trap buildup along the gate/channel interface and along the upper corner of the STI sidewalls.

In the 16 nm InGaAs-based FinFET generation, the production process uses the FinFET layout combined with a new InGaAs-channel material and a gate stack formed by HfO_2/Al_2O_3. Halo are not used in InGaAs technology. The experimental results show large negative threshold voltage shift, increases in subthreshold stretchout, and in the leakage current. TID degradation is dominated by hole trapping in the gate stack and in the shallow trench isolation. By combining experimental DC and noise measurements with DFT calculations, I demonstrate that oxygen vacancies in the HfO_2 are primarily responsible for the radiation-induced hole trapping in the gate dielectric layers, causing threshold voltage shift in the transistor response, while oxygen vacancies located in the Al_2O_3 layer contribute to the increase of noise and subthreshold stretchout. Additional contributions to the noise occur from As vacancies located in the GaAs buffer layer.

Finally, I investigate the TID mechanisms in a new laboratory-stage InGaAs MOSFET. Similar to the 16 nm InGaAs FinFETs, irradiated InGaAs MOSFETs show large negative threshold voltage shifts, increase of subthreshold stretchout and large hysteresis. Hysteresis tests and DC measurements from cryogenic to high temperatures suggest net positive charge trapping in the gate oxide with an additional generation of interface and border traps. The radiation-induced buildup of hole in the gate stack is attributed to oxygen vacancies in Al_2O_3. The observed hysteresis is most likely due to acceptor defects induced by dangling Al bonds in the near-interfacial Al_2O_3.

In conclusion, each technological node is influenced by one or multiple TID mech-

anisms, which can impact at different levels the TID electrical response of the devices. Figure 7.2 summarizes the dominating TID-induced degradation mechanisms in all analyzed technologies. The scaling down of the technological nodes has required a continuous change of materials, structures, processes, and layouts, inducing both advantages and disadvantages toward the TID sensitivity of transistors. If halo implantations and thin gate dielectrics improve the TID tolerance, on the other side the introduction of STI oxides, spacers, III-V materials and high-k dielectrics has enhanced the TID sensitivity of modern devices. The evolution of the fabrication processes in the semiconductor industry leads to an unpredictable trend in the TID effects, requiring continuous efforts in the testing and qualifications of the electronics, which keeps high the interest of the scientific community into the research of TID effects on electronic devices.

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