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Analysis and Design of a Transmitter for Wireless Communications in CMOS Technology

Tesi di

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Abstract

The number of wireless devices has grown tremendously over the last decade. Great technology improvements and novel transceiver architectures and circuits have enabled an astonishingly expanding set of radio-frequency applications.

CMOS technology played a key role in enabling a large-scale diffusion of wireless devices due to its unique advantages in cost and integration. Novel digital-intensive transceivers have taken full advantage of CMOS technology scaling predicted by Moore's law. Die-shrinking has enabled ubiquitous diffusion of low-cost, small form factor and low power wireless devices.

However, Radio Frequency (RF) Power Amplifiers (PA) transceiver functionality is historically implemented in a module which is separated from the CMOS core of the transceiver. The PA is traditionally dictating power and battery life of the transceiver, thus justifying its implementation in a tailored technology. By contrast, a fully integrated CMOS transceiver with no external PA would hugely benefit in terms of reduced area and system complexity.

In this work, a fully integrated prototype of a Switched-Capacitor Power Amplifier (SCPA) has been implemented in a $28\,nm$ CMOS technology. The SCPA provides the functionalities of a PA and of a Radio-Frequency Digital-to-Analog Converter (RF-DAC) in a monolithic CMOS device. The switching output stage of the SCPA enables this circuital topology to reach high efficiencies and offers excellent power handling capabilities. In this work, the properties of the SCPA are analyzed in an extensive and detailed dissertation.

Nowadays Wireless Communications operate in a very crowded spectrum, with strict coexistence requirements, thus demanding a strong linearity to the RF-DAC section of the SCPA. A great part of the work of designing a good SCPA is in fact designing a good RF-DAC. To enhance RF-DAC linearity, a precision of the timing of the elements up to the *ps* range is required. The use of a single core-supply voltage in the whole circuit including

the CMOS inverter of the switching output stage enables the use of minimum size devices, improving accuracy and speed in the timing of the elements.

The whole circuit operates therefore on low core-supply voltage. Throughout this work, a detailed analysis carefully describes the electromagnetic structures which maximize power and efficiency of low-voltage SCPAs.

Due to layout issues subsequent to limited available voltages, however, there is a practical limitation in the maximum achievable power of low-voltage SCPAs. In this work, a Multi-Port Monolithic Power Combiner (PC) is introduced to overcome this limitation and further enhance total achieved system power. The PC sums the power of a collection of SCPAs to a single output, allowing higher output powers at a high efficiency. Benefits, drawbacks and design of SCPA PCs are discussed in this work.

The implemented circuit features the combination of four differential SCPAs through a four-way monolithic PC and is simulated to obtain a maximum drain efficiency of 44 % at a peak output power of 29 dBm on 1.1 V supply voltage. Extensive spectrum analysis offers full evaluation of system performances. After exploring state-of-the-art possibilities offered by an advanced 28 nm CMOS technology, this work predicts through rigorous theoretical analysis the expected evolution of SCPA performances with the scaling of CMOS Technologies. The encouraging forecast further emphasizes the importance of SCPA circuits for the future of high-performance Wireless Communications.

Sommario

Il numero dei dispositivi senza fili è cresciuto esponenzialmente negli ultimi dieci anni. Grandi progressi tecnologici e nuove architetture di ricetrasmettitori hanno reso possibile un'impressionante insieme di applicazioni a radio-frequenza.

La tecnologia CMOS ha giocato un ruolo centrale nel rendere possibile una diffusione in larga scala di dispositivi senza fili grazie ai suoi esclusivi vantaggi in termini di costo e integrazione. Nuovi ricetrasmettitori marcatamente digitali hanno preso pieno vantaggio dell'evoluzione tecnologica prevista dalla legge di Moore. La riduzione della dimensione degli integrati microelettronici ha permesso una diffusione capillare di dispositivi senza fili a basso costo, di ridotte dimensioni e dal basso consumo.

D'altra parte, la funzionalità degli amplificatori di potenza (PA) per radio frequenza (RF) è storicamente implementata in un modulo che è separato dal nucleo CMOS del ricetrasmettitore. Il PA determina tradizionalmente la potenza e la durata della batteria del ricetrasmettitore, e per ciò è giustificata la sua implementazione in una tecnologia dedicata. All'opposto, un ricetrasmettitore CMOS pienamente integrato senza PA esterno beneficerebbe largamente in termini di riduzione di area e di complessità di sistema.

In questo lavoro, un prototipo completamente integrato di Amplificatore di Potenza a Capacità Commutate (SCPA) è stato implementato in una tecnologia CMOS a $28\,nm$. L'SCPA fornisce le funzionalità di un PA e di un Convertitore Digitale-Analogico in Radio Frequenza (RF-DAC) in un dispositivo CMOS monolitico. Lo stadio d'uscita commutato dell'SCPA rende questa topologia capace di raggiungere alte efficienze e offre un'eccellente capacità di generare potenza. In questo lavoro, le proprietà dell'SCPA sono analizzate in una discussione estensiva e dettagliata.

Le comunicazioni senza fili di oggi operano in uno spettro molto affollato, con requisiti

di coesistenza molto stretti, che quindi richiedono un'alta linearità alla sezione RF-DAC dell'SCPA. Una grande parte del lavoro di progetto di un SCPA è infatti progettare un buon RF-DAC. Per migliorare la linearità dell'RF-DAC, è richiesta una precisione della temporizzazione degli elementi fino all'ordine di grandezza dei ps. L'uso di una singola tensione di alimentazione, incluso l'invertitore CMOS dello stadio di uscita commutato, rende possibile l'uso di dispositivi di dimensione minima, migliorando l'accuratezza e la velocità della temporizzazione degli elementi.

L'intero circuito opera quindi su una bassa tensione di alimentazione. Nel corso di questo lavoro, un'analisi dettagliata descrive con attenzione le strutture elettromagnetiche che massimizzano la potenza e l'efficienza degli SCPA a bassa tensione.

A causa di problemi di maschere dovuti alle limitate tensioni disponibili, comunque, c'è una limitazione pratica nella massima potenza che un SCPA a bassa tensione può raggiungere. In questo lavoro, un Sommatore di Potenza Monolitico Multi-Porta (PC) è introdotto per superare questa limitazione e incrementare ulteriormente la potenza di sistema totale. Il PC somma la potenza di una collezione di SCPA in una singola uscita, rendendo possibili potenze più alte con un'alta efficienza. I benefici, i problemi e il progetto dei PC per SCPA sono discussi in questo lavoro.

Il circuito progettato comprende la combinazione di quattro SCPA attraverso un Sommatore di Potenza (PC) monolitico ed è simulato ottenere un'efficienza massima di collettore del $44\,\%$ con una potenza di picco di $29\,dBm$ da una tensione di alimentazione di $1.1\,V$. Estensive analisi di spettro offrono una completa valutazione delle prestazioni di sistema. Dopo aver esplorato le prestazioni dello stato-dell'arte offerte da un'avanzata tecnologia CMOS a $28\,nm$, questo lavoro predice attraverso un'analisi teorica rigorosa l'evoluzione attesa delle prestazioni dell'SCPA con l'evoluzione delle tecnologie CMOS. L'incoraggiante previsione enfatizza ulteriormente l'importanza dei circuiti SCPA per il futuro delle comunicazioni senza fili ad alte prestazioni.

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List of Symbols and Abbreviations

AM/AM Amplitude-to-Amplitude

AM/PM Amplitude-to-Phase

C-DAC Capacitive Digital-to-Analog Converter

CA Carrier Aggregation

CDMA Code-Division Multiple Access

CIM Counter Inter-Modulation

DAB Digital-Audio Broadcast

DAC Digital-to-Analog Converter

DCO Digital Control Oscillator

DFE Digital Front-End

DNL Differential-non-Linearity

DPA Digital Power-Amplifier

DPD Digital Pre-Distortion

DPLL Digital Phase-Locked Loop

DSB Double-Sided Bandwidth

DVB Digital-Video Broadcast

EDA Electronic design automation

EM Electro-Magnetic

EN European Standard

ETSI European Telecommunications Standards Institute

EVM Error-Vector Magnitude

FCC Federal Communications Commission

FDD Frequency Division Multiplex

FFT Fast-Fourier Transform

FM Frequency Modulation

FOM Figure-of-merit

I/Q In-Phase and Quadrature-Phase

IEEE Institute of Electrical and Electronics Engineers

IFFT Inverse Fast-Fourier Transform

INL Integral-non-Linearity

IOT Internet Of Things

JTAG Joint Test Action Group

KPI Key-Performance Indicator

LAN Local-Area Network

LDO Low-Dropout Voltage Regulator

LTE Long-Term Evolution

MIC Japan Ministry of Internal Affairs and Communications

MIMO Multiple-Input Multiple-Output

OFDM Orthogonal Frequency Division Multiplex

PA Power Amplifier

PSD Power Spectral Density

PSK Phase-Shift Keying

PSRR Power-Supply-Rejection-Ratio

QAM Quadrature-Amplitude Modulation

RF-DAC Radio-Frequency Digital-to-Analog Converter

SCPA Switched-Capacitor Power Amplifier

SNR Signal-to-Noise Ratio

SSB Single-Sided Bandwidth

TDC Time-to-Digital Converter

TDD Time Division Duplex

Chapter 1

Introduction

Past and future development trends of Wireless Communications, the broad adoption of Wireless Technologies and the important minimum requirements mandatory for safe operation of Wireless devices are the key elements which are described throughout the Introduction of this Work. At first, an historical *excursus* identifies the origin of IEEE 802.11 standard popularly known, as, Wireless. Subsequently, facts concerning the diffusion of Wireless Communications remark a broad, and growing, world-wide adoption of the Technology. Next, present and future evolution of the Technology, including novel target applications, are discussed. Finally, the origin of the minimum requirements set by the law for safe operation of Wireless devices are tracked back to their essential motivations.

1.1 Growth of Wireless Communications

In 1990, a new committee under the IEEE organization, called IEEE 802.11, was set up to look into getting an open standard started [5]. A decision in 1985 by the United States Federal Communications Commission (FCC), in fact, opened several bands of the wireless spectrum for use without a government license. These so-called "garbage bands" were allocated to equipment such as microwave ovens which use radio waves to heat food [6].

The standard was published seven years later, in 1997. However, demand for wireless devices was so high by the time, that devices adhering to the new standard were already shipping by then.

IEEE 802.11 standard defines an over-the-air interface between a wireless client and a base station (or access point), or between two or more wireless clients. IEEE 802.11 is inherently compatible with 802 networks, specifically with the 802.3 wired Ethernet networks. In fact, and perhaps a cornerstone of the success for the standard, the 802.11 address space allows 802.11 networks to interact with the original 802.1 Local-Area-Network (LAN) specification that provides for bridging between separate physical networks. Accordingly, Wireless devices can operate seamlessly together with their wired counterpart.

As capabilities were are added over the years to the IEEE 802.11, some become known by the name of the amendment, such as IEEE 802.11b, IEEE 802.11g and IEEE 802.11n. Each of these amendments defines a maximum speed of operation, the radio frequency band of operation, how data is encoded for transmission, and the transmitter and receiver features. The amendments to which a device adheres are referred to in a sequential manner, for example 802.11 b/g/n indicates that a device can operate against amendment b, g and n of IEEE 802.11.

Lately, IEEE 802.11 standard, which celebrated its first 25 years in 2015, is so widely diffused that it is usually thought as a synonymous of Wireless LAN in general. Subsequently, IEEE 802.11 standard is colloquially simply referred to as "Wireless". For simplicity, the keyword Wireless, with capital letter, is then sometime used for referring to IEEE 802.11 throughout the entire scope of this Work as well.

1.2 Ubiquitous Diffusion

As already hinted in the previous section, the diffusion of Wireless Technologies is remarkable. Evidences of ubiquitous Wireless Diffusion, include

- Large wireless diffusion in private households, i.e. to semi-static contexts. Worldwide home network penetration is expected to climb up from 24.8% in 2013 to 33.2% by 2018. I.e., in the present, one out of four inhabitants of the planet have access to a Wireless Network at home, and this ratio is expected to climb up to one over three in the near future. Growth is being driven by the continued spread of broadband services and demand for multi-screen video services. Wireless is seen as commonplace in mature

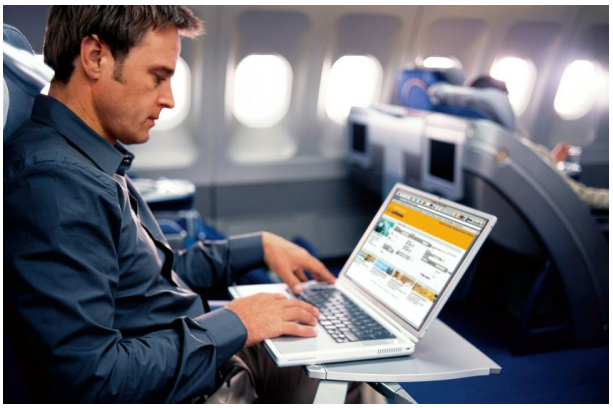


Figure 1.1: In-plane Wireless Connections have been lately deployed by all major airlines companies and are available, while flying, on selected airplanes

markets, including server provided broadband routers with integrated Wireless access points. [7]

- Wild diffusion of Wireless in hotels, i.e. to users on-the-go. 57%, i.e. over one half of all European hotels offer nowadays a Wireless connection to guests. Wireless is greatly appreciated by guests, and sometime even a deal breaker, for example, a report from Forrester Consulting discovered that more than 90% of business travelers, i.e. the vast majority, wanted Wireless in their room, and for a third it was a deal breaker – without it they would not return. [8]

- Major airlines companies offering the possibility to subscribe an in-flight Wireless service on selected planes, i.e. diffusion of Wireless in technologically-challenging environments, as per Fig. 1.1. For example, the three leading American airlines companies including American Airlines Group, Delta Air Lines and United Continental Holdings offer in-flight wireless connections, and, in Europe, the two leading airlines companies, such as Lufthansa and Airfrance-KLM offer in-flight wireless connection on selected planes. The number of airline companies offering this possibility has been rapidly expanding over the years.

Similar statistics can be obtained about any other facility where users are likely to stay with a laptop, including, airports, cafes, libraries and public spots, with the notable exception of Hospital. However, Wireless connection could get into Hospitals as well. In fact, free

Table 1.1: Wireless LAN Throughput by IEEE Standard

WLAN Standard	**MIMO streams, Bandwidth**	**Operating Frequency**	**Single-User Throughput**
IEEE 802.11b	1x20MHz	2.4GHz	11Mbit/s
IEEE 802.11g	1x20MHz	2.4GHz	54Mbit/s
IEEE 802.11n	1x40MHz	2.4GHz, 5.4GHz	150Mbit/s
	4x40MHz	2.4GHz, 5.4GHz	600Mbit/s
IEEE 802.11ac	1x160MHz	5.4GHz	867Mbit/s
	4x160MHz	5.4GHz	3.47Gbit/s
IEEE 802.11ad	1x2.16GHz	60GHz	6.757Gbit/s

Wireless in the Hospitals would allow patient hospitalized for long periods of time, to keep-up with their daily life, for example, to keep updated with their businesses, or, for kids, to keep up with their school classes.

1.3 Standard Development

Whilst 802.11 standard is originally intended to provide a Wireless Local-Area Network access, IEEE 802.11ad extends the purpose of the wireless link to novel applications. For instance, a primary target for IEEE 802.11ad is streaming HD video. For example, a person could bring a laptop into a room and have it automatically linked wirelessly to a large display, digital projector and/or storage system to stream video or data. [9]

However, IEEE 802.11ad provides a viable solution delivering high speeds for applications requiring just a few meters of transmission [9], in fact, IEEE 802.11ad compatible APs are able to cover not much more than a room. Communication in the 60 GHz range are in fact not as robust as those used in previous standards. Should the high-speed connection be lost for any reason, devices will fall back to 2.4 GHz and 5 GHz signals to continue communications without interruptions. For aforementioned motivations, critical for future Wi-Fi adapters is to support both IEEE 802.11ad and IEEE 802.11 previous standards,

backwards.

The deployment of novel Wi-Fi transceivers requires thus the integration of a high number of circuits, for delivering all standards required. Beside implementing circuits enabling new standards, it is then as well critical to innovate circuits implementing legacy standards, so that they can be implemented in a smaller area and at a high efficiency, enabling future devices offering interoperability to a large number of standards to be small and slim regardless on their functionalities.

1.4 Mandatory Requirements

Importantly, for a Wireless transceiver being allowed to operate, it is required, not to harm human health, neither for the active user of the transceiver, nor for other people staying nearby, and not to disturb other transceivers operating in other frequency bands. Minimum requirements are set so that safety of health, and of communications are met.

Any transmitter operating in the European region shall adhere European Telecommunications Standards Institute (ETSI) requirements [10]. Other world regions are governed by Federal Communications Commission (FCC), Japan Ministry of Internal Affairs and Communications (MIC) and Korean Standard. Technical requirements are described in the following-chapter, with a particular focus for ETSI standard, since this Work has been developed in the European Union. It is important to notice that, for the legislator, the fact that the transceiver is, or is not, able to communicate with the others, is irrelevant. In fact, the effectiveness of the wireless transmission is not ruled by the ETSI, which is concerned about safety of health and of the communications.

In order not to harm human health, transmitters are only allowed to operate below a certain maximum power level. As a general principle, an idea behind the specification of the maximum power level is that, a transmitter which could harm human health produces a potentially-harming field F which is inversely proportional to the square of the distance d, and directly proportional to the transmitted power P,

$$F \propto \frac{P}{d^2} \tag{1.1}$$

therefore, the farther a human body is located from a transmitter, the lower the potentially harmful field to the body. Therefore, devices which are supposed to be kept i.e. by hand, are subject to severe laws, limiting maximum transmittable power and thus maximum operating range, whilst, i.e. TV broadcasting antenna towers, high-on-the-ground and far from any urban environment are allowed to transmit at a much higher power level, and offer larger operating ranges.

Next, it is in the legislator interest to ensure that licensed band operations are not harmed by unlicensed band transmitter. In fact, it is important to keep in mind that, to be awarded the permission to operate in the licensed frequencies, big operators, such as Radio and Video broadcasters and Mobile operators, have to pay an important fee, and that, even more critical, certain frequencies are of crucial importance for the state itself, i.e., are allocated for the military forces.

To ensure safety and pacific inter-operations of the totality of deployed transceivers, every transceiver which is directly available on the market to a final consumer, has to undergo a certification process, ensuring that it is safe for health and that it does not disturb any other licensed transceivers.

Chapter 2

System Analysis

This part of the Work describes a Wireless Transmitter System and the Standards and Technical Specifications which the System has to fulfill. At first, an introductory section mentions the Standards which are relevant to a Wireless Transmitter. With the knowledge of the Standards, and of ETSI and IEEE Technical Documentations, important metrics of the Transmitter are reviewed, including Peak Power, Unwanted Emission Spectrum, and Error-Vector Magnitude. The major System non-idealities contributors to these Transmitter metrics, including Supply Noise, Spectral Images, Quantization Noise, Harmonic Distortion and Phase Noise are then analyzed. Next, after a read-through of in-device Receiver Desensitization Issue, a Survey of Transmitter Architectures is proposed. Thread-offs of Classical and Evolved Transmitter Architectures are analyzed, and finally, the proposed Digital I/Q Architecture is chosen due to its superior Modulated Bandwidth Performance.

2.1 Relevant Standards

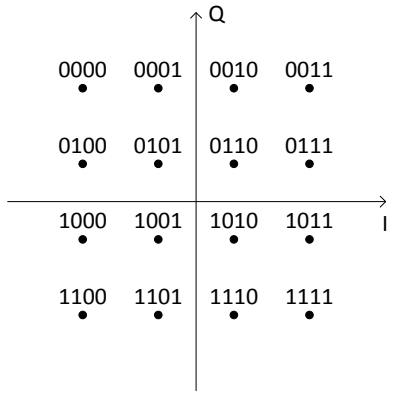
The vast majority of Radio-Frequency Communications are either digital already or slowly transitioning towards digital domain, with the last notable example of analog transmission found in the FM radio, which is anyhow slowly fading towards digital-audio-broadcast (DAB) as well. Television, which used to rely on analog communications not long ago, has recently undergone an evolution towards digital-video-broadcast (DVB). Therefore, during any evolved Radio-Frequency Communication, digital symbols are being transmitted all the

time. The air is but always a physical object, therefore, before transmission, digital signal are always converted to an analog counterpart. Analog symbols are then transmitted through the air, and converted back to their digital counterparts at the receiver side. There are many ways into which the digital information can be encoded into analog symbols.

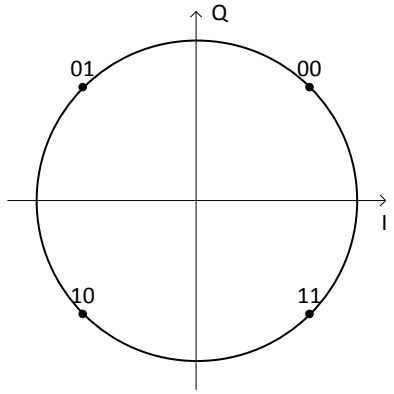
In the case, for example, in which the radio link includes a carrier being transmitted at a fixed frequency from a Transmitter to a Receiver, the amplitude of the carrier can be varied over time, in a discrete manner, to encode many different digital symbols. Or, alternatively, the phase of the carrier can be modulated, in a discrete manner, to differently encode many digital symbols (PSK). Most notably, if the information of a symbol is encoded in a combination of both phase and amplitude modulation of a carrier, the System operates a Quadrature-Amplitude-Modulation (QAM), as in Fig. 2.1. [11]

Digital systems are extremely sensitive to noise in the digital domain. A single wrong bit in a long sequence of words can invalidate a whole content transferred Wirelessly. Immunity to interferences is therefore critical and immunity in the digital domain is improved by adding redundancy to the transmitted information. By means of redundant codes, it is possible to identify and even correct errors (i.e., Hamming Distance), or automatically request for a new copy in case of invalidated contents. Since typical RF interferers are narrow-band and have a short time-duration, Orthogonal-Frequency Division Multiplexing (OFDM), as in Fig. 2.2b, encoding is a good way to resist interferers. A temporary interfering spur typically invalidates only a small offsets of frequencies, making therefore possible for standards where each frequency bin represent one symbol only, to guarantee that in the transmitted symbol only few bits are wrong. Such an error is even recovered directly through forward error correction techniques, since it is an invalidation of only one little part of the stream, making the narrow-band interferer irrelevant to the correct radio-device link operation. Beside, since OFDM encodes information into a large set of sub-carriers, a way to maximize spectral efficiency is provided.

To enable simultaneous connection between many devices and avoiding large interferences between simultaneously operating Transceivers, the whole spectrum is divided in channels. These channels can be assigned permanently to a single link between devices, dynamically assigned at the beginning of the device connections, or, such as in Bluetooth Devices, con-



(a) 16-QAM, Constellation Diagram

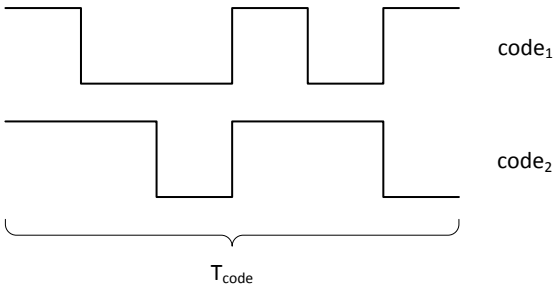


(b) 4-PSK, Constellation Diagram

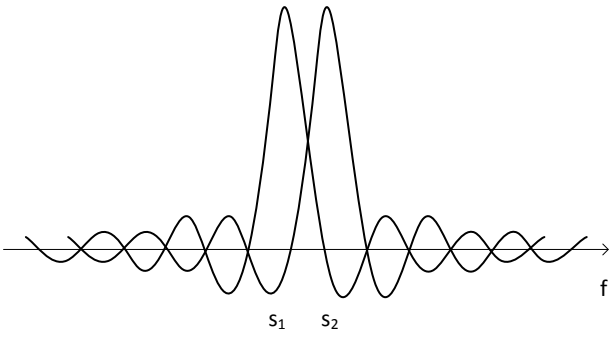
Figure 2.1: Means of encoding digital information into one carrier

tinuously re-assigned during transmission (frequency hopping).

Many applications require to enable simultaneous Transmission and Reception of data between devices. With a unique channel being assigned, one could assign the channel for Transmission at a certain moment, and switch it to Reception subsequently. This method, which requires accurate synchronization between receiver and transmitter, providing a half-duplex transmission rate, is called Time-Domain-Division (TDD) and is depicted in Fig. 2.3. Alternately, for full-duplex transmissions, one channel is dedicated for Transmission and another channel for Reception. In Frequency-Domain-Division (FDD), a particular care



(a) Code-Division Multiple Access (CDMA)



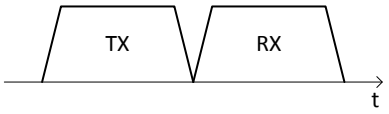
(b) Orthogonal-Frequency Division Multiple Access (OFDM)

Figure 2.2: Means of multiple access at one physical channel

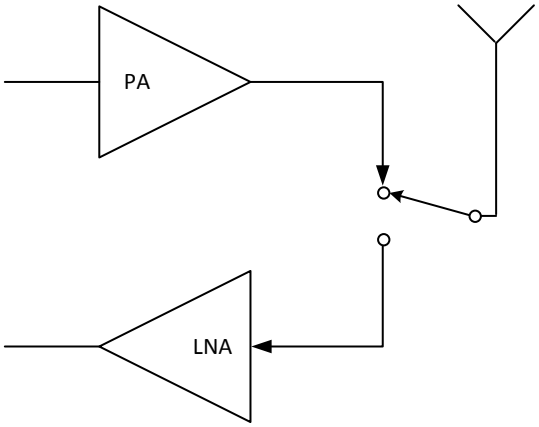
has to be given to avoid the generated spectrum to couple between the Transmitter and received channel at the Receiver, which would result in a decreased receiver sensitivity. In fact, in FDD both receiver and transmitter are active at the same time as shown in Fig. 2.4.

In some cases, many devices can transmit and receive at the same time on the same channel. In CDMA standard, as in Fig. 2.2a, i.e., one transceiver always operates on codes which are orthogonal to the codes operated by other transceivers. This way, all transceivers can operate a the same time on the same channel. By contrast, in Orthogonal-Frequency-Division-Modulation (OFDM) channel division, the orthogonality between the transceivers is obtained by allocating different sub-carriers within the channel bandwidth to each of the users of the channel. Each transceiver operates then on an assigned subset of the available carriers which is orthogonal to the subset assigned to other transceivers, and therefore

multiple transceivers can operate at the same time on the same channel. OFDM as a way to split a channel to multiple users, requires spurious emissions of the Transmitters to be low enough not hurt adjacent subcarriers of other Transmitters. Since guaranteeing such an orthogonality is a challenging topic, CDMA, where orthogonality is instead obtained in the time-domain has often been preferred for Wireless and Mobile Communications.



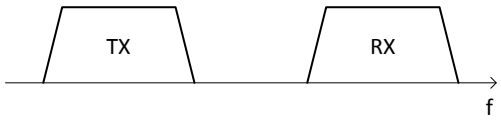
(a) Time Division Multiplex (TDD)



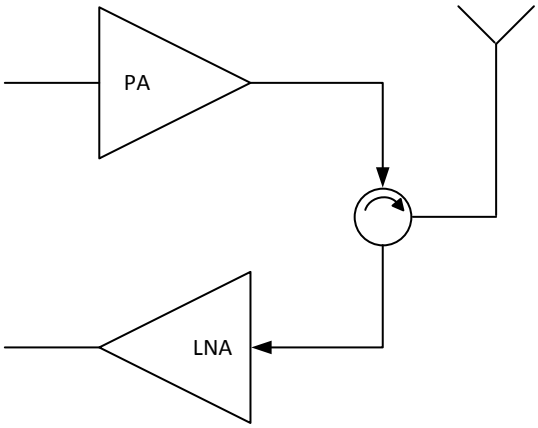
(b) Time Division Duplex. Either Transmitter or receiver are active at once.

Figure 2.3: Means of duplexing transmission and reception through TDD

Modern communications techniques include as well Carrier-Aggregation (CA), Fig. 2.5, standards where many channels are employed at the same time for one link, improving overall Transmission and Reception throughput. Furthermore, lately, multiple-input-multiple-output (MIMO) transceivers have been introduced, empowered by multiple, spatially separated, independently driven antennas. MIMO transceivers feature higher spectral efficiency compared to single-antenna systems, and can route optimal channels even in case of poor line-of-sight visibility or of crowded spectrum by means of constructive/disruptive interfer-



(a) Frequency Division Multiplex (FDD)



(b) Frequency Division Duplex. Transmitter and receiver are both active at the same time.

Figure 2.4: Means of duplexing transmission and reception through FDD

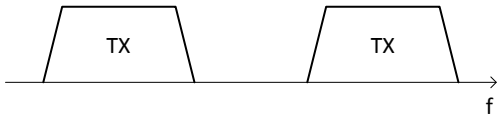


Figure 2.5: Carrier-Aggregation (CA)

ence with the environment building up diverse transmissions paths.

A practical implementation of the OFDM transceiver concept already described before, is provided in Fig. 2.7. The standard is particularly relevant to Wireless Communications, since by means of orthogonal-frequency division multiplexing (OFDM) the allocated channel is divided in a collection of sub-carriers, improving spectral efficiency and providing resilience

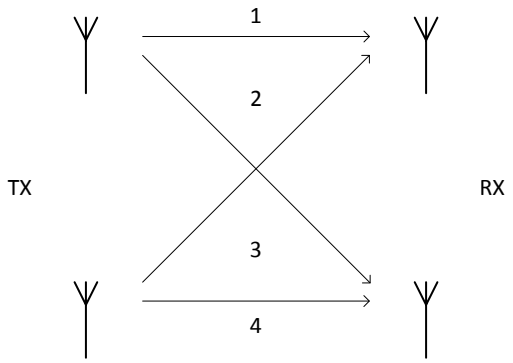


Figure 2.6: Multiple-Inputs Multiple-Outputs (MIMO)

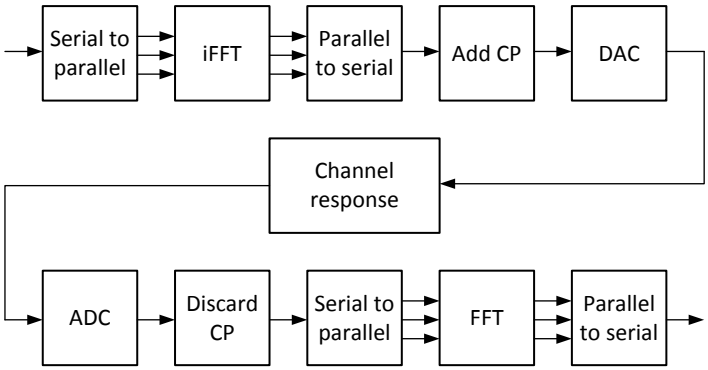


Figure 2.7: Orthogonal-Frequency Division (OFDM) System

to interferes, which easily crowd the Wireless frequencies spectrum. The Transmitter System comprises a scheme where,

- Digital information is encoded into QAM symbols
- QAM symbols are grouped to form OFDM subcarriers, through IFFT
- Cyclic Prefix is added to avoid Inter-Symbol-Interference (ISI)

consequently, and in the opposite order, the Receiver rejects the Cyclic Prefix and QAM symbols are reconstructed through FFT.

2.2 Maximum Radiated Power

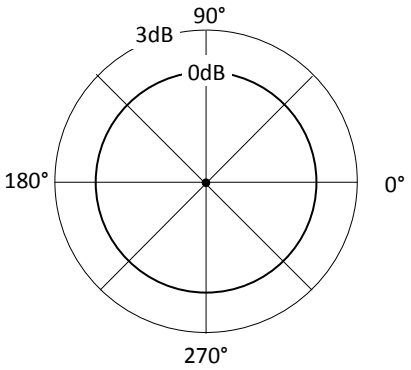
The European Telecommunications Standards Institute (ETSI) is an European Standards Organization, which produces standards to support European regulation and legislation. By adhering to these standards, manufacturers and service providers can claim 'presumption of conformity' with the essential requirements of a directive by self-declaration. Rather than having to go through costly type approval processes in different Members States, by respecting ETSI standards, manufacturers and service providers safely ensure that their devices operate in conformity with applicable regulations.

2.2.1 Equivalent Isotropic Radiated Power

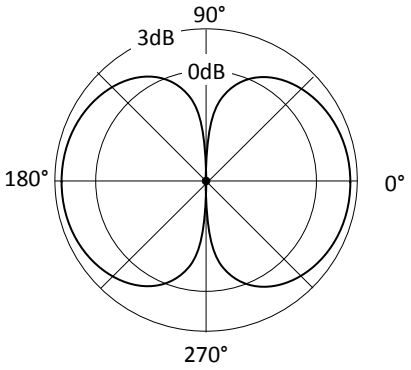
ETSI EN 300 328 V1.9.1 Harmonized European Standard (EN) [12] is the reference for Wide Band Data Transmission equipments such as IEEE 802.11™ RLANs, Bluetooth® Wireless Technologies, Zigbee™, etc. capable of operating in the band $2.4GHz$ to $2.4835GHz$. The document describes requirements for RF output power, defined as the mean equivalent isotropic radiated power (EIRP), of aforementioned equipments that typically operate on a fixed frequency, during a transmission burst. To comply with the European Standard, RF output power of devices operating under these conditions shall not exceed (clause 4.3.2.2.3) $20dBm$, for any combination of power level and intended antenna assembly.

Equivalent isotropic radiated power, referred to by the EN as RF output power, is the power that a theoretical isotropic antenna, evenly distributing power in all directions, would radiate to produce the peak power density observed in the particular direction of maximum antenna gain. For the same transmit power, in fact, different antenna types have different radiation patterns, with a higher field being radiated in some directions compared to other directions, i.e., antennas which are directional enhance the radiated field in some directions and weaken it in some others. In the direction where the field is enhanced, a higher power is measured when a directional antenna is operated compared to that which would be radiated in the that direction by an isotropic antenna.

The simplest and most widely used antenna, the dipole, has a radiation pattern which covers 360° uniformly on the horizontal plane, and has a direction of zero gain (node) at ±90°



(a) Horizonal Radiation Pattern



(b) Vertical Radiation Pattern

Figure 2.8: Half-Wave Dipole Antenna Radiation Pattern

on the vertical plane. A half-wave dipole is typically chosen for Wireless Communications, due to its smaller size compared to the dipole antenna. Physical size of the a half-wave dipole antenna l_h is in fact half the size of a dipole antenna for the same frequency, namely

$$l_h = \frac{1}{2}\lambda = \frac{1}{2}\frac{c}{f} = \frac{1}{2}12.5cm \tag{2.1}$$

Radiation patter of the half-wave dipole antenna is shown in Fig. 2.8. Fig. 2.8a shows that horizontal radiation pattern of a half-wave dipole antenna is isotropic. Vertical radiation pattern of Fig. 2.8b, instead, exhibits a direction of maximum power, where power is $2.15dBi$.

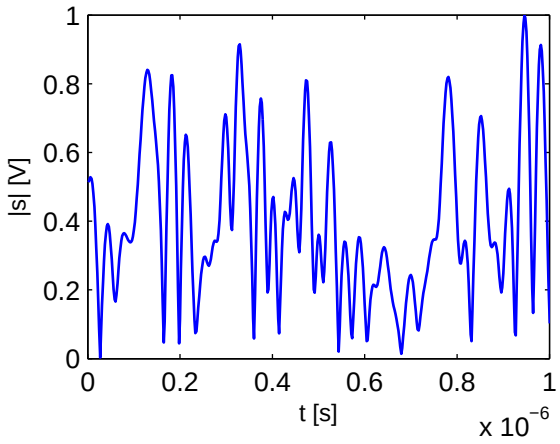


Figure 2.9: Magnitude of the trajectory of an IEEE 802.11 Signal

Therefore, combining horizontal and vertical radiation patterns, overall antenna gain of the half-wave dipole antenna is observed to be $2.15dBi$.

To improve the coverage range of a transceiver, i.e. the maximum distance at which a link is available, the receiver is designed for low-noise and high-sensitivity and the transmitter is designed to have high-power and low error-vector-magnitude. The maximum RF power which can be allowed at the RF transmitter output connector is therefore transmitted, and since

$$EIRP = P_{RF} + G_{antenna}[dB] \tag{2.2}$$

the maximum power results $P_{RF} \approx 17.85dBm$.

2.2.2 Peak-to-Average Power Ratio

High-speed IEEE 802.11 standards encode information in a number of OFDM sub-carriers within the transmitted spectrum, tightly spaced one another, as shown in Fig. 2.2b. Each sub-carrier's amplitude and phase information resemble a fragment of the information which is being transmitted, encoded i.e. with a QAM modulation. A time-domain signal is obtained through Inverse-Fast-Fourier Transform (IFFT) from the OFDM signal. Amplitude and phase of the transmitted signal vary over time resembling the desired OFDM signal frequency content.

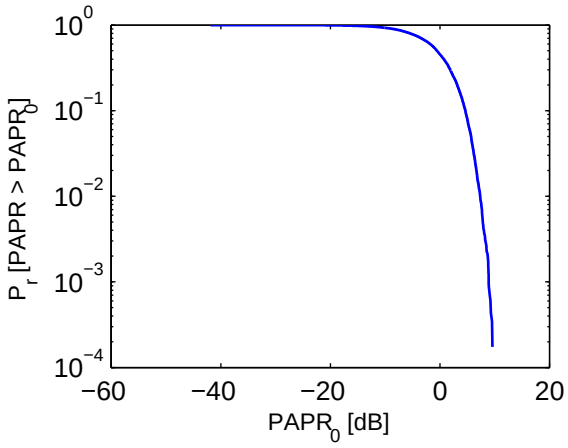


Figure 2.10: Cumulative distribution function of an IEEE 802.11 Signal

The trajectory of a high-speed IEEE 802.11 signal, as per Fig. 2.9, contains symbols whose magnitude can be subsequently large and small in magnitude. Over time, the signal exhibits therefore a peak-to-average ratio (PAPR); i.e., the maximum magnitude of transmitted symbols is higher than the average transmitted symbol magnitude. Namely,

$$PAPR = \frac{\max(P)}{\frac{1}{T}\int P \cdot dt} \tag{2.3}$$

usually expressed in decibel. ETSI EN 300 328 V1.9.1 Harmonized European Standard claims (clause 4.3.2.4.3) that RF output power is the highest average equivalent isotropic radiated power measured on any $10ms$ or less Tx-sequence. A $10ms$ Tx-sequence contains a large number of subsequent transmitted symbols. As shown in Fig. 2.9, a large number of symbols is in fact already observed in a $1\mu s$ Tx-sequence.

The theoretical PAPR of an OFDM signal with n uncorrelated sub-carriers is [13] $PAPR = 10\log(n) + CFc$ where CFc is the crest factor (in dB) for each sub-carrier. CFc is $3.01dB$ for the sine waves used for BPSK and QPSK modulation. A signal spanning over a $20MHz$ channel, composed by BPSK and QPSK subcarriers spaced 312.5 KHz apart, having 64 sub-carriers, exhibits a theoretical PAPR exceeding $21dB$.

Due to the large-value of the theoretical PAPR, a complementary cumulative distribution function (CCDF) of the PAPR is usually introduced [14]. In fact, it is observed that it is

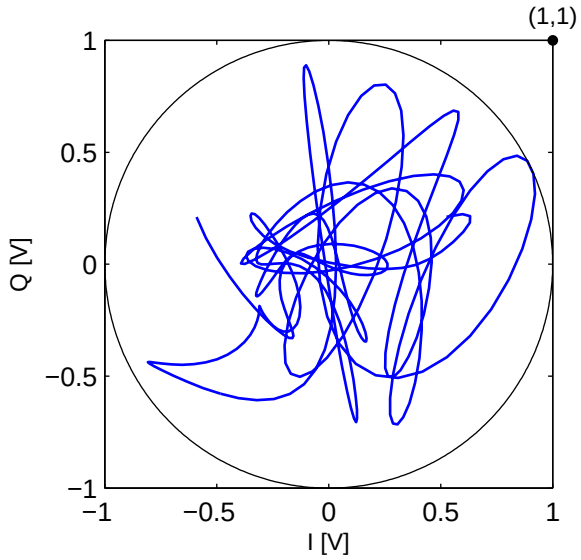


Figure 2.11: Partial Trajectory of an IEEE 802.11 Signal

possible to highly reduce the PAPR by clipping each signal exceeding a practical threshold, with a probability of error $P_r < 10^{-4}$. This reduces the clipped PAPR of a high-speed IEEE 802.11 signal to a value in the range of $PAPR = 12dB$. The clipped PAPR is then subsequently diminished by means of a PAPR reduction techniques (i.e., Clipping and Filtering, Coding, PTS, SLM, Interleaving, TR, TI and ACE [14]) to a reduced value of i.e. $PAPR = 9.6dB$ with a probability of error $P_r < 10^{-4}$, Fig. 2.10.

2.2.3 Constellation Power

IEEE 802.11 standards require high modulation bandwidths, with IEEE 802.11n requiring up to $40Mhz$ base-band signal bandwidth. Due to superior modulation bandwidth performance, as describe in Section 2.6, designed system employs of a Digital I/Q RF architecture. A Digital I/Q RF Transmitter directly generates antenna signal by summing up two vectors, one in-phase with the RF clock and one in-quadrature with the RF clock. Each of the vector amplitude is controlled individually through a digital code.

Fig. 2.11 presents the trajectory of a IEEE 802.11 Signal on an I/Q Diagram. The trajectory can be circumscribed by a circle whose ray is equal to $P_{trajectory} = P_{RF} - G_{antenna} +$

$PAPR$, normalized to $1V$ in Fig. 2.11. However, none of the points inside the circle of ray $P_{trajectory}$ ever reaches the maximum power which a Digital I/Q RF Transmitter can generate. In fact, point $(1V, 1V)$, see Fig. 2.11, does not belong inside the $P_{trajectory}$ circle, and the normalized voltage of point $(1V, 1V)$ is $\sqrt{1^2 + 1^2}V = \sqrt{2}V$. The maximum power generated by a Direct I/Q RF Transmitter is therefore $20 \log \sqrt{2} = 3dB$ above the power of the points within the circle defined by $P_{trajectory}$.

2.2.4 Total Radiated Power

Recalling previously defined figures, maximum RF power which is instantaneously generated by the Transmitter for a high-speed IEEE 802.11 $2.4GHz$ standard is, therefore,

$$\begin{aligned} P_t =& P_{RF} - G_{antenna} + PAPR + P_{constellation} \\ =& 20dBm - 3dB + 9.6dB + 2.15dB \approx 29dBm \end{aligned} \tag{2.4}$$

Losses in the system, such as cable losses, board losses, package losses, variations due to temperature, aging and process, degrade overall antenna radiated power. However this particular P_t specification ensures that, regardless of the entity of the unknown system losses, the system is safe to operate, with an output power which is not exceeding $ETSI$ Harmonized European Standard Recommendations.

2.3 Unwanted Emissions

A Wireless Device does not only radiate useful power, but does also radiate power outside its channel bandwidth. ETSI EN 300 328 V1.9.1 Harmonized European Standard (EN) [12] specifies the level of the unwanted emissions outside the $2.4GHz$ to $2.4835GHz$ operating band, discerning between the out-of-band domain and the spurious domain of unwanted spectral emissions. IEEE 802.11 regulates then unwanted emissions within the $2.4GHz$ to $2.4835GHz$ operating band, to the neighbor channel domain, to ensure the coexistence of multiple channels within allowed operating band as shown in Table 2.1 and Fig. 2.13.

Table 2.1: Transmitter limits for spurious emissions

Frequency range	**Maximum power**	**Bandwidth**
30 MHz to 47 MHz	-36 dBm	100 kHz
47 MHz to 74 MHz	-54 dBm	100 kHz
74 MHz to 87,5 MHz	-36 dBm	100 kHz
87,5 MHz to 118 MHz	-54 dBm	100 kHz
118 MHz to 174 MHz	-36 dBm	100 kHz
174 MHz to 230 MHz	-54 dBm	100 kHz
230 MHz to 470 MHz	-36 dBm	100 kHz
470 MHz to 862 MHz	-54 dBm	100 kHz
862 MHz to 1 GHz	-36 dBm	100 kHz
1 GHz to 12,75 GHz	-30 dBm	1 MHz

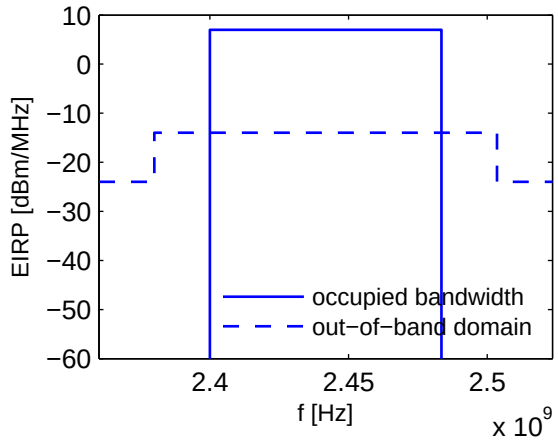
2.3.1 Supply-Noise

A Low-Dropout Voltage Regulator (LDO) typically regulates the supply voltage of the System to a constant voltage reference. On-board DC/DC converter generating low core-supply voltage used in the system introduces, in fact, tones at its switching frequency, which then the LDO removes through its voltage drop on its series path on the supply. The LDO rejects therefore supply noise and generates a new reference with its own noise spectral content, usually specified in terms of $\mu V/\sqrt{Hz}$ for a given output voltage, i.e. below $0.1\mu V/\sqrt{Hz}$ in the voltages and bands of interest. [15]

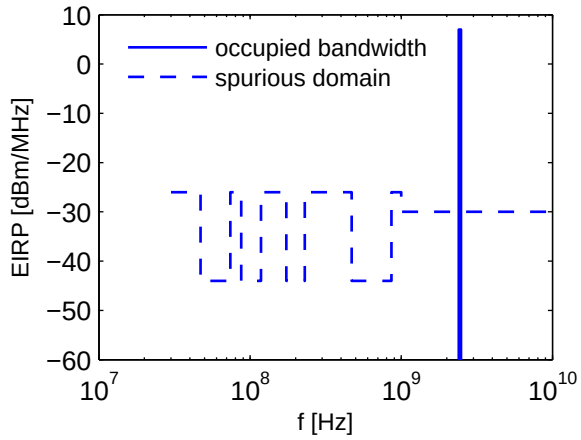
Supply noise translates then to load noise through Power-Supply-Rejection-Ratio (PSRR) of the System. PSRR of an RF-DAC System Architecture is, in this case, a moderate gain. On average, in fact, it is observed that out of the $1.1V$ supply voltage, $17dBm$ of output power is generated on 50Ω load, i.e.

$$V_{rms} = \sqrt{PR} \tag{2.5}$$

therefore, to deliver $50mW$ load output power, $1.58Vrms$ are generated on a 50Ω load



(a) Out-Of-Band Emissions



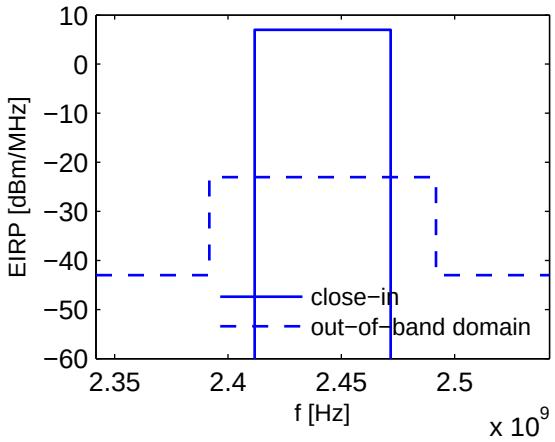
(b) Spurious Emissions

Figure 2.12: ETSI 300 328 Unwanted Spectrum Emissions Limits, Fixed Transmission Frequency, $20MHz$ Channel Bandwidth

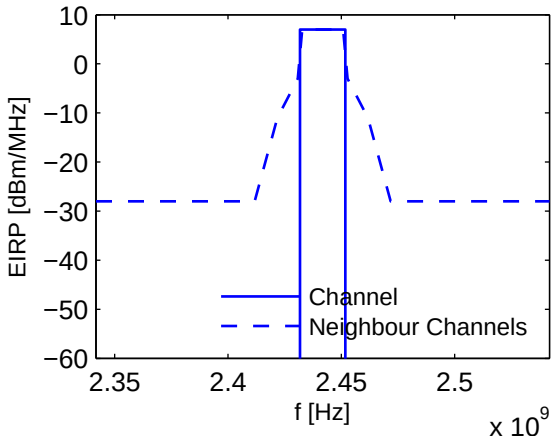
resistance. Ratio between supply and output voltage is 1.43; i.e. any noise with power level P on the supply is translated to a noise with power level $P[dB]+20\log(1.43) = P+3dB$ on the output. The matching network introduces an attenuation outside channel frequencies, but no active feedback mechanism attenuates noise from the supply in the capacitive RF-DAC open-loop design described in Sec. 3 for in-band components.

Output spectral noise contribution from the LDO is calculated to be below

$$P = 20\log(0.1\mu V/\sqrt{Hz}) + 3dB = -137dB/Hz \tag{2.6}$$



(a) IEEE Out-of-Band



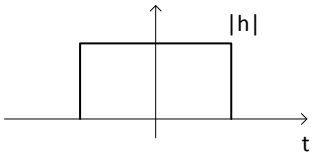
(b) IEEE Neighbour Channels

Figure 2.13: IEEE 802 11 Unwanted Spectrum Emissions Limits, Fixed Transmission Frequency, $20MHz$ Channel Bandwidth

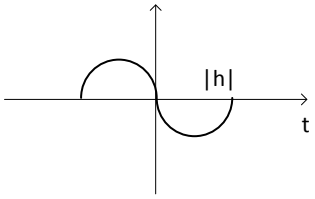
which reads $-107dBm/Hz$, or $-47dBm/MHz$ on ETSI EN 300 328 and IEEE 802.11 spectral mask, and therefore within specifications. For the lower part of the spectrum, i.e., for the part of the spectrum which goes from DC to $1GHz$, the attenuation introduced by the matching network is more pronounced, further helping the design achieving target specifications.

2.3.2 Spectral Images

A zero-order hold Digital-to-Analog Converter (DAC) such as i.e. that of Fig. 3.1, reconstructs digital input to an analog signal with a rectangular reconstruction filter as in Fig. 2.14a. The analog equivalent of digital input signal is held for the time a sample lasts, before the next sample is introduced.



(a) Zero-order Hold



(b) Sine-Wave Zero-order Hold

Figure 2.14: Impulse Response

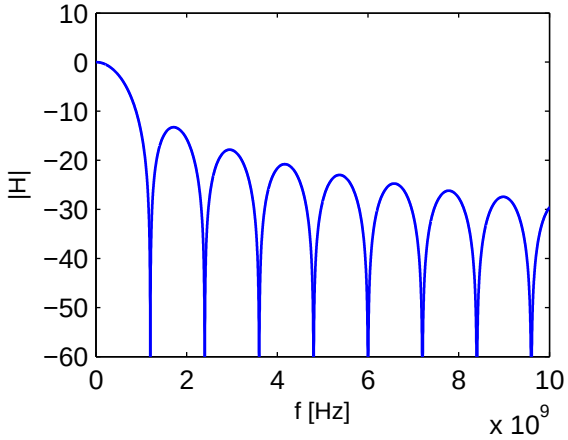
$$x(t) = \sum_{n=-\infty}^{+\infty} x[n] \cdot rect\left(\frac{t - nT_s}{T_s} - \frac{1}{2}\right) \tag{2.7}$$

and

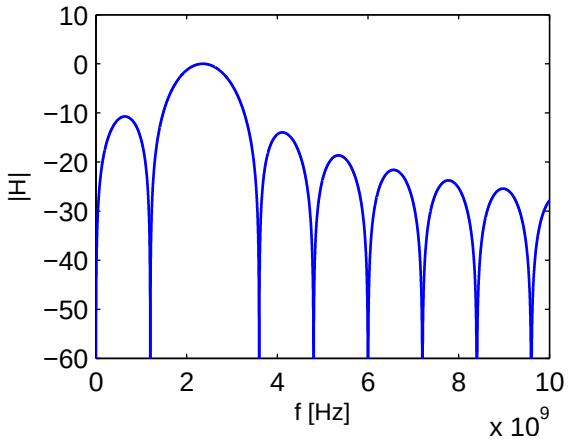
$$\begin{aligned} h_{ZOH}(t) &= \frac{1}{T_s} rect\left(\frac{t}{T_s} - \frac{1}{2}\right) \\ H_{ZOH}(f) &= e^{-i\pi f T_s} sinc(f T_s) \end{aligned} \tag{2.8}$$

Transfer function of zero-order hold reconstruction filter is shown in Fig. 2.15a.

Instead, a Radio-Frequency DAC (RF-DAC), such as i.e. that of Fig. 3.2, ideally produces for each digital sample a sine-wave whose amplitude corresponds to the analog equiv-



(a) Zero-order Hold



(b) Sine-Wave Zero-order Hold

Figure 2.15: Frequency Response

alent of the digital input signal as in Fig. 2.14b. The sine-wave is then held for one sample, before the next sample is introduced.

$$x(t) = \sum_{n=-\infty}^{+\infty} x[n] \cdot sin(2\pi \frac{t - nT_s}{T_{RF}}) \cdot rect\left(\frac{t - nT_s}{T_s} - \frac{1}{2}\right) \tag{2.9}$$

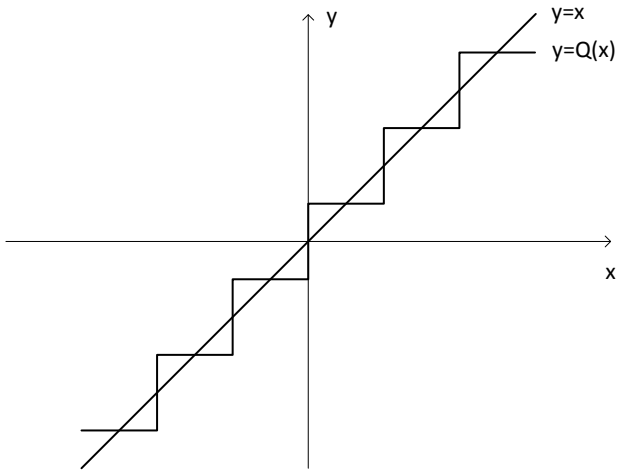


Figure 2.16: Quantization of an Analog Signal

and

$$\begin{aligned} h_{ZOH}(t) &= sin(2\pi\frac{t-nT_{RF}}{T_s})\cdot\frac{1}{T}rect\left(\frac{t}{T_s}-\frac{1}{2}\right) \\ &= a(t)\cdot b(t) \\ H_{ZOH}(f) &= (A*B)(f) \\ &= \int\left[\delta(f-u+f_{RF})+\delta(f-u-f_{RF})\right]e^{-i\pi uT_s}sinc(uT_s)\cdot du \\ &= e^{-i\pi(f-f_{RF})T_s}sinc\left[(f-f_{RF})T_s\right]+e^{-i\pi(f+f_{RF})T_s}sinc\left[(f+f_{RF})T_s\right] \end{aligned} \tag{2.10}$$

The transfer function of sine-wave zero-order hold reconstruction filter is shown in Fig. 2.15b. The main lobe is centered at radio-frequency f_{RF}, and the first zero of the sinc appears at $f_{RF}-f_s$ and then at $f_{RF}+f_s$. Images of the reconstructed signal are generated at frequencies which are integer multiples of f_s, i.e. kf_s. Therefore the strongest spectral component is at f_{RF}, where a replica of the desired signal appears unattenuated.

Undesired replicas of the signal, located at kf_s, are attenuated by the zero of the sinc function. For signals with a small bandwidth, all replicas are hugely attenuate. For signal with larger signal bandwidth, however, spectral images attenuation is limited, with a min-

imum attenuation α at the edge of the signal bandwidth, centered at image frequency, i.e. $f_{edge} = f_{RF} - BW/2$, being,

$$\alpha = 20 \log \left[\left(e^{-i\pi f_{edge} T_s} + e^{-i\pi f_{edge} T_s} \right) sinc \left(f_{edge} T_s \right) \right] \tag{2.11}$$

For example, a signal with $BW = 20MHz$, where $f_{RF} = 2.4GHz$ and $f_s = 1.2GHz$ has a minimum attenuation $\alpha = -40dB$. The attenuation is enough to meet ETSI 300 328 masks. Signal power, measured to be $7dBm/MHz$ in the channel bandwidth, attenuated by $40dB$ drops to $-33dBm/MHz$, meeting the spurious-domain specifications at $1.2GHz$ and at further images frequencies.

2.3.3 Quantization Noise

The uniform quantization of the digital signal operated at the digital-to-analog converter introduces a noise, whose power is uniform over the quantization interval $-\Delta/2$ to $+\Delta/2$. Its integral yields

$$\sigma^2 = \frac{\Delta^2}{12} \tag{2.12}$$

while signal power for full-scale sinusoidal-signal is

$$\sigma^2_{signal} = \left(\frac{2^N}{\sqrt{2}} \Delta \right)^2 \tag{2.13}$$

signal-to-noise ratio (SNR) of the quantized signal, when N bits are employed for quantization thus with a peak signal power of, is therefore

$$SNR = 1.76 + 6.02 \cdot N[dB] \tag{2.14}$$

When transmitting an OFDM signal, however, PAPR and $P_{constellation}$ decrease signal power with respect to full-scale sinusoidal-signal power, of a factor $PAPR + P_{Constellation}$. Furthermore, quantization noise is spread over whole Nyquist Bandwidth, i.e.

$$\begin{aligned} P_{noise}[dBm/MHz] = P_{signal}[dBm/MHz] - SNR - 10 \cdot \log\left(f_{Nyquist}[MHz]\right) + \\ PAPR + P_{constellation} \\ = 6dBm/Hz - 62dB + 9.6dB + 2.15dB - 30dB \approx -74dBm/Hz \end{aligned} \tag{2.15}$$

for $N = 10$ thermometric bits. P_{Noise} stays therefore within ETSI EN 300 328 requirements for the whole spectrum with the proposed number of thermometric bits in example.

2.3.4 Harmonic Distortion

The Amplitude-to-Amplitude (AM/AM) static distortion characterizes the digital-to-analog converter relationship between input-referred voltage, which is linear to digital-code amplitude, and the output voltage, measured at the output. The output voltage of a RF-DAC, is defined as the amplitude of the fundamental-tone measured on the output. Since the measure is static, after changing input-referred voltage, enough time is allowed for the output to settle before measuring the output voltage. Integral-non-linearity (INL) and differential-non-linearity (DNL) are derived out of AM/AM characterization of the circuit.

AM/AM curve can be often approximated by a polynomial equation, i.e.

$$y = x + \alpha x^2 + \beta x^3 \tag{2.16}$$

where if $\alpha = 0$ and $\beta = 0$ the AM/AM relationship of an ideal DAC if found, where output voltage is perfectly linear to the input-referred voltage. When, for example, $\beta = 0$ and $\alpha \neq 0$, a sinusoidal tone at the input of the circuit is distorted to

$$\begin{aligned} y &= sin(\omega t) - \alpha sin(\omega t)^2 \\ &= sin(\omega t) - \frac{\alpha}{2}\left[1 - cos(2\omega t)\right] \end{aligned} \tag{2.17}$$

and a tone with frequency 2ω is appearing in the spectrum. In the specific case of the RF-DAC, the sum of many sinusoidal tones, building up the OFDM base-band spectrum, is shifted at frequency f_c, and then undergoes a high-order polynomial distortion. In particular, the third-order distortion of a sine-wave tone at frequency ω_2 mixed with a tone at frequency

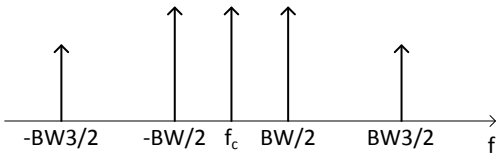


Figure 2.17: Third-order Harmonics of a Sine-Wave centered at f_c

ω_1 introduces tones at frequencies $\omega_1 \pm \omega_2$, $\omega_1 \pm 3\omega_2$, $3\omega_1 \pm \omega_2$ and $3\omega_1 \pm 3\omega_2$, with a spectrum which resembles that of Fig. 2.17,

In a modulated signal, a tone at the edge of the bandwidth BW, i.e. at frequency $f_c - BW/2$, produces a harmonic tone at $f_c - BW \cdot 3/2$. Furthermore, all tones between $f_c \pm BW/2$ produce harmonic tones between $f_c \pm BW \cdot 1/2$ and $f_c \pm BW \cdot 3/2$. The distance between $f_c \pm BW \cdot 3/2$ and $f_c \pm BW/2$ is BW, so that all close-in third-harmonics inter-modulation products fall within ETSI 300 328 out-of-band emissions specifications, which have to be met when both first or last channels within ISM bandwidth are selected. The distance measured between in-band and out-of-band power on Fig. 2.12a is $21dB$, therefore this is the maximum level of $CIM3$ which can be allowed.

In case $CIM3$ is too high, with respect to achieved system performance, a Digital Pre-Distortion (DPD) algorithm can reduce the amount of second and higher-order distortion with a counter-equalization curve. However, the presence of hysteresis in the distortion could require a very complex and computation-intensive algorithm, and in general degrade SNR performance of the system, therefore the level of inter-modulation products should be kept as low as possible.

2.3.5 Phase Noise

Active and passive devices in the signal chain of the System introduce thermal noise which sums up to other circuit's noise sources. The analog signal is generated at the node where the digital-input code is converted to an analog voltage, by means of switching as many cells from V_{ss} to V_{dd} as required, as described in Sec. 3.1. The impact of noise introduced by active devices, when operated in linear region, i.e. when operating as a clamp, is limited. By

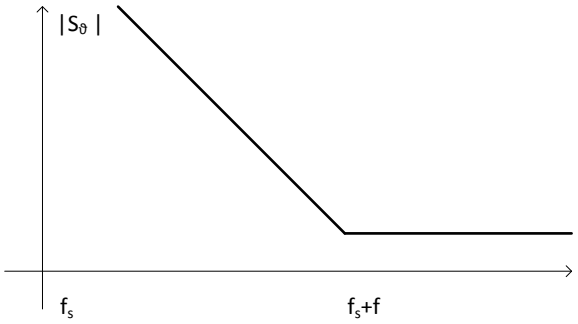


Figure 2.18: Reference clock phase-noise

contrast most of the noise accumulates during switching activities, in terms of phase noise, translating into an uncertainty in RF-DAC clock timing, i.e. jitter.

A detail explanation of off-band phase-noise of over-sampled DAC systems can be found in [16]. Formally, given the signal at the output of the DAC,

$$S_{output}(\omega) = \frac{1}{T}\frac{4sin^2\left(\frac{\omega T}{2}\right)}{\omega^2}S_{baseband}(\omega) \tag{2.18}$$

noise spectral density is calculated by means of a convolution of the spectral noise of the clock at f_{sample} with the signal itself, i.e.

$$S_{noise}(\omega) = \frac{1}{T}\left[\frac{4sin^2\left(\frac{\omega T}{2}\right)}{\omega^2}S_{baseband}(\omega) * \frac{\omega^2}{f_{sample}^2}S_{phase\,noise}\right] \tag{2.19}$$

therefore, for a single tone signal (i.e., $A_i \cos \omega_i t$), phase noise error becomes

$$S_{noise}(\omega) = \frac{1}{T}\left[\frac{4sin^2\left(\frac{\omega T}{2}\right)}{\omega^2}\frac{\pi A_i^2}{2}\left(\delta(\omega-\omega_i)+\delta(\omega+\omega_i)\right)(\omega) * \frac{\omega^2}{f_{clock}^2}S_{phase\,noise}\right] \tag{2.20}$$
$$= \frac{1}{T}\frac{4sin^2\left(\frac{\omega T}{2}\right)}{\omega^2}\frac{\pi A_i^2}{2}\frac{\omega^2}{f_{clock}^2}\left[\left(S_{phase\,noise}(\omega-\omega_i)+S_{phase\,noise}(\omega+\omega_i)\right)\right]$$

and

$$\frac{S_{noise}}{S_{output}} = \left(\frac{\omega_i}{\omega_s}\right)^2\left(S_{phase\,noise}(\omega-\omega_i)+S_{phase\,noise}(\omega+\omega_i)\right) \tag{2.21}$$

For a multi-toned signal, in case the phase noise frequency curve is flat in the off-band frequencies of interest such as in Fig. 2.18, which is usually the case for typical $CMOS$ phase noise spectrum for large frequency offsets, it is

$$\frac{S_{noise}}{S_{output}} = 4S_{phase\,noise}\sum_{k=1}^{M}\left(\frac{\omega_k}{\omega_s}\right)^2 \tag{2.22}$$

or, in dBc/Hz,

$$\frac{S_{noise}}{S_{output}} = S_{phase\,noise}[dBc/Hz] - 20\log(f_s/2) + 10\log\sum_{k=1}^{M} f_k \tag{2.23}$$

By choosing an adequate clock source and designing the LO-path of the System so that it overall exhibit a thermal noise below $-150dBc/Hz$ at large offsets, for sure out-of-band and spurious domain ETSI noise specifications requiring $-41dBc/MHz - 10\log 1MHz = -101dBc/Hz$ are met. In fact, applying Eq. 2.23

$$\frac{S_{noise}}{S_{output}} = -150 - 20\log\left(0.6\cdot 10^9\right) + 10\log\left(\sum_{k=1}^{N}\frac{k}{N}B\right) = -150 - 175 + 160 = -165dBc/Hz \tag{2.24}$$

where $B = 20MHz$ and $n = 64$ subcarriers have been considered in the calculations, is

found.

2.4 Contributors to Error-Vector Magnitude

The effect of a high noise within signal bandwidth is that of a degradation of the transmitted signal as shown in Fig. 2.19. A number of wrong symbol could, as in the case shown in Fig. 2.19, be received by the receiver. The quality of in-band transmitted signal is in-fact often measured in terms of error-vector magnitude (EVM). The error-vector measures the distance between each transmitted signal and its corresponding constellation point, which in an ideal System would be zero for all transmitted points. The root-mean-square of all collected error-vectors represents the collected error power, i.e. P_{error}. EVM is then defined as the ratio between the power of the error P_{error} and the power of the signal P_{signal}

$$EVM[dB] = 10 \log \frac{P_{error}}{P_{signal}} \tag{2.25}$$

The Wi-Fi Alliance enforces the use of the Wi-Fi brand only to devices fulfilling technological requirements based on the IEEE 802.11 standards from the IEEE. Therefore, a device marketed with Wi-Fi brand, has to adhere IEEE 802.11 standard. The IEEE standard defines a minimum transmitter modulation accuracy EVM test [17]. The maximum allowed EVM readouts are shown in Table 2.2.

In total, to fulfill EVM requirements, an SNR of

$$SNR[dB] = EVM[dB] + PAPR[dB] = 36dB \tag{2.26}$$

has to be achieved for a sinusoidal-tone within the signal bandwidth. The in-band SNR is affected by Quantization Noise, Harmonic Distortion and Phase Noise. With 10 thermometric bits and $1.2GHz$ bandwidth, Quantization Noise integrated over $20MHz$ bandwidth, i.e. $QN - 10 \log {}^{1.2GHz}/_{20MHz}$ meets the specifications with margin, whilst other relevant non-idealities are analyzed in the following sections of this Work.

Table 2.2: Allowed relative constellation error versus constellation size and coding rate

Modulation	**Coding rate**	**EVM [dB]**
BPSK	1/2	–5
QPSK	1/2	–10
QPSK	3/4	–13
16-QAM	1/2	–16
16-QAM	3/4	–19
64-QAM	2/3	–22
64-QAM	3/4	–25
64-QAM	5/6	–27

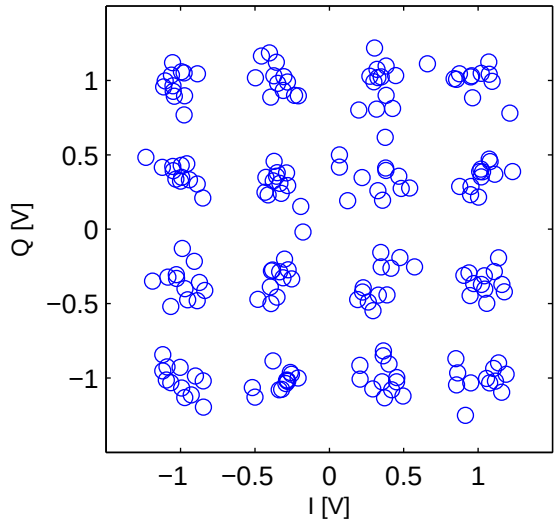


Figure 2.19: Noisy Constellation

2.4.1 Phase Noise

When phase error ϕ is small, transmitted OFDM Signal is rewritten as,

$$\begin{aligned} s &= \sum_{n=0}^{N-1} e^{-i\frac{2\pi}{N}n} a_n \cdot e^{i\phi(m)} \\ &\approx \sum_{n=0}^{N-1} e^{-i\frac{2\pi}{N}n} a_n \cdot [1 + i\phi(m)] \end{aligned} \tag{2.27}$$

where it possible to recognize the original signal, and an error term which is proportional to the phase error, i.e.

$$s = s_o + \epsilon \tag{2.28}$$

The power of the error can be estimated by taking the expectation of the square of the error signal, $E[|\epsilon|^2]$, which in this particular case results in [18]

$$E[|\epsilon|^2] = \sigma^2 E[|s_o|^2] \tag{2.29}$$

thus

$$SNR = \frac{E[|s_o|^2]}{\sigma^2 E[|s_o|^2]} = \frac{1}{\sigma_2} \tag{2.30}$$

where σ^2 is bounded to phase noise by Eq. 2.31,

$$\sigma^2[rad/s] = 2\pi \int_{b_o}^{b} \frac{2No_p}{C} df \tag{2.31}$$

It is in fact possible in the Receiver to de-correlate an error of phase which is in common with all subcarriers, i.e. an error of phase which is not changing during frame time, and remove it. Therefore, for the sake of EVM impairments, b_o, the edge of the integration bandwidth, can be taken as $\Delta f_{carrier}$, spacing between sub-carriers, i.e. $b_o = 20MHz/64 = 312.5kHz$. Variations of phase below this frequency, are slow enough to impact the whole frame the same, and therefore a rotation at the receiver can reconstruct the original signal.

If in the range of integration, phase noise N has a $1/f$ shape, we have

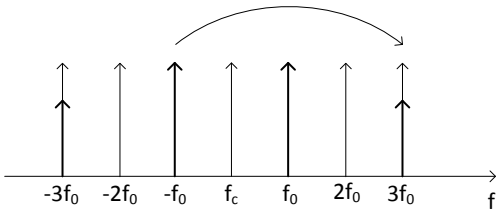


Figure 2.20: Degradation of Signal Quality by Harmonic Distortion

$$\int_{b_o}^{b} \frac{N(b)}{b}\frac{1}{f}df = \frac{N(b)}{b}(ln(b) - ln(b_o)) \tag{2.32}$$

i.e. with $N(20MHz) = -150dBc/Hz$, the EVM specification is fully satisfied, in fact in the case applying Eq. 2.32,

$$\begin{aligned} SNR &= -\left[+10\log 2\pi + 10\log 20MHz - A[dBc/Hz] + 3dB + ln(20MHz) - ln(312.5kHz)\right] \\ &= 61dB \end{aligned} \tag{2.33}$$

2.4.2 Harmonic Distortion

The harmonics of the close-in sub-carriers of transmitted OFDM signal might fall within signal bandwidth and therefore affect the accuracy of the transmitted signal. Since sub-carriers are uncorrelated one another, a sub-carrier falling as an harmonic into another sub-carrier can be considered as a noise source for the victim sub-carrier. Signal harmonics falling within bandwidth acting as a noise source, degrade overall signal-to-noise ratio of the transmitter.

The harmonics power is usually dominated by counter-inter modulation harmonics of third-order, which appear at

$$f_h = f_c + 3N \cdot f_s \tag{2.34}$$

with f_c being channel frequency and f_s spacing between subcarriers, where it is possible to see that, all sub-carriers located at frequencies f_h are affected by impairments from harmonic distortion. One-third of the whole set of sub-carriers is affected by close-in third-order harmonics distortion. Therefore, the maximum third-order harmonics power allowed to meet the error-vector-magnitude is,

$$27dB - 10\log(3) = 23dBc \tag{2.35}$$

However, pre-distortion techniques can reduce the amount harmonic distortion generated through the radio-frequency digital-to-analog converter, improving the error-vector-magnitude performance at the cost of an increased complexity of the transmitter, especially in case the distortion is affected by memory effects.

2.4.3 In-Phase/Quadrature-Phase Imbalance

The I/Q imbalance is limited in the particular System Design adopted, as described in Sec. 4.1.1. In fact, the whole clock distribution delivers a 4.8GHz clock, out of which a 2.4GHz clock with I and Q edges are derived locally as shown in Fig. 4.1. From the node where the 4.8GHz is locally divided, then, subsequent paths to the output are completely symmetrical. It is therefore safe to expect negligible performance degradation due to I/Q imbalance.

2.5 Receiver Desensitization

Tougher out-of-band specifications arise in case the Wi-Fi device is required to cooperate with other standards in a mobile device. A typical use case where the cooperation of multiple standard of communications within one device is important is, for example, when LTE is considered as a backhaul link to access the Internet, and the connectivity is shared by other local users using Wi-Fi. For example, this happens when the Wi-Fi transceiver acts as an access point (AP) sharing an available in-device LTE Connection [19].

As can be seen in Table 2.3, for example, TDD licensed band 7, 38, 40 and 41 reach close-by to unlicensed $2.4GHz$ ISM band. The level of coupling between in-device Wi-Fi and LTE antenna cannot be calculated through classic Friis Transmission Equation, since

Table 2.3: Evolved Universal Terrestrial Radio Access (E-UTRA) operating bands [4]

E-UTRA Band	**Uplink (UL) Operating Band**	**Downlink (DL) Operating Band**	**Duplex Mode**
1	1920 MHz – 1980 MHz	2110 MHz – 2170 MHz	FDD
2	1850 MHz – 1910 MHz	1930 MHz – 1990 MHz	FDD
3	1710 MHz – 1785 MHz	1805 MHz – 1880 MHz	FDD
4	1710 MHz – 1755 MHz	2110 MHz – 2155 MHz	FDD
5	824 MHz – 849 MHz	869 MHz – 894MHz	FDD
6	830 MHz – 840 MHz	875 MHz – 885 MHz	FDD
7	2500 MHz – 2570 MHz	2620 MHz – 2690 MHz	FDD
8	880 MHz – 915 MHz	925 MHz – 960 MHz	FDD
9	1749.9 MHz – 1784.9 MHz	1844.9 MHz – 1879.9 MHz	FDD
10	1710 MHz – 1770 MHz	2110 MHz – 2170 MHz	FDD
11	1427.9 MHz – 1447.9 MHz	1475.9 MHz – 1495.9 MHz	FDD
12	699 MHz – 716 MHz	729 MHz – 746 MHz	FDD
13	777 MHz – 787 MHz	746 MHz – 756 MHz	FDD
14	788 MHz – 798 MHz	758 MHz – 768 MHz	FDD
15	Reserved	Reserved	FDD
16	Reserved	Reserved	FDD
17	704 MHz – 716 MHz	734 MHz – 746 MHz	FDD
18	815 MHz – 830 MHz	860 MHz – 875 MHz	FDD
19	830 MHz – 845 MHz	875 MHz – 890 MHz	FDD
20	832 MHz – 862 MHz	791 MHz – 821 MHz	FDD
21	1447.9 MHz – 1462.9 MHz	1495.9 MHz – 1510.9 MHz	FDD
22	3410 MHz – 3490 MHz	3510 MHz – 3590 MHz	FDD
23	2000 MHz – 2020 MHz	2180 MHz – 2200 MHz	FDD
24	1626.5 MHz – 1660.5 MHz	1525 MHz – 1559 MHz	FDD

Table 2.3: Continued

25	1850 MHz – 1915 MHz	1930 MHz – 1995 MHz	FDD
26	814 MHz – 849 MHz	859 MHz – 894 MHz	FDD
27	807 MHz – 824 MHz	852 MHz – 869 MHz	FDD
28	703 MHz – 748 MHz	758 MHz – 803 MHz	FDD
29	N/A	717 MHz – 728 MHz	FDD
30	2305 MHz – 2315 MHz	2350 MHz – 2360 MHz	FDD
31	452.5 MHz – 457.5 MHz	462.5 MHz – 467.5 MHz	FDD
32	N/A	1452 MHz – 1496 MHz	FDD
33	1900 MHz – 1920 MHz	1900 MHz – 1920 MHz	TDD
34	2010 MHz – 2025 MHz	2010 MHz – 2025 MHz	TDD
35	1850 MHz – 1910 MHz	1850 MHz – 1910 MHz	TDD
36	1930 MHz – 1990 MHz	1930 MHz – 1990 MHz	TDD
37	1910 MHz – 1930 MHz	1910 MHz – 1930 MHz	TDD
38	2570 MHz – 2620 MHz	2570 MHz – 2620 MHz	TDD
39	1880 MHz – 1920 MHz	1880 MHz – 1920 MHz	TDD
40	2300 MHz – 2400 MHz	2300 MHz – 2400 MHz	TDD
41	2496 MHz – 2690 MHz	2496 MHz – 2690 MHz	TDD
42	3400 MHz – 3600 MHz	3400 MHz – 3600 MHz	TDD
43	3600 MHz – 3800 MHz	3600 MHz – 3800 MHz	TDD
44	703 MHz – 803 MHz	703 MHz – 803 MHz	TDD

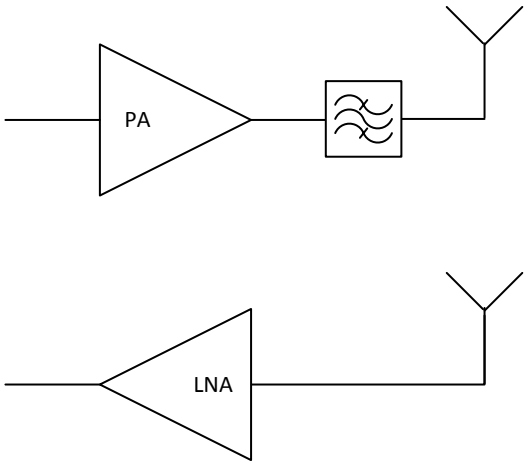


Figure 2.21: Coexistence

this equation does not apply when the distance between receving and transmitting antenna is comparable to wavelength $\lambda = \frac{c}{f} = 12.5cm$, with an attenuation varying a lot between different antenna sizes and configurations. However, between a Wireless transmitter and an LTE receiver operating at the same time on the same device, 10 or more dB of antenna attenuation [20], depending on antenna orientations and distances can be assumed.

Typically, a BAW, or SAW filter is inserted in the Wireless Transmitter chain to mitigate in-device coexistence problems, as shown in Fig. 2.21. However this filter is both lossy, and has a transition region which is not infinitely sharp, and which might depend on temperature and process variation, making it hard to filter out Wi-Fi unwanted emissions exactly in the near-by of an LTE channel. The filter has in fact to be quite steep since the transition region has a limited span in frequency, i.e. between Wi-Fi Channel 13 extending up to $2.4835GHz$, only $11MHz$ of guard interval exist to the lower edge of LTE Band 41, located at $2.496GHz$.

Whilst maximum allowed power for meeting ETSI specifications for out-of-band emissions in a $20MHz$ channel is of $-30dBm + 10\log(20) = -17dBm$, the sensitivity of a LTE receiver, is to signals down-to below $-90dBm$ [4]. Even accounting the $10dB$ or more intrinsic attenuation between the antennas operating the different standards, the requirements on the filter for this approach are very though, especially for the critical use-case where transition

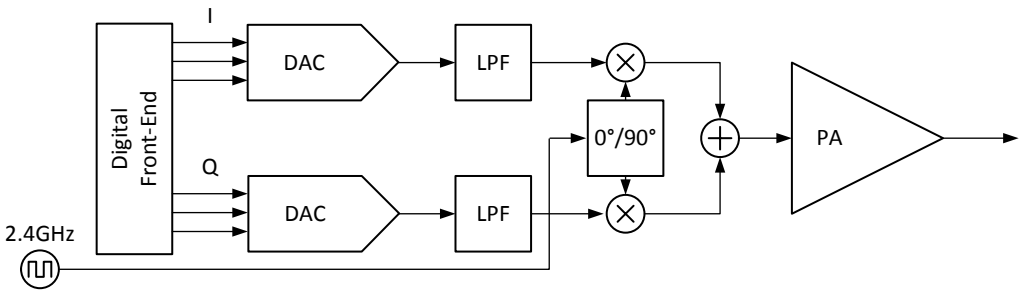


Figure 2.22: Analog Intensive Architecture

band is limited. To avoid excessive de-sensitization of receivers and relax filter specifications, lower emissions than those allowed by ETSI and IEEE standards for the sake of device certification, are targeted in the Transmitter, in case a device is designed to operate multiple wireless transceivers standards at the same time.

2.6 Survey of Transmitter Architectures

2.6.1 State-of-the-art Analog-Intensive Architecture

A textbook design of a Transmitter for Wireless Applications [21] comprises several analog and mixed/signal blocks, and is therefore an analog-intensive Architecture. As it is shown in Fig. 2.22, the Architecture comprises,

- A Digital Front-End (DFE). The Digital Front-End is the source of the samples which are subsequently transmitted by the Wireless Transmitter. The Symbols sourced by the DFE are, in case an OFDM System is designed, already the time-domain representation of the transmitted OFDM Symbol, as shown in Fig. 2.2b, and therefore comprise the time-set of digital Symbols which represents the frequency-set of Symbols transmitted by the Transmitter

- Two twin Digital-to-Analog Converters (DAC), operating the conversion of the I and of the Q time-set of digital Symbols into I and Q analog trajectories respectively.

Each of the symbol sourced by the DFE is in-fact complex, and comprises an In-Phase component and a Quadrature-Component. At this stage, only a base-band signal is synthesized, including all desired Transmitted Signal frequency components centered at DC frequency

- Two twin Low-Pass Reconstruction-Filters (LPF). The filter removes undesired frequency components arising from digital-to-analog conversion process. A cut-off frequency set after the edge of the bandwidth of the synthesized digital Signal, guarantees that wanted spectral components are neither attenuated, nor distorted, and at the same time enough attenuation is provided to the unwanted frequency components

- A Quadrature-Mixer, shifting synthesized frequency components of the Signal to the selected channel-frequency provided by the Reference RF Clock. The two twin I and Q paths are mixed with the Reference RF Clock and with the Reference RF Clock phase-shifted by 90°, respectively. When the two twin Signal paths are summed up one with the other, the twin real-signals generate a complex signal, which does not exhibit a Hermitian Symmetry around the Reference Clock frequency, but instead exhibits Hermitian Symmetry around DC Frequency only. In fact, thanks to the Quadrature-Mixer, the twin Single-Side-Band (SSB) Signals which are the generated at the output of the digital-to-analog converters (DAC) are combined to form a double side-band (DSB) Signal around Reference Clock frequency

- A Power-Amplifier (PA). The PA receives the signal of the Transmitter and adds adequate power to it so that it can operate the Antenna adequately. In fact, the chain of analog-blocks preceding the PA operates with Signals at low power-level and therefore amplification is required. A significant amount of unwanted noise and distortion is added during the amplification of the signal operated by the PA. Previous stages noise specifications are constrained, in order to accommodate for the significant degradation of performance which is induced by the PA

Nyquist-Shannon sampling theorem ensures that a Signal sampled at a sampling frequency $f_{sampling}$, which has to be at least two-times that of the Signal with bandwidth $f_{bandwidth}$, can ideally be exactly reconstructed through an adequate reconstruction filter,

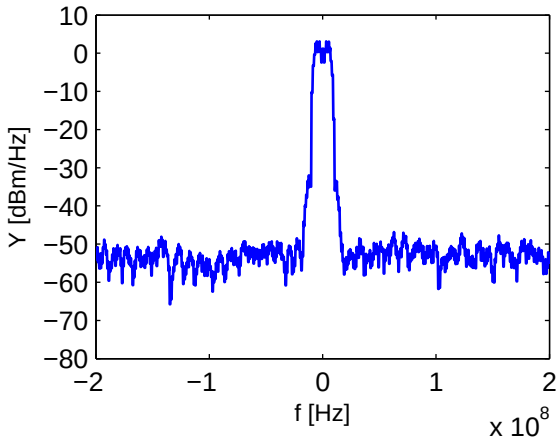


Figure 2.23: Absolute Value of Signal Frequency Components

to the analog-domain. The Analog-Intensive System described in this Section comprises a quadrature mixer, which forms a double-sided Signal after mixing each of the two twin single-sided I and Q Signals sourced by the Digital-Front-End. Therefore, at the output of the quadrature mixer, frequency components in the range q,

$$q = [-\frac{f_{sampling}}{2}, +\frac{f_{sampling}}{2}] + f_{RF} \tag{2.36}$$

where $f_{sampling}$ is the sampling frequency at which the Synthesizer operates, can be correctly reconstructed. I.e., the Synthesizer operated as a source of two digital Signal sampled at $f_{sampling}$ frequency, correctly sets the frequency components of channel of bandwidth $f_{bandwidth} = f_{sampling}$. Quantization noise requirements of the DAC for EVM impairments are explained in Sec. 2.4.

However, to relax the specifications of Low-Pass Reconstruction-Filter, the digital-front-end $f_{sampling}$ frequency is generally extended above $f_{bandwidth}$, to take advantage of the zero of the sinc around sampling frequency explained in Sec. 2.3.2. In fact, by increasing the sampling frequency the images of the reconstructed Signal are pushed to higher frequencies, minimizing the amplitude of the images, and improving the attenuation of the filter. Allowing a lower-order filtering is in fact often more critical than increasing the digital-front end operating frequency over the minimum frequency allowed by Nyquist-Shannon sampling theorem.

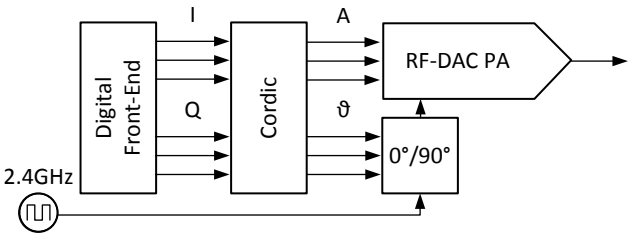


Figure 2.24: Polar Digital-Intensive Architecture

The analog quadrature mixer specifications, instead, cannot be relaxed by tweaking the digital-front end. Any non-linearity in the mixer degrades in fact out-of-band emissions and in-band signal quality, as explained in Sec. 2.4.2 and 2.3.4. Furthermore, unwanted effects of phase-noise in the mixer are described in Sec. 2.4.1 and Sec. 2.3.5.

Finally, the Power-Amplifier has to provide required power gain so that antenna power level is reached. The PA shall exhibit the power level which has been described in Sec. 2.2 at its output, at the same time, nonetheless, the PA shall meet the distortion specifications explained in Sec. 2.4.2. Furthermore, in order not to impair noise specifications achieved in the DAC, in the Filters and in the Mixer, an adequate PA noise-figure is required.

2.6.2 Polar Digital-Intensive Architecture

The introduction of high dynamic-range digital-to-analog converter (DAC) running at RF frequency, i.e. the RF-DAC, enables the development of a more digital-intensive System [22] and [23]. The digital-intensive polar architecture can be seen as an evolution of the analog-intensive Architecture, relying on the excellent performance of digital and mixed/signal blocks achieved in advanced CMOS Technologies. It comprises,

- A Digital Front-End (DFE). As already described in Sec. 2.6.1, the Digital Front-End is the source of the samples which are subsequently transmitted by the Wireless Transmitter. The Symbols sourced by the DFE are, in case an OFDM System is designed, again already the time-domain representation of the transmitted OFDM

Symbol, as shown in Fig. 2.2b, and therefore comprise the time-set of digital Symbols which is represents the frequency-set of Symbols transmitted by the Transmitter

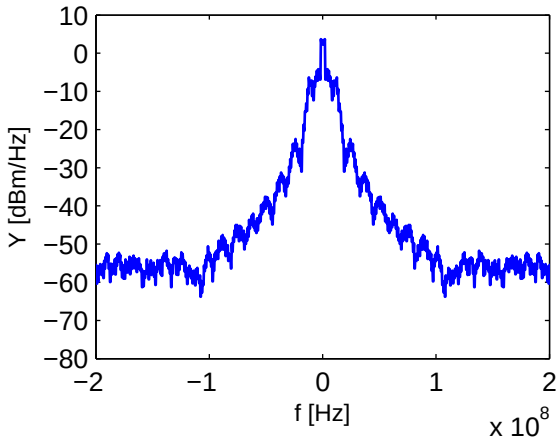
- A Cordic Converter turning the In-Phase/Quadrature-Phase digital Signal into an Amplitude/Phase digital Signal [24]. The Cordic is a fully-digital block which complements the DFE and does not introduce any change to the Transmitted Signal, but it allows the Polar Transmitter to operate with digital samples defined in the Amplitude/Phase domain rather than in the In-Phase/Quadrature-Phase domain

- A Digital Phase-Locked Loop (DPLL) turning Phase Information on the Phase component of the digital Signal into a Phase-Modulation of the Reference RF Clock. Inside the DPLL, there is a Digital-Control Oscillator (DCO) which generates a clock at desired channel frequency, whose phase information is measured by a time-to-digital converter (TDC) and adjusted in feedback by the DPLL to track the changes of the Phase digital Signal

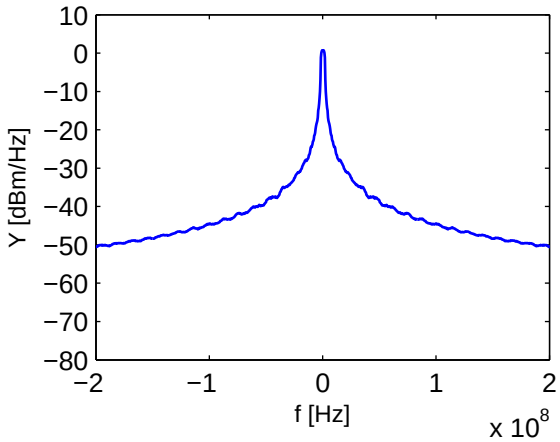
- A RF-DAC PA modulating the Amplitude of its Reference RF Clock to the Amplitude of the digital Amplitude Signal. Since the Reference RF Clock of the RF-DAC is modulated by the DPLL according to the Phase component of the digital Signal, the mixing operation described in Sec. 2.3.2, which the RF-DAC operates between the Amplitude and the modulated Reference RF Clock, fully reconstructs the Transmitted Signal. Furthermore, thanks to a high-power output stage design, the RF-DAC PA does not require further Amplification Stages and can be directly connected to an Antenna load. The required Antenna output power, described in Sec. 2.2, is in fact directly generated in the RF-DAC output stage

In a comparison to the Analog-Intensive System previously described in Sec. 2.6.1, a highly digital line-up is observed in the Polar Digital-Intensive Architecture. Both the RF-DAC, and the DPLL, are in fact mixed/signal blocks, whilst the Cordic and the DFE are fully-digital blocks.

The Polar Digital-Intensive Architecture embeds the Power Amplifier functionality in the Mixed/Signal Architecture of the RF-DAC. In the RF-DAC, the output stage which is delivering the power to the load is a switching-output stage, and thus rail-to-rail voltage



(a) Amplitude Frequency Components



(b) Phase Frequency Components

Figure 2.25: Polar Digital-Intensive Architecture Frequency Components

swing can be achieved, maximizing the power handling capabilities and the efficiency of the topology. The addition of a Cordic converter, does not alter the power consumption of the Transmitter significantly, and the Cordic can be placed and routed through the use of automated tools in a small area.

However, the Polar System achieves a lower maximum Synthesized Signal Bandwidth compared the maximum Synthesized Signal Bandwidth achieved by the previously described In-Phase/Quadrature-Phase Architecture. When the Amplitude/Phase digital Signal transformed by the Cordic are analyzed, in fact, expanded spectral components, compared to the In-Phase/Quadrature-Phase digital Signal is observed. In example, in the Single-Side-Band

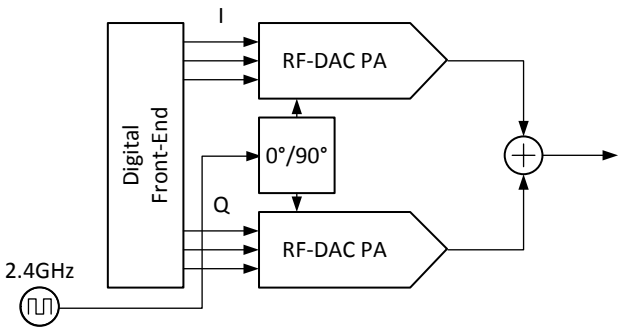


Figure 2.26: Digital I/Q Architecture

Bandwidth of the digital Signals shown in Fig. 2.25a and 2.25b Signal frequency components extend up to $100MHz$, whilst in the Single-Side-Band Bandwidth of the very same digital Signals depicted in Fig. 2.23 for In-Phase/Quadrature-Phase digital Signal, and extension of only $10MHz$ is observed.

In fact, the geometric functions which map In-Phase/Quadrature-Phase Coordinates to Amplitude/Phase Coordinates in the Cordic are highly non-linear. Therefore, the Signals at the output of the Cordic exhibit relevant harmonic components introduced by the non-linearity of the mapping. In practice, for a required Synthesized Signal Bandwidth, the design of a Polar System does either stress the specifications of the Mixed/Signal Blocks to their extremes, or, for some Applications, might not be a viable choice.

2.6.3 Proposed Digital I/Q Architecture

In order to avoid the limitations of the Polar Digital-Intensive Architecture, without falling back to the Analog-Intensive Architecture previously described, a novel Digital-Intensive Architecture is proposed. On the basis of an In-Phase/Quadrature-Phase digital Signal Path, the proposed Digital I/Q Architecture comprises,

- A Digital Front-End (DFE). As already described in Sec. 2.6.1, the Digital Front-End is the source of the samples which are subsequently transmitted by the Wireless Transmitter. The Symbols sourced by the DFE are, in case an OFDM System is

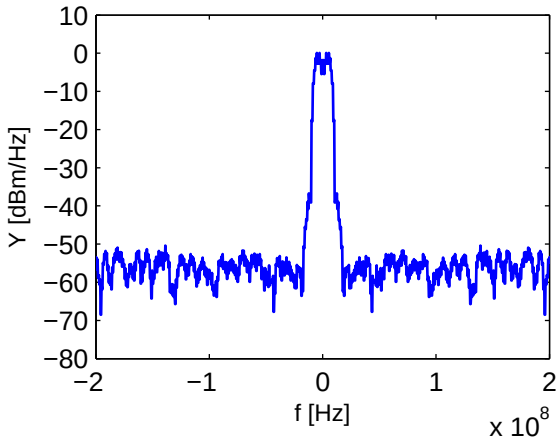
designed, again already the time-domain representation of the transmitted OFDM Symbol, as shown in Fig. 2.2b, and therefore comprise the time-set of digital Symbols which represents the frequency-set of Symbols transmitted by the Transmitter

- Two twin RF-DAC PA modulating the Amplitude of their Reference RF Clocks to the In-Phase and to the Quadrature-Phase Components of the Synthesized Digital Signal respectively. The two twin In-Phase and Quadrature-Phase RF-DAC are connected to the Reference RF Clock and to the Reference RF Clock phase-shifted by 90° respectively. Therefore, when the two twin Signal paths are summed up one with the other, the twin real-signals generate a complex signal, which does not exhibit a Hermitian Symmetry around the Reference Clock frequency, but instead exhibits Hermitian Symmetry around DC Frequency only. In fact, thanks to the Quadrature-Mixing, the twin Single-Side-Band (SSB) Signals which are the generated at the output of the digital-to-analog converters (DAC) are combined to form a double side-band (DSB) Signal around Reference Clock frequency, analogously to the Quadrature Mixer operation of Sec. 2.6.1

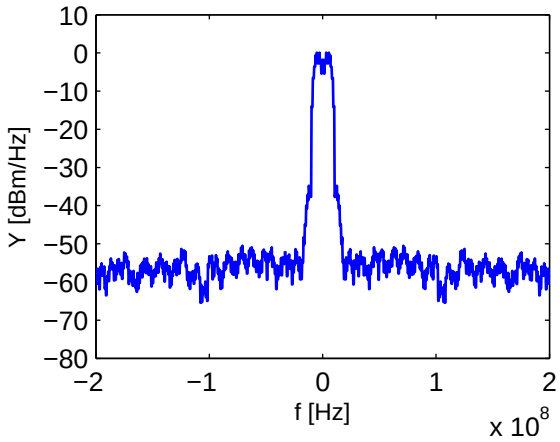
Analogously to the Polar Digital-Intensive Architecture, the Digital I/Q Architecture is completely made out of either digital or mixed/signal blocks, in fact, no analog blocks are employed within the transmitter. Furthermore, this Architecture has only one node where the voltage is necessarily analog, in the node where the voltages generated by the two twin RF-DAC is summed up, which is the output node of the Architecture.

Synthesized Digital Signals bandwidth of the Digital I/Q Architecture is lower in comparison to the Synthesized Digital Signals bandwidth required in the Polar Digital-Intensive Architecture described in Sec. 2.6.2. As shown in Fig. 2.27a and in Fig. 2.27b, in fact, due to the consideration described in Sec. 2.6.1, the Synthesizer, when operated as a source of In-Phase/Quadrature-Phase digital Signal sampled at $f_{sampling}$ frequency, correctly sets the frequency components of channel of bandwidth $f_{bandwidth} = f_{sampling}$.

A drawback of the Proposed Digital I/Q Architecture, is that in comparison with the Polar Digital-Intensive Architecture, for the same Modulated Output Power of the Transmitter, $3dB$ higher Output Power might be required in the Digital I/Q Architecture. In fact, due to the consideration described in Sec. 2.2.3, the maximum transmitted Signal Power,



(a) In-Phase Frequency Components



(b) Quadrature Frequency Components

Figure 2.27: Digital I/Q Architecture Frequency Components

occurring at $\pm 1 \pm j$ on the I/Q phase-diagram as shown in Fig. 2.11, is higher than the Maximum Transmit Power occurring at valid symbols originated from the DFE, comprising all the points within the circle of ray 1 around the origin on the Phase Diagram. As a result, efficiency of the Transmitter could be lower in the Proposed Digital I/Q Architecture comparing to the Polar Digital-Intensive Architecture. However, the benefits of the Digital I/Q Architecture, which is both completely digital and as well enabling high Modulation Bandwidths, justify the choice of the Architecture in Applications requiring high Modulation Bandwidths, including modern Wireless Communications as well.

Chapter 3

Circuit Design

This part of the Work details the Design of the Transmitter Circuit, and studies the Optimal Design Choices enhancing critical Transmitter Figures-Of-Merit (FOM). First, Capacitive Digital-to-Analog Converter (C-DAC) Circuit is described. Next, after having introduced Radio-Frequency C-DAC Circuit (RF-DAC), as an evolution of C-DAC building-block, the Switched-Capacitor Power-Amplifier (SCPA) is presented. It is seen, that SCPA Switching Output Stage offers excellent power-handling capabilities and high-efficiency at the same time. Subsequently, a companion Matching Network of the SCPA is carefully analyzed, enhancing power transferred at high-efficiency to Antenna load-resistance. Finally, a Series Power Combiner is introduced, further enhancing available output power up to the required Transmit Power at an optimized Transmitter Efficiency.

3.1 Capacitive and Radio-Frequency Digital-to-Analog Converter

The Digital-to-Analog Converter (DAC), as per Sec. 2.1, is a fundamental block in Wireless Transmitters. A DAC Circuit is implemented by using reference Voltages and Currents, generated in Resistor Strings, Resistor Ladders, Current Steering Mechanisms, and Charge-Scaling Architectures. Oversampling Techniques, Loop and Pipeline Techniques are often used to enhance DAC performance [25].

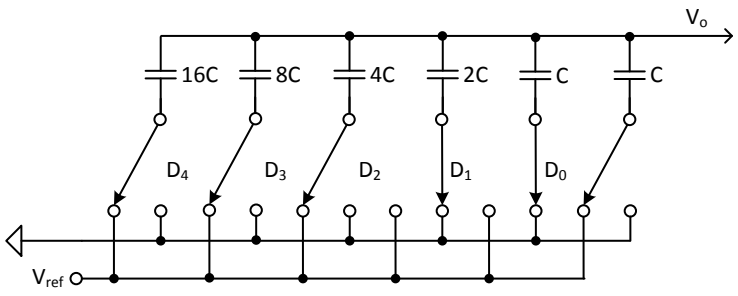


Figure 3.1: Capacitive Digital-to-Analog Converter

Due to its capability to take advantage of Modern CMOS Technology Scaling, the Charge-Scaling C-DAC is often regarded to as one the best Choices for Modern CMOS Designs. This Part of the Work discusses the fundamental equations of the C-DAC building-block, its evolution to the RF-DAC and the highly-linear Thermometric RF-DAC implementation.

3.1.1 Capacitive Digital-to-Analog Converter

The Capacitive Digital-to-Analog Converter (C-DAC) Circuit is formed by a number of Capacitances and Switches connected together as shown in Fig. 3.1. The purpose of the Circuit is that of generating a Voltage on output node V_o, which is proportional to selected input code D [25]. The transfer function from the input code to the output node, is found by applying,

- Superposition-Of-Effects Principle, saying that the Voltage in a given node of a linear circuit can be obtained by superposing Delta-Voltages introduced by the effect of each Voltage source to the given node. This Principle applies to the output node V_o of the C-DAC circuit as well; and

- Capacitive-Divider formula, saying that the Voltage induced by a Voltage generator applied to a Network made by two series Capacitances connected to ground, to the unbounded node of the network, is equal to the Voltage of the Voltage generator scaled down by the ratio of the Network's Capacitance to ground to the Network's total Capacitance.

The C-DAC Circuit, shown in Fig. 3.1 where switch position is set to ground for $D_i = 0$, and to V_{ref} for $D_i = 1$, induces therefore an output Voltage V_o equal to

$$\begin{aligned} V_o =& D_0 \cdot V_{ref} \cdot \frac{C}{C + C + 2C + ... + 2^n C} + \\ & D_1 \cdot V_{ref} \cdot \frac{2C}{C + C + 2C + ... + 2^n C} + \\ & ... + \\ & D_n \cdot V_{ref} \cdot \frac{2^n C}{C + C + 2C + ... + 2^n C} \end{aligned} \tag{3.1}$$

The C-DAC output Voltage V_o is thus given by the equation

$$\begin{aligned} V_o =& V_{ref} \cdot \sum_{i=0}^{i=n} D_i \frac{2^i C}{2^{n+1} C} \\ =& V_{ref} \cdot \sum_{i=0}^{i=n} D_i \frac{2^i}{2^{n+1}} \end{aligned} \tag{3.2}$$

which corresponds to the analog representation of the binary code D. For example, the output node V_o of Fig. 3.1 with binary code

$$D = \left(\begin{array}{c} 00011 \end{array} \right) \tag{3.3}$$

is set to,

$$\begin{aligned} V_o =& V_{ref} \left(\frac{2^1}{2^5} + \frac{2^0}{2^5} \right) \\ =& V_{ref} \frac{3}{32} \end{aligned} \tag{3.4}$$

In Eq. 3.4, 3 is the decimal representation of the number D. 32 at the denominator is instead a constant, setting the minimum voltage step V_{step} which can be represented by this DAC when a unitary change of D is applied, in this case,

$$V_{step} = \frac{V_{ref}}{2^{n+1}} \tag{3.5}$$

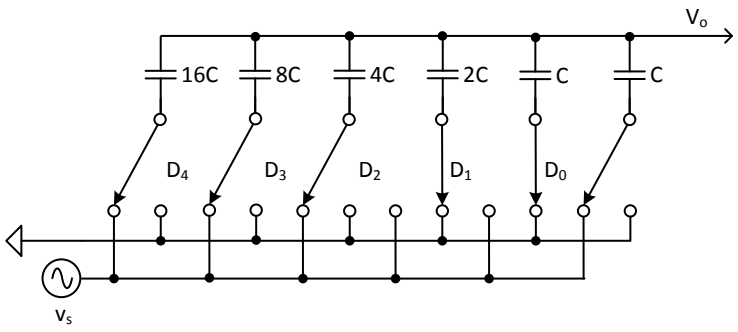


Figure 3.2: Radio-Frequency Capacitive Digital-to-Analog Converter

It is observed that by increasing the number of bits $n+1$ in Eq. 3.5, the magnitude of V_{step} decreases and thus the resolution of the C-DAC is enhanced.

3.1.2 Radio Frequency Digital-to-Analog Converter

Wireless Transmitters transmit on a limited interval of frequencies located around the frequency of the selected Channel. The Digital-to-Analog Converter (DAC) Synthesized Output Signal extends from DC up to half the frequency at which the DAC code D is updated. As shown in Sec. 2.6.1, the DAC is then designed to operate from DC to the bandwidth of the interval of frequencies which are part of the transmission, and a Mixer takes care of shifting the frequency components generated by the DAC to the selected channel frequency. Filters are inserted in the Architecture to avoid unwanted Signal components.

Direct synthesis of the channel and of the transmitted frequency components around the channel, through a DAC, is theoretically possible but would require a very high DAC code D update frequency. DAC code D update frequency would in-fact in this case extend up to two times the frequency at which the Channel is operated, i.e. more than $4.8GHz$ for IEEE 802.11 Standard. In this regard, the Radio-Frequency Digital-to-Analog Converter (RF-DAC) is a useful development of the classic Digital-to-Analog Converter circuit which operates a Direct Channel Synthesis, i.e. it does not require an external Mixer, and has reasonable bandwidth requirements on the digital code Signal D. An example of an RF-DAC is drawn in 3.2, in the form of an RF C-DAC.

The RF-DAC of Fig. 3.2 connects through its switches, again commanded by the input code D, selectively, either to ground, when switch position is set by $D_i = 0$, or to v_s when switch position is set by $D_i = 1$. The set of formulas presented in Sec. 3.1.1 is again valid, with the only difference that in the case of an RF-DAC, $V_{ref} = v_s$ is not a static voltage. In fact, the RF-DAC modulates the sine-wave amplitude of its reference voltage with the envelope contained in the sequence of codes $d(t)$, i.e. yielding

$$V_o(t) = v_s(t) \cdot \sum_{i=0}^{i=n} d_i(t) \frac{2^i}{2^{n+1}} \tag{3.6}$$

As described in 2.3.2, where a detailed mathematical analysis of the RF-DAC is given both in time and frequency domain, in case a zero-order hold is assumed, i.e.

$$d(t) = \sum_{k=-\infty}^{+\infty} rect(t - kT) D(k) \tag{3.7}$$

and in case v_s is synchronous to D update period T, then, the RF-DAC exactly reconstructs a sine-wave whose envelope corresponds to that expressed by the digital Signal D. RF-DAC Synthesized Output Signal, contains therefore a sine-wave located at v_s frequency, modulated by the digital Signal D envelope or, in other terms, comprises a limited interval of frequencies located around the frequency of the selected Channel.

3.1.3 Thermometric Radio-Frequency Digital-to-Analog Converter

RF-DAC INL and DNL are critical in order to obtain good RF performance in terms of error-vector magnitude, spurious content and noise-floor in the System. To obtain the best performance, the C-DAC is organized in a thermometric fashion, so that monotonicity of the transfer curve is guaranteed by design, and matching between edges constant-of-time is ensured by identical layout of each of the designed cell. Furthermore, to avoid back and forth switching of cells of the same column during a ramp-up or ramp-down transition, the array is organized so that, during such an event, the cells are always gradually activated from left to right, and, when then one column fills, columns are added from the top to the bottom

[26]. A number of tricks is subsequently implemented, including the snake-shape trick [27], to improve the RF performance of the RF-DAC.

The thermometric array shown in Fig. 3.3 is organized in Columns and Rows. Each cells receives three signals,

- C horizontal column signal; signaling whether column to which the cell belongs is active or not
- C_{+1} subsequent column signal; signaling whether subsequent column to which the cell belongs is active or not
- R vertical row signal; signaling whether row to which the cell belongs is active or not

A column is active if, and only if, either the subsequent column is active, or, if both current column and current row are active at the same time. Therefore, starting from a unitary code $D_i = 1$ the switching sequence is as follow:

$$S = \begin{pmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \tag{3.8}$$

when control signals are

$$R = \begin{pmatrix} 1 & 0 & 0 \end{pmatrix}, C = \begin{pmatrix} 1 \\ 0 \\ 0 \end{pmatrix} \text{ and } C_{+1} = \begin{pmatrix} 0 \\ 0 \\ 0 \end{pmatrix}$$

Subsequently, the when input D_i is increased by one unit $D_i = 2$,

$$S = \begin{pmatrix} 1 & 1 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \tag{3.9}$$

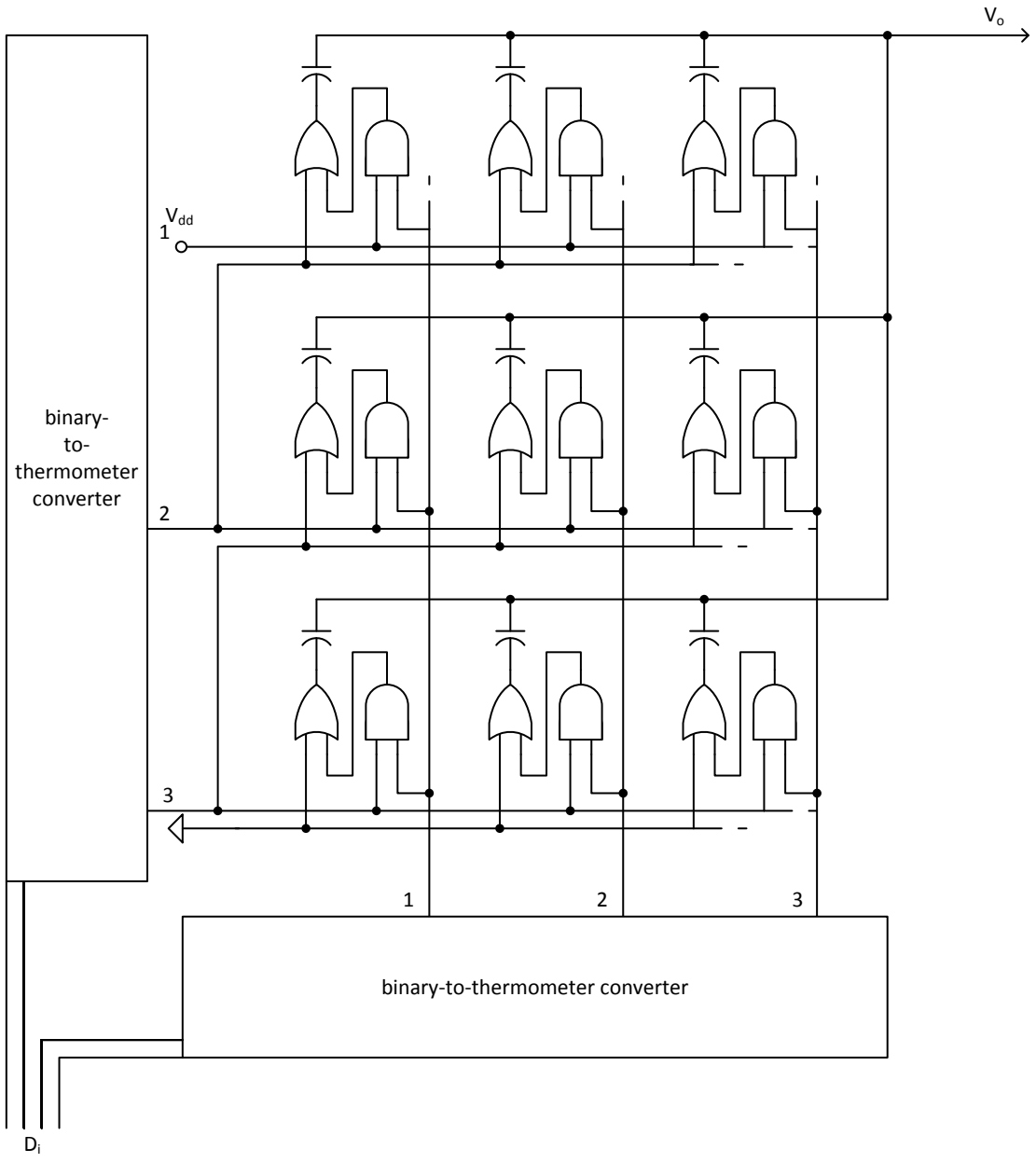


Figure 3.3: Thermometric Array

after control signals are

$$R = \begin{pmatrix} 1 & 1 & 0 \end{pmatrix}, C = \begin{pmatrix} 1 \\ 0 \\ 0 \end{pmatrix} \text{ and } C_{+1} = \begin{pmatrix} 0 \\ 0 \\ 0 \end{pmatrix}$$

Furthermore, when subsequent column is turned on by $D_i = 4$,

$$\begin{pmatrix} 1 & 1 & 1 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \tag{3.10}$$

when control signals are

$$R = \begin{pmatrix} 1 & 0 & 0 \end{pmatrix}, C = \begin{pmatrix} 1 \\ 1 \\ 0 \end{pmatrix} \text{ and } C_{+1} = \begin{pmatrix} 1 \\ 0 \\ 0 \end{pmatrix}$$

At null input code $D_i = 0$, all control signals are zero, as well as status of all cells. By contrast when input code is maximum $D_i = 9$, all control signals are unitary, and as well status of all cells is set to active.

All three signals are necessary for tracking the status of each cell. Intuitively, in fact, the goal of the control Signals is that to define which part of the array is active, and move the edge between active and inactive part of the array, sensitive to row signals, further as the code grows. The position of the edge etween active and inactive part of the array is defined by the C_{+1} signals, the number of active cells on the edge is defined by R signals, and C signals define active and inactive side of the array.

As seen in Fig. 3.3, the RF-CDAC is implemented so that it operates on a square-wave clock, and a sine-wave is then reconstructed at the output by using an LC filter. In this way, all the signals going to the DAC are digital, and therefore the full advantage of CMOS technology scaling are deployed, as is desirable for a C-DAC Architecture.

3.2 Switched-Capacitor Digital-to-Analog Power-Amplifier

At low-frequencies, the Capacitive Digital-to-Analog Converter (C-DAC) does not transfer a significant amount of Power through its output. A resistive load connected from the output to ground, would in fact discharge any charge formed at the output node V_o of the C-DAC in Fig. 3.1, each time this charge is updated by digital input Signal D. However, when the C-DAC switches at fast frequency, such as in the RF-DAC shown in Fig. 3.2, then the absolute value of the impedance of the total C-DAC capacitance C becomes low, and power can transit from the supply to the output load resistance. A RF-DAC operated to transfer power to the load forms therefore a Switched-Capacitor Power-Amplifier (SCPA). In the following pages of the Work, the Design of the SCPA, and of its companion Matching Network, are subsequently described.

3.2.1 A linear Model of Switching Output Stage Efficiency

Traditional transmitter (TX) lineups (see Fig. 2.22) are analog intensive [23], and do not benefit from CMOS technology scaling. The introduction of high dynamic range digital-to-analog converter (DAC) running at RF frequency, a.k.a. RF-DAC, enables a digital intensive solution [23]. The entire TX chain is implemented by digital-like circuit blocks and strongly benefits from CMOS technology scaling, except for the off-chip analog Power Amplifier (PA) [22]. The next step towards the software defined radios forcast by Mitola [28] is to incorporate the PA in the mixed-signal output stage of the DAC [23]. A digital TX with no external PA has already been demostrated in [29] and in [30] as sketched in Fig.2.24, where a SCPA has been adopted.

This part of the Work presents a linear model for the power and efficiency of the SCPA at full scale. This model can be used to accurately size the output stage of this new class of circuits by means of simple equations.

3.2.1.1 Full-Scale Model

A SCPA is a Capacitive-DAC (C-DAC) capable of delivering high output power [30]. The key building blocks of the SCPA are the scalable switched capacitor networks connected to the load via the output matching network (Fig. 3.4), driven by the local oscillator (LO) signal at RF frequency. The PA can be arranged as an array of identical cells. Depending on the digital input code c, the array is dynamically split between n *on* cells, which switch their output stage from 0 to V_{dd} (Fig. 3.6), and $N - n$ off cells which tie their output to ground. Being N the total number of cells in the array, the output voltage at the fundamental frequency of the LO signal is proportional to the number of cells which are in the switching *on* state [30],

$$V_o \propto \frac{n}{N} V_{dd}. \tag{3.11}$$

As a consequence, the power on the load resistance increases with the C-DAC output voltage

$$P_o \propto \frac{V_o^2}{R_l} \propto n^2. \tag{3.12}$$

Since all the cells in the array are equal, when all the cells are turned *on*, the entire array resembles a single unitary cell whose multiplicity is N, as sketched in Fig. 3.5.

The output stage of the equivalent full scale cell connects for half the period the output to GND through the $nMOS$ and for half the period the output to V_{dd} through the $pMOS$. The $pMOS$ devices feature approximately twice the W/L ratio of the $nMOS$ devices in order to achieve the same ON resistance $R_{on\,n,p}$ for both high and low input signals

$$R_{on} = R_{on\,p} = R_{on\,n}. \tag{3.13}$$

During the transition phase, the ON resistance peaks because during that time $MOSFETs$ exit linear operation region. Assuming that the rise and fall time of the input signal is small compared to the input signal period, as in Fig. 3.6, then the impact of the increased output resistance during the transitions is negligible and R_{on} can be approximated as a constant.

The switching output stage is thus modeled as an input voltage commutating at the LO

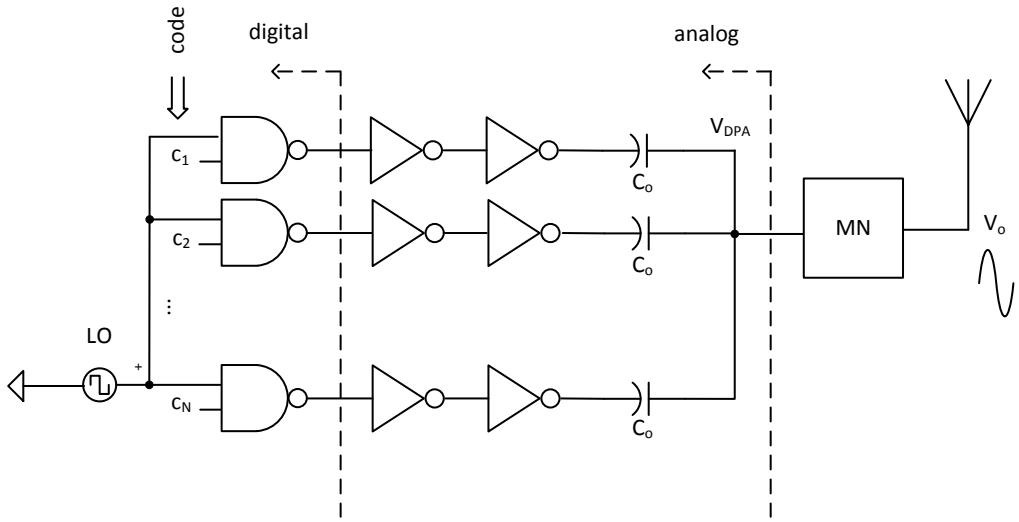


Figure 3.4: SCPA array circuit

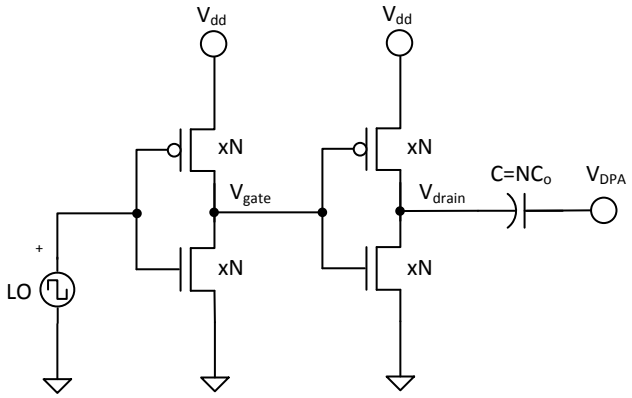


Figure 3.5: SCPA equivalent full scale circuit

frequency driving the capacitance C through a constant resistance R_{on} (see Fig. 3.7).

C_p accounts for all the dynamic losses caused by the capacitive parasitics of the $CMOS$ devices as well as the parasitics of the load capacitance C. $I_{sc\,avg}$ is the average short circuit current during the LO period.

Since the scope of this Part of the Work is to model and evaluate the efficiency of the active part of the SCPA, an ideal lossless matching network is assumed. For the sake of simplicity, the matching network is assumed to be made of a single inductor L, while R_l in Fig. 3.7 is the load due to the antenna. Since the input signal of the linear model is a square wave, the circuit has to be analyzed at all the harmonics. The ideal lossless inductance L

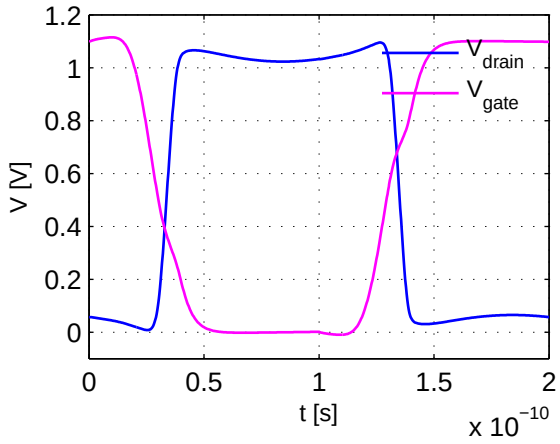


Figure 3.6: Example of output $MOSFETs$ drain voltage at LO operating frequency of $5GHz$. $MOSFETs$ always work in linear region except while switching. Gate voltage in dotted line.

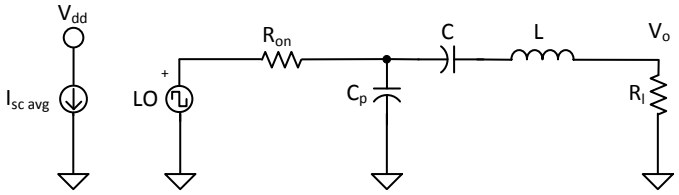


Figure 3.7: Linear model of the SCPA at full scale.

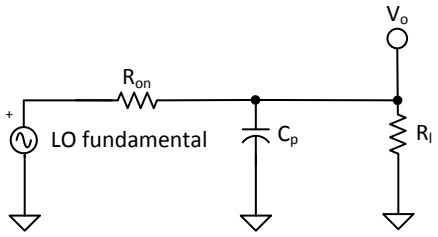
series resonates the SCPA capacitance C at the fundamental frequency of the LO. Therefore, at this frequency the LC can be modeled with a short, as in Fig. 3.8a. The fundamental tone of the input voltage is directly transferred to the load through R_{on}.

On the other hand, the LC series appears as a high impedance at all the other harmonics. As a consequence, only the fundamental flows to the load (Fig. 3.8b) while $I_{sc\,avg}$ and the current through the capacitor C_p make up for the additional losses.

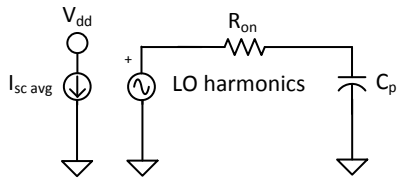
By means of this simplified linear model, the various power contributions can be analyzed. The parasitic capacitor C_p is charged and discharged at the LO frequency. The power loss on C_p can be coarsely estimated as

$$P_{C_P} = fC_pV_{dd}^2 \tag{3.14}$$

while the power loss due to $I_{sc\,avg}$ is



(a)



(b)

Figure 3.8: Single tone equivalent circuit model for the fundamental tone (Fig.3.8a) and the harmonics (Fig.3.8b) of the LO signal

$$P_{I_{sc}} = I_{sc\,avg} V_{dd}. \tag{3.15}$$

Assuming $1/(R_l C_p)$ is much larger than the fundamental frequency, the output power is given by:

$$P_{R_l} = \frac{1}{R_l} \left(\frac{V_f}{\sqrt{2}} \frac{R_l}{R_{on} + R_l} \right)^2 \tag{3.16}$$

where V_f is the fundamental tone of the input square wave swinging from 0 to V_{dd}

$$V_f = \frac{2}{\pi} V_{dd}. \tag{3.17}$$

The output signal current also dissipates power on R_{on}, generating an additional power loss:

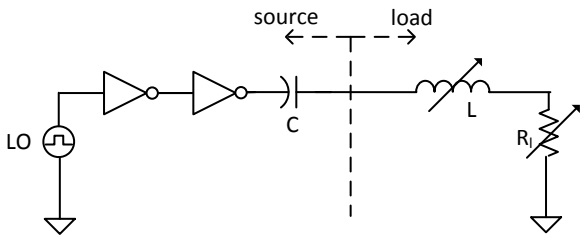


Figure 3.9: Load pull analysis to find the optimal load for a fixed source

$$P_{R_{on}} = \frac{1}{R_{on}} \left(\frac{V_f}{\sqrt{2}} \frac{R_{on}}{R_{on} + R_l} \right)^2 . \tag{3.18}$$

3.2.1.2 Efficiency Analysis

Load-pull analysis is used to find the optimum load impendance to achieve the highest efficiency. During the load-pull analysis L and R_l are swept until the best operating point is found (see Fig. 3.9).

The efficiency is defined as

$$\eta = \frac{P_{R_l}}{P_t} \tag{3.19}$$

where P_t is total power drawn from the supply.

To make the following analysis independent from the absolute value of R_{on} we define

$$\alpha \triangleq \frac{R_l}{R_{on}}. \tag{3.20}$$

Equation (3.19) can be rewritten as:

$$\begin{aligned} \eta &= \frac{P_{R_l}}{P_{switch} + P_{R_l} + P_{R_{on}}} \\ &= \frac{\frac{1}{\alpha R_{on}} \frac{V_f^2}{2} \left(\frac{\alpha}{1+\alpha} \right)^2}{P_{switch} + \frac{1}{R_{on}} \frac{V_f^2}{2} (1+\alpha) \left(\frac{1}{1+\alpha} \right)^2} \end{aligned} \tag{3.21}$$

where

$$P_{switch} \triangleq P_{C_p} + P_{I_{sc}} \tag{3.22}$$

is the total power dissipated by the output stage at open load condition (i.e. $R_l \to \infty$). Defining

$$\beta \triangleq \frac{2R_{on}P_{switch}}{V_f^2} \tag{3.23}$$

(3.21) can be rewritten in a compact fashion as:

$$\eta = \frac{\alpha}{\beta(1+\alpha)^2 + (1+\alpha)} \tag{3.24}$$

where β, according to (3.23), is defined once P_{switch}, R_{on} and V_f are known. P_{switch} is measured as the power taken from the supply for switching the output inverter at open load condition.

It is worth to mention that β is a technology parameter independent from the CMOS inverter size. We show this by rewriting the average short circuit current as

$$I_{sc\,avg} = 2NfT_{sc}\frac{V_{dd}}{R_{sc\,0}}. \tag{3.25}$$

$R_{sc\,0}$ is defined as the average short circuit resistance offered during commutation times by one inverter. Equation (3.25) makes the dependance of I_{sc} from the operation frequency f explicit. For longer switching time T_{sc}, and for an increased frequency of operation f, $I_{sc\,avg}$ increases linearly.

Moreover, the capacitance C_p is proportional to the number of inverters in the output stage

$$C_p = NC_{p\,0} \tag{3.26}$$

where $C_{p\,0}$ is the parasitic capacitance of one output stage and thus

$$P_{switch} = fC_pV_{dd}^2 + V_{dd}\left(Nf2T_{sc}\frac{V_{dd}}{R_{sc\,0}}\right)$$
$$= V_{dd}^2\left(NfC_{p\,o} + Nf2T_{sc}\frac{1}{R_{sc\,0}}\right). \quad (3.27)$$

Using (3.17) and (3.27), (3.23) can be rewritten as follows

$$\beta = \frac{2R_{on\,0}f\left(C_{p\,o} + 2T_{sc}\frac{1}{R_{sc\,0}}\right)}{\left(\frac{2}{\pi}\right)^2}, \quad (3.28)$$

where $R_{on\,0} = NR_{on}$ is the on resistance of one output inverter. Equation (3.28) depends only on technology parameters $R_{on\,0}$, $C_{p\,0}$ and $R_{sc\,0}$, while T_{sc} and the operation frequency f are design parameters. It is worth to note that when the short circuit current can be neglected,

$$\tau_{on} = R_{on\,0}C_{p\,0} \quad (3.29)$$

determines β, and thus maximum efficiency, for a given frequency of operation.

The point of maximum efficiency can be found directly from (3.24) by differentiation:

$$\left.\frac{\delta\eta}{\delta\alpha}\right|_{\alpha_{max}} = 0 \;\Rightarrow\; \alpha_{max} = \sqrt{\frac{\beta+1}{\beta}}. \quad (3.30)$$

Substituting (3.30) in (3.24) and approximating $\beta+1 \approx 1$, the maximum efficiency, η_{max}, can be approximated as:

$$\eta_{max} \cong \frac{1}{1+2\sqrt{\beta}}. \quad (3.31)$$

3.2.1.3 Model Validation

The linear model presented in Sec. 3.2.1.1 is validated against *SpectreRF* simulations of a 28nm CMOS technology. Results refer at nominal corner and temperature $T = 27°$,

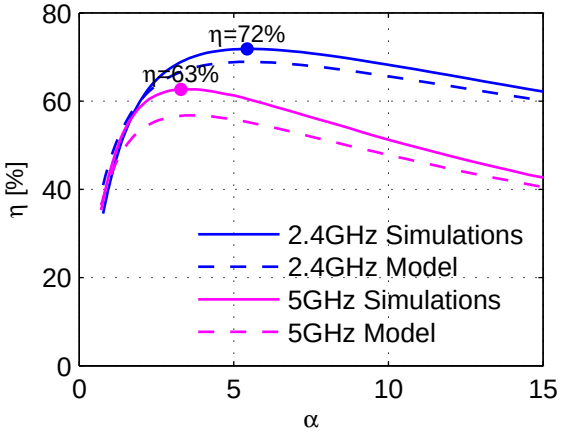


Figure 3.10: Comparison between linear model and *SpectreRF* simulations . Linear model results are plotted with coefficient $\beta = 0.035$ as calculated from $P_{switch} = 67.73mW$, $R_p = R_n = 0.13\Omega$, $f = 2.4GHz$ and $\beta = 0.082$ as calculated from $P_{switch} = 133mW$, $R_p = R_n = 0.155\Omega$, $f = 5GHz$. $V_{dd} = 1.1V$. [1]

$f = 2.4GHz$ and $f = 5GHz$. These are frequencies of interest for many wireless applications, such as WiFi and Bluetooth. The simulated efficiency (solid lines) is compared to the linear model results (dotted lines) in Fig. 3.10, showing good agreement.

Table 3.1 compares α_{max} and η_{max} calculated with (3.30), (3.24) and (3.31) to the results of *SpectreRF* simulations. The linear model, i.e. (3.24) and (3.30), gives a slightly underestimated η_{max} (in this example: 3% less at $2.4GHz$), due to overestimation of P_{C_P} in (3.14). α_{max} is predicted accurately. The approximated model, i.e. (3.31), is also in good agreement with the simulation results.

3.2.1.4 Optimal Design

The presented model can be used for the optmimal sizing of the output stage of the SCPA.

For a given R_l and technology parameters, the value of α_{max} sets the multiplicity N of the output stage of the SCPA. If a higher level of output power is required, both R_l and the multiplicity of the output stage must be scaled by the same factor M (the multiplicity becoming $M \cdot N$), resulting in

$$P_{R_l}* = \frac{1}{\frac{R_l}{M}} \left(\frac{V_f}{\sqrt{2}} \frac{\frac{R_l}{M}}{\frac{R_{on}}{M} + \frac{R_l}{M}} \right)^2 = M P_{R_l} \tag{3.32}$$

Table 3.1: Comparison of Maximum Efficiency in Simplified Model, Linear Model and *SpectreRF* Simulations

(a) α_{max}

Frequency	**Equation (3.31)**	**Equation (3.24)**	**Simulations**
$2.4GHz$	5.43	5.43	5.43
$5GHz$	3.6	3.6	3.6

(b) η_{max}

Frequency	**Equation (3.31)**	**Equation (3.24)**	**Simulations**
$2.4GHz$	73%	69%	72%
$5GHz$	64%	57%	63%

where, in the maximum efficiency conditions, we have

$$P_{R_l} \approx \frac{1}{R_l}\left(\frac{V_f}{\sqrt{2}}\right)^2 \frac{1}{(1+\sqrt{\beta})^2} \approx \frac{1}{R_l}\left(\frac{V_f}{\sqrt{2}}\right)^2 \eta_{max}. \tag{3.33}$$

The scaling of R_l can be achieved by means of an impedance transformation network. Typically, the higher the transformation ratio, the larger the losses introduced by the matching network [21]. This can be a bottleneck on high power circuit implementations with low voltage power supply.

Equation (3.31) points out the important fact that the smaller the β, the higher the efficiency. Combining (3.31) with β as defined in (3.28) it turns out that better efficiency is obtained when the short-circuit current, i.e. (3.25), is small and τ_{on} as in (3.29) is small. As a consequence, scaled technologies featuring lower τ_{on} are expected to yield higher efficiencies. There is not any direct dependance of the intrinsic efficiency on the supply voltage. The SCPA efficiency decreases when increasing the operating frequency due to the direct proportionality between P_{switch} and f as shown in (3.27).

3.2.2 Third-order Matching Networks for Maximum Power and Efficiency

The SCPA is connected to a companion Matching Network (MN) providing both resonance for intrinsic C-DAC capacitance and impedance transformation. The design of the matching network, assumed to be ideal in Sec. 3.2.1, is critical to achieve both required output power and high efficiency on typical 50Ω antenna load.

To enhance output power and linearity, the SCPA is designed with differential outputs, but the antenna is single-ended. Therefore the matching network is as well required to provide differential to single-ended conversion. The building block of choice for the SCPA Matching Network is thus the transformer. No extra capacitance is needed in the MN since the high-quality output capacitance of the SCPA is designed to resonate with the imaginary part of the transformer load, thus minimizing the number of passive components in the network.

The SCPA Matching Network can be implemented off-chip, e.g. [31] and [32] or on the DPA die. The work in [30] shows that a MN for a Wifi application can be built on a single SCPA die operating at the required output power with good efficiency. In this work, the focus is on a systematical analysis of the performance of the integrated MN that allows to select the MN parameters to maximize its efficiency for the desired output power level.

3.2.2.1 Switched-Capacitor Power Amplifier Model

A Switched-Capacitor RF Power Amplifier can be modeled, at full-scale, as a voltage source with low output resistance and a series capacitance as shown in Sec. 3.2.1 [1] and in Fig. 3.11. To obtain the highest efficiency the ratio between load and source resistance has to be large, close to 7 in a CMOS $28nm$ low-power technology [1].

Since the source resistance is very small compared to the load resistance in case of a SCPA designed for high efficiency, the Switched-Capacitor Power Amplifier is modeled by an ideal voltage source V with a series capacitance C, neglecting the source resistance R_s. Furthermore, the source voltage at the first harmonic of a single-ended Class-D circuit is $V_f = \frac{2}{\pi}V_{dd}$. The Root-Mean-Square (RMS) voltage at the first-harmonic of the differentially driven circuit is then $V = \frac{2}{\sqrt{2}}\frac{2}{\pi} \cdot V_{dd} \approx 1V$ at $V_{dd} = 1.1V$.

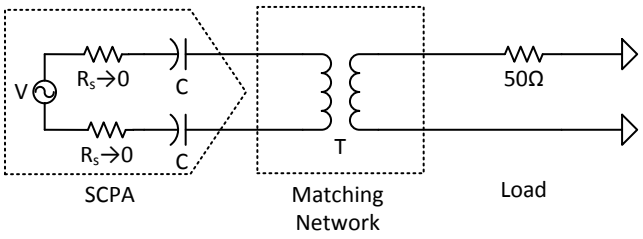


Figure 3.11: Simplified Full-Scale Model of SCPA as shown in Sec. 3.2.1 [1]

Due to the assumption on R_s, all figures of efficiency and power presented here are modeling losses on MN separately from losses in the active part of the circuit, discussed in Sec. 3.2.1 [1].

3.2.2.2 Power and Efficiency Analysis

Figure 3.12 shows a generic circuit transferring power from an ideal voltage source through a transformer to a load R [33]. The magnetic coupling factor between primary and secondary is k, thus $L_1 = (1-k)L_p$, $M = kL_p$ and $L_2 = (1-k)n^2L_p$. L_p is the inductance of the primary winding of a transformer with a $1:n$ turn ratio. Let $R_1 = \dfrac{\omega L_p}{Q_1}$ and $R_2 = \dfrac{\omega n^2 L_p}{Q_2}$ represent the lossess at the primary and secondary side of the transformer, and capacitor C have a high quality factor so that its series resistance can be neglected.

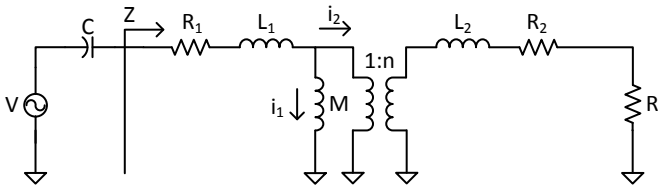


Figure 3.12: Equivalent Single-Ended Circuit of the SCPA. The transformer is modeled by an equivalent T-network

The capacitance C is sized to resonate with the impedance Z (see Fig. 3.12), i.e.,

$$C = \frac{1}{\omega \Im(Z)} \tag{3.34}$$

where

$$\Im(Z) = \omega L_p \left(1 - \frac{k^2}{1+Q^2}\right) \tag{3.35}$$

$$Q = \frac{R_2 + R}{n^2 \cdot \omega L_p} \tag{3.36}$$

Given that P_o is the power on the load resistance R, P_{R1} and P_{R2} the power dissipated on the parasitic resistances R_1 and R_2 respectively, the efficiency is [1]

$$\eta = \frac{P_o}{P_o + P_{R_2} + P_{R_1}} \tag{3.41}$$

$$= \frac{R}{R + R_2 + \dfrac{(R+R_2)^2 + \omega^2(n^2M + L_2)^2}{\omega^2 k^2 L_p^2 n^2} \cdot R_1} \tag{3.42}$$

[1] We have

$$\frac{I_1}{I_2} = \frac{\dfrac{R_2 + R + j\omega L_2}{n^2}}{j\omega M} \tag{3.37}$$

and thus,

$$\eta = \frac{P_o}{P_o + P_{R_2} + P_{R_1}} \tag{3.38}$$

$$= \frac{|I_2|^2 \cdot \dfrac{R}{n^2}}{|I_2|^2 \cdot \dfrac{R+R_2}{n^2} + |I_1 + I_2|^2 \cdot R_1} \tag{3.39}$$

$$= \frac{\dfrac{R}{n^2}}{\dfrac{R+R_2}{n^2} + \left|\dfrac{R + R_2 + j\omega L_2 + j\omega M n^2}{j\omega M n^2}\right|^2 \cdot R_1} \tag{3.40}$$

The output power results

$$P_o = \frac{\eta^2 n^2 V^2}{R} \frac{\left(R + \frac{n^2 \omega L_p}{Q_2}\right)^2 + \omega^2 (n^2 M + L_2)^2}{\omega^2 k^2 L_p^2 n^4} \tag{3.43}$$

(3.42) shows that efficiency is maximized by choosing L_p as:

$$L_{p\,opt} = \frac{R}{\omega \cdot n^2 \sqrt{k^2 \frac{Q_1}{Q_2} + \frac{1}{Q_2^2} + 1}} \tag{3.44}$$

Replacing (3.44) in (3.42) gives maximum achievable efficiency,

$$max(\eta) = \frac{1}{1 + 2\beta + 2\sqrt{\beta\,(1 + \alpha + \beta)}} \tag{3.45}$$

with

$$\alpha = \frac{1}{k^2} \frac{Q_2}{Q_1} \tag{3.46}$$

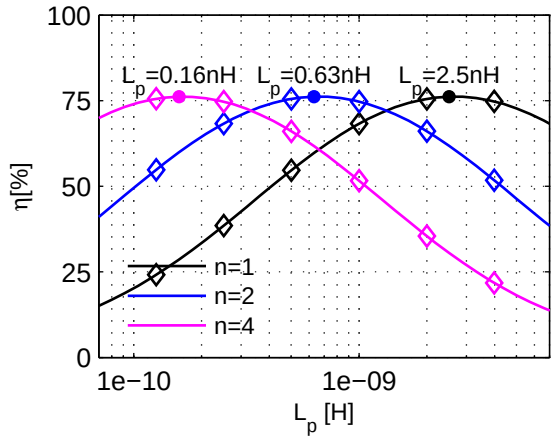
$$\beta = \frac{1}{k^2 Q_1 Q_2} \tag{3.47}$$

Equations (3.42) and (3.43) are plotted as a function of L_p in Figs. 3.13 (a) and (b) (symbols), assuming a typical RF metal stack. The model is validated versus circuit simulations in Figs. 3.13 (a) and (b) (lines). Since no approximation has been used in the calculations, the model perfectly matches the simulations.

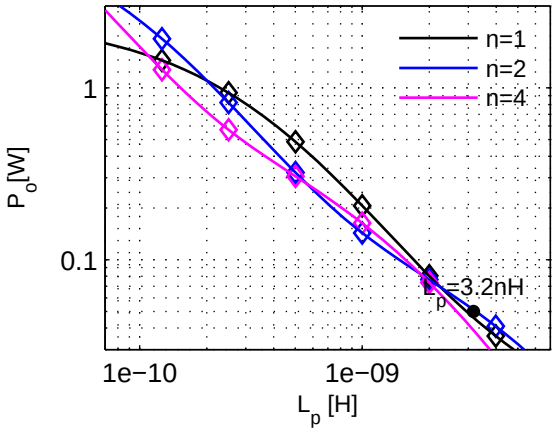
3.2.2.3 Design Example

The third-order MN is designed to maximize the efficiency i.e., minimize the IL, and meet the power specification. The Class-2 Bluetooth application for which the MN has been designed in this Example has a target RMS output power level of $16dBm$ at $2.4GHz$, similar to [34].

Power and efficiency as a function of L_p, turn ratio n and technological parameters Q_1, Q_2 and k have been calculated in Section 3.2.2.2.Under the hypothesis of high Q_1, Q_2 and



(a) Efficiency



(b) Power

Figure 3.13: Model plots for typical RF stack quality and coupling factor at $2.4GHz$ of $Q_1 = Q_2 = 15$ and $k = 0.75$ respectively. For the sake of power calculations $V = 1Vrms$ has been considered. Due to layout considerations, a primary to secondary turn ratio of $n = 4$ might be hard to obtain with such quality and coupling factors. Equation (solid lines) and measurements (diamond points) coincide

k, (3.43) simplifies to

$$P_o \approx \frac{\eta^2 n^2 V^2}{k^2 R} \left(Q^2 + 1\right) \tag{3.48}$$

where Q is given by (3.36). Through (3.48) and Fig. 3.13 (b) we observe that output power P_o increases for smaller L_p. The efficiency peaks to (3.45) for L_p given by (3.44). Figure

3.14 shows η as as a function of P_o.

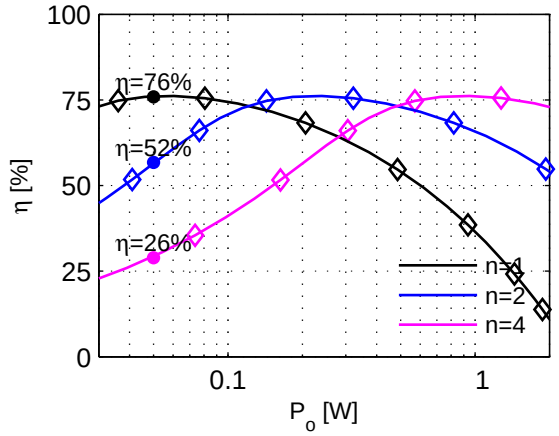


Figure 3.14: Design Choices with $Q_1 = Q_2 = 15$ and $k = 0.75$ annotated for specification power $P_o = 0.05W$

The dotted line in Fig. 3.14 shows the power specification of our design i.e., with some margin, $P_o = 0.05W$. All the intersections of $P_o = 0.05W$ with η curves are possible design solutions meeting the specification. The optimal solution with maximum efficiency is found at the intersection of $P_o = 0.05W$ with $n = 1$, predicting an efficiency of $\eta = 76\%$. After choosing $n = 1$, desired L_p is found by intersecting the dotted line representing $P_o = 0.05W$ with the curve for $n = 1$ in Fig. 3.13 (b) to be close to $3nH$.

In an area of $300x300\mu m^2$, an octagonal shape has been chosen for the transformer due to its better performance compared to the square shape [35]. An initial guess of $n_p = 3$ interleaved turns has been used to implement the primary and secondary side. In fact [35],

$$L \approx \frac{\mu_o n_p^2 d_{avg} c_1}{2} \left[ln\left(\frac{c_2}{\rho}\right) + c_3\rho + c_4\rho \right] \approx 2.8nH \tag{3.49}$$

with $c_1 = 1.07$, $c_2 = 2.29$, $c_3 = 0$ and $c_4 = 0.19$ for the octagonal shape, with fill factor in the layout $\rho = 50\%$. The fabricated transformer is shown in Fig. 3.15 and in Table 3.2, Structure I.

Equation (3.34) yields that a single-ended series capacitance of $2.3pF$, or equivalently, two capacitances of $4.6pF$ in differential operation are needed to resonate the MN.

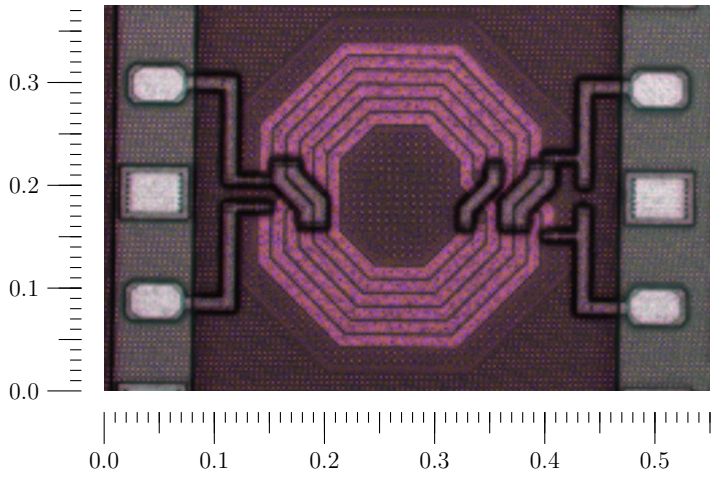


Figure 3.15: Die photo of the fabricated $16.7dBm$ transformer (Structure I in Table 3.2) with millimeter ruler. Primary is at the left side and secondary at the right side

It is worth noting that, both in Fig. 3.13 (b) and in Fig. 3.14, a limit in the maximum power available for a given turn ratio exists. Replacing (3.42) in (3.43), we analytically calculate this limit

$$\lim_{\omega L \to 0} P_o = \frac{k^2 Q_1^2 V^2 n^2}{R} \tag{3.50}$$

e.g., in agreement with the simulations, (3.50) yields $P_o \to 2.53W$ for $n = 1$ in the given technology. Since $\eta \to 0$ while approaching the limit, this analytical maximum power level cannot anyhow be achieved in practical implementations.

The model can also be used to predict and compare the performance of third-order SCPA Matching Networks in different technologies. In particular, Fig. 3.16 shows that the maximum efficiency achievable by these MN is an increasing function of Q_1, Q_2 and k. In fact, an approximation of (3.45) when $Q_1 \sim Q_2$ and k are high is,

$$max(\eta) \approx \frac{1}{1 + 2\sqrt{2\beta}} \tag{3.51}$$

where β has been defined in (3.47), highlighting the fact that maximum achievable efficiency is an increasing function of coupling k and quality factor Q_1 and Q_2 of inductors used in the matching network.

All the results presented so far are valid only for third-order matching networks. A third-

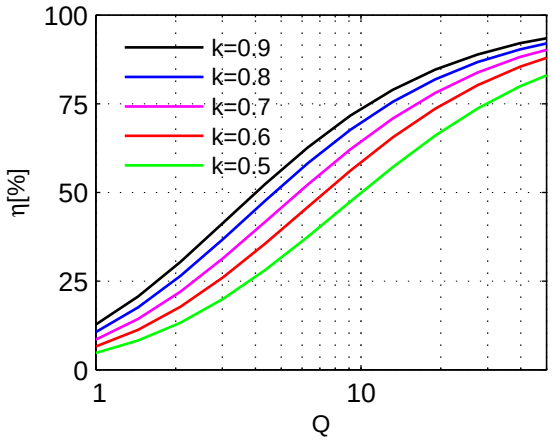


Figure 3.16: Maximum efficiency of third-order matching networks as a function of technological parameters $Q_1 = Q_2$ and k

order Matching-Network is the MN implying the minimum number of reactive components in a SCPA with transformers, thus it is a good starting point for the design of the SCPA MN. Higher order MN can also be used, and e.g. loosely coupled transformers can still give high efficiency [36] in higher order MN.

3.2.2.4 Validation

The designed transformer has been fabricated in a $28nm$ CMOS RF Metal Stack as shown in Fig. 3.15 and measured with a Keysight (Agilent) N5257A Vector Network Analyzer. We used a Cascade E300 Probe Station with Cascade Infinity GSGSG Probes. The measured S-Parameters have been imported in Advanced Design System (Agilent) and used to describe the transformer of circuit of Fig. 3.11. The results are shown in Table 3.2 under Structure I and in Fig. 3.17, where $IL = 10\log_{10}(\frac{1}{\eta})$. The network is achieving $IL = 1.1dB$, i.e. 77% efficiency, at $2.4GHz$ and $48mW$ on 50Ω termination, when fed by a $1Vrms$ differential voltage source with two $4.6pF$ high-quality series resonating capacitances.

The target Bluetooth application, taken as a reference for this Example, is narrowband, thus bandwidth of the matching network is not the focus of this work, but it is interesting to note that the designed matching network is achieving a large $3dB$ bandwidth as well. The $3dB$ bandwidth of the $16.7dBm$ fabricated Matching Network of Fig. 3.17 is $1.5GHz$. The wide value of the bandwidth can be explained by the small Q employed in the impedance

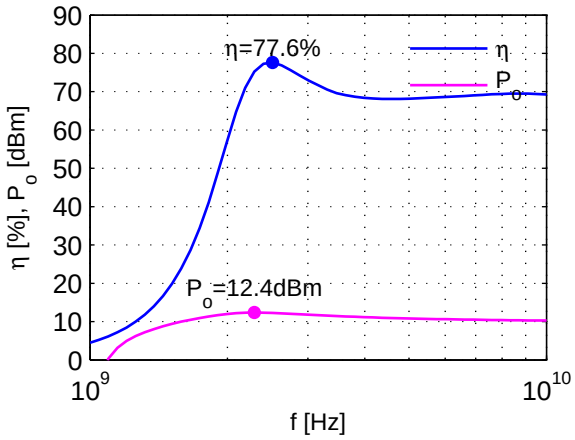


Figure 3.17: Measured Output Power and IL of Structure I

transformation, were transformation Q is defined in (3.36).

Additional Test Structures (Structures II-V in Table 3.2) have been fabricated on the same chip with different winding arrangements, confirming the accuracy of the model. The measured L, Q and k parameters have been substituted in (3.42) and (3.43) to verify that the model predicts correctly power and efficiency. Table 3.2 shows good agreement between modeled and measured P_o and η.

Test Structure II provides $22.3dBm$ output power at $2.4GHz$, i.e. $5.6dB$ more than I. Unfortunately, due to the reduced quality factor on primary side of the structure, lower efficiency of 65% is achieved. A reduced quality factor, due to technology and geometry constraints, measured in the $0.9GHz$ structures again decreases the efficiency achievable with Test Structures III IV and V, as correctly predicted by the model.

It is important to note that the proposed model is accurate when the distance between Self-Resonance-Frequency (SRF) and operating frequency is large enough. When the transformer is operated close to its SRF, the effect of the parasitic capacitances dominates the transformer operation and the model of Fig. 3.12 needs to be adapted consequently.

Table 3.2: Measured Test Structures at frequency f. P_{model} and η_{model} are estimated by (3.42) and (3.43) with $V = 1Vrms$ [2]

STR	**I**	**II**	III	IV	V
$\boldsymbol{L_p}$	**2.5nH**	**0.56nH**	3.4nH	5.6nH	8.6nH
$\boldsymbol{L_s}$	**2.3nH**	**2.66nH**	3.7nH	5.5nH	8.1nH
$\boldsymbol{k}$	**0.85**	**0.79**	0.92	0.93	0.91
$\boldsymbol{Q_p}$	**13.6**	**6.6**	6.7	7.4	8.6
$\boldsymbol{Q_s}$	**14.4**	**19.7**	2.2	2.76	8.6
$\boldsymbol{SRF}$	**9GHz**	**10.6GHz**	3.3GHz	2.75GHz	3.9GHz
$\boldsymbol{P_o}$	**47mW**	**170mW**	70mW	40mW	27mW
$\boldsymbol{P_{o\ model}}$	**49mW**	**173mW**	70mW	40mW	28mW
$\boldsymbol{\eta}$	**77%**	**65%**	55%	60%	70%
$\boldsymbol{\eta_{model}}$	**79%**	**64%**	53%	59%	72%
$\boldsymbol{C}$	**2.3pF**	**1.6pF**	10pF	7pF	5.5pF
$\boldsymbol{f}$	**2.4GHz**	**2.4GHz**	0.9GHz	0.9GHz	0.9GHz

3.2.3 Power-Combiners for Highly-Mismatched Transformation Ratios

Power transferred to load by a differential switched-capacitor PA is directly proportional to its output stage supply voltage V_{dd} and inversely proportional to the effective resistance R_{eff} seen at its output stage, namely, as presented in Sec. 3.2.1 [1]

$$P_o = \left(\frac{2 \cdot 2V_{dd}}{\pi\sqrt{2}}\right)^2 \left(\frac{R_{eff}}{R_{switch} + R_{eff}}\right)^2 \frac{1}{R_{eff}} \tag{3.52}$$

A low-supply voltage SCPA with V_{dd} limited to, for example, core-voltage of a CMOS $28nm$ which is $1.1V$, has a low voltage level compared to typical supply levels of PAs published in literature [37]. With a differential $1.1V$ supply SCPA design, neglecting the losses of the switches modeled by R_{switch}, in fact, specifically

$$R_{eff} \approx \frac{1V_{rms}^2}{P_o} \tag{3.53}$$

therefore, to design a Low-Voltage SCPA for Wireless Applications, with output power as high as 1 Watt, a 1Ω SCPA load resistance is required. Typical system load is, however, an RF antenna, which exhibits a single-ended load of 50Ω. For this application $R_{antenna}$ has therefore to undergo a huge $50:1\Omega$, differential to single-ended, transformation down to $R_{eff} = 1\Omega$.

Such a transformation is however hard to obtain in practice with integrated inductors. To get such a transformation targeting a low-voltage SCPA working at i.e. $2.4GHz$ with reasonable efficiency using a single monolithic transformers, in a typical $28nm$ metal stack, one needs a transformer with a primary inductor of $L = 175pH$, and $1:4$ turn ratio between primary and secondary [2] with quality factors exceeding i.e. $Q \geq 10$ both for primary and secondary inductance of the transformer.

Few reports are available in literature of monolithic transformers obtaining such characteristics, and those who reported them, usually measure a reduced quality factor when providing such a impedance transformation ratio [38]. Multistage approach, where the impedance level is transformed with a subsequent set of transformations using lumped element, has low efficiency when high transformation ratios are required [33]. This again decreases total available output power due to losses in the transformation itself.

3.2.3.1 Series Power Combiner Circuit

A reduced area footprint, which is important when targeting a monolithic transformer implementation in a CMOS Technology, pushes for the use of a Power-Combiners employing lumped-elements only. Transformers are used to perform a differential to single-ended conversion. Furthermore, Switched-Capacitor sources act as a voltage sources, rather than as a current sources, therefore their outputs are combined in series, so that the total output voltage is enhanced. A series power combiner using a series combination of transformers, with a one transformer for each differential SCPA, limiting the number of passive components required, is therefore chosen.

The SCPAs have been modeled as in Sec. 3.2.1 [1], so that the overall circuit is that of

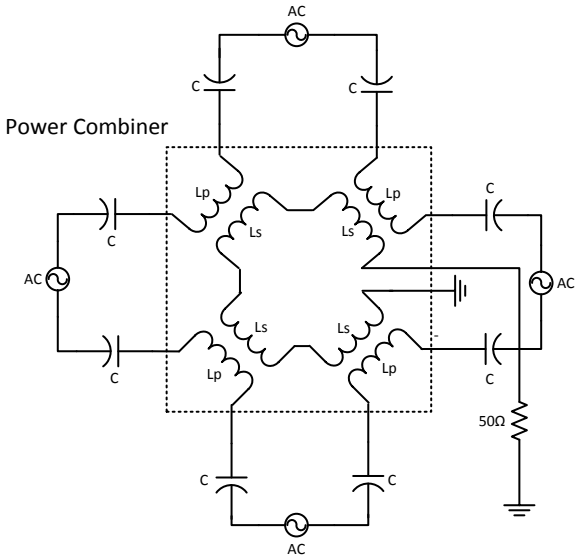


Figure 3.18: Series Power Combiner Circuit

Fig. 3.18. Out of the circuit of Fig. 3.18 we calculate the power transferred to the load, which is

$$P = \frac{\left(\dfrac{R/(Nn^2)}{R/(Nn^2) + (\dfrac{2}{sC} + sL_s)\dfrac{sL}{sL + \dfrac{2}{sC} + sL_s}} \dfrac{sL}{sL + \dfrac{2}{sC} + sL_s} Nn(V_a - V_b) \right)^2}{R} \tag{3.54}$$

where n is the ratio between primary and secondary number of inductances, N is the number of combined circuits, $V_a - V_b$ the equivalent AC voltage source at the fundamental tone of one SCPA, C the output capacitance of the SCPA, L the mutual inductance, and R the load Z, here supposed to be resistive [2].

[2]Alternatively, Eq. 3.54 can be written as

Since in this simplified model primaries and secondaries meshes are all isolated one-another, except for directly-coupled spires, then, for the sake of calculating mesh voltages and currents at the secondary, absolute potential of the primary meshes can be neglected.

Then, looking from the secondary mesh, a Thevenin equivalent of one SCPA circuit and one transformer is calculated. One transformer and its coupled SCPA circuit are therefore modeled by an equivalent impedance Z_{th} and an equivalent voltage Z_{th}. The equivalent circuits are reported to the secondary mesh, resulting in the circuit of Fig. 3.19a. The circuit of Fig. 3.19a is further simplified to the circuit of Fig. 3.19b by observing that both circuits transfer the same power P_o to their load impedance.

3.2.3.2 Design Example

On the basis of the equivalent circuit of Fig. 3.19b, the series Power Combiner is modeled as a block which operates a $1 : N$ down-conversion of the load impedance, and which increases

---

$$P = \frac{\left(\frac{R/(Nn^2)s^2LC}{s^3LL_sC + R/(Nn^2)s^2(L+L_s)C + 2sL + 2R/(Nn^2)} Nn(V_a - V_b) \right)^2}{R} \tag{3.55}$$

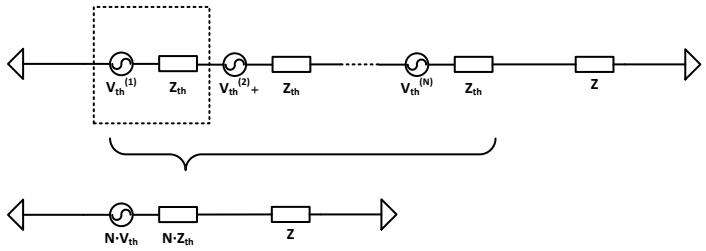
Eq. 3.55, in case $k \to 1$ and therefore $L_s \to 0$, simplifies to the transfer function of a second-order high-pass filter, i.e.

$$P_{k\to 1} = \frac{\left(\frac{s^2LC}{s^2LC + \frac{sL}{R/(Nn^2)} + 1} Nn(V_a - V_b) \right)^2}{R} \tag{3.56}$$

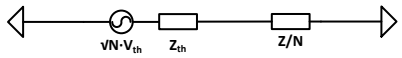
Eq. 3.56, at resonance frequency $\omega = \sqrt{1/LC}$, yields an output power

$$P = \frac{\left(\frac{1}{\frac{\omega L}{R/(Nn^2)}} Nn(V_a - V_b) \right)^2}{R} \tag{3.57}$$

analogously to the approximated result obtained by calculating the limit $k \to 1$ in Eq. 3.61.



(a) Equivalent



(b) Power Equivalent

Figure 3.19: Equivalent Circuit Transformation.

the effective source voltage by a $\sqrt{N}$ factor. Eq. 3.52 is therefore updated to

$$P_o = \left(\frac{2 \cdot 2\sqrt{N}V_{dd}}{\pi\sqrt{2}}\right)^2 \left(\frac{R_{eff}}{R_{switch} + R_{eff}}\right)^2 \frac{1}{\frac{R_{eff}}{N}} \tag{3.58}$$

and Equation 3.53 becomes,

$$R_{eff} \approx \frac{N \cdot 1V_{rms}^2}{P_o} \tag{3.59}$$

Increasing the Number of Combined Circuits (N) both decreases the effective load resistance and increases the required source impedance at the same time, resulting in a required transformation ratio diminished by a factor N^2. Figure 3.20 shows the effective impedance levels of the circuit as a function of N. For example, the $1:50$ transformation, when employing the combination of four SCPA circuits through a four-way Power Combiner, results in a required $4:12.5$, i.e. $1:3.125$ impedance transformation ratio. This impedance transformation ratio is easily achieved with standard $CMOS\ RF$ metal stack and common transformer design.

To finalize a practical implementation, we make use of the previously published model

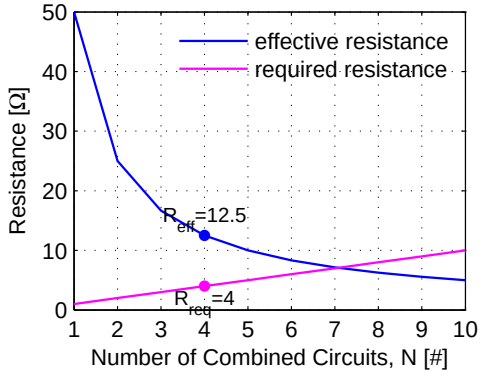


Figure 3.20: Impedance Levels as a function of Number of Combined Circuits (N) for a 1-W 1.1V SCPA

of the SCPA [1] and its matching network [2], adapting the impedance levels according to the Power Combiner transformations of Fig. 3.20, obtaining the circuit of Fig. 3.21 with the T-model of a transformer. In this equivalent circuit, source voltage is increased by a factor $\sqrt{N}$, and load impedance is down-scaled by a factor N. One transformer corresponds to each one of the N transformers of which the power combiner is built. We design an optimal transformation recalling previously published equations in [33] and in Sec. 3.2.2 [2], i.e., optimal transformer size is:

$$\omega L_p \approx \frac{R}{N \cdot n^2 \sqrt{1+k^2}} \tag{3.60}$$

after impedance of the load R is adapted down to effective R/N size. Transformed impedance of the circuit is, overall, roughly

$$\begin{aligned} R_{eff} &= \frac{k^2 R}{N \cdot n^2 (Q^2+1)} \\ Q &= \frac{R}{N n^2 \omega L_p} \end{aligned} \tag{3.61}$$

By sizing the transformer around its optimal size, with a coupling factor of around 0.75, and a transformation Q which at optimal transformer size is about 1, we roughly get a $1:4$ transformation. Therefore, to meet an example target $1W$ output power, a four way power combiner with $1:1$ transformers with an inductance of, according to Eq. 3.60, $L_p = 660pH$ is used. A single-ended capacitance of $6.6pF$ is required to resonate each of the designed

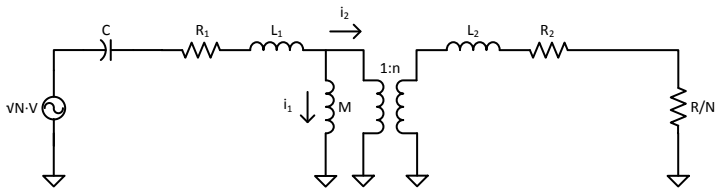


Figure 3.21: Overall Circuit

transformers, thus a total capacitance of $4 \cdot 6.6pF$ is required in the circuit. It is important to notice, that the capacitance required to resonate the design of such a circuit with this power level, is not higher than the capacitance predicted in Section 3.2.3 for a single-transformer design approach.

Finally, we increase the output power and compensate the losses in the Power Combiner, by targeting a lower L_p of $\approx 400pH$. An example design of a Power Combiner is shown in Fig. 3.23. Thanks to the thick metallizations available in the $28nm$ RF metal stack we designed the combiner for, the required transformer characteristics are met with a straightforward stacked design. Primary tracks are drawn in top-most Alu layer, and secondary tracks in a lower Copper layer. For each transformer, with a ray of $100\mu m$ and fill-factor $\rho = 10\%$, an inductance of [21]

$$L = \frac{\mu_o n^2 d_{avg} c_1}{2} = \left[ln\left(\frac{c_2}{\rho}\right) + c_3\rho + c_4\rho^2 \right] = 384pH \tag{3.62}$$

with $c_1 = 1.00$, $c_2 = 2.46$, $c_3 = 0.00$ and $c_4 = 0.20$ is found. The four transformers have then been connected together in a star-shaped configuration resembling the circuit of Fig. 3.18.

The overall transformation is then examined on the Smith Chart, as shown in Fig. 3.22. Moving from the load to the generator: first, the four-way Power-Combiner scales the load impedance down to 12.5Ω. Second, a parallel inductance, with optimal inductance size, moves the load on a constant-parallel admittance circle to $0.08 + j0.12$ position. Third, a series capacitance neutralizes the imaginary part of the transformed impedance, down to 0.08 real only. Finally, the target impedance level is larger than that required in a non-

combined circuit, because, due to effective source voltage boost operated by the four-way Power-Combiner, 4Ω effective resistance is enough to yield desired output power.

3.2.3.3 Validation

One transformer has been designed with the aid of $VeloceRF$ tool [39]. $VeloceRF$ tool, provided with transformer geometric dimensions and characteristics, can automatically design such a transformer. Subsequently, the designed transformer has been flattened and placed four times to make the shape of the Power-Combiner shown in Fig. 3.23. $VeloceRaptor$ has finally been run on the complete Power Combiner layout for characterizing the Power-Combiner. Simulator accuracy has been proven to be quite good on previously taped-out test-structures as shown in Sec. 3.2.2 [2].

Interaction between non-overlapped coils is limited, and we neglect coupling between coils as shown in the model of Fig. 3.18, characterizing each of the transformers individually. Namely, more than $20dB$ of isolation between non-directly coupled coils for the frequencies of interest is measured, as shown in Fig. 3.25a. Each transformer has a primary inductance of $360pH$ and a secondary inductance of $320pH$ at $2.4GHz$ frequency. At this frequency the simulated quality factor of the coils is around 10, and simulated coupling factor between primary and secondary is $k = 0.6$. The full EM characterization of the structure against the model of Fig. 4.3 is shown in Fig. 3.25a, 3.24a, 3.25b and 3.24b.

Overall circuit performances, where the power combiner is inserted in the circuit shown in Fig. 3.18, are presented in Fig. 3.26. The series differential resonating capacitance value C is $2 \cdot 24pF$, which is equivalent to a $12pF$ single-ended resonating capacitance. A maximum output power of $31.2dBm$ is simulated and the maximum circuit efficiency of the combiner is simulated to be 66.2%.

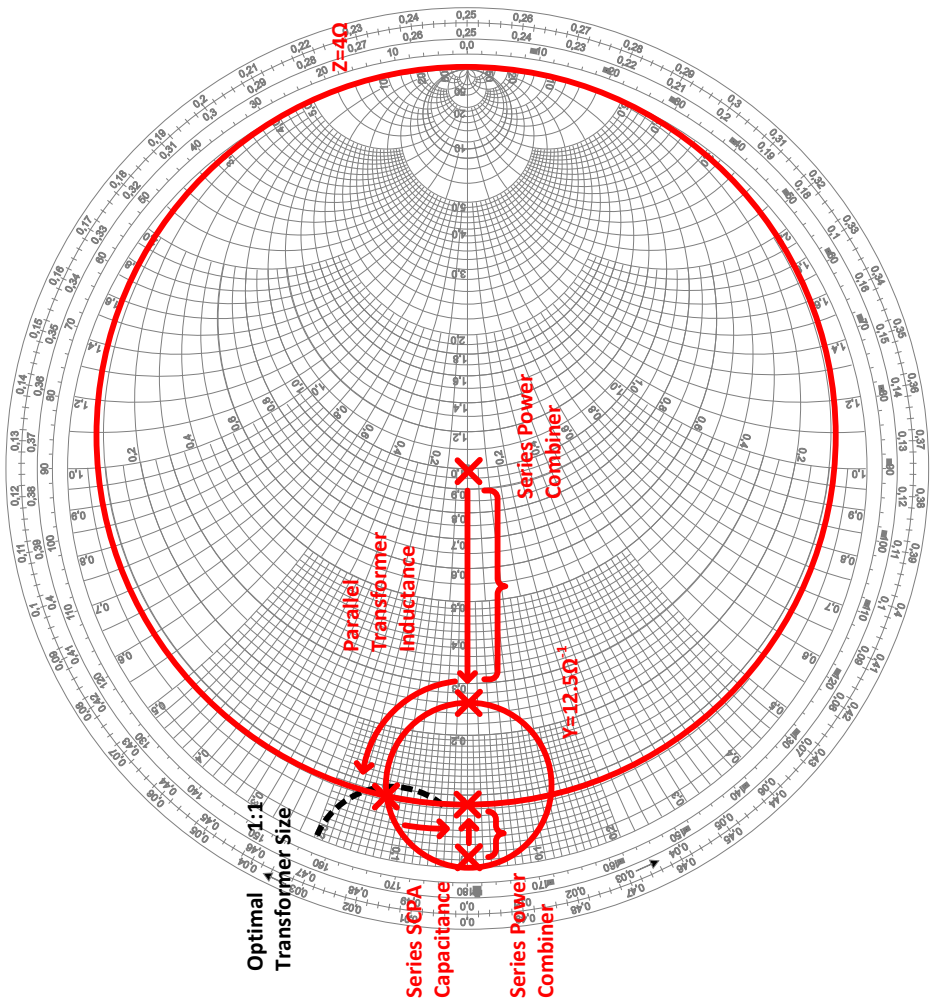


Figure 3.22: Overall Impedance Transformation on the Smith Chart

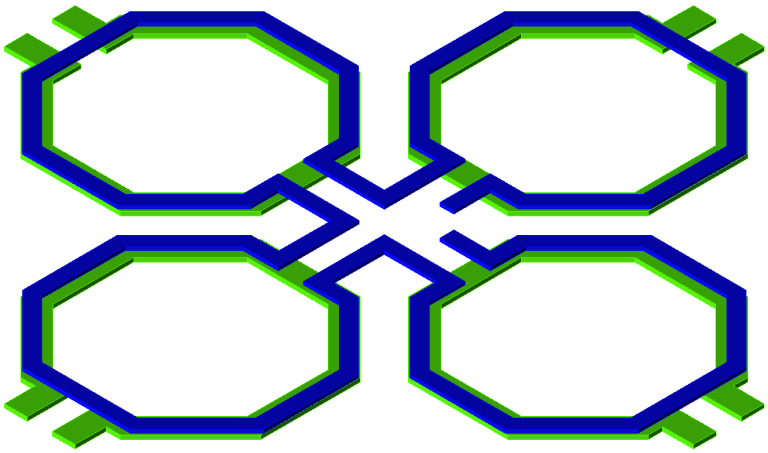
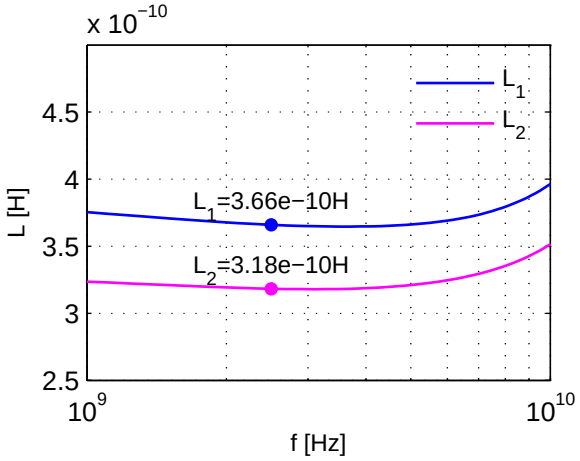
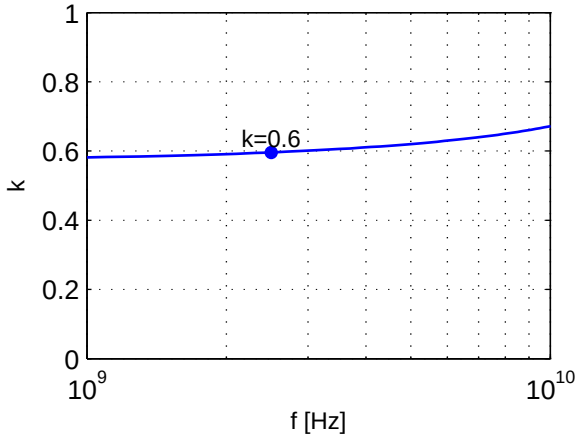


Figure 3.23: Designed $1:50\Omega$ Power Combiner. Size of one transformer is $200\mu m \cdot 200\mu m$, whole structure is $450\mu m \cdot 450\mu m$ wide, and total area footprint is $0.2mm^2$.

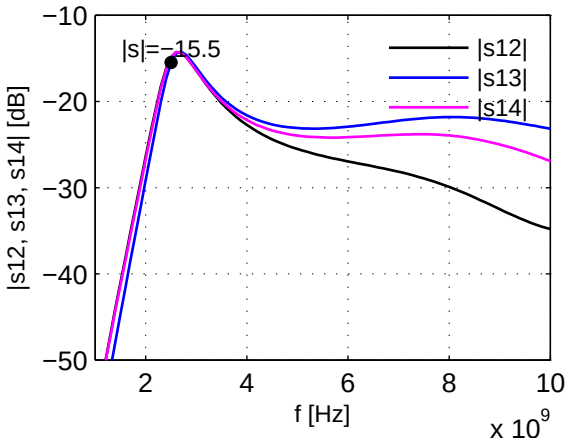


(a) Simulated Primary and Secondary Inductance of one Transformer

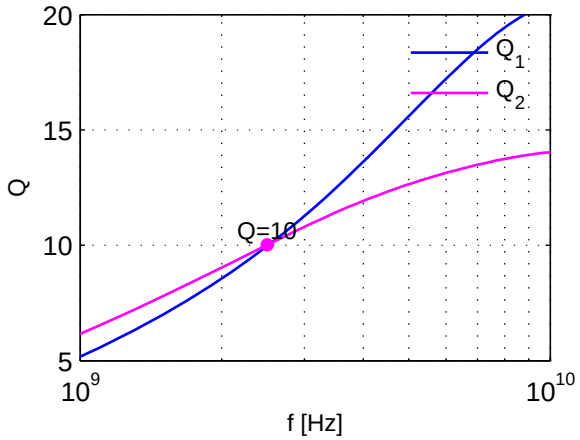


(b) Simulated Coupling Factor between Primary and Secondary of one Transformer

Figure 3.24: Inductances and coupling factors



(a) Isolation between Transformers



(b) Simulated Quality Factors of Primary and Secondary Coils of one Transformer

Figure 3.25: Evaluation of the Parasitics of the Combiner

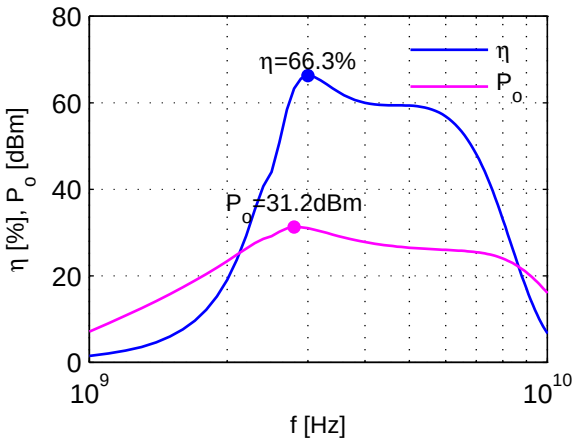


Figure 3.26: Simulated Output Power and Efficiency of the Resonated Power Combiner Circuit

Chapter 4

Results

In this Part of the Work, the results of the Design which has been implemented in a $28nm$ CMOS Technology are shown, including simulations of System performance, photographs of the die and of the package, and a description of the Variants which have been implemented. Both Variant (a), comprising a Power-Combiner In-Package, and Variant (b), comprising a Power-Combiner In-Die, are described in detail. Next, before providing a complete characterization of the performance of the system, the enhancements to the System efficiency achieved operating the implemented Programmable Pre-Scaler are presented. Finally, achieved results are compared with the state-of-the-art publications in terms of Key-Performance Indicators.

4.1 Samples Description

Leveraging design techniques presented in Sec. 3, a Transmitter fulfilling the requirements described in Sec. 2 is implemented. The implemented Transmitter Architecture comprises four Switched-Capacitor Power Amplifiers (SCPAs), each operated at core $1.1V$ Supply Voltage. A four-way Power Combiner sums the Power of the four SCPAs to a single-ended 50Ω Antenna Load. A Clock Tree distributes a $4.8GHz$ Reference Clock Source synchronously to the SCPAs, where, locally, In-Phase and Quadrature-Phase Clocks are generated.

4.1.1 Block Diagram of the Transmitter

A block diagram of the implemented Transmitter is provided in Fig. 4.1. The floor plan of the Transmitter is arranged so that the Synthesized Digital Signal is received at the bottom and the output connection is located at the top of the Transmitter. The implemented system comprises,

- A set of four Differential Switched-Capacitor PAs capable of In-Phase/Quadrature-Phase operation. The exact number of SCPA elements is chosen according to the Impedance Transformation described in Sec. 3.2.3, so that the number of combined element optimizes Power Combiner efficiency, reducing System Power Consumption for the $29dBm$ required output power level

- A Programmable Pre-Scaler. Instead of hard wiring the Synthesized Digital Signal to the SCPAs, four Programmable Pre-Scaler interface between the Synthesized Digital Signal and the Digital Interface of each SCPA. Each Programmable Pre-Scaler has independent programming registers, allowing an asymmetric distribution of the Synthesized Digital Signal amongst the SCPAs, or identical distribution for symmetric System operation, depending on selected operation. As explained in Sec. 4.2.1, a higher efficiency is achieved when the System is operated asymmetrically

- A Clock Tree distributing a $4.8GHz$ Reference Clock Source symmetrically to each SCPA. The In-Phase and Quadrature-Phase clock edges are generated locally within each SCPA. The Reference Clock, operated at $4.8GHz$, contains in fact both In-Phase edges and Quadrature-Phase edges of a $2.4GHz$ clock. Thanks to the symmetry of the Clock Tree, it is guaranteed that each SCPA operates on identical Reference Clocks. This property is, in fact, leveraged in Sec. 2.4.3.

4.1.2 In-Die (a) and In-Package (b) Power Combiner

As described in Sec. 3.2.1, 3.2.2 and 3.2.3, the optimal Design of the Switched-Capacitor PA (SCPA) Circuit is achieved after optimizing both the Design of the CMOS Devices and as well the Design of the Passive Structures comprising the Circuit. Whilst SCPA CMOS Devices

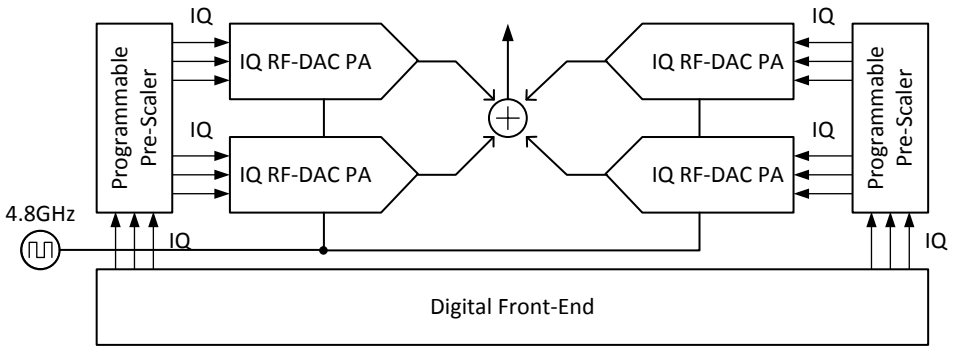


Figure 4.1: System

are optimized by correctly sizing the output stage of the Power Amplifier, designing efficient Passive Structures requires the selection of optimal component parameters, as shown in 3.2.3, and as well a careful Layout of the Electro-Magnetic Structures. Passive Structures such as Power Combiners, in fact, don't come in pre-built templates adjustable through EDA Tools such as MOSFETs and capacitors do, therefore it is a task of the designer that of optimizing and arranging the preferred shape and layer combinations which attains required components parameters.

Furthermore, due to the high number of ports and connections, the Power Combiner is an area-intensive structure. A lot of efforts have thus been spent in the direction of minimizing the area of the layout of the Power Combiner, while achieving high quality-factors in the inductors, as per Sec. 3.2.3. A hand-crafted layout based on coupled transmission-lines was built, where patches of metals have been attached in parallel together, and interleaved with the coupled secondary at the layer above, as shown in Fig. 4.2. Having many patches in parallel, allows to place larger metallization widths comparing to the width allowed for a single patch of metal by the physical design rules of the Technology. Furthermore, interleaving primary and secondary patches, enhances the coupling-factor without increasing the capacity between primary and secondary coils C_{ps} which would de-tune the transformation.

A complete characterization of the in-die Power Combiner against the model of Fig. 4.3 is shown in Fig. 4.4 and in 4.5. Beside attaining the required inductivity, a good quality factor exceeding 10 for both primary and secondary at $2.4GHz$ is achieved at a high coupling factor

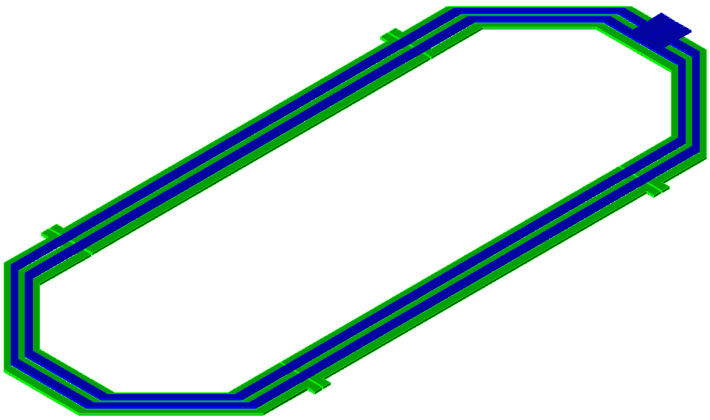


Figure 4.2: Three-Dimensional View of the Combiner-in-die

of almost 0.9. The parasitic capacitances are negligible, with the exception of C_{ps} which is valued $1.2pF$. Due to the asymmetrical shape of the combiner amongst the primary ports, such as between the inductance L_{1a} formed between port 1 and 2 of the Power Combiner and the inductance L_{1b} formed between port 3 and 4 of the Power Combiner of Fig. 4.3, it is important to evaluate the symmetry of the combiner. As shown in Fig. 4.10b a good symmetry is achieved. L_{1a} physically characterizes the inductance built by the straight transmission-line of the layout of the Power Combiner of Fig. 4.2, whilst L_{1b} characterizes the inductance build by bent transmission-line of the Power Combiner of Fig. 4.2.

To reduce the total area usage of the Power Combiner, novel implementations of the Power Combiner have then been evaluated. In particular, it is identified that a significant part of the area of the Power Combiner is empty, and could be potentially filled by CMOS devices, such as i.e. devices comprising the SCPA output stage, or synthesized digital Circuits, and other circuits. One way of reducing the area usage is therefore potentially that of designing an RF-DAC Circuit which fits within the Power Combiner, thus filling the void area within the Power Combiner with the SCPAs Circuits themselves. However, since the upper metal layer is blocked by the Power Combiner, all-around the set of SCPAs, no low-ohmic interconnection layers would be available for routing the supply, which, cannot be routed in thin lower metallizations.

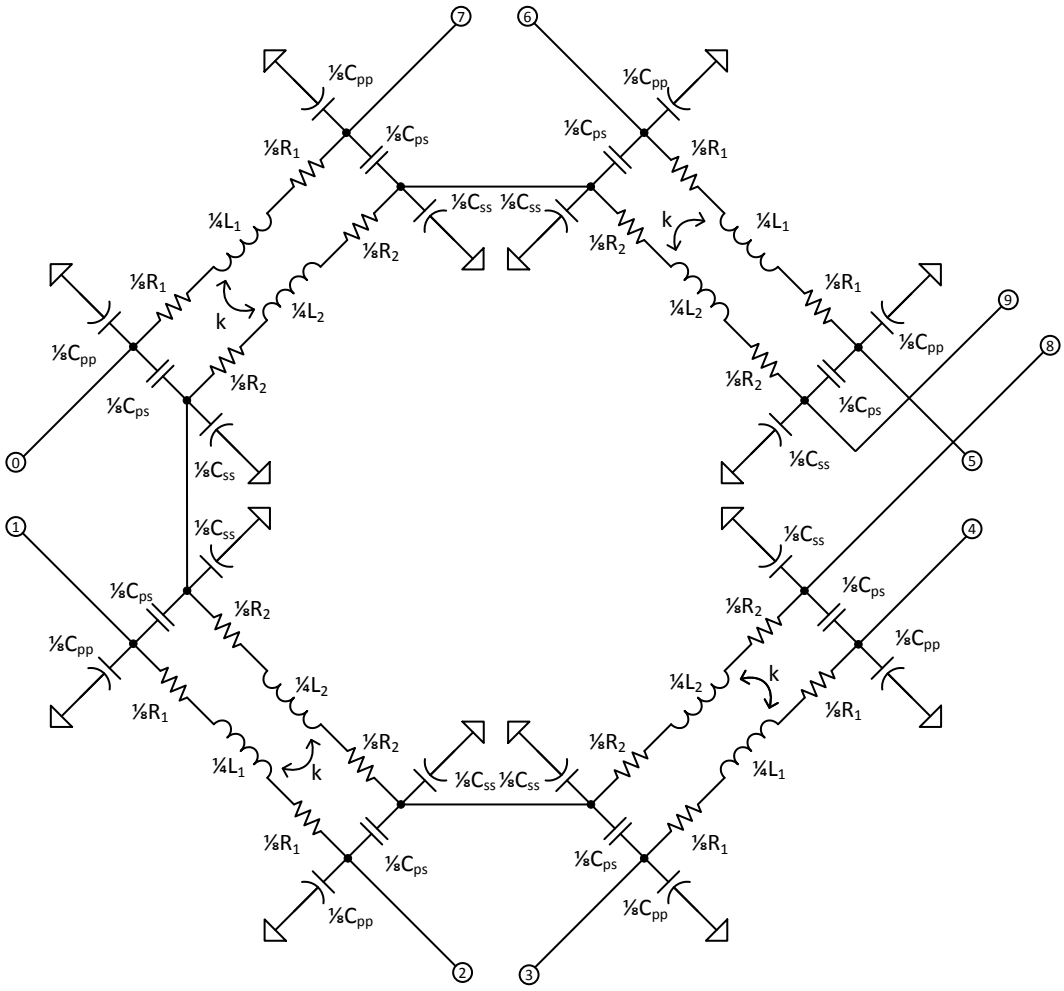
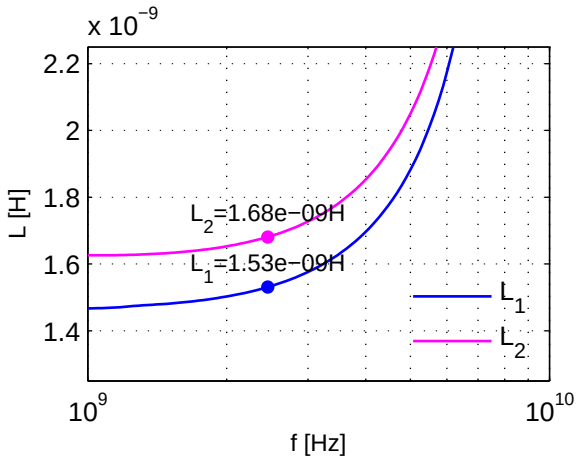
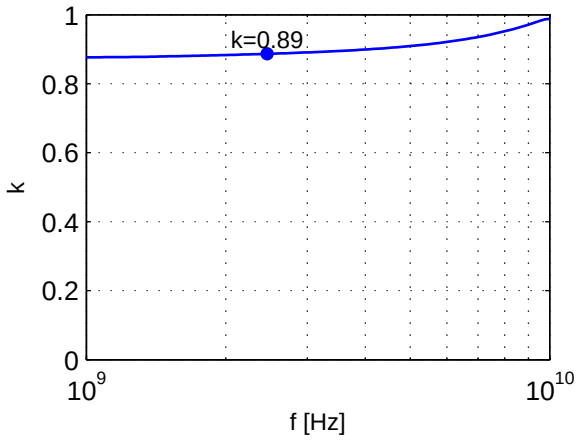


Figure 4.3: Symmetrical model of the power combiner, where $R_1 = {}^{\omega L_1}/_{Q_1}$ and $R_2 = {}^{\omega L_2}/_{Q_2}$



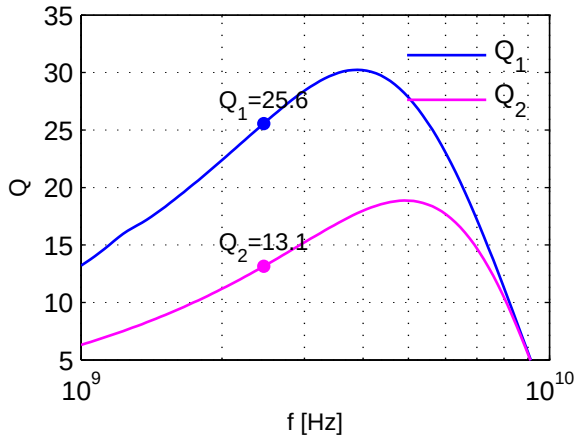
(a) L_1, L_2



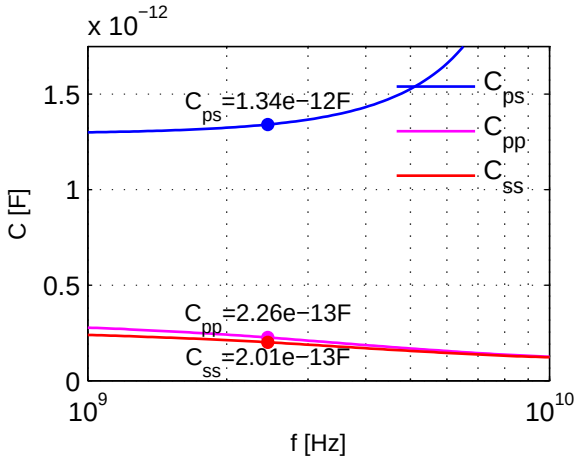
(b) k

Figure 4.4: Characterization of the combiner-in-die

High-performance RF Circuits are nonetheless often enclosed by sophisticated packaging-technologies, where multiple layers are drawn and assembled in a printed manner. The package metallizations are thick and wide, they have wide spacing between neighbors track and a thick filling to the layer above, since are meant for long interconnections of the Circuit. Thanks to their printed Technology, the package layers are quite well controlled, in the sense that their configuration can be repeated as many time as necessary, for every produced chip. Furthermore the package metallizations locate far away from the conductive substrate which is on the die, and thus they induce low Eddy currents, and have low capacitance, to the substrate, thus offering less unwanted parasitics compared to those typically found with



(a) Q_1, Q_2



(b) C_{ps}, C_{ps}, C_{ss}

Figure 4.5: Characterization of parasitics of the combiner-in-die

in-die metallizations. [40]

In Fig. 4.6 a System comprising the use of packaging-technologies in the implementation of electro-magnetic Structures is shown. Implementing a Complex Structure such as a Power Combiner using in-package metallizations is potentially a challenging task. In fact, the packaging-technology is not meant for this applications, and thus the lack of tools and models can require a significant extra amount of work both for the circuit designer and for the package designer to achieve optimal performance. Even more, customized packages require long preparation time, and a die co-design, according to bump interconnection placement in the package.

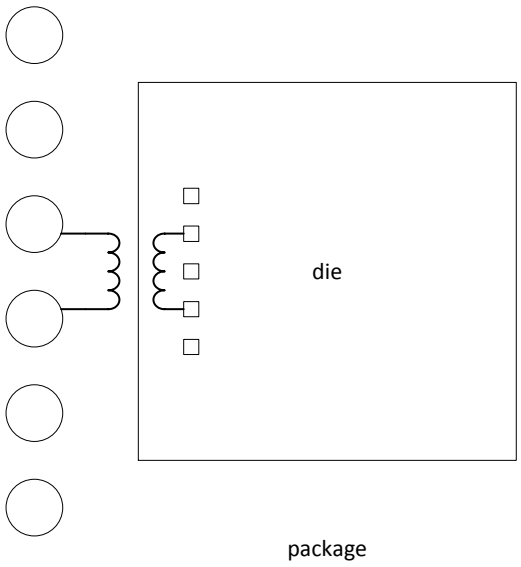


Figure 4.6: Implementation of in-package passives

In this Work, an in-package Power Combiner has been designed, and is shown in Fig. 4.7. As can be seen in Fig. 4.3, the in-package Power Combiner design is rather different than the in-die Power Combiner design shown in Fig. 4.2. Especially, the design is less detailed, since the design grid in package technologies is much larger, and the rules in the interconnections are tougher. In particular, the interleaved design has been abandoned in favor of a straightforward stacked design. The coupling-factor between distant primary and secondary layers is in fact low, and becomes a dominant concern over primary to secondary capacitance C_{ps} impact, and the wide gap between subsequent primary coils, determined by through-holes distances rules, furthermore decreases the coupling between primary and secondary coils. The coupling between primary and secondary coils is therefore improved by stacking primary and secondary exactly on top one of the another. A thick track width, reducing the parasitic resistance in the Combiner, is used in the whole Design of the in-package Power Combiner.

Referring again to the model of Fig. 4.3 it is observed, in Fig. 4.8 and 4.9, that the inductances of the in-die Power Combiner are smaller, comparing to the inductances of the in-

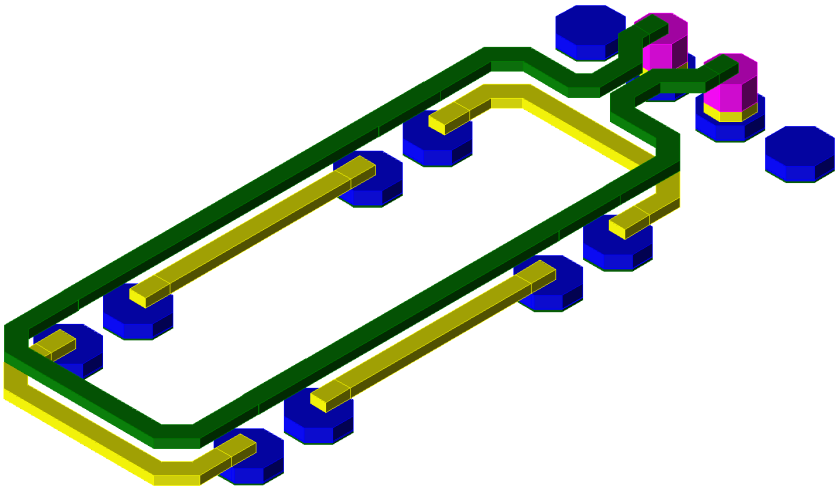
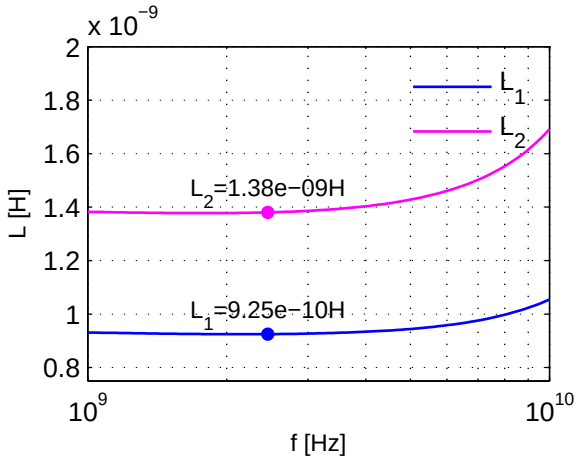


Figure 4.7: Three-Dimensional View of the Combiner-in-package

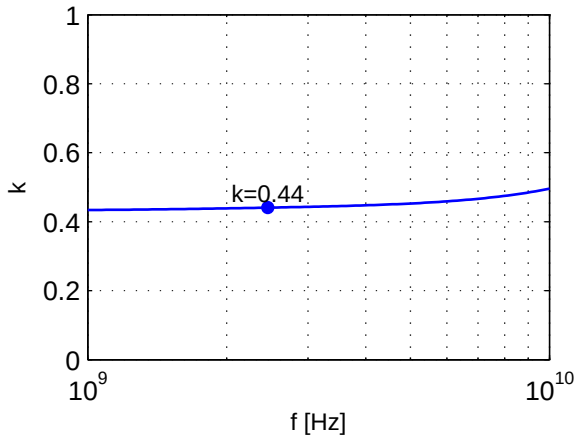
die Power Combiner. Quality-factors are high, reaching up to 50 for certain frequencies, and as already mentioned, coupling factor is limited, below 0.5. C_{ps}, C_{pp} and C_{ss} are negligible in the combiner in-package circuit.

Due to the limited coupling factor between primary and secondary coils, a higher-order Matching Network topology comparing to the Matching Network which is used for the Circuit comprising the in-die Power Combiner, is implemented. In fact, as predicted in Sec. 3.2.2 and 3.2.3, a third-order matching network would not achieve high efficiency, even though high quality-factors are obtained by passive in-package technology. Therefore an additional capacitance is added in parallel to the load resistance, so that both the primary, and the secondary inductors, are optimally resonated.

Finally, the asymmetry arising between adjacent primary coils of the in-package Power Combiner is evaluated in Fig. 4.10b. It is observed that a good symmetry of the combiner in-package is achieved, similarly to the in-die Power Combiner Symmetry. Therefore, the asymmetrical shape of the Power Combiner, is not expected to impair the symmetrical operation of the Circuit.



(a) L_1, L_2



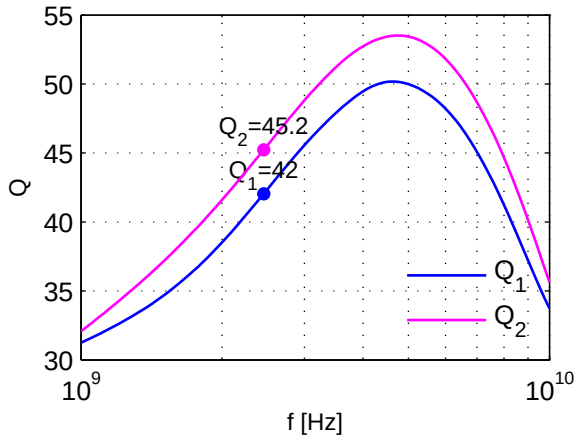
(b) k

Figure 4.8: Characterization of the combiner-in-package

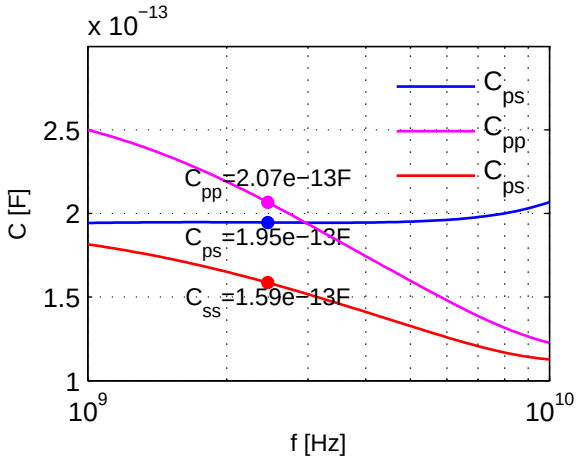
4.1.3 Die and Substrate Photographs

The in-die and the in-package Circuit samples occupy a different amount of CMOS die area. In fact, whilst the in-die circuit requires, as shown in Fig. 4.11, roughly $1mm^2$ of area of which, respectively, $0.5mm^2$ are used for the SCPA and $0.5mm^2$ for the Power Combiner, by contrast the Circuit comprising the in-package Power Combiner, Fig. 4.12, occupies an area of only $0.5mm^2$ in the CMOS die.

The packages assembled with the in-package Power Combiner is shown in Fig. 4.16. The Power Combiner shown in Fig. 4.16, is placed multiple times in the package, in fact, the



(a) Q_1, Q_2



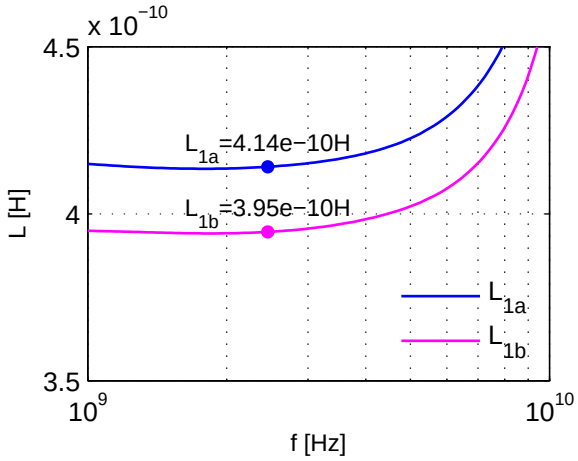
(b) C_{ps}, C_{ps}, C_{ss}

Figure 4.9: Characterization of parasitics of the combiner-in-package

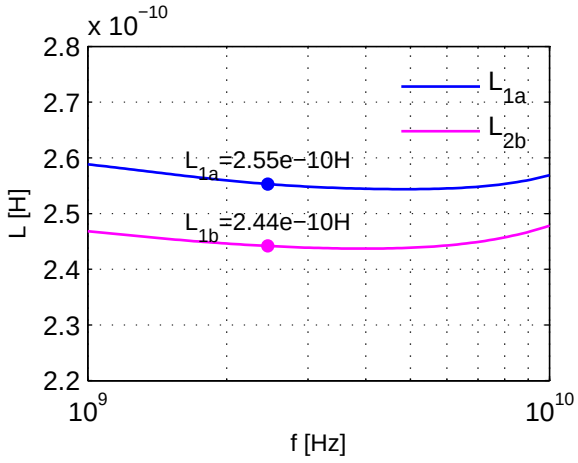
package is designed so that a copy of the Power Combiner is available for measurements through a probe-station. Measurements of the in-package Power Combiner are necessary to track fabrication process accuracy, and improve modeling of the passive in-package technology topic and thus enhancing subsequent design cycles.

4.1.4 Engineering Platform

The Circuit which has been implemented, shown in Fig. 4.13, requires a special engineering of the supply connections. The circuit, in fact, does not exhibit an intrinsic Power-Supply



(a) L_{1a}, L_{1b}, in-die power combiner



(b) L_{1a}, L_{1b}, in-package power combiner

Figure 4.10: Asymmetry in the power combiner

Rejection Ratio (PSRR), as highlighted in Sec. 2.3.1, therefore it relies on the low-dropout regulator (LDO) for supply regulation as shown in Fig. 4.15. Since the LDO is located on the board, and is connected to the Circuit through the Package, then extremely low-ohmic V_{dd} package connections are required. Due to the high Transmitter output power, achieved with a low supply voltage, the connections from the LDO Module to the circuit carry up to $500mA$ root-mean-square current during regular operation, with an instantaneous current as high as $1.5A$, and up to $3A$ for Sample comprising the in-die Power Combiner and the in package Power Combiner respectively.

Due to the high current which is transferred, even a small series supply impedance would

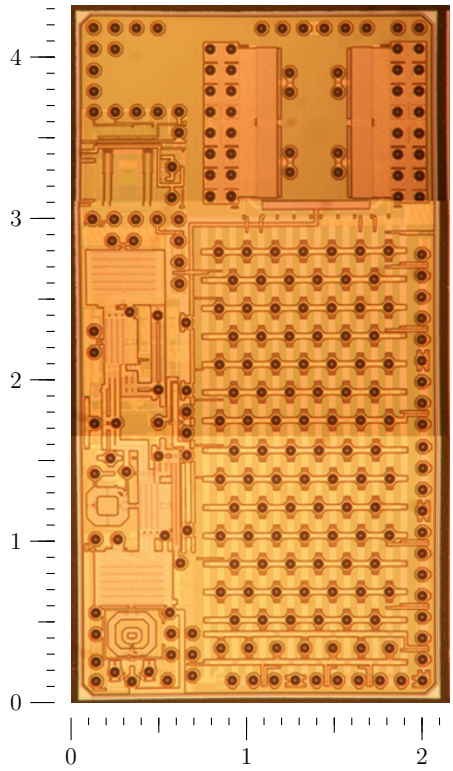


Figure 4.11: ATELP Die with Combiner-in-die with millimeter ruler. Implemented Transmitter is located at the north-east edge of the Die. Die edges are $4.32x2.16mm$ wide

induce a Voltage swing to the internal supply connection of the circuit, resulting in spurious inter-modulation products being generated at the output, and in a decreased total available Transmitter output power. A tailored Package Substrate has therefore been engineered, offering the lowest possible supply connection available in the deployed package technology, obtained by means of having multiple-parallel V_{dd} and V_{ss} bumps, up to sixteen, connected to as many balls in the board, all routed through low-ohmic supply planes. The package interconnections are shown in Fig. 4.14.

The Engineering Board furthermore comprises a socket, the aforementioned LDO and its blocking capacitance, input and output connectors and a transformer. A zero-insertion-force socket is mounted so that different samples can be fitted. To improve Engineering Board's LDO blocking capacitance, many capacitances all over the balls are implemented as a parallel combination of different capacitance values, distributing blocking cap impedance as low ohmic as possible amongst all balls and on the whole length of the interconnections. Different

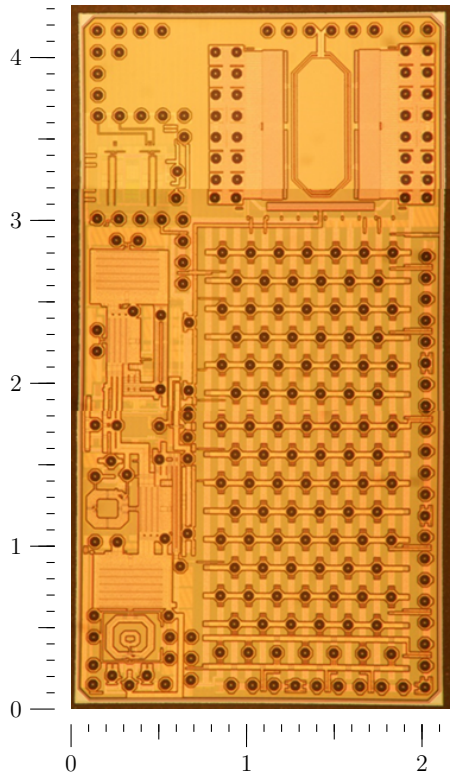


Figure 4.12: ATETP Die with Combiner-in-package with millimeter ruler. Implemented Transmitter is located at the north-east edge of the Die. Die edges are $4.32x2.16mm$ wide

capacitance values help in reducing the blocking cap impedance for a huge set of operation frequencies. Furthermore, all radio-frequency input and output connectors do have stubs, enabling fine tuning of impedance matching within the board. Spare outputs, thought for future releases of the circuit, have been implemented. A transformer, performing differential-to-single ended conversion, is optionally placed at the Circuit output, so to improve the decoupling of the circuit to the silicon substrate. Finally, a JTAG interface connects the digital part of the circuit to the testing equipments. The complete board design is shown in Fig. 4.15.

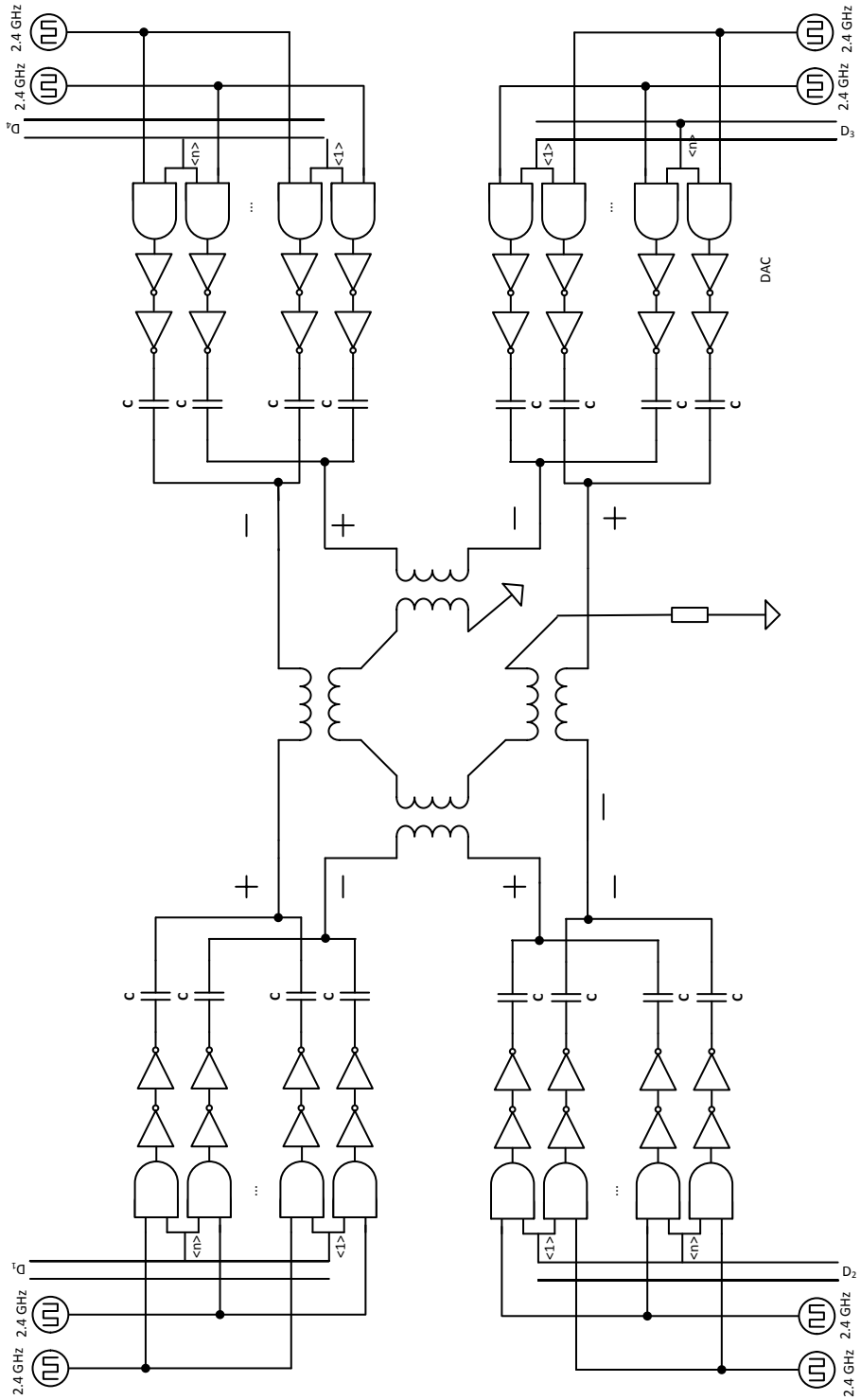


Figure 4.13: ATETP/LP DPA Circuit

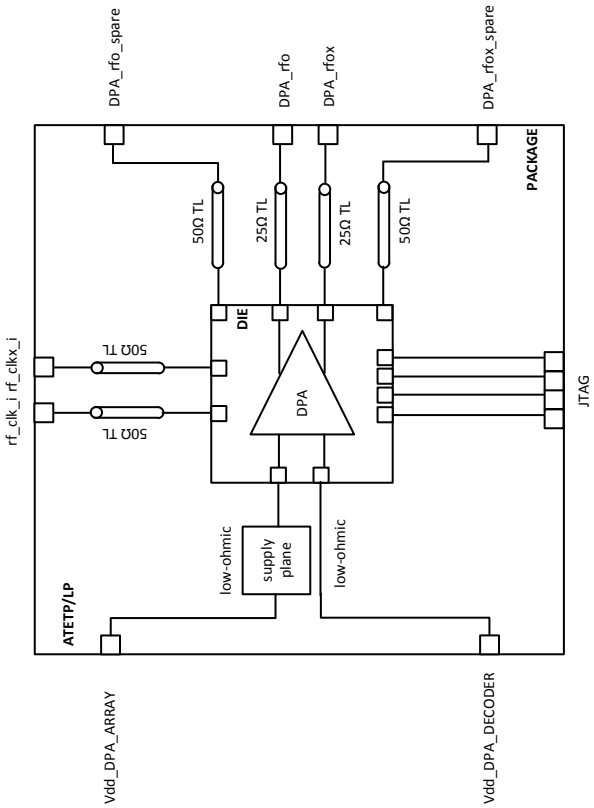


Figure 4.14: ATETP/LP Package

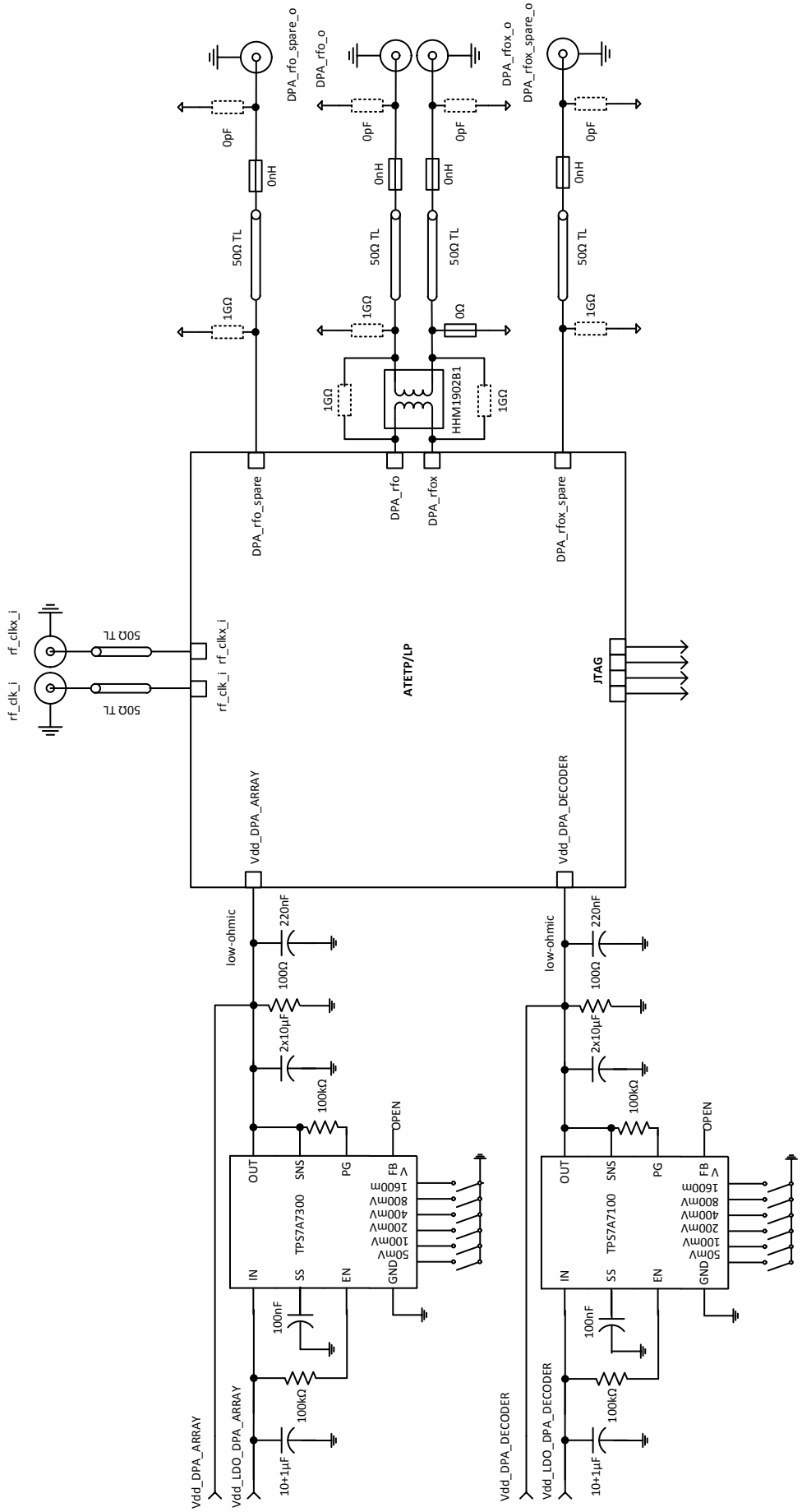


Figure 4.15: ATETP/LP Board

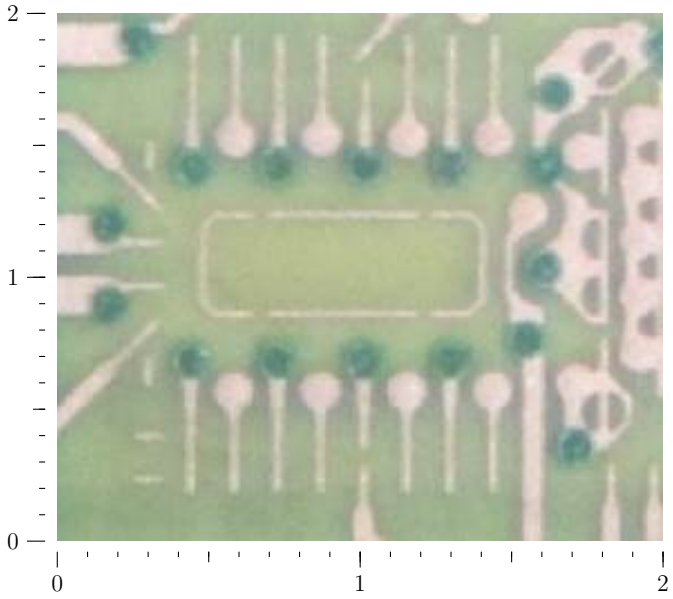


Figure 4.16: ATETP implemented combiner-in-package with millimeter ruler. Combiner edges are $0.5x1mm$ wide

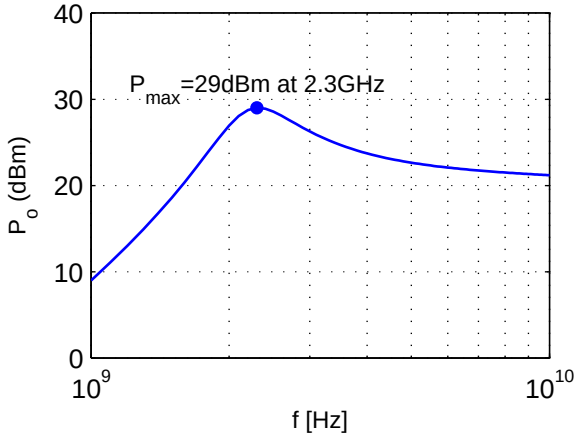
4.2 Simulation Results

4.2.1 Continuous-wave Simulations

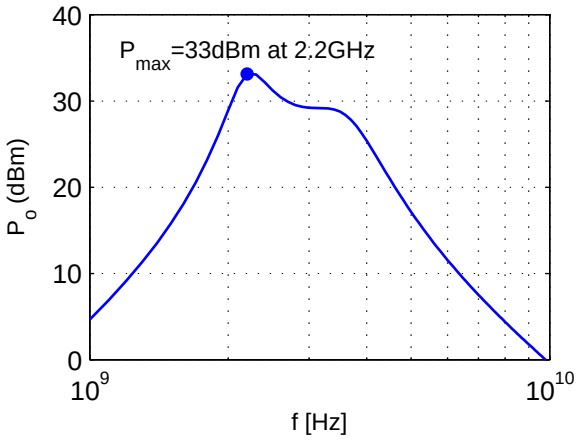
To test the efficiency of the Switched-Capacitor Power Amplifier output stage, the System is operated with a static code. At a static input code the System generates an un-modulated continuous wave at the 50Ω output load, at which output power and efficiency are measured.

As described in Sec. 4.1.1, a Pre-Scaler circuit, shown in Fig. 4.18, allows the code to be dynamically split between the SCPAs comprising the Digital-Power Amplifier (DPA). All the coefficients of the Pre-Scaler are set through configuration registers, and the Pre-Scaler itself is implemented in VHDL and synthesized and Place & Routed through Synopsis IC Compiler. Each of the four Pre-Scalers interleaving each SCPA Data Connection is configured independently.

Thanks to the Programmable Pre-Scalers, the System can take advantage of the multiple efficiency curves shown in Fig. 4.19. In Fig. 4.19, for example, at first only one out of the four available SCPA is operated. In this case, when only one out of four SCPA is operated, up to $-12dB$ with respect to the maximum peak power are obtained. A first efficiency curve



(a) On-Die Power Combiner



(b) In-Package Power Combiner

Figure 4.17: Continuous-wave Simulations, Power

as a function of the output power generated by the System, is plotted for this particular configuration. Next, two out of four SCPAs are activated, and the output power reaches up to -6dB with respect to the maximum peak power. A second efficiency curve is plotted. Finally all four SCPAs are operated at the same time, yielding up to the full peak power, and yet another efficiency curve.

Basing on the schematic of the circuit shown in Fig. 4.13, by applying superposition of effects principle one can in fact conclude [31] without further calculations, that, the maximum output voltage which is generated using one and two SCPAs is one fourth and one half the voltage generated using the set of four SCPAs, respectively. The Power Combiner sums up

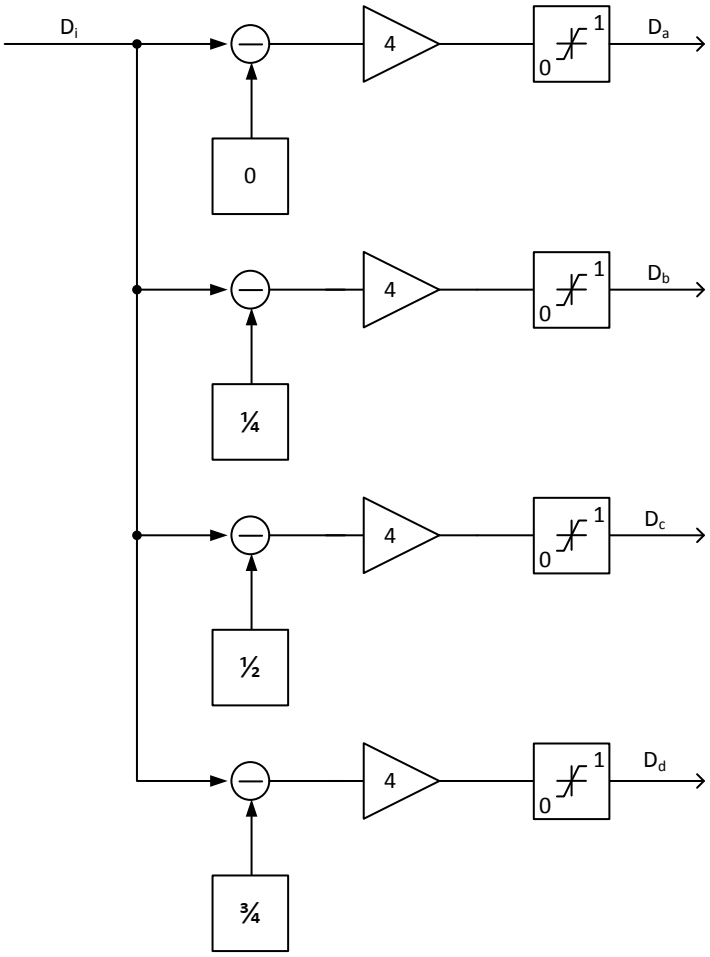


Figure 4.18: Flow-diagram of VHDL Programmable Pre-Scaler annotated with Efficiency Enhancement Operation Coefficients

in fact the Output Voltages of the SCPAs in a series fashion, and the load power on the fixed output load is then proportional to the power of the two, of the Generated Voltage. Maximum generated power is therefore -12dB and -6dB below the power generated by all four SCPAs, respectively, when only one or two SCPAs are operated.

As seen in Fig. 4.19, and for example [41], for reduced Power Levels, the efficiency of the System changes depending on the number of SCPAs which are activated, yielding the multiple efficiency curves which are plotted in the graph. The exact shape of the efficiency curves depends on the balance between the power which is lost in the Power Combiner, and

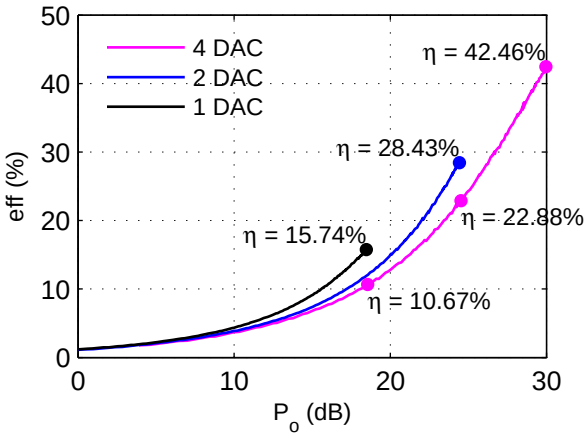


Figure 4.19: Continuous-wave Simulations, Drain Efficiency

the power which is lost in the SCPAs output stages. For a fixed level of current flowing on the primary and secondary sides of the Power Combiner, the losses in the Combiner are constant. Thus, neglecting second-order effects, at a required Power Level the losses in the Power Combiner are as well constant. However, depending on the number of SCPAs selected for generating a required power level, the power which is lost in the CMOS output stages of the circuit varies. In fact, it is known that an SCPA operated at full-scale has an higher efficiency than an SCPA is operated below full-scale [42]. Since operating only one SCPA at its full power at a time allows to minimize the power consumption in the SCPA output stage, with respect to the operation of four SCPAs at a reduced digital code, and the Power lost in the Power Combiner is constant, the asymmetric operation described is then advantageous in terms of System Power Consumption.

When the Pre-Scaler is loaded with the coefficients shown in Fig. 4.18, the code on each activated RF-DAC is maximized, therefore for a given target power level the Circuit consumption behavior is jumping between the efficiency curves of Fig. 4.19, and offers an enhanced efficiency for low required output Power. Whilst Drain Efficiency peak at 44% is unaffected, the median, i.e. $19dBm$ transmission Efficiency, is improved from 10.7% to 15.7% by asymmetric codes distribution. Median efficiency is particularly important when a signal with a high Peak-to-average Power-Ratio (PAPR) is Transmitted. In this case, $12dB$ of PAPR are observed while operating the Transmitter for Wireless Communications, as discussed in Sec. 2.2.2. Therefore, System power consumption is reduced, when modulating,

to an amount of up to 47% the total System Power when the Pre-Scaler is enabled. However, the operation of the Pre-Scaler can be programmed, since, by operating asymmetrically each of the SCPA in the System, the linearity of the System could potentially be reduced, and therefore it is important to test the difference in linearity observed during symmetric and asymmetric Circuit operation.

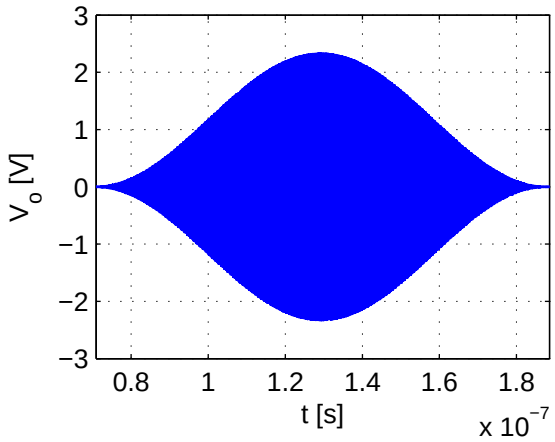
4.2.2 Envelope simulations

To test Radio-Frequency Digital-to-Analog Converter (RF-DAC) performance of the SCPA, an envelope is injected in the system. Through Envelope simulations, in fact, key performance indicators which typically characterize a RF-DAC Circuit can be measured, such as, INL, DNL, ENOB, SINAD and so on.

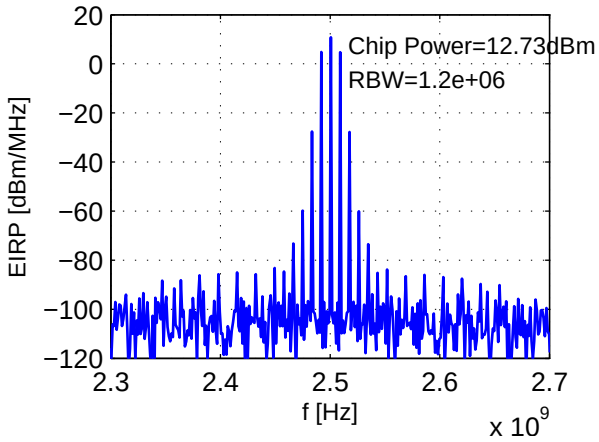
Contrary to the operation of a classic DAC, the RF-DAC defines a range of the spectrum which goes from $f_{LO} - f_{Nyquist}$ and $f_{LO} + f_{Nyquist}$, as described in Sec. 2.3.2. The spectrum outside this range, is then filled-up by the aliases and spectral images of the Synthesized Signal. Therefore, for the sake of performance calculations, noise and signal power are integrated within this range. A double-sided-spectrum (DSB) is usually considered when defining the figures-of-merit of the RF-DAC, even though, the transmitted signal exhibits Hermitian Symmetry around f_{LO} when operated under constant-phased signal operation. By contrast, when the System is operated in In-Phase/Quadrature-Phase mode, however, the Hermitian Symmetry of the signal around f_{LO} is broken, and the I/Q RF-DAC tracks the whole $f_{LO} - f_{Nyquist}$ to $f_{LO} + f_{Nyquist}$ range, as described in Sec. 2.6.3.

For the sake of these Simulations, only the In-Phase path of the implemented System has been activated, in order to evaluate the performances of the designed RF-DAC, and, to reduce Simulation time, only one RF-DAC is simulated at a time, using a tailored matching network where only one section of the Power Combiner primary and secondary coils is coupled to the output of the SCPA and to the output load, resulting, as expected, in a reduced output power at full-scale signal.

After injecting a sinusoidal envelope as a Synthesized Digital Signal, a period of the Envelope of the output of the RF-DAC is collected and evaluated through Fast-Fourier Transform. Given $W(f) = |\mathcal{F}(V_o)|^2/50$, the Power-Spectral-Density (PSD) at the output of



(a) Envelope while transmitting a $1 + cos(\omega t)$ signal centered at $8.5MHz$



(b) Spectrum while transmitting a $1 + cos(\omega t)$ signal centered at $8.5MHz$

Figure 4.20: Envelope Simulations

the RF-DAC, Noise and Signal power are calculated as follow,

$$P_N = \left[\int_{f_{LO}-f_{Nyquist}}^{f_{LO}-f_{distortion}} W(f) \cdot df + \int_{f_{LO}+f_{distortion}}^{f_{LO}+f_{Nyquist}} W(f) \cdot df \right] \cdot \frac{f_{Nyquist}}{f_{Nyquist} - f_{distortion}} \tag{4.1}$$

$$P_S = \int_{f_{LO}-f_{distortion}}^{f_{LO}+f_{distortion}} W(f) \cdot df \tag{4.2}$$

and

$$SNR = 10 \cdot log\left(\frac{P_S}{P_N}\right) \tag{4.3}$$

Table 4.1: Sinusouidal Envelope

(a) Setup Parameters

Generator	**Frequency**
Local-Oscillator (f_{LO})	$2.5GHz$
Synthesizer ($2 \cdot f_{data}$)	$1.2GHz$
Synthesized Sinusoid (f_s)	$8.5MHz$

(b) Setup Results. Effective-Number-of-Bits $ENOB = 12.75$ when spurious-range noise is neglected up to $f_{distortion} = 100MHz$ from calculations

Metric	**Power**
Signal (P_S)	$18mW$
Noise (P_N)	$0.25nW$
Signal-to-Noise Ratio (SNR)	$77.5dB$

yielding

$$ENOB_{out\,of\,SNR} = \frac{SNR - 1.76}{6.02} \tag{4.4}$$

$ENOB_{out\,of\,SNR}$ has been used as a figure of merit, instead of $ENOB$, because $ENOB$ is highly impacted by Counter-Inter Modulation (CIM) products. Counter-Inter Modulation products fall, in fact, at frequencies which are close by to the frequencies of the transmitted signal and since therefore do not impair far-off noise of the transmitter significantly it makes sense to use $ENOB_{out\,of\,SNR}$ as an important metric. Transmitted signal, whose envelope is $1 + cos(\omega t)$, contains only f_{LO} and $f_{LO} \pm f_s$ frequencies, whilst other harmonics appearing in the spectrum shown in Fig. 4.20b are CIM products. When calculating $ENOB_{out\,of\,SNR}$, CIM products up to the ninth order are rejected from SNR calculations, through the choice of $f_{distortion} = 100MHz$. The observed values of the CIM products are reported in Table 4.2. The mechanism and the effects generating unwanted counter-inter modulation products of the signal is described in Section 2.4.2.

Table 4.2: Counter-Inter Modulation (CIM) Products

Harmonic	**Absolute Level**
0	10.8dBm
1	4.7dBm
3	-27.7dBm
5	-60dBm
7	-73.5dBm
9	-85.2dBm

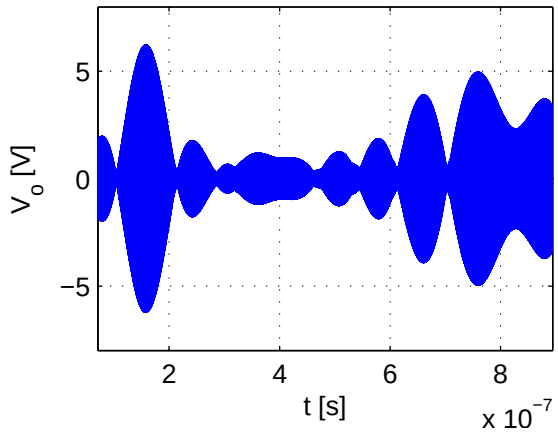


Figure 4.21: Envelope while transmitting a $20MHz$ signal

4.2.3 Simulations of System Performance

The system is as well tested with a modulated signal resembling the signal transmitted by a Wireless Transmitter. As described in Sec. 4.2.2, to speed up simulations, only one SCPA is operated at a time, using a tailored matching network where only one section of the power combiner primary and secondary coils is coupled to the SCPA and to the output, resulting in a reduced signal power at full-scale signal. To compare the observed spectrum against ETSI EN 300 328 masks, output signal power of the simulated SCPA has been up-scaled to the required Transmitter power level, using a scale factor of 4, plus antenna gain, and therefore obtaining the required reference power level.

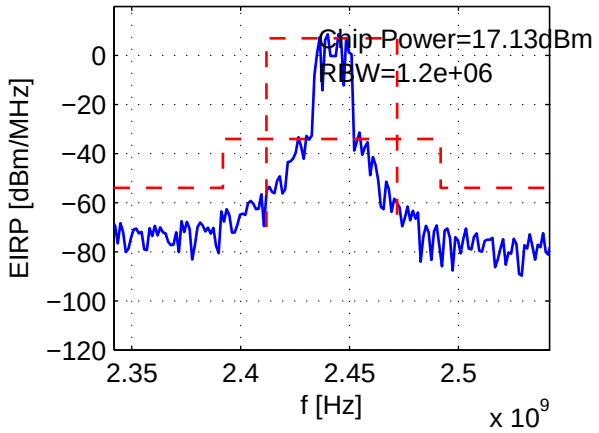


Figure 4.22: Close-in spectrum while transmitting a $20MHz$ signal. ETSI EN 300 328 limits in red, dashed line

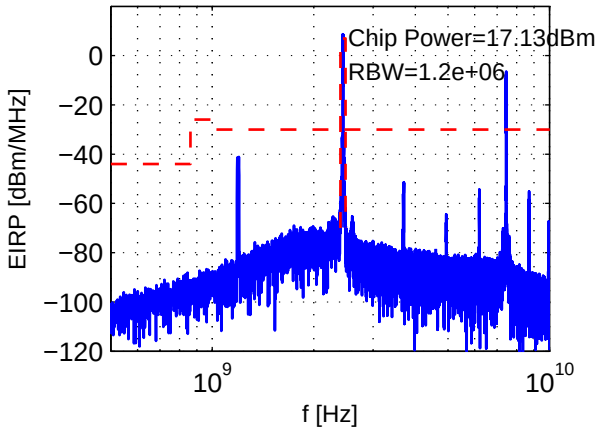


Figure 4.23: Far-off spectrum while transmitting a $20MHz$ signal. ETSI EN 300 328 limits in red, dashed line

Simulations shown in Fig. 4.22 and in Fig. 4.23 prove that the Transmitter satisfies ETSI EN 300 328 requirements for certifications both for close-in and for far-off spectrum, and show that the circuit grants enough margin to the specifications, so that the Transmitter can as well be used in case of in-device coexistence of multiple standards, as discussed in Sec. 2.5.

4.3 Comparison with the State-of-the Art

Finally, in this part of the Work, the performance of the Transmitter is compared with the State-of-the Art. Selected State-of-the Art references include 2010-2015 International Solid-State Circuit Conferences Papers [43], [44], [45], [46], [47], [48], [49], [50], [51], [52], [53], [54], [55], and [42]. Area, Power, here intended as Output Power, and Efficiency, here intended as drain Efficiency, are evaluated in this Comparison. An optimal Transmitter shall in fact have minimum Area and maximum Efficiency, while achieving the required Output Power Level, without introducing a high-level of noise and distortions.

Transmitters operating at a much lower or much higher frequency one another do not compare fairly, since power consumption is a function of the operating frequency, varying both on the CMOS output stage of the Circuit and on the Passive Structures, as shown in Sec. 3.2.1 and Sec. 3.2.3. The selection of References is therefore restricted to Circuits operating at a frequencies of operation which are located at, or close to, the ISM range of frequencies $2.4GHz$ to $2.4835GHz$.

In terms of Power and Efficiency, a comparison of the Simulated Performance of this Work to the State-of-the-art Measured Performance is shown in Fig. 4.24. Efficiency is a Key Figure-of-merit for Transmitters, and is especially important for Transmitters which are meant to be battery operated. As this Transmitter is meant for Wireless Communications, it is therefore critical to have a high Transmitter efficiency. Efficiency is defined as per Eq. 4.5. In Eq. 4.5, P_i is the Power going to the SCPA output stage, and P is the Power measured at the load, when the SCPA is operated at full-scale. Current spent in the Thermometric Decoder, shown in Sec. 3.1.3, and in the Clock Tree, presented in Sec. 4.1.1, is neglected from efficiency calculation, since this Circuit is compared with a set of Power Amplifier

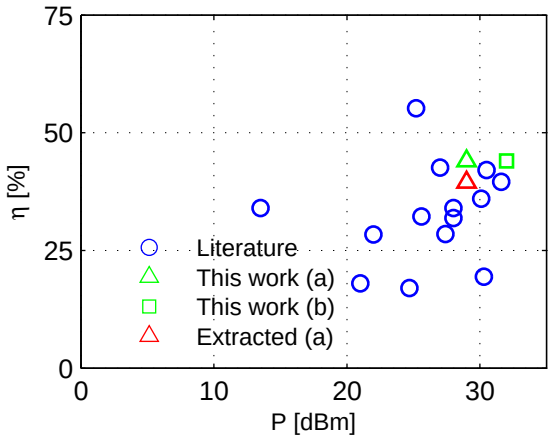


Figure 4.24: Power and Efficiency of the State-of-the-art and of this Work

Circuits, do not include digital-to-analog conversion circuits current contributors at all.

$$\eta = \frac{P}{P_i} \tag{4.5}$$

As shown in Fig. 4.24, the efficiency of the proposed circuit is in-line or better that the state-of-the-art. [42] offers the best published efficiency with $\eta = 55.2\%$, particularly high since it was obtained in an older $90nm$ CMOS technology [1] using a regular metal stack [2]. Other notable published results include [52] and [45] with $\eta = 42.1\%$ and 42.6% respectively.

Circuits exhibiting high power and high efficiency, located in the north-east corner of Fig. 4.24, are particularly attractive for building high power Transmitters. Comparing to the State-of-the-art, this Circuit is a good candidate for such an Application, both for the $29dBm$ Transmitter comprising the in-die the Power Combiner, and for the $32dBm$ Transmitter comprising the in-package Power Combiner.

The Area of the Transmitter is again an important figure-of-merit. Transmitters with a small Area footprint are in fact attractive in many regards. Compact Transmitters are especially well-suited for Multi-Input Multiple-Output Applications, where multiple Transmitters are integrated in one System. Fig. 4.25 compares Power and Area Simulated Performance of this Work to the State-of-the-art Power Amplifier Circuits Measured Performance, each Circuit being represented by a point with coordinates (Power, Area).

The Power Amplifiers presented in [51], [50], [44] and [43] offer sub-square millimeter Area

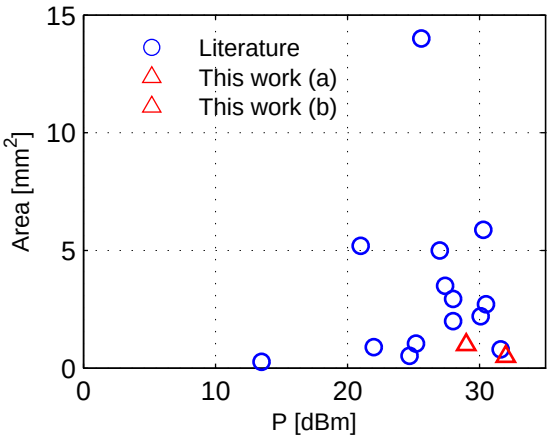


Figure 4.25: Power and Area of the State-of-the-art and of this Work

occupation. In particular, [51] has a very small area footprint of only $0.27mm^2$, however at a power level of $13.5dBm$. This work offers a high peak power of $29dBm$ and $32dBm$ in an area footprint which is of only $1mm^2$ and $0.5mm^2$ for the Transmitter comprising respectively the in-die and the in-package Power Combiner.

Key-Performance-Indicator (KPI) of power-vs-area $K_A = {}^{P}/_{A}$ is a good indicator of Circuits which can be used for building compact high power Transmitters, suitable for example for applications comprising multiple integrated transmitters, such as i.e. MIMO Applications. This Work, located in the south-est corner of Fig. 4.26, has a high Simulated value of $K_A = 0.8W/mm^2$ and $K_A = 3.2W/mm^2$ in the Transmitter comprising respectively the in-die and the in-package implementation of the Power Combiner.

An innovation which is part of this Work is the low-supply Voltage empowering the whole Transmitter. A low supply Voltage enables the Transmitter to operate from a single-supply source shared between the digital and the analog circuits comprising the Wireless Transceiver. Fig. 4.26 compares Simulated Performance of this Work to the Measured Performance of State-of-the-art Power Amplifiers, each Circuit being represented by a point with coordinates (Power, Voltage).

The Circuits at the South of the graph in Fig. 4.26 use a low Supply-Voltage. In comparison to this Work, [55], [50] and [47] operate on low supply Voltages, but higher than the $1.1V$ supply voltage empowering this Work. The lowest supply Voltage amongst selected papers is found in [47], which implements a Doherty amplifier exhibiting $28dBm$

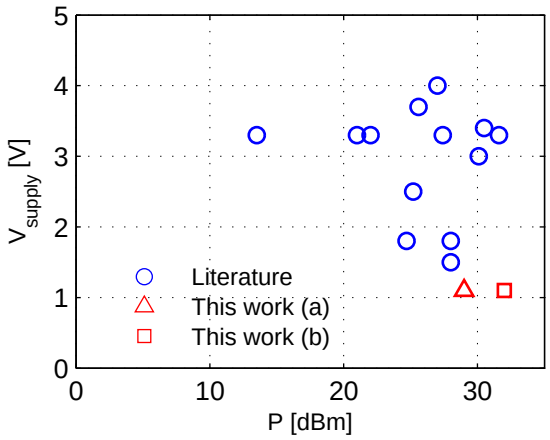


Figure 4.26: Power and Supply Voltage of the State-of-the-art and of this Work

Table 4.3: Extracted and Schematic Simulation Results. Cadence Spectre has been run in APS mode, using 16-cores of an Intel(R) Xeon(R) CPU E5-2690 @ 2.90GHz including a Helic Veloce/Raptor [39] Spectre View of the Power Combiner

Combiner Model	**Array Model**	**Power**	**Efficiency**	**Simulation Time**
Veloce/Raptor	Schematic	868mW	44.1%	2h 8m 38s
Veloce/Raptor	RC Extracted	730mW	39.5%	12d 4h 21m

output power and 34% PAE from a $1.5V$ Supply, in an area of $2.94mm^2$.

The Key-Performance-Indicator (KPI) of power-vs-supply-voltage $K_V = {}^{P}/_{V}$ is introduced as a good indicator of Circuits which can be used for building high power single-supply Voltage Transmitters, suitable for example for Applications comprising a minimum number of supply connections, such as i.e. Internet Of Things (IOT) Applications. The South-East corner of Fig. 4.26 contains the Circuits which are obtaining the highest Power at the lowest Supply Voltage. With this regard, [47] exhibits an excellent power-vs-voltage ratio K_V of $K_V = 0.42W/V$. However, this Work offers an enhanced Simulated power-vs-voltage ratio K_V which is $K_V = 0.73W/V$ and $K_V = 1.45W/V$ for the Transmitter comprising, respectively, the in-die and the in-package implementation of the Power Combiner.

Before concluding the Comparison, it is necessary to highlight the fact that the Comparison has been comparing Simulated Circuit Performance to Published Measured Performance

of State-of-the-art Circuits. In case of limited accuracy of design models, of process variations and unexpected Circuit behaviors, Measured Results do, from time to time, exhibit significant differences from Simulated Performances. A novel comparison is planned to be repeated against Measured Circuit Performances, not available at the time this Work is published. In the meantime, many Simulations have been run, to validate the accuracy of the Simulated Results. For example, RC Extracted Simulations of the layout have shown, at a fixed frequency of operation, an efficiency drop being lower than 5% comparing to Schematic Simulations, as annotated in Fig. 4.24 and shown in Table 4.3.

Chapter 5

Conclusions

Wireless Technologies are ubiquitously diffused to an ever expanding set of contexts. The IEEE 802.11 standard empowering Wireless Communications is subject to a continuous development which is pushing forward new features, increased capacities and is introducing novel applications. To guarantee backward compatibility to previous-generation standards, novel Wireless Transceivers are capable of operating selectively on multiple operating frequencies and multiple channel bandwidths. Enabling a slim, multiple standard-complaint Transceiver requires compact, reliable and flexible solutions capable of operating both with legacy and with novel Wireless Communication Standards.

In this work, a $2.4GHz$ Wireless Transmitter is developed. A rigorous analysis of official ETSI and IEEE Documents enables the definition of major Transmitter specifications. Critical System non-idealities have an important impact on these specifications, including Transmit Power, Error-Vector Magnitude and Unwanted Spectrum Emissions Masks, and are therefore carefully evaluated. Subsequently, applicable system architectures capable of fulfilling these specifications in CMOS Technology are surveyed. The benefits and limitations of Classic and Innovative System Designs are evaluated, leading to the proposal of an Innovative Digital I/Q System Architecture.

The design of the System starts with a first, a quick glimpse through $C-DAC$ and $RF-DAC$ circuits. A detailed analysis of the output stage of the $SCPA$, comprising the rail-to-rail Class-D output-stage of the $CDAC$, confirms the superior power-handling capabilities of the chosen Topology and the potentialities leveraged by digitally-intensive low-

supply voltage modern CMOS Technologies. The circuit pairs in fact nicely to the deployed deep-scaled $28nm$ CMOS technology. In the circuit, the Class-D output stage makes use of a companion Matching Network, providing an impedance transformation which ensures to reach meaningful Power Specifications. Efficiency is a major concerns during the whole design of the $SCPA$ output stage. Therefore, to further enhance the available output power, without sacrificing the efficiency, a Power-Combiner is introduced. The whole transmitter comprising several combined $RF-DACs$ is optimized against all optimal design parameters.

Finally, a Wireless Transmitter operating at $2.4GHz$ frequency and meeting previously discussed System Specifications is presented. The Transmitter is simulated to peak at $29dBm$ Continuous-Wave Output Power and is capable to provide up to $17dBm$ of Modulated Output Power while transmitting a Wireless Synthesized-Signal. Thanks to a large Base-Band Bandwidth of $1.2GHz$, and thanks to the Digital I/Q System, the Transmitter is capable of modulate a large Signal Bandwidth centered at Carrier Frequency. Furthermore, the System efficiency is simulated to peak at 44%. Thanks to a Programmable Pre-Scaler which can optimally distribute codes amongst the multiple $RF-DACs$ comprising the transmitter, up to 15% Modulated Efficiency while transmitting a Wireless Synthesized-Signal at $17dBm$ is reached, with an improvement of up to 40% compared to the case where all codes are distributed equally amongst the multiple $RF-DACs$ comprising the Transmitter.

A Variant of the Transmitter, comprising a novel Power-Combiner Structure has been developed. In the Variant, the Power-Combiner is implemented by taking advantage of novel In-Package Technologies. The In-Package Technology, offers a low-enough process-variation for large structures, and, thanks to the large metal tracks, far from the conductive silicon substrate, which can be drawn in-the-package, higher quality factors are obtained compared to classic passive-in-die Technology. A unique Test Platform enables the two Variants of the Transmitter to be tested against identical boundaries conditions. The in-package variant is simulated to yield up to $3dB$ more power than the in-die one, at a comparable level of efficiency. Furthermore, displacing the Power-Combiner in-the-package frees up up to 50% of the die-area of the Transmitter.

Thanks to the accurate $RF-DAC$ design, the Transmitter System is simulated to meet ETSI Technical Requirements and IEEE 802.11 Standard Requirements for both Variants,

which are sharing identical $SCPA$ Core Design. Key Performance Indicators show that the Circuit is at the edge of the State-of-the-art in multiple respects, especially with regard to the most innovative Variant of the Transmitter which is taking advantage of novel in-package Technologies. With respect to the simulated performances, it is seen that a modern $28nm$ CMOS Technologies offers the possibility to integrate highly efficient switched output-stages, and that, leveraging new synergies between in-die and in-package Technologies all-together, is a promising approach in the development of Innovative Systems for high-performance Wireless Communications.

List of Publications

[1] A. Passamani, D. Ponton, G. Knoblinger, and A. Bevilacqua, "A linear model of efficiency for Switched-Capacitor RF Power-Amplifiers," in *10th Ph.D. Research in Microelectronics and Electronics Conference (PRIME)*, June 2014, pp. 1–4.

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List of Patents

[3] A. Bevilacqua, D. Ponton and A. Passamani, "Injection Locked Ring Oscillator Based Digital-to-Time Converter and Method for providing a filtered interpolated Phase Signal," Patent, January, 2016.

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