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High-Temperature PCBA Baking Process Optimization

Bachelor's Thesis (12 ECTS)

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High-Temperature PCBA Baking Process Optimization

Abstract:

Baking prior to repair and rework processes is one of the steps in PCBA production that adds to the total manufacturing cycle time but is essential for quality and reliability. An analysis of the optimization of the baking process for printed circuit board assemblies is carried out. The current recommended industry baking temperature of 125°C is compared to proposed 150°C temperature for printed circuit board assemblies with halogen-free flame-retardant epoxy resin reinforced with woven glass (HFFR4) substrate material, having glass-transition temperature above 170°C prior to repair and rework processes. The goal of this analysis is to estimate the approximate time reduction by increasing the baking temperature and verify the physical effects of the same, providing a physical parameter basis for further investigations. No physical degradation is observed at both the baking temperatures, with the proposed 150°C baking temperature having a higher efficiency of moisture removal. The thesis is concluded by recommendations for further future investigations.

Keywords:

PCBA, PCB, Baking, Moisture, MSD, Delamination, Crack, SMD

CERCS:

T130: Production Technology

Kõrgtemperatuurilise kuumtöötluse optimiseerimine

Lühikokkuvõte:

Paranduse ja praagiparanduse eelne kuumtöötlus on üks trükkplaadi koostu tootmise etappidest, mis küll pikendab tootmistsüklit, aga on vajalik kvaliteedi ja töökindluse tagamiseks. Viiakse läbi trükkplaadi koostude kuumtöötluse optimiseerimise analüüs. Praegusel ajal tööstuses halogeenivabade tulekindlate tugevdatud epoksüvaigu ning kootud klaasiga (HFR4) substraatmaterialiga trükkplaatide koostude jaoks kasutatavat soovituslikku kuumtöötluse 125°C temperatuuri võrreldakse pakutud 150°C temperatuuriga. Klaasi ülemineku temperatuur parandusele ja praagiparandusele eelnevalt on 170°C. Analüüsi eesmärk on hinnata kuumtöötlustemperatuuri tõstmisega kaasnevat aja kokkuhoidu ja kontrollida selle füüsikalisi mõjusid, pakkudes välja füüsikalise parameetri edasisteks uuringuteks. Kummal kuumtöötlustemperatuuril ei täheldatud füüsikalist

lagunemist. 150°C kuumtöötlustemperatuuril oli niiskuse eemaldumine tõhusam. Uurimustöö lõpus on soovitused tulevasteks uuringuteks.

Võtmesõnad:

PCBA, PCB, Kuumutamine, Niiskus, MSD, Irdumine, Mõra, SMD

CERCS:

T130: Tootmise tehnoloogia

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TERMS, ABBREVIATIONS AND NOTATIONS

Printed Circuit Board (PCB) (*Trükkplaat*) is a laminated sandwich structure of conductive and insulating layers. It is a bare surface, with no components soldered to it (Keim, 2020).

Printed Circuit Board Assembly (PCBA) (*Trükkplaadi koost*) is an assembled PCB, containing all electronic parts required for board functioning.

Institute of Printed Circuit (IPC) *(Trükkplaatide Instituut)* is a member-driven organization that was formed with the intention of creating industry standards and supporting the advancement of the electronics industry (Kumar, 2020).

Moisture-Sensitive Devices (MSDs) (*Niiskustundlikud seadmed*) are electronic components encapsulated with plastic compounds and other organic materials (Weber, 2006).

Factory Ambient Conditions (*Niiskustundlikkuse tase*) is the environmental condition to be maintained in an electronics manufacturing factory- below 30°C /60% relative humidity (RH) (IPC/JEDEC J-STD-033D, 2018).

Floor Life (*Ajavahemik, mille jooksul tohib komponenti kasutada, enne kui see on imanud endasse liiga palju niiskust)* is the allowable time period after removal of moisture-sensitive devices from a moisture-barrier bag, dry storage, or dry bake and before the soldering process (IPC/JEDEC J-STD-033D, 2018).

Repair *(Parandus)* Action on a nonconforming product to make it conform to form, fit and functional attributes, but will not meet all drawing requirements. It may involve materials and processes that are not specified by the controlling drawing. Unlike rework, repair can affect or change parts of the nonconforming product. (IPC-T-50N, 2021)

Rework (*Praagiparandus*) is the removal of a device for scrap, reuse, or failure analysis; the replacement of an attached device; or the heating and repositioning of a previously attached device (IPC/JEDEC J-STD-033D, 2018).

Crack (*Mõra*) is a separation within a bulk material (IPC/JEDEC J-STD-020E, 2015).

Delamination (*Irdumine***)** is an interfacial separation between two materials intended to be bonded (IPC/JEDEC J-STD-020E, 2015).

INTRODUCTION

A printed circuit board assembly (PCBA) consists of various sub-parts apart from the circuit design which can affect its reliability and performance such as the materials used in the printed circuit board (PCB), solder paste, and electronic component packages as well as the assembly/repair or rework process temperature exposure. One of the critical factors associated with the PCBA material properties is the ingress of moisture in the PCBA when the prescribed floor life at factory ambient conditions has been exceeded (IPC/JEDEC J-STD-033D, 2018) or the PCBA has been subjected to conditions outside the factory, for example, field returns. This could cause subsequent critical damage to quality of the product if not treated (IPC/JEDEC J-STD-020E, 2015). High-temperature baking is one of the methods to remove moisture from electronic packages. It exposes the packages to be heated in a set-controlled environment to allow the moisture to be removed at a slow and steady rate.

MSL 1	**Floor Life (out of bag) is Unlimited**
Other MSLs	**Floor Life (out of bag) at factory ambient ≤30°C/60% RH**
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake must be reflowed within the time limit specified on the label.

Table 1. MSL classification with their respective Floor Life at factory ambient conditions. Source: IPC-J-STD-033D (IPC/JEDEC J-STD-033D, 2018).

Moisture sensitivity level (MSL) is a rating globally accepted by the electronic manufacturing companies where the component manufacturer indicates the component's susceptibility to damage due to absorbed moisture over the due course of time in normal working conditions (IPC/JEDEC J-STD-033D, 2018). The reference Table 1. illustrates the floor life of different MSL component under factory ambient conditions is below. As a PCBA often consists of various components with different MSLs, the highest MSL should be considered for controlling their production processes to ensure better quality yield.

Moisture-related concerns have heightened since the advent of surface mount devices (SMDs) and have grown increasingly common in electronics manufacturing (IPC/JEDEC J-STD-033D, 2018). Electronic packages made of plastic (as most SMD packages are) are especially susceptible to moisture and moisture-induced failure mechanisms (Weber, 2006).

Moisture enters the package mainly via diffusion when there is a difference in surface temperatures. The trapped moisture can have significant damage when exposed to high assembly/repair or rework process temperatures. The sudden variation in the temperature turns the condensed moisture turns to steam and expands rapidly creating high pressure within the package. The pressure caused due to such rapid vaporization could cause blistering (Sood and Pecht, 2010) and internal delamination, internal cracks, wire necking, thin-film cracking and in most severe cases, the "popcorning" where the internal stress is so great that it causes the package to bulge and crack with an audible "pop" sound (IPC/JEDEC J-STD-020E, 2015). Besides, physical defects, moisture can affect the overall quality of a board by altering the quality, thermo-mechanical properties, etc. It could also lower the glass-transition temperature and increase the dielectric constant, which could lead to reduction in circuit switching speeds and increasing in propagation delay times (Sood and Pecht, 2010). It can also reduce the glass-transition temperature (T_g), and cause oxidation of copper surfaces leading to poor wettability finish and solder and ionic corrosion (Sood and Pecht, 2010). Given the advancements in electronic package design, reductions in package body thickness and lead pitch are continued to be seen which make moisture sensitivity of components a bigger concern than it used to be (Weber, 2006).

Additionally, after the lead-free solder Restriction of Hazardous Substances (RoHS) directive took effect on July 1, 2006, eliminating the use of lead in solder, the assembly and repair/rework processes such as reflow and BGA machine repair/rework temperatures have increased by 20-30°C, exposing the moisture-sensitive components to even greater potential damage due to increased rate of moisture of vaporization (Sanapala *et al*., 2009).

Existing IPC/JEDEC standards help determine the bake-out times and temperatures to eliminate/reduce moisture prior to high-temperature processes or dry-pack, however, recommendations are mainly for PCBs and components separately (IPC/JEDEC J-STD-033D, 2018). For assembled boards that require high-temperature heating, manufacturers should come up with a time that works for their products (IPC/JEDEC J-STD-033D, 2018). IPC-JEDEC-J-STD-033D, under "baking of populated boards" recommends a bake-out temperature of 125 °C unless the devices or board materials cannot withstand this temperature (IPC/JEDEC J-STD-033D, 2018).

The maximum baking temperature in the table mentioned above in the standard is 125°C, with approximately 4-6 hours being the baking schedule used by some of the leading manufacturers in the industry. Determining an appropriate bake time for different products is difficult and potentially unrealistic for large-scale manufacturers due to the quantity and variety of PCBAs that require repair/rework and baking.

The bake time becomes critical since manufacturers do not want long baking times as it adds to the Total Manufacturing Cycle Time (TMCT) and reduces the production capacity (Lin *et al.*, 2022). It thus becomes important to optimize the baking schedule to come to the shortest bake time without compromising the quality of the PCBA. Here we propose to investigate the physical effects and time required to effectively remove absorbed moisture from PCBAs prior to high-temperature post-assembly process, specifically rework and repair. This will be achieved by raising the baking temperature from 125°C to 150°C prior to high-temperature post-assembly processes such as repair and rework for halogen-free flame-retardant epoxy resin reinforced with woven glass (HFFR4) substrate material, a commonly used material in mobile and telecommunication companies, with T_g above 170°C.

Package Body Thickness	**Level**	**Bake @125°C +10/-0°C <5%RH**	**Bake @150°C +10/-0°C <5%RH**
≤ 1.4mm	2	7 hours	3 hours
	2a	8 hours	4 hours
	3	16 hours	8 hours
	4	21 hours	10 hours
	5	24 hours	12 hours
	5a	28 hours	14 hours
> 1.4mm ≤ 2.0mm	2	18 hours	9 hours
	2a	23 hours	11 hours
	3	43 hours	21 hours
	4	48 hours	24 hours
	5	48 hours	24 hours
	5a	48 hours	24 hours
> 2.0mm ≤ 4.5mm	2	48 hours	24 hours
	2a	48 hours	24 hours
	3	48 hours	24 hours
	4	48 hours	24 hours
	5	48 hours	24 hours
	5a	48 hours	24 hours

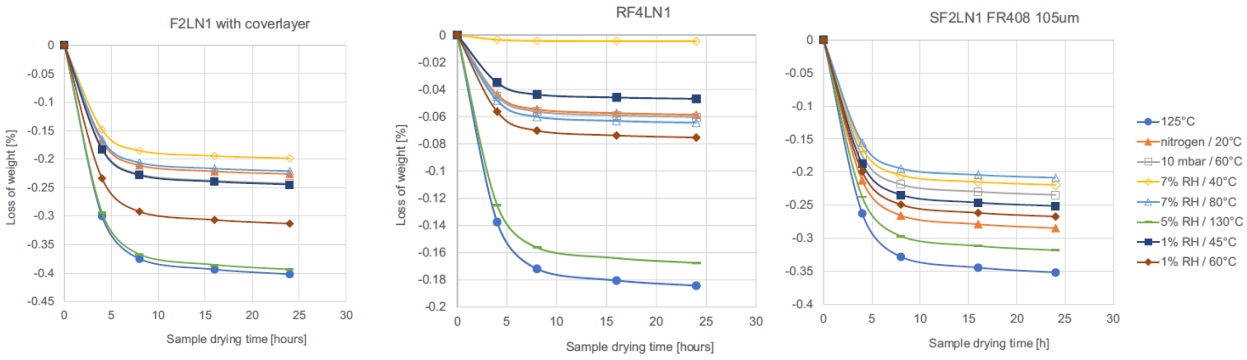
Table 2. Baking Schedules prior to Dry Pack in IPC- JEDEC-J-STD-033D.

As per Table 2. from IPC-JEDEC-J-STD-033D, 150°C was chosen in this research as it was below the used PCB material T_g and could reduce baking time by half.

1 LITERATURE REVIEW

Moisture is an invisible pest in the electronics industry. A lot of factors such as factory environment conditions, device packaging properties, and exposure time of devices to the environment can play a role in moisture absorption and consequent damage such as delamination, cracking, and warpage when subjected to high-temperature processes. Besides, physical defects, moisture can affect the overall quality of a board by altering the quality, thermo-mechanical properties, etc. It could also lower the glass-transition temperature and increase the dielectric constant. (Weber, 2005)

(Sanapala *et al.*, 2009). studied the effect of changes in key FR-4 PCB laminate material properties and their possible variations due to lead-free soldering exposures. In the study, it was found that high-temperature assembly/repair and rework process exposures tended to lower the glass-transition temperatures and out-of-plane coefficient of thermal expansion (CTE) of the laminate materials and increase water absorption. This could be attributed to the degree of cross-linking and the extent of water absorption in the exposed laminates, resulting in a more hydrophilic sample after reflow.



(i) (ii) (iii)

Figure 1. The weight loss over time for A) FLEX B) RIGID-FLEX C) SEMI-FLEX.

(Ciszewski *et al.*, 2022). compared a few moisture removal methods on FLEX, RIGID-FLEX, and SEMI-FLEX PCB, using the Fickian law to discuss their results. Eight drying tests were studied, some with changes in their physical attribute to compare the acceleration in moisture removal. The boards were first humidified using a climate chamber at 40˚C and 93%RH for 24 hours. The drying methods were then used to remove moisture from the PCBs in an annealing chamber at 125˚C without humidity control, in a nitrogen-filled chamber at a temperature of 20˚C and humidity below 1% RH, in a vacuum chamber at a pressure of 10

mbar and in a chamber with humidity control at 40˚C/7% RH, 80˚C/7% RH, 130˚C/5% RH, 60˚C/<1% RH and 45˚C/<1% RH separately. To prevent any negative effects of the drying temperatures, the moisture removal time was assumed to be the time when characteristics of the changes in weight loss reached saturation point. As expected, for all the PCB types, temperatures above 100˚C were most effective, as it is above water's boiling point. 125 ˚C and 130˚C/5%RH drying parameters had the fastest effect on moisture removal respectively while other methods such as nitrogen-chamber at 20˚C (in SEMI-FLEX) and 45˚C/60 ˚C at <1%RH came close as is evident from Figure 1. All the drying techniques took approximately 8 hours to remove moisture before reaching saturation point.

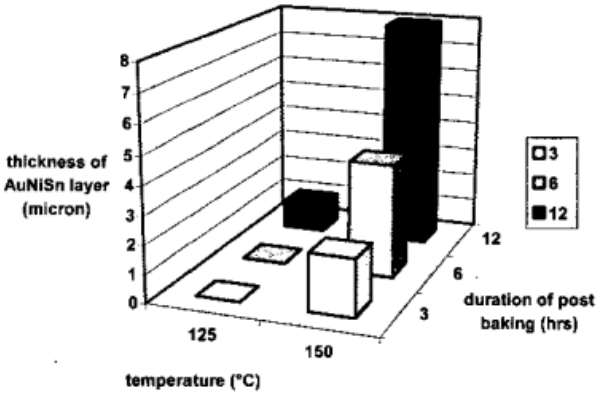


Figure 2. Impact of baking on the IMC thickness.

(Lin *et al*., 2004) point out and explain that baking could reduce moisture-induced failures but could at the same time lead to weak intermetallic compound (IMC) formation (from Sn-Pb solders on BGA components) stressing the importance of a risk trade-off to optimize baking parameters. The paper compares two baking temperatures- 125°C and 150°C for up to 168 hours and using scanning electron microscopy, concludes that the IMC formation is greatly reduced at 125°C compared to 150°C as shown in Figure 2. There was also a strong correlationbetweenh the silver content in the solder paste and the IMC formation. Howevnce after the RoHS lead-free directive, this study does not hold high importance as the paper does its analysis on leaded solders.

(Technical Report submitted to Area Array Consortium, 1999) compared the solderability of components of leaded and lead-free solder alloys after baking. Sn/Pb, Sn/Ag, and Sn/Ag/Cu/Sb solder alloys were evaluated and solderability tests for each were done pre-bake as well as after 24 hours, 48 hours and 72 hours at 150°C. This was done to expose the bumpcomponentstns to levels of oxidation whiaffects on the solderability, and thus an effect on the yield and reliability of the produced PCBA. It was found that the lead-free solders

did not show any signs of degradation, while the leaded solders did show some solderability issues after 24 hours which could be attributed to oxide contamination on the solder-bump.

(Horaud *et al.*, 2003) studied the impact of humidity and baking on the wettability of PCB material. Regarding baking suggestions, it was concluded that one hour of baking at 120°C has almost the same efficiency as 1.6 hours at 110°C, 2.1 hours at 100°C, 3.1 hours at 90°C, and 5.6 hours at 80°C. For HF and FR-4 material, 4 hours of baking at 120°C was needed to remove moisture from the PCB thinner than 2.5mm, stored at 50%+/-10%RH, and 8 hours at 120°C for the same if been stored for more than 2 months.

Package Body Thickness	**Level**	**Bake @125°C +10/-0°C <5%RH**		**Bake @90°C +8/-0°C ≤5%RH**		**Bake @40°C +5/-0°C ≤5%RH**	
		Exceeding Floor Life by > 72 h	Exceeding Floor Life by < 72 h	Exceeding Floor Life by > 72 h	Exceeding Floor Life by < 72 h	Exceeding Floor Life by > 72 h	Exceeding Floor Life by < 72 h
< 0.5mm	2a	1 hour	1 hour	2 hours	1 hour	12 hours	8 hours
	3	1 hour	1 hour	3 hours	1 hour	22 hours	8 hours
	4	1 hour	1 hour	3 hours	1 hour	22 hours	8 hours
	5	1 hour	1 hour	3 hours	1 hour	23 hours	8 hours
	5a	1 hour	1 hour	4 hours	1 hour	26 hours	8 hours
> 0.5mm ≤ 0.8mm	2a	4 hours	3 hours	15 hours	13 hours	4 days	3 days
	3	4 hours	3 hours	15 hours	13 hours	4 days	3 days
	4	4 hours	3 hours	16 hours	13 hours	4 days	3 days
	5	4 hours	3 hours	16 hours	13 hours	4 days	3 days
	5a	4 hours	3 hours	16 hours	13 hours	4 days	3 days
> 0.8mm ≤ 1.4mm	2a	8 hours	6 hours	25 hours	20 hours	8 days	7 days
	3	8 hours	6 hours	25 hours	20 hours	8 days	7 days
	4	9 hours	6 hours	27 hours	20 hours	10 days	7 days
	5	10 hours	6 hours	28 hours	20 hours	11 days	7 days
	5a	11 hours	6 hours	30 hours	20 hours	12 days	7 days
> 1.4mm ≤ 2.0mm	2	18 hours	15 hours	3 days	2 days	25 days	20 days
	2a	21 hours	16 hours	4 days	2 days	29 days	22 days
	3	27 hours	17 hours	5 days	2 days	37 days	23 days
	4	34 hours	20 hours	6 days	3 days	47 days	28 days
	5	40 hours	25 hours	8 days	4 days	57 days	35 days
	5a	48 hours	40 hours	10 days	6 days	79 days	56 days
> 2.0mm ≤ 4.5mm	2	48 hours	48 hours	10 days	7 days	79 days	67 days
	2a	48 hours	48 hours	10 days	7 days	79 days	67 days
	3	48 hours	48 hours	10 days	8 days	79 days	67 days
	4	48 hours	48 hours	10 days	10 days	79 days	67 days
	5	48 hours	48 hours	10 days	10 days	79 days	67 days
	5a	48 hours	48 hours	10 days	10 days	79 days	67 days
Exception for BGA package > 17mm x 17mm or any stacked die package	2-5a	96 hours	As above per package thickness and moisture level	NA	As above per package thickness and moisture level	NA	As above per package thickness and moisture level

Table 3. Reference table from IPC- JEDEC-J-STD-033D.

For post-assembly drying processes, little to no research exists to determine baking temperatures and times. As per IPC-JEDEC-J-STD-033D (IPC-JEDEC J-STD-033D, 2018), Table 3. must be considered to determine a bake cycle prior to rework with a default bake-out temperature of 125°C for populated PCBAs.

A general rule of thumb to bake such PCBAs in the electronics manufacturing industry is 125°C for 4-6 hours. (TR1 by Company A., 2014) conducted a study to come up with an easy-to-use rule to find a time and temperature for baking prior to high-temperature rework process. They used a typical company's bare PCBs and components for the analysis. The samples were first baked for 24 hours at 125°C to remove any initial moisture, soaked at 85%RH 85°C for up to six days for moisture absorption, and then baked at 90°C, 105°C, and 125°C for up to 210 mins (or 350 mins in some cases). The weight of the samples was measured regularly for moisture absorption and desorption data. It was found that about half of the moisture remained in the samples.

A second run with IPC- JEDEC-J-STD-033C (latest revision at the time) recommendations with varied times based on sample thickness were followed and it was found that nearly all the moisture escapes from the samples. A table was created with percentage weight loss during bake out of each sample for the three baking temperatures by assuming that the weight loss relationship will continue until the recommended baking time. It was found that baking at 90°C and 105°C did not give clear results for when a baking time can remove enough moisture- at least 60-70%. Time to reach the desired moisture bake-out level for 125°C was found to be 4 hours with 6 hours for some.

Most of the literature on the baking of moisture-sensitive devices (MSDs) is limited to a maximum of 120°C -130°C temperatures and the focus field is the impact of humidity and high reflow temperatures on the quality and reliability of the boards/components. Researches are quite specialized, may it be a particular material/finish or electronic package, or PCB. More attention is paid to comparing different drying methods, a little to none on the effect of increasing the baking temperature.

2 THE AIMS OF THE THESIS

The current baking process uses a 125°C temperature for 4-6 hours which does not guarantee to effectively remove the moisture in the PCBA which gives the opportunity to investigate the optimal temperatures to reduce the baking process time for PCBAs. This thesis work will focus on studying the physical effects of increasing the PCBA baking temperature to optimize the drying process prior to rework and repair.

The aim is to:

- Estimate the approximate reduction in PCBA baking time before rework/repair processes at higher temperatures compared to 125°C, to reduce the existing TMCT.
- Verify the post-baking physical effects/damage.
- To provide physical parameter basis for further electrical and mechanical reliability analysis.

3 EXPERIMENTAL PART

3.1 METHODS

This section introduces various methods that were used for the conduction of the proposed experiment to investigate the effect of higher baking temperature on the physical condition of the PCBAs. The section will give a detailed description of individual methods, individual parameters, and their working conditions.

3.1.1 Moisture Soak

The moisture mass absorbed by a non-hermetic material usually occurs in two states- physical and bound (Placette *et al.*, 2012). The first is known as Fickian diffusion and is the ingress of moisture from the environment to micropores to achieve concentration equilibrium (Placette *et al.*, 2012). The second state is a non-Fickian behaviors and happens when the water molecules become chemically bonded to the polymeric material (Placette *et al.*, 2012). Both the states govern the moisture absorption in a specimen, with one being more predominant than the other at period of time *(Placette et al, 2012)*.

$$M_t = M_{\infty,1}\left[1 - \frac{8}{\pi^2}\sum_{n=0}^{\infty}\frac{1}{(2n+1)^2}\; exp\left[\frac{-(2n+1)^2\pi^2 D_1 t}{4l^2}\right]\right] + M_{\infty,2}\left[1 - \frac{8}{\pi^2}\sum_{n=0}^{\infty}\frac{1}{(2n+1)^2}\; exp\left[\frac{-(2n+1)^2\pi^2 D_2 t}{4l^2}\right]\right] \quad \text{-Eq(1)}$$

Eq. 1 dual-stage absorption with M_t being the sum of moisture at both stages at time t and $M_{\infty,1}$ and $M_{\infty,2}$ being the total moisture mass gain in each state with D_1 and D_2 being the diffusivity (Placette *et al.*, 2012).

Figure 3. Climate Chamber.

Moisture soak is a method for moisture absorption by placing the specimen in a climate chamber for a certain period of time at a set temperature and relative humidity (RH). This method is used in order to replicate the moisture absorption condition by MSDs when placed in normal working conditions outside or within production. The soak parameters in this study were 85°C85%RH for 168 hours according to IPC-J-STD-020E (IPC/JEDEC J-STD-020E, 2015). Figure 3. shows a model of a climate chamber.

3.1.2 Baking

$$M_t = M_{0,1}\left[\frac{8}{\pi^2}\sum_{n=0}^{\infty}\frac{1}{(2n+1)^2}\ exp\left[\frac{-(2n+1)^2\pi^2 D_1 t}{4l^2}\right]\right] + M_{0,2}\left[\frac{8}{\pi^2}\sum_{n=0}^{\infty}\frac{1}{(2n+1)^2}\ exp\left[\frac{-(2n+1)^2\pi^2 D_2 t}{4l^2}\right]\right] \quad \text{-Eq(2)}$$

Similar to moisture absorption, Eq. 2 represents the dual-stage desorption with $M_{0,1}$ being the maximum moisture content that can be desorped at the desorption temperature and $M_{0,2}$ being the trapped moisture represented $M_\infty - M_{0,1}$ with D_1 and D_2 being the diffusivity of the first and second stage respectively (Placette *et al.*, 2012). Desorption occurs not only for the free-state molecules but also for the weakly bound water molecules (Placette *et al.*, 2012). Hence, in this model, the first stage is taken as the moisture that is removal and the second is the trapped moisture (Placette *et al.*, 2012).

Figure 4. Baking Oven.

Baking is a method for removing absorbed moisture by placing the specimen in a baking oven at low or high temperatures for different lengths of time. Forced air circulation for even and efficient heating of specimen, control of humidity at <5%RH as per IPC/JEDEC standards, addition of an inert gas such as nitrogen to reduce the oxygen present in the oven are some modifications that can be added to the drying process to optimize it. The baking oven used in this thesis has forced air circulation and maintained relative humidity of <5%RH. Figure 4. shows a model of a baking oven.

3.1.3 Visual Inspection

Visual Inspection is a method to observe physical visual defects on the device surface usually under a magnified view using an optical microscope with a maximum magnification power of up to 40X depending on what is being inspected as per IPC A-610H (IPC-A-610H, 2020). It can be used to detect visual deformities on the PCBA such as component bulging, PCB surface changes, cracking, melting and oxidation detection.

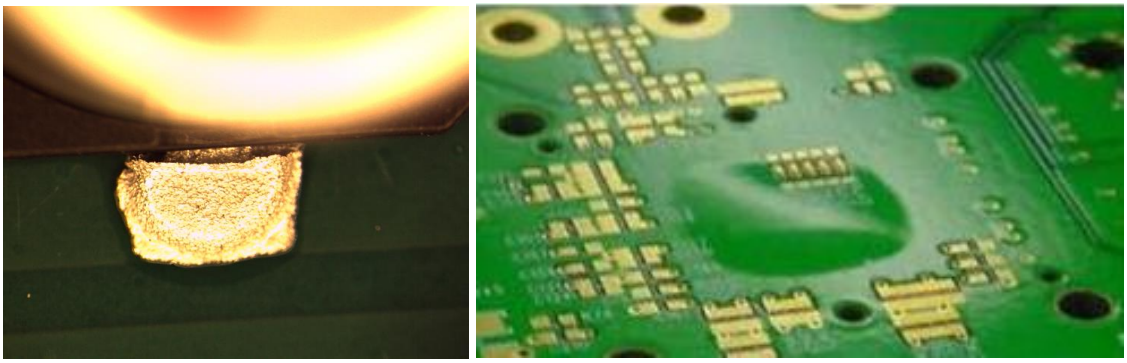


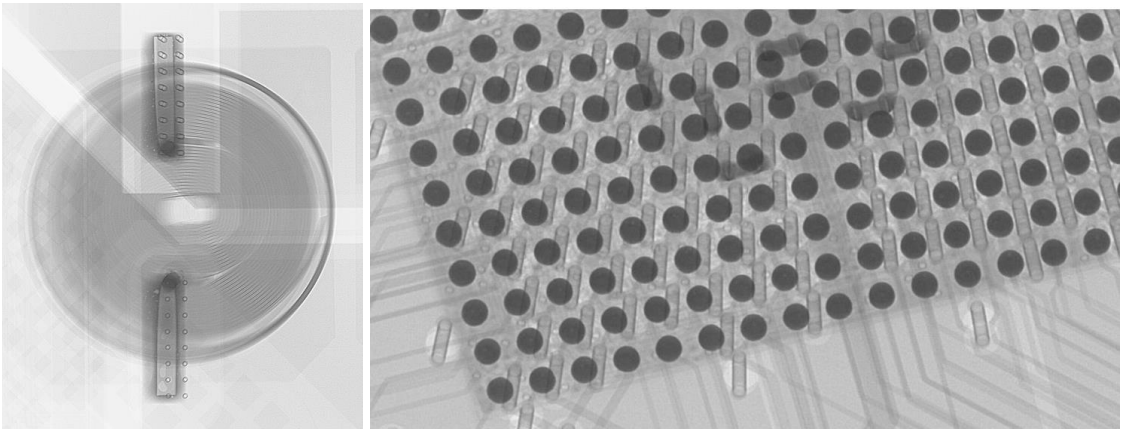
Figure 5. Fault detection via Visual Inspection.

Examples of visual inspection on PCBAs is shown in Figure 5. In the thesis, a digital microscope of up to 136.5d X was used due to the ease in ergonomics when it came to viewing the PCBA at different angles.

3.1.4 X-Ray

X-ray inspection is a non-destructive analysis technique used to inspect parts not visible to the naked eye or via visual inspection. The X-Ray source is able to penetrate through the layers of electronic devices which can help in the examination of various internal parts of the same. 2D, Isocentric Motion Technology (also known as 2.5D) and Computed X-Ray Tomography analysis are some examples X-Ray inspection methods with 2D being the most conventional method able to detect hidden faults such as cracks, voids and delamination due to its ability penetrate substrate materials (Aryan *et al.*, 2018). However, the top-down

approach of 2D X-Ray becomes insufficient to inspect solder joints thoroughly, increasing the research in the Isocentric Motion Technology, which tilts the sample to get an oblique view and Computed X-Ray tomography field which provides a 3D view of the samle (Aryan *et al.*, 2018). The main disadvantage with the Computed X-Ray tomography being the low image resolution and data acquisition and processing times (Aryan *et al.*, 2018).



(i) (ii)

Figure 6. (i) 2D X-Ray Image of an electrolytic capacitor (ii) 2.5D X-Ray Image of a Ball Grid Array Component.

2D and 2.5D X-Ray inspection methods were used for this thesis. Figure 6. shows some examples of images from X-Ray analysis.

3.1.5 Cross-sectioning

To observe the inner vertical planes of the specimen which is not visible via visual inspection or X-Ray inspection, cross-sectioning analysis can be used. Also known as micro-sectioning, this method is a destructive examination technique which involves specimen to be cut and ground through the area of interest in order to expose the inner planes for examination under a microscope (TR2 by Company A., 2020). It provides information on the internal structure, material and design (TR2 by Company A., 2020).

For this, the PCBA section of interest is first sawed at the target line, leaving a margin for later grindings to reduce sample size. It is then embedded into an epoxy block to ease in handling and rigidity and protection. The block containing the section of interest is grinded and polished to smooth out the rough surfaces during cutting and examined under a microscope.

For the study, this analysis method will be used for detection of delamination, IMC growth detection, cracking and voiding in the solder joints. It will also be used to investigate the internal layers of multilayer PCBs. Cross-section analysis is especially considered to investigate vertical areas of interest to corelate it with X-Ray analysis to understand the nature of the fault, defect or problem in detail.

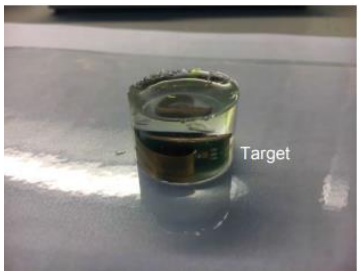


Figure 7. Target molded in epoxy material.

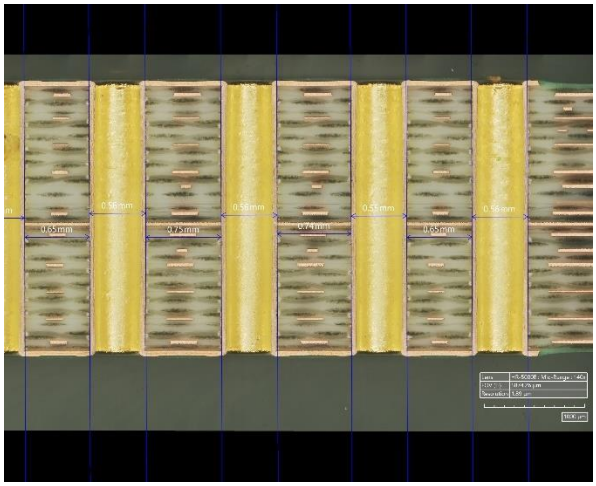


Figure 8. PCB testing via cross-sectioning analysis.

Some limitations to this analysis method include (TR2 by Company A., 2020):

- Limited size of components – must fit into mold
- Tall and big components cannot be cut due to equipment limitations.
- Can only see at a single cross section
- No direct information what is going on elsewhere, since small piece is cut out of board
- Time consuming

Figures 7. and 8. show a target section in epoxy material during the sammple preparation and an image from PCB testing via cross-section analysis respectively.

3.2 MATERIALS

Based on the above-mentioned methods, the following materials were used (TR2 by Company A., 2020).

Critical Component type	**Reasons for failure**
Big Components	Big Components More material = more expansion = more stress on solder joints
Electrolytic Capacitors	Might experience some visual bulge.
Plastic Ball Grid Array (PBGA)	CTE mismatch between packaging body and PCB.
Application Specific Integrated Circuit (ASIC), Field Programmable Gate Array (FPGA)	CTE mismatch between component package and PCB causing delamination of internal planes and internal stress. Moisture absorption in the bond wires can lead to short circuit.
Oven Controlled Crystal Oscillator (OCXO)	CTE mismatch, Moisture ingress in OCXOs can cause fluctuate the frequency of oscillations considerably, causing a short circuit.
Integrated Circuit with Fine Pitch Ball Grid Array (FBGA)	Smalled contact surface with PCBA, chances of solder joint damage.
DC/DC converter components	CTE mismatch Big size transformer in DC/DC part, will mix the mechanical stress and solder joint fatigue together, make the solder joint easier to fail.

Table 4. List of critical components on the PCBA.

- Five identical scrap 26-layers PCBAs with TU-863+ and TU-862HF laminate material with Tg of 170°C due to it being a standard board being produced with average size and thickness along with a good variety of components. The highest MSL on the PCBA was 3. Some of the more sensitive components on the PCBA along with the reason for failure is listed in Table 4.
- High precision scale with a tolerance of ±0.05g for moisture weight gain/loss measurements.
- Climate chamber for moisture soak.
- Baking oven for moisture removal.
- Digital microscope with 168.5d X magnification for visual inspection.
- X-ray machine for X-ray analysis.
- Grinding and polishing equipment for cross-section specimen preparation.
- Digital 3D microscope for cross-section analysis.

3.3 PROCEDURE

The modelling of the experiment was partly based on the methods described in IPC-J-STD-020E (IPC/JEDEC J-STD-020E, 2015).

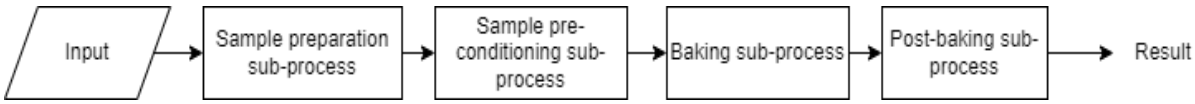


Figure 9. Schematic flow of the experiment.

The experimental part can be divided into four sub-processes as shown in Figure 9 and named as sample preparation sub-process, sample pre-conditioning sub-process, baking sub-process and post-baking sub-process. The input consisted of the five identical 26-layers test PCBAs- P1, P2, P3, P4 and P5. The experimental work initiated with the reception of the 5 test PCBAs.

During sample preparation, the samples underwent long controlled baking to ensure they all had the same initial conditions before proceeding to subsequent steps. They were then pre-conditioned by forced moisture absorption to simulate the moisture present during saturated working conditions. The pre-conditioned boards were subjected to baking sub-processes at high temperatures and then finally analyzed in the post-baking sub-process. Further detail on the sub-processes will be discussed below.

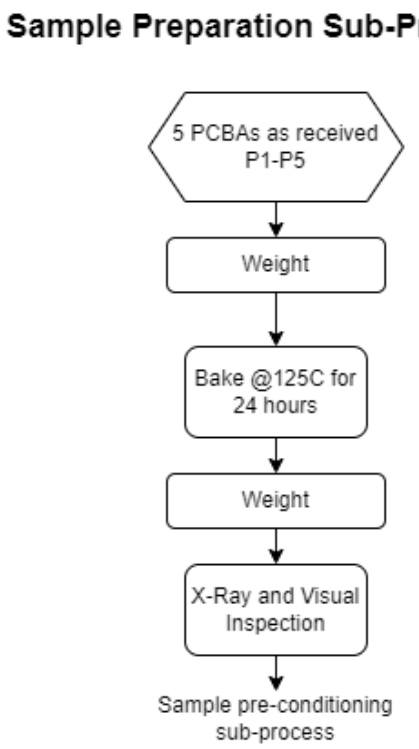


Figure 10. Sample preparation sub-process.

The test specimens- P1, P2, P3, P4 and P5 were baked for 24 hours at 125°C to remove any existing moisture and ensure that all the PCBAs start at the same base point. The samples were weighed pre- and post-bake to obtain the initial and dry weight. X-Ray and Visual Inspection was conducted for all samples as a reference to note down any existing physical defects that were present on the samples. The schematic flow of this sub-process is shown in Figure 10.

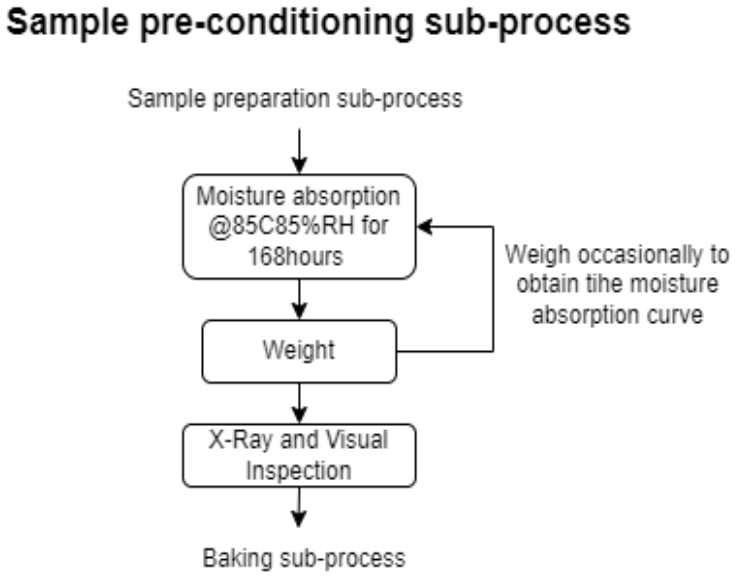


Figure 11. Sample pre-conditioning sub-process.

The prepared samples were then ready to be pre-conditioned as per Figure 11. They were placed in a climate chamber at 85°C and 85% RH for 168 hours to ensure moisture absorption in the samples to simulate the moisture present in normal working conditions. Samples were occasionally taken out and weighed using a high precision scale with a tolerance of ±0.05g to obtain the moisture absorption curve frequently in the beginning and less towards the end of the process as it reached the saturation point.

Now, the PCBAs were soaked in moisture, like they would be if their floor life was exceeded or they were being returns from the customer, i.e., left factory conditions. The soaked boards underwent X-Ray and Visual Inspection to compare pre and post bake conditions

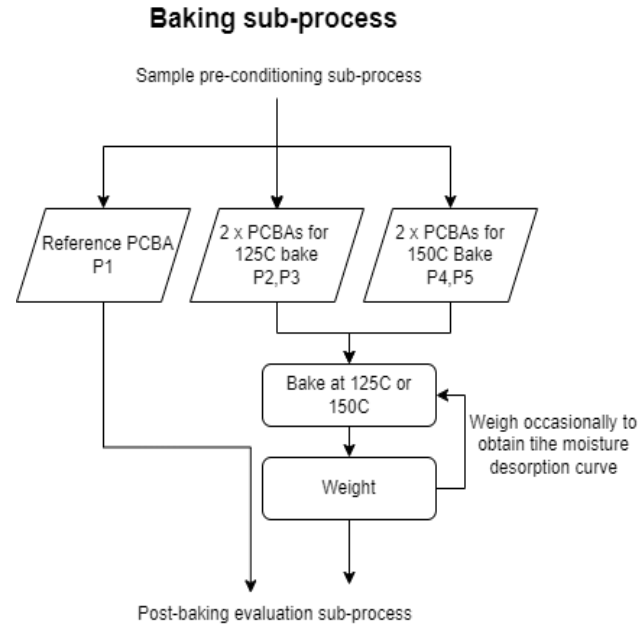


Figure 12. Baking sub-process.

P1 was taken out as a reference board to compare cross-section analysis results with. The remaining four PCBAs- P2, P3, P4 and P5 were divided in two parts as shown in Figure 12. P2 and P3 were used for the 125°C bake temperature to estimate the efficiency of moisture removal. P4 and P5 were used for 150°C bake temperatures.

125°C and 150°C sub-groups were baked in a baking oven until approximately 80% of the moisture by weight was removed from the PCBAs; following the 125°C bake study mentioned in the literature review.

In order to obtain the moisture desorption curve, PCBAs were occasionally weighed, frequently in the beginning of the bake due to a faster moisture removal rate as shown in the literature and less frequently towards the end to get the moisture desorption curve.

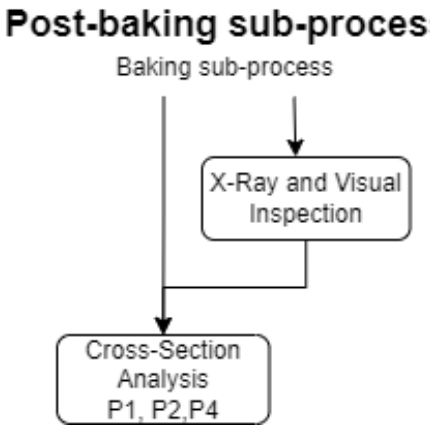
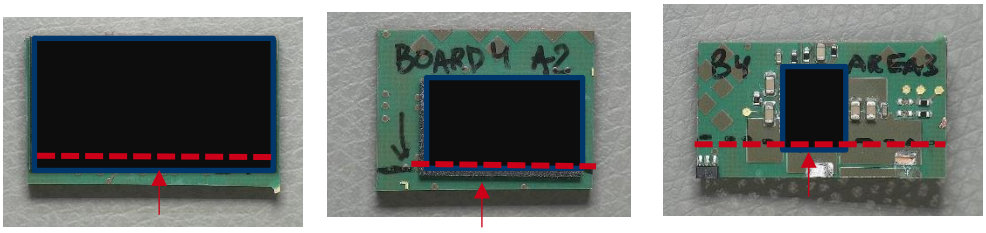


Figure 13. Post-baking sub-process.

The PCBAs underwent X-ray, Visual Inspection and cross-section analysis to study the physical effects the baking temperature might have caused as shown in Figure 13.



(i) (ii) (iii)

Figure 14. Cross-section areas for (i) Area 1 (ii) Area 2 (iii) Area 3.

Three areas on the PCBA were selected for cross-section analysis as shown in Figure 14. Area 1 focuses on analysis of Application Specific Integrated Circuit (ASIC)/Field Programmable Gate Array (FPGA) microcircuit which acts as a CPU for a specific application in the design circuit. As the FPGAs work on low power and is more prone to variations depending on the temperature and moisture changeovers. Bond wires used to interface silicon wafer with package peripherals. These bond wires are made out of gold, aluminium metals. The moisture absorbed in these entities is very ciritical and may lead to the breakdown of the component, making it important to investigate the internal changes with the help of cross-section analysis.

Area 2 focuses on Integrated Circuit (IC) with Fine Pitch Ball Grid Array (FBGA). Ball Grid Arrays (BGA) are widely used in many electronic packages. The special kind of lead arrangement under its component body makes it more critical to solder and repair and rework. A fine pitch BGA provides a smaller contact surface for its solder pin, making it more critical than normal BGA packages. These fine pitch packages are more prone to show solder joint damage due to the effect of entrapped moisture. That is why area 2 was selected

for cross-section analysis to investigate the effect of high baking temperature on its solder joint reliability.

Area 3 focuses on IC for integrated power stage in a high component density area of the PCBA as these power ICs tend to generate excessive heat during its continuous use, which may cause damage due to entrapped moisture.

Only one of the PCBAs from the bake sub-groups were sent for cross-section analysis- P2 and P4 as shown in the schematic. The temperature sub-group samples were randomly selected using the „lottery method“ which chooses a sample at random similar to „drawing from a hat“ (Thomas, 2020). The remaining samples will be analyzed after the conclusion of this thesis.

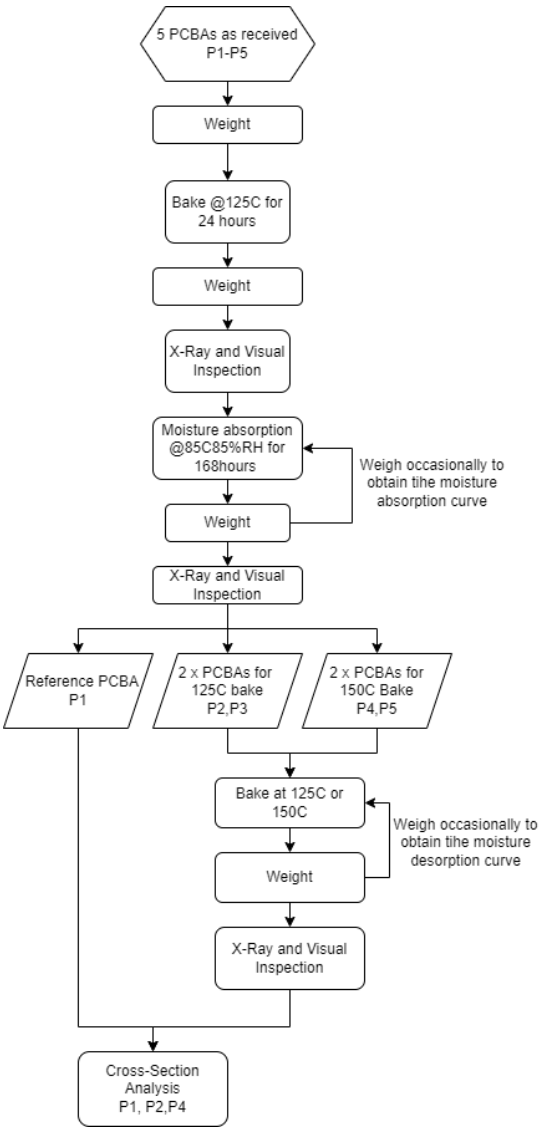


Figure 15. Procedure Flow.

The complete procedure is also shown in Figure 15.

3.4 RESULTS

In this section the results of the work are provided. Moisture variation with respect to relative time will be used to indicate what time interval is suitable to efficiently remove ~80% of moisture. X-Ray, Cross-section and Visual Inspection Analysis will then be used to detect any physical degradation that might have occurred during the experiment.

3.4.1 Moisture Absorption and Desorption Curve

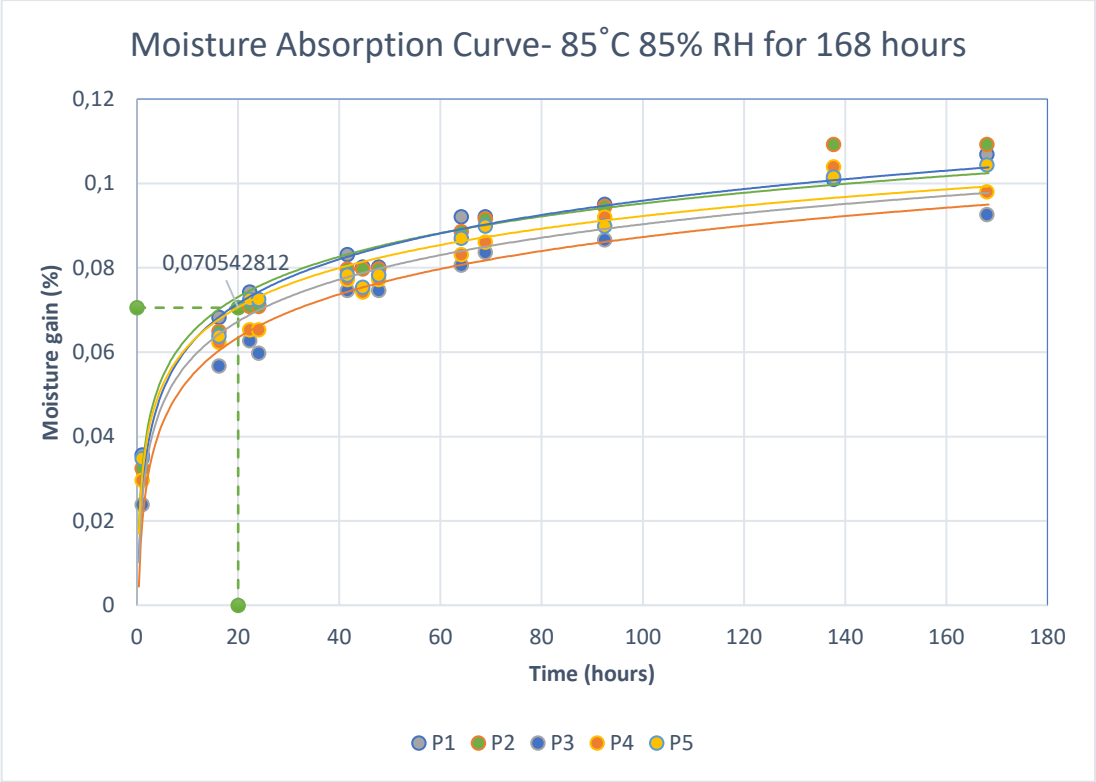


Figure 16. Moisture Absorption Curve of P1-P5.

Figure 16. shows the forced moisture absorption of the samples under 85°C at 85% RH for 168 hours in the climate chamber, all samples having the same absorption curve. The Fickian diffusion rate governs the moisture absorption in the early stages of the moisture soak, causing quick uptake of moisture (Placette *et al.*, 2012).However, with time, as the package gets saturated, the diffusion rate significantly decreases from ~0,06 grams/hour or 0,0035 gain%/hour for the first 20 hours to ~0.004 grams/hours or 0,0002 gain%/hour for the remainder of the period. This could either be because the absorbed moisture could be getting absorbed to polymers, reducing the amount of moisture absorbed via classic diffusion by limiting the space in the nanopores or because the relaxation rate becomes larger than the diffusion rate and governs the rest of the absorption process (Placette *et al.*, 2012).

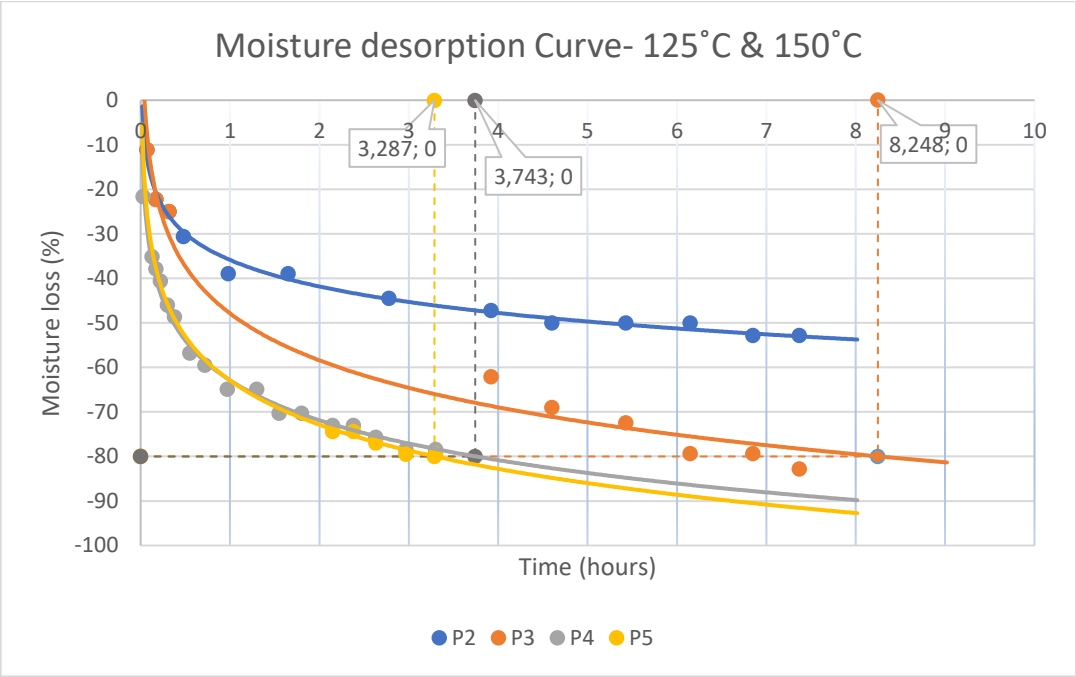


Figure 17. Moisture Desorption Curve of P2-P5.

$$\text{Moisture loss \%} = = \frac{\text{Weight at the time of bake} - \text{Weight at the end of soak}}{\text{Weight at the end of soak} - \text{Weigiht after the initial 24 hr bake}} * 100 \quad \text{-Eq(3)}$$

Moisture loss % needed to create the moisture desoprtion curve was calculated using Equation 3.

As indicated by Figure 17., P2 and P3 moisture desorption curve after 125°C bake is varied. The initial goal was to bake was to bake out ~80% of the absorbed moisture and check the effectiveness of the 4-6 hours bake. The experiment for 125°C was stopped after 7,37 hours with P2 losing ~52% of its absorbed moisture at 7,37 hours and P3 losing ~82% of the moisture at the same time according to weight calculations. This difference in moisture loss may be attributed to the smashing of an electrolytic capacitor off P3 during placement in the baking oven for the 24 hours initial bake in the sample preparation sub-process. Considering that all the samples had similar moisture removal during the initial 24 hours bake and moisture absorption trend, the reasoning for this variation in moisture desorption in Figure 17. is unknown.

P4 and P5 under the 150°C had similar desorption trends, with the experiment ending at 3,3 hours with ~78% and ~79,5% moisture being desorbed by weight calculation. The same reading was observed at 2,97 hours as well.

Sample	Rate of moisture desorption (grams/hour)	
	before 1 hour	after 1 hour
P2	-0,645948	-0,045178603
P3	-0,694202	-0,075155721
P4	-1,1638165	-0,124427609
P5	-1,2274665	-0,140231957

Table 5. Rate of moisture desorption for test samples P2-P5.

There is significant change in the rate of moisture removal observed after 1 hour for all the samples as shown in the Table 5. The significant drop in the rate of moisture loss could be because of the dual desorption model with the free-state moisture escaping quickly at high temperatures and the moisture chemically bound to the materials, reducing the desorption rate (Placette *et al.*, 2012).

Sample	Calculated time for given moisture loss (%)	
	80% moisture loss	100% moisture loss
P2	170,7	1754,7
P3	8,3	29,9
P4	3,7	17,6
P5	3,3	13,3

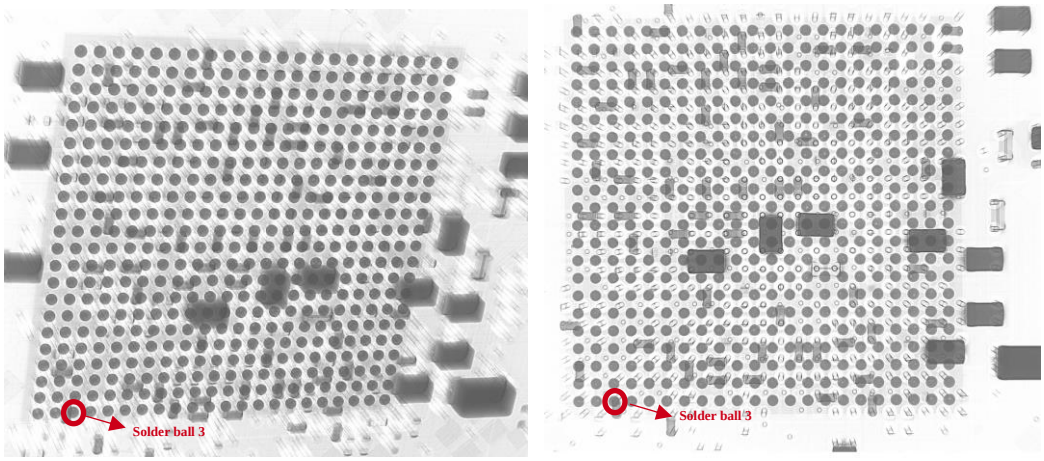
Table 6. Calculated times for 80% and 100% moisture loss.

Extrapolating from the trendline, Table 6. presents the estimated time for 80% and 100% moisture loss for all the test samples. Not only does the 150°C baking temperature effectively remove the moisture compared to 125°C, it also does it faster. This is because higher temperatures have higher energy, which can break more hydrogen bonds that bind to PCBA materials (Placette *et al.*, 2012).

3.4.2 X-Ray and Cross-Section Analysis of Area 1, Area 2 and Area 3

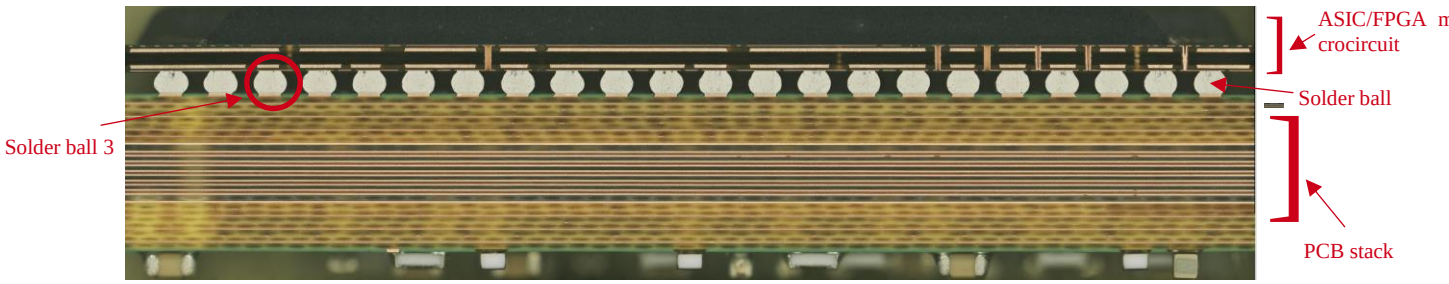
Oblique view X-Rays not presented for P2 and P4 and top and oblique view X-Ray images for P3 and P5 are presented in Appendix I.

3.4.2.1 Area 1- P1

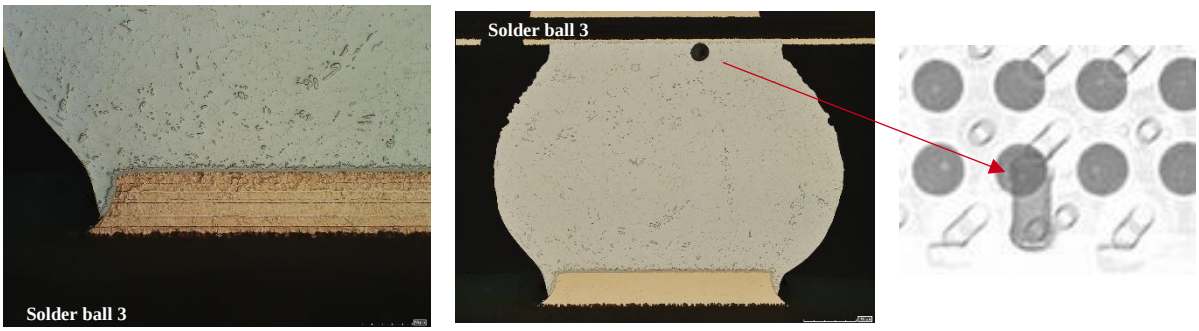


(i) (ii)

Figure 18. Pre-Soak X-Ray Reference Image (i) Top View (ii) Oblique View.



(i)

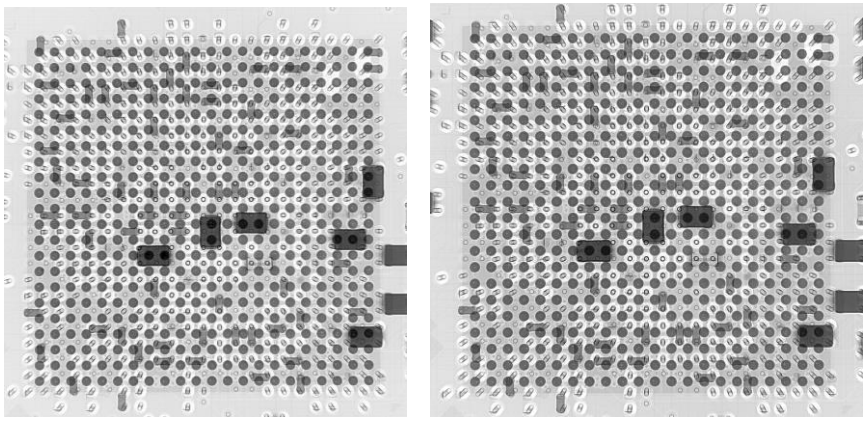


(ii) (iii)

Figure 19. (i) Cross-section overview at 140X magnification of Area 1 (ii) Close-up bottom area of solder ball number 3 (iii) Overview of solder ball 3 showing a void also visible on the X-Ray image.

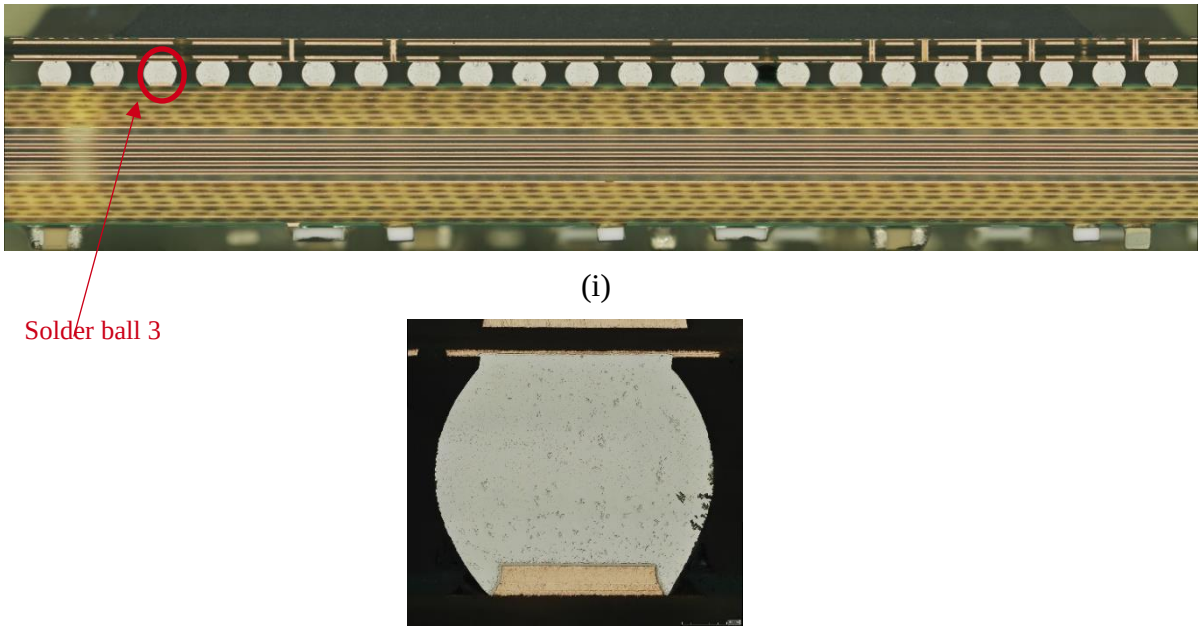
Figure 18. shows the X-Ray Image of the Reference board for cross-section analysis. The ASIC/FPGA microcircuit showed no prior defects except some voiding in the solder balls as is visible in Figure 19 (iii). The voiding is visible in the pre-soak X-Ray image as well, indicating that the voids must have been formed during the reflow soldering process, which is a common occurence and different for each board which is why it will not be compared to the samples. When high heat is applied to such a surface, localized stress might increase, causing the solder balls to crack. Further results will validate if the baking sub-process temperatures could have caused some cracking in the balls. Although unusual for normal baking temperatures, if extremely high-temperatures are applied, cracking may occur.

3.4.2.2 Area 1- P2



(i) (ii)

Figure 20. (i) Post Soak (ii) Post Bake X-Ray Image Top View



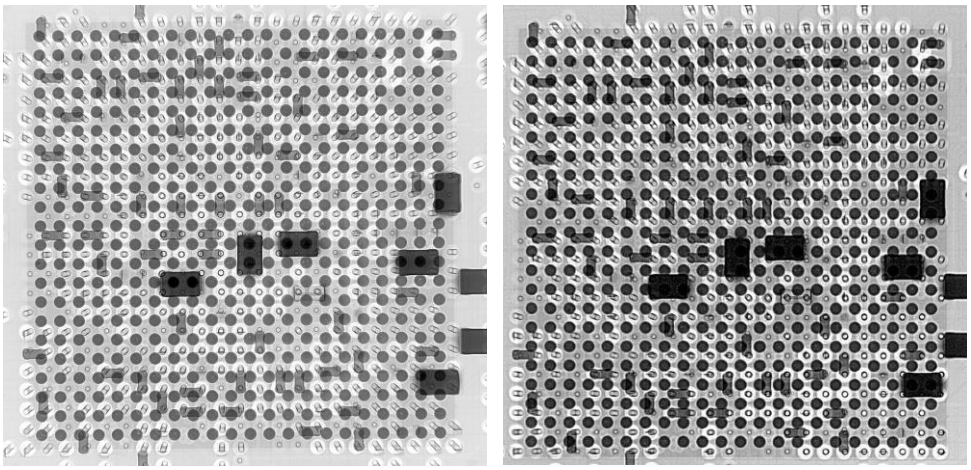
(i)

(ii)

Figure 21. (i) Cross-section overview at 140X magnification of Area 1 (ii) Overview of solder ball 3 showing no signs of defect.

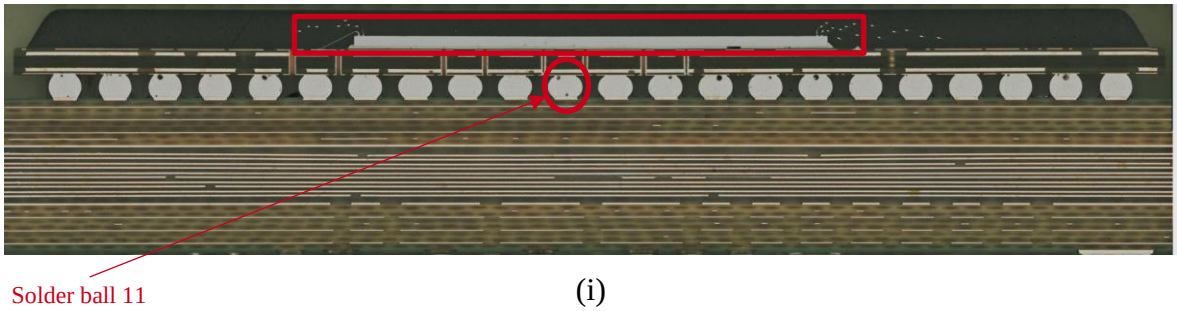
No signs of defects were visible on Figure 20. and Figure 21. The post-soak and post-bake X-Ray analysis in Figure 20 (i) and (ii) were the same. Compared to the reference cross-sectioned image, no changes were observed post-bake. The voiding that occured during in P2 was better as is seen in Figure 21 (ii).

3.4.2.3 Area 1- P4

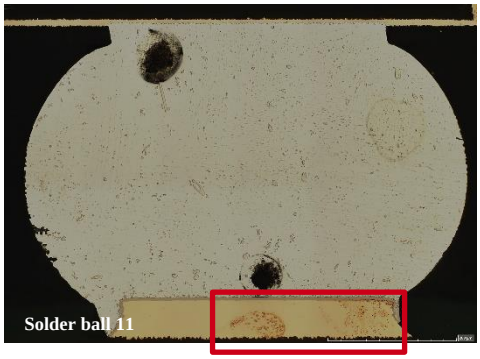


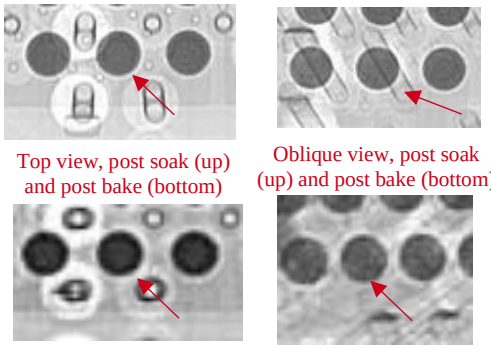
(i) (ii)

Figure 22. (i) Post Soak (ii) Post Bake X-Ray Image Top View



(i)





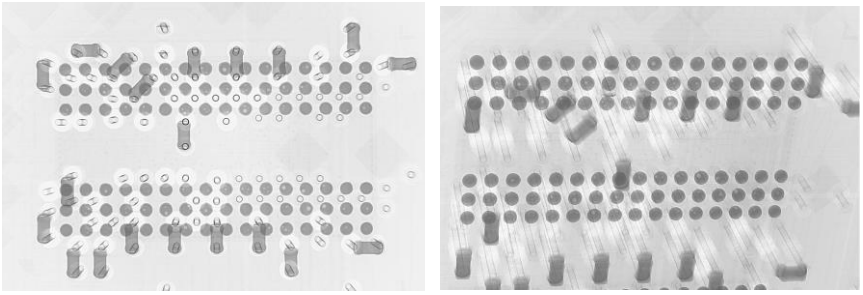
(ii) (iii)

Figure 23. (i) Cross-section overview at 140X magnification of Area 1 (ii) Overview of solder ball 11 (iii) Solder ball 11 in post-soak and post-bake X-Ray Image.

The cross-section analysis in this specimen was cut a little further down the package exposing internal structure of the ASIC/FPGA package as is visible in Figure 23 (i). The

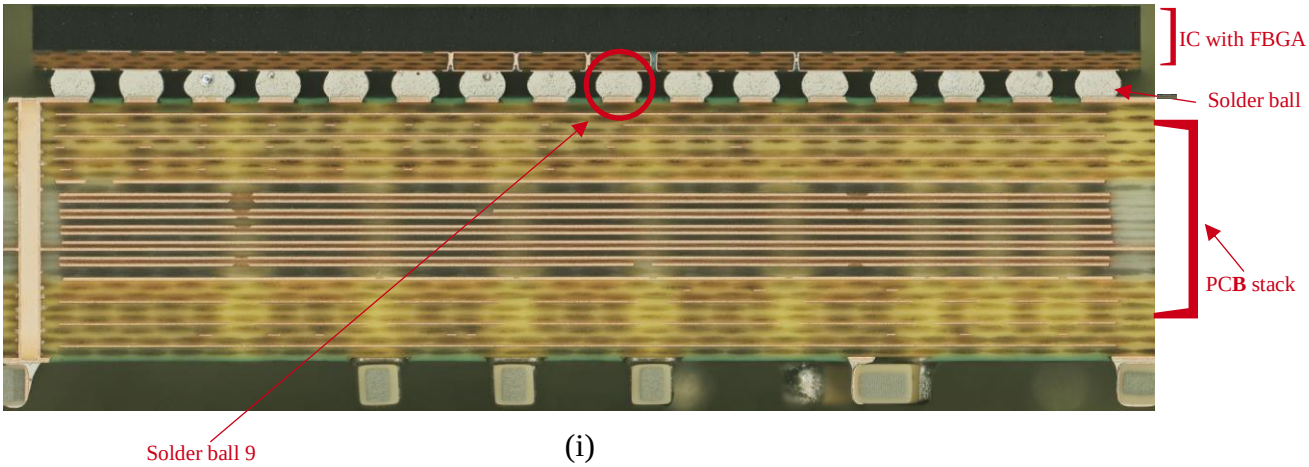
post-soak and post-bake X-Ray analysis in Figure 21 (i) and (ii) were the same. Compared to the reference image, some marks were observed as marked in Figure 23 (ii) on the solder pad which could not be justified as a defect. A lot voiding was present in this sample. The X-Ray Images were referred to find the cause of this, with faint voiding visible only in the oblique post-bake view in Figure 23 (iii). However, since the post soak and post bake oblique view X-Rays were taken at different angles, the voiding might not have been visible at the post-soak X-Ray angle. This is supported by the fact that the voids are not visible in the top view X-Ray images for post soak and bake processes.

3.4.2.4 Area 2- P1



(i) (ii)

Figure 24. Pre-Soak X-Ray Reference Image (i) Top View (ii) Oblique View.



(i)

(ii)

Figure 25. (i) Cross-section overview at 140X magnification of Area 2 (ii) Overview of solder ball 9.

The cross-section and X-Ray analysis in Figure 25. and 24. respectively for Area 2 through the IC with FBGA shows no sign of existing defects. Some voids were present in a few of the solder balls which formed during the reflow soldering process. Different solder ball images will be presented for different test samples to illustrate varied regions of the component. However, all the balls will be examined and verified to ensure that no defects occur during baking.

3.4.2.5 Area 2- P2

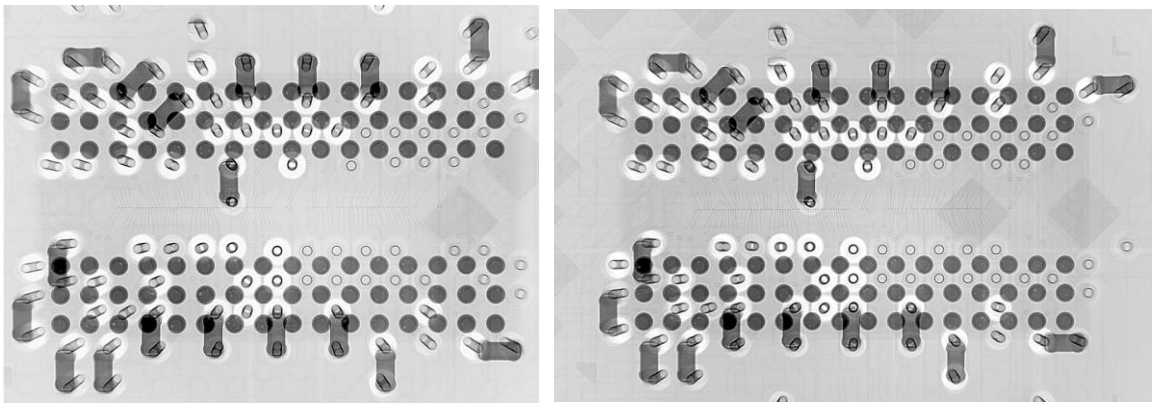
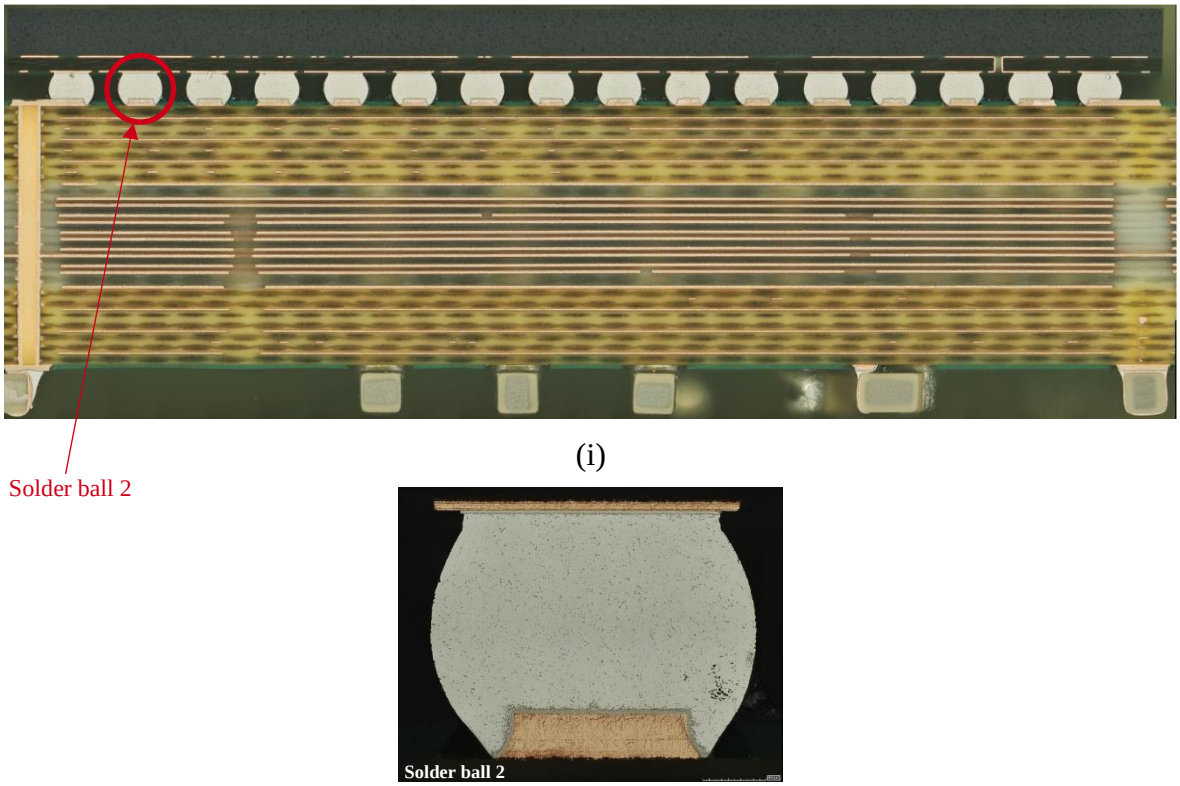


Figure 26. (i) Post Soak (ii) Post Bake X-Ray Image Top View



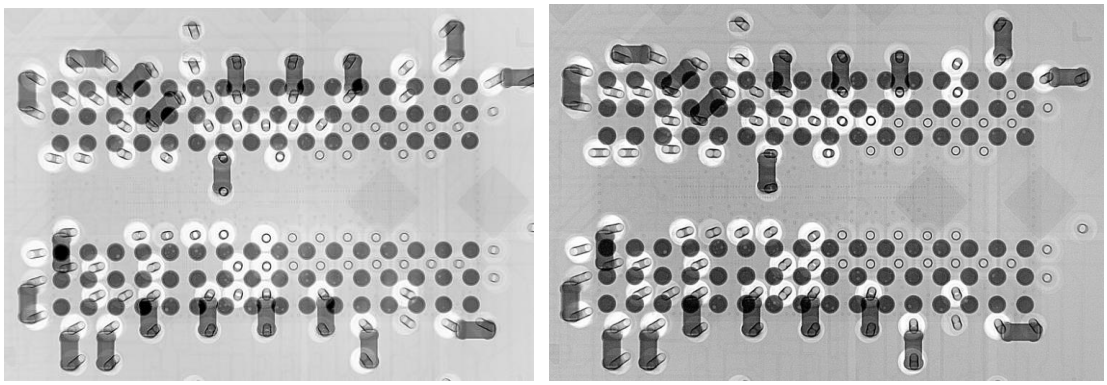
(i)

(ii)

Figure 27. (i) Cross-section overview at 140X magnification of Area 2 (ii) Overview of solder ball 2.

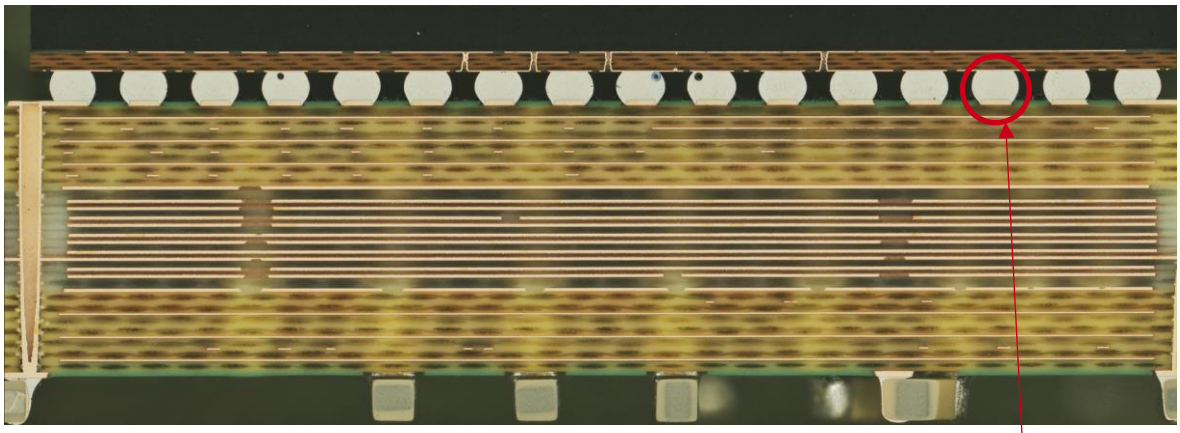
The post-soak and post-bake X-Ray images in Figure 26. show no changes, indicating no damage during the baking process. The cross-section analysis in Figure 27. do not indicate any damage either.

3.4.2.6 Area 2- P4

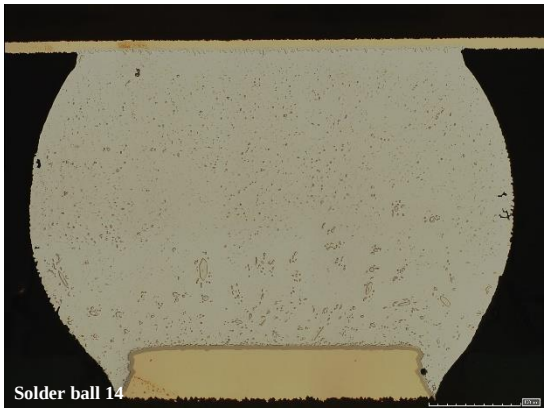


(i) (ii)

Figure 28. (i) Post Soak (ii) Post Bake X-Ray Image Top View



(i)

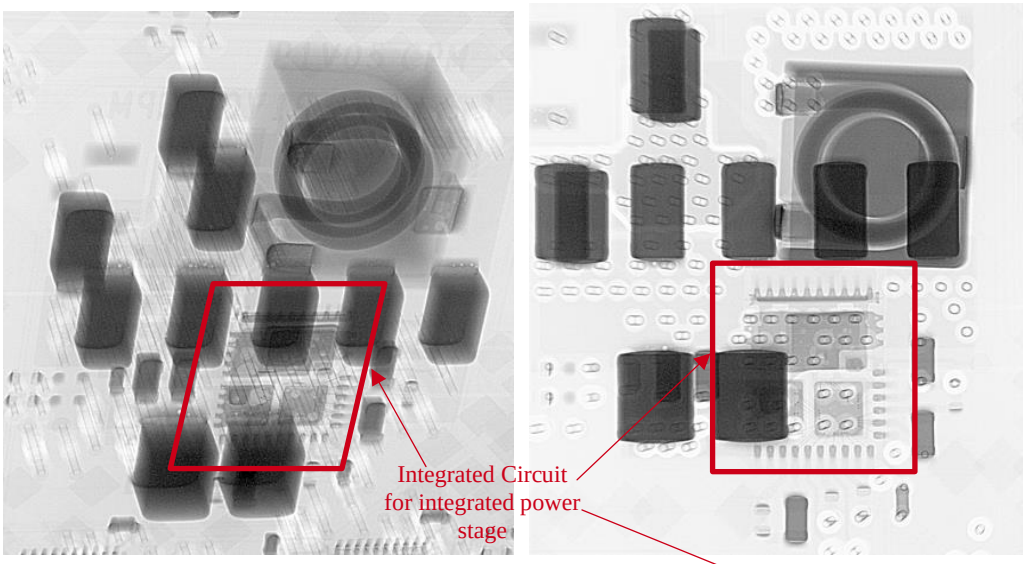


(ii)

Figure 29. (i) Cross-section overview at 140X magnification of Area 2 (ii) Overview of solder ball 14.

The post-soak and post-bake X-Ray images in Figure 28. show no changes, indicating no damage during the baking process. The cross-section analysis in Figure 29. do not indicate any damage either.

3.4.2.7 Area 3- P1



(i) (ii)

Figure 30. Pre-Soak X-Ray Image

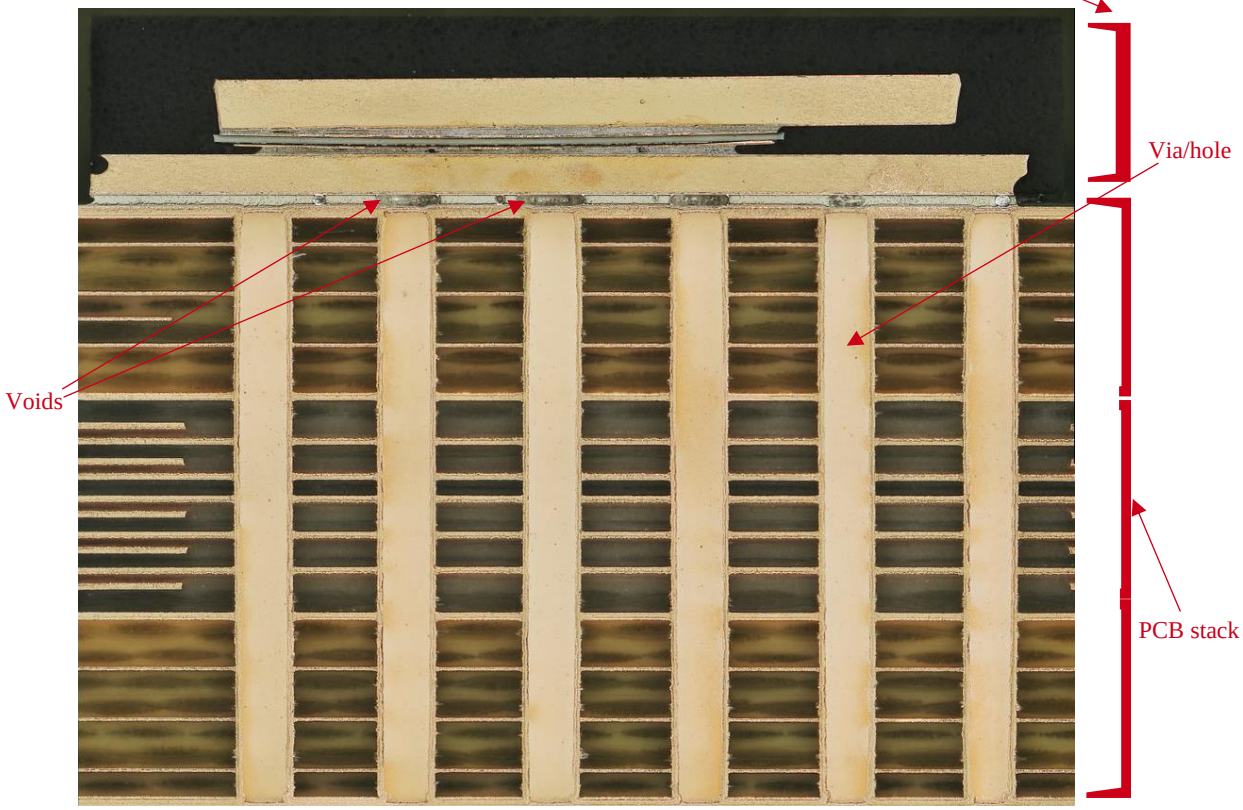


Figure 31. Cross-section overview at 140X magnification of Area 3.

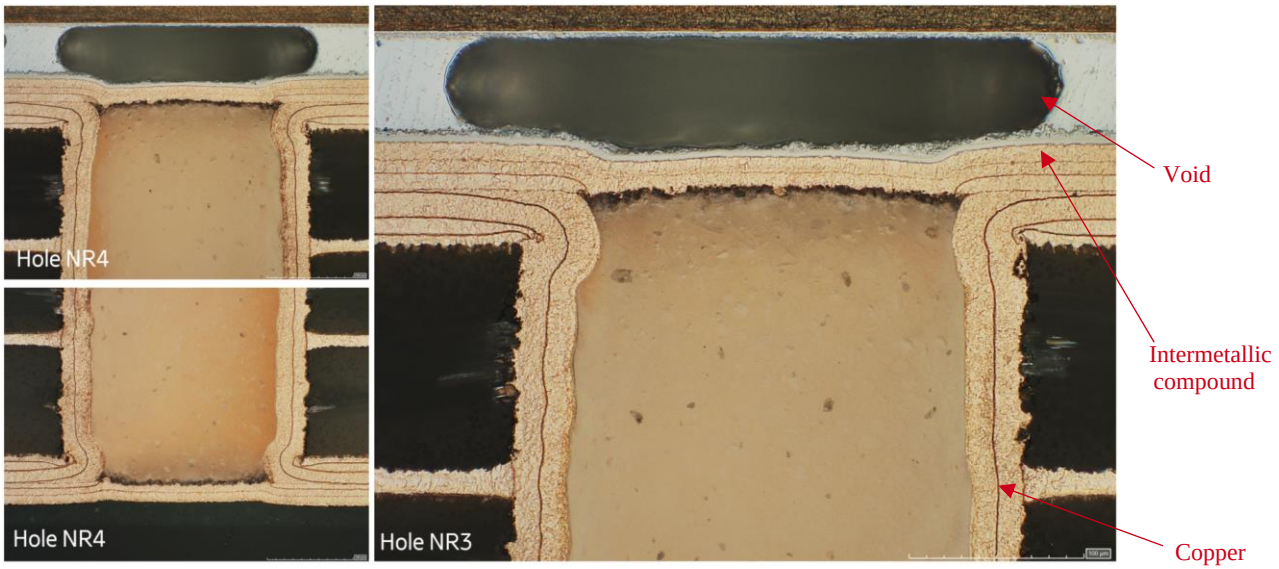
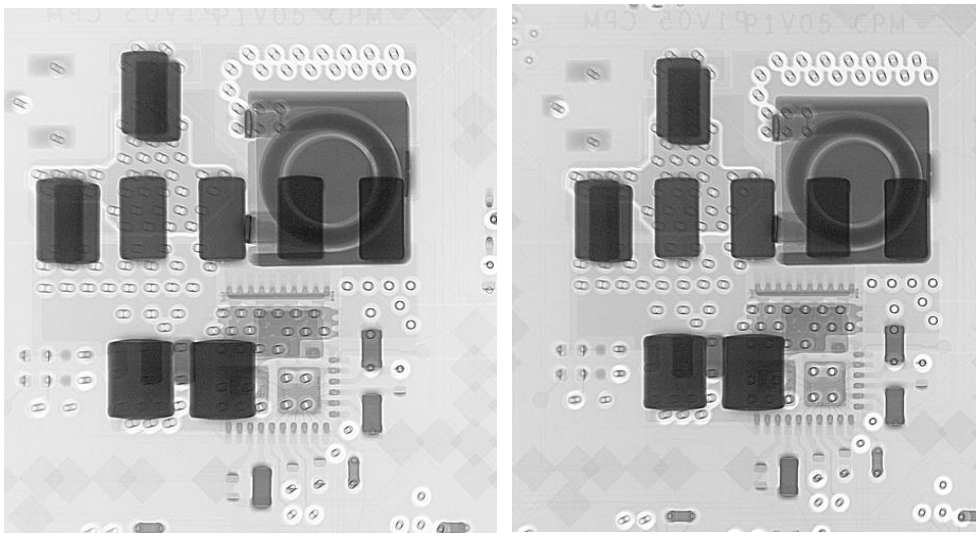


Figure 32. Hole numbers 3 and 4 in cross-section of Area 3.

Figures 31. and 32. illustrates the cross-section analysis of the IC for integrated power stage in a populated component density for Area 3. A number of voids as shown in both the figures is observed which are verified by the X-Ray images of Figure 30. indicating that the voids were formed during the reflow soldering process. This area introduces us to via holes which are metalic lined holes electrically connected to different PCB layers. Between the IC component and PCB, an intermetallic compound (IMC), which if in the correct thickness, is important for good soldering. As indicated in the literature (Lin *et al.*, 2022), the baking process can lead to change in the IMC composition and thickness, which can degrade PCBA quality.

3.4.2.8 Area 3- P2



(i) (ii)

Figure 33. (i) Post Soak (ii) Post Bake X-Ray Image Top View

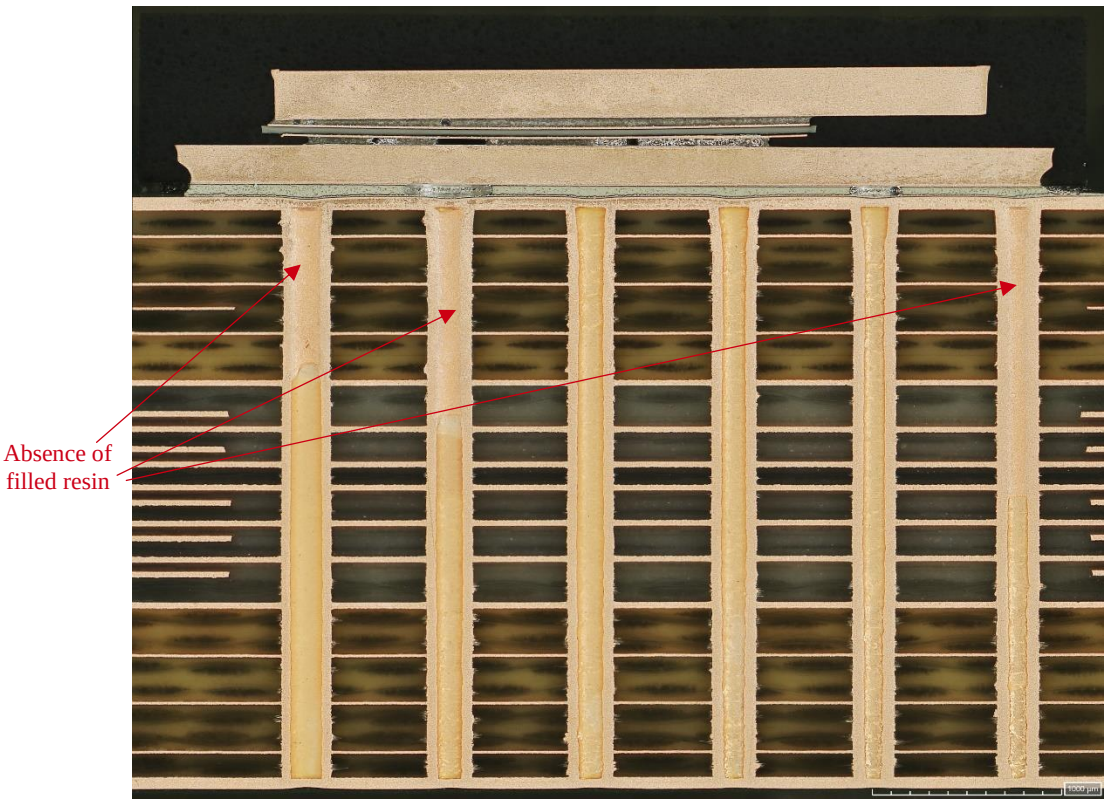


Figure 34. Cross-section overview at 140X magnification of Area 3.

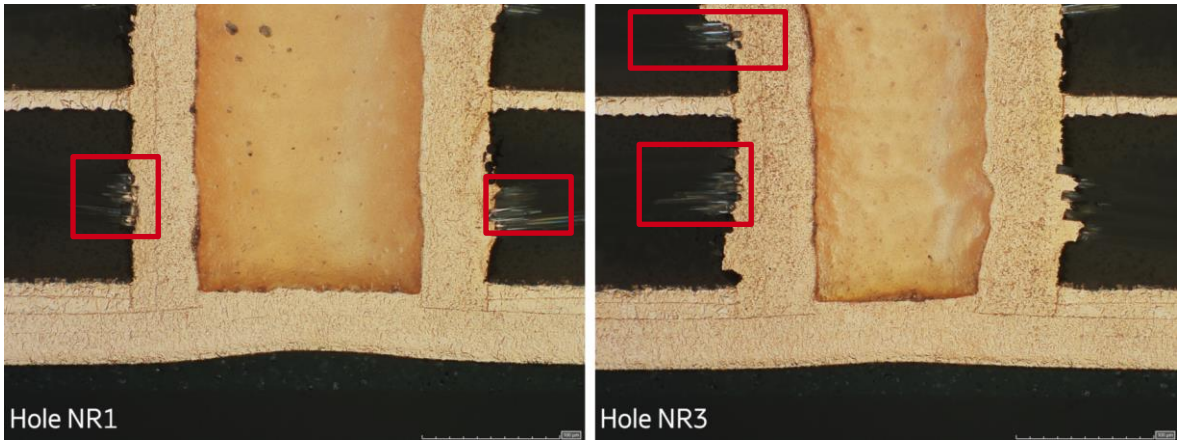
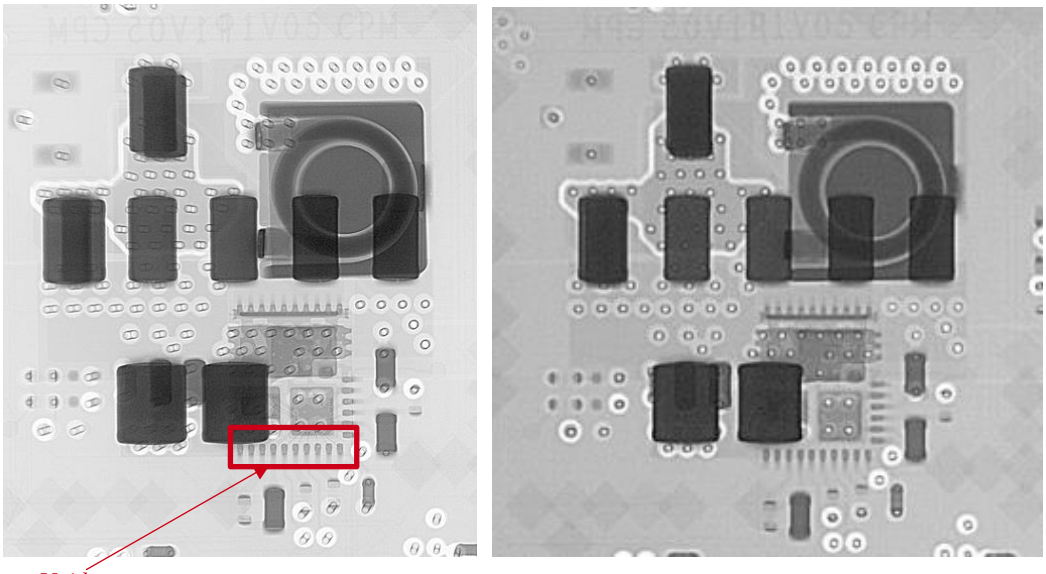


Figure 35. Hole numbers 1 and 3 in cross-section of Area 3.

No changes or physical defects were observed in the X-Ray analysis and cross-section analysis shown in Figures 33., 34. and 35. The IMC thickness remained the same as shown in the reference image in Figures 30. and 31. An absence of filled resin was observed in Figure 34., which could be attributed to overgrinding of the sample during the preparation, leading to a decrease in the hold diameter where the absence of resin is observed. The regions marked in Figure 35. were also caused during the sample preparation during the grinding or polishing step.

3.4.2.9 Area 3- P4



(i) (ii)

Figure 36. (i) Post Soak (ii) Post Bake X-Ray Image Top View

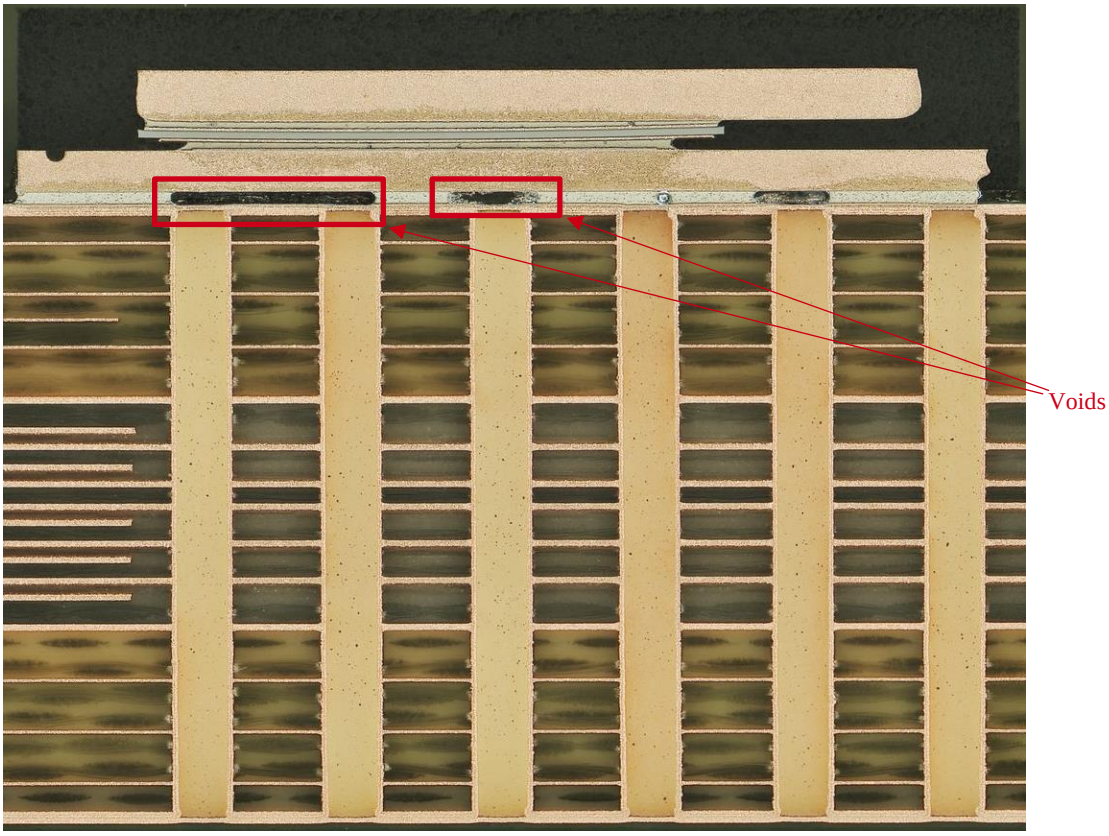


Figure 37. Cross-section overview at 140X magnification of Area 3.

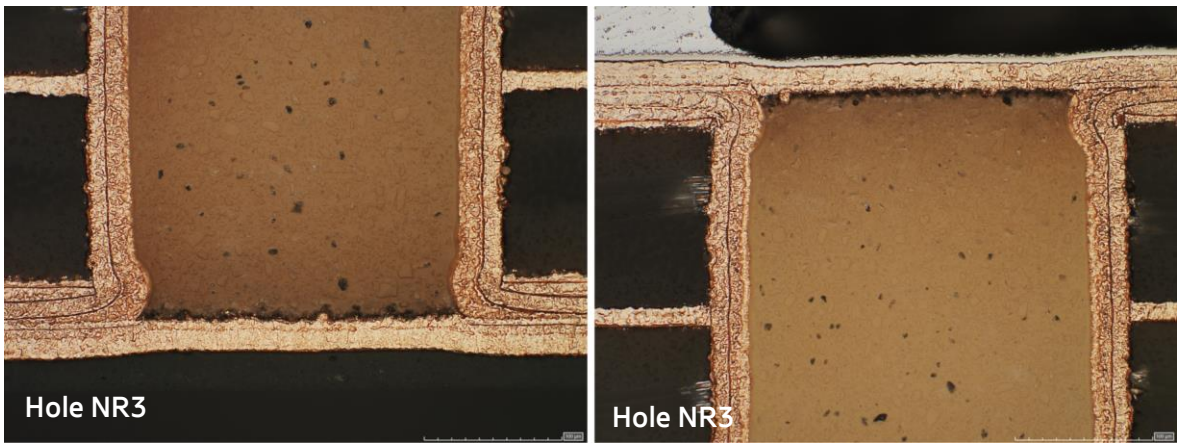
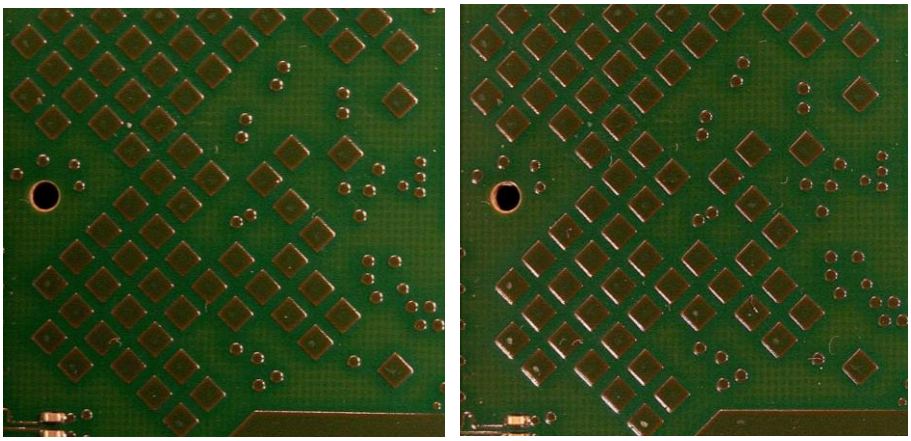


Figure 38. Hole numbers 3 and 4 in cross-section of Area 3.

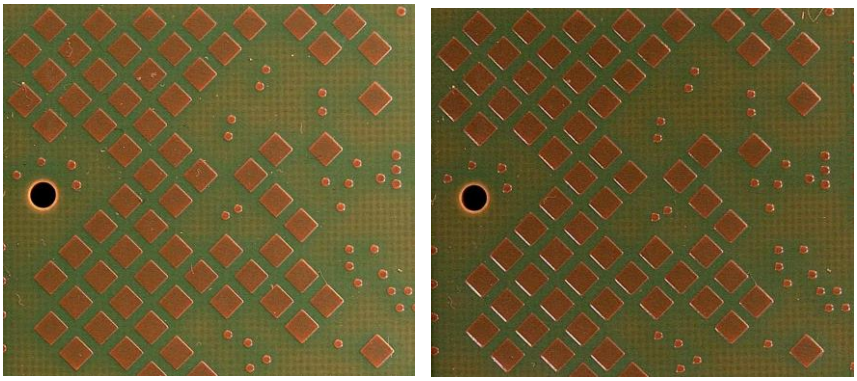
Huge voids are observed in the cross-section in Figure 37. which are cross-referenced with the post-soak X-Ray Image in Figure 36. to confirm they were formed during the reflow process. No physical defects such as increase in IMC thickness, change in X-Ray images, cracking or oxidation of metals is observed.

3.4.3 Surface Visual Inspection



(i) (ii)

Figure 39. (i) Post Soak (ii) Post Bake Visual Image of Surface Area 1 of P2.

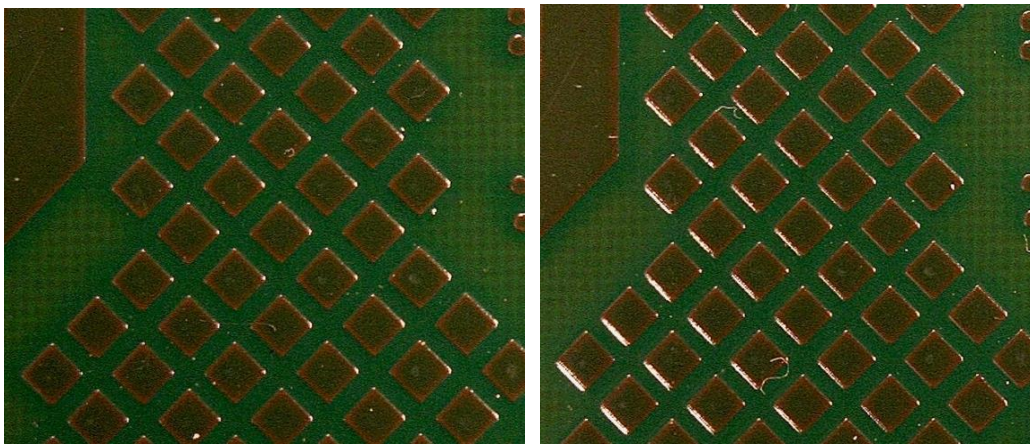


(i) (ii)

Figure 40. (i) Post Soak (ii) Post Bake Visual Image of Surface Area 1 of P4.

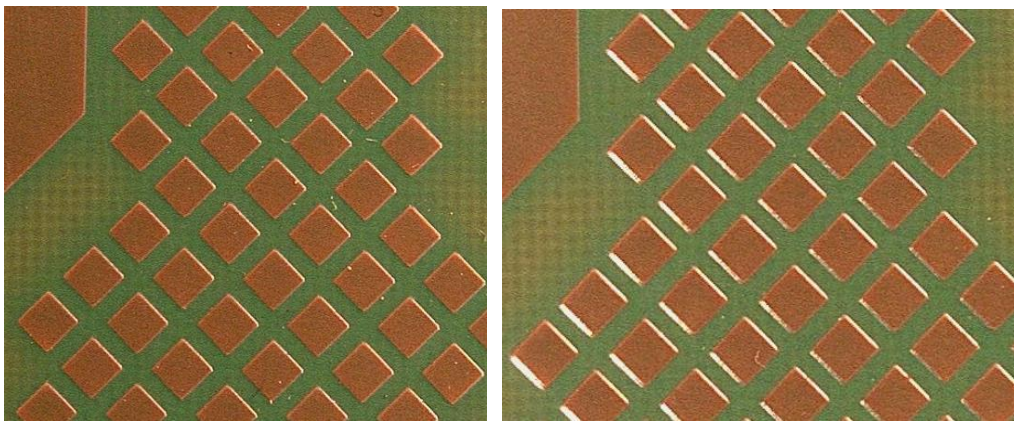
Different sections of the PCBA were analyzed not only for surface inspection but also to check the effect the baking temperatures might have visually on the component surfaces. However, due to company sensitive information, only some parts of the surface visual inspection are shown. No signs of external visual change was observed for the component visual inspection. Area 1 for the surface visual inspection was chosen in a high component density region of the PCBA whereas Area 2 was chosen in a low component density region to observe the effect this might have on our results.

Figures 39. and 40. examine the PCB surface post soak and post bake to investigate any degradation of the PCBs which includes damage or bistering to board finish or solder mask (Sood and Pecht, 2010). The lighting and microscope parameters were kept as same as possible during this investigation. No defects were observed between the two sub parts (i) and (ii) of Figures 39. and 40. Some slight variations such as the brightness observed were seen on the areas marked in the images, but this was due to the reflection of light.



(i) (ii)

Figure 41. (i) Post Soak (ii) Post Bake Visual Image of Surface Area 2 of P2.



(i) (ii)

Figure 42. (i) Post Soak (ii) Post Bake Visual Image of Surface Area 2 of P4.

As seen for Area 1 of the visual inspection discussion, Area 2 did not show any surface damage. The areas marked in Figure 42 (ii) are the reflection of light from the microscope during the inspection.

Images from the P3 and P5 surface visual inspection is in Appendix II. The results are the same as dicussed here, with no signs of degradation visible.

3.5 DISCUSSION

The moisture absorption and desorption curve graphs in Figures and 16. and 17. are consistent with the graphs seen in the literature (TR1 by Company A., 2014) (Ciszewski *et al.*, 2022), with a high rate of moisture gain or loss followed by the saturation point being reached quite soon after a certain period of time due to the dual diffusion model of the system.

Test sample P2 under the 125°C bake only removed ~50% of the absorbed moisture after 4 hours of baking which remained consistent until the end of the experiment at 7,7 hours. Calculating from the trendline, it would take 170,7 hours to remove 80% of the absorbed moisture. The results correspond with the literature (TR1 by Company A., 2014) where only 50% of the moisture was lost after 210 minutes (or 350 minutes) bake period at 125°C. Considering P3 with smashed electrolytic capacitor which shows ~80% of moisture removal at 8 hours as a viable test sample, the data remains consistent with PCB bake-out time for PCBs greater than 2.5mm (Horaud *et al.*, 2003). Further analysis with more samples must be conducted to verify the anomalous behaviour of the two 125°C test samples- In either case, it is evident that the 4-6 hours bake period is not sufficient for efficient moisture removal.

Test samples P4 and P5 at 150°C bake temperatures show similar moisture desorption curves, removing 80% of the moisture at approximately 3,5-4 hours, reducing baking time by 46,13 times and 2,24 times for P2 and P3 samples, with the latter being the expectation at the beginning of the experiment.

No physical defects are seen in the X-Ray and Visual Inspection analysis. IMC thickness increase (IPC/JEDEC J-STD-033D, 2018), oxidation of exposed metals (IPC/JEDEC J-STD-033D, 2018), PCB surface damage and internal cracking were some of the physical defects being analyzed. Only some of the inspection images are shared here due to company sensitive information, hence only the areas where the cross-sectioning was done is shown in the thesis. The entire PCBA was analyzed via both X-Ray and Visual Inspection and no

deformities were observed post baking. Cross-section analysis on three selected areas were also normal, with no defects observed.

The 150°C bake temperature has so far shown to be more effective than the 125°C bake temperaure, both in terms of time as well as the efficiency of moisture removal. As no physical deformities have been spotted, further experiments now need to be conducted focusing on components, PCBs and PCBAs in order to closely examine the physical and functional effects the 150°C baking temperature might have.The bake-out time for 150°C is 3,7 hours. The validity of this time must be verified on other products (PCBAs) while conducting further studies.

SUMMARY

Parameters	Values	
	with 6 hours bake time	with 3,7 hours bake time
PCBAs that can be baked in a day	39	78
Cost per board in terms of energy consumption (euros)	0,11	0,05

Table 7. Cost comparison of a 6 hour and 3,7-hour bake.

To conclude, the experiment verified that the 125°C at 4-6 hours is not sufficient to remove the absorbed moisture. Efficient moisture removal at 125°C for the test PCBAs requires at least 8 hours, if not more. The 150°C baking temperature proves to be a better baking temperature as it not only reduces the baking time by 46,13 times or 2,2 times for P2 and P3 samples respectively while comparing the results that were calculated during the experiment or by 1,62 times if compared to the initial 6 hours baking time. Table 7. illustrates the significant reduction in cost per board in terms of energy consumption for a 6 hour and a 3,7 hour bake respectively.

Physical analysis of the samples using X-Ray, Visual Inspection and Cross-section methods did not show any defects, confirming that it is safe to continue the 150°C study without degrading the PCBA quality.

The next steps of the thesis would be to investigate the impact of the 150°C on various individual unsoldered components, PCBs, and PCBAs in order to clearly study and understand the effect the higher baking temperature might have on the same. Along with the tests conducted in this thesis, some recommended tests for future work would be:

1. Functionality Tests.
2. Reliability Tests such as Thermal Cycling.
3. Scanning Acoustic Microscopy.

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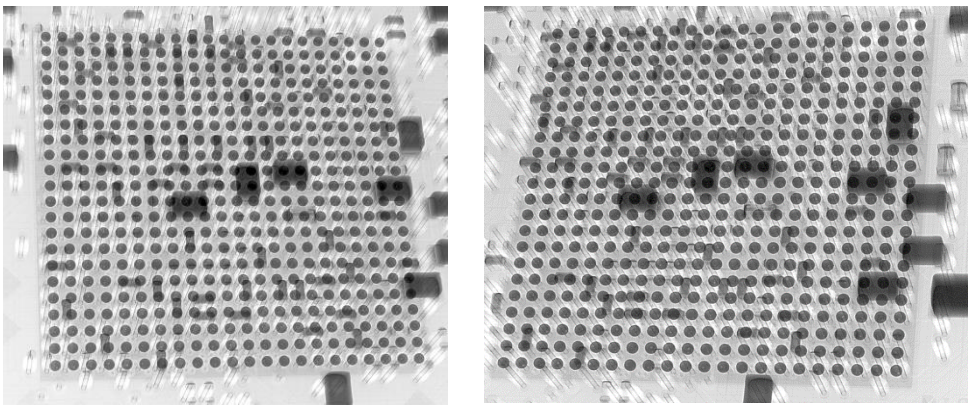
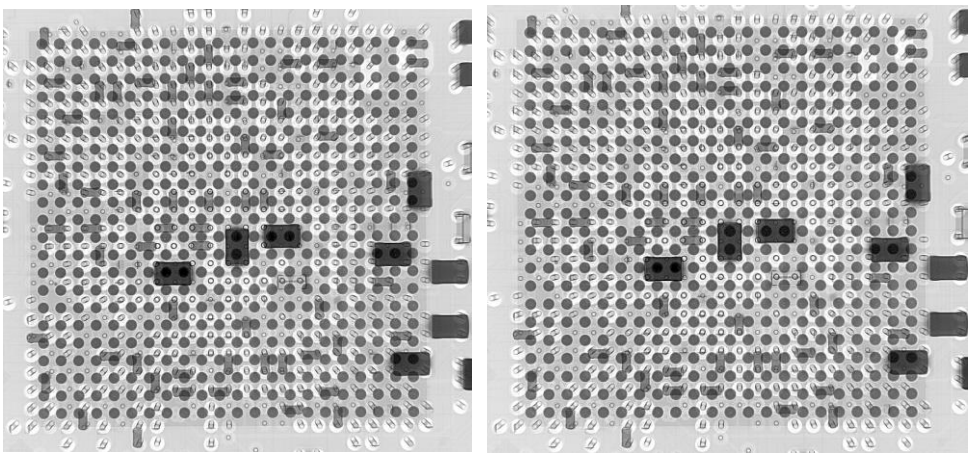
Appendix

1. X-Ray Images for Area 1, Area 2, and Area 3



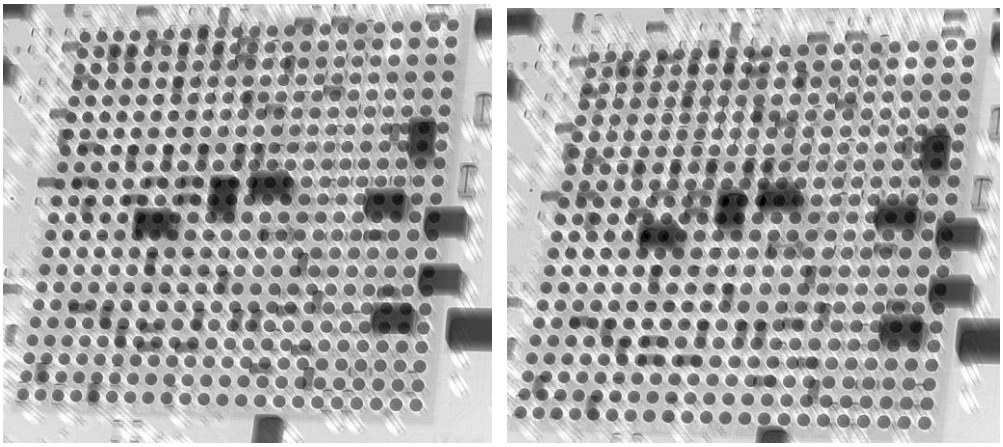
(i) (ii)

Figure 43. P2 Area 1 (i) Post Soak (ii) Post Bake X-Ray Image Angle View.



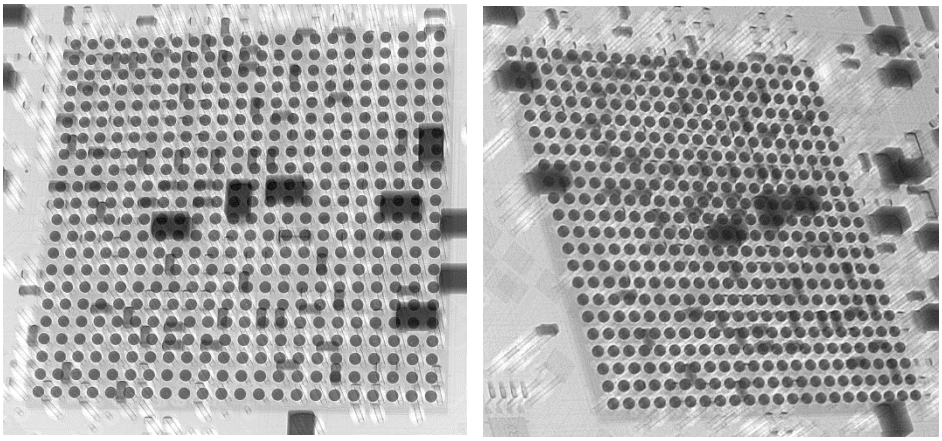
(i) (ii)

Figure 44. P3 Area 1 (i) Post Soak (ii) Post Bake X-Ray Image Top View.



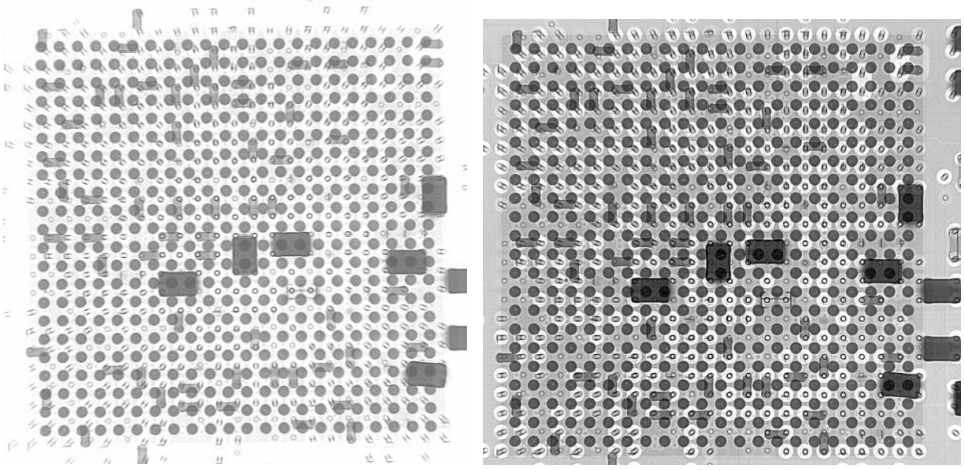
(i) (ii)

Figure 45. P3 Area 1 (i) Post Soak (ii) Post Bake X-Ray Image Angle View.



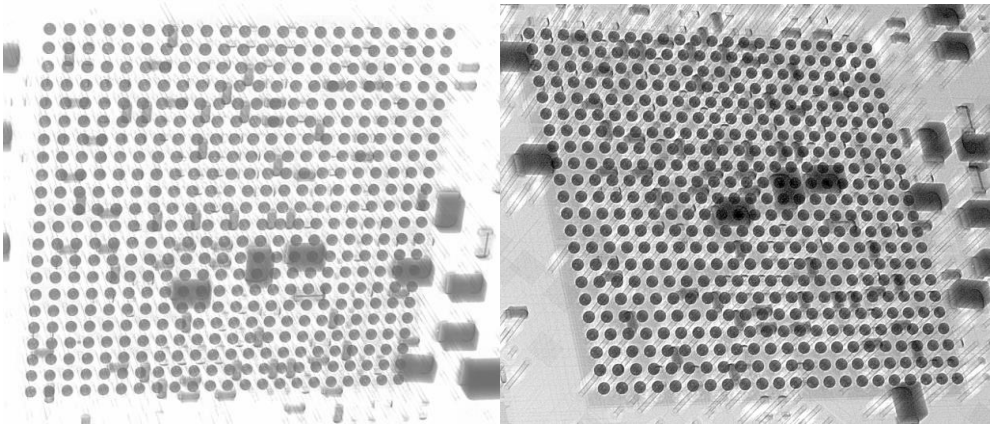
(i) (ii)

Figure 46. P4 Area 1 (i) Post Soak (ii) Post Bake X-Ray Image Angle View



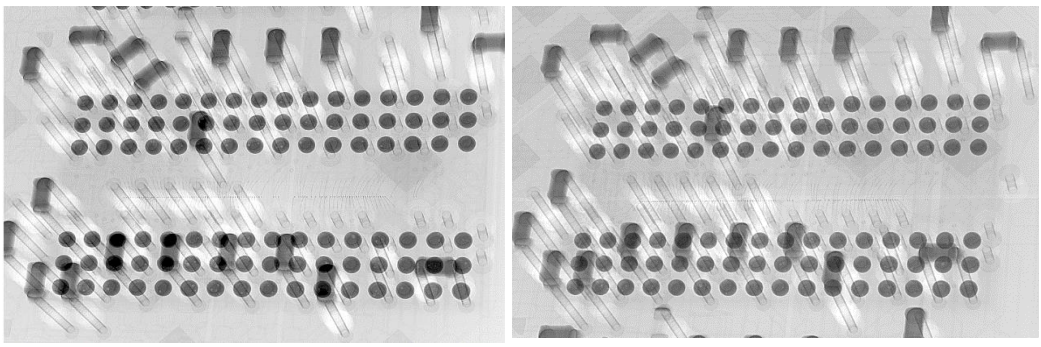
(i) (ii)

Figure 47. P5 Area 1 (i) Post Soak (ii) Post Bake X-Ray Image Top View



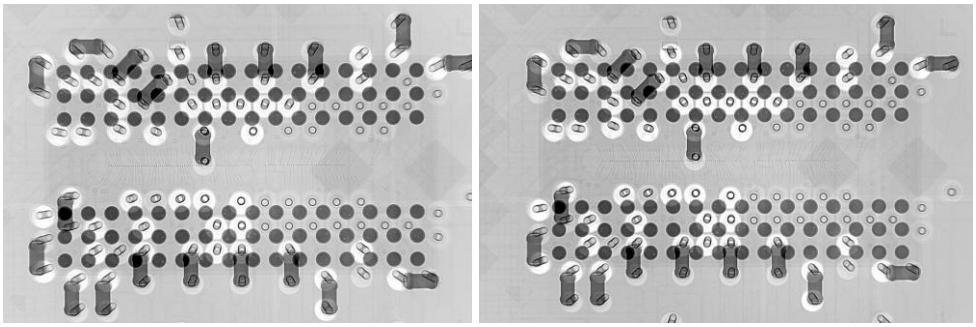
(i) (ii)

Figure 48. P5 Area 1 (i) Post Soak (ii) Post Bake X-Ray Image Angle View



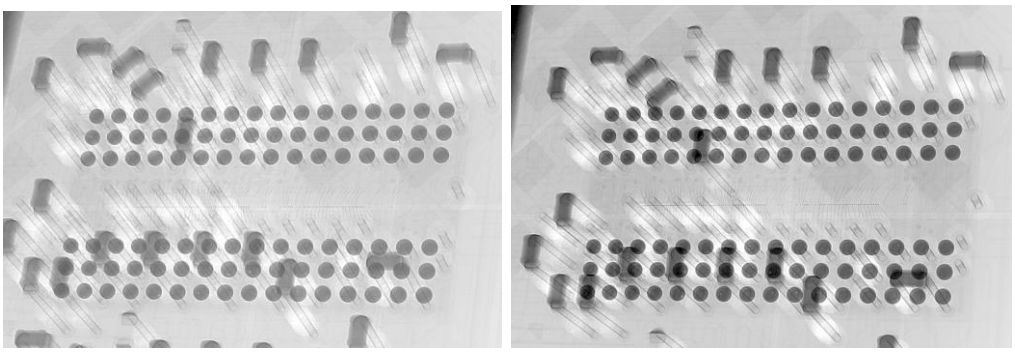
(i) (ii)

Figure 49. P2 Area 2 (i) Post Soak (ii) Post Bake X-Ray Image Angle View



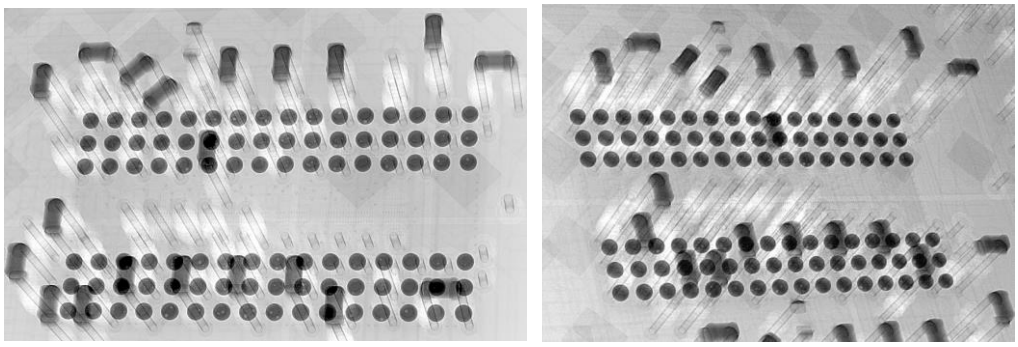
(i) (ii)

Figure 50. P3 Area 2 (i) Post Soak (ii) Post Bake X-Ray Image Top View



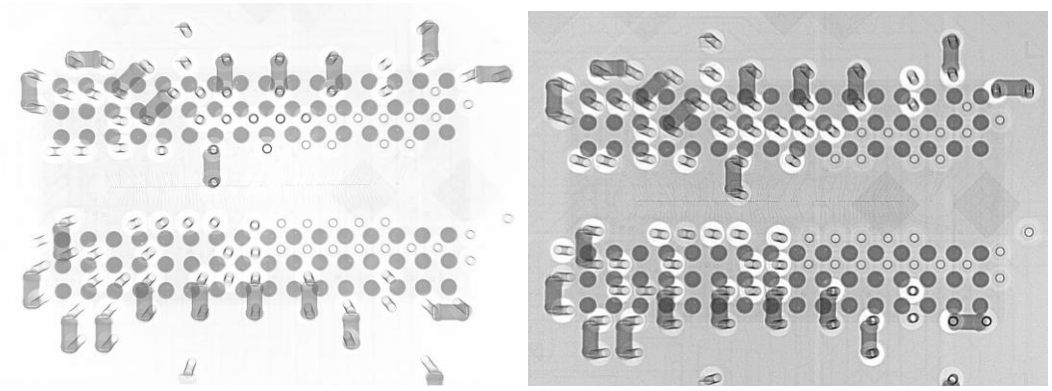
(i) (ii)

Figure 51. P3 Area 2 (i) Post Soak (ii) Post Bake X-Ray Image Angle View



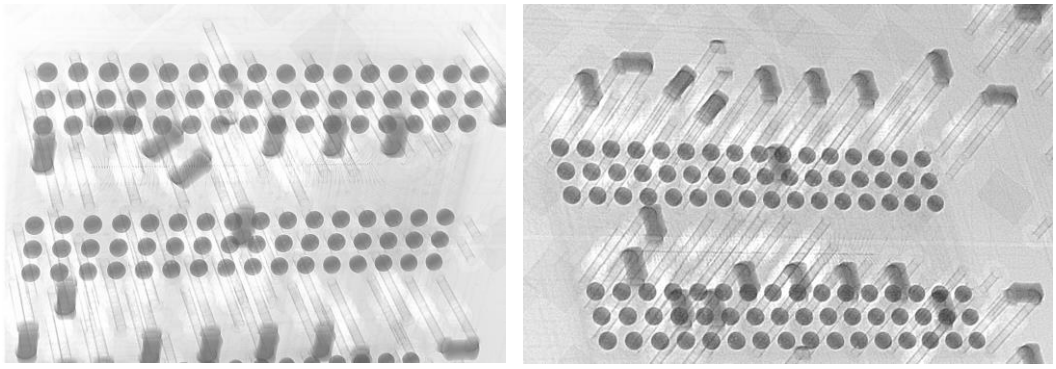
(i) (ii)

Figure 52. P4 Area 2 (i) Post Soak (ii) Post Bake X-Ray Image Angle View



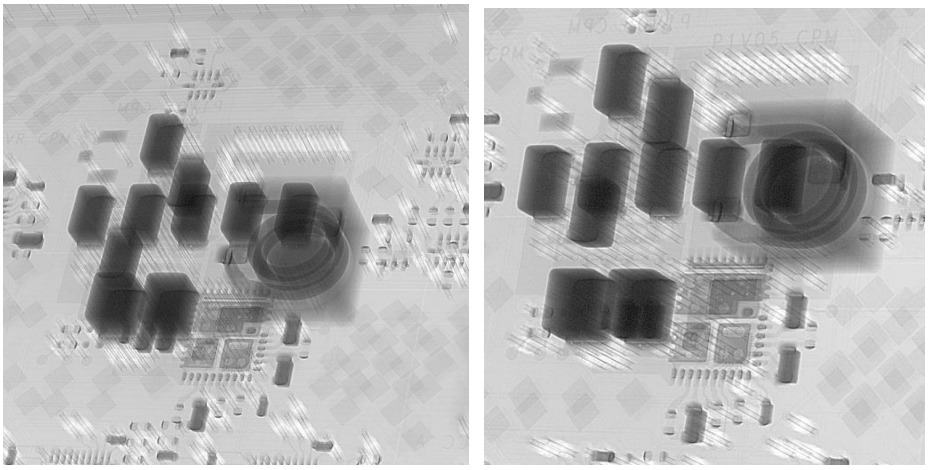
(i) (ii)

Figure 53. P5 Area 2 (i) Post Soak (ii) Post Bake X-Ray Image Top View



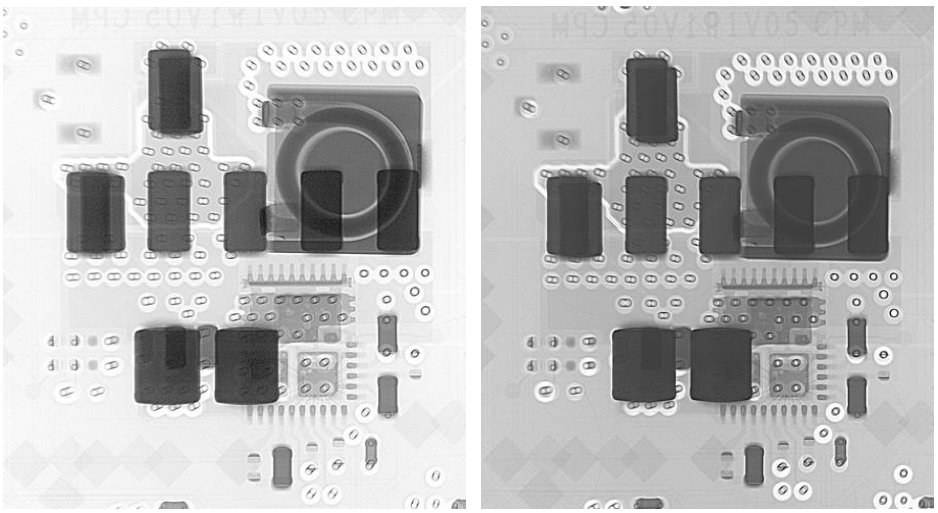
(i) (ii)

Figure 54. P5 Area 2 (i) Post Soak (ii) Post Bake X-Ray Image Angle View



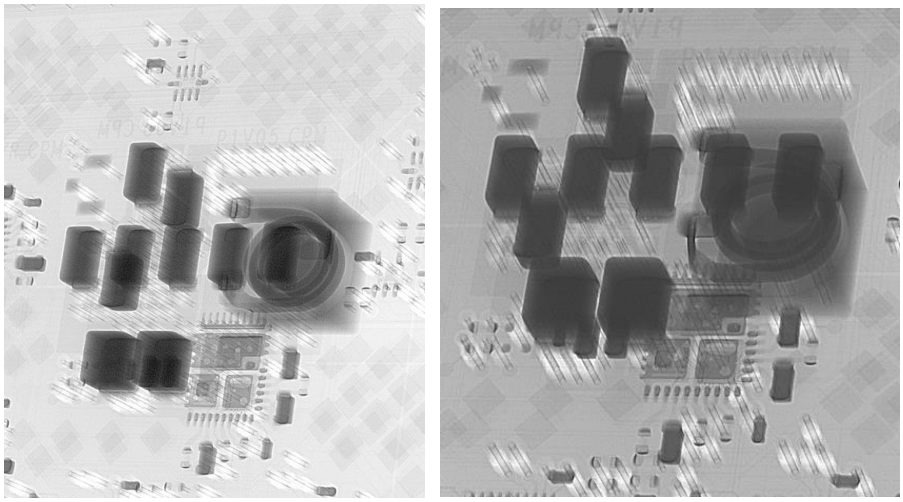
(i) (ii)

Figure 55. P2 Area 3 (i) Post Soak (ii) Post Bake X-Ray Image Angle View



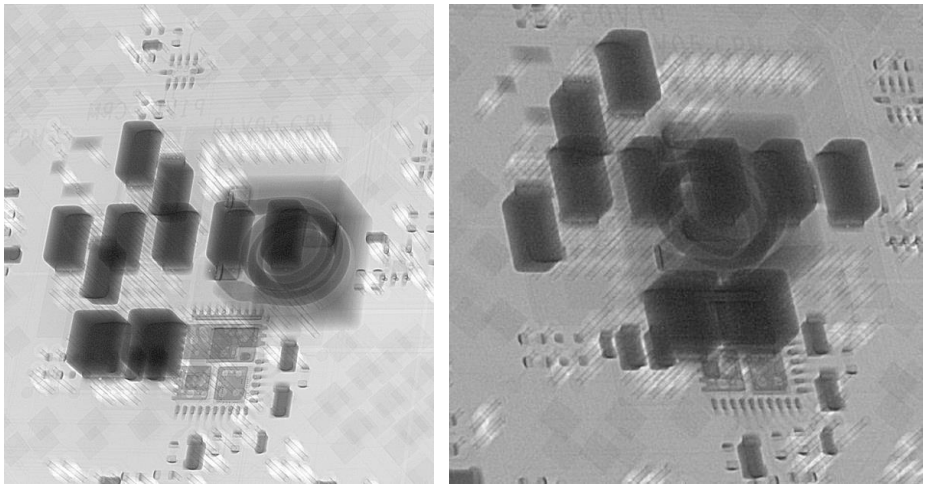
(i) (ii)

Figure 56. P3 Area 3 (i) Post Soak (ii) Post Bake X-Ray Image Top View



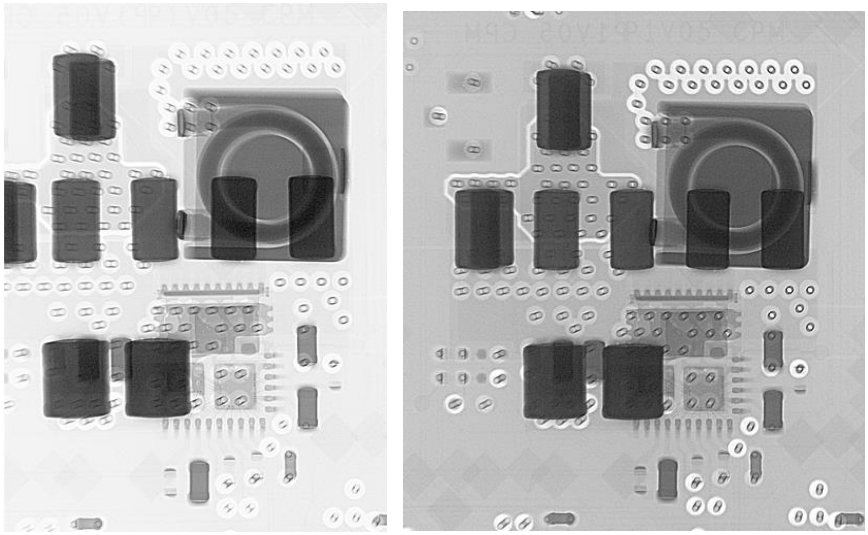
(i) (ii)

Figure 57. P3 Area 3 (i) Post Soak (ii) Post Bake X-Ray Image Angle View



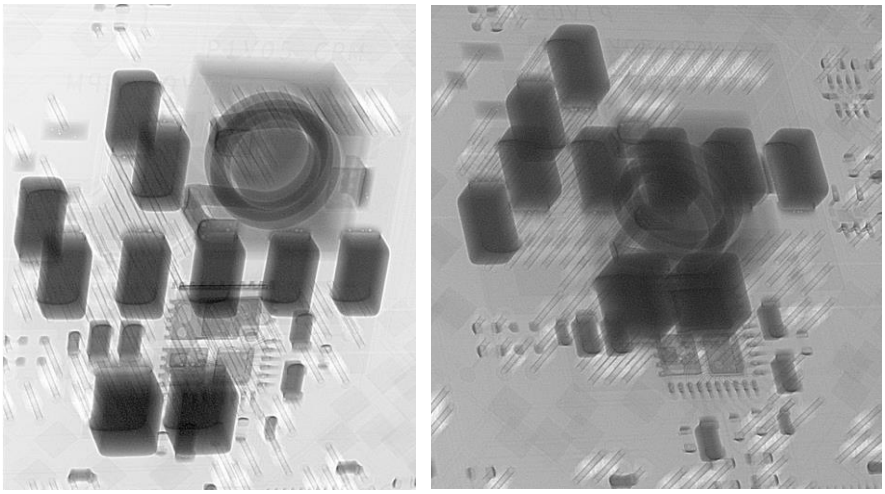
(i) (ii)

Figure 58. P4 Area 3 (i) Post Soak (ii) Post Bake X-Ray Image Angle View



(i) (ii)

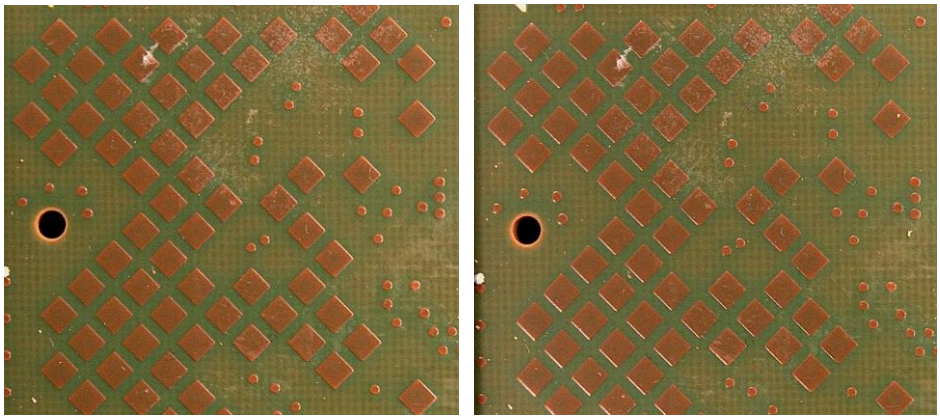
Figure 59. P5 Area 3 (i) Post Soak (ii) Post Bake X-Ray Image Top View



(i) (ii)

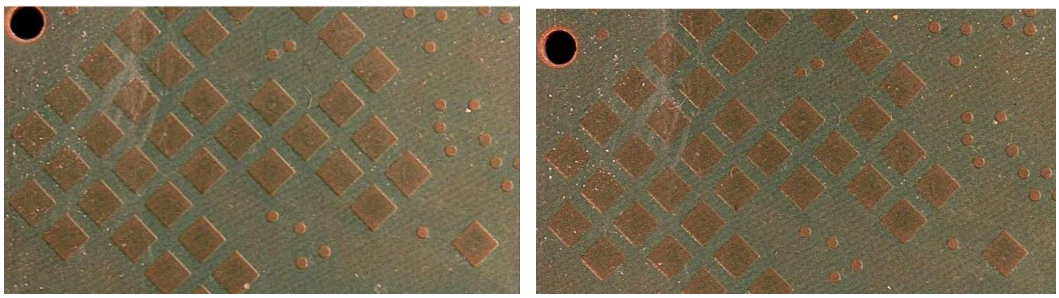
Figure 60. P5 Area 3 (i) Post Soak (ii) Post Bake X-Ray Image Angle View

2. Surface Visual Inspection



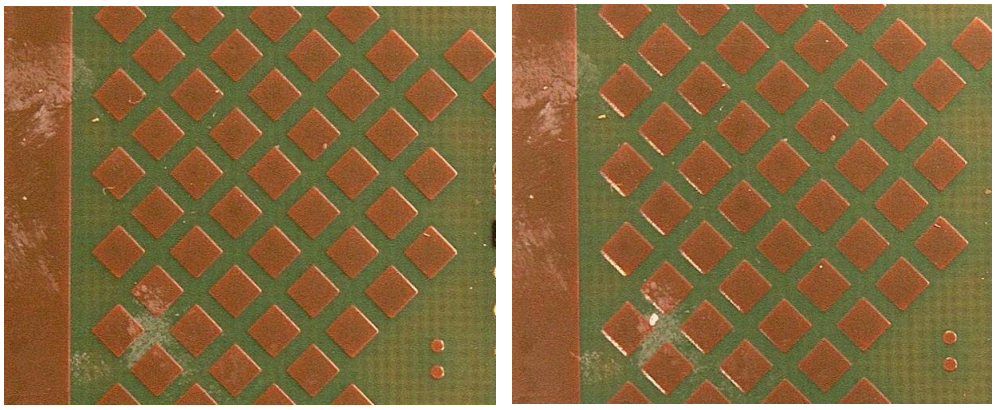
(i) (ii)

Figure 61. (i) Post Soak (ii) Post Bake Visual Image of Surface Area 1 of P3



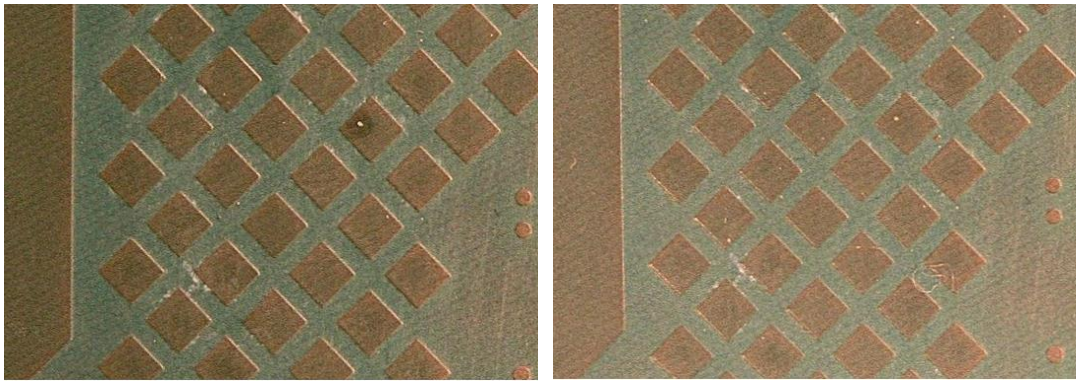
(i) (ii)

Figure 62. (i) Post Soak (ii) Post Bake Visual Image of Surface Area 1 of P5



(i) (ii)

Figure 63. (i) Post Soak (ii) Post Bake Visual Image of Surface Area 2 of P3



(i) (ii)

Figure 64. (i) Post Soak (ii) Post Bake Visual Image of Surface Area 2 of P5

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