A Thesis for the

Master in Telecommunication Engineering

L-Band Solid State Power Amplifier for space applications

by

Walid Hlou Midane

Company Supervisor: Oscar Cuñado

Electrical Engineering Department

Communications Division
SENER Aeroespacial

Academic Supervisor: Pedro de Paco

Departament de Telecomunicació i Enginyeria de Sistemas

Escola Tècnica Superior d'Enginyeria (ETSE)
Universitat Autònoma de Barcelona (UAB)

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El sotasignant, *Pedro de Paco*, Professor de l'Escola Tècnica Superior d'Enginyeria (ETSE) de la Universitat Autònoma de Barcelona (UAB),

CERTIFICA:

Que el projecte presentat en aquesta memòria de Treball Final de Master ha estat realitzat sota la seva direcció per l'alumne *Walid Hlou Midane*.

I, perquè consti a tots els efectes, signa el present certificat.

Bellaterra, *17 de gener del 2022*.

Signatura: *Pedro de Paco*

Resum

Aquesta tesi es va fer al departament d'enginyeria elèctrica de la Divisió de Comunicacions de l'empresa SENER Aeroespacial. A causa de la demanda creixent d'Amplificadors de Potència d'Estat Sòlid (SSPA) de GaN per a aplicacions espacials, l'empresa va promoure un projecte intern R+D per superar els reptes clau de la implementació de la tecnologia GaN en amplificadors de potència qualificats per a l'espai, combinant l'experiència multidisciplinar de SENER Aeroespacial que inclou el disseny de RF, el disseny mecànic-tèrmic, la fabricació i la qualitat.

Entre totes les disciplines esmentades, aquesta tesi se centra especialment en la part corresponent al disseny i caracterització RF dels SSPAs. Es proposa el disseny i desenvolupament complet del producte des d'un transistor MMIC de potència GaN en format die fins a la fabricació dels prototips representatius. La validació de les proves dels prototips es realitza a la Sala Neta utilitzant instruments de RF, i posteriorment, a partir dels resultats inicials, es fa la correlació de les mesures i la simulació per corregir i validar els models de simulació considerats inicialment.

Resumen

Esta tesis se realizó en el departamento de ingeniería eléctrica de la División de Comunicaciones de la empresa SENER Aeroespacial. Debido a la creciente demanda de Amplificadores de Potencia de Estado Sólido (SSPA) de GaN para aplicaciones espaciales, la empresa promovió un proyecto interno I+D para superar los retos clave de la implementación de la tecnología GaN en amplificadores de potencia calificados para el espacio, combinando la experiencia multidisciplinar de SENER Aeroespacial que incluye el diseño de RF, el diseño mecánico-térmico, la fabricación y la calidad.

Entre todas las disciplinas citadas, esta tesis se centra especialmente en la parte correspondiente al diseño y caracterización RF de los SSPAs. Se propone el diseño y desarrollo completo del producto desde un transistor MMIC de potencia GaN en formato die hasta la fabricación de los prototipos representativos. La validación de las pruebas de los prototipos se realiza en la Sala Limpia utilizando instrumentos de RF, y posteriormente, a partir de los resultados iniciales, se realiza la correlación de la medidas y la simulación para corregir y validar los modelos de simulación considerados inicialmente.

Abstract

This thesis was carried out in the electrical engineering department at the Communications Division of the company SENER Aeroespacial. Due to the increasing demand of GaN Solid State Power Amplifiers (SSPA) for space applications, an internal R+D project was promoted by the company to overcome the key challanges to implement GaN technology in space-qualified power amplifiers by combining the SENER Aeroespacial multi-disciplinary expertise including, RF design, mechanical-thermal design, manufacturing and quality.

Among all the cited disciplines, this thesis is focused particularly on the part corresponding to the SSPA RF design and characterization. Complete product design and development is proposed from a GaN power MMIC transistor in die format to the manufacturing of the representative prototypes. Test validation of the prototypes is performed in the Clean Room using RF instruments, then, based on the initial results, correlation of the measurement and simulation is performed to correct and validate the simulation models considered initially.

Acknowledgements

This thesis is a result of my final Master year devoted to research and study, thus, I would like to acknowledge all the people who have been part of this journey with me.

I would like to express my gratitude to Oscar Cuñado. Thank you for giving me the opportunity to work on this amazing project and for giving me advice and support. I would like also to express my gratitude to Ivan Baro and Mohamed Chaibi for their support and instructions about RF design and measurements techniques.

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Acronyms

- **ACPR -** Adjacent Channel Power Ratio
- **ADS -** Advanced Design System
- **ATC -** American Technical Ceramics
- **DC -** Direct Current
- **DPD -** Digital Predistortion
- **DUT -** Device Under Test
- **ESR -** Effective Serial Resistance
- **EVM -** Error Vector Magnitude
- **FET -** Field Effect Transistor
- **GaAs -** Gallium Arsenide
- **GaN -** Gallium Nitrite
- **GSM -** Global Systems for Mobile Communications
- **HD -** Harmonic Distortion
- **HEMT -** High Electron Mobility Transistor
- **IMD -** Intermodulation Distortion
- **IMN -** Input Matching Network

- **LNA -** Low Noise Amplifier
- **MMIC -** Microwave Monolithic Integrated Circuit
- **OMN -** Output Matching Network
- **PA -** Power Amplifier
- **PAE -** Power Added Efficiency
- **PCB -** Printed Circuit Board
- **RF -** Radio Frequency
- **RFFE -** Radio Frequency Front-End
- **SRF -** Self-Resonance Frequency
- **THD -** Total Harmonic Distortion
- **TL -** Transmission line
- **WLAN -** Wireless Local Area Network
- **GMSK -** Gaussian Minimum Shift Keying

Chapter 1

Introduction

This Masther Thesis has been carried out at the Communications Division of the company SENER Aeroespacial as a result of a collaboration project with the Autonomous University of Barcelona (UAB), Engineering School.

1.1 Context

A satellite is a complex system with a huge number of electronic components working in harsh environmental conditions. Thus, robustness and reliability are key characteristics that have to be guarantee to assure the overall success of the mission. Moreover, due to the high cost per kilogram of the payload, space and weight of every subsystems have to be reduced as much as possible to maximize the cost-benefits tradeoff of the mission. Therefore, the design of space borne microwave components is usually the result of a compromise among several aspects. In this contest, the power amplifier represents the most critical block since it heavy affects mass,dc power consumption, thermal and mechanical management [6] [7].

1.1.1 Satellite Amplifier Technology

As with nearly all communications systems, satellite transponders include transmit and receive modules. In the traditional architecture, the uplink signal is passed through a low noise amplifier

to a frequency converter, then to the transmit module. Amplifying the signal to the required output level is typically the role of a Travelling Wave Tube (TWT) high-precision amplifiers. This complexity drives the high price of TWTs and increases the risk of failure. TWT amplifiers also require very high bias voltage, usually thousands of volts, generated by a high voltage supply, which is expensive realization processes to avoid multipaction and corona effects. Moreover, they need large volume and heaviness especially in the lower frequency bands such as L and S [6] [8].

A solid-state solution offers a more robust, compact option. A GaN power amplifier uses standard IC manufacturing processes, producing small devices only a few millimeters on each side. Instead of using artisan-style manufacturing, GaN devices are produced using automated semiconductor processes at low-cost. While a single GaN device is unable to deliver the same output power as a TWT amplifier, multiple GaN devices can be combined in a small package. As an added benefit, GaN amplifiers only require bias voltages of 28 to 50 V. Given the differences between GaN and TWT amplifiers, GaN is particularly attractive for applications sensitive to size, weight and cost, as well as those that require less transmit power[8].

1.1.2 Challanges of GaN technology in space

While GaN amplifiers offer compelling benefits for satellite applications, specific challenges must be overcome to successfully use GaN in space-qualified hardware. The first and most obvious challenge arises from the high power density of the device. While TWT amplifiers also require a complex cooling system, a GaN IC generates significant heat in a very small space. For example, a 30 W solid-state GaN amplifier can easily draw 2.5 A biased at 28 V, resulting in 40 W power dissipation in an area not much larger than 10 mm^2. If the thermal transfer is inadequate to cool the device, the elevated junction temperature will lower output power and possibly even causing catastrophic failure [8].

This raises the second challenge: reliability. The hig power dissipation common with GaN devices results in a significant temperature rise in the active region; as the temperature in the device increases, the reliability of the amplifier degrades. The temperature rise depends on the

power dissipation in the GaN and the thermal resistance between the device and the case, both difficult to model and control. Power dissipation depends on multiple factors such as RF drive and load impedance, and the thermal resistance is highly dependent on minor variations in the assembly process [7] [8].

Even under ideal circumstances, where the temperature is carefully controlled, high RF drive levels can cause permanent damage to the GaN lattice, resulting in degraded output power. Compared to GaAs, GaN is a much newer technology, and the lack of heritage raises reliability concerns. While this applies to all applications using GaN, operating in a space environment requires an extra focus to assure reliability. Since repair is generally not an option, a single device failure can be extremely expensive [7] [8].

This discussion highlights several key challenges to implement GaN technology in space-qualified power amplifiers. Addressing these requires multi-disciplinary expertise including, RF design, mechanical design, manufacturing and quality. Chapter 3 discuss possible approaches to managing these challenges when the Solid State Power Amplifier (SSPA) design is considered.

1.2 Motivations

SENER Aeroespacial promotes internal research and development tasks to increase its technologic knowledge (heritage) according to the demands of the space satellite systems. Hence, an R+D internal project has been promoted to address the increasing new demands for GaN SSPAs, especially, based on the Galileo Second Generation navigational satellite system needs.

Galileo navigational satellite system determine location on or near the Earth using radio signals broadcast by a constellation of satellites in different orbits around the planet. These satellites operate primarily at L-Band (1-2GHz) and on power generated by solar panels. Thus, every watt of electrical power is truly valuable, bringing a great need for Power amplifiers to be highly efficient. High efficiency is achieved at the expense of linearity and finding a trade-off between the two is one of the most challaging aspects of the power amplifiers design since it depends on the application of the whole system. In this case, the development of new modulation techniques is increasing the linearity required by PAs used for navigation systems

[1].

From a PA-designer's point of view, it is challenging to achieve high efficiency and high linearity simultaneously. However, on one hand , it is well known that a PA, in general, can operate efficiently only at a high level of device saturation, which is also the extremely non-linear region. On the other hand, for linear amplification, the transistor needs to be unsaturated and most of the dc input power is sacrificed in generating head room for a good linearity. Such scarified dc power transforms to heat, which can bring reliability issues and degrade the performance of the power amplifier itself as highlighted in previous section.

Therefore, an excellent approach for the space navigational application considered would be designing a high efficiency power amplifier at the expense of linearity, then, resolve the conflict of linearity-efficiency by means of using a linearizer to operate linearly as shown in figure 1.1. Note that linearization techniques are out of scope of this project.

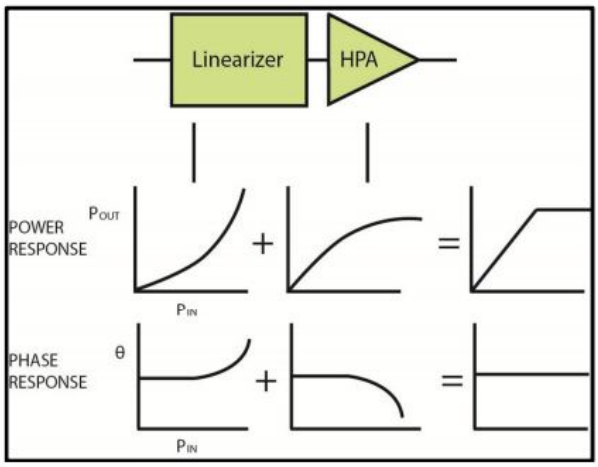


Figure 1.1: Linearizer [1]

1.3 Scope and objectives

Due to the increasing demand for high efficiency power amplifiers for space applications as highlighted in the previous section, the scope of this thesis is to explore with the nature of SSPAs at L-bands matched in terms of high efficiency, output power and high harmonic rejection while matched to 50 Ω input and output impedance. Such SSPA is intended for satellite navigation

systems and Mobile Satellite Services (MSS) covered by Galileo Second Generation program.

Taking into account the project scope defined, the following objectives are set and must be satisfied during the development of the project:

1. Research and study of the state of the art of the power amplifier design, where the efficiency enhancement techniques and PA operation classes must be investigated.
2. Learning about the layout design rules and the manufacturing processes as well as the understanding of the electrical models provided by the foundry of each element of the circuit.
3. 3D and lumped modeling of the parts of the circuit whose electrical models is unavailable using RF/microwave techniques and CAD tools.
4. Reliability Analysis according to ESA and NASA standards.
5. Preparation of manufacturing data (layouts, list of material, etc)
6. Test validation of first prototype in Clean Room using RF instruments.
7. Correlation of measurements and simulation.
8. Preparation of documentation, including design and validation.

In order to achieve these objectives, the Master Thesis here developed describes the procedure from the applied theory to the final SSPA design, prototyping and testing according to an internal specifications defined base on the Galileo Satellite Navigation System requirements and the state of the art of the possible competitors (very important for R+D projects).

1.4 Thesis Outline

This thesis is organized in six chapters. The first chapter introduces the project context, motivation, scope/objectives and outline of this thesis. Chapter 2 to 5 contain the main contributions of this research as following:

- **Chapter 2** provides state of the art of power amplifiers. Several aspects such as PAs figures of merit, efficiency enhancements mechanism and PA classes are detailed. Given a general overview of PA fundamentals, definitions and different operation classes.

- **Chapter 3** Describes and presents an SSPA topology design using microstrip technology. General aspects related to the simulations models, microstrip technology and schematic/momentum simulation are detailed in this chapter. Furthermore, given that the thermal management is a critical issue in GaN technology, an general overview about mechanical and thermal management is presented in this chpater.

- Chapter 4 provides a functional test of the designed SSPA. Small and large signal measurement test bench and results are detailed in this chapter.

- **Chapter 6** provides simulation and measurement results correlation where 3D models of the different parts of the circuit are created to be able to extract the electrical models.

And finally, the document is concluded in chapter 6, summarizing the main results and contributions presented.

Chapter 2

State-of-the art

This chapter aims to provide the state of the art of power amplifiers. Several aspects such as PAs figure of merit, efficiency enhancement techniques and PA classes are detailed.

2.1 PA figures of merit

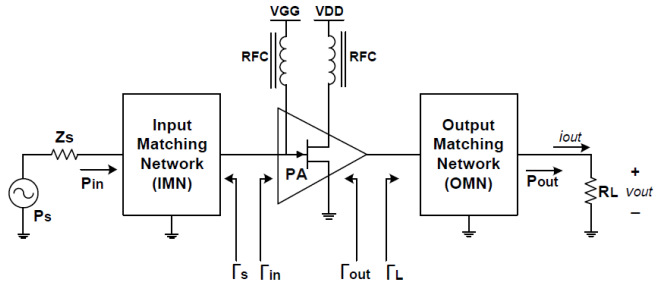
Important considerations for RF and microwave power amplifiers are efficiency, power, gain, stability,harmonic distortion, intermodulation distortion, Adjacent Channel Power Ratio (ACPR), Error Vector Magnitude (EVM) and thermal effects.

2.1.1 Power

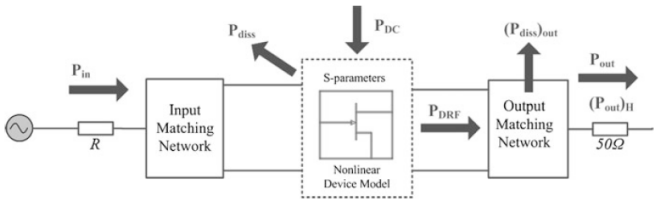
Output/Delivered Power

One of the most important characteristics of PA is the ability to deliver a certain amount of power into the load. The 50 ohms load represents the Zin of the next stage of the RF system. There are two ways to measure the power, instantaneous power and average power, which are defined as follows:

$$P_{ins} = p(t) = v(t) \cdot i(t) \tag{2.1}$$



(a) Basic power amplifier diagram [2]



(b) Power flow depiction in a power amplifier [3]

Figure 2.1: PA diagrams

$$P_{avg} = \frac{1}{T}\int_0^T p(t)dt \tag{2.2}$$

Amplifier's output power is considered to have a linear to its input power until P_{1dB}(1dB-compression point), which is the power at which output power drops 1dB below its linear expected value (figure 2.2). In addition to P_{1dB}, P_{3dB} is defined as the power where the output power drops 3dB below its linear expected value. P_{1dB} is used in literature as the point where amplifier starts to be nonlinear, while P_{3dB} is commonly used in practice to define final stage power in high power amplifiers[2].

DC Power (P_{DC})

It refers to the power used from the power supply in all DC terminals (drain and gate). DC power is calculated as follows:

$$P_{DC}(W) = V_{drain} \cdot I_{drain} + V_{gate} \cdot I_{gate} \tag{2.3}$$

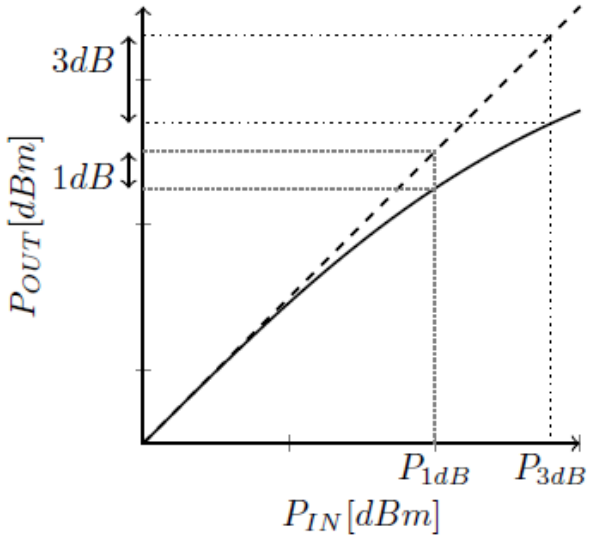


Figure 2.2: P_{1dB} and P_{3dB} definition [2]

For the PA in this thesis, Gate DC power can be neglected, since Gate current is intended to be too small($I_{gate} \approx 0$).

Input Power

Is the RF power RF power available at the source (or the power delivered by the Previous stage of the RF system), it's used to drive the amplifier.

2.1.2 Gain

In lineal scale, Gain is the ratio between output and input power, whereas is their difference in dB scale:

$$G(dB) = 10log_{10}(\frac{P_{out}(W)}{P_{in}(W)}) = P_{out}(dBW) - P_{in}(dBW) \tag{2.4}$$

Gain is constant at low input power and as the input power is increased, the amplifier starts compressing and gain starts decreasing. Hence two gain calculations can be made, and they are used differently.

Small signal gain

It corresponds to $|S21|^2$ parameter, and it is often used in signal amplifiers such as Low Noise Amplifiers (LNA) and receiving sections. As it is measured under very low input power (deep back-off) the behavior is linear, and hence cannot be extrapolated for high power amplifiers where compression effects and non-linear parasitics play a key role in amplifier's behavior [2].

Large signal gain

is obtained with the PA working at higher power, where nonlinear effects such as non-linear capacitances and amplifier saturation take place. At low power levels, the gain is linear, but as power increases the gain decreases. Due to the non-linear behavior, simulation of G_p should be done by Harmonic Balance [2].

2.1.3 Efficiency

The power amplifier is usually the primary consumer of DC power in most hand-held wireless devices, so amplifier efficiency is an important consideration. One measure of amplifier efficiency is the ratio of RF output power to DC input power:

$$\eta = \frac{Pout}{Pdc} \tag{2.5}$$

This quantity is sometimes referred to as drain efficiency (or collector efficiency). One drawback of this definition is that it does not account for the RF power delivered at the input to the amplifier. Since most power amplifiers have relatively low gains, the efficiency of (2.5) tends to overrate the actual efficiency. A better measure that includes the effect of input power is the power added efficiency, defined as:

$$PAE = \frac{Pout - Pin}{Pdc} = (1 - \frac{1}{G})\frac{Pout}{Pdc} = (1 - \frac{1}{G})\eta \tag{2.6}$$

Where G is the power gain of the amplifier. Power amplifiers are often designed to provide the best efficiency, even if this means that the resulting gain is less than the maximum possible.

2.1.4 Stability

Stability is one of the most important factors in the PA that should be considered from the early stage of the design in order to avoid undesired oscillations that would result in signal distortion among others. Oscillations can happen at low frecuency or at RF frequency. Low frequency stability is controlled by the bias network (gate and drain) design. However, RF stability depends on the circuit design,for example, in the circuit of figure 2.1a, oscillation is possible if either the input or output port impedance has a negative real part; this would then imply that $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$. Because γ_{in} and Γ_{out} depend on the source and load matching networks, the stability of the amplifier depends on Γ_S and Γ_L as presented by the matching networks. Thus, we define two types of stability:

- Unconditional stability: The network is unconditionally stable if $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ for all passive source and load impedances (i.e., $|\Gamma_S| < 1$ and $|\Gamma_L| < 1$).
- Conditional stability: The network is conditionally stable if $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ only for a certain range of passive source and load impedances. This case is also referred to as potentially unstable.

Note that the stability condition of an amplifier circuit is usually frequency dependent since the input and output matching networks generally depend on frequency. It is therefore possible for an amplifier to be stable at its design frequency but unstable at other frequencies.

Test for Unconditional Stability

The stability circles discussed in [9] can be used to determine regions for Γ_S and Γ_L where the amplifier circuit will be conditionally stable, but simpler tests can be used to determine unconditional stability. One of these is the **Rollet's condition**, defined as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{2.7}$$

The device will be unconditionally stable if the 2.7 condition is satisfied in conjunction to the auxiliary condition defined as:

$$\Delta = |S_{11}S_{22}| - |S_{12}S_{21}| < 1 \tag{2.8}$$

These two conditions are necessary and sufficient for unconditional stability, and are easily evaluated. If the device scattering parameters do not satisfy the K - Δ test, the device is not unconditionally stable, and stability circles must be used to determine if there are values of Γ_S and Γ_L for which the device will be conditionally stable. Also recall that we must have $|S_{11}| < 1$ and $|S_{22}| < 1$ if the device is to be unconditionally stable, whereas in unilateral amplifiers (S12 = 0) fulfilling only $|S_{11}| < 1$ and $|S_{22}| < 1$ signify unconditional stability.

Note that K-factor can not be used directly to compare the relative stability of two or more devices, however, a new criterion has been proposed that combines the scattering parameters in a test involving only a single parameter,μ, defined as:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}| + |S_{12}S_{21}|} > 1 \tag{2.9}$$

Thus, if $\mu > 1$, the device is unconditionally stable. In addition, it can be said that larger values of μ imply greater stability. More details about μ factor can be found in [9].

2.1.5 Intermodulation and Harmonic Distortion

A power amplifier is a nonlinear system that generates harmonic components in addition to the frequency corresponding to the excitation signal. Intermodulation and harmonic distortions quantify the impact of distortion associated with the harmonic components and provide a measure of linearity performance of a power amplifier.

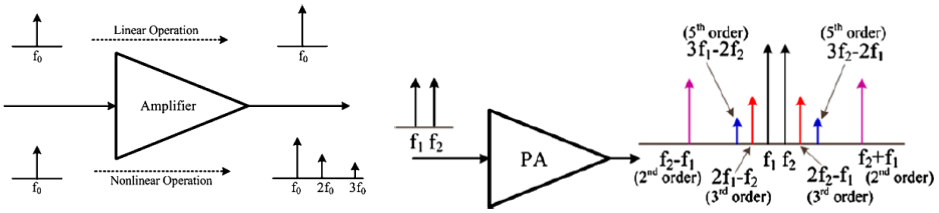
Harmonic distortion is measured when the amplifier is excited with a single-tone test signal

and harmonic distortion components are generated at the output, as depicted in figure 2.3a. Usually the second and third harmonics carry most of the energy; therefore, the harmonic distortions are defined for these harmonic components.

$$HD_{2,dBc} = 10log_{10}(\frac{P_{out}(2f_0)}{P_{out}(f_0)} \tag{2.10}$$

$$HD_{3,dBc} = 10log_{10}(\frac{P_{out}(3f_0)}{P_{out}(f_0)} \tag{2.11}$$

The harmonic distortions are expressed in dBc relative to the fundamental frequency power. The power level of the harmonics changes with the input power; therefore, the corresponding harmonic distortion figures in dBc change as well.



(a) Harmonic distortion (b) Intermodulation distortion

Figure 2.3: Intermodulation and harmonic distortion [3]

Another harmonic distortion term that is very commonly used is called total harmonic distortion (THD), It includes all the harmonics distortion components in one figure of merit:

$$THD_{dBc} = 10log_{10}(\frac{\sum_{n=2}^{\infty} P_{out}(nf_0)}{P_{out}(f_0)}) \tag{2.12}$$

Intermodulation distortion (IMD) is more realistic for the actual wireless communication system. It is the result of two or more signals interacting in a power amplifier to produce additional unwanted signals. For example, the additional unwanted signals (intermodulation products) for two input signals occur at the sum and difference of integer multiples of the original frequencies given by Eq. (2.13) and as depicted in figure 2.3b.

$$IMD_{products} = mf_1 \pm nf_2 \tag{2.13}$$

where m and n are integers and define the order of intermodulation products as a sum of m+n.

As shownin figure 2.3b, 3rd components($2f_1$-$f2$ and $2f_2$-fa) are the most relevant, as they are very close to the fundamental components, therefore, cannot be easily filtered. Higher order intermodulation products generally do not affect the performance of PAs significantly, as these components either possess very low amplitudes or are far from the fundamental components [3].

Eq. (2.14) corresponds to third-order intermodulation product (IMD3) when the fundamental components f_1 and f_2 are very close.

$$IMD_{3,dBc} = 10log_{10}(\frac{P_{out}(2f_2 - f_1)}{P_{out}(f_2)} \approx 10log_{10}(\frac{P_{out}(2f_1 - f_2)}{P_{out}(f_1)} \tag{2.14}$$

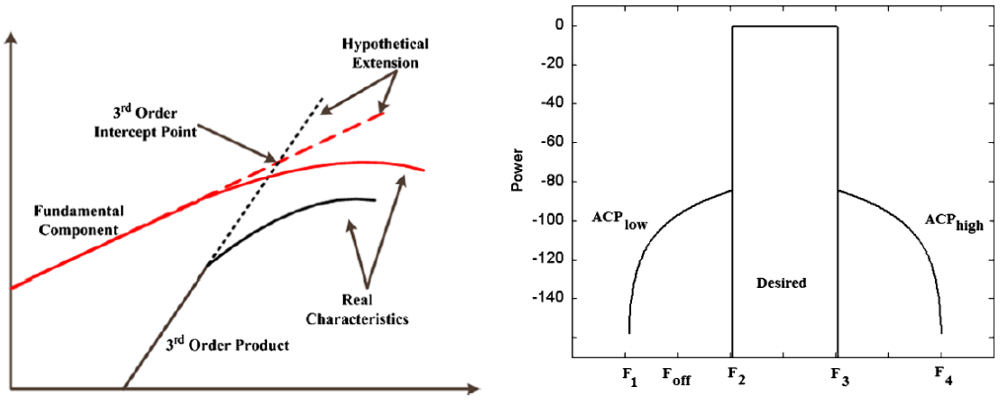
Another metric to describe the linearity performance of a power amplifier is known as the intercept point. For third-order products, it is known as the third-order intercept point (IP3), as shown in figure 2.4a.

It is important to understand that THD, IMD3, and IP3 are good metrics for describing the performance of PAs exhibiting weak memory effects [3]. However, these are insufficient for the situations when the PAs exhibit strong nonlinearity.

2.1.6 Adjacent Channel Power Ratio

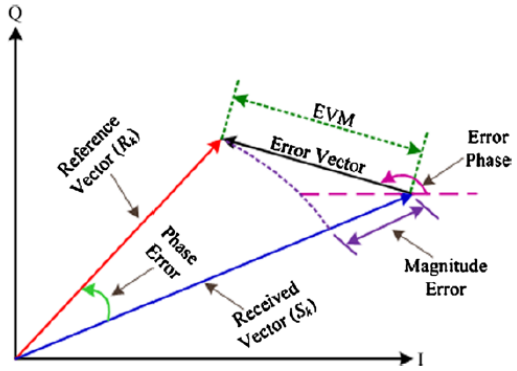
For amplifiers exhibiting strong nonlinearity or for digitally modulated excitations, adjacent channel power ratio (ACPR) is more relevant considering that harmonic distortion is applicable for single tone excitation and the usefulness of intermodulation distortion is limited to excitations with specified number of tones (usually 2).

ACPR describes the level of spectral regrowth and is often expressed in dB below the main



(a) Representation of third-order intercepts point

(b) Ideal representation of main and adjacent channel power spectra and their respective frequency band definitions



(c) Illustration of error vector magnitude (EVM) and its components

Figure 2.4: Representation of the figures of merit when a the PA exhibits strong nonlinearity [3]

carrier power (dBc) as depicted in Fig. 1.8 and is expressed as the ratio of the power leaking into the adjacent channel to the power in the main channel given by[3]:

$$ACPR_{dBc} = 10log_{10}(\frac{\int_{F_2}^{F_3} P(F)dF}{\int_{F_1}^{F_2} P(F)dF}) \tag{2.15}$$

Figure 2.4b The plot shows a representative power spectrum showing the driving signal (between frequencies F_2 and F_3) and the adjacent channel power (ACP) resulting from third order interactions only. In an ideal system, ACPR should be as high as possible as it conveys that the leakage from the main channel to the side channel is low.

2.1.7 Error Vector Magnitude

According to 3GPP standards, EVM is a measure of the difference between the reference waveform and the measured waveform [3]. The difference is called error vector, illustrated in figure 2.4c, and the EVM, usually mentioned in percentage, is defined as the square root of the ratio of the mean error vector power to the mean reference power expressed as:

$$EVM_{RMS} = \sqrt{\frac{\sum_{k\epsilon K} |S_k - R_k|^2}{\sum_{k\epsilon K} |R_k|^2}} \tag{2.16}$$

where S_k is the received (measured) vector, R_k is the reference symbol vector, and K is the total number of symbols.

The ACPR provides information about the out-of-band distortion, the error vector magnitude (EVM) estimates the in-band distortion caused by the amplifier nonlinearities. EVM possesses a direct relation with the signal to noise ratio and can be used to determine the physical error introduced at different stages of communication system and thus serves as an easily tool for designers in troubleshooting specific problems.

2.2 PA classes

Before introducing the different power amplifier classes, as this this thesis is focused in the energy efficiency, let's take a look on some efficiency enhancement mechanisms. The point is, how will efficiency enhancement mechanisms improve the energy efficiency? The following classifications is done in [4] in order to reduce the wasted power in power amplifiers:

Waveform Engineering - The shape of the voltage and/or current waveform is modified, which is what happens when passing through the class A to C continuum. Harmonic content is introduced into the current, modifying its waveform, in a predictable but restricted way. Alternatively, the ratio of the current's harmonic content may be modified by injecting harmonics from either the input side or output side. For the current's harmonic content to affect the voltage waveform, a non-zero impedance must be present at that harmonic frequency. In the limiting

case, both current and voltage waveforms are square waves and antiphase. As one of them is zero at any instant in time, the power dissipation is zero. This zero dissipation applies at least to the device, but it could just be shifted elsewhere in the system.

Supply Modulation - The average or envelope supply voltage across the device, V_{supply}, is modified. With a perfect device, V_{supply} is the root-mean-square value of the voltage waveform, set so the minimum value of vd reaches zero

Load Modulation - The Zload presented to the device at the fundamental frequency is modified, ideally so the voltage (vd) swings from 0 to 2 times the supply.

Popular enhancement methods according to the mechanisms they use, are depicted in figure 2.5, using a Venn diagram for classification helps identify where additional schemes are complementary and may further improve efficiency. Once the different mechanisms are presented, different classes based on waveform engineering will be discussed, since the PA design of this thesis is based on the waveform engineering efficiency enhancement.

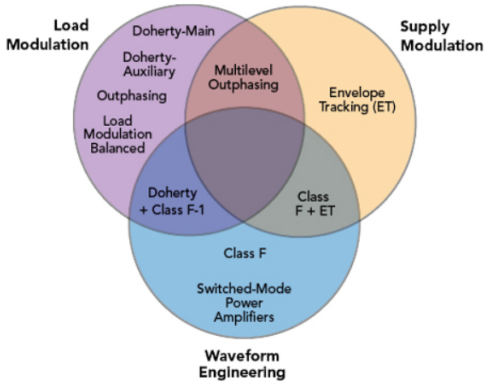


Figure 2.5: Efficiency enhancement mechanisms their hybrids and possible areas for further improvement [4]

The PAs are classified into several operation classes depending on different voltage and current waveforms. These classes can be categorized into two major groups [5]. The first group is known as transconductance PAs, in which case the transistor, i.e., field effect transistor (FET), is considered as a current source controlled by the gate voltage. The second group is called high-efficiency PAs, including switch-mode, such as the class-E and D, and harmonically tuned ones such as class-F.

2.2.1 Transconductance Power amplifiers

For transconductance PAs, the most critical parameter is the transistor gate bias that sets the operating point for the device, which typically determines the class or conduction angel of the operation, i.e., Class A, AB, B, and C(the conduction angel, θ, is defined as the number of degrees in a full RF duty-cycle that current flows). Figure 2.6 illustrates various bias condition of these PA's, and figure 2.7 illustrates they drain voltage waveform [5].

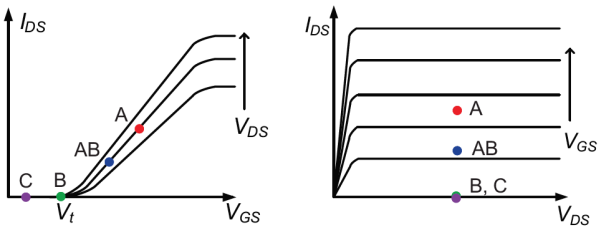


Figure 2.6: Various DC bias points of Class-A,AB,B and C [5]

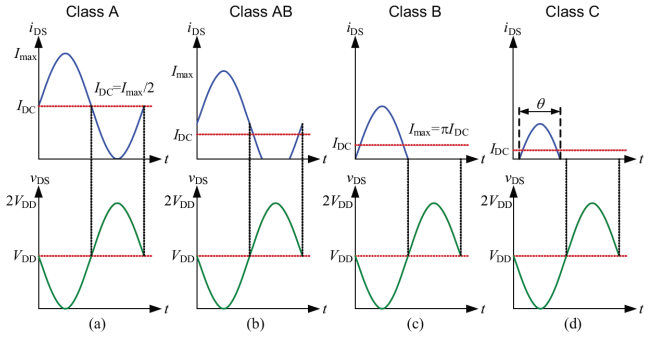


Figure 2.7: Voltage and current waveform [5]

Class A operates in full input and output ranges (θ=360º) where the current waveform has no clipping or distortion, which makes it perfect operation for an amplitude-modulated signals. However, it requires a high quiescent current $(= \frac{Imax}{2})$ and delivers a maximum efficiency of 50%. The quiescent current of the transistor can be reduced to below Imax/π by decreasing the gate bias voltage to the threshold point, resulting in a Class-B operation. Thus, the conduction angle is reduced to 180º, which means for a certain fraction of the signal period, the transistor is in complete cut off. Therefore, compared to Class-A, Class-B operation is more efficient, but it is less linear due to its half-sinusoidal current-waveform that contains high-order harmonics

and generates inherent non-linearity. If both linearity and efficiency are both concerned, a better option is to operate the amplifier between the class-A and class-B region to alleviate linearity issues while still having better efficiency than Class-A. Such an operation is called Class-AB, which is often used in the applications that require a good trade-off between linearity and efficiency. If the transistor operates for less than half of the cycle or with the conduction angle smaller than 180º, it results in the Class-C operation. This mode is highly efficient and non-linear, and thus it is mostly used for amplifying constant-envelope signals that only use phase and frequency to convey data. To sum up, the bias point determines the amplifier performance in terms of gain, power, and efficiency.

2.2.2 High Efficiency Power amplifiers

High-efficiency PAs, such as Class-E, Class-F, their duals, in theory can deliver a 100% efficiency since they are not dissipating any power internally. However, the linearity of these PAs is very poor due to the switching operation of the transistor. This group of amplifiers can be further divided into two subgroups: a) harmonic-tuned PAs, e.g., Class-F, class F^{-1} and saturated PA, and b) switching-mode PAs, e.g., E and D. Unlike the transconductance PAs, the design of high-efficiency PAs usually require harmonic impedance matching as well as the fundamental one. Hence designing this kind of amplifiers has been a challenge for designers, in part due to poor control of harmonic load impedances.

2.2.2.1 Switch-mode PAs

The **Class-D** PA shown in figure 2.8 involves two transistors to switch between, resulting in a square waveform across the switch without the coexistence of current. Each switch conducts a half sinusoidal wave that is combined to form a full sinusoidal wave via the series LC resonator. Class-D is normally used in the low-frequency range ($<$ 100 MHz) where the parasitic effect is nearly negligible.

Another switch-mode PA, **Class-E**, uses a single transistor to switch the current flows through itself and the output capacitor (C_p), as shown in Fig. 2.9 [5]. It can be seen that

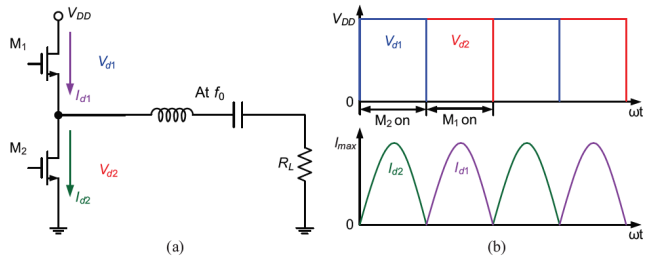


Figure 2.8: Voltage-mode Class-D PA: (a) simplified circuit schematic, (b) voltage and current waveforms [5]

the current and voltage waveforms are slightly out-of-phase, requiring a inductive load. The Class-E PA can operate at a higher frequency (giga-hertz level), as it is insensitive to parasitics since the parasitic capacitance of the transistor (C_{DS}) can be completely absorbed into C_p. More details about switch-mode PAs can be found in [5, 10].

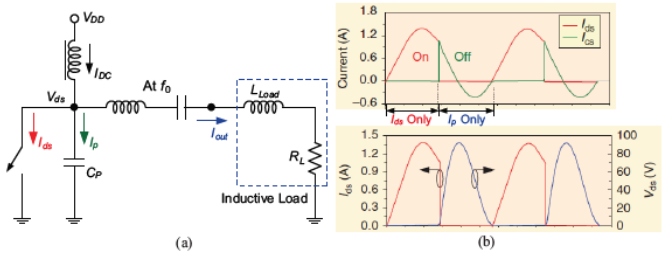


Figure 2.9: Class-E PA: (a) simplified circuit schematic, (b) voltage and current waveforms [5]

2.2.2.2 Harmonic-tuned PAs

Class F and F^{-1} PA

Figure 2.10 [5] shows the circuit schematics of Class-F and inverse Class-F PAs. By providing open-circuit and short-circuit at odd and even harmonic frequencies, the ideal Class-F PA exhibits a half-rectified sinusoidal current and rectangular voltage at the drain node, as shown in Fig. 2.10(b). There is no power dissipation in the device due to non-overlapping between voltage and current, yielding 100% efficiency. The Class-F^{-1} is the dual of Class-F, where the current and voltage waveforms are exchanged as are the harmonic loads, as shown in Fig.

2.10(c).

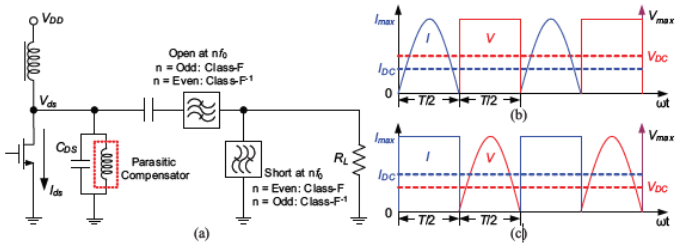


Figure 2.10: Frequency-domain high-efficiency PAs (Class-F and Class-F^{-1}): (a) simplified circuit schematic, and voltage and current waveforms of (b) Class-F and (c) Class-F^{-1} PAs.

Class F and F^{-1} PA Theory

The standard Class-F PA is developed from the Class-B PA mode by loading the active device output with proper terminations at its fundamental and harmonic frequencies [5, 10]. The half-sinusoidal current waveform, formed by the Class-B bias condition, has the following expression:

$$\begin{aligned} i_F(\theta) &= I_{peak} cos(\theta) \qquad \frac{-\pi}{2} < \theta < \frac{\pi}{2} \\ &= 0 \qquad -\pi < \theta \leq \frac{-\pi}{2}, \ \frac{\pi}{2} \leq \theta \leq \pi \end{aligned} \tag{2.17}$$

The above equation can be expressed using Fourier series (normalized to I_{peak}), given by [5]:

$$i_F(\theta) = \frac{1}{\pi} + \frac{1}{2} cos(\theta) + \frac{2}{3\pi} cos(2\theta) - \frac{2}{15\pi} cos(4\pi) + ... \tag{2.18}$$

The output matching network (filter) is required to provide open-circuit terminations at odd harmonics and short-circuit terminations at even harmonics, as shown in figure 2.10. Thus, a square voltage waveform is shaped which has no overlap with the half-sinusoidal current, leading to a theoretical 100% efficiency. In practice, harmonic control is usually conducted up to the third order, as further harmonic control yields limited efficiency improvement but

significantly increased implementation difficulty. Thus, the normalized voltage waveform of a Class-F PA with a finite number of harmonic terminations can be expressed as [5]:

$$v_F(\theta) = 1 - \frac{2}{\sqrt{3}}cos(\theta) + \frac{1}{3\sqrt{3}}cos(3\theta). \tag{2.19}$$

The above equation is able to deliver a 90.7% efficiency at the maximum power level.

Inverse Class-F PA mode is the dual of Class-F mode. It exploits dual harmonic loading conditions with open-circuit even-harmonic loads and short-circuit odd-harmonic loads, as shown in figure 2.10. This forms a square-wave current and half-sinusoidal-wave voltage, which can also lead to a theoretical 100% efficiency. In the practical case of controlling three harmonics, the voltage waveform is shaped by second-harmonic peaking [5]:

$$v_{F^{-1}} = 1 + \frac{2}{\sqrt{2}}cos(\theta) + \frac{1}{2}cos(2\theta) \tag{2.20}$$

while the current waveform takes the form of:

$$i_{F^{-1}} = i_{DC} - i_1 cos(\theta) + i_3 cos(3\theta) \tag{2.21}$$

where i_{DC} = 0.37, i_1 = 0.43, and i_3 = 0.06 [5]. Note that the voltage and current waveforms of the standard class F and F-1 where finite harmonic are considered (up to third harmonic) aren't the perfect half sinusoidal and the rectangular waveforms as shown in figure 2.10, but they are quasi-rectangular and quasi-half-sinusoidal waveforms. Figure 2.11 shows an example for a class F.

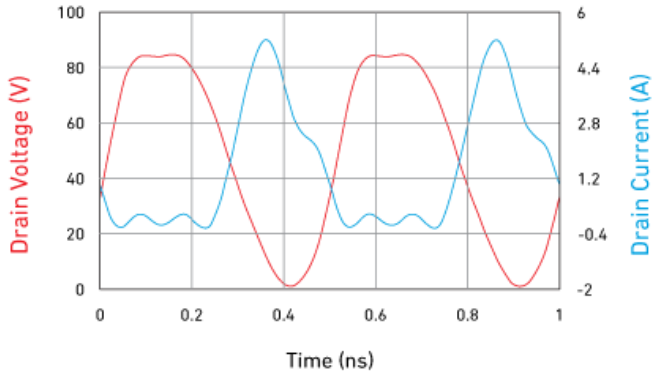


Figure 2.11: Class F waveforms considering finite harmonics (up to third harmonic)

Chapter 3

SSPA design using Power Bar

The aim of this chapter is to introduce the design flow of SSPAs that minimizes uncertainties using a bare die model. The bere die model is 85W Gallium Nitride High Electron Mobility Transistor which offers a general purpose and broadband solution for variety of RF applications such as radar and telecommunications. The circuit is manufactured on a 0.25μm gate length GaN HEMT technology on SiC substrate. It is proposed in a bare die form and requires an external matching circuitry.

3.1 Mechanical and Thermal Design

Even though the mechanical and thermal design is out of scope of this thesis, it has been considered by mechanical engineers in parallel with electrical design considered in scope of this thesis in order to overcome successfully the challenges cited in chapter 1. Figure 3.1b shows the 3D view of the SSPA prototype baseplate where the input and output network substrates will be mounted together with MMIC baseplate (Carrier) shown in figure 3.1a which will carry the MMIC power transistor together with its pre-matching network. The mentioned input, output and pre-matching network will be explained in the electrical design section.

As explained in chapter 1, the high power density in GaN semiconductors presents a major thermal management challenge. Pulling the heat away from the active region of the device is critical to maximizing the output power and reliability. Starting with the bare die, proper

thermal management requires an optimal die attach process. Since even a small increase in thermal resistance results in a significant temperature rise, use of a high thermal conductivity material for die attach is critical [1].

For example, using a gold-tin eutectic or Namics die attach process provides much better thermal conductivity than silver epoxy. However, achieving good die attach with high thermal conductivity requires more than simply choosing the correct material. The process must be carefully controlled. Since even small air voids under the die can greatly increase thermal resistance (creating hot spots), they must be minimized, which requires experience, careful process control and techniques such as performing die attach in a vacuum [1].

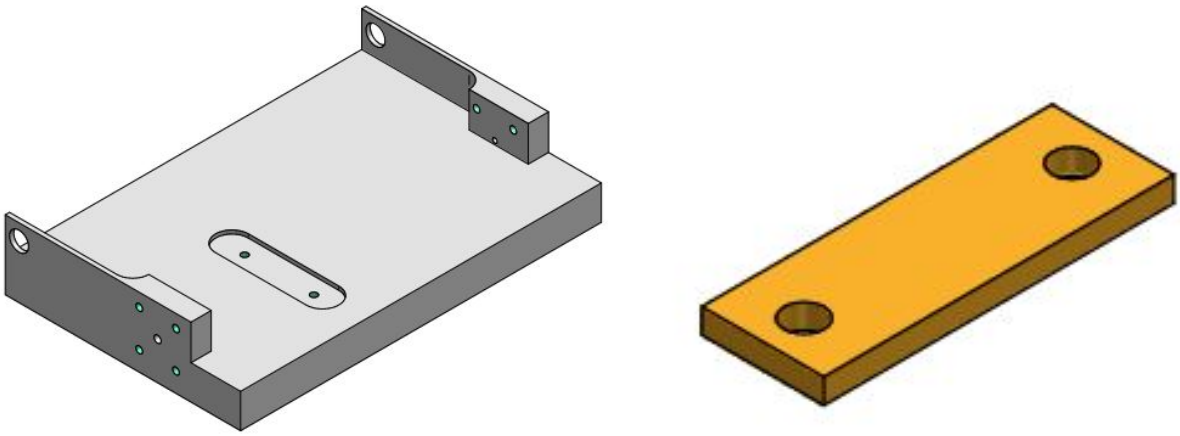
The thermal conductivity of the baseplate material holding the die (figure 3.1a) must also be maximized. For lower power applications, die is often installed on a Kovar baseplate, chosen because of its matched coefficient of thermal expansion (CTE). However, when thermal conduction is critical like in this case, a material such as copper molybdenum (CuMo) is a better choice.

The process of choosing materials to optimize the thermal conductivity of each interface continues through the entire design, i.e, from the MMIC to MMIC baseplate (figure 3.1a), then, from MMIC baseplate to SSPA baseplate (figure 3.1b) and so on. While this thermal design approach is used for GaN amplifier designs regardless of application, it is particularly important for space-qualified hardware. The size and weight constraints common to space programs increase power density by limiting the volume, while the reliability requirements for space operation require maximum cooling of the active devices [1].

3.2 Electrical design

3.2.1 8-cells Power Bar Description

The device is composed of 8x11W elementary cells. These cells are connected together with a specific network providing a good trad-off between performance and stability (resistance between gates and drains as described on figure 3.2). The reference planes are on the center of the



(a) SSPA baseplate (b) CuMo Carrier: MMIC baseplate

Figure 3.1: Baseplate 3D view

bonding pads.

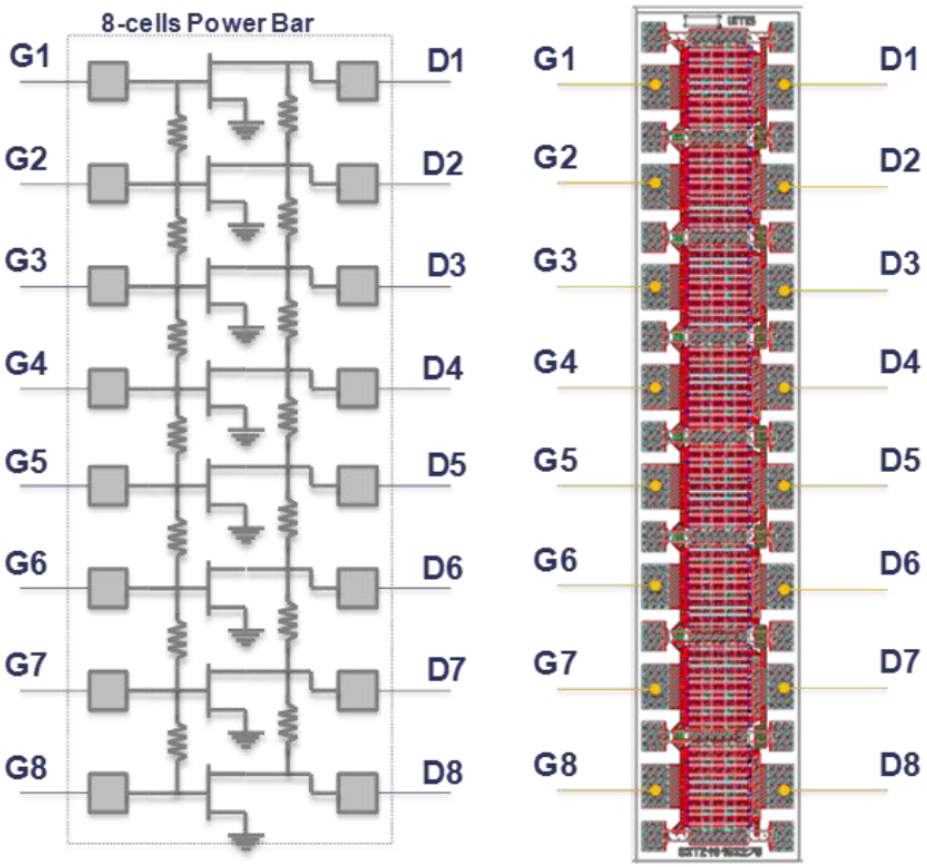


Figure 3.2: Power Bar configuration

Elementary Cell Maximum Gain and stability characteristics

Figure 3.3 shows Maximum Gain and stability simulated performance available on datasheet considering T_{ref}=+25ºC, $V_{DS} = +30V$, $I_{D_Q} = 140mA$.

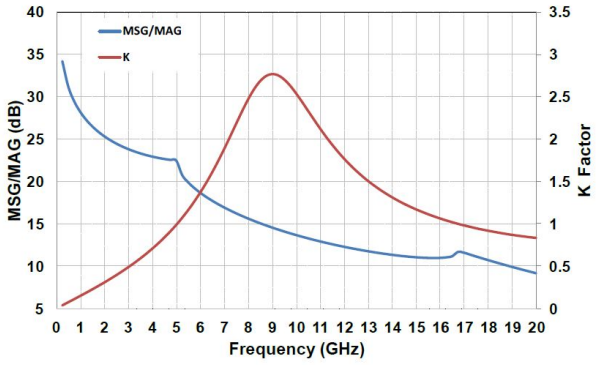


Figure 3.3: Maximum Gain and stability simulated performance

Elementary Cell Load Pull Performance

Table depicted in figure 3.4 shows the load pull simulated performance available on datasheet considering T_{ref}=+25ºC, $V_{DS} = +30V$, $I_{D_Q} = 140mA$. The impedances are chosen as a trade-off between Output Power, PAE and Stability of the device.

Frequency (GHz)	Zs	Zl	Gain (dB) @PAE_{max}	Pout (W) @PAE_{max}	PAE_{max} (%)	$Pout_{max}$ (W)
1	11.6+ j28.4	51+ j20.3	16	12.5	75	13.2
3	2.2+ j11	23.8+ j27.1	16	11.4	72	12.4
5	1.3+ j5.5	11.4+ j20.7	15	11.3	69	12.3
7	1.5+ j2.9	8.7+ j15.4	11.5	11.2	63	12
8	1.3+ j1.6	5.4+ j13.4	10	10.5	62	11

Figure 3.4: Elementary Cell Load Pull Performance

3.2.2 Biasing procedure

As explained in the previous chapter, bias point sets the class mode operation. In this case, bias point provided by the datasheet is selected ($V_{DS} = 30V$ and $I_{D_Q} = 140mA$ for a single unit

cell) which correponds to class-AB operation. In order to set the biasing point, the following procedure is recommended:

1. Bias power bar gate voltage at V_g close to $V_{pinch-off}$ (typically: $V_{GS} = -5V$)

2. Apply V_{DS} bias voltage.

3. Increase V_{GS} up to quiescent bias drain current I_{D_Q}.

3.2.3 Optimal load and source impedance extraction

Given that the biasing point provided by the datasheet is selected, optimal source and load impedance of the fundamental tone provided by the datasheet are used since they are extracted under same biasing condition. Therefore, the initial step would be running an Harmonic balance simulation using the simplest schematic as shown in figure 3.5 to be able to compare the obtained and datasheet performance.

Harmonic balance simulation results are depicted in figure 3.6, achieving 49.9 dBm output power, 17.9 dB gain and 69.12% Power Added Efficiency (PAE). To achieve higher PAE levels, harmonic loading should be considered in order to mitigate the power carried by second and third harmincs. To do so, Load Pull simulation should be performed in order to find the optimum harmonic loads.

Harmonic Load pull has been performed using the template provided by Advanced Design System (ADS). Once the optimum harmonic loads have been obtained, Harmonic Balance simulation is carried out again using the simplest schematic presented previously in figure 3.5. The obtained results are shown in figure 3.7, observe that when harmonics power is absorbed properly, such power is added to the fundamental tone which leads to an improvement in P_{out}, Gain and PAE as depicted in table 3.1.

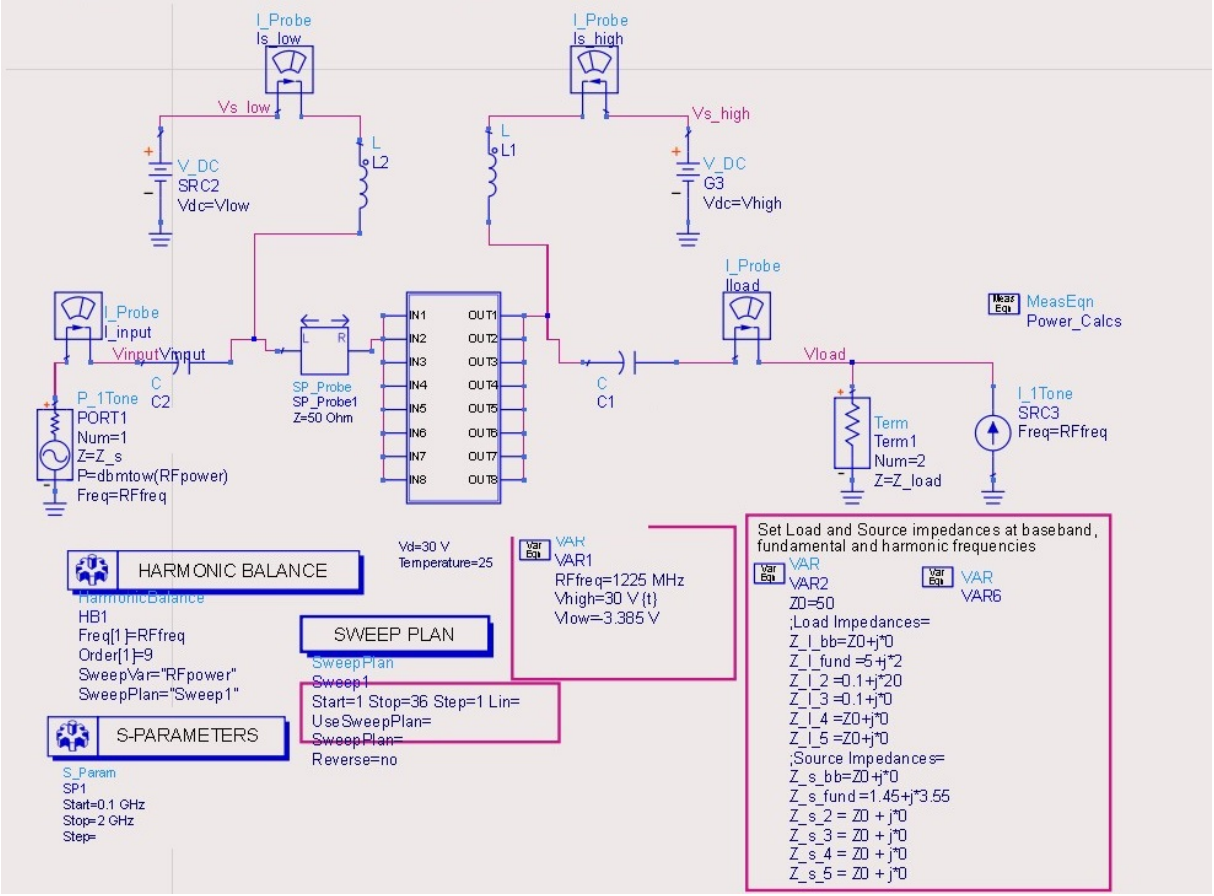
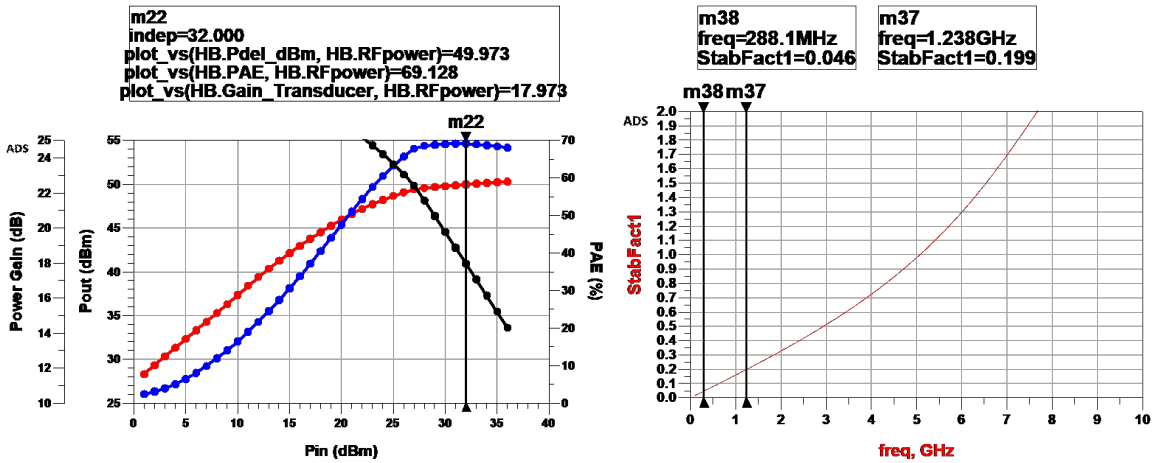
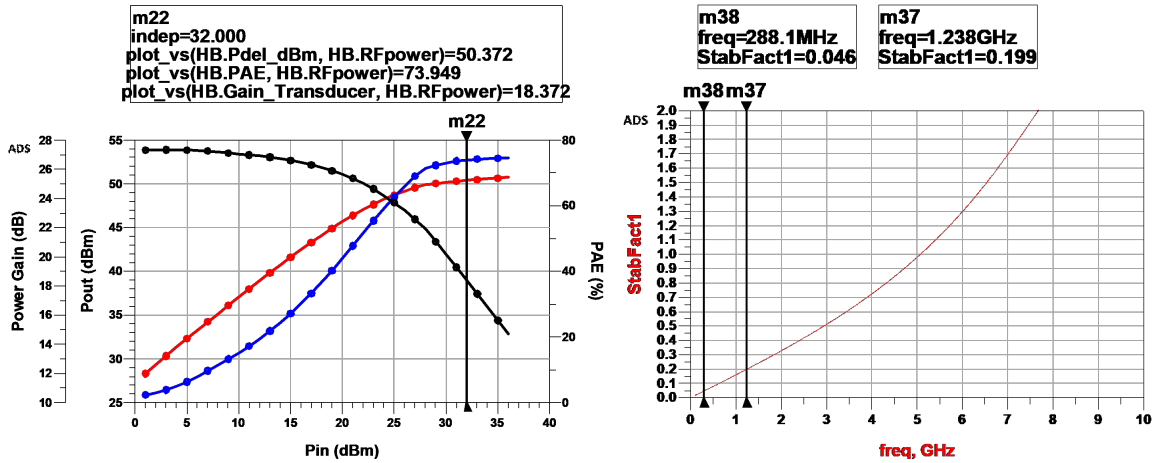


Figure 3.5: Harmonic Balance Simulation schematic



(a) P_{in} (dBm) vs P_{out} (dBm)/PAE (%)/Gain (dB) (b) Stability factor

Figure 3.6: Harmonic Balance Simulation performance



(a) P_{in} (dBm) vs P_{out} (dBm)/PAE (%)/Gain (dB) (b) Stability factor

Figure 3.7: Harmonic Balance Simulation performance using Harmonic Loads

	PAE (%)	P_{out}(dBm)	Gain (dB)
Ideal Schematic: Non-Harmonic Loading	69	49.9	17.9
Ideal Shcematic: Harmonic Loading	74	50.4	18.3

Table 3.1: Harmonic Balance simulated performance

3.2.4 Stability Network Design

At this point, having obtained the optimal impedances, it is time design the stability network in order to achieve Stability factor higher than unity at lower and design frequencies. Depending on the working frequency and transistor mode, different stability network typologies could be considered. In this case, the designed topology is shown in figure 3.8. The parallel RC (Resistor, Capacitor) plus the series Resistor placed on the RF path control the stability at higher frequencies while the elements placed on the bias network control the stability at lower frequencies.

Having included the stability network, Harmonic Balance simulation is carried out and results shown in figure 3.9 are obtained. Observe that stability factor higher than unity is achieved

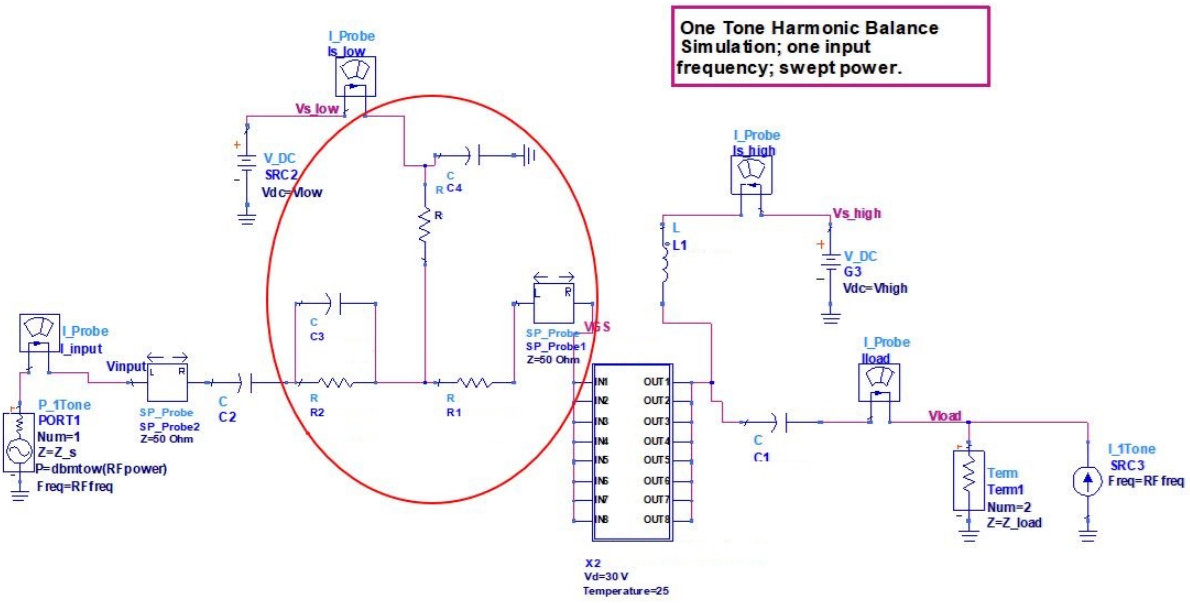
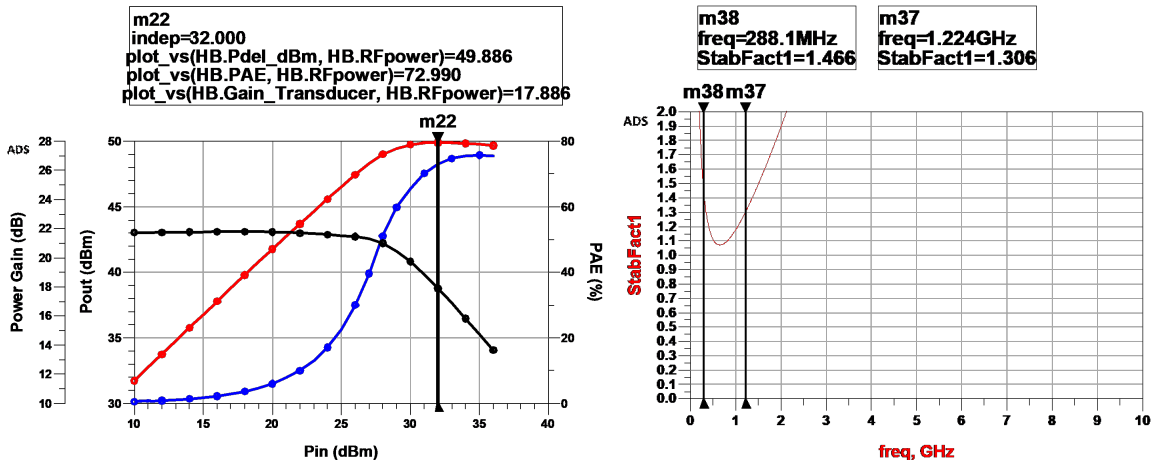


Figure 3.8: Harmonic Balance Simulation schematic including stability network

in broadband frequency range.



(a) P_{in} (dBm) vs P_{out} (dBm)/PAE (%)/Gain (dB) (b) Stability factor

Figure 3.9: Harmonic Balance Simulation performance including stability network

3.2.5 Pre-matching network design

Now, the next step is to design the pre-matching network and add it to previous simulation, then, re-adjust it to maintain the previous obtained performance. Pre-matching network is usually

used in power transistors package (in this case, in the carrier) to convert the MMIC gate low impedance to a higher impedance which can be matched to the source impedance by means of an external input matching network. Pre-matching network is the combination of bonding wires (inductors) + capacitors.

It must be taken into account that in the the taper + pre-matching network (R+ L + C), is the set of elements that must be adjusted to obtain the optimal impedance to the input of the transistor, since the stability network will have a fixed impedance marked by the elements that compose it which can not be modified since they are necessary to stabilize the SSPA. Figure 3.10 shows the designed Taper and Carrier pre-matching Network, it is composed by Resistors (used to stabilize) + Inductors + Capacitors where Inductors are modeling bonding wires to be used in practice.

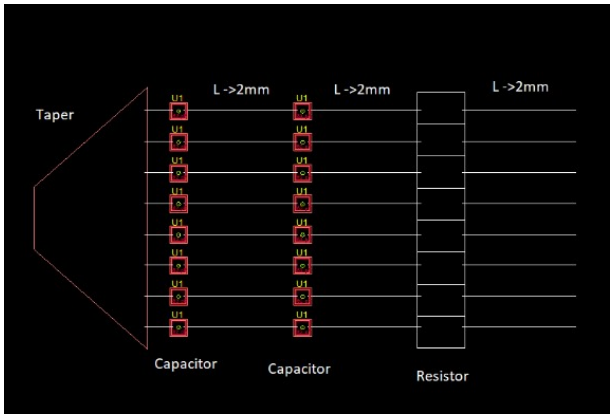
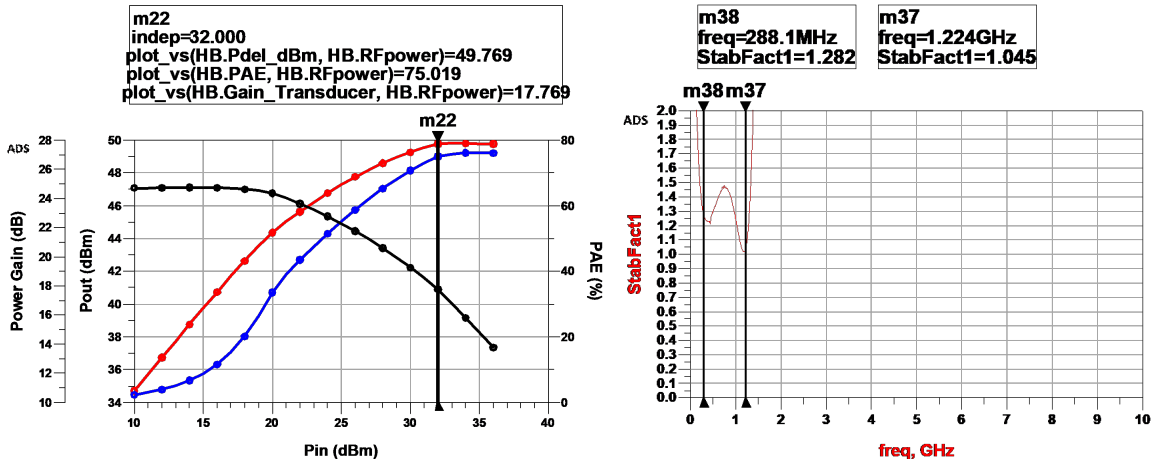


Figure 3.10: Pre-matching Network

Once the pre-matching is designed and taper is modeled in momentum together with stability network, Harmonic Balance simulation is carried out and results shown in figure 3.11 are obtained where it can be seen that the previous performance is maintained as required.

3.2.6 Input Matching Network Design

Once the Taper and stability network are designed, the next step is to measure the input impedance at begging of the stability network as the reference point. In this case, $Z_{in} = 15.5 + j16$ is measured at established reference point, therefore, a matching network should



(a) P_{in} (dBm) vs P_{out} (dBm)/PAE (%)/Gain (dB) (b) Stability factor

Figure 3.11: Harmonic Balance Simulation performance including stability network + Taper

be designed in order to convert such impedance into $Z_{in} = Z_0 = 50\Omega$. Figure 3.12 shows the proposed matching network, a series Inductor + shunt Capacitor.

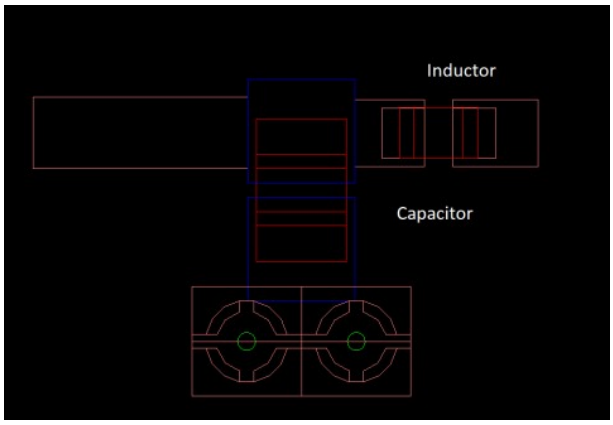


Figure 3.12: Input Matching Network

At this point, the designed input matching network must be incorporated to the entire input network of the SSPA and simulate it in momentum. Then, perform Harmonic Balance simulation to verify whether the designed input matching network is working properly or not. In this case, similar results to the ones shown previously in figure 3.11 are obtained.

3.2.7 Output Matching Network

In this subsection, a matching network able to match fundamental, second and third harmonic frequencies will be presented based on [11]. Initially, second and third harmonic loads extracted in load pull simulation will be synthesized by means of shunt stubs as shown in figure 3.13. Then, fundamental frequency matching must be considered by means of adjusting the entire topology.

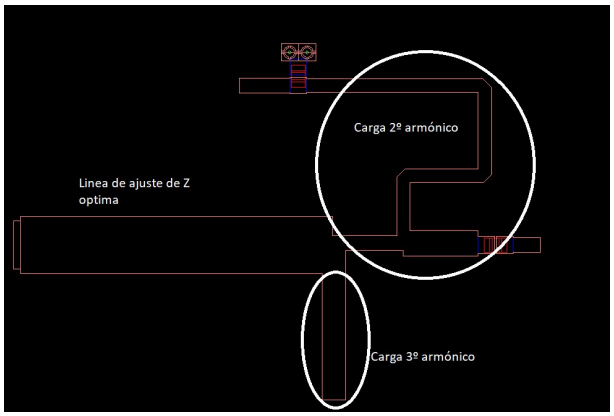


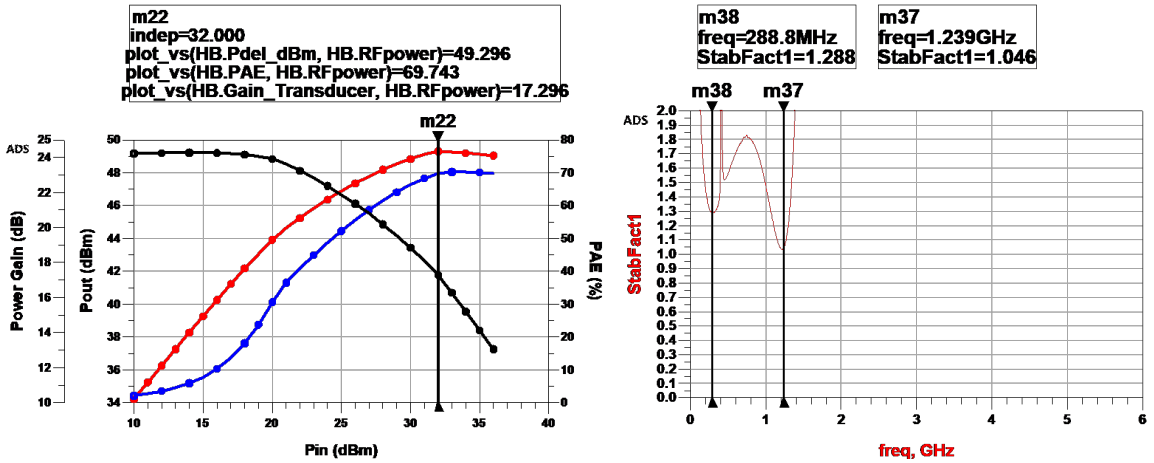
Figure 3.13: Output Matching Network

The presented topology have been designed using passive S-parameters simulation to assure that the input impedance seen from the transistor side corresponds to the impedance given by the datasheet at fundamental frequency and to the loadpull extracted impedances at harmonic frequencies. In order to verify its functionality, it is incorporated to the Harmonic Balance simulation setup and the results obtained are shown in figure 3.14.

At this point, the SSPA design could be closed, however, before doing so, part stress and derating analysis should be performed in order to verify if the different components (mainly at the input network) withstand the power or current flowing through them. Such analysis will be detailed in the following subsection.

3.2.8 Part Stress and Derating Analysis

Part stress analysis is based on placing two probes at the border of the component to be analyzed to be able calculate the power and current at the simulation level. Once these values



(a) P_{in} (dBm) vs P_{out} (dBm)/PAE (%)/Gain (dB) (b) Stability factor

Figure 3.14: Harmonic Balance Simulation performance including input and output networks

are determined, component power and current handling must be checked on datasheet to verify how much power/current is able to withstand. Apart of complying with the analyzed value, it is necessary to leave a margin (derating) stipulated by the ECCS standard, i.e, if a 0.1 A RF and 90mA DC current are measured on a 50Ω, that is 0.9W, a minimum margin of 1.8W must be kept.

Having said that, part stress analysis of the input network components has been performed, mainly the stability network resistors presented previously in figure 3.8, and the corresponding layout is presented in figure 3.15. Observe that instead of using a single Resistors value in the stability network as in figure 3.8, several Resistors have been arranged in parallel to achieve the desired value, this is done to withstand the power/current and to comply with ECCS standard derating values. Performing such modifications in the input network layout may produce some changes on the performance, therefore, possible adjustments of the input network may be required.

3.2.9 SSPA full layout

Figure 3.16 shows the SSPA full layout as the result of joining all the parts described in the previous subsections: input network, carrier (pre-matching network + MMIC) and output network.

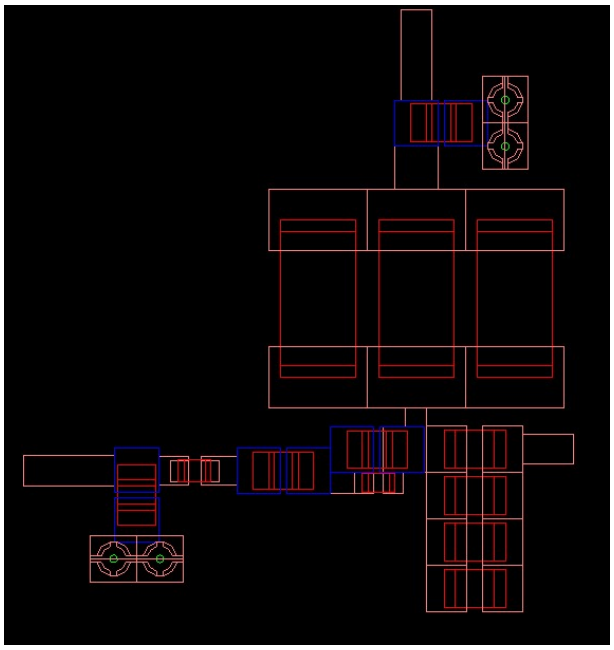


Figure 3.15: Input network considering Resistors deratings

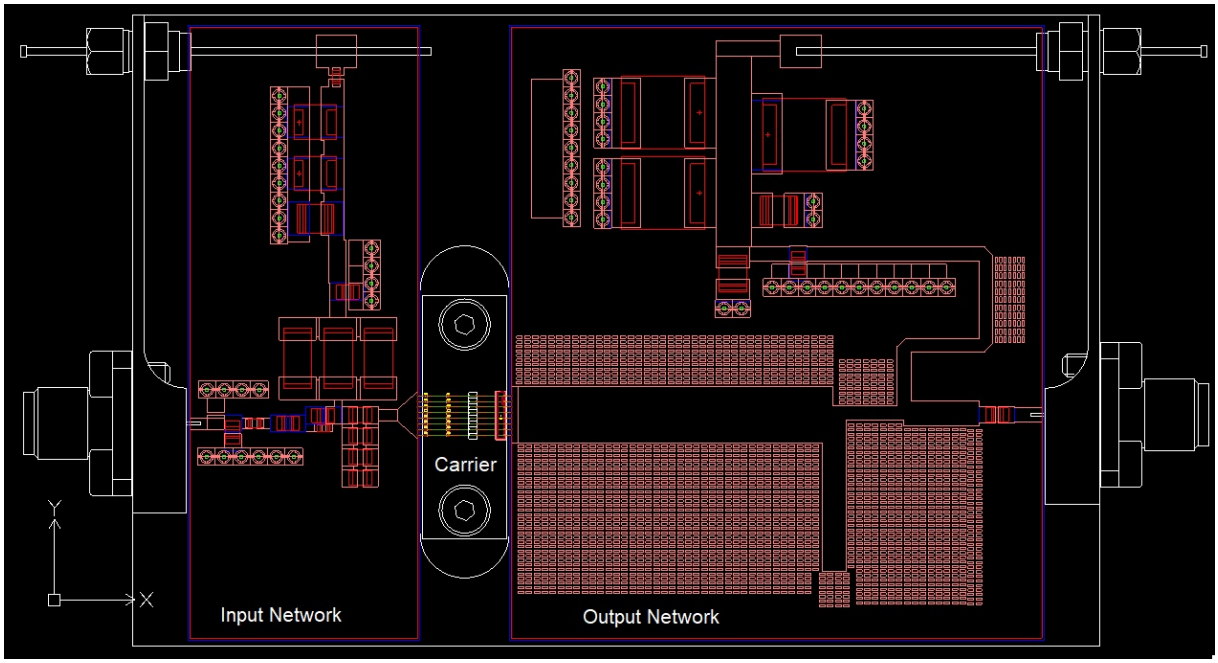


Figure 3.16: SSPA full layout

Such layout have been simulated and optimized to achieve a quite similar performance to the one obtained previously in figure 3.14 where the full design was simulated without taking into account the part stress and derating analysis. Table 3.2 illustrates a summary of the full layout and initial obtained performance, observe that the full layout design achieves 49.2 dBm output

power, 17.3 dB gain and 69.12 % Power Added Efficiency.

	PAE (%)	P_{out}(dBm)	Gain(dB)
Ideal Schematic: Non-Harmonic Loading	69	49.9	17.9
Ideal Schematic: Harmonic Loading	74	50.4	18.3
Full Layout	69,7	49,2	17,3

Table 3.2: Harmonic Balance simulated performance summary

Chapter 4

SSPA Functional Test

This chapter aims to present the functional test of two prototypes. Such prototypes are mounted and tested at ambient temperature under small and large signal conditions.

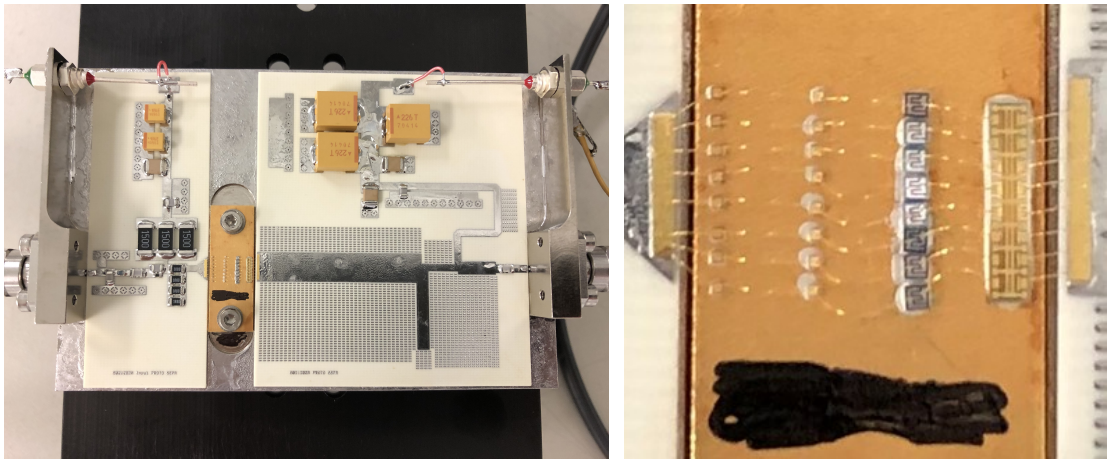
4.1 Prototype 1

The mounted prototype 1 is shown in figure 4.1, observe that it is composed by an input network (left), output network (right) and the carrier where the MMIC power transistor is mounted together with its internal matching network. Components mounted on the carrier are interconnected using wire bonding technology.

4.1.1 Small signal measurement

To be able to perform small signal measurement, it is necessary to bias the transistor previously. To do so, the following biasing procedure is proposed:

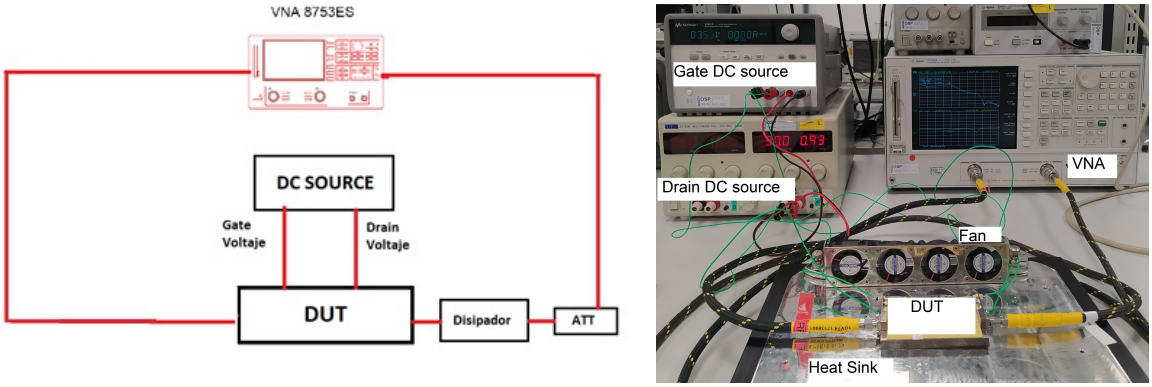
1. Bias power gate voltage at V_g close to $V_{pinch-off}$: typically: V_{GS}=-5V
2. Apply V_{DS} bias voltage (Typically: $V_{DS} = 30V$)
3. Increase V_{GS} up to quiescent bias drain current I_{D_Q}



(a) Prototype 1 (b) Carrier zoom in

Figure 4.1: Fabricated SSPA prototype 1

The quiescent current steady state must be carefully controlled as it is influenced by the operating mode, the temperature and the overall thermal resistance. A drain current control is recommended on the biasing network.



(a) Bloch diagram (b) Laboratory

Figure 4.2: Small signal measurement test bench

Once the biasing procedure is completed, the next step is perform the small signal measurement, to do so, the test bench shown in figure 4.2 will be used where the following instruments are required:

1. **Vector Network Analyzer (VNA)** to perform S-parameters measurement.
2. **DC source** to bias the transistor.

3. **Attenuators** to protect the VNA (in this case, it is optional if the test is at very small signal levels).

4. **Dissipator** to achieve good heat dissipation.

5. **Calibration** kit for de-embedding additional elements placed in the RF path (harness, transitions, attenuators, etc...).

Measurement results are shown in figure 4.3, it can be observed that measurement traces present a frequency shift compared to simulation. Given this situation, two options could be considered. On one side, carry out power measurement at the frequency where the prototype 1 is centered (990 MHz), this will give us an idea about how the SSPA behaves when RF power is injected, however, efficiency and Power Added Efficiency cannot be calculated efficiently given that the output matching network was designed at 1.225GHz as the central frequency. On the other hand, shift back the prototype response to the design frequency in order to carry out power measurement efficiently.

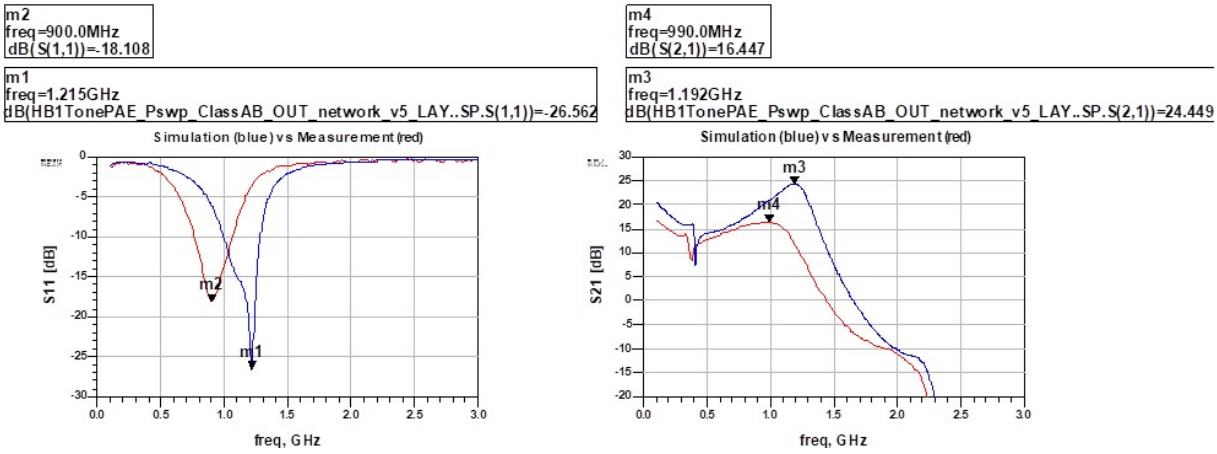


Figure 4.3: Prototype 1 Small signal measurement: measurement vs simulation

4.1.2 Large signal Measurements

To be able to carry out power measurements, a more sophisticated test bench is required. Figure 4.4 shows the mounted test bench at the laboratory, it is equivalent to the block diagram shown in figure 4.5.

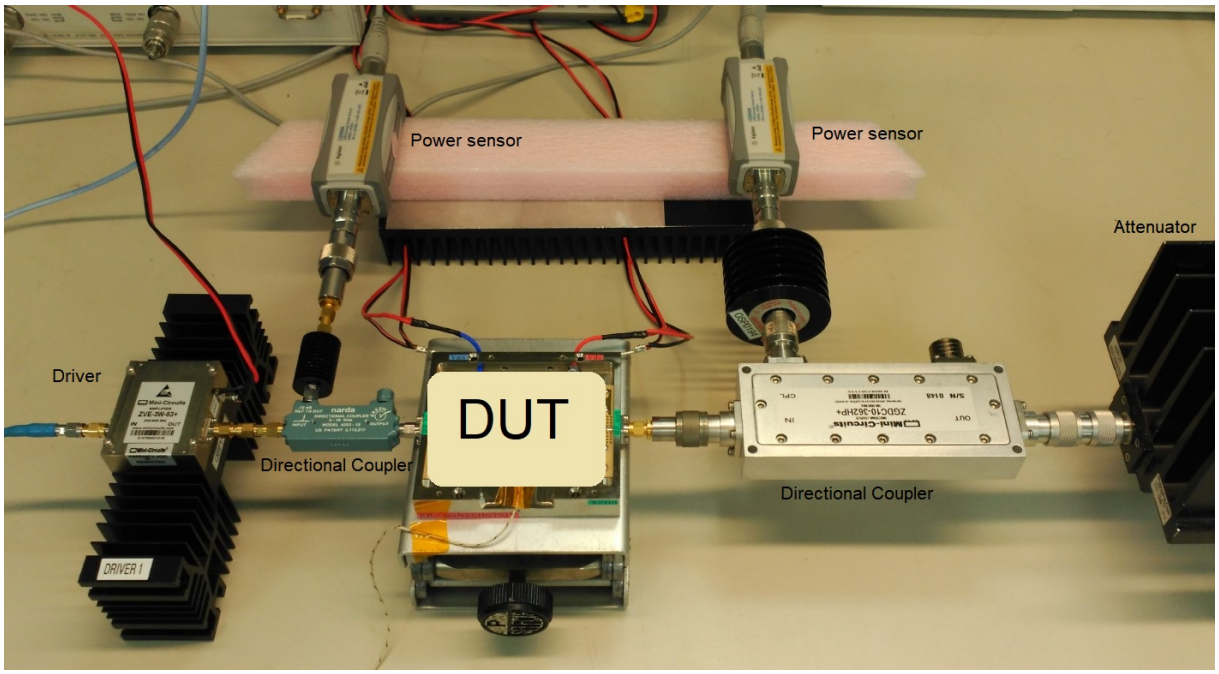


Figure 4.4: Large signal measurement laboratory test bench

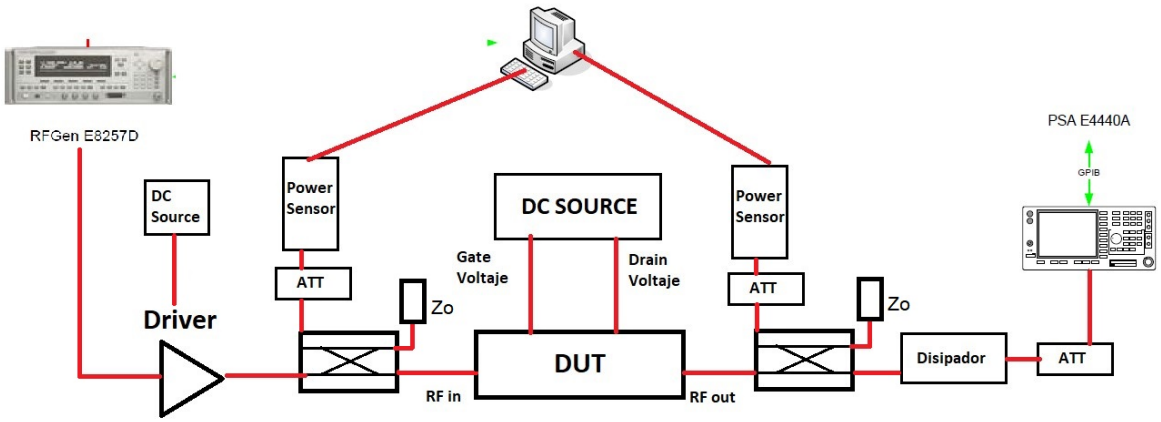


Figure 4.5: Large signal measurements Bloch diagram test bench

In order to be able to mount the previously mentioned test bench, the following instruments are required:

1. **RF generator** to generate the RF signal.

2. **Directional couplers** to take samples of the signal at input and output of the DUT.

3. **Power sensors** to measure the signal power received at the coupled ports (input and

output power of the DUT).

4. **Attenuators** to protect power sensors and Power Signal Analyzer.

5. **Driver** to achieve the input power required by the DUT.

6. **Heatsink** to achieve good heat dissipation.

7. **DC source** for Driver and DUT biasing.

8. **Power Signal Analayzer (PSA)** to analyze the power signal at output of the DUT.

9. **Calibration Kit** for de-embedding additional elements placed at the RF path (harness, transistions, attenuators, couplers, etc)

4.1.2.1 Line-up

To be able to test the DUT at large signal levels, a line-up must be defined in order to identify the necessary power amplification sections at the input of the DUT to achieve the required input power and the necessary attenuation at output to protect the instruments at the output of the DUT. Besides, line-up provides information about the input power of each stage of the RF path, this helps to select the model of each instrument in terms of power handling.

Having said that, let us introduce the two possible scenarios to be considered. The first one is one shown in figure 4.6 where the RF generator is able to handle up to -10 dBm RF power, this leads us to use a 48 dB pre-amplification stage. The second one is shown in figure 4.7 where the RF generator is able to handle up to +15 dBm RF power, this leads us to use a 24 dB pre-amplification stage. Both scenarios may be considered at the testing phase depending on the RF generator availability in the laboratory.

4.1.2.2 Pre-amplification stage characterization

As stated previously, pre-amplification stage depends mainly on the RF generator maximum available power. Thus, considering the first case where the RF generator is able to handle up to +15dBm, a pre-amplification stage of 24 dB is required to achieve the input power required by

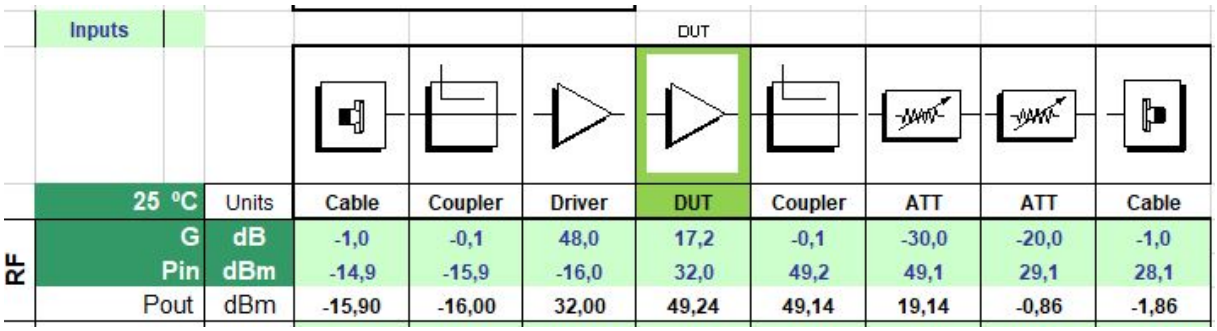


Figure 4.6: Line-up using a -10 dBm maximum power RF generator

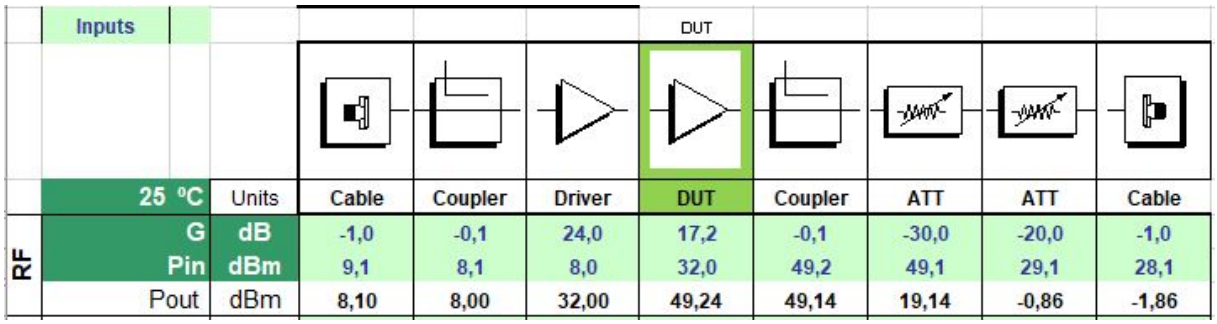
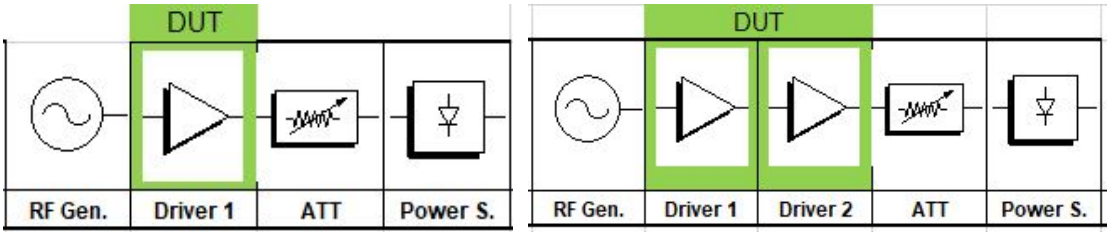


Figure 4.7: Line-up using a +15 dBm maximum power RF generator

the DUT ($P_{in} = 32dBm$). SPA029 SARAS Technology is the selected driver to be used in the pre-amplification stage, such power amplifier has been characterized in the laboratory using the test bench block diagram depicted in figure 4.8a.



(a) Single amplifications stage (b) Double amplification stage

Figure 4.8: Drivers characterization test bench block diagram

The obtained results are depicted in figure 4.9 and table 4.1, observe that the analyzed driver is able to handle up to $P_{1dB} \geq 33dBm$ providing 23 dB power gain as stated by the manufacturer in the datasheet. Therefore, it will work perfectly for the SSPA power measurement given that it is able to handle 32 dBm at input of the SSPA below 1dB compression point.

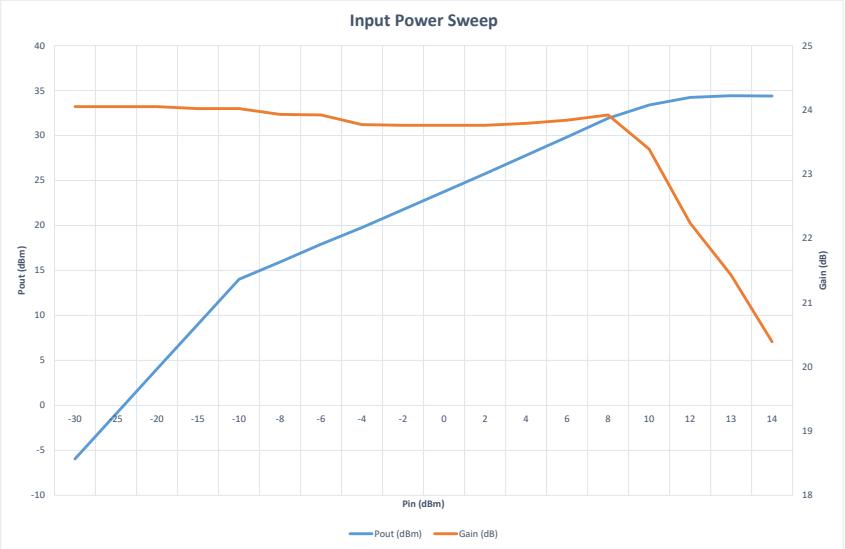


Figure 4.9: Single Driver Input Power Sweep

Even though the analyzed driver works properly for the intended SSPA power measurement, the problem may come from the availability of the 15 dBm RF generator as mentioned previously. Hence, other solutions must be considered for the case where the RF generator is able to handle up to -10 dBm RF power. Such scenario requires higher gain in the pre-amplification stage, therefore, two options may be considered:

1. Single pre-amplification section using a single driver able to provide 48 dB power gain as stated in the line-up section.

2. Two pre-amplification sections concatenating two drivers as the one analyzed previously (SPA029 SARAS Technology) to provide 48 dB total power gain as stated in the line-up section.

In this case, option 2 will be consider due to the availability of the instruments. Such scenario where two drivers are concatenated has been characterized in the laboratory using the test bench shown in figure 4.8b and the results obtained are depicted in table 4.2. In the same way as in case of a single driver, the proposed pre-amplification stage is able to handle

RF Gen.	Driver			
P_{av} (dBm)	Gain (dB)	Comp (dB)	P_{out} (dBm)	P_{out} (W)
-30	24,05	0	-5,95	0,0003
-25	24,05	0	-0,95	0,0008
-20	24,05	0	4,05	0,0025
-15	24,02	0,03	9,02	0,01
-10	24,02	0,03	14,02	0,03
-8	23,93	0,12	15,93	0,04
-6	23,92	0,13	17,92	0,06
-4	23,77	0,28	19,77	0,09
-2	23,76	0,29	21,76	0,15
0	23,76	0,29	23,76	0,24
2	23,76	0,29	25,76	0,38
4	23,79	0,26	27,79	0,60
6	23,84	0,21	29,84	0,96
8	23,92	0,13	31,92	1,56
10	23,39	0,66	33,39	2,18
12	22,24	1,81	34,24	2,65
13	21,43	2,62	34,43	2,77
14	20,39	3,66	34,39	2,75

Table 4.1: Single Driver Input Power Sweep

$P_{1dB} \geq 33dBm$ providing 48 dB power gain, therefore, in addition to single diver solution, two concatenated drivers solution may also be considered due to its good performance.

4.1.2.3 SSPA characterization

Having characterized the pre-amplification stage, it is time to carry out the large signal measurement of the designed Solid State Power Amplifier, to do so, the test bench presented in figure

RF Gen.	Drivers			
Pav (dBm)	**Gain (dB)**	**Comp (dB)**	**Pout (dBm)**	**Pout (W)**
-35	48,5	0	13,5	0,02
-20	48,5	0	28,5	0,71
-18	48,5	0	30,5	1,12
-16	48,5	0	32,5	1,78
-14	48,23	0,27	34,23	2,65
-13	47,77	0,73	34,77	3,00
-12	47,11	1,39	35,11	3,24
-11	46,26	2,24	35,26	3,36
-10	45,84	2,66	35,84	3,84

Table 4.2: Two Drivers Input Power Sweep

4.5. Due to the instruments availability, the -10 dBm available power RF generator will be used, therefore, the scenario with two concatenated drivers will be considered in the pre-amplification stage.

Before presenting the large signal measurements, it is of great importance to remember that the prototype to be measured at the large signal domain presents a maximum small signal gain at 990 MHz as the central frequency whereas the design frequency is 1.225 GHz, in addition to the fact the measured gain is smaller than the simulated gain. These two facts will lead to the following issues:

- As stated previously, performing large signal measurement at 990MHz (measured central frequency) leads to an inefficient PAE measurement given that the output matching network was designed for maximum PAE at 1.225GHz as the central frequency.
- Furthermore, given that measured gain is smaller than the simulated one, the required input power must be increased to achieve the design output power condition for maximum PAE. In this case, requiring higher power levels ($> 32dBm$) at the DUT input may lead pre-amplification stage analyzed previously (drivers) to work beyond P_{1dB} compression

point and additional tones will be injected to the DUT due to non-linear behaviour of the pre-amplification stage.

The mentioned issues can be noticed in table 4.3 where the SSPA power measurement results are depicted. Observe that 50 Watts (46.99 dBm) was the maximum achievable power due to limitation of the test bench, mainly due to the RF generator ($P_{av_{max}}$=-10 dBm). Even if the RF generator could handle more than -10 dBm available power, a second limitation would come from the pre-amplfication stage given that it compresses 2.66 dB (near to 3 dB compression point) which makes the spectrum dirty at the input of the DUT.

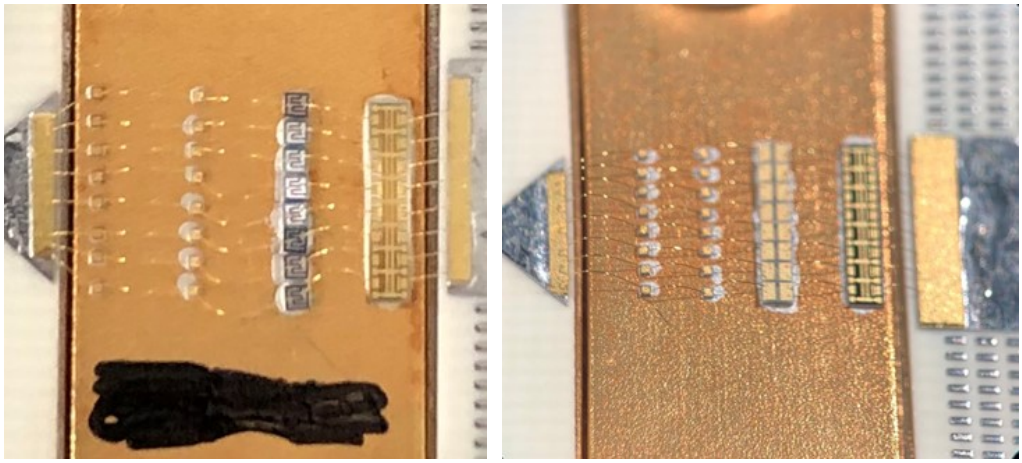
Results shown in table 4.3 provide information about how the SSPA behaves when RF power is injected, however, such results cannot be compared to the simulation given that they are performed under different conditions as mentioned previously (Frequency and power). Therefore, to be able to perform large signal measurements under the same conditions, prototype 1 small signal response must be shifted back to the design frequency.

RF Gen.	Drivers				DUT					
Pav (dBm)	Gain (dB)	Comp (dB)	Pout (dBm)	Pout (W)	Gain (dB)	Comp (dB)	Pout (dBm)	Pout (W)	DC Power (W)	Efficiency (%)
-35	48,5	0	13,5	0,02	16,2	0	29,7	0,93		
-20	48,5	0	28,5	0,71	13,84	2,36	42,34	17,14	57,12	30,0%
-18	48,5	0	30,5	1,12	13,4	2,8	43,9	24,55	71,1	34,5%
-16	48,5	0	32,5	1,78	12,92	3,28	45,42	34,83	84,6	41,2%
-14	48,23	0,27	34,23	2,65	12,28	3,92	46,51	44,77	96,3	46,5%
-13	47,77	0,73	34,77	3,00	12,05	4,15	46,82	48,08	99	48,6%
-12	47,11	1,39	35,11	3,24	11,9	4,3	47,01	50,23	102,3	49,1%
-11	46,26	2,24	35,26	3,36	11,83	4,37	47,09	51,17	103,8	49,3%
-10	45,84	2,66	35,84	3,84	11,15	5,05	46,99	50,00	102,9	48,6%

Table 4.3: SSPA Input Power Sweep

4.2 Prototype 2

In order to correct such frequency shift, a second prototype is mounted where the capacitors mounted at left-hand side of the carrier are shifted to right making the bonding interconnecting the border capacitors shorter as shown in figure 4.10.



(a) Prototype 1 (b) Prototype 2

Figure 4.10: Carrier configuration

4.2.1 Dissipation Issues

During the functional test of the SSPA, several issues related to the remarked challenges of GaN technology in chapter 1 and 3 have been experienced. During the biasing procedure, the following issues have been experimented leading to damage and replace the MMIC power transistor multiple times:

1. MMIC-1 (attached with ablebond epoxy): Drain current increases exponentially from 0.8-1A until reaching the source limitation (set to 1.3 -1.5A). Below this point, the current increases slowly along time. After several iterations, the MMIC performance started to degrade. This justifies the importance of the die attachment mentioned in chapter 3 (section 3.1). Due to the Ablebond poor thermal conductivity (3 W/(m·K)), the die have been damaged, therefore, an other die attach material should be used.

2. MMIC-2 (attached with Namics): Initially, it is biased at lower Iq levels (Iq=0.5A) and small signal measurements are performed, during the measurements, drain current increases slowly along time. However, it has been possible to bias the SSPA up to 1.1 A without damaging the MMIC which confirms the Namic good conductivity (240 W/(m·K)).

Drain current instability can be caused by two options, on one side, it can be caused by some oscillations due to SSPA instability. On the other hand, it can be caused by dissipation issues. To verify that the SSPA is not really oscillating, the output has been connected to a Power Signal Analyzer (PSA) while loading the input with a 50Ω, then, if the SSPA is oscillating (unstable), RF signal would be generated by the SSPA and detected by the Power Signal Analyzed (PSA). In this case, no-RF signal was detected by the PSA which means that the SSPA is not oscillating, that is, it is stable.

Having discarded instability, it is time to verify whether the problem is due to dissipation issues or not. To do so, drain current have been monitored along time (1h) and it can be confirmed that the problem is effectively due to dissipation issues given that the drain current stops increasing when fan is used. Therefore, from now on small and large signal measurement will be carried out using fan in order to keep drain current stable.

4.2.2 Small signal measurements

Initially, protoype 2 is biased at I_q= 0.5 A and the small signal measurement results obtained are shown in figure 4.11. Observe that the re-arrangement of the bordercap capacitors mounted on the carrier has not shifted back the response to the design frequency as predicted. Note that proto-1 is biased at Iq=1.1A whereas proto-2 is biased at Iq=0.5A, therefore, lower gain is expected.

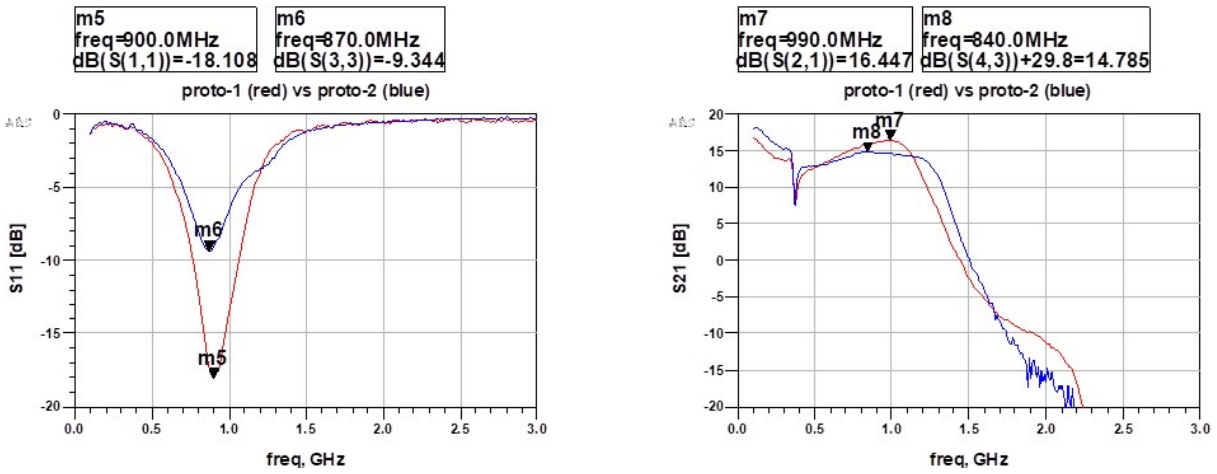


Figure 4.11: Small signal measurement: Prototype 1 vs Prototype 2

Taking advantage of the prototype 2 MMIC replacement, S_{11} of the input passive network was measured when the MMIC was extracted, response obtained is shown in figure 4.12. Observe that the measured response is shifted in frequency compared to the simulated response, therefore,it can be confirmed that the frequency shift observed in the small signal measurement of both prototypes comes from the input passive network. Such frequency shift could be produced by several reasons:

- Border capacitors: modeled as ideal capacitors → Very likely
- Wire bondings: modeled as ideal inductors with a series resistance → Very likely
- Input matching network LC elements: real model is used → Unlikely

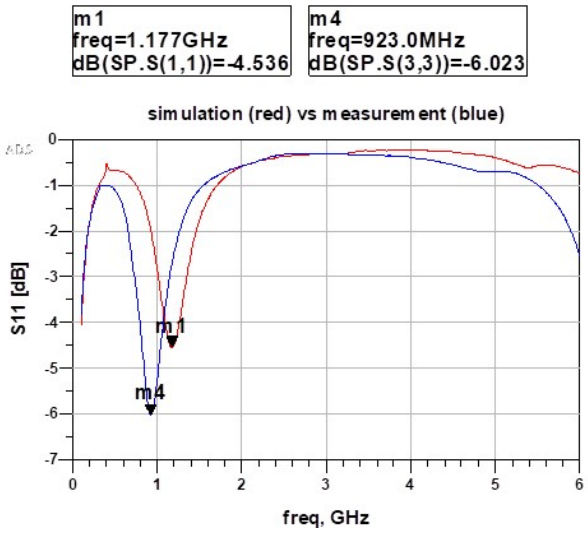


Figure 4.12: Input passive network S-parameters measurement (no-MMIC)

Having detected that the frequency shift observed in small signal measurement comes from the input passive network, one should characterize and correlate the response of such network individually in order to reduce complexity and uncertainty. Such correlation will be detailed in the next chapter.

Chapter 5

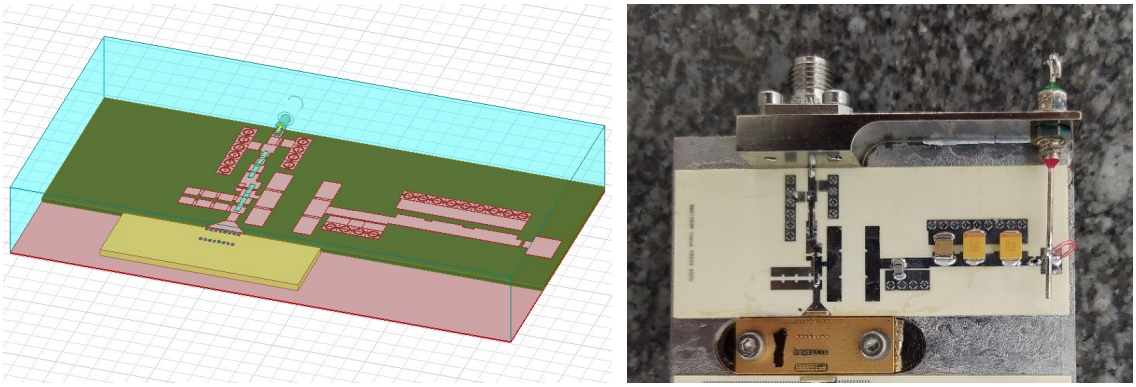
Simulation and Measurements Correlation

This chapter aims to introduce the measurement and simulation performance correlation, starting with a basic configuration, then, it is scaled up until the performance of SSPA full layout is correlated. To perform such correlation, 3D models of the border capacitors and bonding wires have been created and simulated in HFSS, then, electrical models have been extracted to be used in other simulators such ADS.

5.1 Input network

To be able to correlate the measurement with the simulation results, it is necessary to begin with a basic configuration in order to correlate the magnitude and phase. The basic configuration is the one shown in figure 5.1 where all the components in the RF path are removed. To simplify the analysis for phase correlation, the first measurement is performed without any bonding wire connection, that is, input network is measured considering an open circuit condition at edge of the taper.

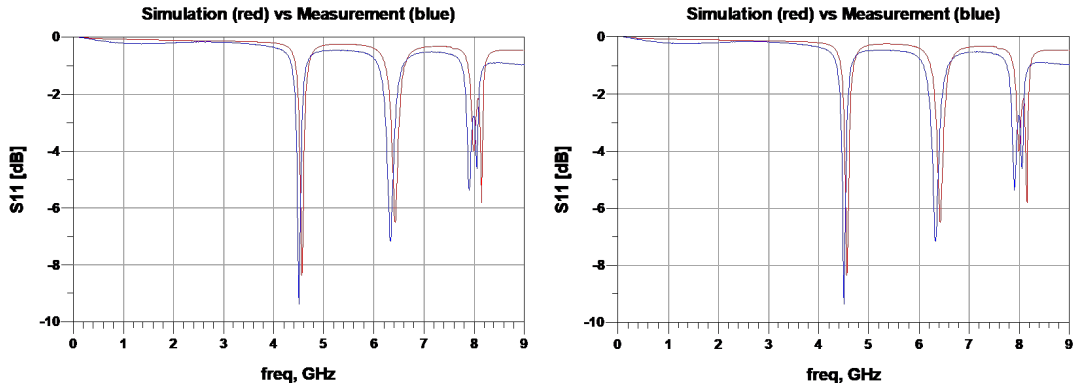
Measurement versus simulation results are shown in figure 5.2a, 5.3a and 5.4a, good agreement between measured and simulated S_{11} magnitude is achieved, however, observing the response in the Smith chart a disagreement in the phase can be observed. Such disagreement comes from the SMA flange which is not taken into account in the calibration process. To mitigate such disagreement, an ideal 50 Ω transmission line which simulates the SMA flange must



(a) 3D model (b) Prototype 1

Figure 5.1: Input passive network: taper open circuit (no-components)

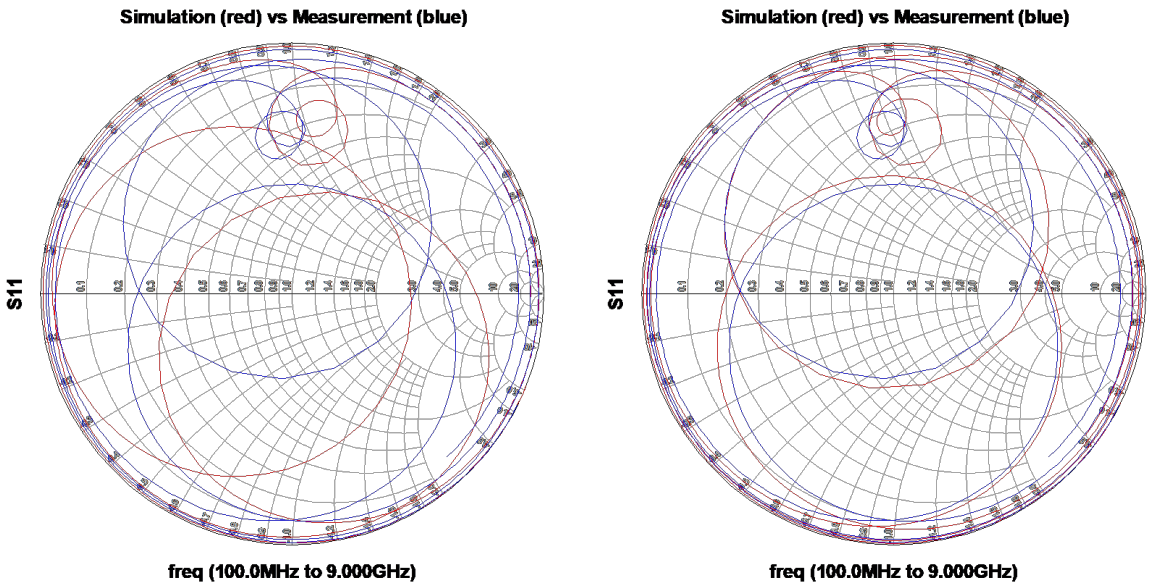
be added to the simulated model at its input and sweep its electrical length until good agreement on both magnitude and phase is achieved as shown in figure 5.2b, 5.3b and 5.4b. Such correlation will be useful for further circuits characterization on the smith chart when the complexity of the considered configuration gets increased.



(a) no-additional TL considered (b) additional TL considered

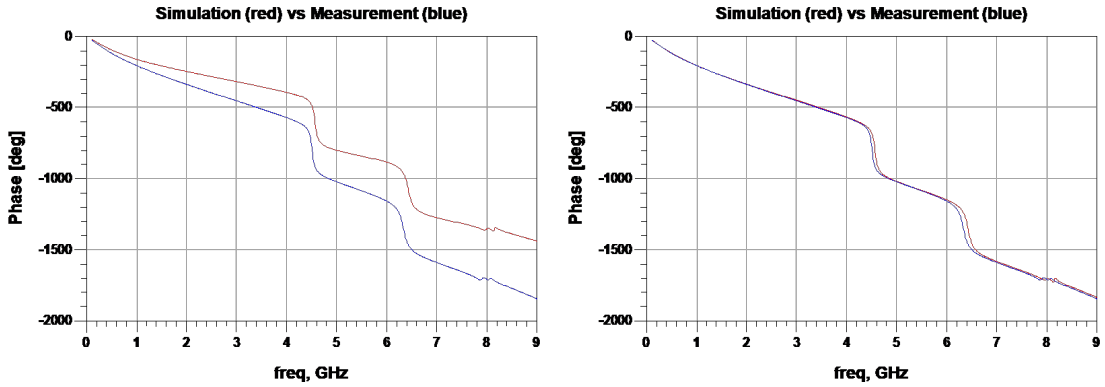
Figure 5.2: Input passive network S_{11} rectangular plot: taper open circuit

Having correlated the input network phase and magnitude under open circuit condition at the taper edge, one should consider increasing a little bit the complexity of the input network by means of introducing border capacitors and bonding wires connections to be able characterize and correlate their electrical behaviour. Initially, a single row as shown in figue 5.5 is considered to simplify the analysis.



(a) No-additional TL considered (b) Additional TL considered

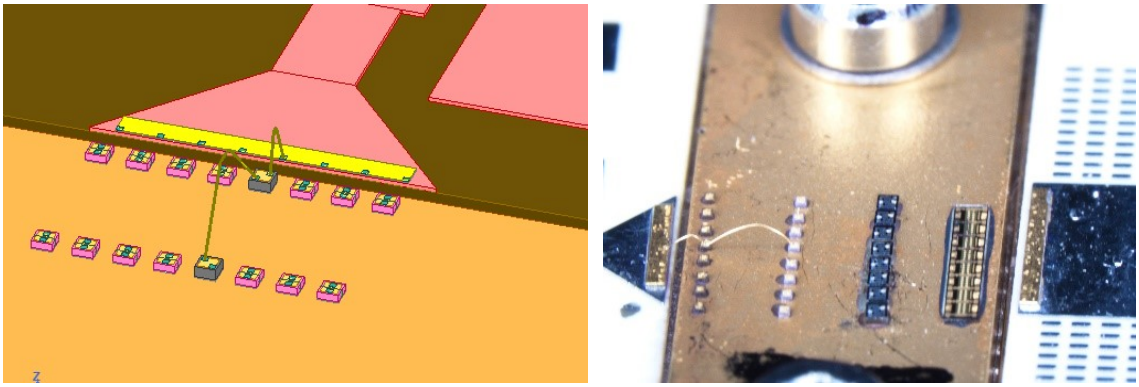
Figure 5.3: Input passive network S_{11} smith chart: taper open circuit



(a) no-additional TL considered (b) additional TL considered

Figure 5.4: Input passive network phase rectangular plot: taper open circuit

To be able to compare simulation versus measurement successfully, it is required to use the border capacitors values mounted in prototype 1 and to replicate the bonding wires shape in the 3D model, that is, border capacitors and bonding wires should be modeled and characterized individually before introducing them into the input passive network configuration shown in figure 5.5. This will be done in the following subsections, then, based on the obtained models, simulation versus measurement of the configuration 5.5 will be discussed.



(a) 3D model (b) Prototype 1

Figure 5.5: Input passive network: bonding wires and border capacitors

5.1.1 Border capacitors

Border capacitors 3D model can be easily constructed based on the information available on the data sheet provided by the manufacturer (Knowles). Figure 5.6 provides information for any given Part Number, then, its dimensions can be obtained in figure 5.7, observe that Length/Width, Pad Size and border are fixed values for each style (DXX) whereas Thickness may vary depending on the value of the capacity. Therefore, a model must be constructed, then, sweep its thickness until the desired value is achieved. Details about Dielectric constant and dissipation factor for each material can be found in the data sheet.

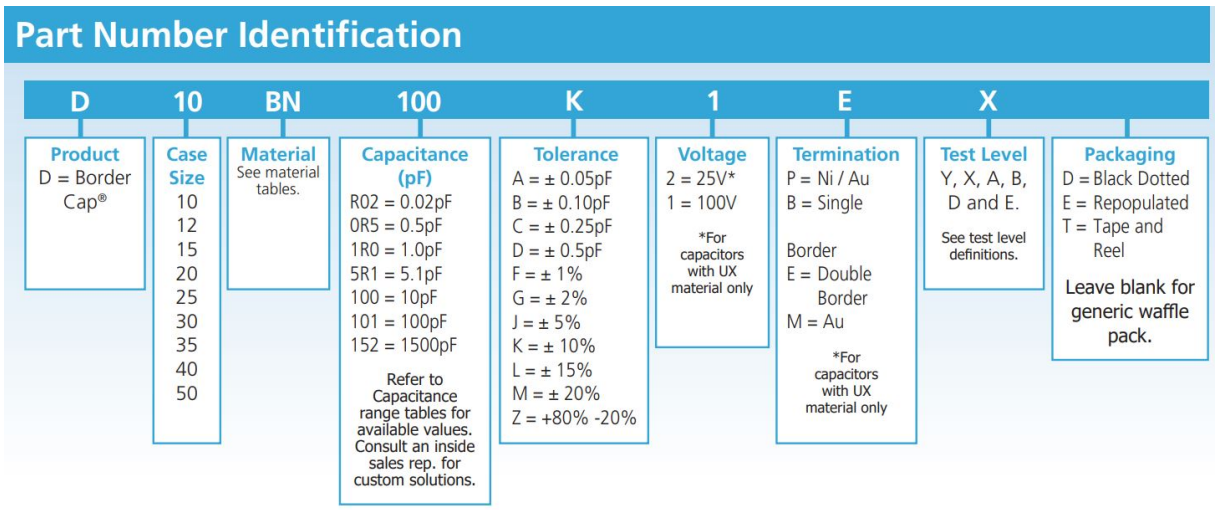


Figure 5.6: Border capacitors Part Number Identification

Dimensions

Style	Length / Width	Pad Size	Border	Thickness
D10	0.010" ±0.001" (0.254mm ±0.025)	0.008" (0.203mm)	0.001" (0.025mm)	0.006" ±0.0025" (0.152mm ± 0.064mm)
D12	0.012" ±0.001" (0.305mm ±0.025)	0.010" (0.254mm)	0.001" (0.025mm)	0.006" ±0.0025" (0.152mm ± 0.064mm)
D15	0.015" ±0.001" (0.381mm ±0.025)	0.011" (0.279mm)	0.002" (0.051mm)	0.006" ±0.0025" (0.152mm ± 0.064mm)
D20	0.020" ±0.001" (0.508mm ±0.025)	0.016" (0.406mm)	0.002" (0.051mm)	0.006" ±0.0025" (0.152mm ± 0.064mm)
D25	0.025" ±0.001" (0.635mm ±0.025)	0.021" (0.533mm)	0.002" (0.051mm)	0.006" ±0.0025" (0.152mm ± 0.064mm)
D30	0.030" ±0.001" (0.762mm ±0.025)	0.026" (0.660mm)	0.002" (0.051mm)	0.006" ±0.0025" (0.152mm ± 0.064mm)
D35	0.035" ±0.001" (0.889mm ±0.025)	0.031" (0.787mm)	0.002" (0.051mm)	0.006" ±0.0025" (0.152mm ± 0.064mm)
D40	0.040" ±0.001" (1.016mm ±0.025)	0.036" (0.914mm)	0.002" (0.051mm)	0.006" ±0.0025" (0.152mm ± 0.064mm)
D50	0.012" ±0.001" (1.27mm ±0.025)	0.046" (1.168mm)	0.002" (0.051mm)	0.006" ±0.0025" (0.152mm ± 0.064mm)

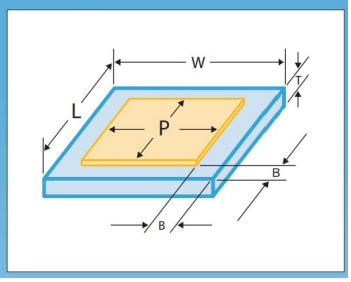


Figure 5.7: Border capacitors dimensions

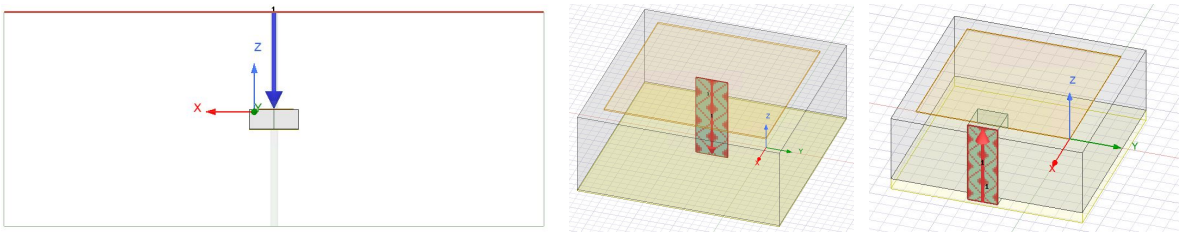
In addition to HFSS simulation of the input passive network, being able to simulate a single border capacitor 3D model leads us to obtain the electrical model by means of extracting the s2p (touchestone) file which can be used in ADS for SSPA full layout simulation. To characterize a single capacitor in Ansys environment, Q3D is the most optimal way to calculate capacitance (RLCG Matrix), however, it is not possible to obtain the s2p file. If a real model is needed, in addition to the capacitance, series inductance and resistance must be calculated, then, construct the model based on lumped elements, the limitation may come from the series inductance and resistance computation given that source and sink must be defined in the same conductor net (for more details refer to Q3D Ansys environment).

It is also possible to compute the capacitance using HFSS, There are several methods to calculate the C in this model, it is always necessary to previously calculate the C in the Output Variable, the defined expression will be used as a convergence criterion:

1. HFSS wave port: Laboratory setup can be reproduced where two probes are placed at each side (conductor pads). It is of great importance to define a deembeding on the ports with the length of the probes to reduce parasitic effects. figure 5.8a shows the described setup.

2. HFSS lumped/circuit port: it can be defined internally or externally. On one hand, the internal setup shown in 5.8b has a limitation, which is not being able to introduce the Lumped RLC, since it would overlap with the Lumped Port. On the other hand, for the external setup shown in figure 5.8c, two strips coming out of the component are created and an external connection with Lumped Port is defined. The problem with this

methodology is that it introduces a parasitic component to the two strips that can mask the results.Therefore this method is recommended for low frequency or higher C values. In this case the result is pF, so the parasitic effect can hide the real value.



(a) Wave port (b) Internal lumped/circuit port (c) External lumped/circuit port

Figure 5.8: Border capacitor simulation techniques

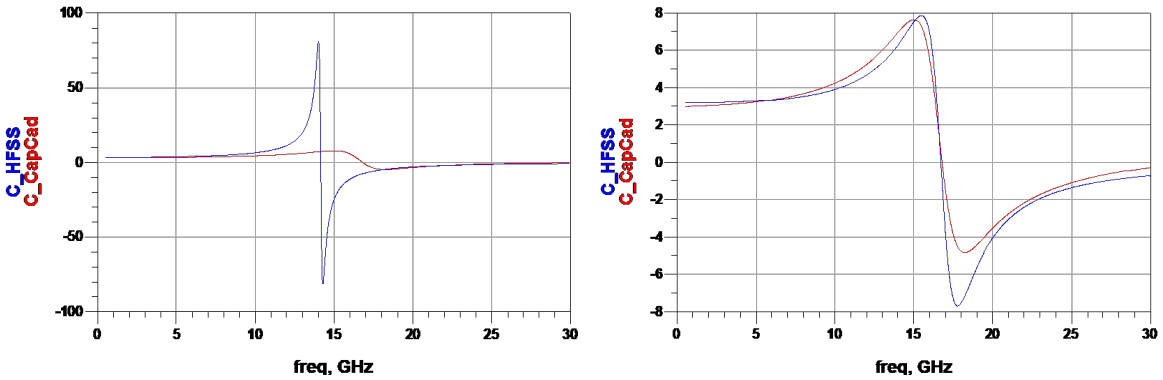
HFSS wave port have been identified as the best option for broadband simulation since the other solutions used in hfss (lumped and circuit port) don't simulate properly the Self Resonance Frequency (SRF), that is, the parasitic series Inductance and Resistance along frequency.

A good strategy for modeling border capacitors in 3D is starting with Q3D for determining the capacitance value based on the data sheet information, then, sweep the capacitor thickness until the desired value is achieved. Once the initial dimensions are determined, use hfss wave port setup to perform broadband simulation in order to extract the electrical model (s2p file).

A prof of work of the presented methodology can be demonstrated using a 3 pF border capacitor. C=3 pF is chosen given that the real model provided by the manufacturer is available to compare it with obtained results in HFSS. The described methodology have been carried out and the first results obtained when Wave Port setup is used are shown in figure 5.9a.

When using Wave Port setup, it is of great importance to consider that the surrounding box should be made as large as possible, however, if the box is too large the problem cannot be handled by the solver due to limited memory. The strategy to follow is to start with a reasonable small box and to increase the dimensions gradually until the computed capacitance/parasitic inductance, which have an impact on the self resonance frequency, does not depend on the box dimensions. Furthermore, in this case it can be observed that the Equivalent Series Resistance

computed by hfss dos not agree with real model since the simulated resonance is more abrupt, this comes from the dissipation factor (Tand) set in the material definition. The value used is the one given in the data sheet at 1 MHz, therefore, it must be correlated to achieve a response similar to the real model. Taking into account these considerations, a correlated model have been obtained where reasonable dimensions have been defined for the surrounding box and the dissipation factor at self resonance frequency (SRF) has been found to be $Tand_{SRF} = 13xTand_{1MHz}$. Correlated model results are depicted in figure 5.9b.



(a) Initial model

(b) Correlated model (Tand and surrounding box dimensions)

Figure 5.9: 3 pF Border capacitor: HFSS model versus Real model

The considered surrounding box dimensions and the correlated dissipation factor ($Tand_{SRF} = 13xTand_{1MHz}$) are applicable for any other D10 border capacitor value, therefore, such considerations will be taken into account for modeling the required capacitor values in the pre-matching network.

5.1.2 Bonding Wires

This section presents the modeling of arrays of bonding wires used in the SSPA prototypes. The SSPA prototypes contain 5 arrays of bonding wires, one on the drain side and four on the gate side (pre-matching network), each array has eight bonding wires in parallel. All the bonding wires are made from gold and have a diameter of 25um. In modeling, each bonding wire is represented by a specific number of straight segments (Piecewise aproximation), This is

illustrated in figure 5.10.

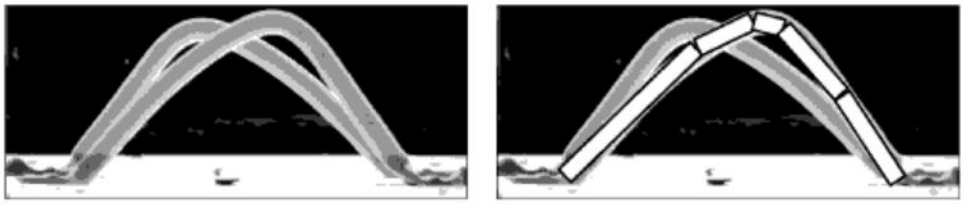
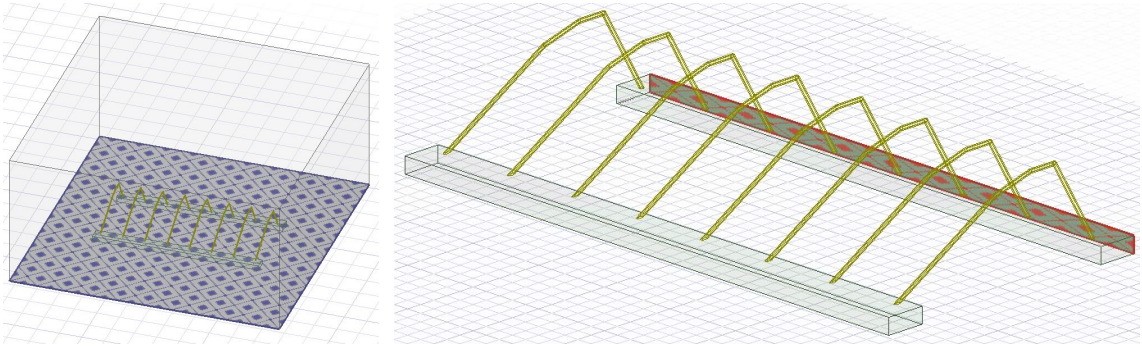


Figure 5.10: Piecewise Approximation of Bonding wires

Taking this into account, the geometry of the bonding wires with their corresponding length, heights above ground planes and separating distances between can be reproduced in HFSS. Figure 5.11a shows a 3D view of the geometry of the approximation detailed in literature [12]. In this picture, a box of vacuum with eight coupled bonding wires inside it is shown, the bottom of the box is a perfect ground plane. The bonding wires are from gold and they are connected together with a metal plate over a box of vacuum on the on the sides. Figure 5.11b shows a close view of the bonding wires and the lumped port 1 (highlighted) assigned on the side of the box of vacuum, port 2 (not-highlighted) is assigned on the side of the other box of vacuum.



(a) HFSS geometry (b) Closer view

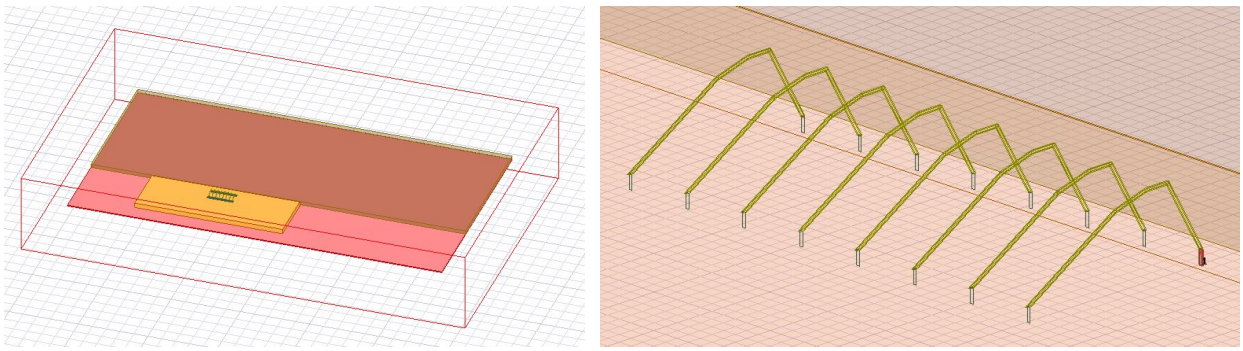
Figure 5.11: Bonding wires modeling: option A

Again, the box surrounding the bondwires should be made as large as possible. If the box dimensions are too small, the inductance computed is too low. If the box is made too large the problem cannot be handled by the solver due to limited memory or box resonances may occur. The strategy to follow is to start with a reasonably small box and to increase the dimensions gradually until the computed inductance does not depend on the box dimensions [12].

The inconvenience of this solution is that the metal plate connecting the bonding wires together acts as a parasitic capacitor which must be subtracted to the bonding wires model whenever it is used, mainly, such models were thought to be used in ADS in the SSPA layout simulation. To do so, it is necessary to extract the capacitance formed by the two plates by doing simple simulation for the geometry above without the bonding wires.

Even though the parasitic capacitance can be subtracted, it is preferable to avoid such computation in order to reduce ambiguity. Hence, another solution is proposed based on multiple lumped ports definition (at both sides of each bonding wire) as shown in figure 5.12b. This type of solution is ideal for this case where the objective is to obtain an electrical model (s16p file) which has 8 ports at each side (16 total ports) where the components of the pre-matching network will be connected. As an advantage, this kind of S-parameters matrix enables to obtain directly bonding wires coupling, mutual inductance, etc.

Furthermore, as it can be seen in figure 5.12a, real geometry (ground plane) is used instead of a sheet with a perfect conductor boundary as in solution A (figure 5.11a). This will provide accurate results in the correlation. In addition to the presented bonding wires array, the remaining arrays are modeled in the same way and their corresponding electrical model have been extracted in order to be used in ADS for the SSPA full layout correlation.

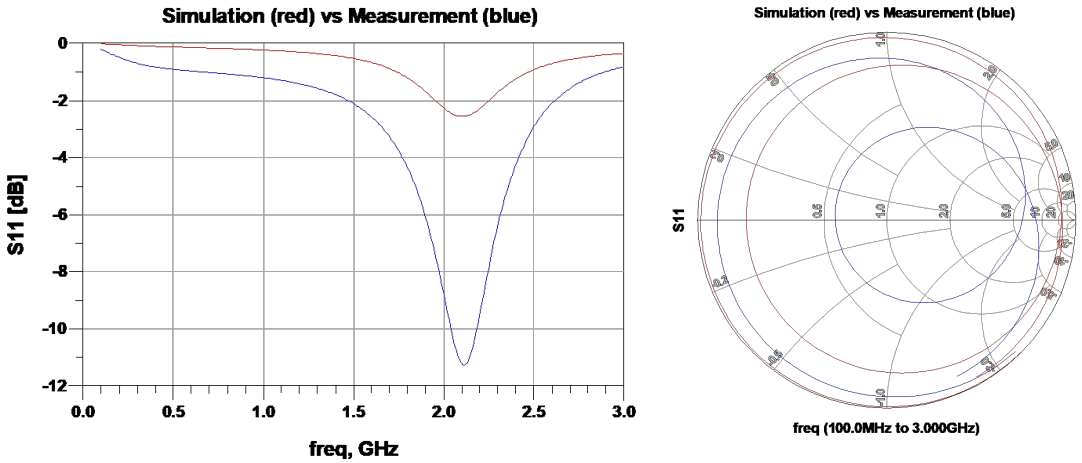


(a) HFSS geometry (b) Closer view

Figure 5.12: Bonding wires modeling: option B

Having obtained the 3D models of the Bonding Wires and Border Capacitors, it is time to go back to the input passive network correlation where a single row of Bonding Wires + Border Capacitors illustrated in figure 5.5 was considered. Now, it is possible to simulate the

input passive network using the corresponding model of each border capacitor value mounted in prototype 1 and the constructed Bonding Wires shapes. Simulation versus measurement results of figure 5.5 are illustrated in figure 5.13. As it can be observed, even though both simulation and measurement are centered at the same frequency, a disagreement in the S_{11} magnitude is detected. Observing the smith chart representation, it can be seen that such disagreement in the S_{11} comes from the impedance real part, that is, the mounted prototype has higher losses compared to simulated model. Therefore, additional losses must be considered in the simulation model to match the simulated response.



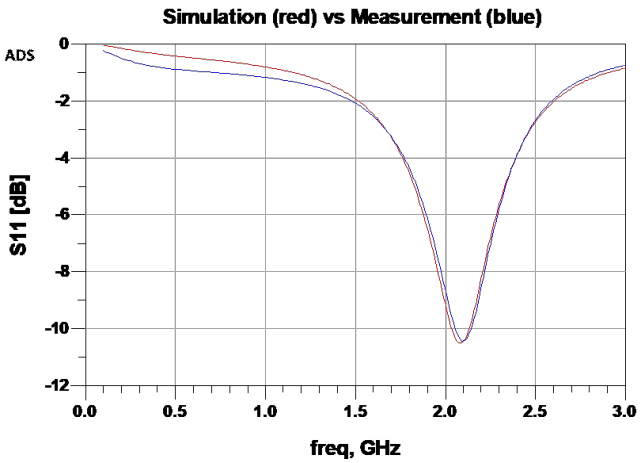
(a) Rectangular plot

(b) Smith chart plot

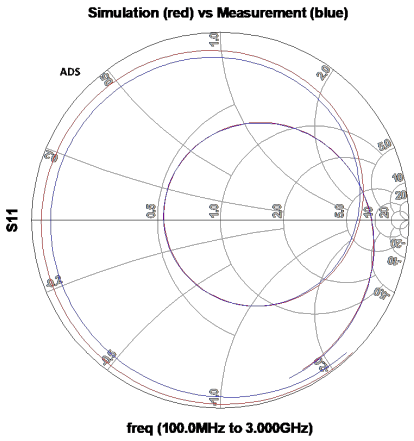
Figure 5.13: Bonding wires and border capacitors (figure 5.5) S-parameters

Adding losses can be considered in the simulation model by adding a series resistance to the ”Bonding wire + Border capacitor” Bloch. Doing so, it has been found that an additional 4Ω resistance should be considered in order to correlate the simulation versus measurement as illustrated in figure 5.14.

To better analyze the discrepancy detected in the simulated versus measured losses, the configuration considered initially in figure 5.5 have been simplified to the one shown in figure 5.15a where the bonding wire connecting first and second capacitor has been removed. Simulated versus measured response of the simplified version shown in figure 5.15a is quite similar to results illustrated previously in figure 5.14 and 5.14 for the initial version, where additional losses were required at the simulation level to meet the measured response. This is because the impact of



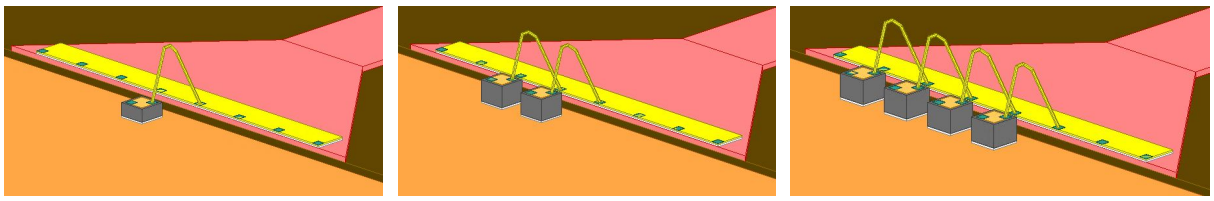
(a) Rectangular plot



(b) Smith chart plot

Figure 5.14: Bonding wires and border capacitors (figure 5.5) S-parameters

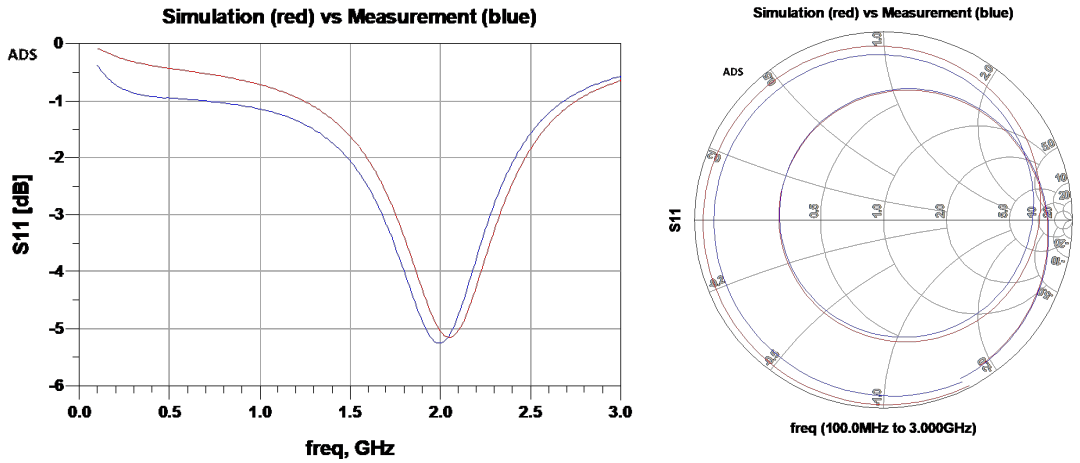
the removed bonding wire + second capacitor is negligible since the second capacitor has a very high value and behaves practically as an open circuit.



(a) Single connection (b) Two connections (c) Four connections

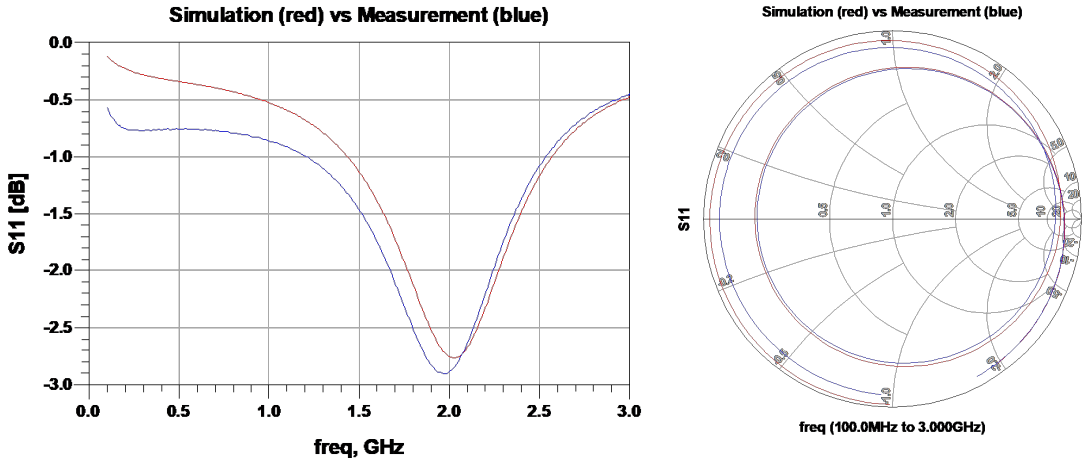
Figure 5.15: Bonding wires and border capacitors

In order to obtain more information, the problem is scaled up by means of considering more bonding wire connections as shown in figure 5.15b and 5.15c. Results obtained are shown in figure 5.16 and 5.15c, note that the 4Ω additional losses detected previously are considered at the simulation level. An important fact to highlight is that as the number of connections (Bonding wire + Border capacitors) increases, the discrepancy between simulation and measurement losses increases, such discrepancy is more notable at lower frequencies (around the frequency band of interest, 1.225 GHz) as it can be seen in figure 5.16 and 5.15c, smith chart representation enables to see such discrepancy in the impedance real part as the number of connections increases.



(a) Rectangular plot (b) Smith chart plot

Figure 5.16: Bonding wires and border capacitors: Two connections S-parameters



(a) Rectangular plot (b) Smith chart plot

Figure 5.17: Bonding wires and border capacitors: Four connections S-parameters

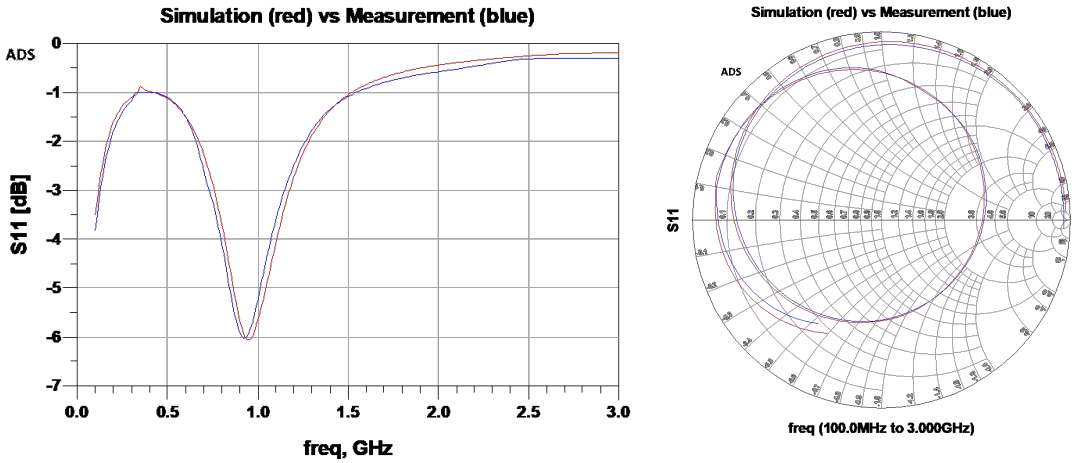
Higher discrepancy at the frequency band of interest means additional losses in the mounted prototype which must be considered at simulation level to correlate simulation versus measurement at frequency band of interest. This can be verified by modeling the full input passive network (measured response centered at 1GHz approx) which simulation versus measurement results were presented in the previous chapter in figure 4.12 where the input passive network was measured when the MMIC was extracted. Pre-correlation simulation model showed a frequency shift compered to the measurement response, however, using the 3D simulation models presented in this chapter (taking into account the 4Ω additonal losses) it has been found that both

simulation and measurement are centered at the same frequency but with different magnitude, this justifies the additional losses at lower frequencies observed previously as the number of connections increases. Figure 5.18 shows the correlated simulation versus measurement of the input passive network (MMIC extracted) considering more addional losses ($> 4\Omega$), observed that a good agreement between simulation and measurement is achieved .

The additional losses detected in the measurement which were not contemplated in the simulation model may come from different sources:

- Border capacitor dissipation factor: Even though the dissipation factor was correlated based on the 3pF border capacitor real model, it should be taken into account that the other values used are made of different materials which have different properties (Dielectric constant and dissipation factor). Therefore, such materials may have a different behaviour along frequency.

- Carrier assembly: different materials (CuMo, border capacitors, epoxy, foil, etc) used in the carrier assembly may be adding a common node series resistance to ground. A simpler carrier topology should be used for border capacitors testing in order to reduce the ambiguity.



(a) Rectangular plot

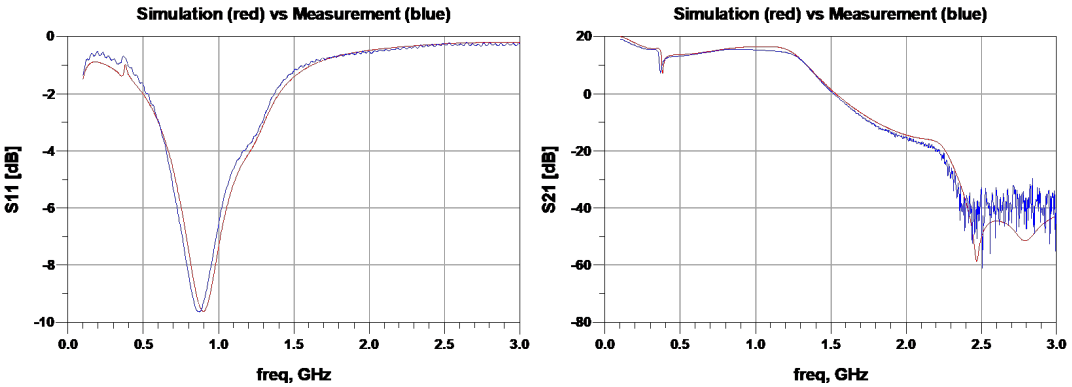
(b) Smith chart plot

Figure 5.18: Input passive network correlation (figure 4.12) S-parameters

5.2 SSPA full layout

Having correlated the input passive networks, it is time to consider the SSPA full layout in order to check the validity of the created electrical models and the supposed additional losses detected in the passive network correlation. Figure 5.19 shows the correlated simulation versus measurement results, observe that good agreement on both S_{11} and S_{21} is achieved.

Pre-correlation simulation versus measurement results presented in the chapter 4 showed a discrepancy in small signal gain (S_{21}) in addition to the frequency shift observed. Correlating the SSPA full layout, It has been found that the frequency shift is due to the bonding wires and border capacitors electrical models whereas gain discrepancy is due to the additional losses detected in the passive network.



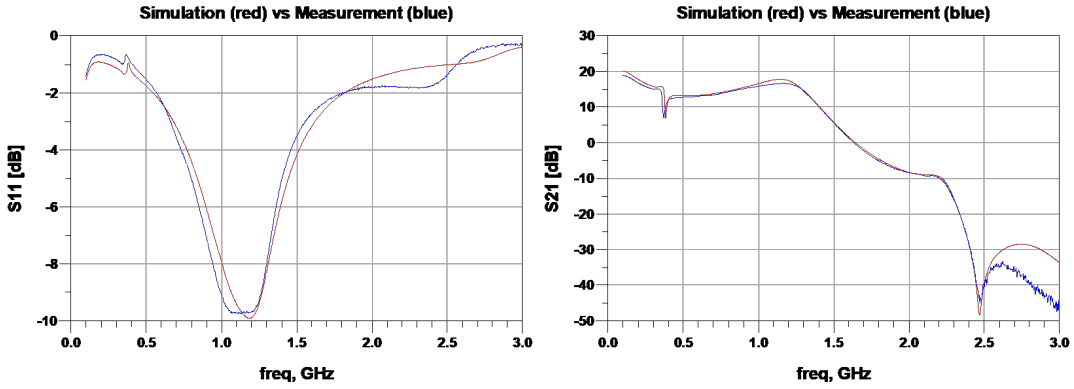
(a) S_{11} (dB) (b) S_{21} (dB)

Figure 5.19: SSPA small signal measurement correlation

Now, having correlated the SSPA full layout response, one should perform a final validation to the correlated model by performing a modification on both simulation model and real model (prototype) to verify if the agreement between simulation and measurement is still achieved. In this case, the modification is done with the aim of shifting back the SSPA small signal response to the design frequency. To do so, a tuning has been performed in the input matching network (LC) and it has been found that by modifying the value of the shunt capacitor is is able to achieve the desired frequency shift.

Figure 5.20 illustrates the simulation versus measurement results after modifying the value

of the input matching network capacitor, as it can be observed, good agreement is still achieved after the modification which means that the correlation has been performed successfully.



(a) S_{11} (dB) (b) S_{21} (dB)

Figure 5.20: SSPA small signal measurement correlation: input matching network tuning

Chapter 6

Conclusions and Future work

6.1 Conclusions

In this thesis, an SSPA complete product design and development has been proposed. Design simulation results showed a promising performance, however, initial test results of the first prototype showed a disagreement between simulation and measurements where small signal measurement response showed a frequency shift, in addition to the gain magnitude discrepancy (measured gain was very small compared to the simulated one). It has been found that the simulation model is uncorrelated with mounted prototype since a given change in the simulation model behaves differently when it is applied in the prototype. This caused a deviation in the work plan, instead of characterizing the SSPA in the large signal domain, priority has been given to correlation of measurements and simulation which has been performed from bonding wires and border capacitors to the SSPA full layout. The outcome of the performed correlation is successful since the reason of the frequency shift and the gain discrepancy are identified and corrected.

Throughout this thesis, In reference to the design phase, layout design rules and manufacturing processes understanding have been achieved as well as the reliability analysis according to ESA and NASA standards. The skills related RF/microwave design tools have been achieved successfully, moreover, the key aspects related to lumped elements modeling have identified and put into practise by creating the 3D models. In reference to the testing phase, test bench defini-

tion and RF instruments management is considered part of the learning outcomes of this thesis. Therefore, it can be concluded that the objectives initially established have been successfully achieved.

6.2 Future work

After correcting the frequency shift observed in small signal measurement by tuning the input matching network, it was still observed that the measured gain is small due to the additional losses detected in the correlation. This leaves the following topics for further development:

- Identify the source of the additional resistance. A simple carrier topology with a 50Ω access line will be used for individual border capacitors testing in order to verify whether the additional comes from border capacitors dissipation factor or the SSPA carrier assembly.
- SSPA large signal characterization. Given that additional resistance is detected in mounted topology, it is possible to reduce the total resistance by removing some of the chip resistors used to stabilize. That is, evaluate how much chip resistor it is possible to remove without affecting the stability. By reducing the total resistance, higher gain will be obtained and large signal characterization can be carried out successfully.

Bibliography

[1] A. Katz, J. MacDonald, R. Dorval, B. Eggleston, P. Drexler, and C. Liang, "High-efficiency high-power linearized l-band sspa for navigational satellites," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, pp. 1834–1837, 2017.

[2] M. Gilasgar, *Reconfigurable high efficiency class-F power amplifier using CMOS-MEMS technology*. PhD thesis, Universitat politècnica de catalunya, 2017.

[3] F. M. Ghannouchi and M. S. Hashmi, *Load-pull techniques and their applications in power amplifiers design*. Springer, 2011.

[4] G. Lloyd, "The maximally efficient amplifier, the april 2020 digital issue of microwave journal," *microwave journal*, April 2020.

[5] K. Chen, *High-Power Microwave/ Radio-Frequency Components, Circuits, and Subsystems for Next-Generation Wireless Radio Front-Ends*. PhD thesis, Purdue University, 2013.

[6] R. Giofré, P. Colantonio, E. Cipriani, R. Danieli, F. Giannini, L. Gonzalez, F. De Arriba, L. Cabria, and D. Baglieri, "A first step towards a 230w sspa for galileo system exploiting european gan technology," in *2015 European Microwave Conference (EuMC)*, pp. 1168–1171, 2015.

[7] R. Giofrè, P. Colantonio, L. Gonzalez, L. Cabria, and F. De Arriba, "A 300w complete gan solid state power amplifier for positioning system satellite payloads," in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, pp. 1–3, 2016.

[8] M. LaMarche, "Gan sspa technology for space-based applications," *microwave journal*, April 2019.

[9] D. M. Pozar, *Microwave engineering, Fourth edition.* Hoboken, NJ : Wiley, 2012.

[10] S. C. Cripps, *RF Power Amplifiers for Wireless Communications, Second Edition (Artech House Microwave Library (Hardcover))*. USA: Artech House, Inc., 2006.

[11] A. Grebennikov, "Load network design technique for class f and inverse class f power amplifiers," *HIgh Frequency Electronics*, vol. 10, pp. 58–76, 05 2011.

[12] EL-Rashid and Y. Tawk, "Current distribution in high rf power transistors," *University of Gavle*, 2007.