Universitat Autònoma de Barcelona

A Thesis for the

Master in Telecommunication Engineering

Characterization of RTN in FD-SOI transistor

by

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January 2021

El sotasignant, *Albert Crespo Yepes*, Professor de l'Escola Tècnica Superior d'Enginyeria (ETSE) de la Universitat Autònoma de Barcelona (UAB),

Fa constar:

Que el projecte presentat en aquesta memòria de Treball Final de Master ha estat realitzat sota la seva direcció per l'alumne *Daniel Bernal Cervera*.

I, perquè consti a tots els efectes, signa el present document.

Bellaterra, *data_de_sol.licitud_de_lectura*.

Signatura: *Albert Crespo Yepes*

Resum:

El projecte se centra en l'estudi dels transistors amb tecnologia FD-SOI per aportar i corroborar informació sobre la seva degradació a l'aplicar la inestabilitat de temperatures de tendència (BTI) i el canal de portadors calents (CHC). Aplicant als dispositius la tècnica d'estrès per voltatge constant, observant com evoluciona el seu comportament en la seva vida útil a més de centrar l'estudi en el soroll de telègraf aleatori (RTN).

Es comparen els resultats de la caracterització fresa i estressada dels dispositius per conèixer com varien després de diferents tensions d'estrès a partir de les corbes característiques I_G-V_G, I_D-V_G i I_D-V_D. A partir del mètode gràfic de retard de temps (W-TLP) s'aconsegueix identificar els nivells rellevants del RTN en què funcionen els dispositius en estat fresc i estressat.

Concloent que els efectes de la degradació en aquesta tecnologia afecten en el seu funcionament i aporta un augment del RTN en els dispositius.

Resumen:

El proyecto se centra en el estudio de los transistores con tecnología FD-SOI para aportar y corroborar información sobre su degradación al aplicar la inestabilidad de temperaturas de tendencia (BTI) y el canal de portadores calientes (CHC). Aplicando a los dispositivos la técnica de estrés por voltaje constante, observando cómo evoluciona su comportamiento en su vida útil además de centrar el estudio en el ruido de telégrafo aleatorio (RTN).

Se comparan los resultados de la caracterización fresa y estresada de los dispositivos para conocer como varían tras diferentes tensiones de estrés a partir de las curvas características I_G-V_G, I_D-V_G y I_D-V_D. A partir del método gráfico de retardo de tiempo (W-TLP) se consigue identificar los niveles relevantes del RTN en los que funcionan los dispositivos en estado fresco y estresado.

Concluyendo que los efectos de la degradación en dicha tecnología afectan en su funcionamiento y aporta un aumento del RTN en los dispositivos.

Summary:

The project focuses on the study of transistors with FD-SOI technology to provide and corroborate information on their degradation when applying Bia Temperature Instability (BTI) and Channel Hot Carriers (HCC). Applying the constant voltage stress technique to the devices, observing how their behaviour evolves during their useful life, in addition to focusing the study on random telegraph noise (RTN).

The results of the fresh and stressed characterization of the devices are compared to know how the transistors vary after different stress tensions from the characteristic I_G-V_G, I_D-V_G and I_D-V_D. From the method of time lag plot (W-TLP) it is possible to identify the relevant levels of RTN in which the devices work in fresh and stressed state.

The conclusion is that the effects of degradation in this technology affect their operation and provide an increase in the RTN in the devices.

Presentation

At the moment the demand to improve the requirements of the devices is in constant increase and new focuses are appearing where the necessity has been created to have a smaller consumption, a greater capacity of computation of processing that of greater speed of calculation, maintaining and reducing the cost. The current technology is advancing to meet these objectives and achieve prolong the life of devices batteries or exploit the possibilities of the Internet of Things.

In order to achieve these goals, work is being done to reduce the size of transistors. So far, there have been few complications when it comes to reducing them, but it is becoming increasingly expensive to reduce a few nanometres and to be able to comply with Moore's law, the actual limit where appears more problems is in 90 nm.

In this project analyses and test part of the feasibility of the FD-SOI technology, exactly the UTBB FD-SOI. Focusing on the degradation caused by the Bias Temperature Instability aging mechanism and the variability produced by the random telegraph noise observed on the channel current, with the aim of seeing how these devices age. Applying different set-ups to obtain the RTN and the temporal resolution that is found and comparing it in different periods of its useful life applying stress techniques. The main degradation applied is bias temperature instability although degradation by channel hot carriers has also been briefly studied.

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1. Introduction

The fully depleted silicon on insulator (FD-SOI) technology appeared just a few years ago to solve the problems in the technological advances of transistor downscaling. For many years it was not a big complication to reduce the size of the transistors with which great advances in performance were obtained and complying with Moore's law. Which mentions that the density of transistors doubles every 2 years approximately. [1] The actual limitation appears in the conventional transistors that do not manage to overcome the barrier of 90 nm successfully, reduced energy consumed in the devices by both vertical and horizontal scaling without affecting the performance, but now this is affected by problems such as short channel effects (SCE) and drain-induced barrier lowering (DIBL). FD-SOI innovation leverages the established planar process and Moore's Law compliance, which means no more complex manufacturing processes [2]. In addition, FD-SOI transistors promise a reduction in energy consumption along with a higher processing speed, more efficiently and less expensively. This technology covers a large part of the needs created by new devices that today's transistors cannot meet. Currently, energy storing is the great requirement to prolong the use of batteries, focused on the sectors of mobile devices and Internet of Things (IoT) sensors.

To ensure that this new technology is viable it is important to carry out a multitude of tests, some of which are carried out in this thesis to check unwanted effects such as noise, focusing on one in particular, random telegraph noise.

1.1 Objectives

The main objective of this master’s project is the study of the FD-SOI technology and how these devices are degraded by the Bias Temperature Instability (BTI). Moreover, the variability caused by the Random Telegraph Noise (RTN) is also analysed on the fresh devices and in a combination with the aging suffered, which could be affected by the damage produced in the device.

The main tasks of the project to achieve the objective have focused on:

1. Theoretical section where all the information necessary has been documented to know the causes of the degradation and the behaviour of the devices.
2. By means of the setup used to obtain the degradation and the random telegraph noise of the transistors to be analysed.
3. Analyse and compare the fresh characterization of the transistors to know the characteristic curves (I_G-V_G, I_D-V_G and I_D-V_D), the threshold voltage and the mobility depending on the dimensions (area) and the applied back gate.
4. Analyse and compare the stressed characterization of the devices depending on the dimensions and the voltages applied in the stress and comparing the stressed characterization with the fresh ones to observe the degradation.
5. Detect the RTN of the devices and apply a higher time window to detect the uncaptured RTN.

1.2 MOSFET transistors

In order to know how the FD-SOI transistors were obtained, the study is focused to the origin of these transistors and why this technology was used to solve the problems that emerged, these problems include degradation by bias temperature instability and channel hot carriers as an addition to undesired noise such as random telegraph noise. The operation of MOSFET transistors is briefly explained, as well as how to scale these transistors up to the limit with which one wants to work with the new transistors and what the disadvantages are that appear, such as degradation.

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a transistor that has an oxide metal gate electrode, which is isolated from the n or p channel (depending on the transistor, it can be seen in Figure 1) by an insulating layer like silicon dioxide. This gate has the property of applying resistance at the entrance of the channel (megaohms) when voltage is applied to it, thus affecting the channel, and giving the opportunity to control the current that passes through it [3].

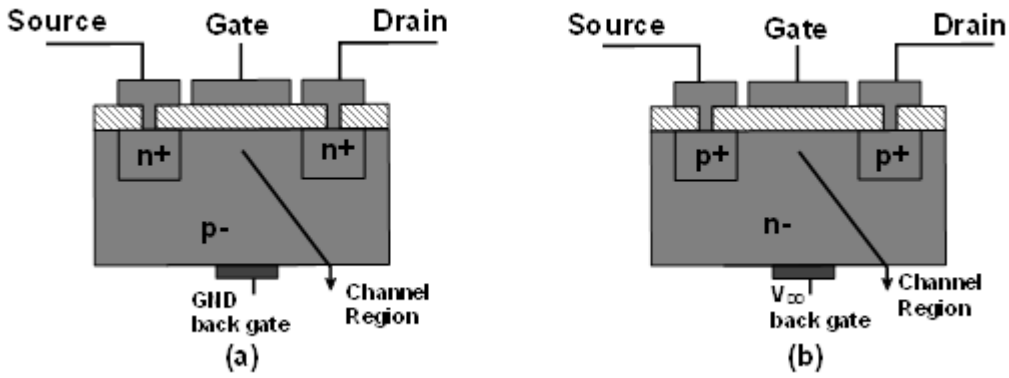

Figure 1 – MOSFET cross sections (a) NMOS transistor and (b) PMOS transistor [4].

The following tables show the different regions of operation for both P-type and N-type transistors, marking the limits of the different voltages applied to them and the region to which they work according to the applied voltage.

Regions of operations	NMOS	PMOS
Linear region	$V_{GS} > V_{TH}$ $V_{DS} \leq V_{GS} - V_{TH}$	$V_{GS} > V_{TH}$ $V_{SD} \leq V_{SG} - V_{TH}$
Saturation region	$V_{GS} \geq V_{TH}$ $V_{DS} > V_{GS} - V_{TH}$	$V_{GS} \geq V_{TH}$ $V_{SD} > V_{SG} - V_{TH}$
Cut-off region	$V_{GS} \leq V_{TH}$	$V_{GS} \leq V_{TH}$

Table 1 – Regions of operations to NMOS and PMOS transistors, where 'V' is the voltage and the sub-indexes mark whether it is the gate (G), the drain (D), the source (S) or voltage Thevenin (TH).

The formulas just described represent the following fig.2 where it can be seen a vision of where the transistors work (regions), it is worth mentioning that the ideal is that the transistors work in saturation but it depends on the desired application.

On the other hand, depending on the region in which they are working, the current is described with different dependencies. Table 2 and 3 describe the currents according to the linear and saturation region. It should be noted that for cut-off the current is equal to zero.

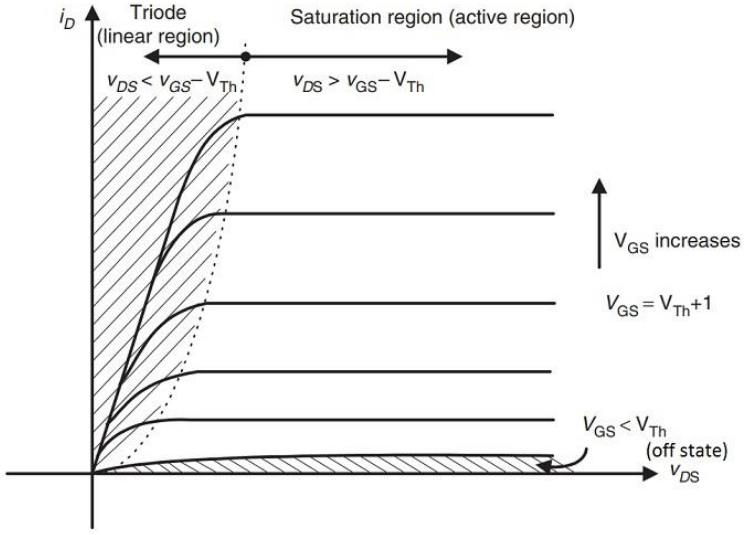

Figure 2 – MOSFET Regions of operations [5].

Regions of operations	NMOS Currents
Linear region	$I_{DSLIN} = \mu_n * C_{ox} * \frac{W}{L} * [(V_{GS} - V_{TH}) * V_{DS} - \frac{{V_{DS}}^2}{2}] * (1+\lambda V_{DS})$
Saturation region	$I_{DSSAT} = \mu_n * C_{ox} * \frac{W}{L} * (V_{GS} - V_{TH})^2 * (1 + \lambda V_{DS})$

Table 2 – NMOS Transistor currents for minimum output voltage.

Regions of operations	PMOS Currents
Linear region	$I_{DSLIN} = \mu_p * C_{ox} * \frac{W}{L} * [(V_{SG} - \lvert V_{TH}\rvert) * V_{SD} - \frac{{V_{SD}}^2}{2}] * (1+\lambda V_{SD})$
Saturation region	$I_{DSSAT} = \mu_p * C_{ox} * \frac{W}{L} * (V_{SG} - V_{TH})^2 * (1 + \lambda V_{SD})$

Table 3 – PMOS Transistor currents for minimum output voltage.

1.2.1 Scaling and principal problems in MOSFET transistors

Scaling is the process by which the size of devices is reduced to achieve greater performance at a lower cost, offering a greater number of devices for the same area, following the Moore's Law [1]. This scaling is achieved by reducing the thickness of the dielectrics which cause effects of oxide, interface, border traps in MOS gate oxides and leakage currents that are solved by applying new technologies both in manufacturing processes and materials. However, when the devices reach the nanometric level, their total-ionizing-dose (TID) response is usually more

complex and presents greater disadvantages [6]. TID appears when electrons and protons produce an overcharge in the dielectric layers used to insulate the devices. The effects they produce are cumulative and in a continuous exposure the degradation of the transistors appears [7].

Applying the downscaling on the devices many parameters are affected, such as, gate dielectric thickness, effective channel length, supply voltage and device leakage, reaching the limit. With all the effects that were appearing during the scaling, a series of physical, technological and economic challenges had to be met. The physical challenges highlight the materials that did not fulfil the task and the short channel effects (SCE), the drain-induced barrier lowering (DIBL) and the channel modulation effect, both the SCE and the DIBL are explained in more detail. On the other hand, another challenge to be overcome has been the dissipation of heat by the increase of devices in the same area. Technologically, manufacturing techniques have been generated to provide the appropriate resolution.

Horizontal scaling and vertical scaling are used to comply with the reduction of the devices. In the horizontal scaling it has the peculiarity that the long channel devices behave in a different way from the original, affecting the threshold voltage of the transistors depending on the length and width of the channel. In addition, the DIBL degrades the sub-threshold and the effective length is affected by the modulation of the channel length.

The vertical scaling affects the thickness which has to be proportional to the length of the channel. But this produces a current that degrades the impedance that particularizes the MOS by the electric field that is created, causing an increase in consumption and a decrease in performance [8].

1.2.2 Short-Channel Effect and Drain-Induced Barrier Lowering

Short-channel effects (SCE) in MOSFET devices are a phenomenon of manifestations that appear when the length of the channel obtains the same magnitude as the load regions: source and drain junctions with the substrate. This results in undesired performance, modelling and reliability behaviour. The results demonstrate a problem where drain-induced barrier lowering (DIBL) is included among several such as threshold voltage roll-off, velocity saturation,

mobility reduction or hot carriers effects. The performance is affected by these effects and makes its behaviour different along the channel, the solutions lie in options such as cutting the thickness of the gate, use of high-k dielectrics, it is worth mentioning that devices smaller than 90 nanometres are severely affected [9].

Drain-induced barrier lowering (DIBL) is a short-channel effect that appears in the short channel devices as long channel devices do not affect because they were sufficiently far away from the channel formation of the drain contact. In short channel transistors the drain manages to close the channel due to the distance they have and affects their behaviour.

Figure 3 shows how the short-channel effect is intensified by the polarisation of the drain, due to the drain induced barrier lowering [10].

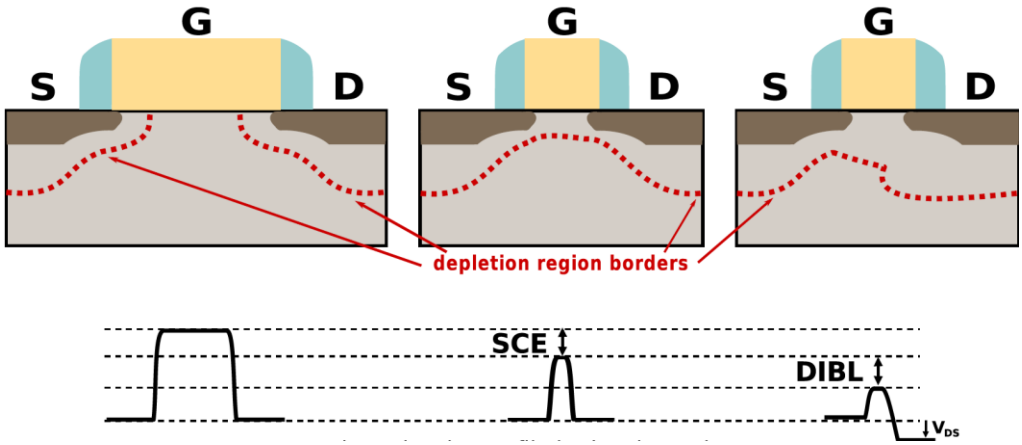

Figure 3: Effect by reducing the length of the transient gate affects the tension barrier by reducing it [10].

1.3 FD-SOI technology

FD-SOI Technology was created to cover the undesired effects of scaling and to be able to exceed the barrier of 90 nm for industrialisation which creates a limit in conventional technology. The disadvantages of scaling have been described in the previous point and are intended to be resolved with this new technology called Fully Depleted Silicon On Insulator (FD-SOI) which competes with Fin Field Effect Transistor (FinFET) technology.

Manufacturing transistors with FD-SOI technology drastically reduces the short-channel effect and the subthreshold leakage [11, 12], in addition to making the manufacturing process less complex. FD-SOI devices achieve a reduction in power consumption and leakage current by

applying a layer of undoped silicon to the gate and drain, thus achieving better control of the channel even if the gate length is shorter. In this way the performance is increased by the electrostatic control in the gate. Another advantage is the reduction of the threshold voltage variation in the manufacturing process [8, 10].

Figure 4 shows the different branches that were carried out to arrive at the technology that has been chosen in this thesis. It can be seen how silicon is used in the insulation, differentiating between them by the thickness of the layers, both of the upper part (t_{si}) and the thickness of the box (t_{box}). The first branch (PD-SOI) was eliminated due to the fluctuation of the threshold voltage, and the second (FD-SOI) was improved by reducing the box and becoming the Ultra-Thin Body FD-SOI (UTBB FD-SOI), which is the one being used in this project.

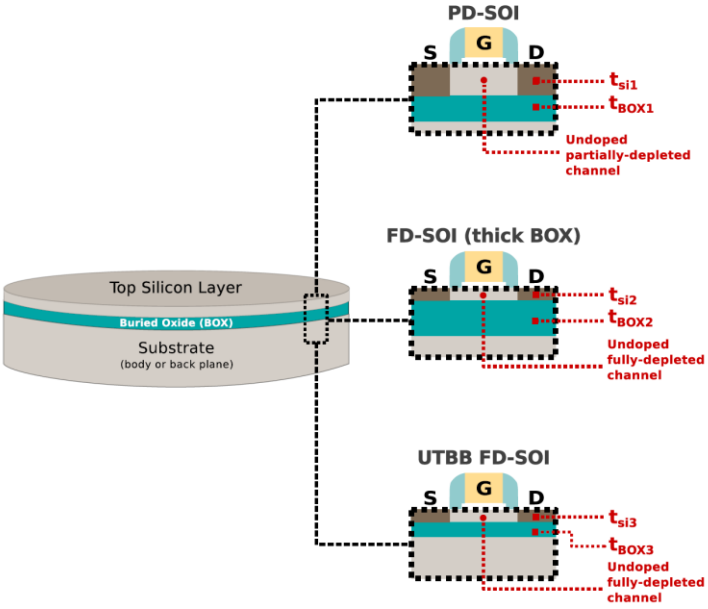

Figure 4: Evolution of FD-SOI technology [10].

In the Figure 5 show the current n-MOSFET devices against the UTBB FD-SOI to know the structure just described. Specify the thin layer of silicon found in the source, drain and substrate of the transistor. The leakage currents of the two transistors are shown in red, where it can be seen that the leakage currents of the junction disappear while the gate and subthreshold currents are reduced.

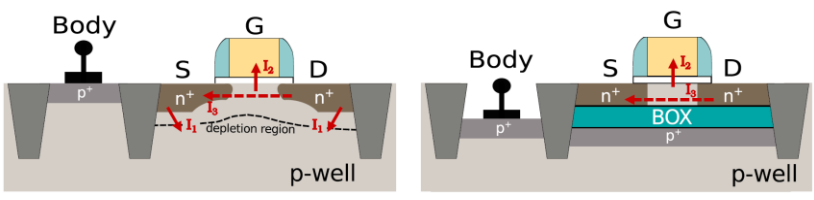

Figure 5: Typical n-mosfet transistor cutting compared to FD-SOI technology cross section [10].

1.3.1 Advantages of the FD-SOI technology

The thin top layer of the UTBB FD-SOI devices provide electrostatic control, this layer (t_{si}) must be one third of the length of the gate. By providing a reduction of the sub-threshold slope on the one hand, this parameter reflects the current control capability of the gate. While a reduction of the short channel effects (DIBL) is achieved due to the depth of the joints is t_{si}, which is lower than in conventional ones [13][14]. The comparison can be seen in Figure 6.a.

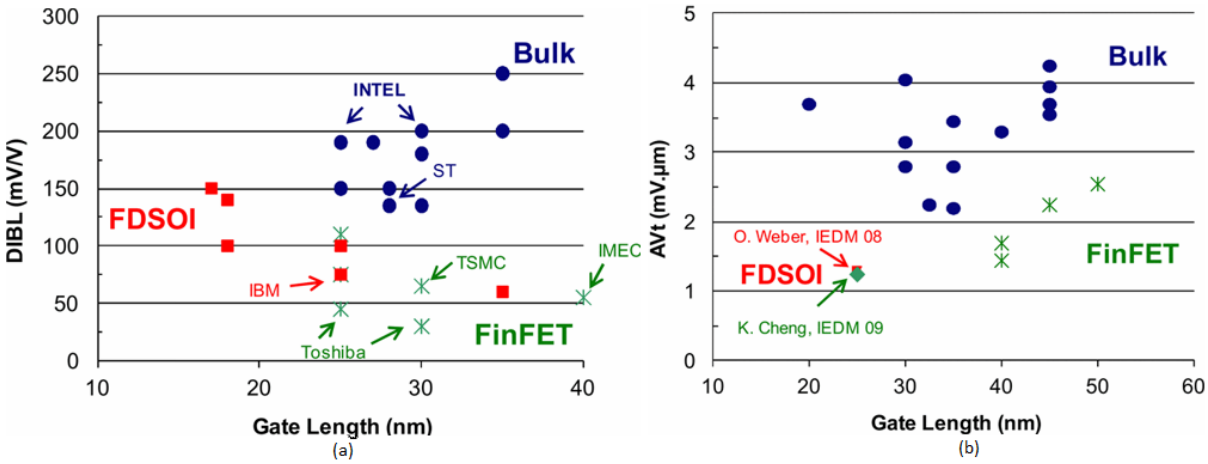

Figure 6: (a) DIBL measurements for different gate lengths for different technologies. (b) Threshold voltage measurement for different gate lengths for different technologies [15].

Furthermore, the UTBB FD-SOI technology box prevents channel doping by eliminating random fluctuations in doping (RDF) in the channel and reducing the variability of the threshold voltage. As shown in Figure 6.b, the V_{TH} variability is reduced by up to 3 times in FD-SOI technology compared to conventional transistors (bulk), thus obtaining less power difference [15]. FD-SOI technology works at a higher frequency than conventional ones, apart from limiting the drainage leakage induced by the gate, pA/µm levels [16].

The box eliminates the source/bulk current leakage to the substrate and allows for a reduction in static energy consumption [10]. It reduces the parasitic union capacity by reducing the diffusion surface because the depth of the source and the drain is limited [14].

1.3.2 Threshold voltage in FD-SOI technology

There is a great diversity of applications to be covered with a variety of transistors with different threshold voltages, FD-SOI technology must continue to provide the same range of opportunities.

To achieve the desired voltage thresholds on conventional transistors, the channel or gate-stack doping is varied [17], but on UTBB FD-SOI the doping cannot be increased because the variability increases and the gate-stack increases the price and process of manufacture. In this new technology, the substrate below the box is highly doped, and the V_{TH} varies according to this doping. Getting low level V_{TH} (LVT) and high level V_{TH} (RVT or HVT), for the high level the doping (RTV) is different from the source and drain doping, as shown in top Figure 7, while in LTV it is the same as shown in bottom Figure 7, known as flip-well. In the middle point there is a level, but it is close to LTV, it is the STV (standard), where it is not doped at all.

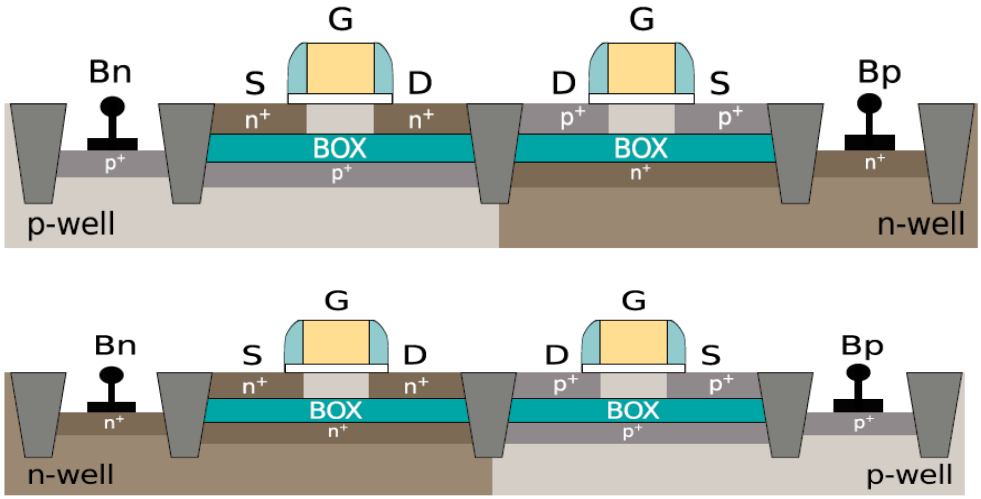

Figure 7: Top figure represents a NMOS and PMOS UTBB FD-SOI transistors configuration RTV transistor. Bottom figure shows NMOS and PMOS UTBB FD-SOI transistors configuration LTV transistor [10].

The threshold voltage of conventional transistors cannot be modified once they are manufactured but the UTBB FD-SOI has the possibility of applying a voltage to the back plane modifying the V_{TH}, adjustable during operation to improve frequency or consumption, known as body biasing [10] [19]. The body biasing is achieved by adding positive voltage in one n-well and negative voltage in the other p-well (in a NMOS transistor), achieving an excess of loads that makes the V_{TH} decrease. In the case of increasing V_{TH}, positive voltage must be introduced in well n and negative voltage in n-well (in a NMOS transistor) [20].

1.4 Aging and variability mechanisms

1.4.1 Bias Temperature Instability

Bias Temperature Instability (BTI) is a phenomenon that affects integrated circuits by degrading the electrical properties of MOSFET transistors. This degradation is caused by voltage and temperature conditions during operation, scaling of the transistor and the nitriding process in the gate dielectric to reduce leakage currents. Therefore, the aim is to design more robust circuits so that the effect of the BTI is as low as possible and this can be evaluated by characterising the effects of the degradation [21][22].

The degradation produced by the Bias Temperature Instability is associated with the gate dielectric, characterised by the threshold voltage (V_{TH}) as it increases along with other electrical parameters such as transconductance in MOSFET devices [23]. At high temperatures and high voltages in the gate is where their effects are most evident. As for the voltages applied to the gate, they can be positive voltage (Positive Bias Temperature Instability) or negative voltage (Negative Bias Temperature Instability), depending on the polarity.

The negative bias temperature instability in the pMOSFET reliability is relevant as they operate with a negative voltage in the gate to source channel. This affects an increase in threshold voltage, a decrease in mobility, current drainage, and trans-conductivity. While new technologies with high-k oxide gate materials, where positive temperature instability only works on NMOS transistors, where positive voltage is applied to the gate and nothing on the drain and the source, giving higher values are assigned to the threshold voltage. Figure 8 shows how both NBTI and PBTI are affected [8].

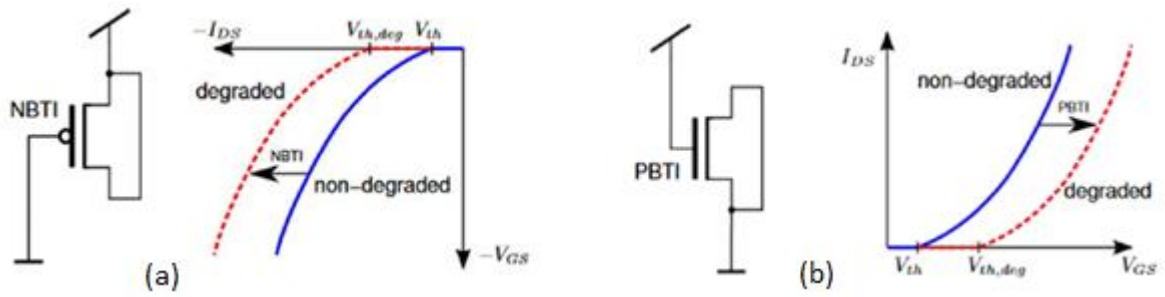

Figure 8: (a) NBTI to PMOS transistors degradation. (b) PBTI to NMOS transistors degradation [8].

In general, the effects of PBTI have always been less than the effects of NBTI. In SiON- and high-k based technologies, the increase in the threshold voltage in NBTI is associated with traps generated at the silicon and dielectric interface during stress, whereas the PBTI is proposed to be due to the charge trapped in the high-k material [22][24][25][26]. In the case of FDSOI technology, where the NBTI has been evaluated through the effect of substrate polarisation, power consumption and transistor operating frequency, a reduction of the NBTI has been obtained [23]. On the other hand, FinFET technology competes with it and also achieves a considerable reduction in BTI [28].

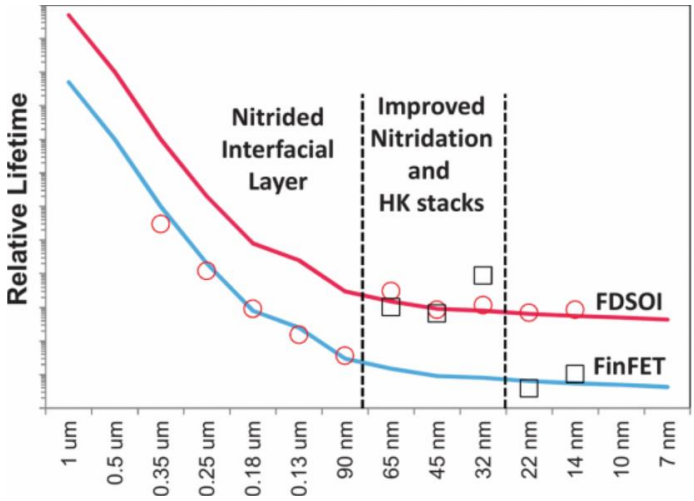

Figure 9: Relative lifetime in FDSOI (red line) and FinFET (blue line) technology when applying NBTI stresses for different channel lengths [29].

In order to obtain the BTI experiment, the I_D-V_{GS} curve must be characterised in a fresh and stressed way. When referring to a fresh characterisation, it is when the device has not been manipulated (Time 0) while the stressed is detached from applying certain tensions in time. In order to obtain this information, the source, drain and bulk connections are connected to ground, while the gate receives high voltages to achieve an accelerated degradation so that the experiments can be carried out in a reasonable period of time.

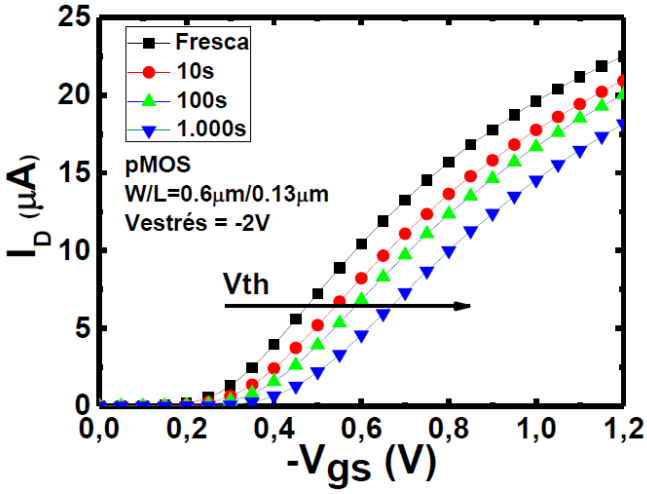

Figure 10: I_D-V_{GS} characteristic curve after applying a constant NBTI stress, in times of 10s, 100s and 1000s [22]. Displacement of the $V_{TH.}$

The variation of the threshold voltage varies as a constant high voltage is applied to the gate. This type of stress is called Constant Voltage Stress (CVS) which will be deepened at the next point.

1.4.1.1 Constant voltage stress

Constant voltage stress (CVS) is typically used for experiments focused on knowing the useful life of transistors, creating a projection which can be extrapolated to reality due to accelerated testing. This type of stress is able to measure the temporal evolution of the bias temperature instability (BTI). It should be noted that complementing this type of stress with ramp voltage stress offers an extrapolation of the useful life according to the conditions of use. It is important to know the evolution BTI because it offers knowledge of the dielectric degradation that limits the transistors and that is why this new alternative of the FD-SOI transistors. [30]

It would take a long time, months and years, to know the life span of the devices being studied, to obtain the results. But the constant voltage stress tests accelerate this process to observe the degradation and the breakdown of the transistors, obtaining test times of only hours or days (reasonable stress time) thanks to the increase of the drain in the gate above the required value. The results obtained with these tests help to clarify the reliability of the devices.

In this project is focused on this type of stress in order to know the degradation of the UTBB FD-SOI transistors, by introducing a voltage in the gate of different voltages to achieve relevant results.

Returning to the figure previously shown (Figure 10) to which the stress just described has been applied, it can be mentioned that its curves follow the following variation of the threshold voltage:

$$\Delta \mathrm{Vth} = \mathrm{A} * t_{stress}^{b} \qquad \text{(eq. 1)}$$

Where the parameters 'A' and 'b' are governed by transistor technology, temperature, and applied stress voltage. Thus, Figure 10 shows the temporal evolution of the variation of the threshold voltage (V_{TH}) when the NBTI is interrupted at a constant voltage and at different temperatures [31].

1.4.1.2 Recovery of the BTI

Another characteristic is that when stress voltage is no longer applied to the transistor gate, the threshold voltage begins to recover temporarily (BTI relaxation, it is reduced as time passes). It is important to emphasize this point of the theoretical study because in this work this recovery will be observed quite a lot in the results.

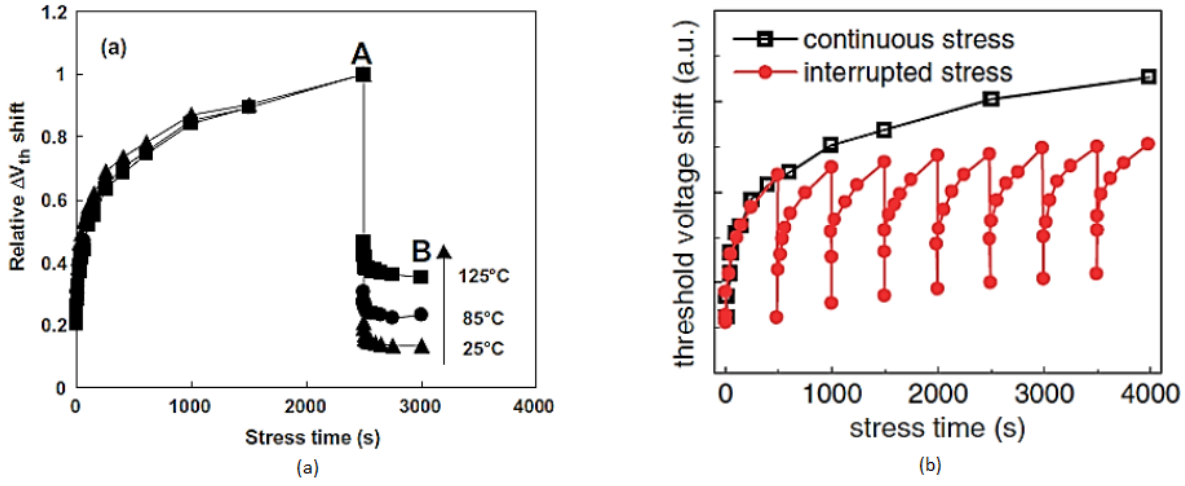

Figure 11: Figure (a) shows how stress is removed from t = A for different temperatures. Figure (b) shows in red several interruptions of the stress and in black a continuous stress, showing that the threshold voltage ends up being higher in the range because there is no recovery [32].

1.4.2 Channel Hot Carriers

Channel Hot Carrier (CHC) degradation, also known as Hot Carrier Injection (HCI), is a degradation of the transistor gate that impairs its threshold voltage, saturation current and transconductance. The CHC is another aging mechanism associated to the gate dielectric (like the BTI) and is produced as a consequence of the current that circulates through the device channel. This happens when the voltage at the gate is higher than the threshold voltage and in addition the drain has voltage applied. When the drain voltage exceeds the saturation voltage of the drain, the carriers that reach the pinch-off are accelerated by the electric field. Some of these carriers generate electron-hole pairs in the region near the drainer. If a large electric field is added, these are injected into the dielectric of the gate and end up degrading it, suffering an undesirable variation [22].

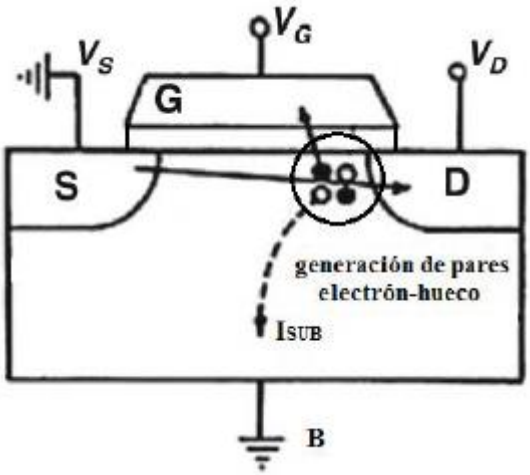

Figure 12: Electron hollow pair near the drainer during channel hot carriers stress [33].

The maximum CHC degradation of a device depends on the length of its channel. In addition to the fact that the most used parameter for quantifying channel hot carriers and substrate current, this current is measured when voltage is applied to the drain and gate of the transistor. When the substrate current is maximum, it means that the degradation will also be maximum [22].

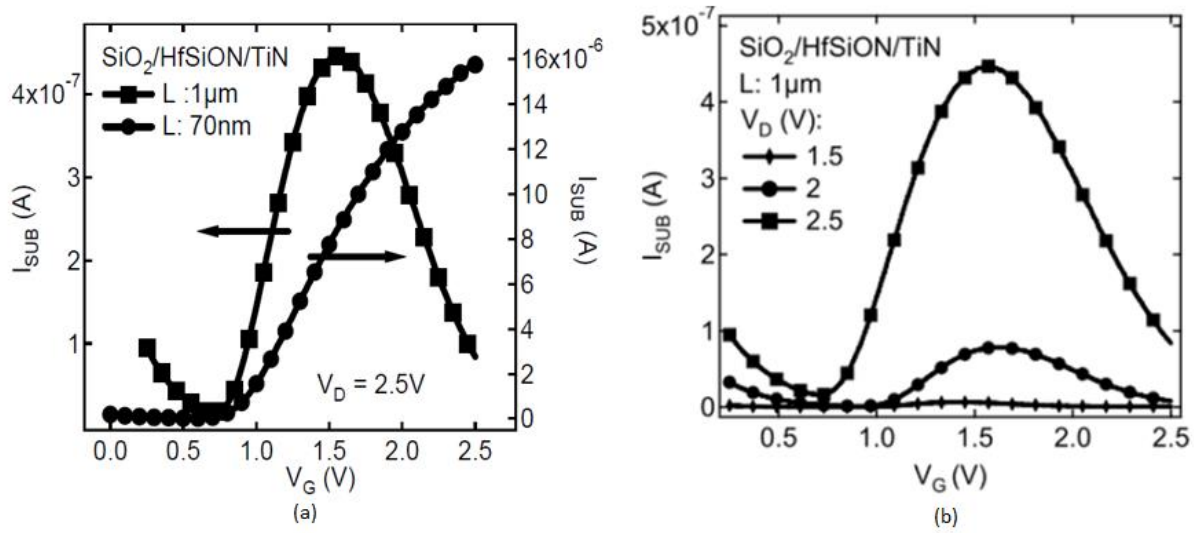

Figure 13: (a) Maximum degradation per short and long channel hot Carrier [33]. (b) Substrate current for different gate voltages [34].

So it can be concluded that for a long channel NMOS device (1µm) the maximum degradation is obtained when the voltage at the gate is half that of the drain. While for a short channel n-MOS device (70nm) its maximum degradation is obtained when the gate voltage is equal to the drain voltage [34].

It also has a recovery period, so the threshold stress starts a recovery process, and its speed depends on the applied stress conditions.

1.4.2.1 Bias Temperature Instability and Channel Hot Carriers simultaneously

The total degradation of the gate is divided into the BTI and CHC components. BTI near the source and CHC near the drain, the predominance of one over the other depends on the stress conditions (gate and drain voltages, temperature, and type of transistor).

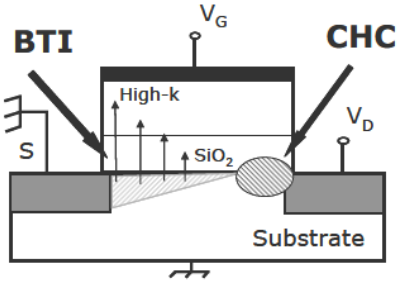

Figure 14: Degradación BTI y CHC simultáneamente. [33].

1.4.3 Random Telegraph Noise

Random telegraph noise (RTN) is the cause of nanoscale electron device failures that affect device performance and should be studied carefully. It is a kind of electronic noise that appears as fast transitions of a measured quantity. [35]

It is a low-frequency noise that increases as the size of the device decreases, manifested as fluctuations in the channel current and threshold voltage between different discrete levels. These fluctuations are due to the capture and emission of carriers on the channel [36].

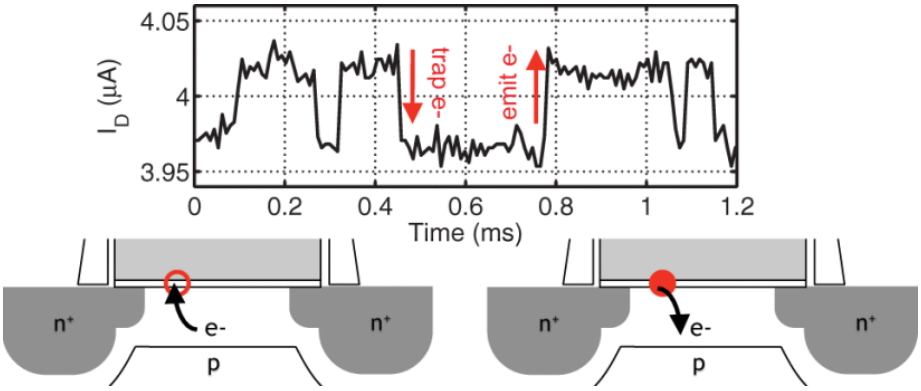

Figure 15 - Two-level RTN waveform along with an illustration of the underlying carrier trapping process. [36].

The study of this noise serves to know the failures in the physics and reliability of the devices, through the set-up that will be explained in the following point, the experiments are automated obtaining data analysis, verifications and simulations **[**37]. The measurements will be performed from the different inputs and outputs of the transistors to know in detail the transistor when it is new (fresh) and after applying the stress techniques, to compare the behaviour and find the defects that appear.

Then, due to the random telegraph noise are not able to maintain a constant current for a MOSFET transistor working in inverted mode with FD-SOI technology, it is due to the random exchange of the charge with the substrate. As can be seen in Figure 16, fluctuations in the value of the current are shown, where from now is focusing on its analysis in order to know these defects. These defects directly affect the threshold voltage and give a behaviour which is not ideal. Furthermore, these defects follow a Poisson distribution where in small areas discrete levels appear.

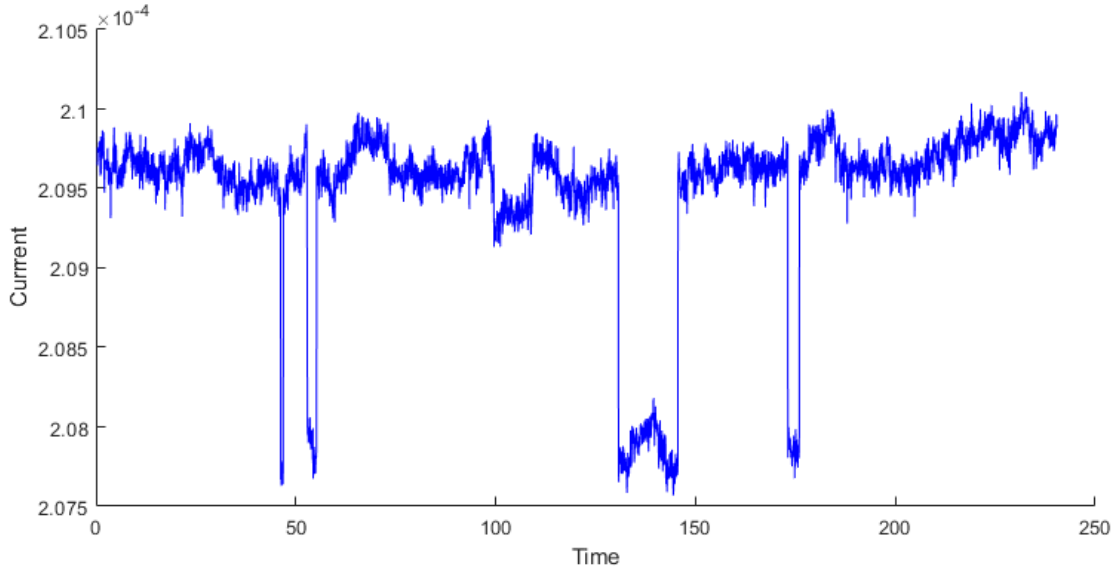

Figure 16 - RTN example obtained in the measurement.

2. Samples used and set-up

In this section, the thesis focuses on the development carried out in the experiments to know the RTN of the FD-SOI transistor in the fresh state and how it evolves in later stress states applied.

It will be described which set-up is used to obtain the measurements, the processes implemented together with the characterization of the parameters to be evaluated and finally the measurements obtained for their later analysis.

2.1 Principal characterizations processes

2.1.1 I_G-V_G Characterization

To obtain the I_G-V_G characteristic curve, the current that moves through the gate when a voltage is applied to the gate must be measured. This voltage varies in order to carry out a sweep and to know the current values. While the rest of the terminals are connected to the ground.

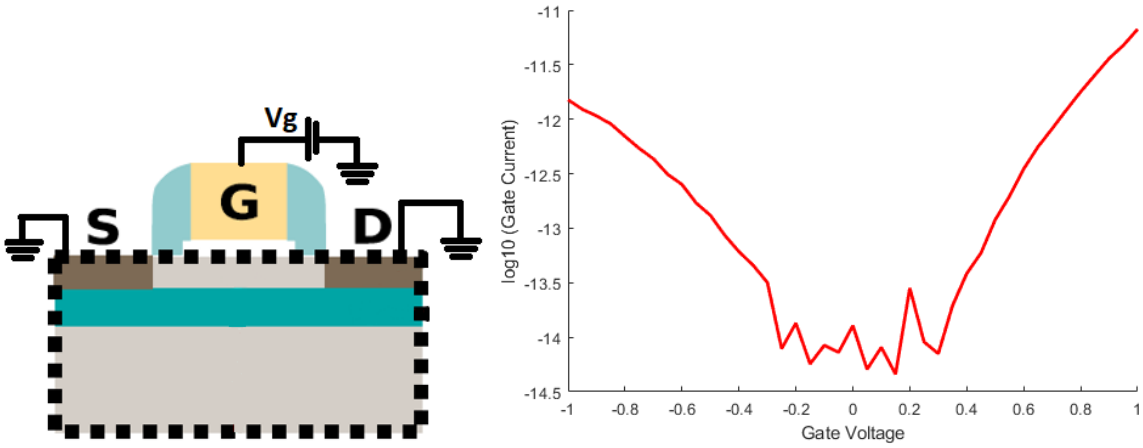

Figure 17 - Left figure represents the terminal connection and right figure shows the characteristic curve I_G-V_G obtained by changing the voltage applied to the gate.

This characterization shows the degradation of the gate oxide, where a fresh device will show less current than a stressed device. Figure 17 shows how the UTBB FD-SOI transistor is connected and the characteristic curve that can be obtained. Obtaining a curve model of a correct operation.

2.1.2 I_D-V_{GS} Characterization

The I_D-V_{GS} characteristic curve is achieved by measuring the I_D current when a voltage sweep is applied at the gate and constant voltage is applied to the drain. While the rest of the terminals are connected to ground. The threshold voltage is the voltage applied in the gate that gives current to drain.

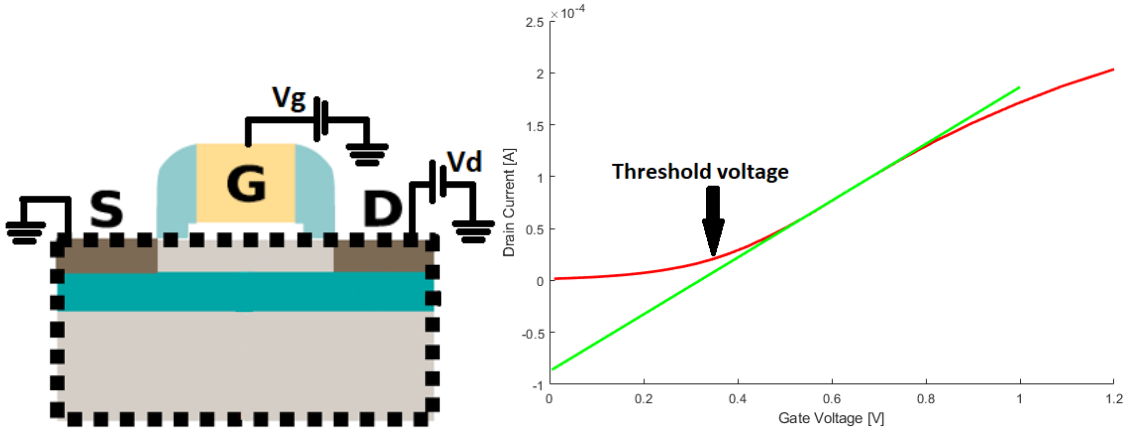

Figure 18 - Left figure represents the terminal connection and right figure shows the characteristic curve I_D-V_G obtained by changing the voltage applied to the gate where can be appreciate the threshold voltage.

2.1.3 I_D-V_{DS} Characterization

The representation of this curve belongs to the current of the drain together with the sweep of the drain voltage while different constant voltages are applied in the gate, the rest of the terminals connected to ground.

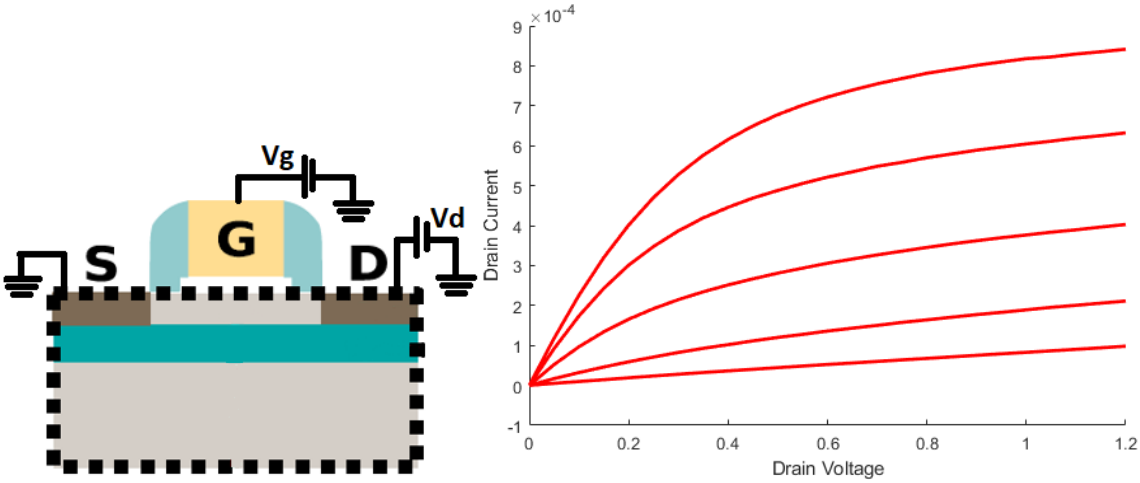

Figure 19 - Left figure represents the terminal connection and right figure shows the characteristic curve I_D-V_D obtained by changing the voltage applied to the drain.

This characteristic curve corresponds to Figure 2 of this thesis where the different working regions of the transistor are shown. If the constant voltage of the drain is low, it will work in the linear region and if it is lower than the threshold voltage it means that it is in cut-off.

2.1.4 RTN Characterization process

This section explains the procedure used to obtain the RTN. It is not always possible to observe RTN from the graphs that are obtained. In some cases, it is necessary to work on the information obtained because the background noise masks the current changes that the RTN involves. In case of not using and investigating the RTN detection processes, the defects are not detected.

Two types of analysis then appear, the first where the RTN is not masked by the background noise and the second where the RTN is hidden in the background noise. In the first case to identify the random telegraph noise the Time Lag Plot (TLP) is used. The TLP draws a series of ‘i’ data plus the next ‘i+1’, so that the traps can be displayed [38][39].

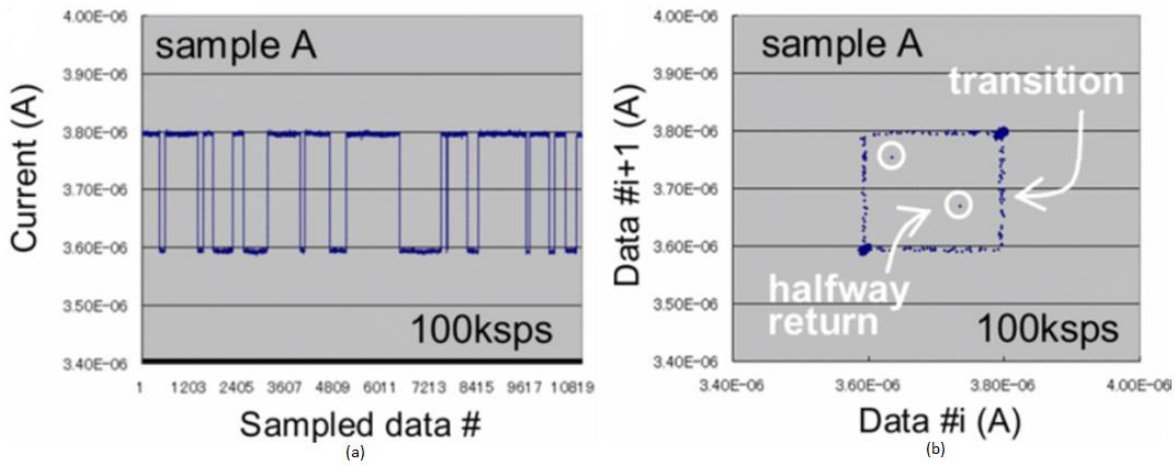

Figure 20 - (a) It is a waveform with two levels, the first level is at 3.80 µA and the second level at 3.60 µA. (b) In the figure give a vision of the TLP that shows two states (2 levels described in (a)), plus points that it has detected in the middle of a transition. [38].

The process described above can be seen in Figure 20 where the TLP chooses the samples obtained from the experiment and graphs them, obtaining the number of levels that the RTN has and the path of the transitions. This process manages to obtain a mapping of the transitions and the level in which the defect is found Figure 21.

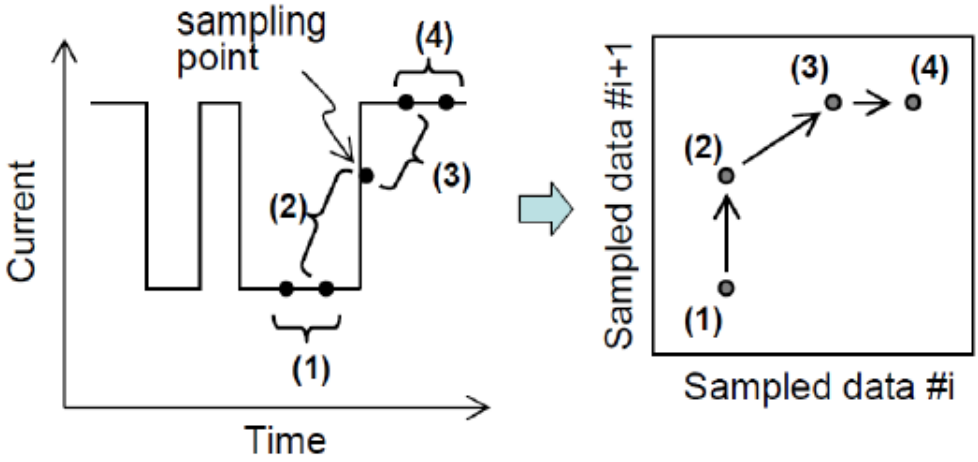

Figure 21 - Explanation of Time Lag Plot (TLP) [38].

The second case, when the RTN is hidden by background noise as shown in Figure 22, uses the Weighted Time Delay Method (W-TLP). This method expands the TLP by minimizing the effect of noise on the RTS, allowing a more accurate extraction of the parameter.

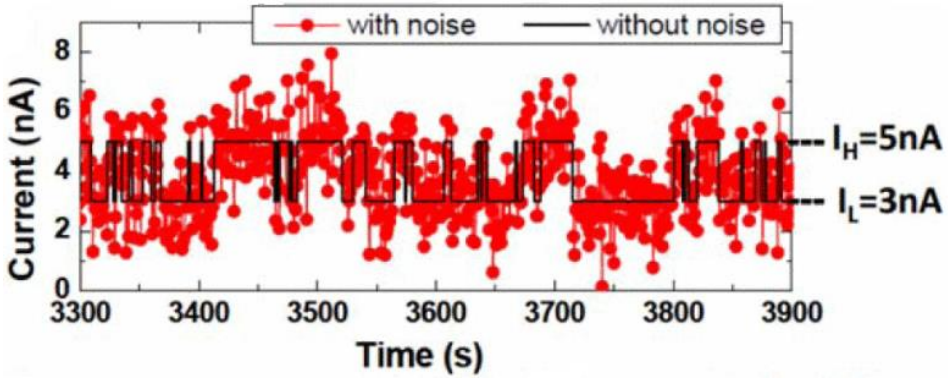

Figure 22 - RTN hidden by background noise [39].

The process consists of marking the coordinates (i, i+1) and defining the equation ϕ_i (x,y). Eq.2 is a bivariate normal distribution with an 'alpha' deviation and a correlation coefficient of zero, representing the probability of corresponding to a level or transition [8][39].

$$\phi_i(x,y) = \frac{1}{2\pi\alpha^2} * \exp\left(\frac{(I_i-x)^2+(I_{i+1}-y)^2}{2\alpha^2}\right) \quad \text{(eq. 2)}$$

The weighted time lag equation is defined as eq. 3, where the value of 'K' which is constant is to normalize the maximum value to '1' and N is the number of points in the RTS. Giving the STR or TLP histogram.

$$\Psi(x,y) = K\sum_{i-1}^{N-1}\phi_i \qquad \text{(eq. 3)}$$

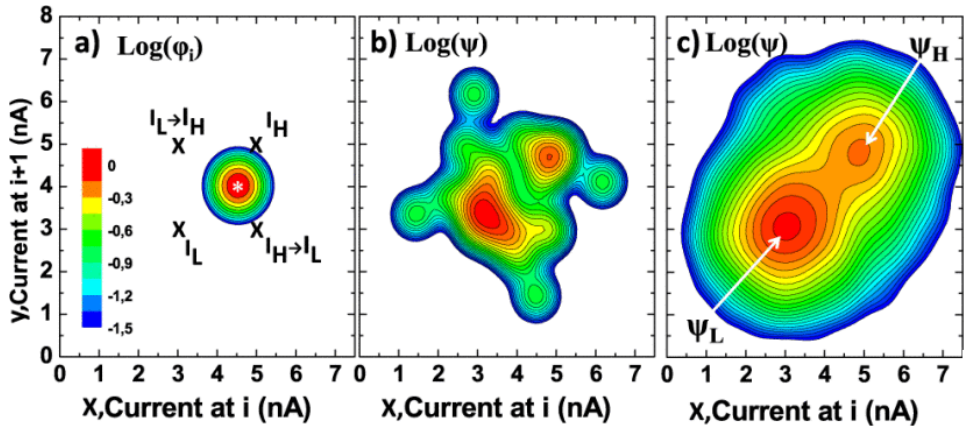

Figure 23 - (a) Representation of Log (ϕi), (b) representation of Log (Ψ) and (c) the full RTS trace [39].

Another information to be highlighted to finish this point is that the RTN can have multiple levels that must be contemplated in the analysis as shown in Figure 24. On the other hand, another parameter that is usually studied in the RTN is the time in which this defect prevails in its level as shown in Figure 25.

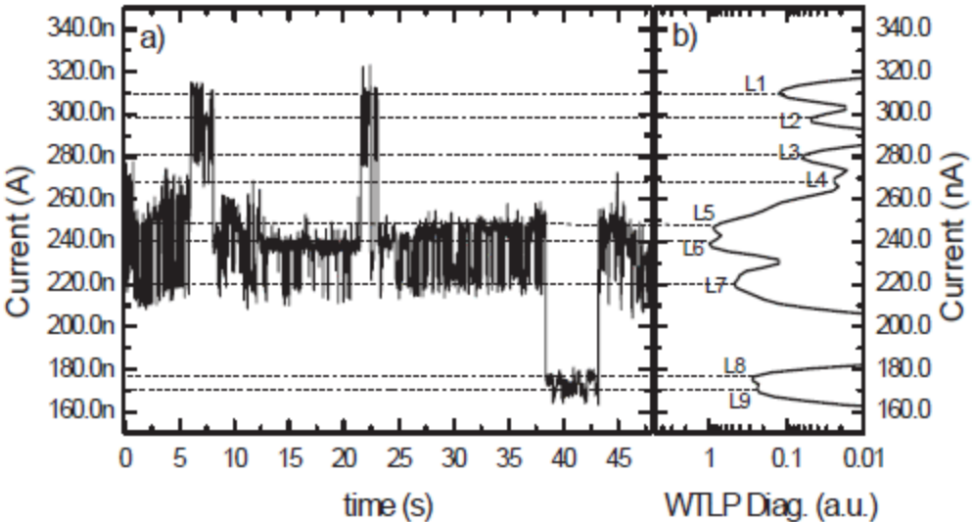

Figure 24 - (a) Typical multilevel RTN signal measured with a semiconductor parameter analyser. V_{APP}=1.25V, step time ~6ms and number of measured points 8000. (b) Trap levels obtained by using the W-TL method [40].

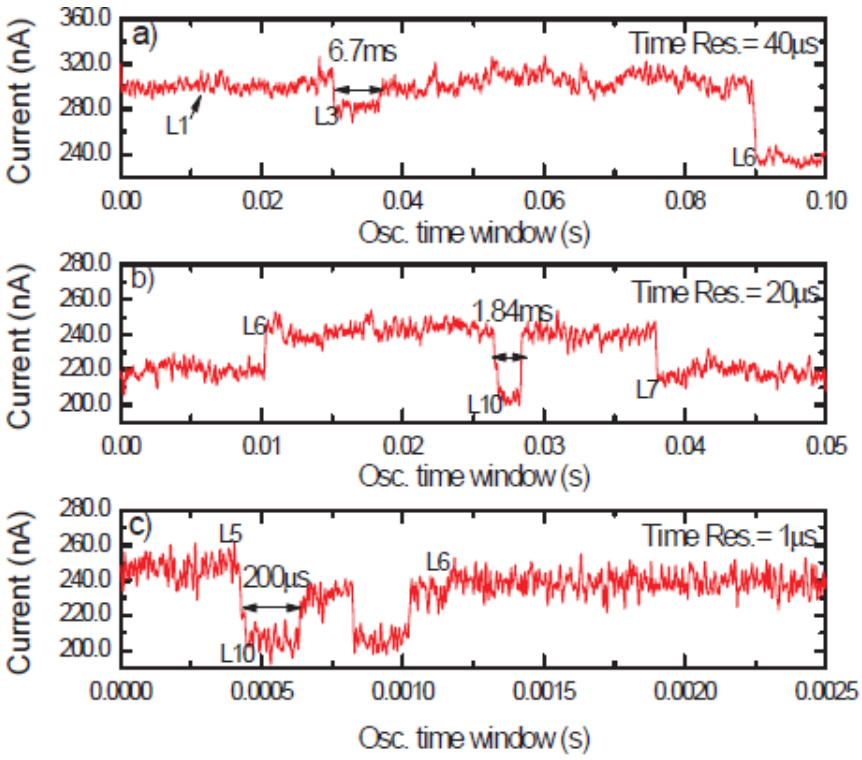

Figure 25 - Oscilloscope traces captured in different time window, obtaining the interval time of a deffect [40].

2.2 Samples

The transistors used were manufactured by CEA-LETI (Laboratoire d'électronique des technologies de l'information). With a buried oxide thickness of 145 nm (tox, UTB) in SOI wafers where the gate stack is composed by HsSiON/TiN (EOT=1.2). They have a width of 200 nm up to 10 nm (WNW) and a height that goes of 11 nm (HNW), observable in the Figure 26 [41][42].

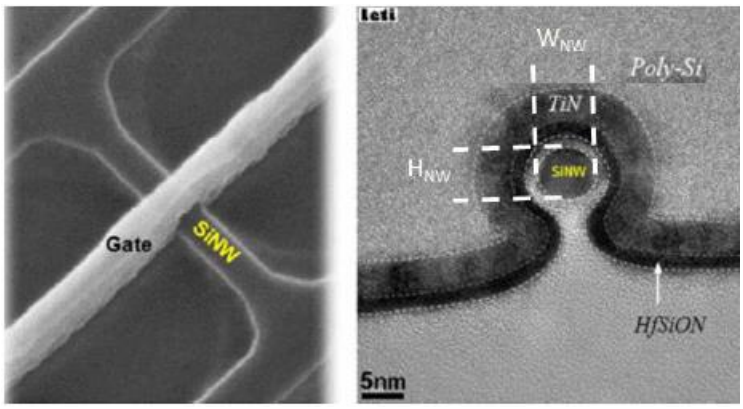

Figure 26 - (Left) SEM and (Right) cross-sectional TEM images of SOI Omega-gate nanowire with an 8 nm diameter [38].

The following table summarizes all the transistors that have been experimented with and different stress techniques have been performed to know their behaviour.

Transistor type	W	L
NMOS	300 nm	10 nm
NMOS	350 nm	10 nm
NMOS	400 nm	10 nm
NMOS	1200 nm	10 nm
NMOS	2400 nm	10 nm
PMOS	100 nm	10 nm
PMOS	300 nm	15 nm
NMOS	300 nm	20 nm

Table 4 – List of transistors used in the experiments

2.3 Set-up

2.3.1 Set-up with Semiconductor Parameter Analyzer

The assembly carried out to find out the RTN of the transistors examined was based on different stages. A first stage where the transistor to be studied was selected and the necessary connections with the tip table were made, a second stage where the SMU was configured to proceed with different scans in the SPA and finally the data processing with the Matlab software. In the following image the three stages mentioned are shown, where the first and the second block belong to the first and the second stage while the rest of the blocks form the third stage.

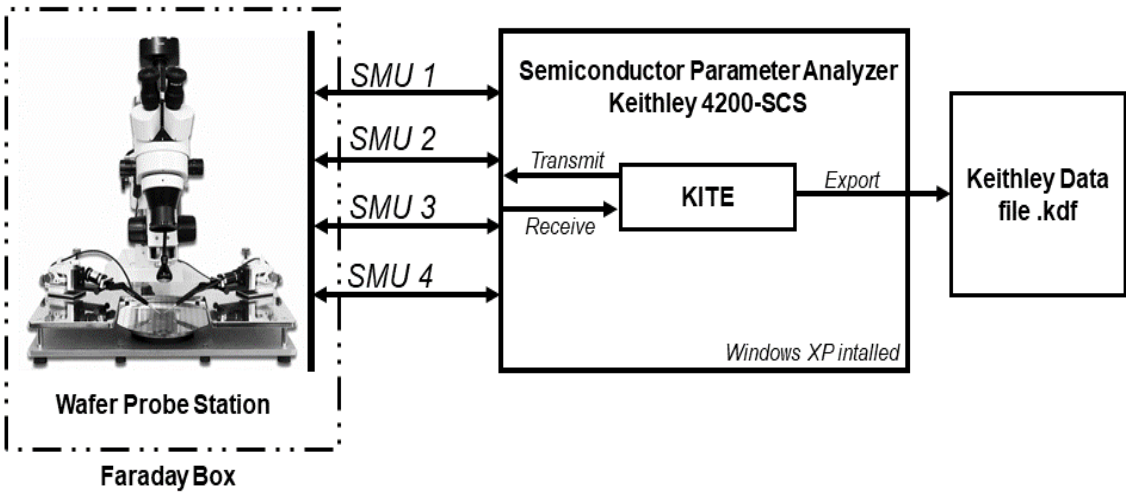

Figure 27 - First and second stage measurement set-up.

Figure 28 - Third stage measurement set-up and analysis.

First stage – Wafer Probe Station

The transistor to be studied must be selected before making the relevant connections with the 4 tips with which the SMU and FD-SOI transistors are connected. The selection of the devices is detailed in the "measurement results" section. Once the desired transistor is located on the wafer with the aid of the microscope, the tips are adjusted to make contact with the transistor pads (Drain, Gate, Source and Bulk). The SMUs are connected to the Semiconductor Parameter Analyzer (SPA).

It should be noted that the light seen in Figure 29 coming from the microscope is turned off and that the box which includes this first stage acts as a Faraday cage, for the reason that it affected the results, obtaining a little more current than expected. Another detail is that the tips have nanometric precision and are vacuum-locked.

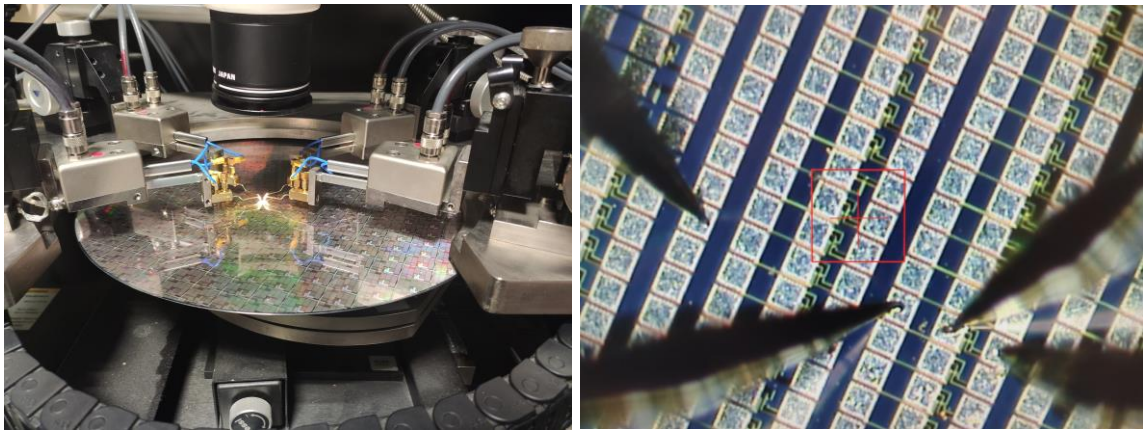

Figure 29 - Connection with the pads in tip table.

Second Stage – Semiconductor Parameter Analyzer

In this second stage the four tips were connected to the SPA (Semiconductor Parameter Analyzer) where it has two connections per tip, force, and sense. The SPA has the KITE program installed with which the different sweeps are configured, and the CVS (Constant Voltage Stress) are performed. Different sweeps have been made with different configurations that last from minutes to several days.

Once the results are obtained, they are exported with a KDF file where the parameters obtained are stored with which they are worked on in the third stage. These data include the times, voltages and currents of the different transistors worked on.

Third Stage – C++ and Matlab

The KDF file is compiled and the data is computed in Matlab codes. In this software, it is possible to program a multitude of graphics that have given the opportunity to choose the samples that provided the most value after the analysis and that were observed throughout the work.

2.3.2 Set-up with Remote Pulse Modulator

In this assembly the set-up is practically the same as the one described above, the workflow does not vary, but some extra devices have been added. Two RPM modules (Remote Pulse Measure unit) are added between the wafer probe station and the SMU with the objective of capturing RTN at a lower level of time than the one that was working in the first set-up.

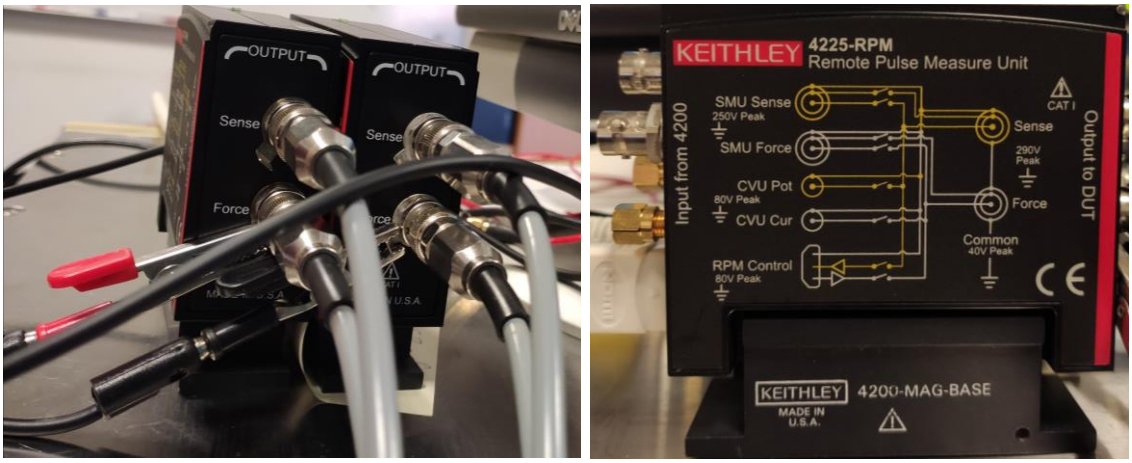

Figure 30 - RPM1 y RPM2.

These two modules are the same (RPM1 and RPM2) and are differentiated by the different outputs they have connected. The purpose of these devices is to unmask the untapped RTN. The RPM1 has the transistor gate as its output and the RPM2 has the drain. On the other hand, the bulk, source and ground outputs of the RPMs are connected to a common ground. Finally, the RPM inputs are connected to the SMU outputs through an HDMI cable.

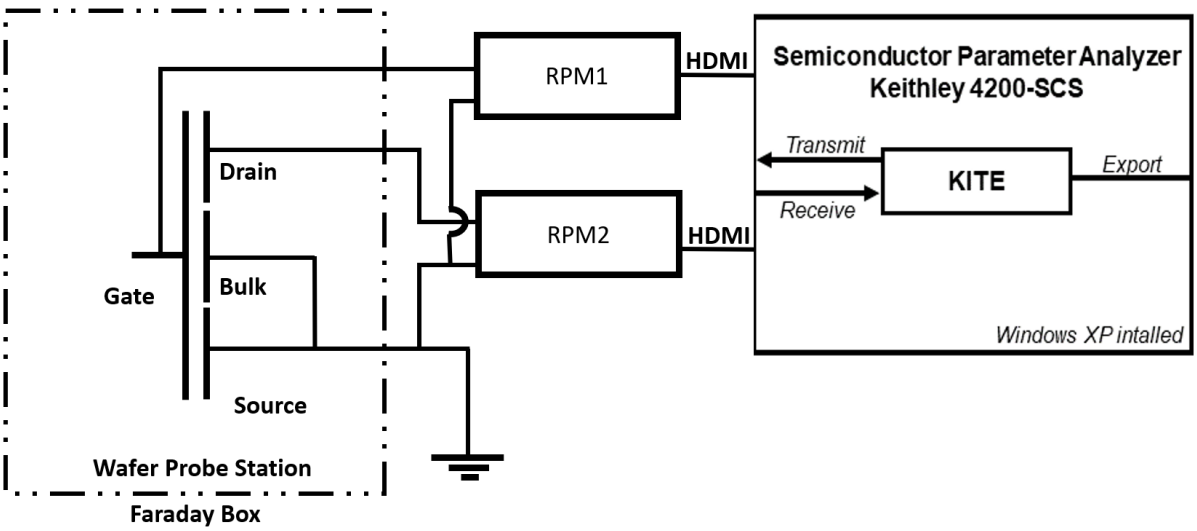

Figure 31 - Second measurement set-up with RPMs.

3. Fresh characterization of FD-SOI transistors

3.1 Fresh procedure

In this chapter the results obtained from the UTBB FD-SOI transistors are analysed, in this case the behaviour will be known through the fresh characterisation of the devices. The following flow shows how the experiments and analysis have been structured the fresh characterization.

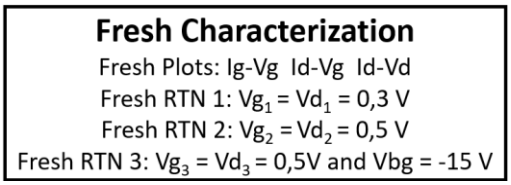

Figure 32 - Fresh characterization with Source Monitor Unit Set-up

The fresh characterization of the devices is divided into the theoretical points of the characterization explained in the previous section with which it is possible to obtain the parametric ranges where the devices work: I_G-V_G, I_D-V_G and I_D-V_D.

Once the characteristics to be obtained are known, this comparison of curves will be made between the dependence of different lengths, different amplitudes, and devices with the same dimensions.

3.2 Length dependence

The study of length dependence has been carried out with 300 nm amplitude transistors and lengths of 10, 15, 20 and 2400 nm.

For the characteristic curves of I_G-V_G, a voltage has been applied to the gate which made the sweep between -0.1 V and 0.1 V to know the value of the current in the gate. It should be mentioned that the logarithm is a standard applied to this curve in order to be able to compare the currents between devices adequately. As a consequence of these curves, it can be seen that the increase of the current is given to an increase of the length of the device increasing the area and corroborating the first theoretical point of this project. In addition, when the voltage of the gate is at or near zero it is reduced to zero values.

On the other hand, to obtain the I_D-V_G curve, a constant voltage of 100 mV has been applied to the drainer and a sweep has been performed on the gate voltage to measure the current of the drainer. It shows that increasing the length and increasing the voltage applied to the gate also increases the drainer current. Independently, both the L dimension and the voltage in the gate increase the drainer current.

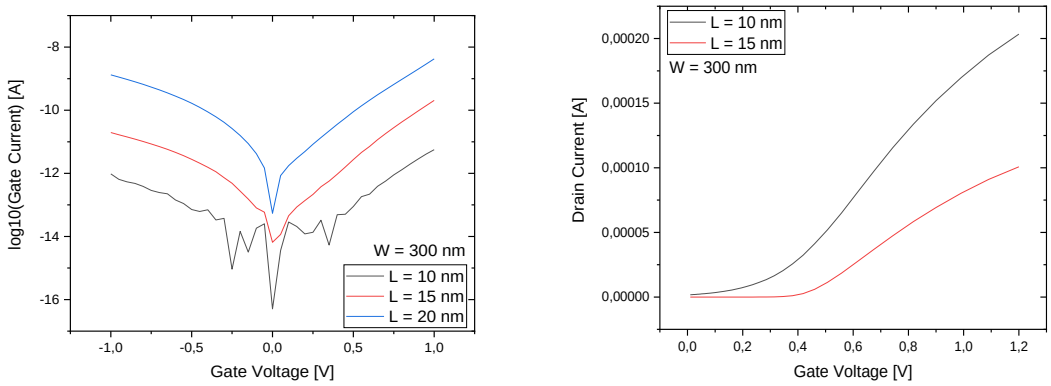

Figure 33 - Left figure represents the I_G-V_G plot and right figure represents the I_D-V_G plot in fresh conditions, the figures depend on the length transistor with constant width.

The following figures show on one side the I_D-V_G curve but this time applying the logarithm to the drain current and the I_D-V_D curve shows the operating regions where the transistor works when the transistor has connected a constant gate voltage and sweep drain voltage. Applying the logarithm to the drain current on the I_D-V_G curve helps to detect the threshold voltage at which the transistor starts working, observing that for bigger L dimensions less voltage is needed to enter the ON regim. The I_D-V_D characteristic curve shows that having larger L dimensions the operating currents will be lower independently if it works in saturation or linear.

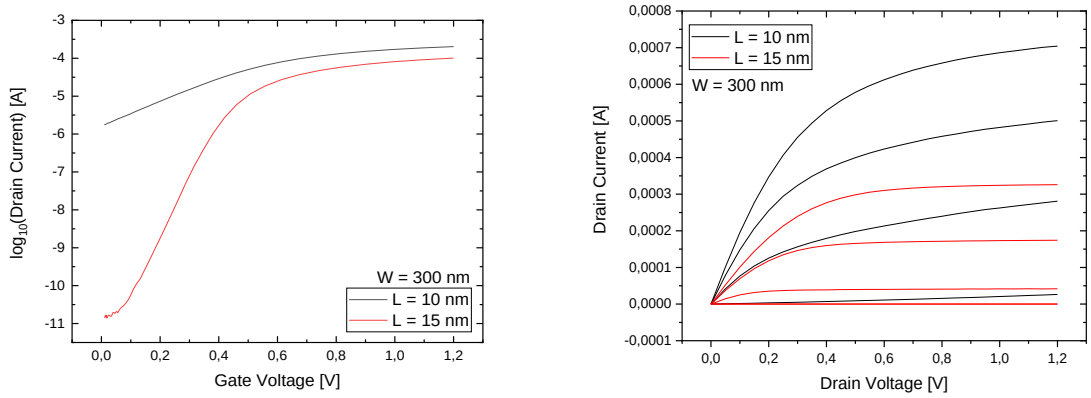

Figure 34 - Left figure represents the I_D-V_G plot and right figure represents the I_D-V_D plot in fresh conditions, the figures depend on the length transistor with constant width.

Concluding that the drain currents increase when the length decreases in all cases of the characteristic curves and the gate current go up with the bigger length.

3.3 Width dependence

In this case, the procedure has the same methodology that has just been done in the case of length dependence. The length devices of 10 nm have been established while the amplitudes worked to be compared are 300 nm, 350 nm, 400 nm and 2400 nm.

The I_G-V_G characteristic curve, as mentioned before, is made by applying a voltage sweep to the gate and capturing the current in the gate. By observing the results, the same conclusion can be drawn as in the case of different lengths. As the amplitude increases, the area increases and with it the current in the gate.

The I_D-V_G characteristic curve does not show the 2400 nm amplitude device because it was far from the small dimensions on which the work is focused. A constant voltage has been applied to the drain and a voltage sweep has been applied to the gate causing a current change in the drain, corroborating the theoretical part, the drain current is bigger in big width than small width.

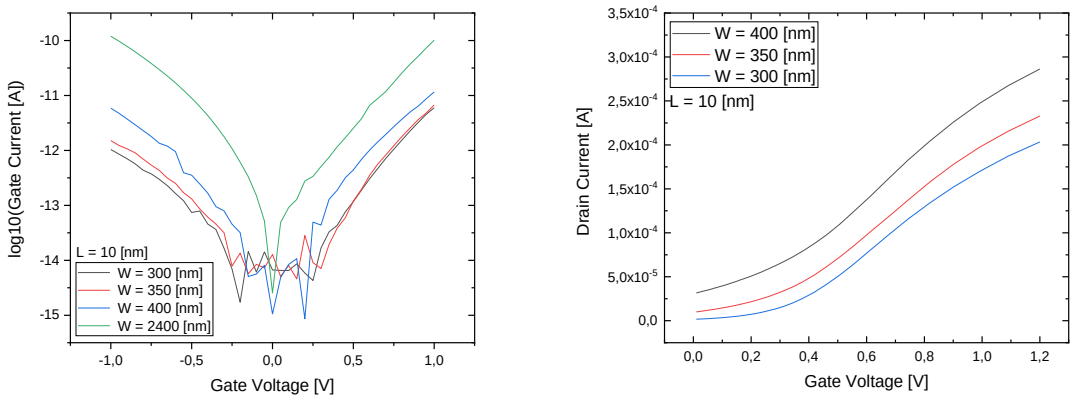

Figure 35 - Left figure represents the I_G-V_G plot and right figure represents the I_D-V_G plot in fresh conditions, the figures depend on the width transistor with constant length.

The following images show the I_D-V_G curve where the current is standardised and the threshold voltage where it starts to work can be seen in more detail, indicating that it is lower for larger amplitudes. On the other hand, as in the case of length dependence, the drainage current for the I_D-V_D curve increases with the increase in amplitude but in a lesser proportion.

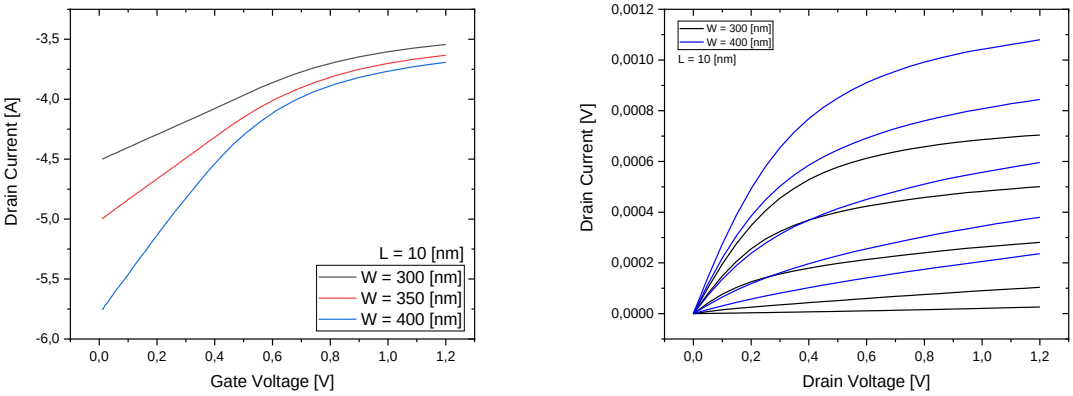

Figure 36 - Left figure represents the I_D-V_G plot and right figure represents the I_D-V_D plot in fresh conditions, the figures depend on the width transistor with constant length.

3.4 Inter device variability

The aim of this section is to compare the behaviour of two equal pristine devices, also through their electrical characteristic. Where the time of the devices is zero (Time-0).

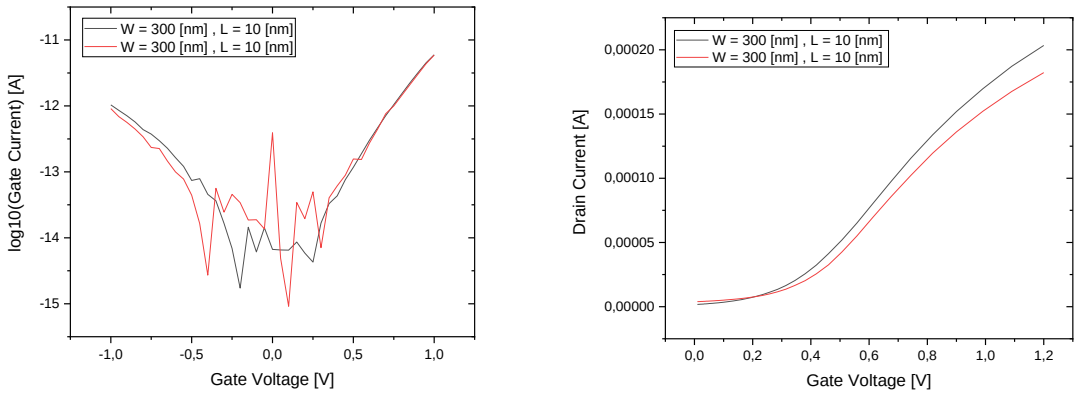

Figure 37 - Left figure represents the I_D-V_G plot and right figure represents the I_D-V_D plot in fresh conditions, the figures depend on the back gate connection with constant dimensions.

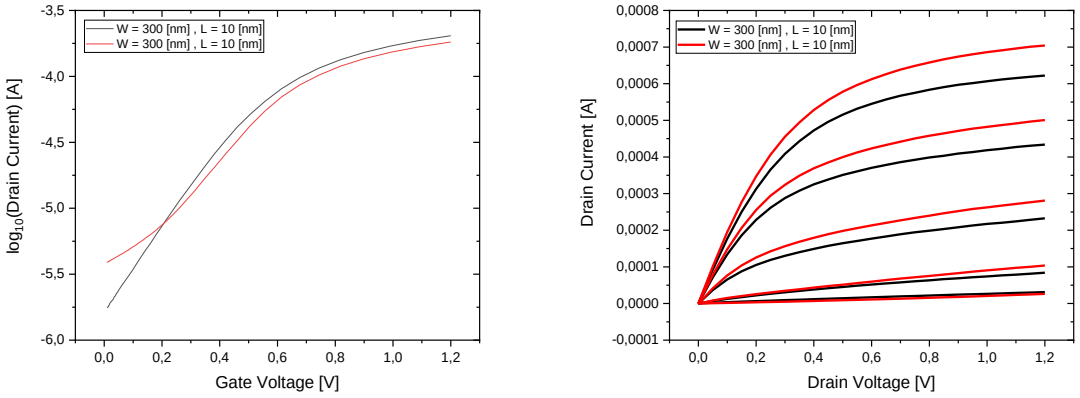

Figure 38 - Left figure represents the I_D-V_G plot and right figure represents the I_D-V_D plot in fresh conditions, the figures depend on the back gate connection with constant dimensions.

As can be seen in the four figures at this point, having different devices has caused differences between them, not so much in the current of the back gate but in the current obtained in the drain. It should be noted that not all the devices give the same values but the same behaviour.

The regions of operation shown in the I_D-V_D curve that shows both this point of dependence on the same device and that of dependence by amplitude Figure 38, leads to the conclusion that different devices can give as different currents as the fact of increasing their amplitude in small devices, in both cases referring to a difference of about 50 A.

4. Characterization of BTI in FD-SOI transistors

4.1 Stress procedure

The stress characterization of UTBB FD-SOI transistors is analysed to know how the device performance is affected by the aging mechanisms. The following flow shows the structure of the experiments to obtain the results.

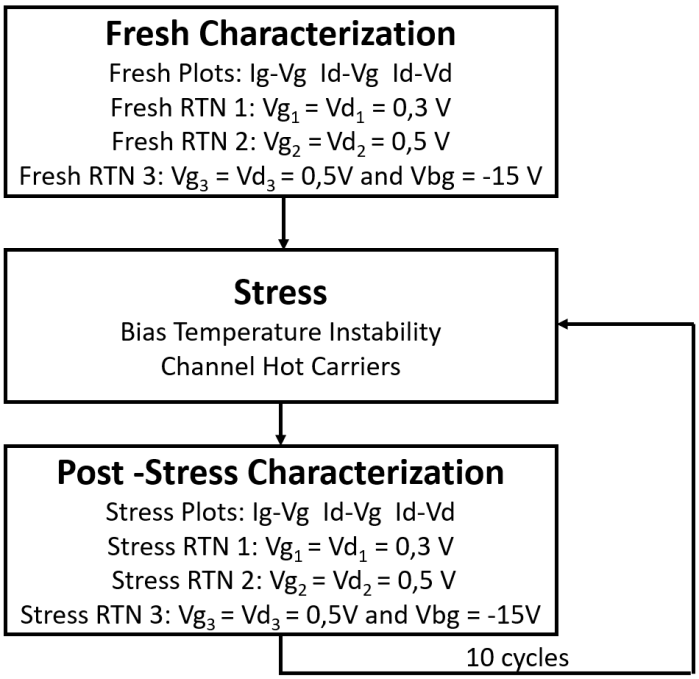

Figure 39 - Fresh characterization and post-stress characterization workflow with Source Monitor Unit Set-up.

Then the devices are stressed, in this case BTI (Bias Temperature Instability) as studied, by applying high voltages to the gate for a period of time in order to degrade it. This stress time has been several hours, so getting the necessary samples to confirm the results has taken weeks of stress on the devices. The time applied to a device has been of hours, so it has affected it as if years had passed to the device (extrapolated with Eq. 1). The applied stress voltages have been established in 1.8 V, 2.0 V and 2.2 V after observing little degradation to lower voltages of 1.6 V and breakage of the devices from 2.2 V.

Exactly the data of the transistors have been collected after each stress, with which the stress is characterized and reapplied, getting to see the progression of the degradation. A total of 10 stresses per device. Once the stress has been applied, the characterization of the devices is carried out and they are compared between them.

The RTN is obtained both in the fresh characterization and in the stressed characterization after each cycle.

4.2 Bias Temperature Instabilities degradation in FD-SOI transistors

The degradation seen in this section is caused by bias temperature instability (BTI), which is produced by applying high voltage for a short time (what is done in this section) or a small voltage over a long period (life of the transistor). As commented in the theoretical section, it is necessary to know the behaviour of the device during its life, but to do this it is necessary to apply high voltages to accelerate the process. The BTI, from the high temperatures and the voltages in the gate, degrades the device affecting the dialectic of the gate.

In order to observe the degradation, it will focus on the characteristic curves of the transistors. First of all, a case is observed to know how the degradation affects the BTI application. To show this, the current of the device has been plotted on the gate. This current begins to decrease because in the case of a NMOS is positive bias temperature instability (BTI), then it is observed that after each cycle of stress, its value decreases.

On the other hand, the current is affected when observing the I_G-V_G, cycles 9 and 10 are not very relevant in this curve since they are very abruptly dependent on the others, but in general after each cycle the current is modified but not in a very considerable form in this case.

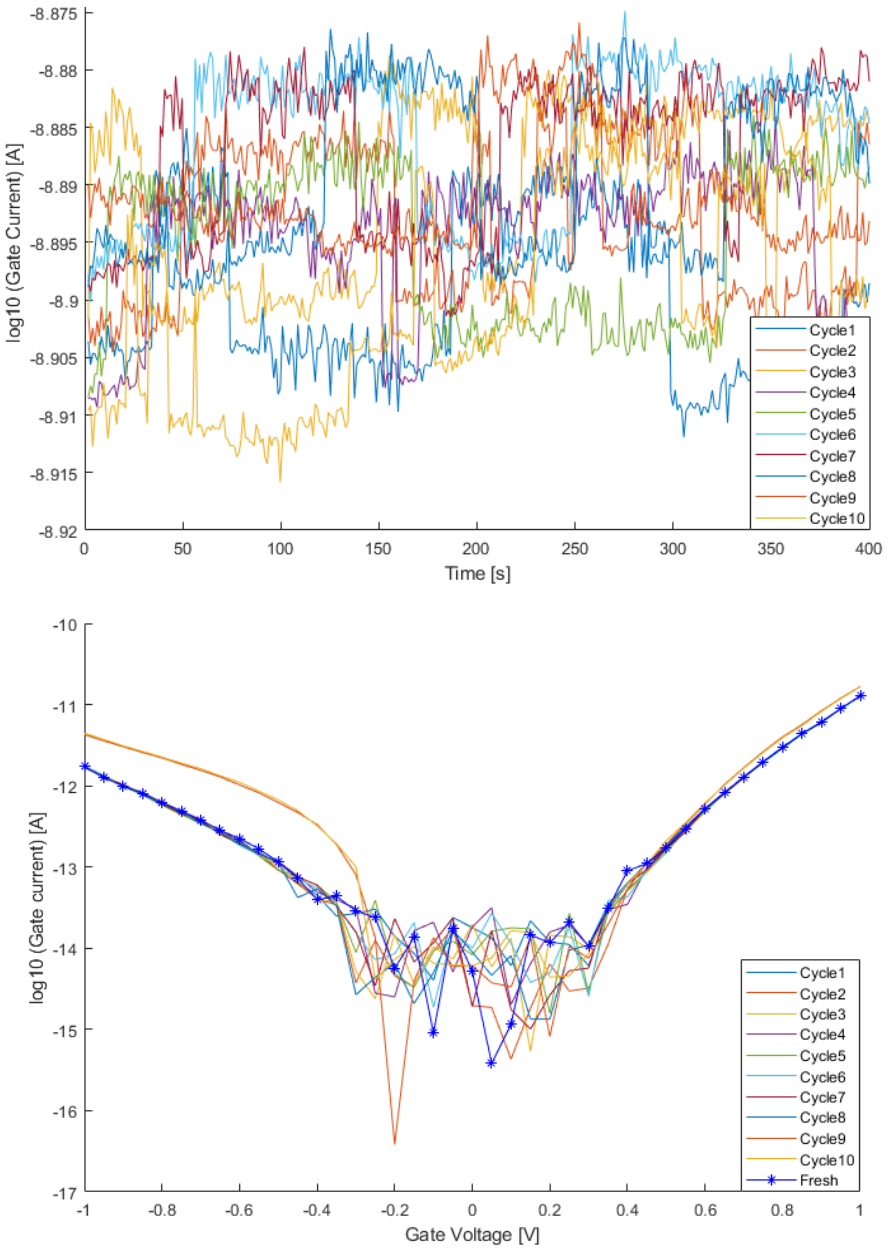

Figure 40 - Top figure represents the post stress plot, each curve represents a cycle of stress and bottom figure represents the I_G-V_G plot. For device of 350 nm width and 10 nm length and stressed with 1,8 V per cycle.

Figure 41 y Figure 42 show the I_D-V_G and the I_D-V_D curves where it should be noted that it is clear how the drain current is reduced after each cycle. In addition, an extension of the image is shown with which it is possible to observe that after each cycle it moves to lower values in the order of µA in this case, over the interval of 1 µA and 4 µA in the two curves but this is specified in more detail in the following point.

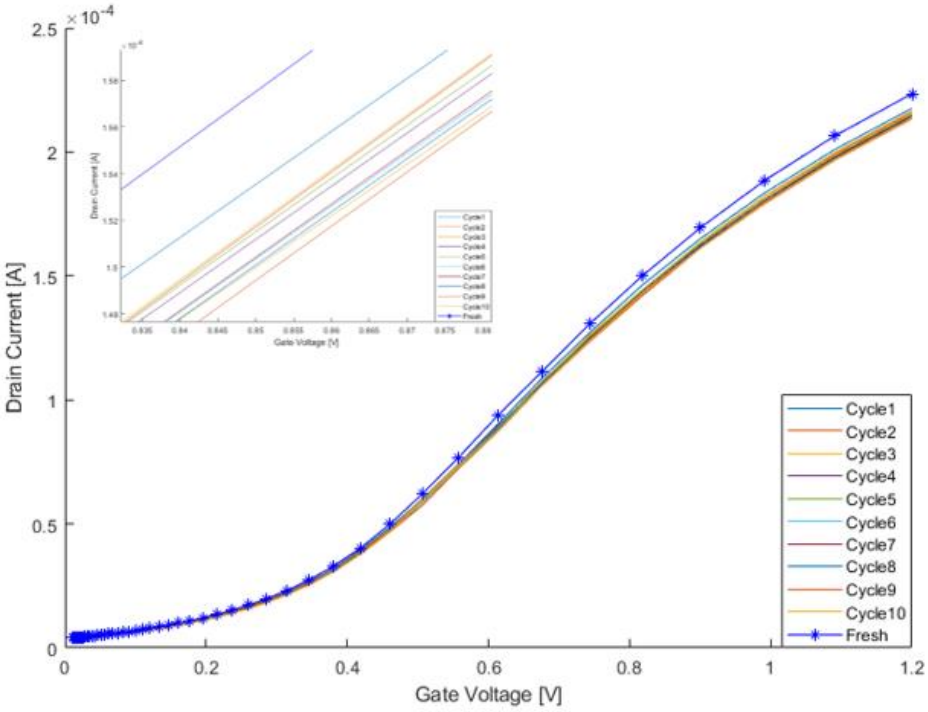

Figure 41 - Figure represents the I_D-V_G plot after the application of stress, each curve represents a cycle of stress and the onside figure represents the same I_D-V_G plot but extended to visualize the degradation.

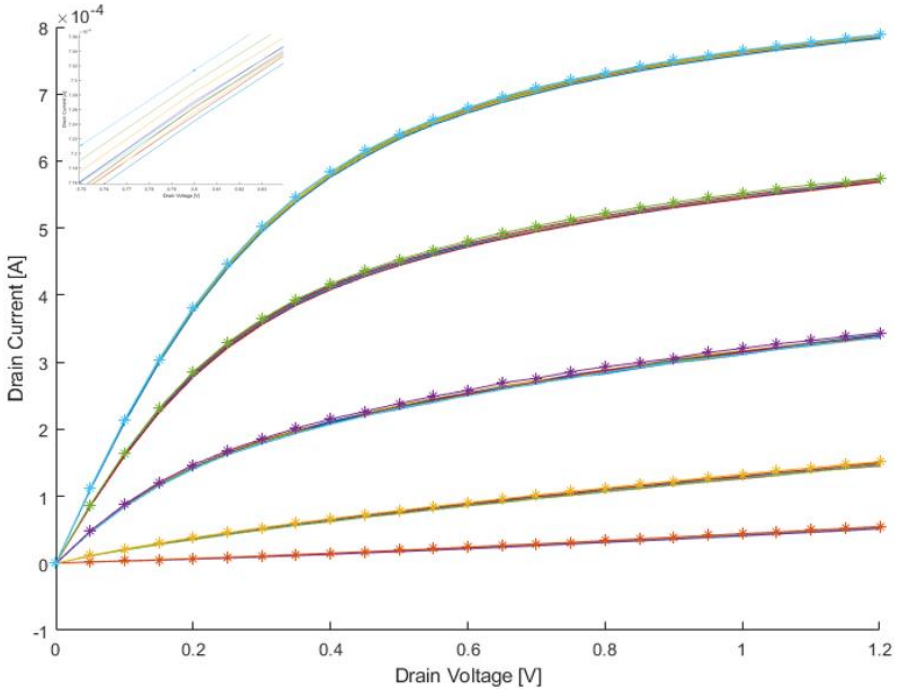

Figure 42 - The figure represents the I_D-V_D plot after the application of stress, each curve represents a cycle of stress and onside figure represents the same I_D-V_D plot but extended to visualize the degradation.

4.3 Channel dimensions dependence

The characteristic curves described previously, which have also been analysed at the fresh characterisation point, are then carried out. The aim of this point is to compare the situation of a device when it is new and after having applied some stress cycles to it in order to observe its degradation.

The study of this point is carried out using transistors of different amplitudes and the same lengths, exactly 300 nm (black) and 400 nm (red) with a length of 10 nm, while the stress cycles are the same with the same voltages. The situation of the fresh state is the solid line while the stressed state after having been stressed 10 cycles at 2.2 [V] per cycle is a discontinuous line. Mention that it is one of the devices with the stress with more cycles and with the highest voltage achieved.

Leaving apart the comparison between the fresh lines as it analysed in previous points, the degradation in the characteristic curve I_G-V_G has not been very impressive in the current of the gate. On the other hand, the current in the drain for the I_D-V_G curve had a negative displacement of less than 40 µA in the case of the 400 nm amplitude device, while the 300 nm device was about 20 µA.

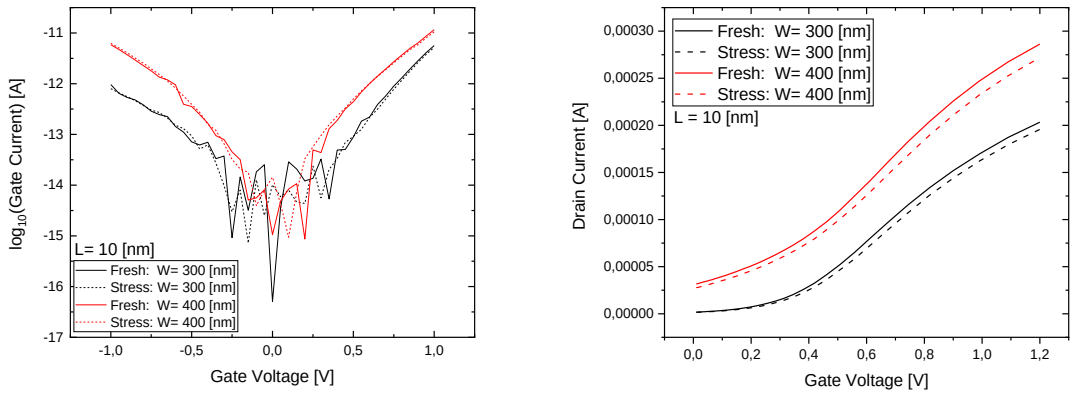

Figure 43 - The left figure represents the I_G-V_G plot (log current) where is compared the fresh vs degraded behaviour for two devices, same length (10 nm) and different width (300 nm and 400 nm). The right figure shows the I_D-V_G plot where is the fresh vs degraded behaviour for the devices mentioned in the left figure. Number of stressed cycles is 10 to 2.2 [V].

The degradation has affected the drain current as can be seen in Figure 43 where the case of the stressed has reduced its current against the fresh state. In the characteristic curve I_D-V_D for the

case of the 400 nm device its negative variation has been 20 µA while the 300 nm one has been lower than 5 µA.

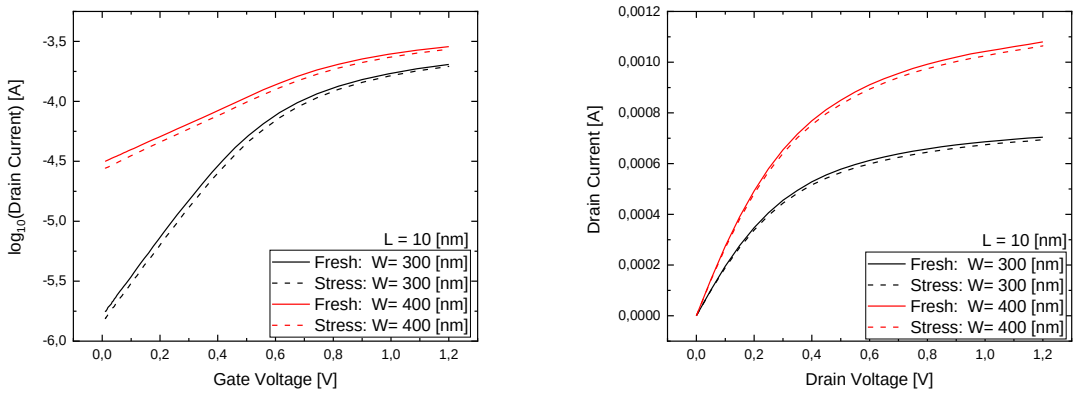

Figure 44 - Left figure represents the I_D-V_G plot where is compared the fresh and stress 10 cycle for different width and equal length. Right figure shows the I_D-V_D plot where fresh and stress 10 cycle are compared for different width and equal length. Number of stressed cycles is 10 to 2.2 [V].

It can be seen that the threshold voltage is not always the same. To observe how the threshold voltage varies, its value has been obtained after each cycle to see at which voltage the transistor starts to operate in the ON regim. Its mobility has also been obtained in order to know its variation cycle after cycle. The following two figures give information about their values and what percentage is deviated from the fresh cycle.

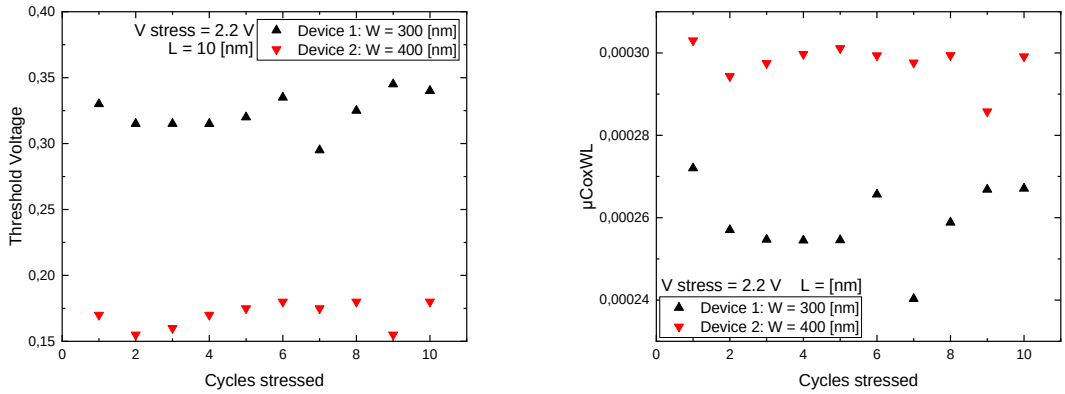

Figure 45 - Left figure V_{TH} post stress. Right figure µCoxWL. Number of stressed cycles is 10 to 2.2 [V].

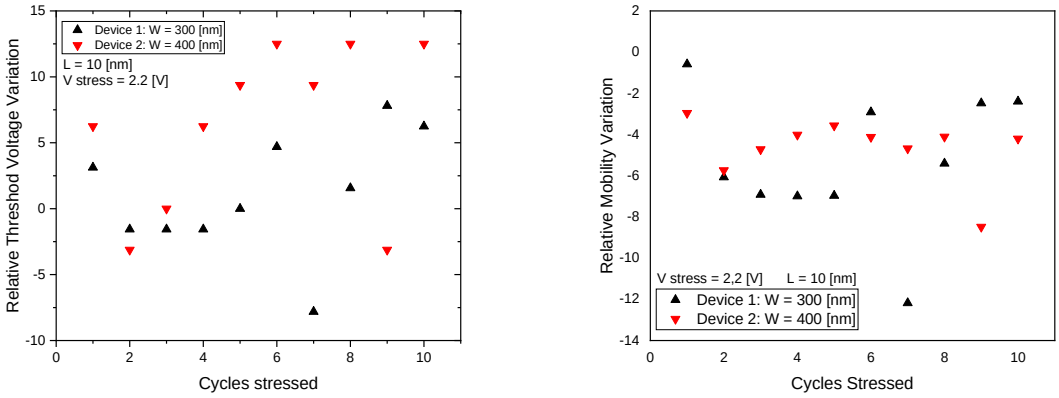

Figure 46 - Left figure %V_{TH} post stress. Right figure %Mobility. Number of stressed cycles is 10 to 2.2 [V].

It can be seen that the threshold voltage is not always the same and varies after each stress, between 0.35 V and 0.31 V in the case of W = 300 nm and between 0.18 V and 0.15 V in the case of W = 400 nm. It varies in percentage terms from -7.5% to 7.5% for 300 nm and about -4.1% to 12.5% for 400 nm. This means that when cycles are applied, the tendency of variation of the threshold voltage is ascending.

On the other hand, mobility is centred on 0.00029 and 0.00031 for the small device and 0.00024 and 0.00028 for the large device with a percentage variation of up to -12% and -8% respectively.

In conclusion, the degradation is visible and affects the currents a few tens of microamperes and the threshold voltage plus the mobility is affected by varying its value increasingly far from the original sample cycle after cycle of stress.

4.4 Stress voltage dependence

In this section the characteristic curves for the same device of 400 nm width and 10 nm length are made but its stress is analysed after applying different voltages and setting different cycles of comparison. On the one hand, the stress for 3 cycles of a voltage of 1.8 V, 2.0 V and 2.2 V is studied, and on the other hand, a stress for 10 cycles of a voltage of 2.0 V and 2.2 V.

Starting from the first case, the characteristic curve I_G-V_G and leaving aside that they are different devices, in all cases after applying a voltage sweep on the gate it is obtained that the stressed curves compared to the fresh ones are reduced. The I_D-V_G results in a degradation of 5

µA for the 2.2 V degradation, to 3 µA for the 2 V degradation and to 1 µA for the 1.8 V degradation, being 3 stress cycles.

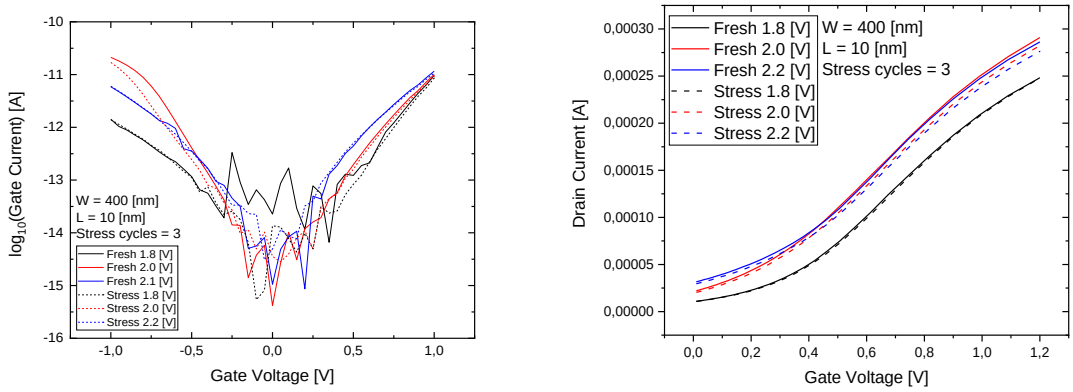

Figure 47 - Left figure shows I_G-V_G plot where the devices have the same dimensions and the 3 cycle stressed applied was different (1.8V, 2.0V, 2.2V), the plot compared the degradation between the fresh and stress state for different stressed voltage. Right figure shows the I_D-V_G plot where the devices have the same dimensions and the three-cycle stressed applied was different (1.8V, 2.0V, 2.2V), the plot compared the degradation between the fresh and stress state for different stressed voltage.

On the other hand, in the second case in which the stress cycles are 10 to 2.0 V and 2.2 V for each of them, it is observed that the I_G-V_G has a similar drop to that of the previous case but observing the I_D-V_G the currents are degraded for the case of 2.0 V between 1 and 2 µA while for 2.2 V about 3 µA. Comparing it with the previous case, similar values are observed.

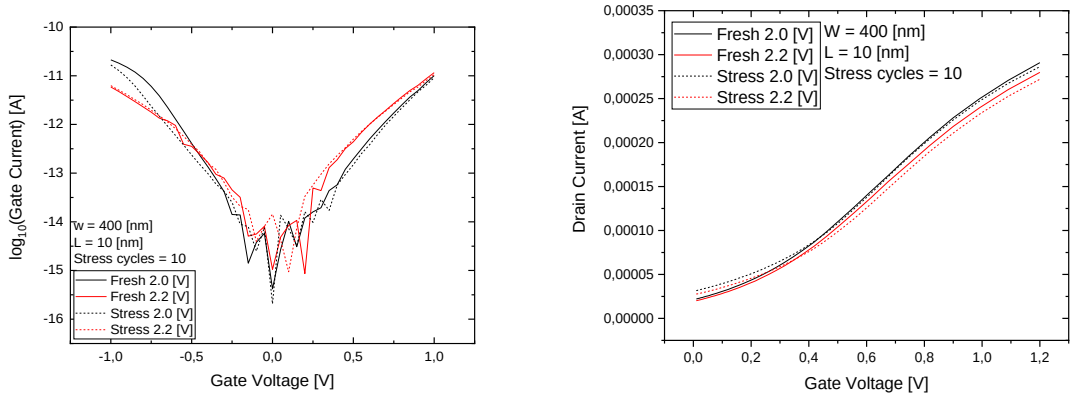

Figure 48 - Left figure shows I_G-V_G plot where the devices have the same dimensions and the ten-cycle stressed applied was different (2.0V and 2.2V), the plot compared the degradation between the fresh and stress state for different stressed voltage. Right figure shows the I_D-V_G plot where the devices have the same dimensions and the ten-cycle stressed applied was different (2.0V and 2.2V) comparing the fresh and stress state.

The following figures show the I_D-V_G curve where the logarithm of the drainage current is made and the I_D-V_D characteristic curve for both cases. It is shown that the degradation is minimum in the two curves so that the behaviour of the transistor remains the same.

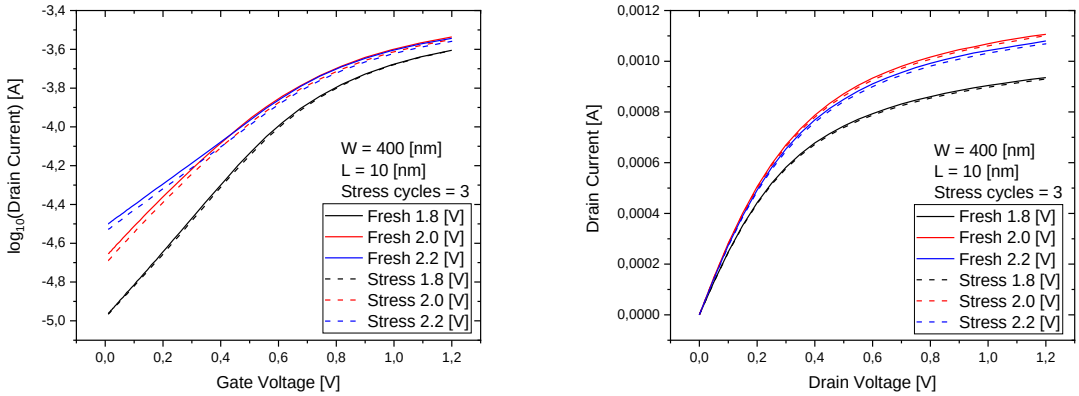

Figure 49 - Left figure shows I_D-V_G plot where the devices have the same dimensions and the three-cycle stressed applied was different (1.8V, 2.0V, 2.2V), the plot compared the degradation between the fresh and stress state for different stressed voltage. Right figure shows the I_D-V_D plot where the devices have the same dimensions and the three-cycle stressed applied was different (1.8V, 2.0V, 2.2V) comparing the fresh and stress state.

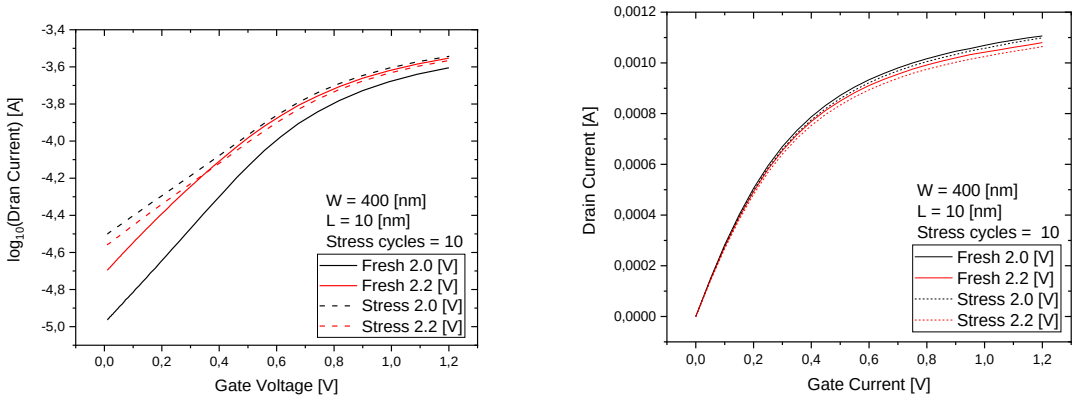

Figure 50 - Left figure shows I_D-V_G plot where the devices have the same dimensions and the three-cycle stressed applied was different (2.0V and 2.2V), the plot compared the degradation between the fresh and stress state for different stressed voltage. Right figure shows the I_D-V_D plot where the devices have the same dimensions and the three-cycle stressed applied was different (2.0V and 2.2V) comparing the fresh and stress state.

The evolution of the threshold voltage after each cycle and mobility is shown below. Indicate that cycle 0 is the fresh state of the device in all cases to properly compare the deviation between the points.

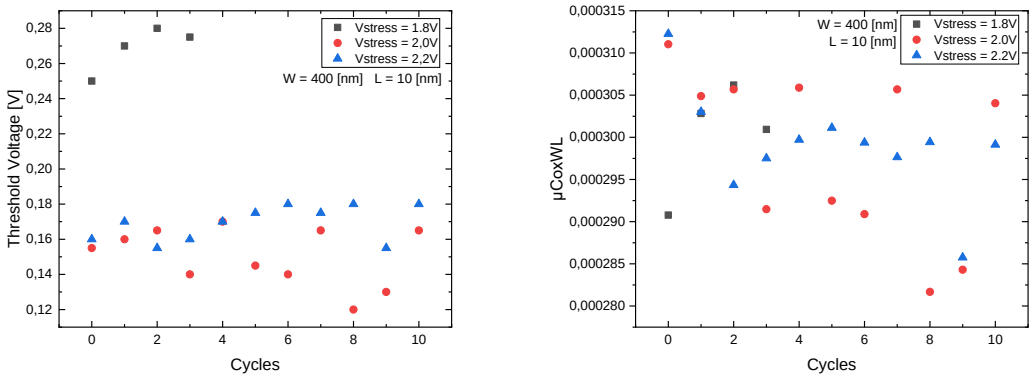

Figure 51 - Left figure V_{TH} post stress. Right figure Mobility. Number of stressed cycles is 10 to 2,0 [V] and 2,2 [V].

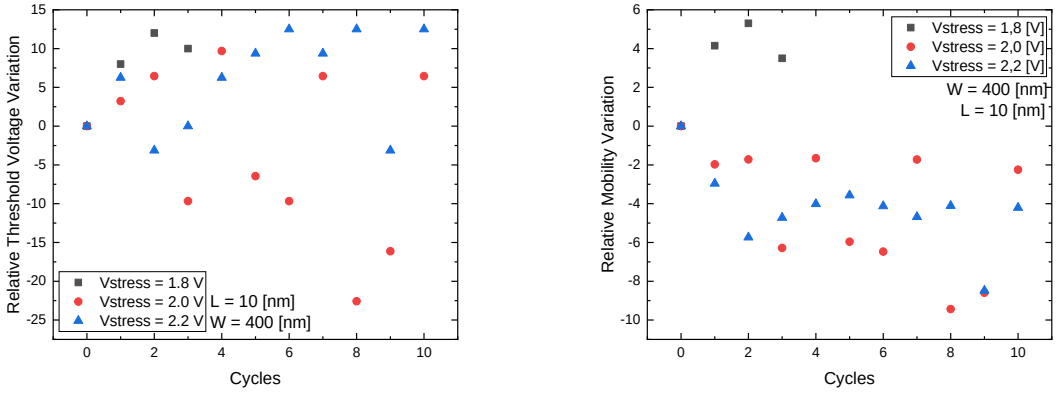

Figure 52 - Left figure %V_{TH} post stress. Right figure %Mobility. Number of stressed cycles is 10 to 2,0 [V] and 2,2 [V].

Finally, it is concluded that the threshold voltage deviates from the sample by about 20 mV, reaching maximum deviations of 40 mV (between 5-25% in the values deviated from the first one). As for mobility, it generally tends to be reduced except for the case of 1.8 V of stress, causing variations of up to 10%.

Mention that the maximum voltage applied in stress is 2.2 V because at higher voltages the transistor finally breakdown because the dielectric in the gate cannot support it. The degradation by BTI of the devices has been minimum so that the behaviour of the transistor remains the same.

5. Random telegraph noise characterization

This section shows the most relevant random telegraph noise obtained with the aim of knowing what its impact is on the device and what change in current it ends up causing in its behaviour. In order to carry out this analysis from the codes, the data acquired from the tip table has been processed, giving the information of the samples collected, obtaining the drain current according to various gate and drain constant voltages.

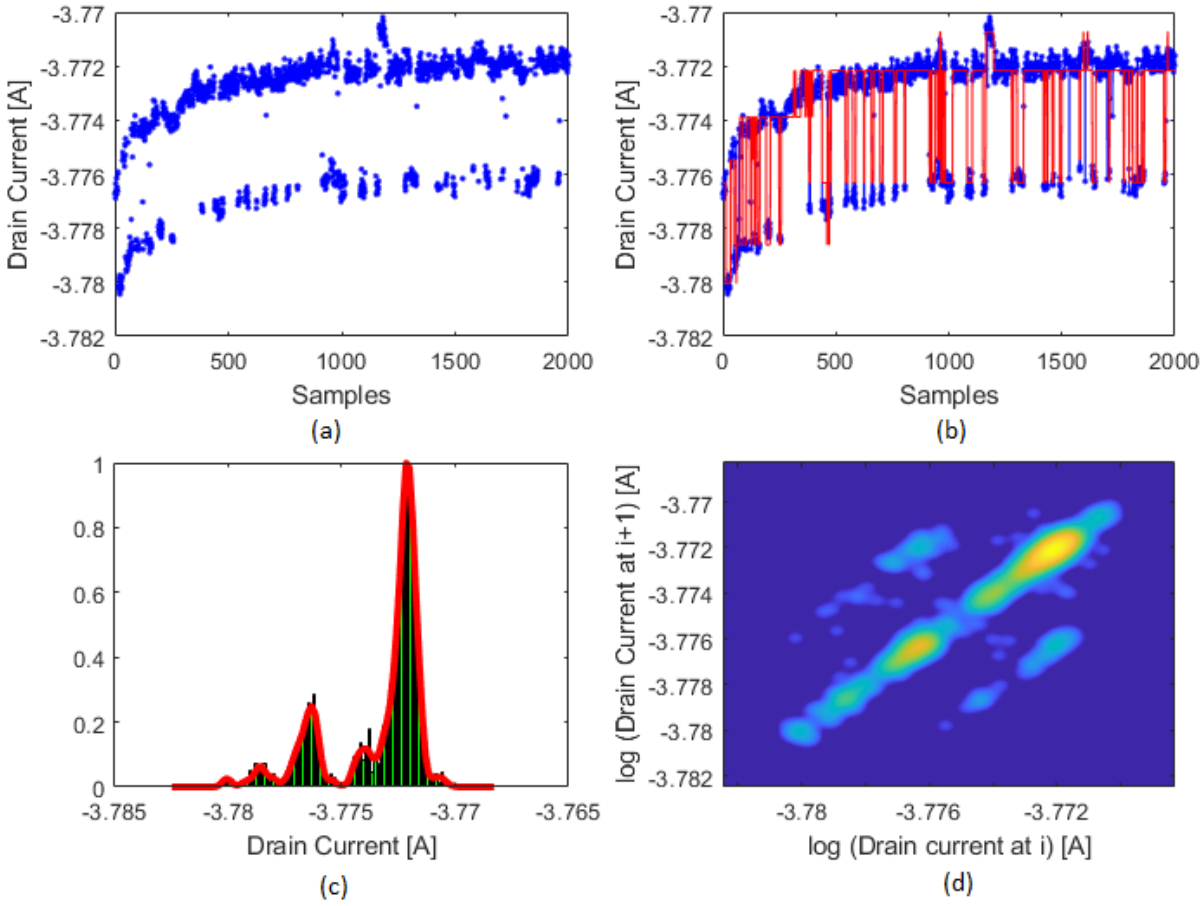

Figure 53 - Fresh RTN1 and W-TLP for transistor of 350 nm width and 10 nm length (1.8 V).

With these graphs of Figure 53, leaving out the transistor that is analysed, the behaviour of the current can be observed. Where it can be seen what is the current behaviour during the time that the voltage is applied (Figure 53.a) together with the current drain values. Figure 53.b shows the different main levels that the RTN has together with sublevels, which will be discussed in more detail in the following points. The axis Y of the figures mentioned is their logarithm current and it is applied in all the document. Figure 53.c is a Gaussian one that informs about

the number of points that are in the different maximum and minimum current levels that give rise to the RTN. Finally, Figure 53.d is the W-TLP (Weighted Time Lag Plot) with which, in a simple form, the RTN levels can be seen together with the sub-levels, as well as the steps between these levels.

5.1 Random telegraph noise results without remote pulse measure unit

In the following two sections the RTN is analysed both in the fresh devices and after having applied a stress of several cycles with Semiconductor Parameter Analyzer (SPA).
The following table give the different configuration to obtain the RTNs. There are different configurations in the project because sometimes to capture the RTN levels is difficult.

	Gate voltage applied	Drain voltage applied	Back gate voltage
RTN 1	0,3 V	0,3 V	0V
RTN 2	0,5 V	0,5 V	0V
RTN 3	0,5 V	0,5 V	-15 V

Table 5 – Different configurations to obtain the RTN levels.

5.1.1 Fresh characterization of random telegraph noise with SPA

Mention that the fresh RTN shown and analysed are the extreme cases observed in the devices, it is the noise that affects the transistors more by doing changes of several µA. The objective is to capture the different level that count as a default.

The first RTN to be analysed is the RTN 1 obtained by applying 0.3 V to the gate and the drain. As it is indicated in the first image of Figure 54, two levels can be observed, several levels can appear as it has been shown in the theoretical section (multilevel RTN), but in this particular case two main levels can be seen that are in 167.3 µA (level 1) and 169 µA (level 2), giving a very significant difference associated to the RTN and not to the background noise. In this case there are two principal defaults.

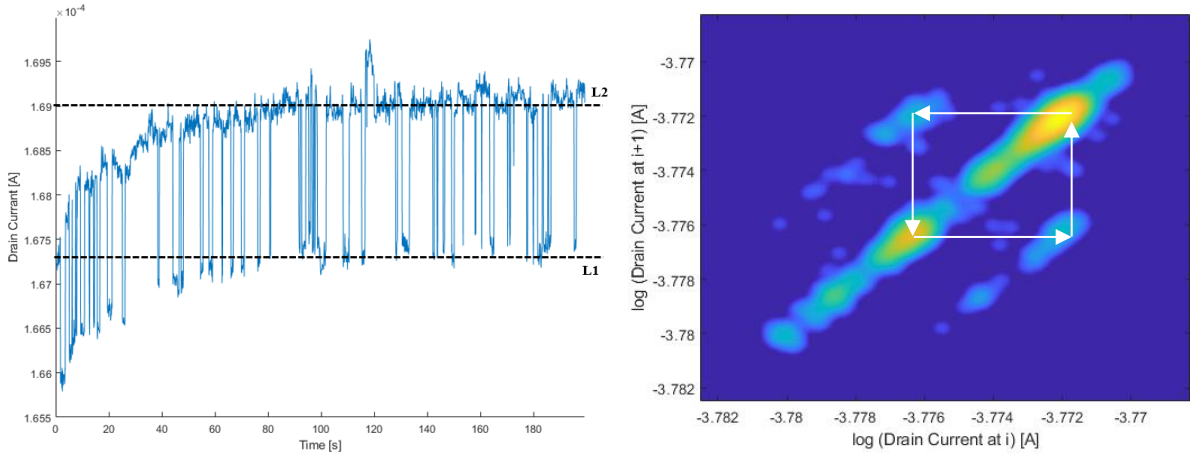

Figure 54 - Fresh RTN1 and W-TLP for transistor of 350 nm width and 10 nm length (1.8 V).

Another point to mention is that it has an increasing tendency at the beginning when a voltage starts to be applied and it stabilizes, this happens in some of the devices. This ascending transition causes levels 1 and 2 to be dispersed in the W-TLP as they move increasing their current. From W-TLP it can be seen how the current makes these steps (white lines) leaving its trace in points parallel to the main diagonal. As mentioned above, the hot colour represents a concentration of points at the same level of the current, while the cold ones represent a smaller quantity.

The following three figures are part of the same device, a transistor of 300 nm width and 10 nm length to which the three configurations proposed to try to capture the RTN are applied.

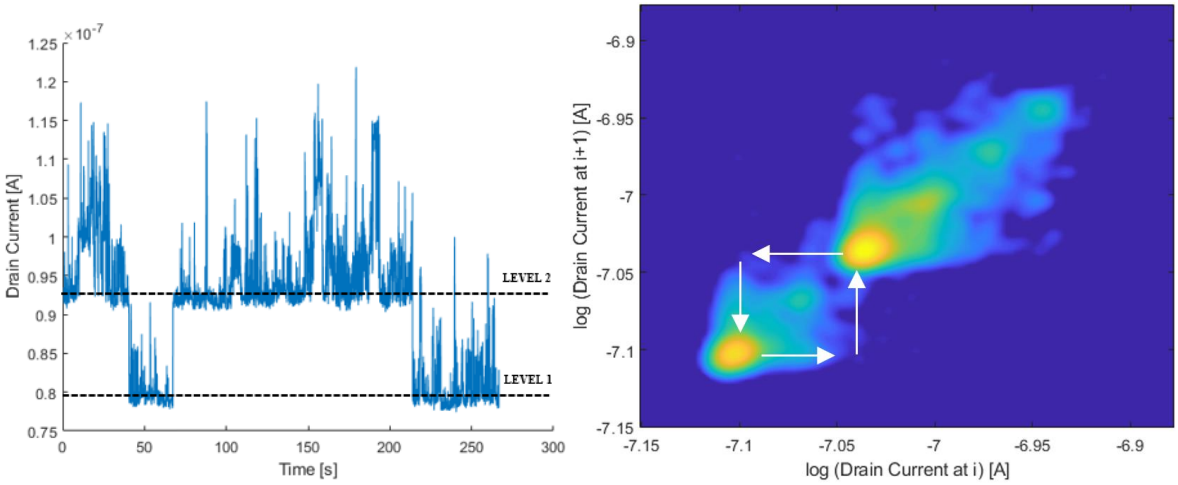

Figure 55 - Fresh RTN1 and W-TLP for transistor of 300 nm width and 10 nm length (1.8 V).

This RTN has been obtained by applying 0.3 V to the gate and the drain. The two levels marked in the figure are the main ones, but other levels with less importance could be allowed. Levels 1 and 2 are at 80 nA and 93 nA respectively, with a difference of 13 nA, an insignificant RTN obtained with the previous case. The other levels, not so relevant and not indicated, are found at 100 nA and 115 nA and are appreciable in the W-TLP together with the steps that reach them.

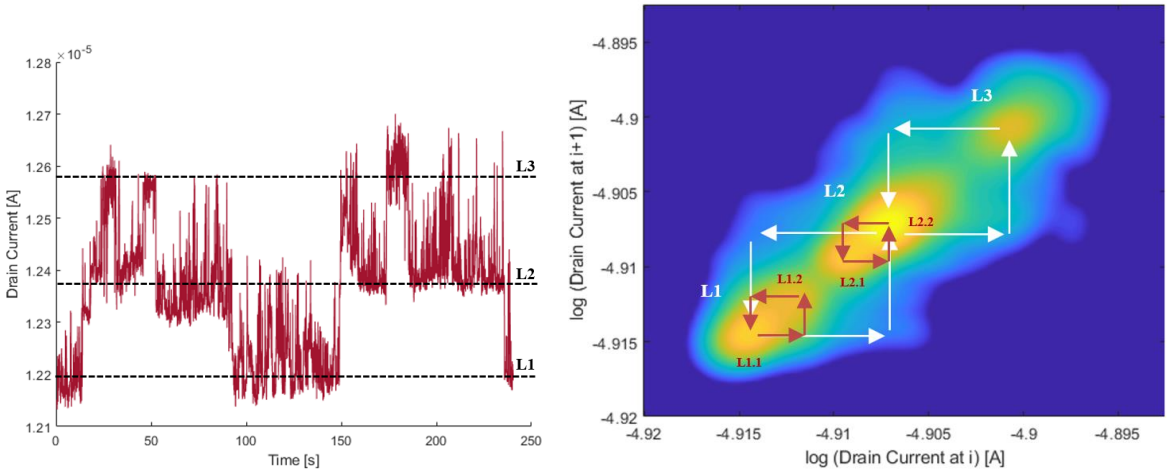

Figure 56 - Fresh RTN2 and W-TLP for transistor of 300 nm width and 10 nm length (1.8 V).

The 0.5 V has now been applied to the gate and the drain. This time there are three main levels centred on 12.2 µA level 1, 12.37 µA level 2 and 12.26 µA level 3. There are sublevels within levels 1 and 2, these are sublevels of the RTN which are shown in red in Figure 56, level 1.1 and 1.2 added to level 2.1 and 2.2, whose current difference is much less than that of the main levels. The difference between sub-levels is 0.01 µA and between main levels 0.2 µA. Then there are two sublevels (2 defaults) that create a level (principal default), this happened two times and another level without sublevels.

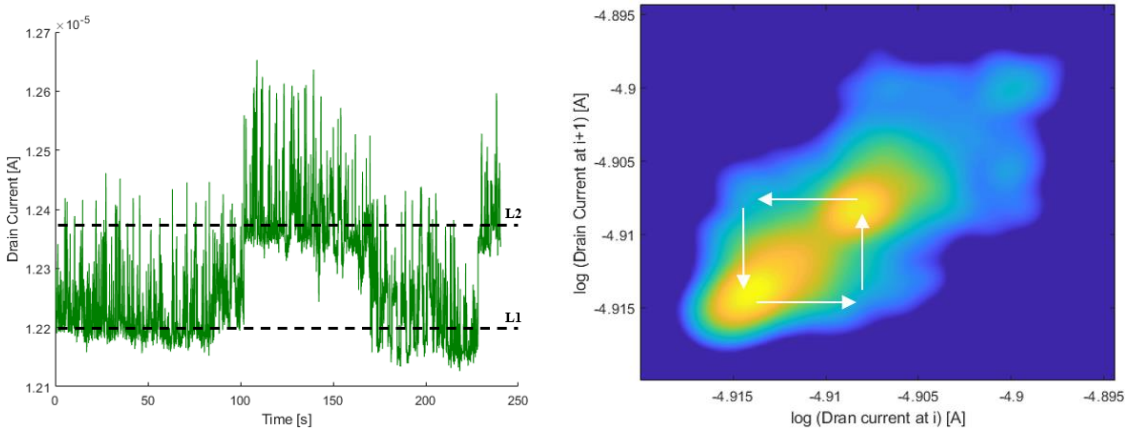

Figure 57 - Fresh RTN3 and W-TLP for transistor of 300 nm width and 10 nm length (1.8 V).

Finally, the fresh RTN 3 has the same configuration as the RTN 2 but applying a voltage of -15 V to the back gate. The levels fall to exactly the same current as the RTN 2 so the current difference is the same, 0.2 µA. Sub-levels could also be considered but they are not significant as in the previous case.

As a conclusion, by applying more voltage to the drain and the gate, a higher current is achieved between the levels of the fresh RTN in the cases studied in the UTBB FD-SOI devices. While applying voltage to the back gate does not affect the current to any great extent when comparing RTN 2 and RTN 3.

The following case meets the majority of the fresh RTNs studied in these devices. Where RTNs are not seen at different levels but the variation in current is significant and background noise is not associated.

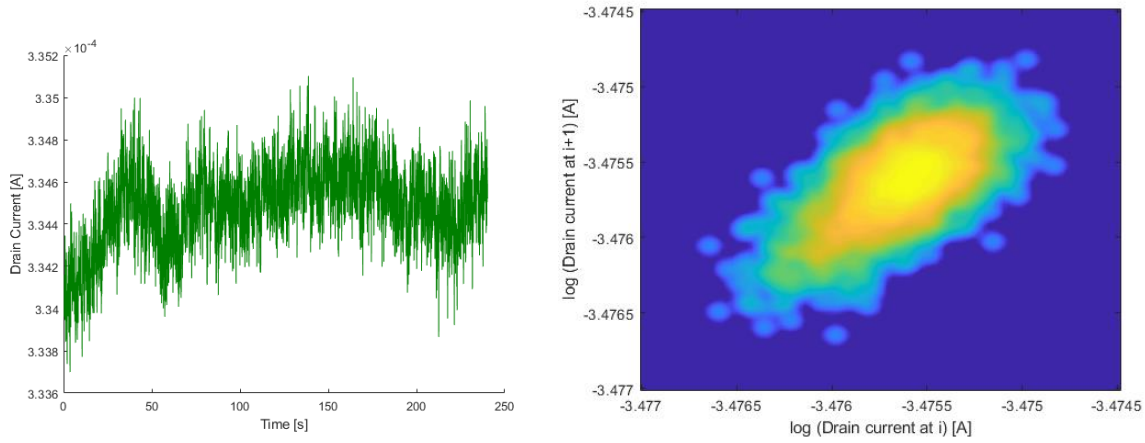

Figure 58 - Fresh RTN3 and W-TLP for transistor of 400 nm width and 10 nm length (2.2 V).

A difference of 1 µA can be seen and in the cases studied it ranges from 1 µA to 100 nm difference between peak and peak current.

The following is another of the most significant cases captured in the study, where it can be clearly perceived that by applying a higher voltage to the drain and the gate, the RTN can be observed. In addition, the W-TLP of the RTN 2 and RTN 3 clearly show the steps between the two levels as indicated.

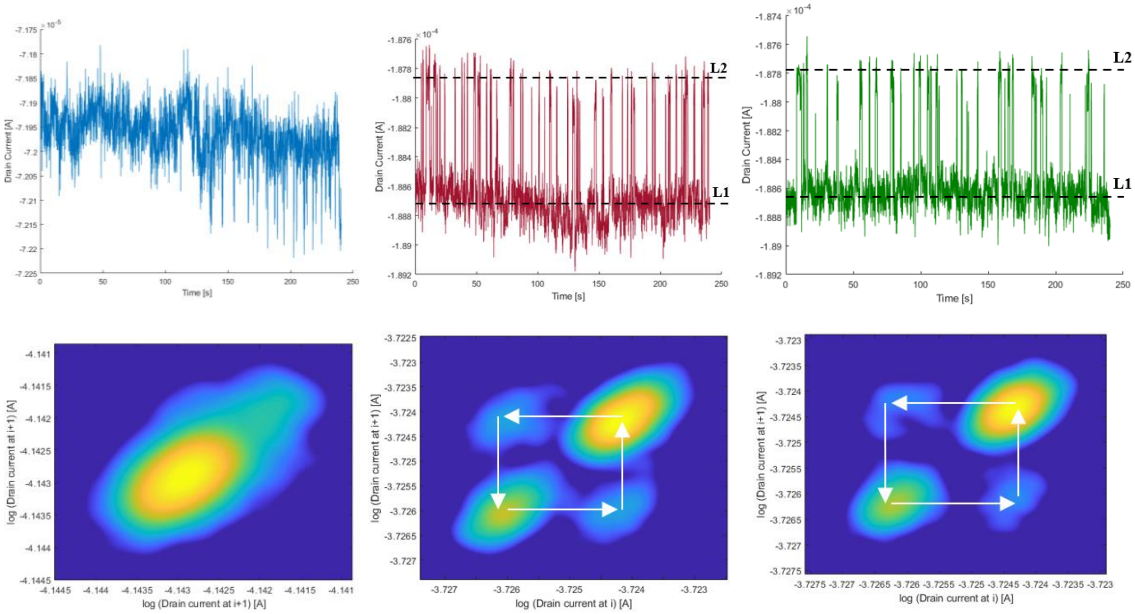

Figure 59 - Left figures represent the fresh RTN1 and W-TLP for PMOS transistor of 350 nm width and 10 nm length (1.8 V). Middle figures represent the fresh RTN2 and W-TLP for PMOS transistor of 350 nm width and 10 nm length (1.8 V). Right figures represent the stress RTN3 and W-TLP for PMOS transistor of 350 nm width and 10 nm length (1.8 V).

For both the RTN 2 and RTN 3 it is again noted that applying a voltage of -15V to the back gate has very little effect on the RTN levels, in this case they are at -187.8 µA and -188.6 µA. These are negative values because a PMOS has been analysed.

5.1.2 Stress characterization of random telegraph noise with SPA

Once the fresh RTN has been analysed, the devices are then stressed to obtain the stressed RTN with the RTN 1, RTN 2 and RTN 3 configurations with which the results are being investigated. These RTNs are obtained after each stress cycle which duration is 200s to 400s at different voltages depending on the device, 1.8V, 2.0V and 2.2V.

In the following case the work is focused in the NMOS transistor of 300 nm width and 10 nm length. Where all the RTNs are sampled for each of the 10 stress cycles at 2.2V in addition to the fresh RTN for comparison. Mention that most of the cases belong to this noise shown below.

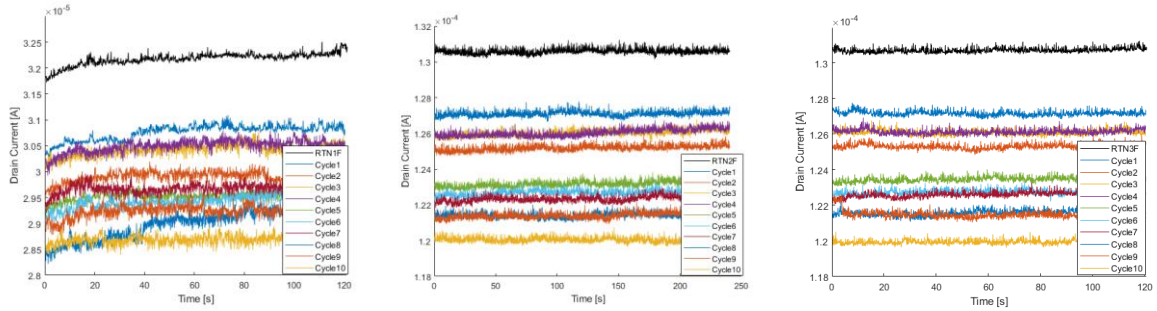

Figure 60 - Ten cycles degradation of RTN 1 (left figure), RTN 2 (middle figure) and RTN 3 (right figure) for transistor of 300 nm width and 10 nm length (2.2 V stress).

As has been seen, the RTN is also affected by degradation by lowering the current levels of the RTN. For each stress cycle applied, RTN 1 reduces the current by between 300 nA and 2.5 µA per cycle, while RTN 2 and 3 reduces the current by between 500 nA and 4 µA. Another relevant fact is that from the first fresh state to the first stress cycle the degradation of RTN is the biggest change of behaviour compared to the other stress cycles.

On the other hand, in devices with greater area, 2400 nm width and 10 nm length, RTN is also observed. As shown in the following figure, the degradation per cycle continues to increase after each cycle and the W-TLP is ruled by cycle 4, in which it has a current drop of 2.2 mA over the second one, which clearly shows the two levels in which it works. The rest of the cycles have a difference between their two main levels of 0.9 mA to 1.6 mA.

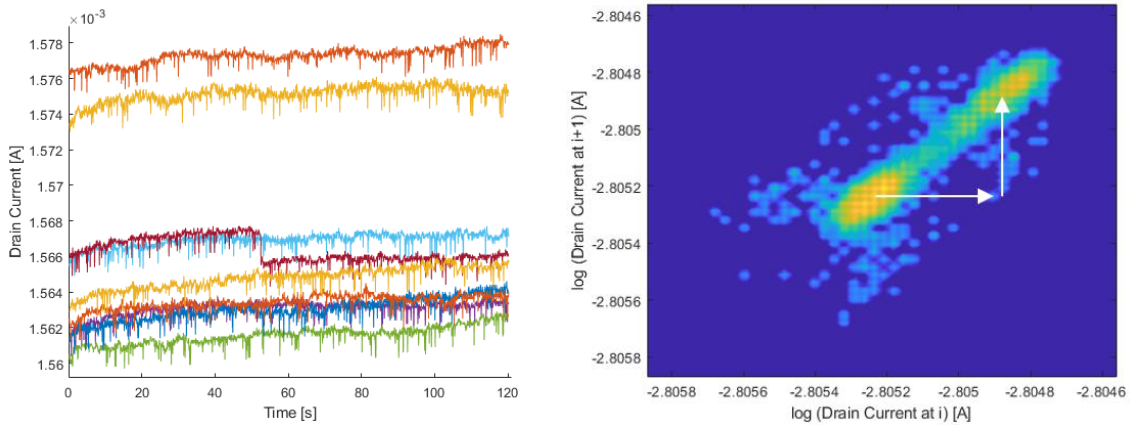

Figure 61 - Stress RTN1 and W-TLP for transistor of 2400 nm width and 10 nm length (1.8 V) in cycle 4.

The following PMOS of 300nm width and 15 nm length have shown relevant RTN levels. A PMOS degradation works in the opposite way to a NMOS.

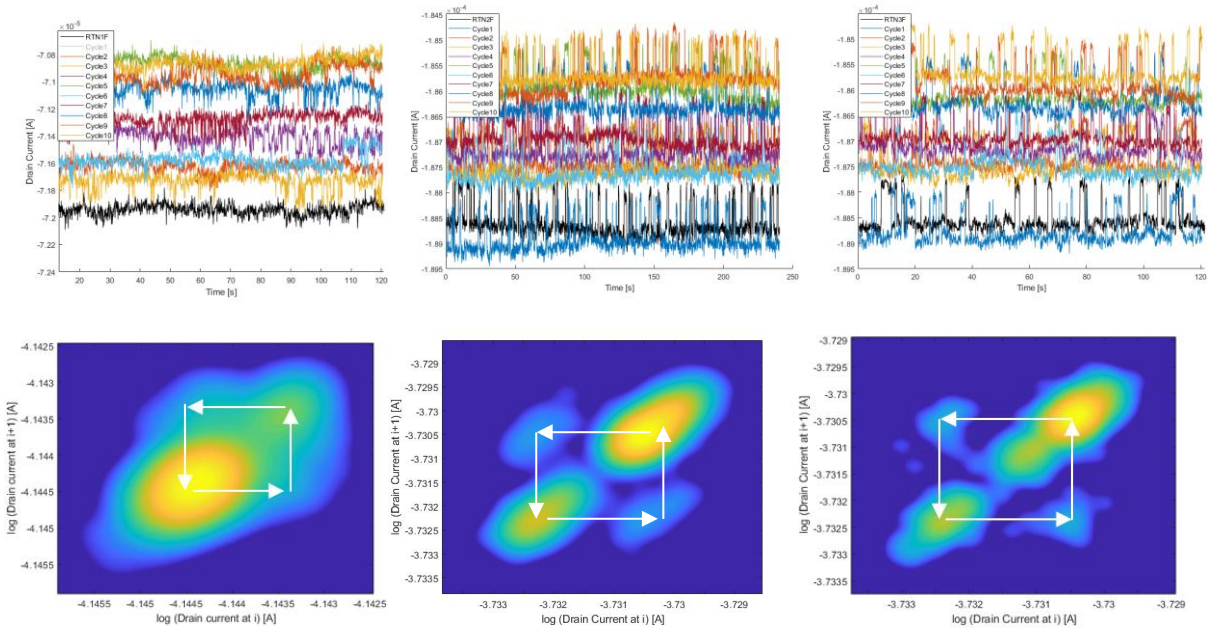

Figure 62 - Left figures represent the stress RTN 1 and W-TLP for PMOS transistor of 300 nm width and 15 nm length (1.8 V) in cycle 4 (purple). Middle figures represent the stress RTN 2 and W-TLP for PMOS transistor of 300 nm width and 15 nm length (1.8 V) in cycle 6 (blue). Right figures represent the stress RTN 3 and W-TLP for PMOS transistor of 300 nm width and 15 nm length (1.8 V) in cycle 8 (blue).

For RTN 1 the degradation between cycles falls between 50 nA and 300 nA while the RTN levels of the cycles are separated between 100 nA and 200 nA. On the other hand, in the case of RTN 2 and RTN 3 their levels are differentiated between 900 nA and 1.1 µA while the degradation is between 200 and 500 nA, higher values than for RTN 1 due to the applied voltage of 0.3 V as opposed to 0.5 V.

The following figures have been made with a device of 350 nm amplitude and 10 nm length applying a stress of 1.8V per cycle, in order to be able to see the RTN for the three configurations described and to see any cycle, in this case cycle 3, to observe the trace of the RTN.

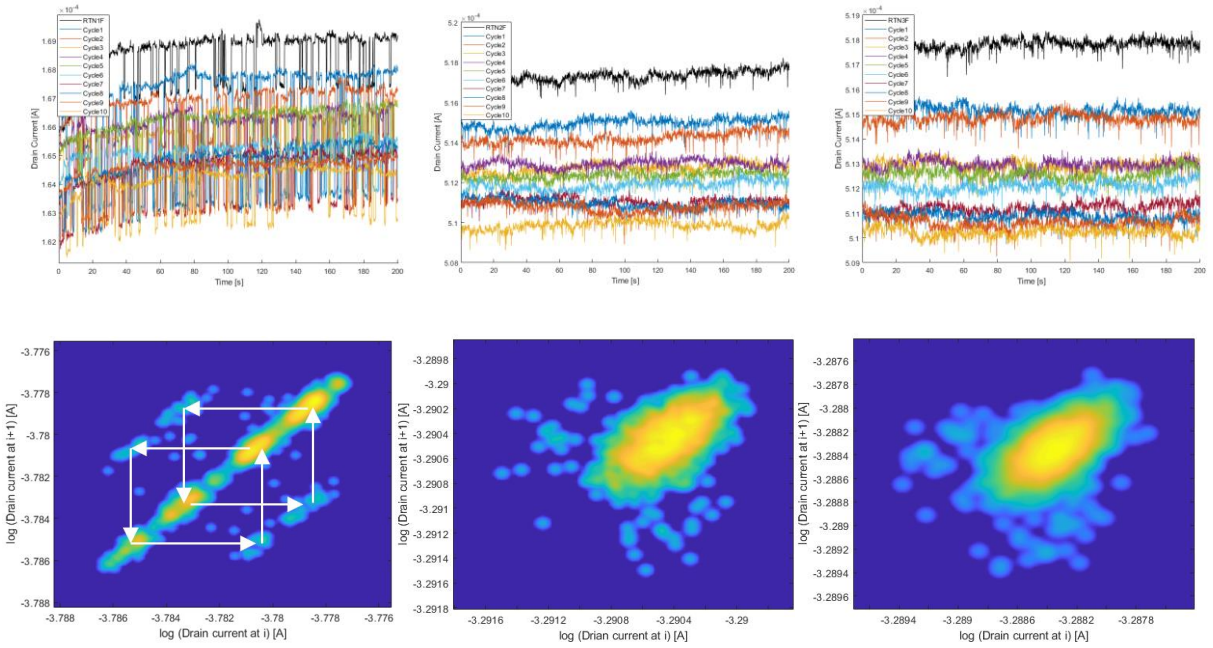

Figure 63 - Top figures show the current traces as a function of time captured to analyse the RTN after each stress cycle (10 cycles), and Bottom figures show the WTLP of the trace of the cycle 3 (orange line in top figures). From left to right figures show the RTN1, 2 and 3 respectively. This RTN was captured in different devices with the same width (350nm) and length (10nm) after each cycle of the BTI stress sequence (Vstress=1.8V).

As observed in the figures the RTN is better observed during the RTN1 characterization (VD=VG=0.3V). The trace shows multiple RTN levels, that appear clearly in the WTLP where multiple peaks are observed in the diagonal. Some of these levels are created by sub-levels of RTN as seen in some cases in this study. In this case, the focus should be on RTN 1, which has the same levels as RTN 2 and 3 compared to the others, and therefore increases the noise considerably.

Finally, in order to summarize the study of the fresh RTN and the stress of all the devices studied, the following table has been made where the dimensions of the devices are shown, if it had tension in the back gate and the cycles that it has been possible to stress along with its voltages. Some of them have not managed to reach 10 cycles because they ended up breaking. The fresh RTN and the stressed RTN that is shown, have different colours that correspond to: red if there is no RTN (the difference in current is not associated with the random telegraph noise), yellow for the case in which no RTN is observed either in the graphics or in the W-TLP but the current cannot be linked to background noise as it is much higher and the currents are similar to those of the random telegraph noise and finally green where the RTN has been captured. Everything for each of the different RTN configurations applied.

Type	Width [nm]	Length [nm]	Back Gate	Fresh RTN			Stress Voltage	Life cycles	Stress RTN		
				RTN1	RTN2	RTN3			RTN1	RTN2	RTN3
NMOS	300	10	-				1.8 [V]	0			
NMOS	300	10	-				1.8 [V]	3			
NMOS	300	10	-				2.0 [V]	9			
NMOS	300	10	-15V				2.0 [V]	4			
NMOS	300	10	-				2.2 [V]	10			
NMOS	300	10	-				2.2 [V]	0			
NMOS	300	10	-				2.2 [V]	8			
NMOS	300	15	-				1.8 [V]	10			
PMOS	300	15	-				1.8 [V]	10			
NMOS	300	20	-				2.2 [V]	9			
NMOS	350	10	-				1.8 [V]	10			
NMOS	350	10	-				2.0 [V]	10			
NMOS	350	10	-				2.0 [V]	2			
NMOS	350	10	-15V				2.0 [V]	2			
NMOS	400	10	-				1.8 [V]	3			
NMOS	400	10	-				2.0 [V]	10			
NMOS	400	10	-15V				2.0 [V]	3			
NMOS	400	10	-				2.2 [V]	10			
NMOS	1200	10	-				2.0 [V]	10			
NMOS	2400	10	-				1.8 [V]	10			
NMOS	2400	10	-				2.0 [V]	10			
NMOS	10000	10	-				2.0 [V]	0			
PMOS	10000	10	-				2.0 [V]	10			

Table 6 – RTN fresh and RTN stress summary. The grey colour is when the devices is broken, the red colour when the RTN is not detected, the yellow colour is when the RTN is not detected but the current fluctuation is not associated to white noise and green colour is when the RTN is detected.

5.2 Random telegraph noise results with remote pulse measure unit

In order to continue to complete the study of the RTN, it has been decided to look at lower time resolutions of seconds and try to see if the RTN continues to appear in these time periods. The

following flow shows how the devices studied have been worked on by applying the RPM, remote pulse measure unit, between the tip table and the SMU.

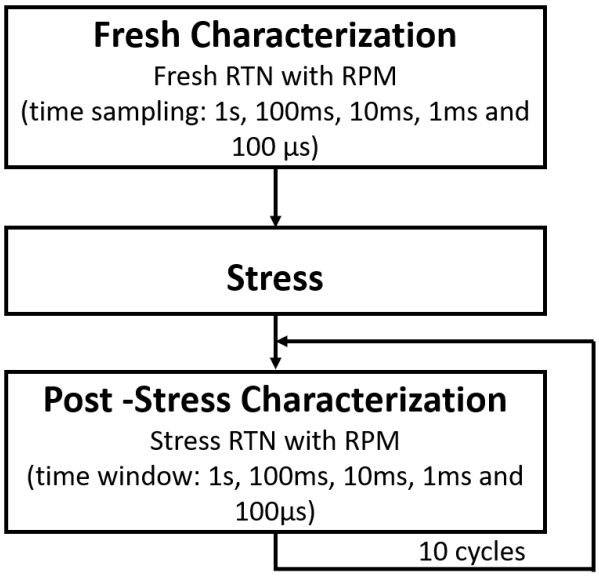

Figure 64 - Workflow for detect RTN post-stressed devices with applying the remote pulse measurement between the SMU and the tip table.

Time resolution times have been reduced from 1s to 100 µs by a factor of 10 in steps. For each time window the maximum number of points that can be acquired with the implemented setup is 4096 so the sampling time is the time executed divided by the 4096 points. So, looking for the fresh RTN in the mentioned temporal resolutions and applying a channel hot carriers stress because the degradation it produces is bigger than if an bias temperature instability stress applied. It has been a 30 second stress with 2.2V voltages.

The configuration of the RTN obtained with the RPM is a 0,7 gate constant voltage and 0,1 drain constant voltage with 0V in the back gate.

Then, in this section is going to observe some cycles of the fresh and stressed RTN of the UTBB FD-SOI to know the behaviour.

5.2.1 Fresh characterization of random telegraph noise with RPM

Both the fresh and the stressed characterisation of the random telegraph noise use the smaller devices analysed because the effect of the RTN is greater than in the larger devices.

The cycle 1 of the 300 nm width and 10 nm length device is shown in the fresh state for the time resolutions of 1 second, 100 ms and 1 ms. Applying 0.5V voltages to the drain and the gate.

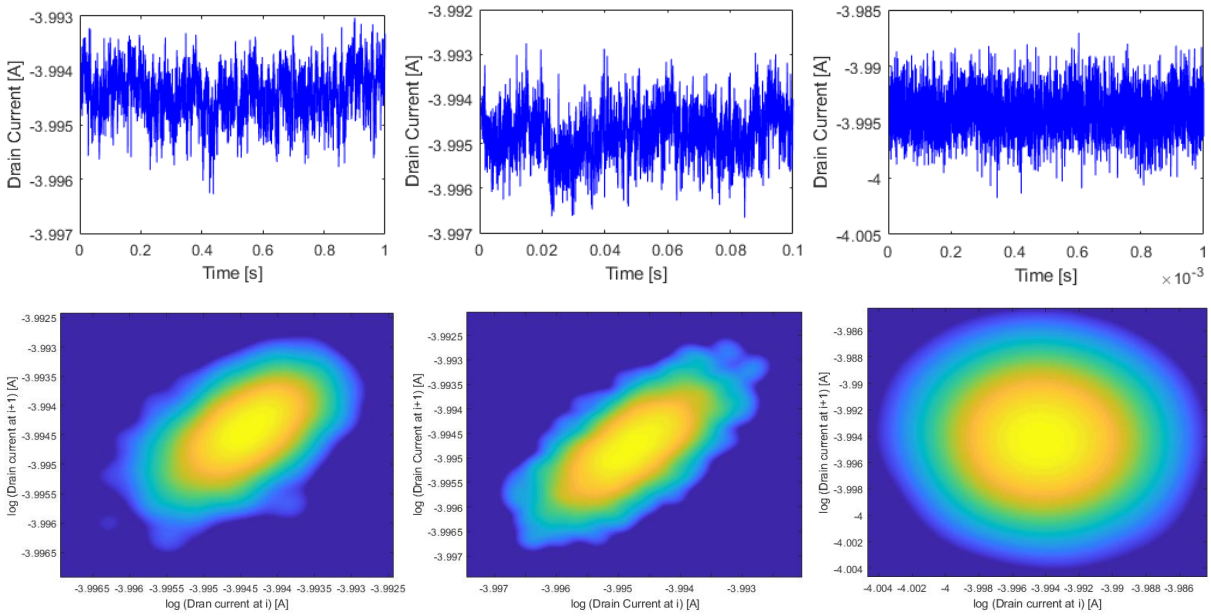

Figure 65 - Left figure is the cycle 1 of fresh device with temporal resolution of 1 s. Middle figure is the cycle 1 of fresh device with temporal resolution of 100 ms. Right figure is the cycle 1 of fresh device with temporal resolution of 1 ms. All the fresh figures are representing a device with 300 nm width and 10 nm length dimensions.

RTN has not been captured in the fresh cycles of the devices and buying it with the previous fresh points still corroborates that it is not very significant. It can be seen that there is only one main level and all the points are grouped together at this point.

5.2.2 Stress characterization of random telegraph noise with RPM

The stressed characterisations of the random telegraph noise are now shown as 30 seconds of channel hot carriers (CHC) at 2.2 V have been applied to them. A study of the different cycles in the same device will be made to know if this is affected and on the other hand the visualization of the RTN in different times will be studied.

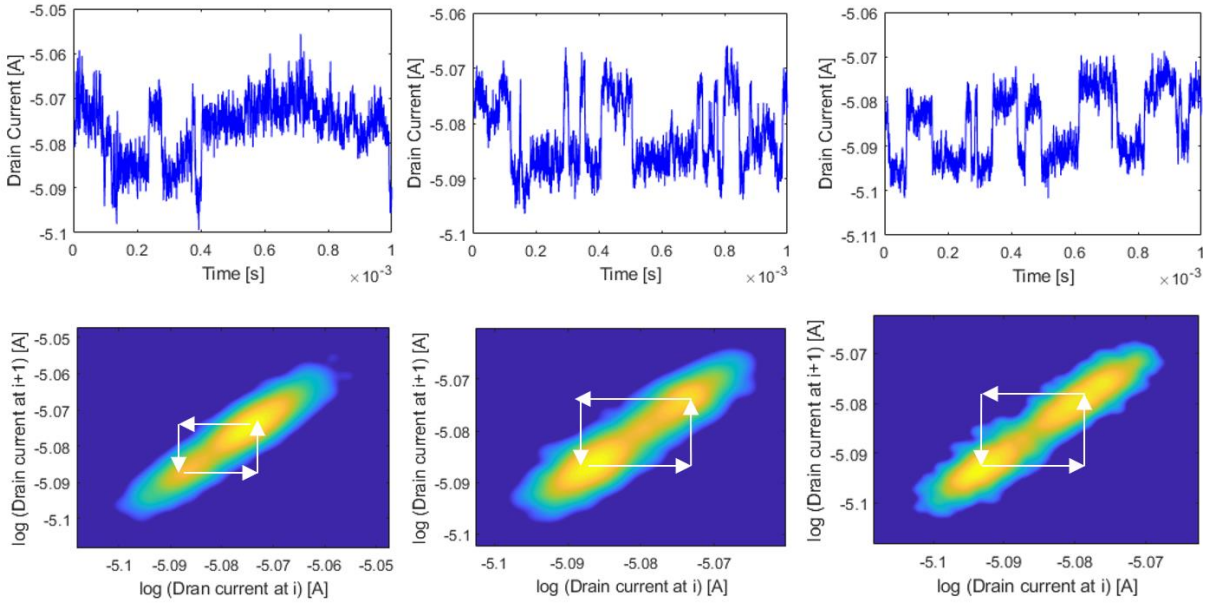

Figure 66 - Right figure is the cycle 1 with temporal resolution of 1 ms. Middle figure is the cycle 3 with temporal resolution of 1 ms. Right figure is the cycle 5 with temporal resolution of 1ms.

As can be seen in Figure 66, the RTN becomes more relevant as the cycle increases, although the currents are the same, the two levels differ more and more cycle after cycle. The only change that has taken place is the change of cycle, the temporal resolution has been 1 ms to be able to see this conclusion.

It is important to mention that de steps of this RTN in this section do not appear because the number of steps (jumps) between levels represent a small number of samples compared to the total, approximately 10 samples versus 4096.

Next, the same cycle is analysed, but at different time resolutions, in order to see where a higher RTN is obtained. The following picture apart to give diversity of time windows, it gives how the W-TLP and the plot of RTN have a connection in the levels (defaults) when the figures are in parallel.

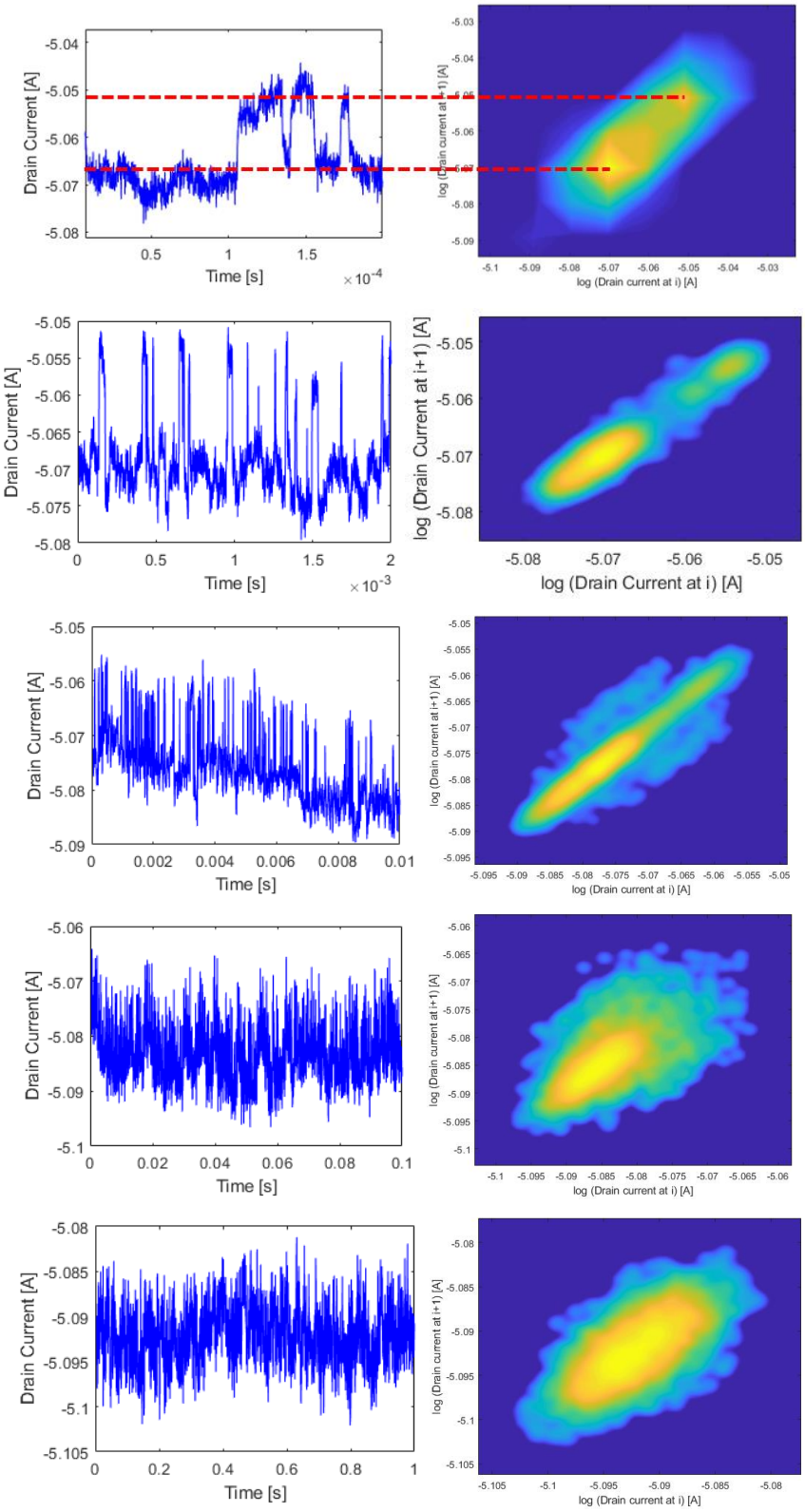

Figure 67 - The figure represents the cycle 1. Left figures have the temporal resolution of 100 µs, 1ms, 10ms, 100ms, 1s. Right figures have the W-TLP of the RTN.

It has been possible to see that in the resolutions of 100 µs and 1 ms the RTN is clearly differentiated while in the other resolutions of 10 ms, 100 ms and 1 s current amplitudes are appearing not associated with the background noise but the RTN is not detected, it is not possible to capture. With this information it is corroborated that it is RTN in the previous cases, but it is masked by the temporal resolution, it is the case that appears in yellow in the table 6.

Finally, as a conclusion, it has been observed that the more stress cycles applied, the more RTN appears, so that the degradation causes RTN, besides the fact that the temporal resolution affects the capture of this RTN.

Lastly, it has been observed, it should be checked, that in most cases the results have a big amplitude too that cannot be associated to the background noise when its studied the RTN without applying the RPMs. This noise has been associated to the RTN that cannot be captured without the RPMs, for this reason the RPM modules have been used, managing to capture RTNs in smaller times.

6. Conclusions

This final master project has focused on the experimental characterization of ultra-scaled FD-SOI N-type transistors. As well as in the study of the effects of BTI (Bias Temperature Instabilities) degradation, and of its variability caused by the RTN (Random Telegraph Noise) effect typical of the channel current of the ultra-scaled transistors.

The fresh characterization of N-type FD-SOI transistors has been observed:

- The channel current observed in the transistor characteristics is dependent on the width W and length L of the transistor channel as indicated. Depending on the length of the transistor, the drain current increases when the device has a smaller length and increases when this dimension decreases, in addition the sub-threshold slope also decreases for larger lengths.
- On the other hand, comparing the devices with different amplitudes and equal lengths, it can be seen that the gate and drain current increase if the amplitude is greater and the sub-threshold slope decreases when the transistor has less W.
- The variability between fresh transistors of the same dimensions, before any stress (in time 0) does not always give the same response, in terms of the currents with which it is in operation. In small devices this variation is as big as changing the length or amplitude of a device, this phenomenon is due to manufacturing defects.

The degradation by BTI studied has been observed:

- By applying different stress voltages to the gate terminal (1.8V, 2.0V and 2.2V) the degradation observed, even if present, is very insignificant. Therefore, the dependence of the degradation on the stress voltage could not be verified very well either.
- A stress of less than 1.8V cannot be applied because the degradation is very small and not more than 2.2V because the transistors cannot support to exceed so much voltage, the oxide of the gate broken (dielectric breakdown).
- By degrading the devices with BTI degradation, it has been possible to observe that all currents are affected as stress cycles are applied, but this variation in current is very small.

- The electrical characteristics of the UTBB FD-SOI are degraded and comparing different channel dimensions it is observed that the degradation is not of great relevance to affect the behaviour of the device. Its degraded threshold voltage differs from the threshold voltage in the fresh state by an average of 8.1% and its mobility is also affected by an average of 9.3% after examining the degraded cycles. Very similar values have also been obtained when comparing the same device with different stress voltages, so that the degradation of the device is not affected. Both the degradation with different dimensions and with different stress values is very small, which means that it is suitable for industrial use.

As for the RTN studied:

- With the capture of the RTN traces by the SPA, little RTN has been observed in general, being this much more notorious or visible in the samples of smaller width. In addition, more RTNs have been observed with small characterization voltages, close to the threshold voltage value of the device.
- Regarding the RTN, by applying more voltage to the drain and the gate (0.3 V vs 0.5 V) a higher current is achieved in the cases studied in the UTBB FD-SOI devices both in fresh and stressed states, apart from having a more noticeable RTN.
- Some tests have been done degrading the device by activating CHC degradation, and it has also been observed that this degradation is more significant than the BTI for the same voltages (~2V). Moreover, the CHC degradation caused generates more defects that cause more RTN than in BTI degraded devices.
- The time resolution affects the capture of the RTN, there are defects that cause current jumps with faster capture and emission times. When using RPM, which allows a higher temporal resolution to capture the intensity, a greater number of defects appear, and therefore many more steps typical of the RTN, only observable at different temporal resolutions greater than that of the SPA. Thus, little RTN has been observed in the time scale of the characterization with the SPA, but the characterization of the RTN with the RPM has revealed many more defects, and therefore more RTN, not captured with the SPA. This shows that for a good and complete characterization of the RTN it is necessary to obtain data with different resolutions and time windows, and therefore to be able to capture slow defects and fast defects, which can both be present in the same device.

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