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# DESIGN AND ANALYSIS OF TWO LOW POWER SRAM CELL STRUCTURES

## *Bachelor of technology in electronics and communication*

*SUBMITTED BY-*

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UNDER THE SUPERVISION OF

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May 2014

## *Certificate*

This is to certify that the thesis entitled Development of two low power Sram cell
Structures by Kirtidipan Behera for fulfillment of requirements for award of bachelor of technology in Electronics and communication engineering at the National Institute of Technology, Rourkela, is an authentic work carried
out by him under my supervision and guidance. To the best of my knowledge, the
matter embodied in the thesis has not been submitted to any other university / insti-
tute for the award of any Degree or Diploma.

Prof. Munshi Nurul Islam

Dept. of Electronics and Communication Engineering

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## Abstract :-

In this paper, two static random access memory (SRAM) cells that reduce the static power dissipation due to gate and subthreshold leakage currents are presented.

The first cell structure results in reduced gate voltages for the NMOS pass transistors, and thus lowers the gate leakage current. It reduces the subthreshold leakage current by increasing the ground level during the idle (inactive) mode.

The second cell structure makes use of PMOS pass transistors to lower the gate leakage current.
In addition, dual threshold voltage technology with forward body biasing is utilized with this structure to reduce the subthreshold leakage while maintaining performance.

Compared to a conventional SRAM cell, the first cell structure decreases the total gate leakage current by 66% and the idle power by 58% while the second cell structure reduces the total gate leakage current by 27% and the idle power by 37% with no access time degradation.

***Index Terms***— Dual threshold, gate leakage, low-power, static power, static random access memory (SRAM) cell, tunneling current

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# I. Introduction

The International Technology Roadmap for Semiconductors predicts the gate equivalent oxide thickness as low as 0.5 nm for future CMOS technologies. Since the gate leakage current of MOS transistors increases exponentially with the reduction of the oxide thickness over the active region of a transistor, the gate leakage power dissipation is expected to become a significant fraction of the overall chip power dissipation in nanometer CMOS design processes. The International Technology Roadmap for Semiconductors predicts the gate equivalent oxide thickness as low as 0.5 nm for future CMOS technologies . Since the gate leakage current of MOS transistors increases exponentially with the reduction of the oxide thickness over the active region of a transistor, the gate leakage power dissipation is expected to become a significant fraction of the overall chip power dissipation in nanometer CMOS design processes . The gate tunneling current is predicted to increase at a rate of 500x per technology generation whereas the subthreshold current increases by only 5x. With the dependence of the leakage power on the number of transistors, and given the projected large memory content of future system on chip (SoC) devices (more than 90% of the die area by 2014 ), it is important to focus on minimizing the leakage power of SRAM structures. There are several sources for the leakage current, i.e., the subthreshold current due to low threshold voltage, the gate leakage due to very thin gate oxides, and band-to-band tunneling leakage due to heavily-doped halo doping profile . Because of the exponential dependency of the gate leakage current on the oxide thickness, this current has the potential to become the dominant factor for future CMOS technologies.

The tunneling current is composed of three major components:

1) gate-to-source and gate-to-drain overlap currents (edge direct tunneling current)

2) gate-to-channel current (direct tunneling current)
3) gate-to substrate current

In bulk CMOS technology, the gate-to-substrate leakage current is several orders of magnitude lower than the overlap tunneling current and gate-to-channel current. In the ON state, in addition to the overlap tunneling currents, the gate-to-channel tunneling is added to the gate current increasing the total gate tunneling current in this state. There are several techniques for reducing the gate tunneling leakage in digital circuits . These techniques reduce the leakage based on the dependencies of the tunneling currents on the terminal voltages, the gate oxide thickness, and the type of the transistor. One of the techniques is to employ PMOS transistors instead of NMOS transistors. In the PMOS transistor, the gate tunneling current is an order of magnitude lower than that of the NMOS transistor in the inversion regime in the same technology. This mainly originates from the higher barrier height (4.5 eV) for the hole tunneling compared to the lower barrier height (3.1 eV) for the electron tunneling . The exponential dependence of the tunneling current on the barrier height and its linear dependence on the transistor width results in a much smaller tunneling current compared to that of NMOS transistor even when the PMOS transistor is made 2–3 times wider than the NMOS transistor. Another method for reducing the gate leakage current minimizes the voltage difference between the gate to the source or the drain terminals.
Historically, VLSI designers have used circnit speed **as** the "performance" metric.
Large gains **in** terms of performance and **silicon area,** have **been** made for digital processors, microprocessors, **DSPs** ( Digital Signal Processors), ASICs (Application Specific ICs), etc. In **general, "small area"** and "high performance" **are** two conflicting constraints. The IC designers' activities have been

involved in trading off these **constraints.** Power dissipation issue **was** not *a* **de**
**sign** criterion but an afterthought. In fact, power considerations have been the
ultimate design criteria in special portable applications such as wristwatches
and pacemakers for a long time. The objective in these applications was minimum
power for maximum battery life time.
Recently, power dissipation is becoming an important constraint in a design.
Several **reasons** underlie the emerging of this issue. Among them we cite:
Battery-powered systems such as palmtop/notebook ,computers, electronic
**organisers,** etc. The need for these systems **arises** from the need to extend
battery life. Many portable electronics **nse** the rechargeable Nickel Cadmium
(NiCd) batteries. Although the battery industry has been making
efforts to develop batteries with higher energy capacity than that of NiCd,
a strident increase does not seem imminent. The expected improvement
of the energy density **is** 40% by the turn of the century. With **recent**
NiCd batteries, the energy density is around 20 Watt-hour/pound and
the voltage is around 1.2 V. So, for example, for a notebook consuming a
typical power of 10 Watts and using 1.5 pound of batteries, the time
of operation bdween recharges **is** 3 hours. Even with the advanced battery

technologies. such as Nickel-Metal Hydride (Ni-MH) which provide large

energy density characteristics (- 30 Watt-hour/pound), the life time of the battery is still low. Since battery technology has offered a limited improvement.
low-power design techniques are essential for portable devices.
Low-power design is not only needed for portable applications but also
to reduce the power of high-performance systems. With large integration
density and improved speed of operation, systeme with high clock frequencies
are emerging. These systems are using high-speed products snch as microprocessors. The cost associated with packaging, cooling and fans
required by these systems to remove the heat is increasing significantly.
At higher frequencies, the power dissipation is too excessive.
Another issue related to high power dissipation is reliability. With the generation of on-chip high temperature, failure mechanisms are provoked
Among them, we cite silicon interconnect fatigue, package related failure, electrical parameter shift. electromigration, junction fatigue, etc..
In addition, there is a trend to keep the computers from using more than
5% scheduled of the total US power budget. Note that 50% of office power
is used by PCs. Since the processors' frequency is increasing, which results
in increased power, then low-power design techniques are prerequisites.
The power dissipation issues and the devices' reliability problems, when they
are scaled down to 0.5 um and below. have driven the electronics industry to
adopt a supply voltage lower than the old standard, 5 V. The new industry standard

for IC operating voltage is 3.3 V (i 10%). The effect of lowering the voltage to much lower values **can** be impressive in terms of power saving.
The power is not only reduced but also the weight and volume associated with
batteries in battery-operated systems.

In order to optimize the power dissipation of digital systems low-power methodology
should be applied throughout the design process from system-level to **processor-level,** while realizing that performance is still essential. During optimization,
it is very important to **know** the power distribution within **a** processor
Thus. the parts **or blocks consuming** an important fraction of the power
**are** properly optimized for power **saving.**
The process technology **is** under the control of
the device/process designer. However, the other levels **are** controlled by the
circuit designer.

We present two design techniques that reduce the gate leakage current in the SRAM cells. In both designs, we focus on the static power dissipation in the idle mode where the cell is fully powered on, but no read or write operation is performed. The rest of the paper is organized as follows. In Section II, we have described about three structures of SRAM cell .While simulations results are discussed in Section III. Finally, summary and conclusions are provided in end.

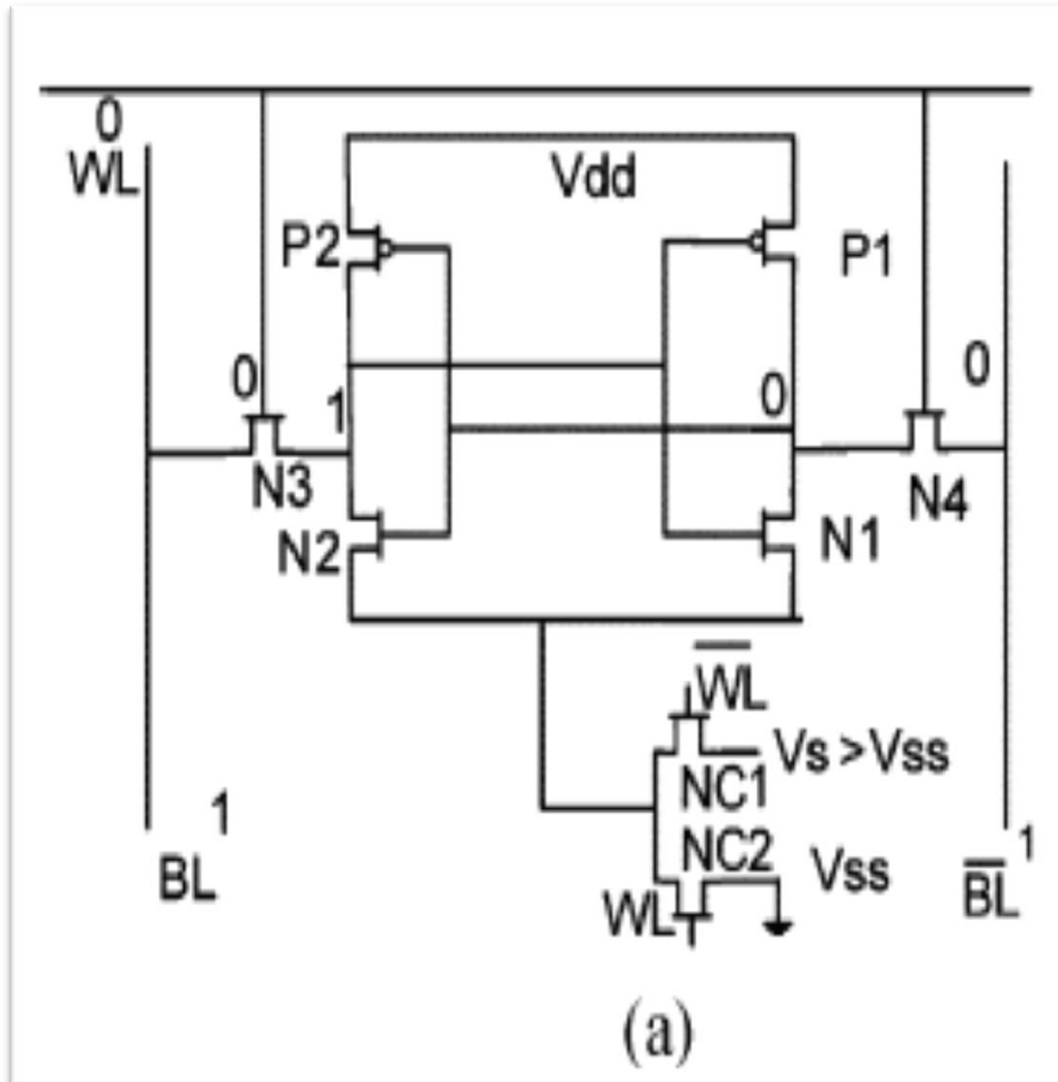
## II. REVIEW OF RELATED WORKS

In this section, we review some of the previously proposed SRAM cell structures. In [6], an asymmetric SRAM cell design is presented where an NMOS transistor is added to the SRAM cell to reduce the magnitude of the gate voltage when the cell stores "0" data (is in the zero state.) As a result, compared to a conventional SRAM cell design, the gate leakage decreases in the zero state while it increases in the one state. The penalty is an increase in the SRAM cell area and longer read access and write times. For this cell, the dc noise margin (data storage integrity) is nearly unchanged [6].

Another method for reducing the gate leakage current in the SRAM cell has been suggested in [3]. In this paper, the NC-SRAM design, whose circuit diagram is shown in Fig. 1(a), employs dynamic voltage scaling to reduce the leakage power of the SRAM cells while retaining the stored data during the idle mode. The key idea behind NC-SRAM is the use of two pass transistors NC1 and NC2 which provide different ground levels to the memory cell in the active and idle modes. The positive

voltage (virtual ground) reduces the gate leakage and subthreshold currents of the cell while degrading the read and write performances [3].

Using dual-gate oxide thicknesses is another approach for reducing the gate leakage current in theSRAMcell [8]. In this technique, the gate



(a)

oxide thicknesses of the NMOS pass transistors and the NMOS pull down transistors are increased. Because the much lower gate leakage of PMOStransistor, no change is made to the gate oxide thickness of the PMOS pull up transistors. To achieve a lower subthreshold current, the

dual threshold voltage technique has been used. The cell evaluation is performed by using the high threshold voltage for different transistors. In the best case, the power consumption is decreased and the stability is improved but the read access time is degraded [8]. In [9], a low power nine-transistor SRAM cell structure has been proposed. In this structure, to improve the stability in the read mode, three NMOS transistors are added to the cell to separate the read and write circuits. Indeed, the cell stability is improved at the cost of increasing the cell area.

## III. LOW GATE LEAKAGE SRAM CELLS

In this section, we describe two low gate leakage SRAM cell structures, which are denoted as IWL-VC and PP-SRAM cells.

### A.IWL VC SRAM CELL

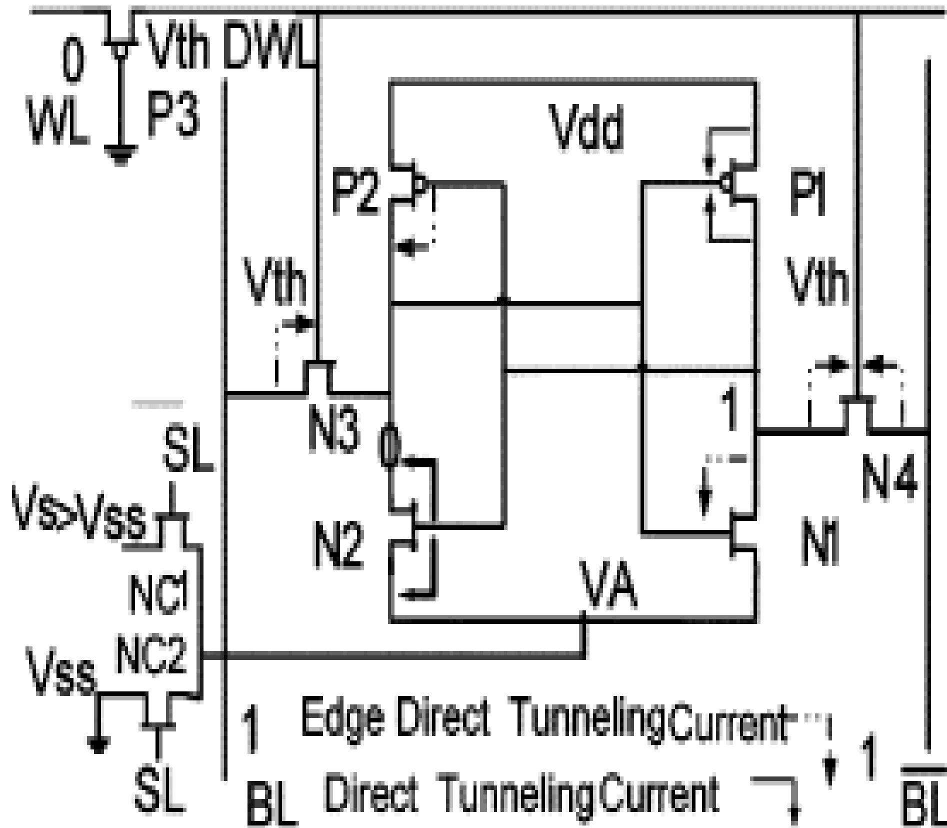
The initial configuration of the proposed SRAM cell is called word line-voltage control (WL-VC) SRAM cell [11]. In this cell, a pass transistor
P3 [similar to P3 in Fig. 1(b)] is added to the NC-SRAM cell to reduce the gate voltage of the N3/N4 pass transistors. This leads to the simultaneous reduction of both the gate tunneling and subthreshold currents
in the idle mode. In the active mode,WLis "1," and the groundedgate PMOS transistor P3 is ON, and hence, "1" is applied to the gates of transistors N3 and N4 while Vss is applied to the sources of transistors
N1 and N2. Therefore, compared to the conventional SRAM, no change in the SRAM cell occurs. When the SRAM cell changes from the active mode to the idle mode, WL changes from "1" to "0" causing the source voltage of P3 to change from Vdd in the active mode to a voltage higher than "0" (the PMOS threshold voltage, Vth in the idle mode. This causes the gate voltages of N3 and N4 to increase to Vth as well. Furthermore, the sources of N1 and N2 are connected to Vs

through NC1. Now, considering the case where a “0” is stored in the cell, Vout increases to Vs, and DWL increases to Vth [see Fig. 1(b)]. Thus, compared to the conventional SRAM cell, the absolute values of the gate-drain and the gate-source voltages of N4 and the gate-drain voltage of N3 decrease from Vdd to Vdd-Vth while the gate-source voltage of N3 is Vth-Vs. Consequently, the gate currents of transistors N3 and N4 is lowered. When the cell is storing “1,” a similar gate current reduction is achieved.

To improve the timing performance of the WL-VC SRAM cell, instead of using WL and /WL in the WL-VC SRAM cell, we use SL and /SL signals to change the ground level sooner during the active mode. Fig. 1(b) shows the new SRAM cell which is called the *improved* WL-VC SRAM (and is referred to as the IWL-VC SRAM from now on). In the read/write mode, WL (word line) and SL (select line) are high while in the idle mode, WL and SL are “0.” In this configuration, the SL is always activated before WL is activated. This minimizes the degradations in the write and read operations compared to those of the conventional SRAM cell. In memories, several control signals, which are activated at different times, are used for the read/write operations. We shall use the first control signal during the operation for activating SL whereas WL is activated similar to the conventional SRAM cell [12]. To generate the first control signal, we use the signal *Read* and /W in the SRAM in the SRAM read and the write circuitry shown in Fig. 2, [13]. In the write mode, when W is activated, the data is applied to the SRAM cell while in the read mode when *Read* is activated, the SRAM cell is ready for the read operation.

For both read and write operations, WL is activated after /W and *Read* signals are activated, and hence, the size of NC2 need not be very large in order to prevent the speed degradation of the read and write operations. When SL becomes high, NC2 turns on taking □_ (sources of N1 and N2) from Vs (0.2 V) to Vss (0). The WL signal is activated after Va has been stabilized at Vss (see Subsection IV-D for the timing diagram). Since there is enough time for discharging the capacitance of the source line, the extra delay in the access time is avoided without resulting in a very large peak current. The static power

consumption due to the two extra NMOS transistors (NC1 and NC2) is not significant. In particular, the extra power dissipation for a row of 128 SRAM cells was estimated by circuit simulation to be less than 4% of the total static power dissipation.




(b)

## B.PP SRAM CELL

We present a gate leakage current reduction method based on PMOS Pass-transistor SRAM structure which is illustrated in Fig. 3. The PMOS Pass-transistor SRAM (called PP-SRAM) cell has lower gate leakage compared to that of the conventional SRAM cell. In order to decrease the gate leakage currents of the SRAM cell, NMOS transistors N3 and N4, are replaced by PMOS transistors P3 and P4. In the active mode, WL is held at "0" to turn on the two pass transistors. In the idle mode, WL is charged to Vdd so that the two PMOS pass transistors are OFF, isolating the PP-SRAM cell from BL and BL. During this time, the bit lines are typically charged to Vdd.
For this cell, the only gate leakage current of the pass transistor is Igd3, while in the conventional SRAM cell, three gate leakage currents, i.e.Igd3,Igd4 and Igs4 are present. This fact alone leads to a considerable reduction in the gate leakage current of the SRAM cell. The use of PMOS pass transistor, however, may lead to performance degradation due to different mobility coefficients for the NMOS and PMOS transistors. To overcome this problem, the width of PMOS pass transistor is selected as 1.8 times of that of the NMOS for the technology used in this work. The ratio was obtained using HSPICE simulations for having the same transient characteristics for both types of transistors.
To decrease the subthreshold current in addition to the gate leakage current, the PMOS transistors with a higher threshold voltage may be used. In the proposed SRAM cell design, PMOS transistors with high threshold voltage (Vth = -0.26V) and NMOS transistor with typical threshold voltage in 45-nm technology (Vth = 0.22 V) are used [14]
As observed from Fig. 3, when "0" ("1") data is stored, the subthreshold currents of P2 (P1) and P3 (P4) are reduced and the subthreshold current

of N1 (N2) remains the same. In order to reduce the negative impact of high threshold voltage on the speed of the PP-SRAM, a forward body biasing method is used. In this method, the body bias voltage of PMOS transistor in the idle mode is set to Vdd (via P5) while in the active mode it is set to Vdd/2 (via P6). The circuit diagram of the PP-SRAM cell with the body bias driver P5 and P6 is shown in Fig. 3. Similar to IWL-VC SRAM cell, the select line (SL) signal is used to switch between the two body bias voltages. The signal is generated by the row decoder circuit. Note that the voltage of Vdd/2 can be generated
using an on-chip dc-dc converter or may be supplied externally. Since SL is activated before WL is activated for the read/write operation,
the timing performance deterioration is prevented. It is important to point out that due to the use of the PMOS transistors, there is an increase
in the dynamic power of the cell which is consumed during the read and write operation. Since static power is much more important than dynamic power in large memories, static power saving will very well compensate for the increase in dynamic power dissipation. In addition,
the static power consumption induced by the two new inserted PMOS transistors (P5 and P6) is small. From circuit simulations, this component of power dissipation for a row of 128 SRAM cells was determined
to be less than 2% of the total static power dissipation.

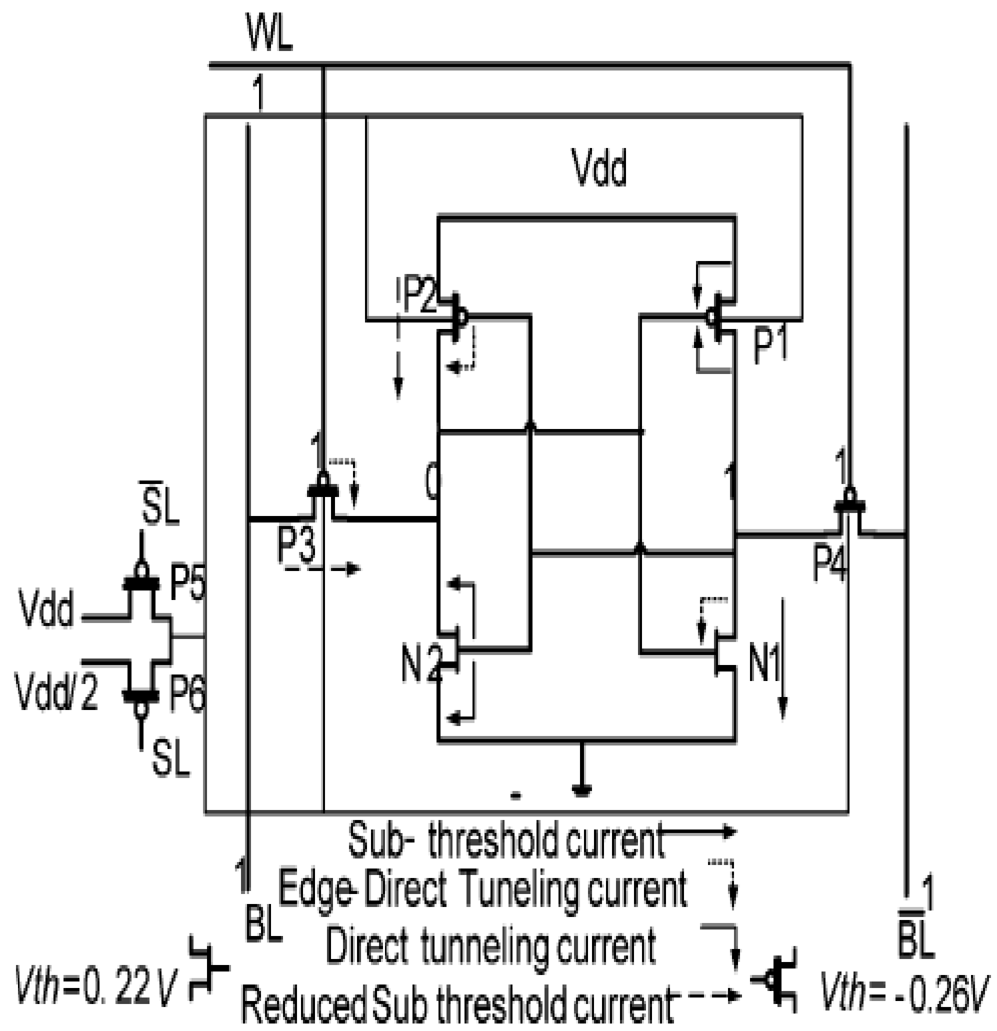



Fig. 3. Proposed PP-SRAM cell (holding "0") with gate leakage currents.

## IV. RESULTS AND DISCUSSION

To evaluate the efficiency of the proposed SRAM cells, we performed HSPICE circuit simulations for a 45-nm technology with the oxide thicknesses of 1.4 nm (the typical oxide thickness in the 45-nm technology is 1.4 nm) [14]. In the simulations, temperatures of 25 C, 50 C, and 100 C and the supply voltage of Vdd= 0.8V were used. The channel widths of the main PMOS and NMOS transistors in the cell were 0.4 um and 0.2 um, respectively.

### *A. Gate Leakage and Static Power Dissipation*

Simulation results of the gate leakage for all structures at the three temperatures of 25C, 50C, and 100C are presented in Fig. 4(a).
As the results reveal, the leakage of the NC-SRAM cell, which makes use of two NMOS transistors for each row, is reduced by almost 50% compared to that of the conventional SRAM cell. The same reduction for the asymmetric SRAM cell of [6] is only about 20%. In the first proposed structure, IWL-VC SRAM, with two NMOS and one PMOS transistors for each row, the gate leakage is reduced by about 66%. For the 9T-SRAM cell of [9], which uses three more NMOS transistors, the gate leakage is lowered by 15%. At last, in the PP-SRAM cell, by replacing
the two NMOS pass transistors with PMOS pass transistors, the gate leakage current is reduced by almost 26%. The maximum leakage reduction is achieved by the IWL-VC SRAM structure while the minimum
reduction is seen in the asymmetric SRAM.

The total static power dissipations (included all leakage current components)
for the SRAM cell structures are given in Fig. 4(b) at 25C, 50 C, and 100 C. As observed from the figure, compared to the conventional
cell, only the asymmetric SRAM cell results in no static power saving. This can be attributed to the added NMOS transistor in this cell. For the 9T-SRAM cell, the static power reduction is smaller (7.7%) because
there are more transistors in the cell. The power dissipations in the NC-SRAM and the IWL-VC SRAM cell are similar and are 57% smaller than that of the conventional SRAM cell. Note that the power dissipations of added transistors in the NC-SRAM and IWL-VCSRAM cells are negligible. In PP-SRAM cell, use of the PMOS pass transistors and the high threshold PMOS transistors reduces the power dissipation by 37%. As will be seen later, although the power dissipation and the leakage of the PP-SRAM cell are higher than those of the NC-SRAM and the IWL-VC SRAM cells, its read and write access times are the same as those of the conventional SRAM cell.
As known in the literature and seen in the figures, the gate leakage current does not depend on the temperature. The subthreshold leakage current, however, strongly depends on the temperature, making the total static power dissipation a strong function of the temperature. The power consumptions at different temperatures reveal that the same trends of power reduction for different cells exist at higher temperatures too. Finally,
although the static power dissipation of the IWL-VC SRAM and NC SRAM cells are the same, the gate leakage of the IWL-VC SRAM is 34% less than that of the NC-SRAM mainly due to lower gate leakage currents of transistors N3 and N4. This is the main advantage of the IWL-VC SRAM compared to NC-SRAM. This gate leakage current

decrease reduces the power dissipation of the row decoder due to the leakage current from the word line of each row which consists of many cells (say, from 32 to 512).

### *B. Area*

The layouts of PP-SRAM and conventional SRAM cells drawn in a 45-nm standard CMOS technology are given in Fig. 5. Since the layout guidelines for the 45-nm technology was not available to us, we have used the layout guidelines presented in [15] which are a scaled version of the 90-nm technology. They could also be obtained by scaling the sizes and dimensions given in [16]. Because of the higher mobility of the NMOS transistors compared to that of the PMOS transistors, two PMOS pass transistors used in PP-SRAM cell are assigned larger widths. Thus, the area of the PP-SRAM cell is increased by 16.4% compared
to that of the conventional SRAM cell. In the asymmetric SRAM cell, the addition of one extra transistor increases the area of the cell by 16.6% [6]. In the IWL-VC SRAM (NC-SRAM) cell, since only 3 (2) transistors are added per row, the increase in the area is negligible. For a row of 128 SRAM cells, the widths for NC1, NC2, and P3 were 4 um, 8um, and 6 um, respectively, leading to a normalized area overhead of about 3%. The NC-SRAM cell has the minimum increase in the area while the 9T-SRAM cell has the maximum area overhead [9].

### *C. Read and Write Performances*

Now, we discuss the read and write performances of the SRAM cells. The timing diagrams in the read and write modes for the IWL-VC SRAM and PP-SRAM cells are depicted in Fig. 6 where the /_ transition is considered as the timing reference (we have assumed an asynchronous SRAM.) There is a delay between the column address transition and the /_ transition which is not included in our access time calculation. This delay, which is the same for all SRAM cells, only increases
the total time, thereby decreasing the normalized increase in the access time (i.e., the ratio of the access time increase to the total access time.) Thus, the actual degradation percentage ought to be lower than the numbers reported here.

As the timing diagram for the IWL-VC write operation [Fig. 6(a)] shows, about 200 ps after the /_ transition (see Fig. 2) the BL and /BL signals become stable in the selected SRAM cell. At this time, the WL signal is activated to select the row and after 350 ps, the writing of the new data is finalized. This suggests that the cell has 200 ps for restoring Va [see Fig. 1(b)] to the actual ground. As shown in Fig. 6(a), the transition
of /_ induces a 0 to Vdd transition of the SL signal. When SL is higher than the threshold voltage of NC2, this transistor turns on [see Fig. 1(b)] taking Va to Vss well ahead of the WL activation. Consequently,
there is no access time increase due to the restoration of actual ground. Notice that, as shown in Fig. 6(d), the amplitude reduction in /BL is less than 10% of the maximum swing, thus, no degradation in

the sensing operation occurs due to the use of PMOS.
The read and write delay increases for each proposed cell compared to those of the conventional cell are reported in Table I. Compared to the conventional SRAM cell, the performances of the read and write operations in NC-SRAM, IWL-VC SRAM, and asymmetric SRAM cells are degraded. In the NC-SRAM, because of using two NMOS transistors, through which a virtual ground is presented to the SRAM cell, the write and read access times are deteriorated by 4.3% and 2.37%, respectively. In the IWL-VC SRAM, the read and write access times are degraded by 2.42% and 4.4%, respectively. Although we activate the SL signal sooner than in the case of NC-SRAM, the existence of the PMOS transistor (P3) which increases the resistance of the word line, degrades the access times. Without the added PMOS transistor, the read access time is degraded by 1.8% which is lower than what is observed in the IWL-VC SRAM cell. In addition, the ON resistance of NC2 increases the path resistance to the ground (Vss). The access time in the asymmetric SRAM cell is 4% larger than that of the conventional SRAM cell. This degradation is due to the added N5 transistor. In the case of PP-SRAM cell, the timing performances remain unchanged. This originates from the fact that the forward body biasing technique is used for the PP-SRAM cell read and write operations.

### *D. Stability*

The stability of the SRAM cells may be determined by measuring the static noise margin (SNM) value. Simulation results for the idle (retention) and read static noise margins of the proposed SRAM cells compared to the case of the conventional SRAM cell are reported in Table II. During the read mode, since the forward body biasing is used (the threshold voltage is decreased), the SNM is improved by 11%. In the idle mode, the higher threshold voltage of the PMOS transistor, makes it more difficult for the access transistors to corrupt the data, thus yielding a 15% higher SNM for this cell. In the IWL-VC SRAM cell, in the read mode, the presence of NC2 increases the path resistance to the ground Vss degrading the read SNM by 12%. Also, in the idle mode, due to the virtual ground which is at a higher voltage than the actual ground, the SNM is degraded by 10%. This is the price paid for lowering the static power consumption. Compared to the conventional SRAM, the stability of the asymmetric SRAM cells is slightly degraded [6], while the stability of 9T SRAM is improved by 100% [9].

Since for the nanoscale SRAM, the Vth variation can be a serious problem, the Vth of the transistors in the SRAM cell is varied by 0.25% to evaluate the effect of Vth on the SNMs. The effects of the Vth variations of transistors N1, N2, P1, P2, P3, and P4 in the PP-SRAM cell on the SNMs are reported in Fig. 7. As the results reveal, the SNM has

a higher sensitivity to the Vth variations of P3 and P4. Since the structure
of the SRAM cell does not change in the IWL-VC SRAM cell,
the effect of the Vth variation on the SNM is similar to the SRAM cell
presented in [17] and is not discussed. Note that since NC1, NC2, and
P3 are not directly involved in the operations of the SRAM cell, the
Vth variations do not directly influence the SNMs.

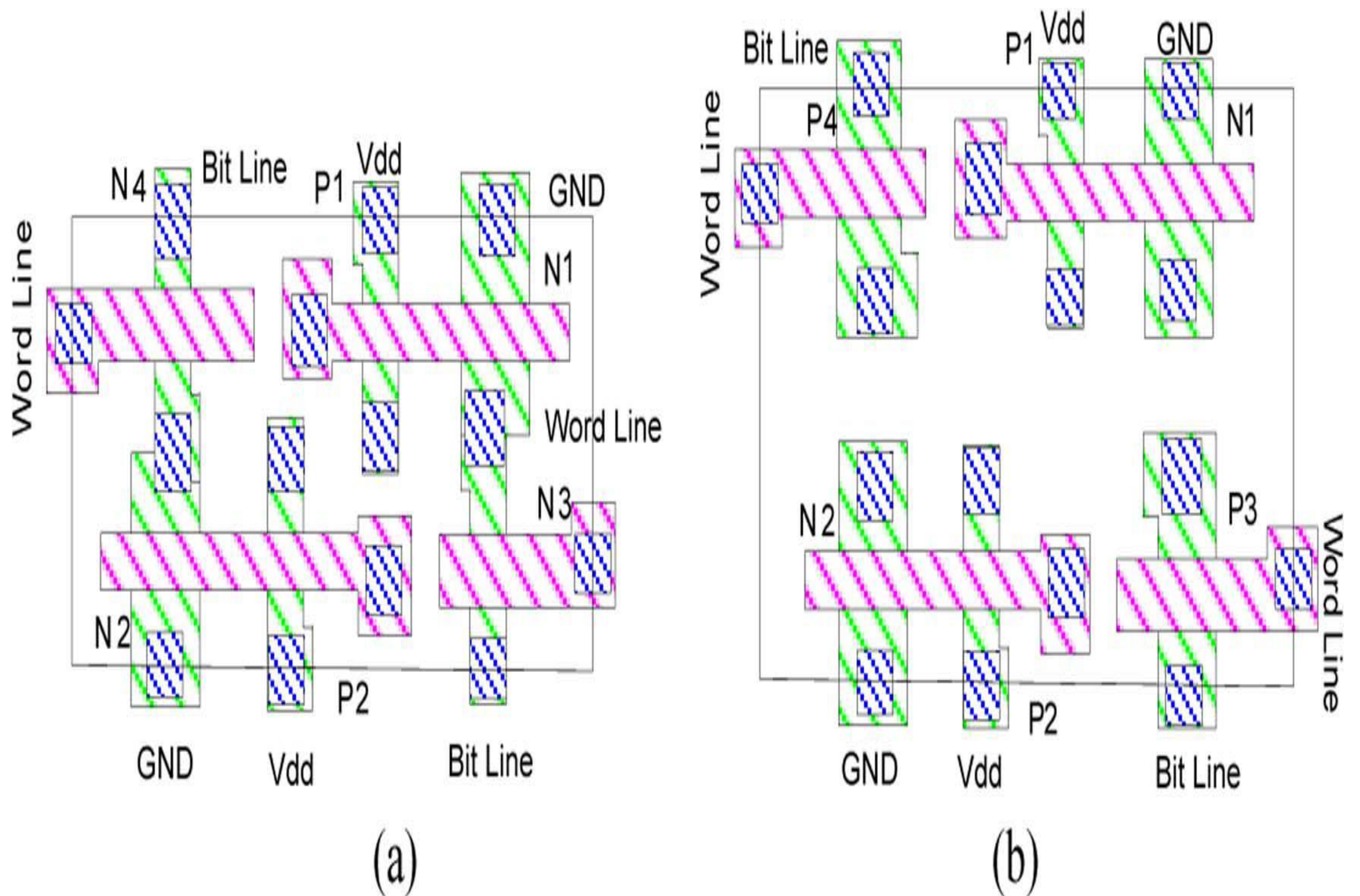
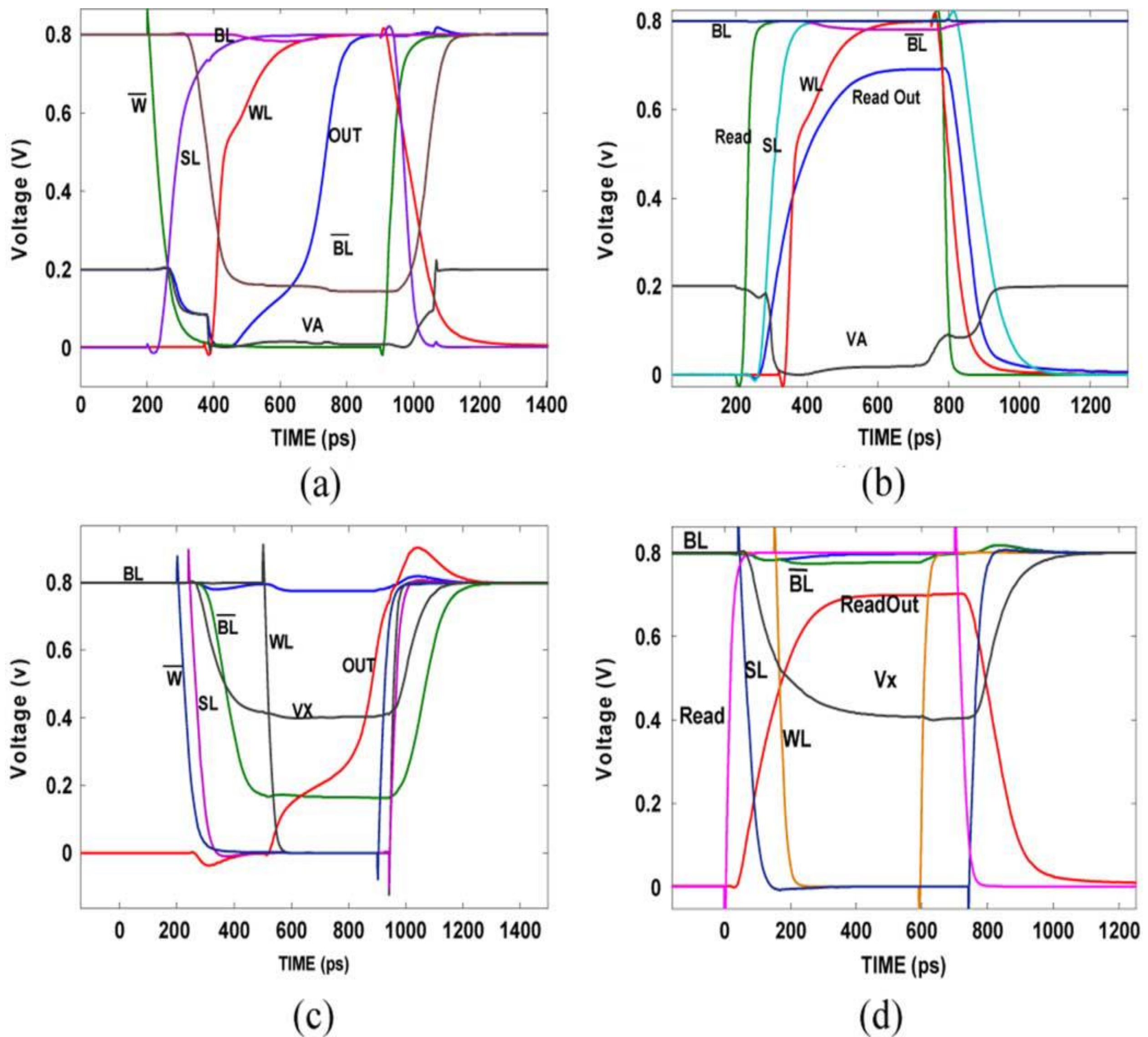
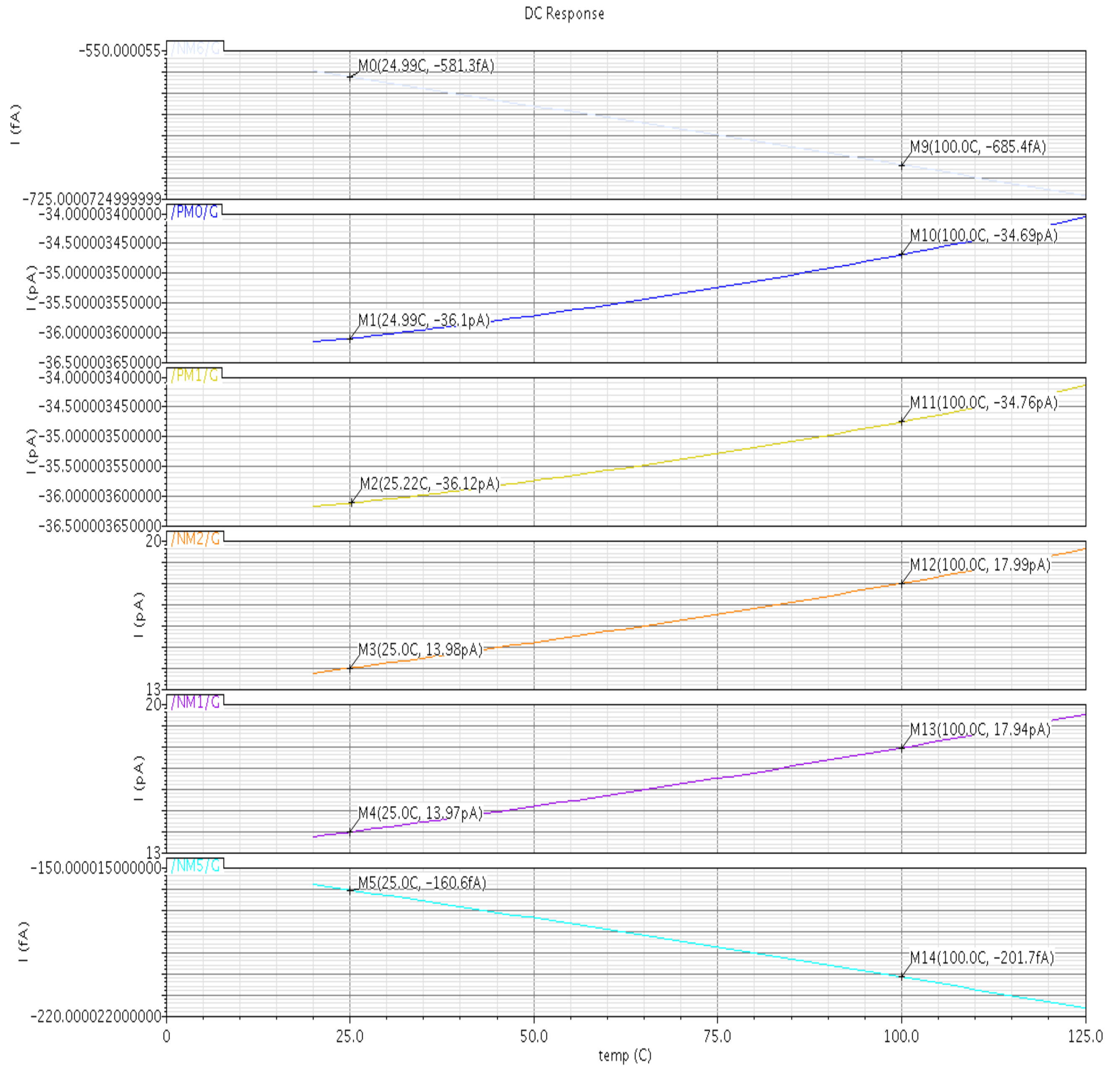



Fig. 5. Areas of (a) conventional SRAM and (b) PP-SRAM cells
in 45-nm technology.

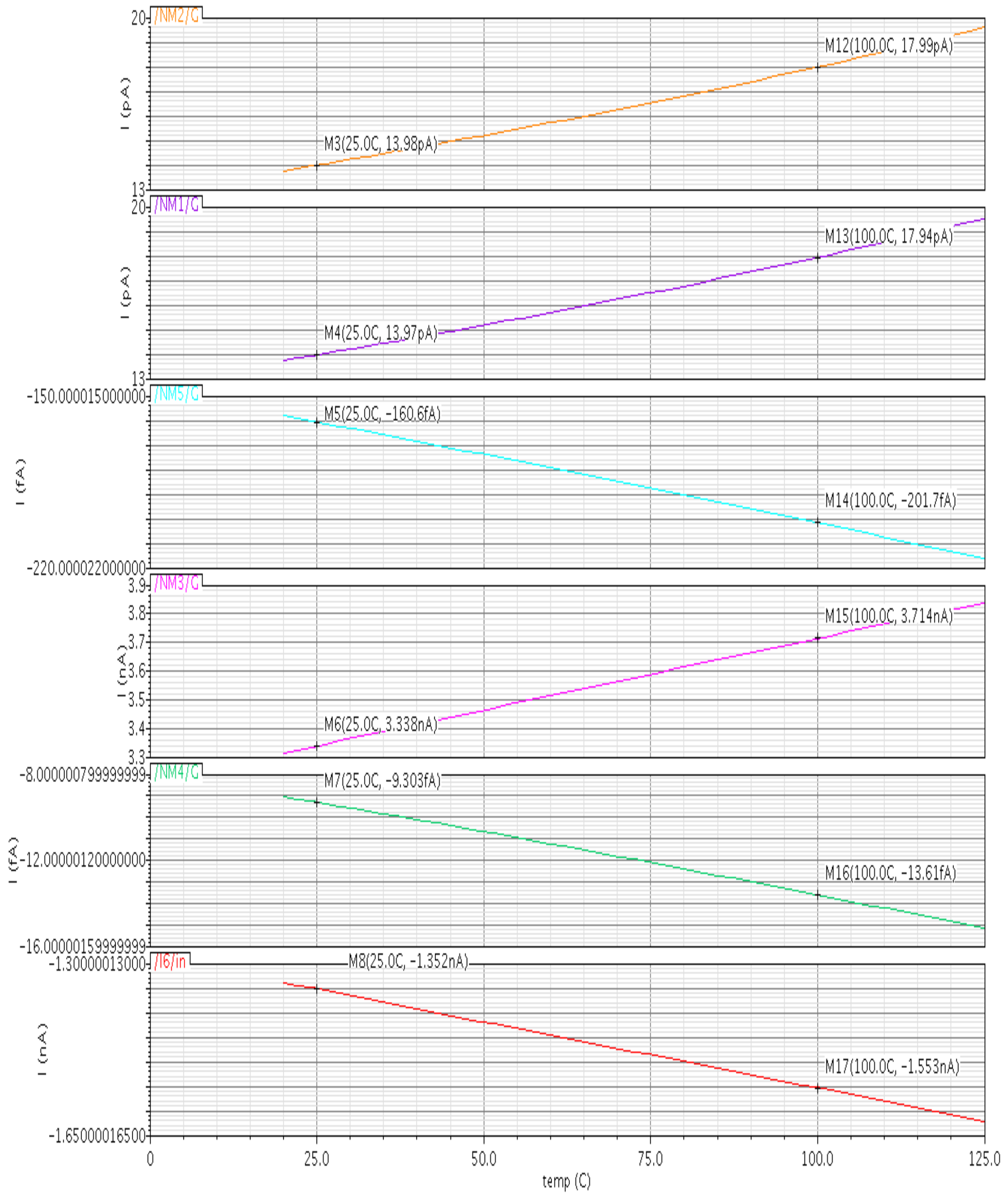
Fig. 6. Timing diagrams: (a) IWL-VC write, (b) IWL-VC SRAM read,
(c) PP-SRAM write, and (d) PP-SRAM read operations.

Gate Leakage Current Vs Temperature (IWL VC SRAM CELL )

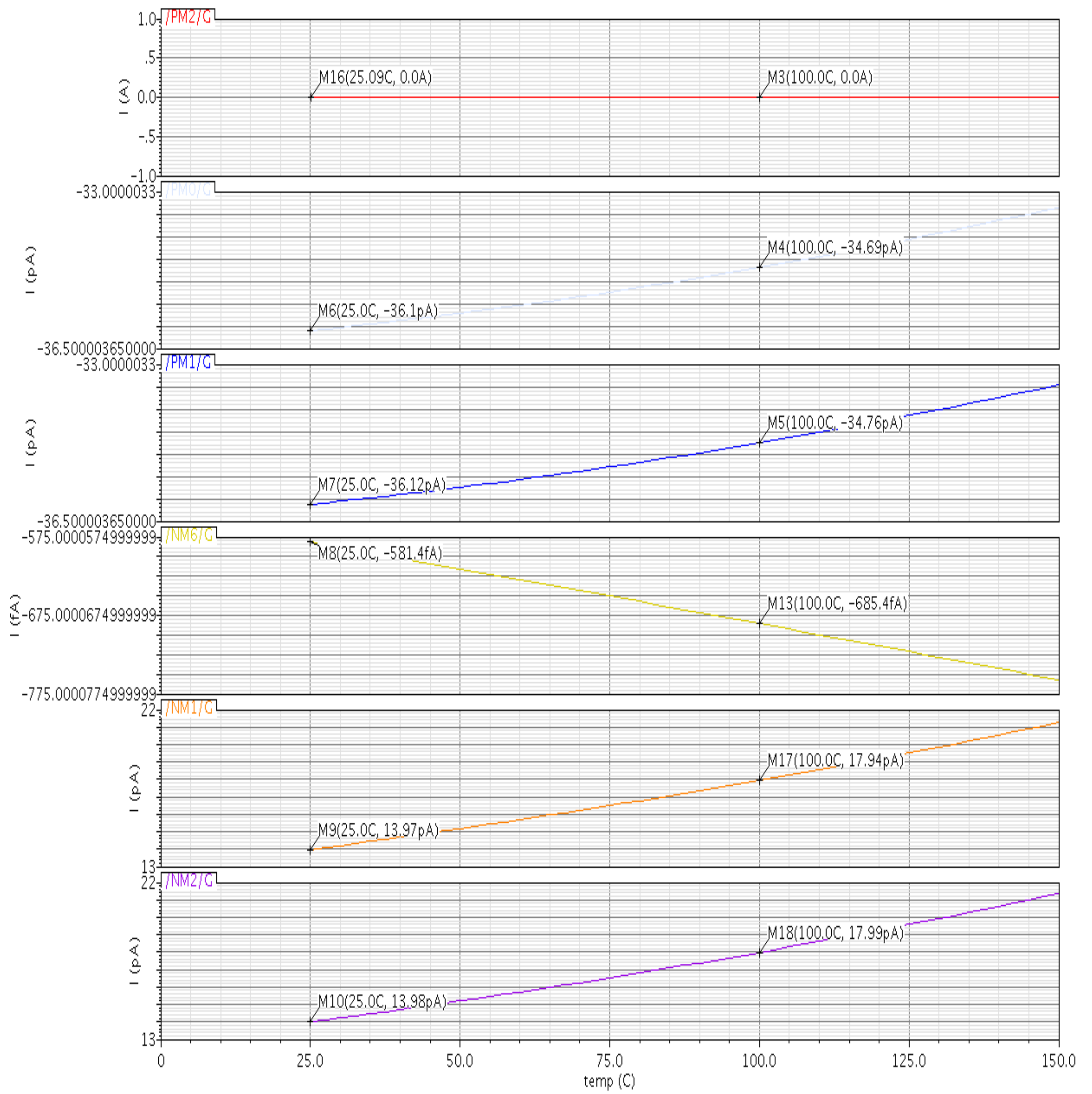


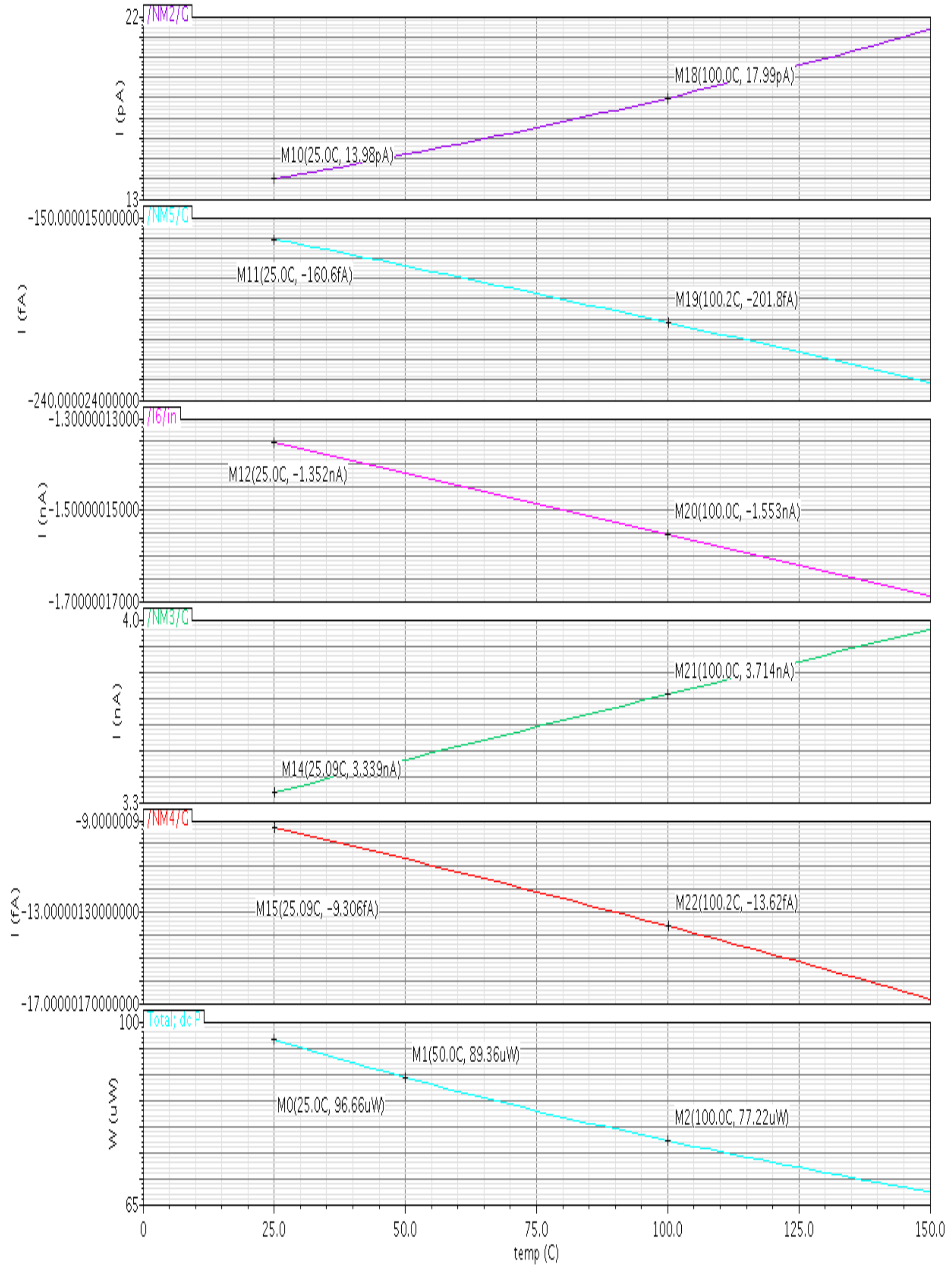


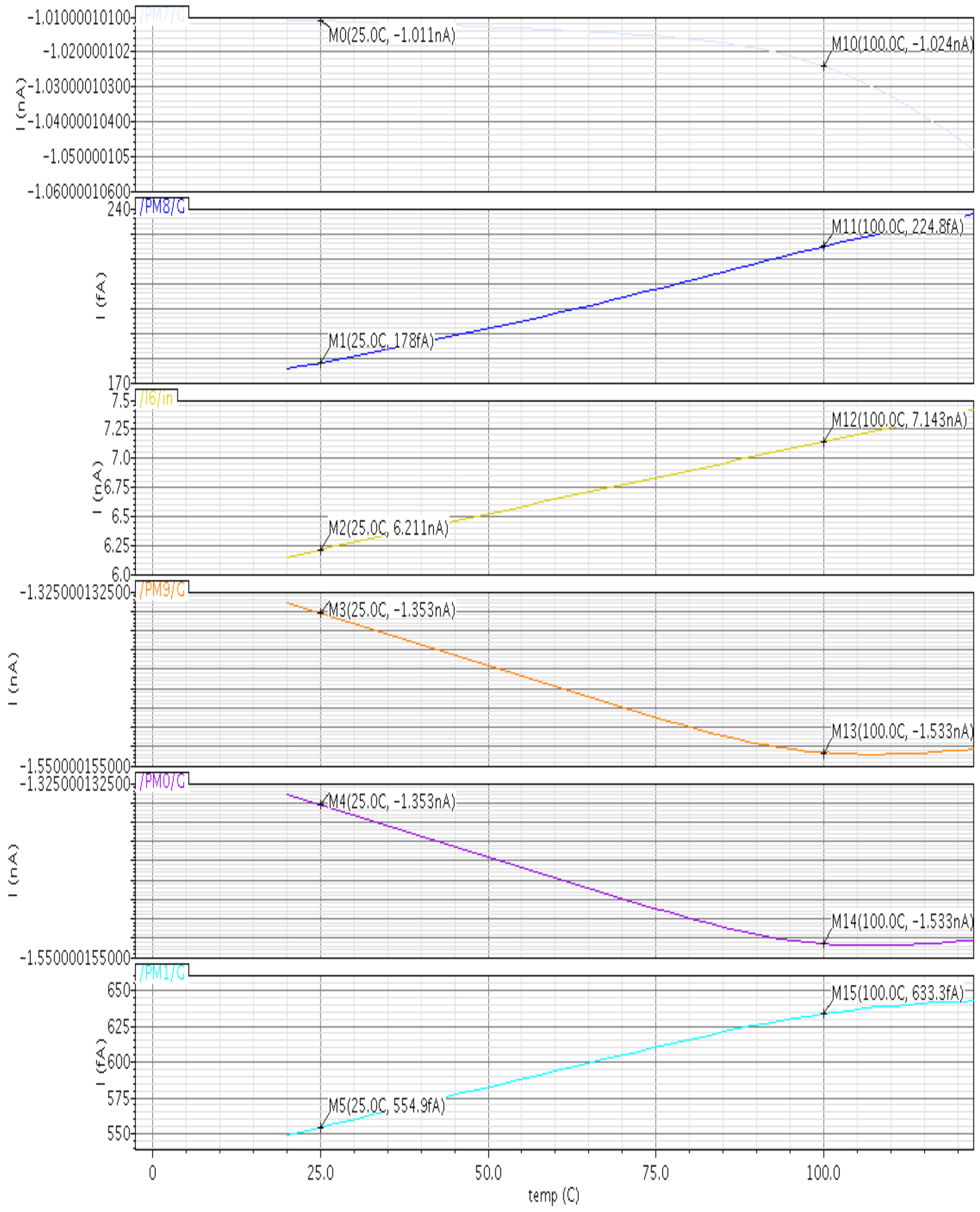

Gate Leakage Current Vs Tempareture

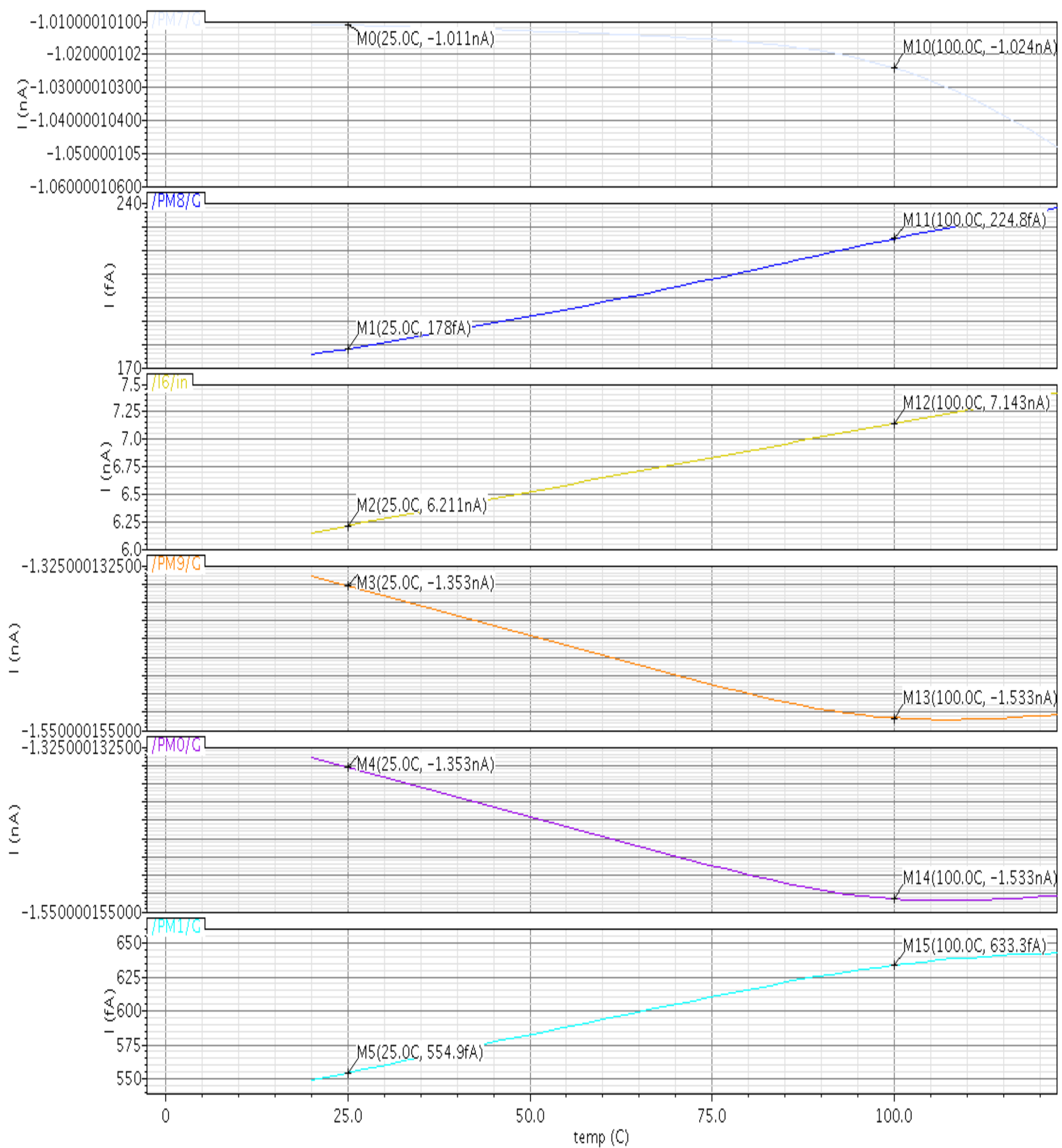



Gate Leakage Current Vs Tempareture


DC Response
/PM2/G
M16(25.09C, 0.0A)
M3(100.0C, 0.0A)
/PM0/G
M4(100.0C, -34.69pA)
M6(25.0C, -36.1pA)
/PM1/G
M5(100.0C, -34.76pA)
M7(25.0C, -36.12pA)
/NM6/G
M8(25.0C, -581.4fA)
M13(100.0C, -685.4fA)
/NM1/G
M17(100.0C, 17.94pA)
M9(25.0C, 13.97pA)
/NM2/G
M18(100.0C, 17.99pA)
M10(25.0C, 13.98pA)
temp (C)

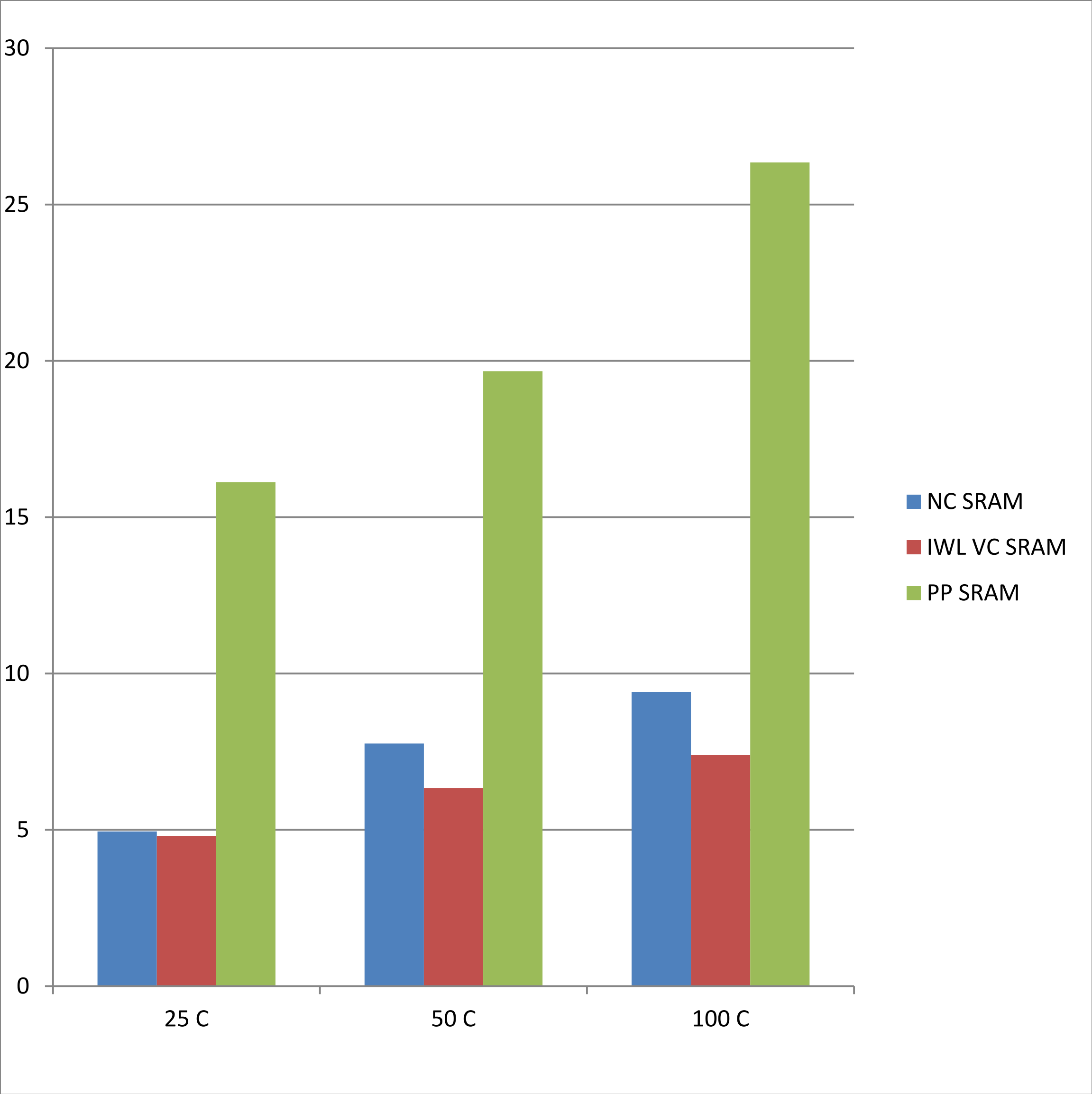

DC Response
/NM2/G
I (pA)
22
13
M10(25.0C, 13.98pA)
M18(100.0C, 17.99pA)
/NM5/G
I (fA)
-150.000015000000
-240.000024000000
M11(25.0C, -160.6fA)
M19(100.2C, -201.8fA)
/I6/in
I (nA)
-1.30000013000
-1.50000015000
-1.70000017000
M12(25.0C, -1.352nA)
M20(100.0C, -1.553nA)
/NM3/G
I (nA)
4.0
3.3
M21(100.0C, 3.714nA)
M14(25.09C, 3.339nA)
/NM4/G
I (fA)
-9.0000009
-13.000001300000000
-17.000001700000000
M15(25.09C, -9.306fA)
M22(100.2C, -13.62fA)
Total; dc P
W (uW)
100
65
M1(50.0C, 89.36uW)
M0(25.0C, 96.66uW)
M2(100.0C, 77.22uW)
0
25.0
50.0
75.0
100.0
125.0
150.0
temp (C)


DC Response
/PM7/G
M0(25.0C, -1.011nA)
M10(100.0C, -1.024nA)
-1.010000010100
-1.020000102
-1.030000010300
-1.040000010400
-1.050000105
-1.060000010600
I (nA)
/PM8/G
M11(100.0C, 224.8fA)
M1(25.0C, 178fA)
240
170
I (fA)
/I6/in
M12(100.0C, 7.143nA)
M2(25.0C, 6.211nA)
7.5
7.25
7.0
6.75
6.5
6.25
6.0
I (nA)
/PM9/G
M3(25.0C, -1.353nA)
M13(100.0C, -1.533nA)
-1.325000132500
-1.550000155000
I (nA)
/PM0/G
M4(25.0C, -1.353nA)
M14(100.0C, -1.533nA)
-1.325000132500
-1.550000155000
I (nA)
/PM1/G
M15(100.0C, 633.3fA)
M5(25.0C, 554.9fA)
650
625
600
575
550
I (fA)
0
25.0
50.0
75.0
100.0
temp (C)

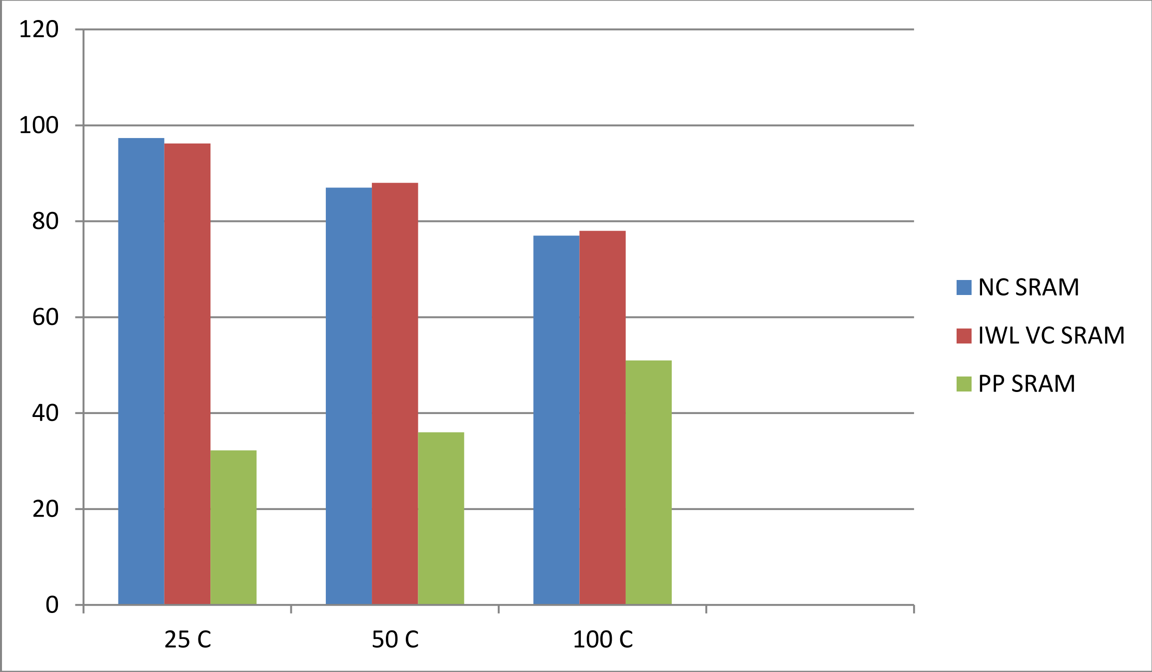


DC Response
/PM7/G
-1.010000010100
-1.020000102
-1.030000010300
-1.040000010400
-1.050000105
-1.060000010600
I (nA)
M0(25.0C, -1.011nA)
M10(100.0C, -1.024nA)
/PM8/G
240
170
I (fA)
M1(25.0C, 178fA)
M11(100.0C, 224.8fA)
/I6/in
7.5
7.25
7.0
6.75
6.5
6.25
6.0
I (nA)
M2(25.0C, 6.211nA)
M12(100.0C, 7.143nA)
/PM9/G
-1.325000132500
-1.550000155000
I (nA)
M3(25.0C, -1.353nA)
M13(100.0C, -1.533nA)
/PM0/G
-1.325000132500
-1.550000155000
I (nA)
M4(25.0C, -1.353nA)
M14(100.0C, -1.533nA)
/PM1/G
650
625
600
575
550
I (fA)
M5(25.0C, 554.9fA)
M15(100.0C, 633.3fA)
0
25.0
50.0
75.0
100.0
temp (C)

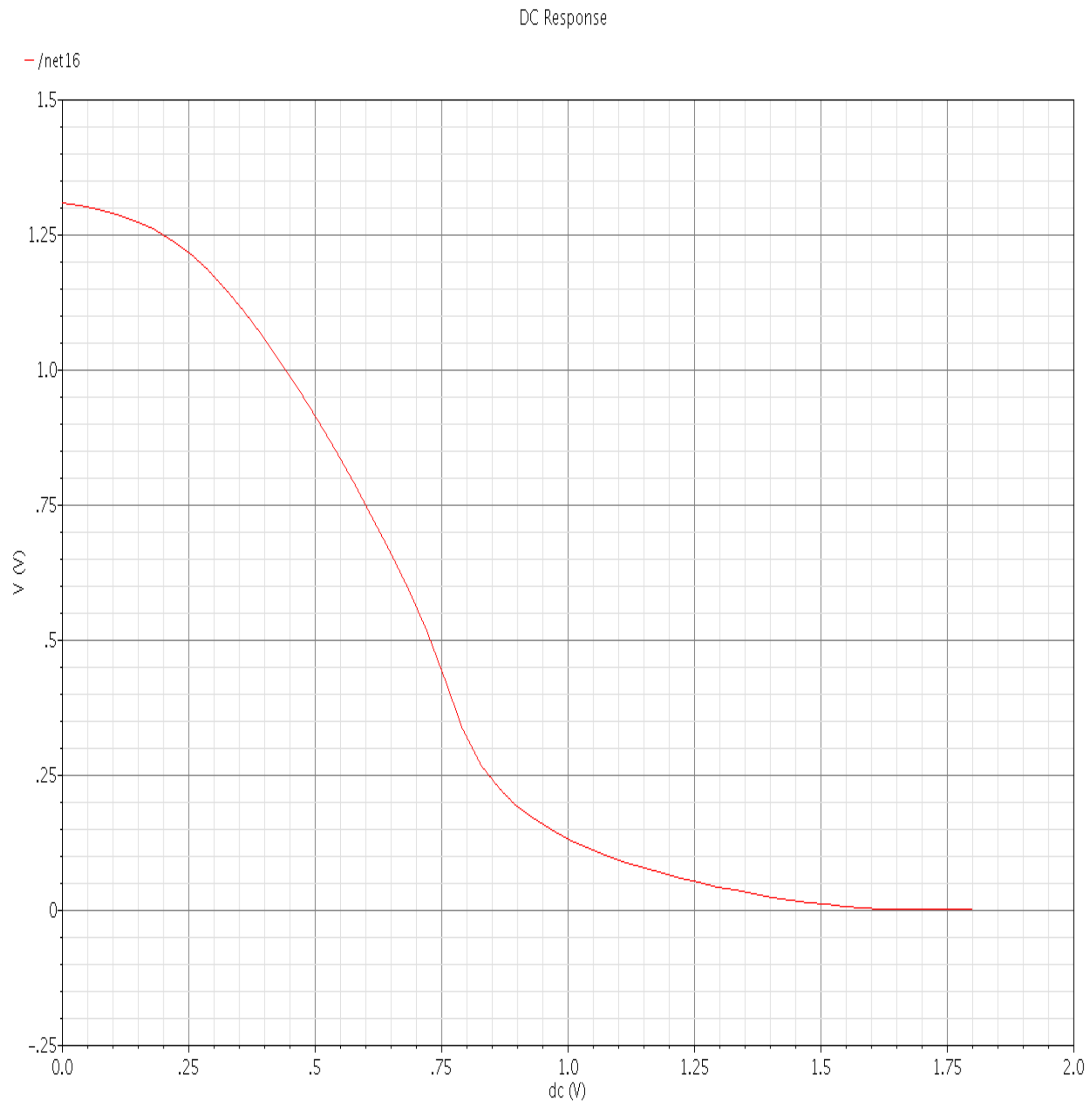
Comparison of Gate Currents (in nA) of SRAM Cells For various Tempareture



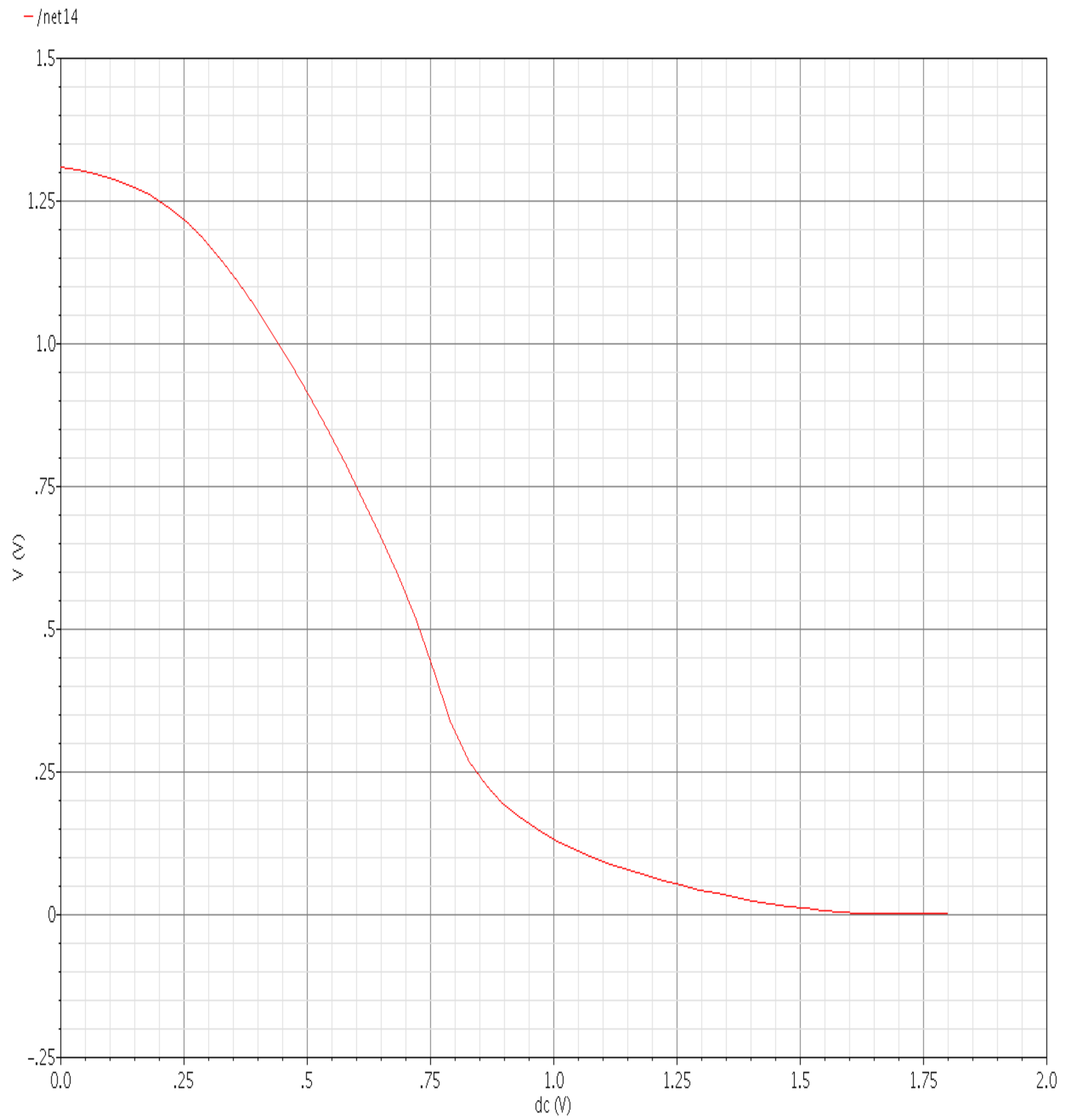
Comparison of Power (in uW) for different SRAM cells for Various tempareture



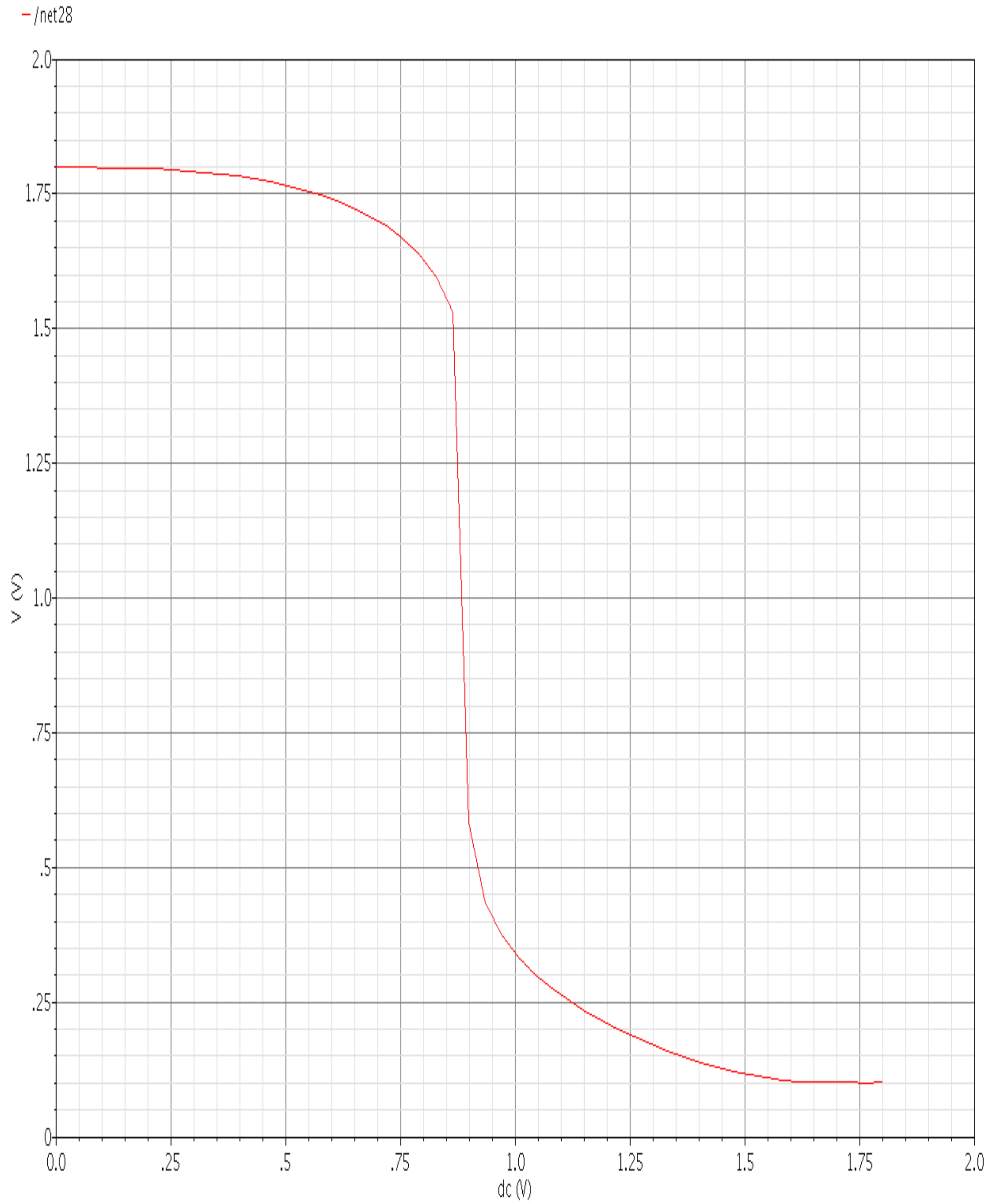
# VTC OF NC SRAM CELL



# VTC OF IWL-VC SRAM CELL



# VTC OF PP SRAM CELL



## TECHNIQUES FOR IMPROVEMENT

- PMOS size is 2 to 3 times greater than NMOS.
- Appropriate calculation of Tox (preferably dual oxide thickness devices).
- Dual threshold body bias technique can be used for NMOS in PP SRAM cell.
- For data to stay for a longer time we need size of pass transistor is greater than nmos of Inverter.

Fig. 4. (a) Gate currents and (b) power dissipations of SRAM cells at 25 C, 50 C, and 100 C.

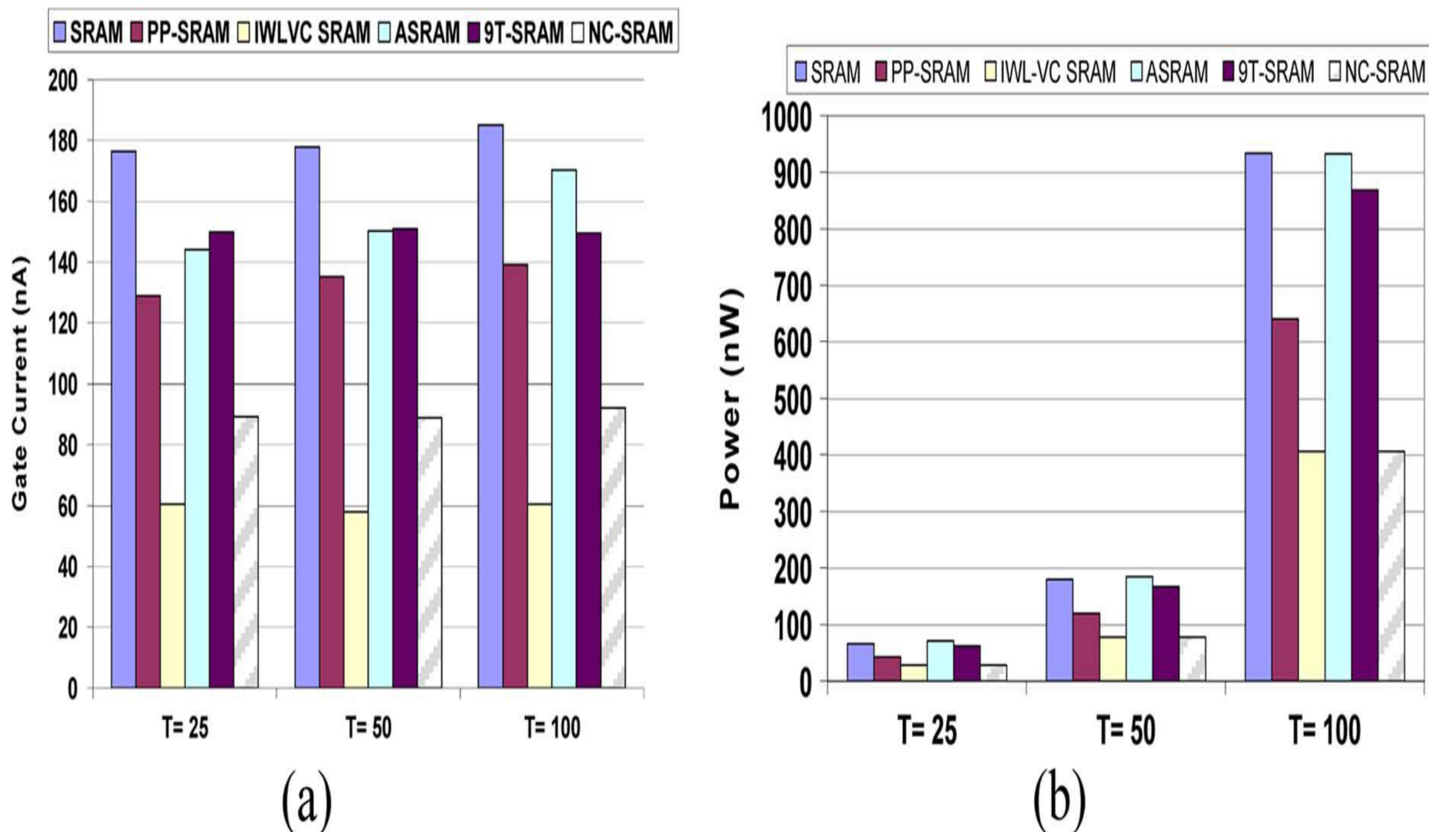


TABLE I
READ AND WRITE DELAY INCREASES FOR EACH PROPOSED CELL COMPARED TO THOSE OF THE CONVENTIONAL SRAM CELL

| OPERATION | A - SRAM | IWL-VC | PP-SRAM | NC- SRAM |
|---|---|---|---|---|
| WRITE TIME | 4% | 4.40% | 0 | 4.30% |
| READ TIME | 4% | 2.42% | 0 | 2.37% |

TABLE II
SNM IMPROVEMENT OF THE PROPOSED CELLS COMPARED TO THAT OF THE CONVENTIONAL SRAM CELL

| | IWL-VCSRAM | PP-SRAM | 9T-SRAM | ASRAM |
|---|---|---|---|---|
| RETENTION MODE | -10% | 15% | 0 | negligible |
| READ MODE | -12% | 11% | 100% | negligible |

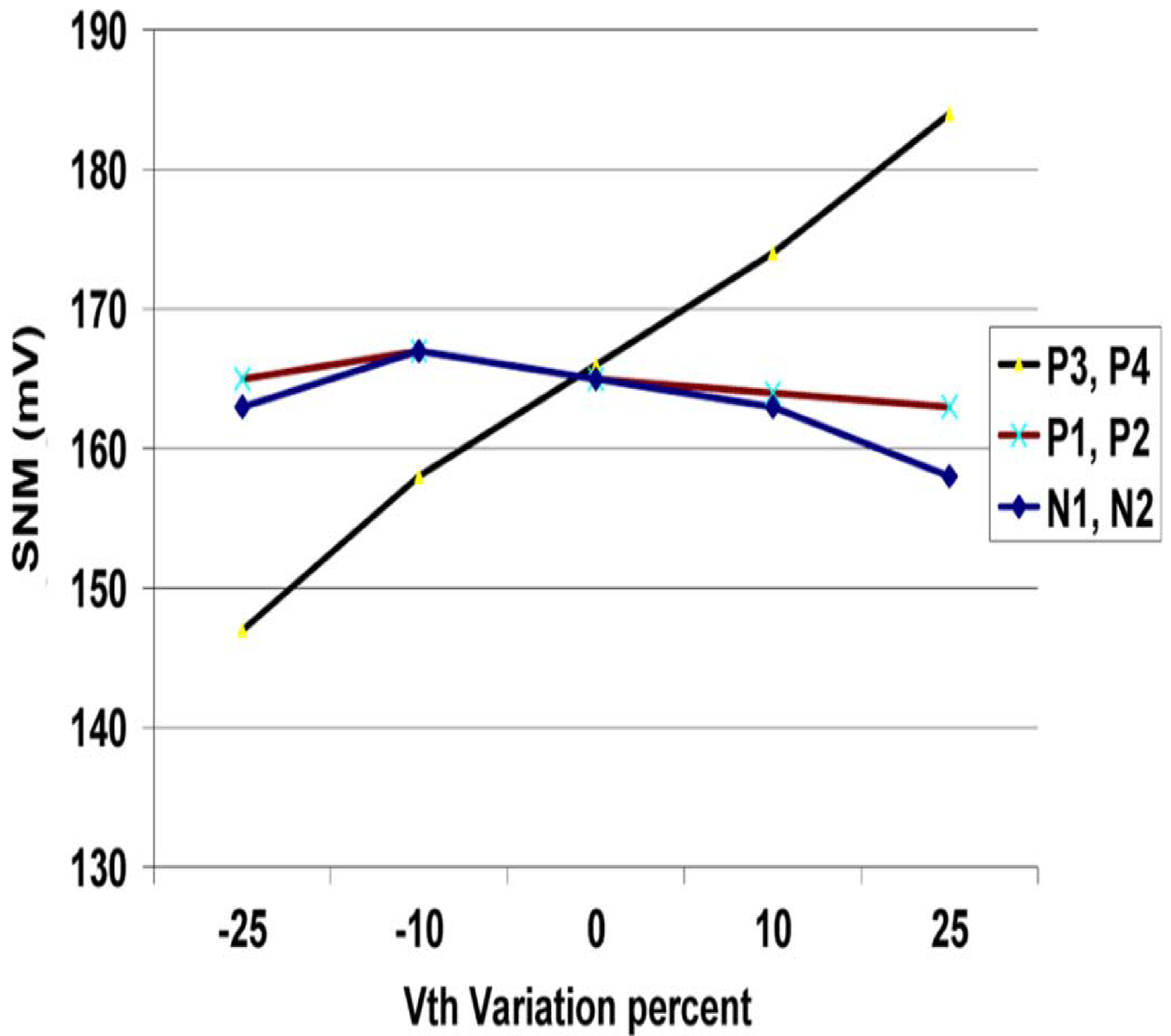



Fig. 7. Read SNM of the PP-SRAM cell as a function of Vth variation.

# V. CONCLUSION

In this paper, two new structures for the SRAM cell called IWL-VC SRAM and PP-SRAM were presented. The first cell structure made use of one PMOS per row of SRAM cells as well as two NMOS transistors for changing the ground voltage during the active and idle modes. This method lowered the gate current leakage of the cell by 58% and, hence, the static power dissipation of the memory with a minimum impact on the area. The read (write) access time of this SRAM was 4.4% (2.42%) slower than that of the conventional SRAM. The static noise margin, however, was also lowered by 10% compared to conventional SRAM cell. In the second cell structure, PMOS pass transistors with high $V_{th}$ and forward biasing method were used to reduce both the gate oxide direct tunneling and the subthreshold currents. In the PP-SRAM cell, the gate leakage current was reduced by 27% and the total static power by 37% while the read and write access times were not degraded. The SNM of PP-SRAM cell was also improved by 15%.

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