

TWO DIMENSIONAL ANALYTICAL THRESHOLD VOLTAGE MODELING OF DUAL MATERIAL GATE S-SOI MOSFET

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TWO DIMENSIONAL ANALYTICAL THRESHOLD VOLTAGE MODELING OF DUAL MATERIAL GATE S-SOI MOSFET

A dissertation submitted in partial fulfillment of the requirements for the degree of

Bachelor of Technology in “Electrical Engineering”

By

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Declaration

I certify that

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This is to certify that the thesis entitled” **TWO DIMENSIONAL ANALYTICAL THRESHOLD VOLTAGE MODELING OF DUAL MATERIAL GATE S-SOI MOSFET**” submitted by **Mr. Girija Sankar Pati (Roll No-110EE0217)** for the award of Bachelor of Technology in **Electrical Engineering** during session 2013-14 at National Institute of Technology, Rourkela is a bona fide research work carried out by him in the department of Electrical Engineering, under my supervision and guidance..

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In my opinion this thesis fulfills a part of requirements for the award of degree of Bachelor of Technology in Electrical Engineering.

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Girija Sankar Pati

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ABSTRACT

MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is the one of the most important and widely used semiconductor devices used in industry for various proposes. Two most important advantages of MOSFETs are their extremely low power dissipation and small area required for fabrication, i.e high packing density .With the advance of technology the feature sizes of MOSFETs are reduced continuously to increase the packing density of very large scale integration (VLSI) circuits. With continuous shrinkage of device geometrics on threshold voltage causes strong deviations from long channel behavior. The effect of such decrease in channel length is called SCE (Short channel Effect). A two dimensional Poisson equation needs to be solved in order to understand the effect of SCE.SCE (Short Channel Effect) is the effect of reduction in the channel length of MOSFET which results in significant differences from ideal characteristic like channel length modulation, carrier velocity saturation, two dimensional charge sharing, drain induced barrier lowering (DIBL), drain source series resistance and punch through. In order to minimize the effect of short channel effect various different modeling has been introduced. Among them DG MOSFET (Double Gate MOSFET), SOI MOSFET (Silicon-On Insulator MOSFET) are particularly important.

Silicon-on-insulator (SOI) has been widely used in CMOS technology because of its higher speed, higher packing density, and reduced second order effect for submicron VLSI application. Fully depleted (FD) SOI devices are preferred to bulk silicon CMOS devices. Various new structure with different gate and channel engineering are proposed to reduce SCEs .Among them Strain engineering and high-k gate dielectric with metal technology are preferred form enhancement of carrier mobility and reduction of gate leakage current.

In this thesis, a two dimensional threshold voltage model is developed for a Dual Material Gate Fully Depleted Strained Silicon on Insulator (DMG-FD-S-SOI) MOSFET considering the interface trap charges. The interface trap charges during the pre and post fabrication process are a common phenomenon, and these charges can't be neglected in nano scale devices. For finding out the surface potential, parabolic approximation is utilized to solve 2D Poisson's equation in the channel region. Further, the virtual cathode potential method is used to formulate the threshold voltage. The virtual cathode potential is considered as the minimum channel potential in the horizontal direction which can be found from the 2-D potential distribution in the channel region. The developed threshold voltage model incorporates both positive as well as negative interface charges. The effect of various parameters like Ge mole fraction, drain bias, gate length ratio variation, and interface charge variation have been considered on surface potential, electric field, and threshold voltage. Finally, validity of the presented model is verified with SentaurusTM, a 2-D device simulator from Synopsis Inc.

Key words: Dual Material Gate DMG), interface trap charges, virtual cathode potential

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Chapter 1

Introduction

The metal-Oxide-Semiconductor Field effect Transistor (MOSFET) has been the key factor in semiconductor industry because of its low power dissipation, greater package density, and superior performance. CMOS technology evolution in the fast few decades has followed the device scaling to achieve density, speed and power improvement by an exponential growth in the number of transistors per integrated circuit as predicted by Moore's law [1]. The future trend as predicted by ITRS (International Technology Roadmap for Semiconductors), dimensional and electrostatic limitations faced by conventional fabrication technology will require dimensional scaling of CMOS devices [2]. With continuous shrinkage of device geometrics on threshold voltage causes strong deviations from long channel MOSFET behavior. The effect of such decrease in channel length is called SCE (Short channel Effect). A two dimensional Poisson equation needs to be solved in order to understand the effect of SCEs .SCE (Short Channel Effect) is the effect of reduction in the channel length of MOSFET which results in significant differences from ideal characteristic like channel length modulation, carrier velocity saturation, two dimensional charge sharing, drain induced barrier lowering (DIBL), drain source series resistance and punch through. In order to minimize the effect of short channel effect various different modeling has been introduced. To address this problem various new technology such as Silicon-On-Insulator(SOI), strained Silicon(s-Si), inclusion of high-k dielectric material, Double Metal Gate(DMG), Gate all around(GAA) have been proposed [3]–[6].

1.1 Moore's Law

According to **Moore's law** is the observation that, over the history of computing hardware, the number of transistors on integrated circuits doubles approximately every two years. The law is named after Gordon E. Moore, who described the trend in his 1965 paper. According to Moore's law since 1965, the price of one bit of semiconductor memory has been dropped ever since. Miniaturizations has been responsible to the improvement in the speed and power consumptions in ICs. Moore's law is a statistical description of the rapid and persistent trend of miniaturization. Each time the minimum line width is reduced, we say that a new technology generation or is introduced. Example of technology is generations is shown in Table 1.1[1].

Table 1.1 Improvements in Technology Node over the years

| Year | 2004 | 2006 | 2008 | 2010 | 2011 | 2013 | 2016 | 2022 |
|----------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Channel Length | 90 nm | 65 nm | 45 nm | 32 nm | 22 nm | 16 nm | 14 nm | 10 nm |

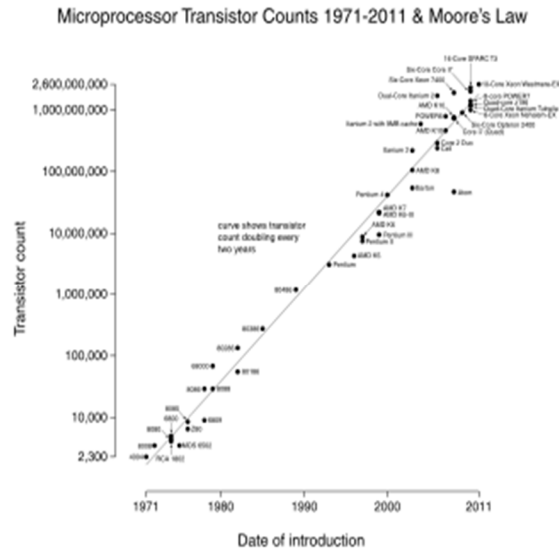
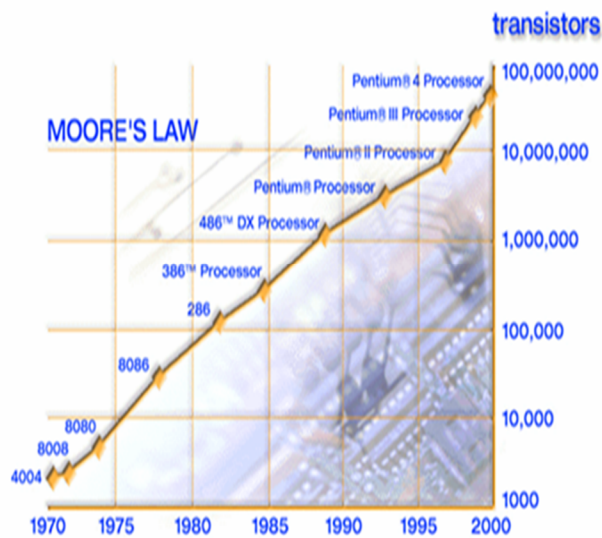


Fig 1.1 Moore's Law [1]

1.2 MOSFET Scaling

The lateral geometric dimensions of devices has been termed as “scaling” of integrated devices(IC). The minimum feature size is smaller size of object (gate length or inter connect line width) on IC. Over the past decades MOSFET has been continually scaled down in size and as a consequence the number of transistors have increased over time. With this scaling the cost of fabrication of IC chips are reduced because the fabrication cost for a semiconductor wafer are relatively fixed, the cost per IC chips is reduced as the no of IC chips from same wafer increases. The switching frequency of smaller transistor are faster. With scaling of channel length, channel width, oxide thickness by equal factors transistors channel resistance doesn't change while gate capacitance is changed which changes RC delay of transistor by a similar factor thus improving the performance of MOSFET [7].

1.3 Effect of Scaling

It is desirable to scale the vertical and lateral dimensions when decreasing the device sizes. The scaling affects both reliability and performance specification of the purpose.

- Constant field scaling strategy
 - Vertical dimension decrease with same lateral dimensions
 - To maintain fixed electric field, operating voltage decrease.
- Constant voltage scaling strategy
 - Attractive due to electrical compatibility with existing circuit.
 - Vertical dimensions decreases quadratically relative to the lateral dimensions.

The following table [2] indicates the effect of MOSFET scaling on various parameter

| Parameter | Symbol | Constant Field Scaling | Constant Voltage Scaling |
|-------------------|----------|------------------------|--------------------------|
| Gate Length | L | 1/K | 1/K |
| Gate width | W | 1/K | 1/K |
| Electric Field | E | 1 | K |
| Oxide Thickness | t_{ox} | 1/K | 1/K |
| Substrate Doping | N_a | K^2 | K^2 |
| Gate Capacitance | C_g | 1/K | 1/K |
| Oxide Capacitance | C_{ox} | K | K |
| Voltage | V | 1/K | 1 |
| Current | I | 1/K | K |
| Power | P | $1/K^2$ | K |

Where K is the scaling factor

Further technology scaling requires major changes in many areas, including:

- Improvement in lithography techniques.
- Improvement in transistor design to attain higher performance with smaller dimensions.
- Change of focus from current bulk CMOS devices to innovative materials and structures, including silicon-on-insulator, strained Si and high k dielectric materials.
- Minimum wiring for on- chip interconnection of the circuits.
- More efficient of design automation tools.
- High density memory cells.
- Low capital costs. Metal gate and high-k gate dielectrics were introduced into fabrication in 2007 to maintain technology scaling trends [8]–[10].

1.4 Challenge to miniaturization of MOSFETs

The International Technology Roadmap for Semiconductor (ITRS), issued by the semiconductor Industry Association estimates that by the year 2010 the major feature (gate length) of 70 nm, isolated transistor with 40 nm have been used in industry and transistor with gate length of 25 nm have been made using strained Silicon(S-Si).

The major problems faced by a device engineer towards miniaturization of MOSFETs are explained below.

1.4.1 High electric Field:

Due to bias voltage being applied over a very short distances, can cause “avalanche breakdown” by striking large numbers of electrons out of semiconductor at high energy. This causes current surges and substantial damage to device.

1.4.2 Heat dissipation:

Heat dissipation of transistors is limited due to thermodynamic efficiency, limits their density in circuits and causes malfunction.

1.4.3 Shrinkage of depletion region:

Depletions regions are too thin to avoid quantum mechanical tunneling of electrons from source to drain when the device is turned off. The functioning of nano-electronics depends on such tunneling of electrons through barrier.

1.5 Objective:

1. To study the short channel effect on single gate and double gate MOSFET by varying channel length, oxide thickness, effect of strain and trapped charges on surface potential, electric field, and threshold voltage.
2. To model and analyze Double material single gate MOSFET considering effect of trapped charges, strained silicon(s-Si) on surface potential, electric field, threshold voltage modelling. The mathematical model is compared to the device structure modelled in SentaurusTM, a 2-D device simulator from Synopsis Inc.
3. To study the effect of high k dielectric material on Double material single Gate MOSFET.

1.6 Thesis Organization

The dissertation is divided into five chapters and its outline is described as follows.

Chapter 1 : Introduction

Fundamental Concept on Scaling, Moore's Law, effect of Scaling, problems due to miniaturization, Objective of the project, outline of the thesis.

Chapter 2: Short Channel Effects in Nano scale MOSFET

This chapter analyses the origin and effect of short channel effects in nano scale MOSFETs, methods to counter the SCEs are also discussed in detail. Comparison between Single Gate MOSFET and Double Gate MOSFET is also considered in this chapter

Chapter 3: modelling of Dual Material Gate Fully Depleted Strained Silicon on Insulator (DMG-FD-S-SOI) MOSFET

This chapter includes mathematical modeling of DMG-FD-S-SOI MOSFET and the effect of trapped charges, dual material, strained silicon(s-Si) by solving 2-D Poisson's equation analytically and considering various Boundary conditions. Further, the virtual cathode potential method is used to formulate the threshold voltage. The virtual cathode potential is considered as the minimum channel potential in the horizontal direction which can be found from the 2-D potential distribution in the channel region. The developed threshold voltage model incorporates both positive as well as negative interface charges. The effect of various parameters like Ge mole fraction, drain bias, gate length ratio variation, and interface charge variation have been considered on surface potential, electric field, and threshold voltage

Chapter 4: Result Analysis and Scope for future Work

Chapter 2

Short Channel Effects in Nano scale MOSFET

2.1 Introduction

With the advance of technology the feature sizes of MOSFETs are reduced constantly to enhance the packing density of very large scale integration (VLSI) circuits. With continuous reduction of device geometrics on threshold voltage causes strong deviations from long channel MOSFET performance. The effect of such decrease in channel length is called SCE (Short channel Effect). A two dimensional Poisson equation needs to be solved in order to understand the effect of SCEs .SCE (Short Channel Effect) is the effect of reduction in the channel length of MOSFET which results in significant differences from ideal characteristic like channel length modulation, carrier velocity saturation, two dimensional charge sharing, drain induced barrier lowering (DIBL), drain source series resistance and punch through. [11], [12].

The Short- channel effect can be attributed to two physical phenomena

- The restriction enforced on electron drift characteristics in the channel.
- Alteration in threshold voltage due to channel length modulation.

Five different short-channel effects are

- Drain Induced Barrier lowering and Punch through
- Velocity Saturation
- Impact ionization
- Surface Scattering
- Hot Electron

2.1.1 Drain Induced Barrier Lowering and Punch Through (DIBL)

This effect is primarily shown by devices biased in sub threshold mode of operation and in conjugation with two dimensional charge sharing. As the threshold voltage increases the barrier height of source channel is reduced. Reduction in the source channel potential barrier would exponentially increase the amount of electron injection from the source to channel region. This results in enhanced sub threshold current from source to channel barrier caused by applied voltage V_{DS} .

2.1.2 Velocity Saturation

The electric field increases with decrease in channel length. Electron drift current is proportional to the magnitude of its drift velocity v_d

$$v_d = \mu_n |\epsilon_x|$$

Where μ_n =electron field mobility, ϵ_x = Electric field

Electron velocity is proportional to electric field till the field reaches a value known as critical electric field ϵ_c . For values of electric field beyond this value the speed is saturated to its maximum value predicted by thermodynamics given by

$$v_{dmax} = \sqrt{\frac{3kT}{m_n}}$$

Where k=Boltzmann's constant, T = temperature in Kelvins scale, m_n = effective mass of electron

Critical electric field ϵ_c is given by

$$\epsilon_c = \frac{v_{dmax}}{\mu_n}$$

$$v_d = v_{dmax} \frac{\epsilon_x / \epsilon_c}{1 + \epsilon_x / \epsilon_c}$$

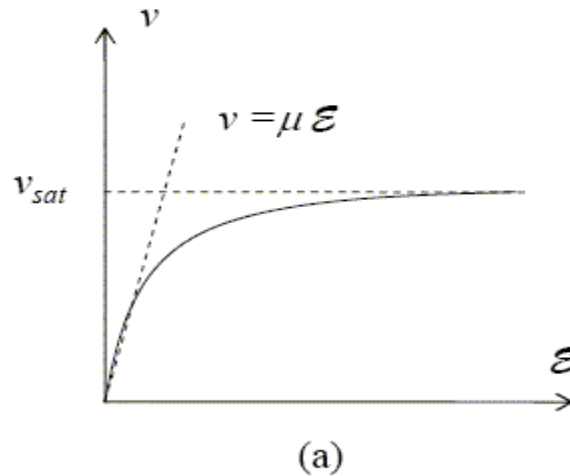


Fig 2.1 Variation of Drift Velocity and Electric Field

2.1.3 Impact Ionization

In NMOS, another detrimental short channel effect, occurs due to high electron velocity in presence of high longitudinal field which generates electron-hole pairs by impact ionization. Most of the electrons are drifted towards the drain, while the hole enters the substrate to form a part of parasitic substrate current. As source acts as emitter and drain as collector of an npn

transistor. If these holes are collected by the source, these creates a reduction of voltage in the substrate region of the magnitude 0.6-0.7 V which injects electrons from source to substrate. This situation becomes worse when some electron produced due to high electric fields escape the drain region to travel into substrate region thus affecting MOSFET performance.

2.1.4 Surface Scattering

As the channel length becomes compact due to crosswise extension of the depletion layer into the channel region the longitudinal electric field E_y increase, and the surface electron mobility converts into field-dependent. This is called surface scattering effect.

2.1.5 Hot Electron

Due to high electric field high energy electrons enter the oxide layer, they became trapped giving rise to oxide charging that can accumulate with time and degrade the device performance by increasing V_t (threshold voltage).

2.2 Solution to short Channel effects

Various techniques have been proposed to overcome short channel effects. These are

1. High ϵ -k dielectric material
2. Silicon On Insulator(SOI)
3. Strained Silicon(s-Si) structure

2.2.1 High K material

The dielectric constant, k , is a parameter which defines the charge storing ability of material. Capacitor is a device which consists of a layer of dielectric material inserted between two metal plates. All other parameters remaining same, k (dielectric strength) would control capacitance of the capacitance or in other words, it is the measure of mutual capacitive coupling between two conducting metal plates – with high- k dielectric such coupling would be strong, and with low- k dielectric being obviously weak. In Silicon device manufacturing and technology, the reference value of k is taken that of silicon dioxide, SiO_2 , which is 3.9. Dielectric material having $k > 3.9$ are referred to as high- k dielectric while dielectric featuring $k < 3.9$ are defined as low- k dielectrics. In nano electronics silicon technology both high- k and low- k dielectrics are needed to implement high speed, high efficiency, and high-density integrated circuit. High- k dielectrics are needed in MOS gate stacks to sustain sufficiently high capacitance of the metal (gate) – high dielectric-Silicon structure in MOS/CMOS transistors. Due to the continuous scaling of the channel length (L), and compact gate area A , it is necessary to maintain sufficiently minimum capacitance of the MOS gate stack was met by continuing reduction of the thickness of SiO_2 gate oxide.

2.2.2 Silicon On Insulator

With physical dimensional separation between discrete devices in ultra-high density CMOS integrated circuits measured in nanometers, proper electrical separation between them is an issue. The SOI (Silicon-On-Insulator) substrate wafers, as against conventional bulk wafers, not only solve the problem of electrical isolation amongst adjacent devices but also allow state-of-the-art device outlines resulting insignificantly better than in the case of bulk substrates performance of CMOS circuitry. Hence, SOI substrates rapidly become a significant element of the cutting-edge silicon IC technology.

2.2.3 Strained Silicon(s-Si) structure

Mobility loss resulted due to higher channel doping and scaled gate dielectrics should be compensated to meet the performance targets of MOSFET device. Mobility-enhancement technology has been more straight forward and cost effective way to improve device performance and scalability. Ge and GaAs provides high mobility [13], [14].

2.3 Advantages of DG MOSFETs

(a) Better scalability- The double-gate MOSFET has superior scalability (i.e., superior control of short-channel effects) than the single-gate SOI MOSFETs due to the electrical isolation action of the bottom gate for electric fields devising from charges in the source and drain. For gate channel-length scaled below 25 nm, the superior scalability of the device could make the DG MOSFET suitable [11], [15].

(b) Better switching characteristics- DG MOSFET provide higher ON-to-OFF current ratio than that of the bulk MOSFET due to sub threshold swing of $\sim 60\text{mV/Decade}$ thereby providing better switching characteristics.

(c) Higher drive current- Since the current can drift along both the top and bottom edges of the silicon wafer body (rather than just along the single top edge as in the ultra-thin body SOI single gate MOSFET), the ON-state drive current can almost be double of that of the single-gate device.

(d) Higher transconductance and linearity- Higher transconductance and greater linearity of DG MOSFETs can be achieved by increasing the doping level in the channel region of device. Doped DG MOSFETs are important for many analog and RF applications[16]–[18].

2.4 Comparison of performance Analysis of Single Gate MOSFET and Double Gate MOSFET

This chapter presents an analytical model of surface potential for short-channel Ultra-Thin Body (UTB) symmetrical Double-Gate (DG) MOSFETs including the effects of the interface charges. The parabolic potential approximation method is utilized while solving the two-dimensional (2D) Poisson's equations along with the assumption that the interface charge distribution is uniform along the channel [19]–[21]. The simulation results from Sentaurus™ are utilized to verify the obtained model. Comparison has been done with Single Gate MOSFET having same dimension as Double Gate.

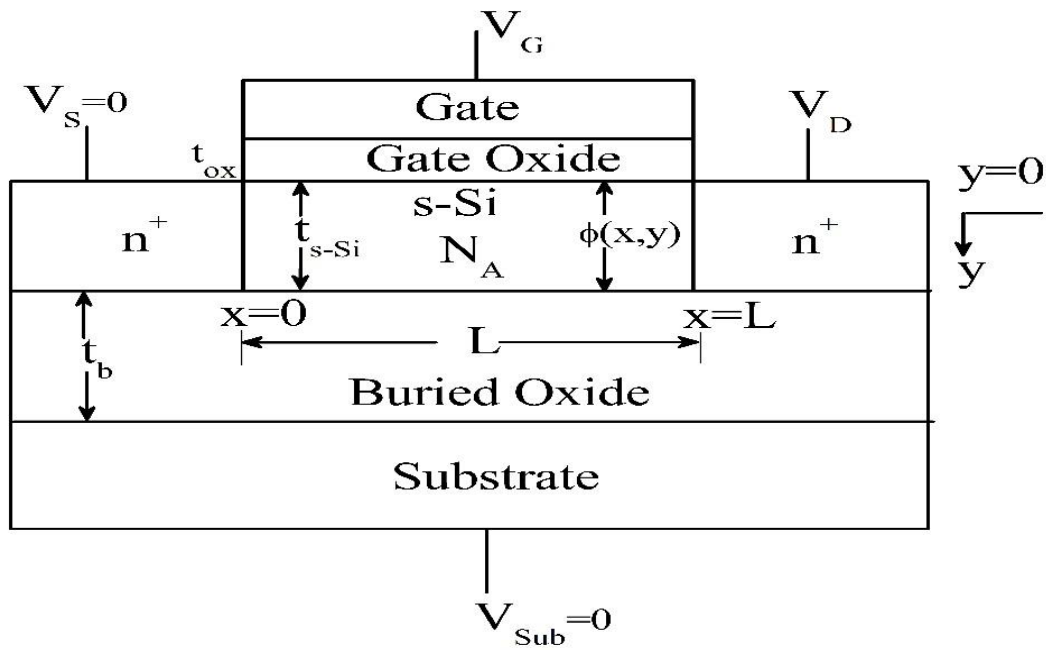


Fig 2.2 Cross-sectional view of the single-Gate FD-SOI MOSFET

2.4.1 Analytical Model Formation

Modeling of the Surface Potential (Single Gate)

Effect of Strain on band structure

Flat band voltage (front channel)

$$(V_{FB,f})_{si} = \phi_M - \phi_{si} \quad (2.1)$$

Where $\phi_{f-si} = V_T \ln\left(\frac{N_a}{n_i}\right)$, $\phi_{si} = \frac{\chi_{si}}{q} + \frac{E_{g,si}}{2q} + \phi_{f-si}$

Back channel flat band voltage (back channel)

$$(V_{FB,b})_{si} = \phi_{sub} - \phi_{si} \quad (2.2)$$

Where $\phi_{sub} = \frac{\chi_{si}}{q} + \frac{E_{g,si}}{2q} + \phi_{f-sub}$, $\phi_{f-sub} = V_T \ln\left(\frac{N_{sub}}{n_i}\right)$

Built in voltage across source-body and drain body junction

$$V_{bi,si} = \frac{E_{g,si}}{2q} + \phi_{f-si} \quad (2.3)$$

Model Formulation

2-D Poisson's equation

$$\frac{\partial^2 \phi_1(x, y)}{\partial x^2} + \frac{\partial^2 \phi_1(x, y)}{\partial y^2} = \frac{qN_A}{\epsilon_{si}} \quad \text{for} \quad 0 \leq x \leq L_1, 0 \leq y \leq t_{s-si} \quad (2.4)$$

$$\frac{\partial^2 \phi_2(x, y)}{\partial x^2} + \frac{\partial^2 \phi_2(x, y)}{\partial y^2} = \frac{qN_A}{\epsilon_{si}} \quad \text{for} \quad L_1 \leq x \leq L, 0 \leq y \leq t_{s-si} \quad (2.5)$$

The potential profile in the vertical direction can be approximated by a parabolic function

$$\phi_1(x, y) = \phi_{s1}(x) + a_{11}(x)y + a_{12}(x)y^2 \quad \text{for} \quad 0 \leq x \leq L_1, 0 \leq y \leq t_{s-si} \quad (2.6)$$

$$\phi_2(x, y) = \phi_{s2}(x) + a_{21}(x)y + a_{22}(x)y^2 \quad \text{for} \quad L_1 \leq x \leq L, 0 \leq y \leq t_{s-si} \quad (2.7)$$

Poisson's equation can be solved by following the boundary condition

1. Electric flux(displacement) at the gate oxide/strained Si film interface is continuous

$$\left. \frac{d\phi_1(x, y)}{dy} \right|_{y=0} = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{\phi_{s1}(x) - V_{GS1}'}{t_f} \quad (2.8)$$

$$\left. \frac{d\phi_2(x, y)}{dy} \right|_{y=0} = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{\phi_{s2}(x) - V_{GS2}'}{t_f} \quad (2.9)$$

Where $V_{GS1}' = V_{GS} - (V_{FB1,f})_{si}$, $V_{GS2}' = V_{GS} - (V_{FB2,f})_{si}$

Where the effect of trapped charges are to be considered as

$$(V_{FB1,f})_{si} = \phi_M - \phi_{si}, \quad (V_{FB2,f})_{si} = \phi_M - \phi_{si} - \frac{qN_f}{C_{ox}}$$

1. Electric field at the interface of the buried oxide and the back channel is continuous

$$\left. \frac{d\phi_1(x, y)}{dy} \right|_{y=t_{si}} = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{-\phi_B'(x) + V_{SUB}'}{t_b} \quad (2.10)$$

$$\left. \frac{d\phi_2(x, y)}{dy} \right|_{y=t_{si}} = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{-\phi_B'(x) + V_{SUB}'}{t_b} \quad (2.11)$$

Where $V_{SUB}' = V_{SUB} - (V_{FB,b})_{si}$

1. Electric flux (displacement) and the electric potential at the trapped charged interface is continuous

$$\left. \frac{d\phi_1(x, y)}{dx} \right|_{x=L_1} = \left. \frac{d\phi_2(x, y)}{dx} \right|_{x=L_1} \quad (2.12)$$

$$\phi_1(L_1, 0) = \phi_2(L_1, 0) \quad (2.13)$$

2. The surface potential at the source end is

$$\phi_1(0, 0) = \phi_{s1}(0) = V_{bi,si} \quad (2.14)$$

3. The surface potential at the drain end is

$$\phi_2(L_1 + L_2, 0) = \phi_{s2}(L_1 + L_2) = V_{bi,si} + V_{DS} \quad (2.15)$$

Using the boundary conditions (8)-(11) we obtain coefficients and obtain the expressions for $\phi_1(x, y)$ and $\phi_2(x, y)$. Substituting $\phi_1(x, y)$ and $\phi_2(x, y)$ into (4) and (5) respectively and substiting $y=0$ we obtain

$$\frac{d^2\phi_{s1}(x)}{dx^2} - \alpha\phi_{s1}(x) = \beta_1 \quad (2.16)$$

$$\frac{d^2\phi_{s2}(x)}{dx^2} - \alpha\phi_{s2}(x) = \beta_2 \quad (2.17)$$

Where $\alpha = \frac{2(C_f C_{si} + C_f C_b + C_b C_{si})}{t_{si}^2 C_{si} (2C_{si} + C_b)}$,

$$\beta_1 = \frac{qN_A}{\epsilon_{si}} - 2V_{GS1}' \frac{C_f (C_{si} + C_b)}{t_{si}^2 C_{si} (2C_{si} + C_b)} - 2V_{SUB}' \frac{C_b}{t_{si}^2 C_{si} (2C_{si} + C_b)},$$

$$\beta_2 = \frac{qN_A}{\epsilon_{si}} - 2V_{GS2}' \frac{C_f (C_{si} + C_b)}{t_{si}^2 C_{si} (2C_{si} + C_b)} - 2V_{SUB}' \frac{C_b}{t_{si}^2 C_{si} (2C_{si} + C_b)}$$

The solution for (16) and (17) are simple second order non-homogenous differential equation with constant coefficients which can be expressed as

$$\phi_{s1}(x) = A \exp(nx) + B \exp(-n * x) - \frac{\beta_1}{\alpha} \quad (2.18)$$

$$\phi_{s2}(x) = C \exp(n(x - L_1)) + D \exp(-n(x - L_1)) - \frac{\beta_2}{\alpha} \quad (2.19)$$

Where $n = \sqrt{\alpha}$, $p_1 = \frac{\beta_1}{\alpha}$, $p_2 = \frac{\beta_2}{\alpha}$

Using the boundary condition (15)-(18) we solve for A, B, C, D

$$A = ((V_{bi,si}(1 - \exp(-nL)) + V_{DS} + (p_1 - p_2) \cosh(nL_2) + p_2 - p_1 \exp(-nL)) / (2 \sinh(nL))) \quad (2.20)$$

$$B = ((V_{bi,si}(\exp(nL) - 1) + p_1 \exp(nL) - p_2 - V_{DS} - (p_1 - p_2) \cosh(nL_2)) / (2 \sinh(nL))) \quad (24)$$

$$C = A \exp(nL_1) + \frac{p_2 - p_1}{2} \quad (2.21)$$

$$D = B \exp(-nL_1) + (\frac{p_2 - p_1}{2}) \quad (2.22)$$

Electric field horizontal component under metal gates M1/M2 can be expressed as

$$E_1(x) = An \exp(nx) - Bn \exp(-nx) \quad (2.23)$$

$$E_2(x) = Cn \exp(n(x - L_1)) - Dn \exp(-n(x - L_1)) \quad (2.24)$$

The minimum potential of front channel can be expressed as

$$x_{\min} = \frac{1}{2n} \ln\left(\frac{B}{A}\right) \quad (2.25)$$

$$\phi_{s,\min} = 2\sqrt{AB} - p_1 \quad (2.26)$$

Threshold voltage modelling

For strained-Si SOI MOSFET the threshold condition under the front gate is modified as

$$\phi_{s,\min} = \phi_{th} = 2\phi_{f,si} \quad (2.27)$$

$$V_{TH} = \frac{-\eta + \sqrt{\eta^2 - 4\sigma\xi}}{2\sigma} \quad (2.28)$$

Where $\gamma = \exp(-nL)$, $\sigma = \frac{1}{\gamma} + \gamma - 2 - \sinh^2(nL)$,

$$V_{bi1} = V_{bi,si}(1 - \gamma) + V_{DS} - (u - v) \cosh(nL_2) - v + u\gamma$$

$$V_{bi2} = V_{bi,si}\left(\frac{1}{\gamma} - 1\right) - V_{DS} + (u - v) \cosh(nL_2) + v - \frac{u}{\gamma}$$

$$u = \frac{C_b}{C_f} V_{SUB}' - \frac{qN_A t_{si}}{C_f} - V_{FB1,si}, \quad v = \frac{C_b}{C_f} V_{SUB}' - \frac{qN_A t_{si}}{C_f} - V_{FB2,si}$$

$$\xi = V_{bi1} V_{bi2} - \sinh^2(nL)(\phi_{th} - u)^2, \quad \eta = V_{bi1}\left(-\frac{1}{\gamma} + 1\right) + 2 \sinh^2(nL)(\phi_{th} - u) - V_{bi2}(1 - \gamma)$$

2.4.2 Modeling of the Surface Potential (Double Gate)

Effect of Strain on band structure

Flat band voltage (front channel)

$$(V_{FB,f})_{si} = \phi_M - \phi_{si} \quad (2.29)$$

Where $\phi_{f-si} = V_T \ln\left(\frac{N_a}{n_i}\right)$, $\phi_{si} = \frac{\chi_{si}}{q} + \frac{E_{g,si}}{2q} + \phi_{f-si}$

Back channel flat band voltage (back channel)

$$(V_{FB,b})_{si} = \phi_M - \phi_{si} \quad (2.30)$$

Where $\phi_{sub} = \frac{\chi_{si}}{q} + \frac{E_{g,si}}{2q} + \phi_{f-sub}$, $\phi_{f-sub} = V_T \ln\left(\frac{N_{sub}}{n_i}\right)$

Built in voltage across source-body and drain body junction

$$V_{bi,si} = \frac{E_{g,si}}{2q} + \phi_{f-si} \quad (2.31)$$

Model Formulation

2-D Poisson's equation

$$\frac{\partial^2 \phi_1(x, y)}{\partial x^2} + \frac{\partial^2 \phi_1(x, y)}{\partial y^2} = \frac{qN_A}{\epsilon_{si}} \quad \text{for} \quad 0 \leq x \leq L_1, 0 \leq y \leq t_{s-si} \quad (2.32)$$

$$\frac{\partial^2 \phi_2(x, y)}{\partial x^2} + \frac{\partial^2 \phi_2(x, y)}{\partial y^2} = \frac{qN_A}{\epsilon_{si}} \quad \text{for} \quad L_1 \leq x \leq L, 0 \leq y \leq t_{s-si} \quad (2.33)$$

The potential profile in the vertical direction can be approximated by a parabolic function

$$\phi_1(x, y) = \phi_{s1}(x) + a_{11}(x)y + a_{12}(x)y^2 \quad \text{for} \quad 0 \leq x \leq L_1, 0 \leq y \leq t_{s-si} \quad (2.34)$$

$$\phi_2(x, y) = \phi_{s2}(x) + a_{21}(x)y + a_{22}(x)y^2 \quad \text{for} \quad L_1 \leq x \leq L, 0 \leq y \leq t_{s-si} \quad (2.35)$$

Poisson's equation can be solved by following the boundary condition

2. Electric flux(displacement) at the gate oxide/strained Si film interface is continuous

$$\left. \frac{d\phi_1(x, y)}{dy} \right|_{y=0} = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{\phi_{s1}(x) - V'_{GS1}}{t_f} \quad (2.36)$$

$$\left. \frac{d\phi_2(x, y)}{dy} \right|_{y=0} = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{\phi_{s2}(x) - V'_{GS2}}{t_f} \quad (2.37)$$

Where $V'_{GS1} = V_{GS} - (V_{FB1,f})_{si}$, $V'_{GS2} = V_{GS} - (V_{FB2,f})_{si}$

Where the effect of trapped charges are to be considered as

$$(V_{FB1,f})_{si} = \phi_M - \phi_{si}, \quad (V_{FB2,f})_{si} = \phi_M - \phi_{si} - \frac{qN_f}{C_{ox}}$$

2. Electric field at the interface of the buried oxide and the back channel is continuous

$$\left. \frac{d\phi_1(x, y)}{dy} \right|_{y=t_{si}} = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{-\phi_B(x) + V'_{SUB}}{t_b} \quad (2.38)$$

$$\left. \frac{d\phi_2(x, y)}{dy} \right|_{y=t_{si}} = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{-\phi_B(x) + V'_{SUB}}{t_b} \quad (2.39)$$

Where $V'_{SUB} = V_{GS} - (V_{FB,b})_{si}$

4. Electric flux (displacement) and the electric potential at the trapped charged interface is continuous

$$\left. \frac{d\phi_1(x, y)}{dx} \right|_{x=L_1} = \left. \frac{d\phi_2(x, y)}{dx} \right|_{x=L_1} \quad (2.40)$$

$$\phi_1(L_1, 0) = \phi_2(L_1, 0) \quad (2.41)$$

5. The surface potential at the source end is

$$\phi_1(0, 0) = \phi_{s1}(0) = V_{bi,si} \quad (2.42)$$

6. The surface potential at the drain end is

$$\phi_2(L_1 + L_2, 0) = \phi_{s2}(L_1 + L_2) = V_{bi,si} + V_{DS} \quad (2.43)$$

Using the boundary conditions (8)-(11) we obtain coefficients and obtain the expressions for $\phi_1(x, y)$ and $\phi_2(x, y)$. Substituting $\phi_1(x, y)$ and $\phi_2(x, y)$ into (4) and (5) respectively and substiting $y=0$ we obtain

$$\frac{d^2\phi_{s1}(x)}{dx^2} - \alpha\phi_{s1}(x) = \beta_1 \quad (2.44)$$

$$\frac{d^2\phi_{s2}(x)}{dx^2} - \alpha\phi_{s2}(x) = \beta_2 \quad (2.45)$$

Where $\alpha = \frac{2(C_f C_{si} + C_f C_b + C_b C_{si})}{t_{si}^2 C_{si} (2C_{si} + C_b)}$,

$$\beta_1 = \frac{qN_A}{\epsilon_{si}} - 2V'_{GS1} \frac{C_f (C_{si} + C_b)}{t_{si}^2 C_{si} (2C_{si} + C_b)} - 2V'_{SUB} \frac{C_b}{t_{si}^2 C_{si} (2C_{si} + C_b)},$$

$$\beta_2 = \frac{qN_A}{\epsilon_{si}} - 2V'_{GS2} \frac{C_f (C_{si} + C_b)}{t_{si}^2 C_{si} (2C_{si} + C_b)} - 2V'_{SUB} \frac{C_b}{t_{si}^2 C_{si} (2C_{si} + C_b)}$$

The solution for (16) and (17) are simple second order non-homogenous differential equation with constant coefficients which can be expressed as

$$\phi_{s1}(x) = A \exp(nx) + B \exp(-n^*x) - \frac{\beta_1}{\alpha} \quad (2.46)$$

$$\phi_{s2}(x) = C \exp(n(x - L_1)) + D \exp(-n(x - L_1)) - \frac{\beta_2}{\alpha} \quad (2.47)$$

Where $n = \sqrt{\alpha}$, $p_1 = \frac{\beta_1}{\alpha}$, $p_2 = \frac{\beta_2}{\alpha}$

Using the boundary condition (15)-(18) we solve for A, B, C, D

$$A = ((V_{bi,si}(1 - \exp(-nL)) + V_{DS} + (p_1 - p_2) \cosh(nL_2) + p_2 - p_1 \exp(-nL)) / (2 \sinh(nL))) \quad (20)$$

$$B = ((V_{bi,si}(\exp(nL) - 1) + p_1 \exp(nL) - p_2 - V_{DS} - (p_1 - p_2) \cosh(nL_2)) / (2 \sinh(nL)))$$

$$C = A \exp(nL_1) + \frac{p_2 - p_1}{2} \quad (2.48)$$

$$D = B \exp(-nL_1) + (\frac{p_2 - p_1}{2}) \quad (2.49)$$

Electric field horizontal component under metal gates M1/M2 can be expressed as

$$E_1(x) = A \exp(nx) - B \exp(-nx) \quad (2.50)$$

$$E_2(x) = C \exp(n(x - L_1)) - D \exp(-n(x - L_1)) \quad (2.51)$$

The minimum potential of front channel can be expressed as

$$x_{\min} = \frac{1}{2n} \ln\left(\frac{B}{A}\right) \quad (2.52)$$

$$\phi_{s,\min} = 2\sqrt{AB} - p_1 \quad (2.53)$$

Threshold voltage modelling

For strained-Si SOI MOSFET the threshold condition under the front gate is modified as

$$\phi_{s,\min} = \phi_{th} = 2\phi_{f,si} \quad (2.54)$$

$$V_{TH} = \frac{-\eta + \sqrt{\eta^2 - 4\sigma\xi}}{2\sigma} \quad (2.55)$$

Where $\gamma = \exp(-nL)$, $\sigma = \frac{1}{\gamma} + \gamma - 2 - \sinh^2(nL)$,

$$V_{bi1} = V_{bi,si}(1 - \gamma) + V_{DS} - (u - v) \cosh(nL_2) - v + u\gamma$$

$$V_{bi2} = V_{bi,si}\left(\frac{1}{\gamma} - 1\right) - V_{DS} + (u - v) \cosh(nL_2) + v - \frac{u}{\gamma}$$

$$u = \frac{C_b}{C_f} V'_{SUB} - \frac{qN_A t_{si}}{C_f} - V_{FB1,si}, \quad v = \frac{C_b}{C_f} V'_{SUB} - \frac{qN_A t_{si}}{C_f} - V_{FB2,si}$$

$$\xi = V_{bi1} V_{bi2} - \sinh^2(nL)(\phi_{th} - u)^2, \quad \eta = V_{bi1}\left(-\frac{1}{\gamma} + 1\right) + 2 \sinh^2(nL)(\phi_{th} - u) - V_{bi2}(1 - \gamma)$$

2.5 Results and discussions

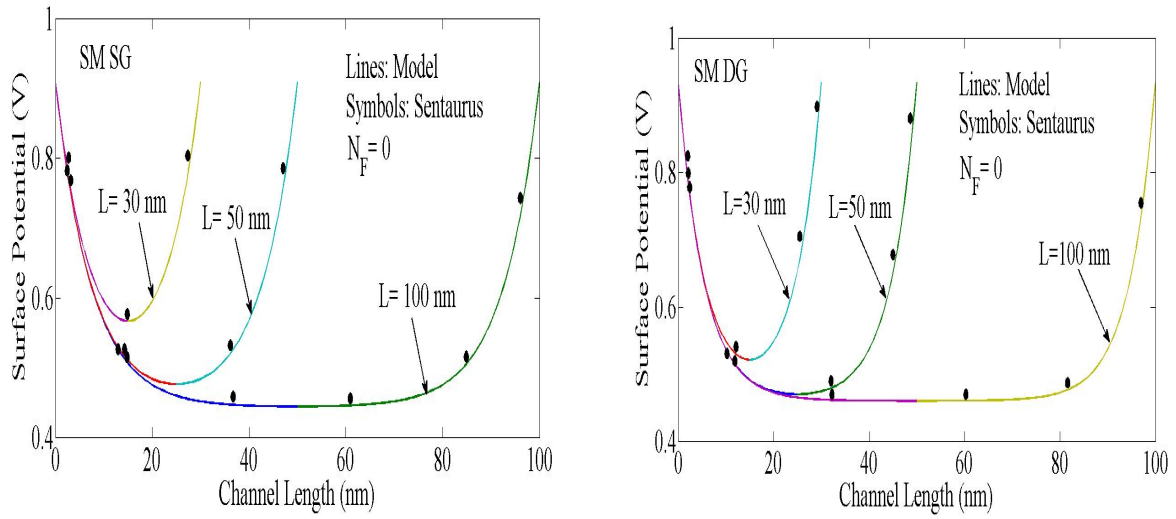


Fig 2.3 Variation of Surface potential for different channel length (Single Gate and Double Gate)

Parameters used are $\phi_M = 4.6$ eV, $N_A = 1 \times 10^{16}$ cm $^{-3}$, $t_{Si} = 10$ nm, $L = 30, 50, 100$ nm, $t_{ox} = 2$ nm, $V_{DS} = 0.0$ V and $V_{GS} = 0.1$ V., $N_F = 0$

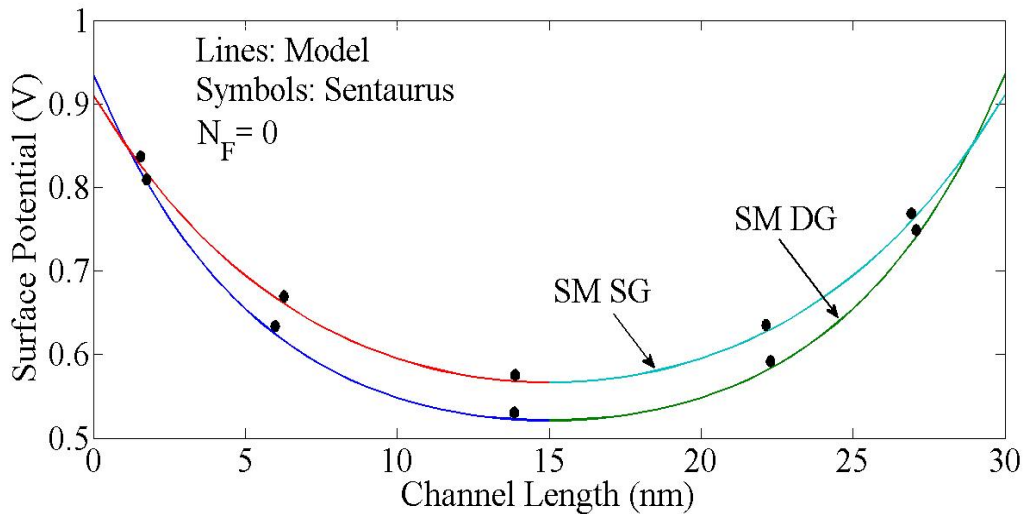


Fig 2.4 Comparison of Variation of Surface potential for (Single Gate and Double Gate)

Parameters used are $\phi_M = 4.6$ eV, $N_A = 1 \times 10^{16}$ cm $^{-3}$, $t_{Si} = 10$ nm, $L = 30$ nm, $t_{ox} = 2$ nm, $V_{DS} = 0.0$ V and $V_{GS} = 0.1$ V., $N_F = 0$.

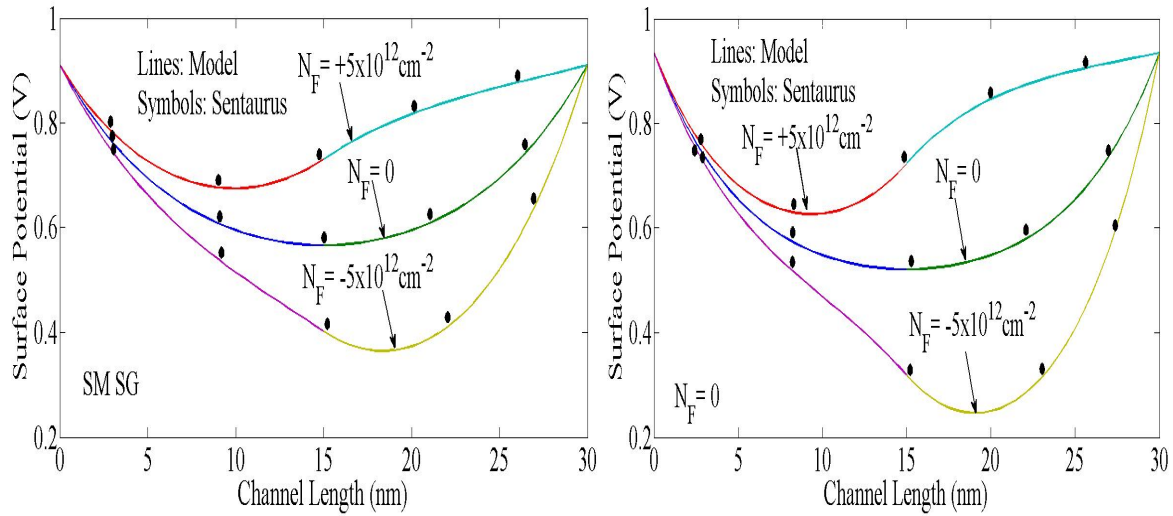


Fig 2.5 Variation of Surface potential for different trapped charge (Single Gate and Double Gate)

Parameters used are $\phi_M = 4.6$ eV, $N_A = 1 \times 10^{16} \text{ cm}^{-3}$, $t_{Si} = 10$ nm, $L = 30, 50, 100$ nm, $t_{ox} = 2$ nm, $V_{DS} = 0.0$ V and $V_{GS} = 0.1$ V., $N_f = 0, 5e12, -5e12$.

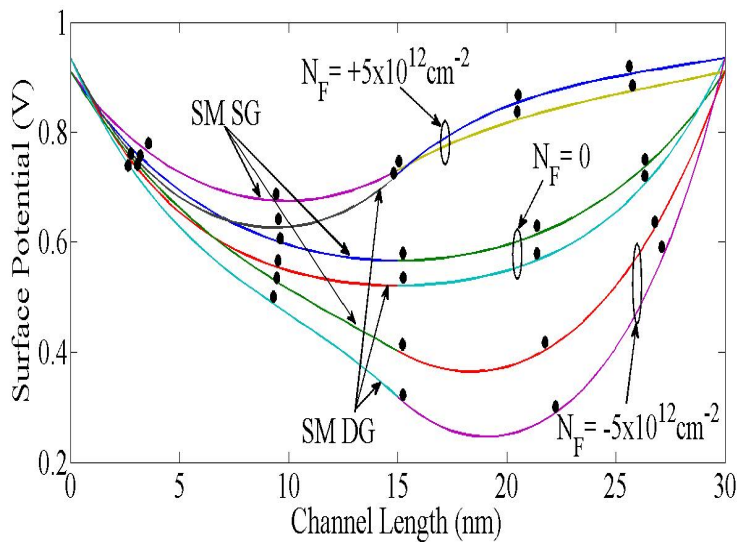


Fig 2,6 Variation of Surface potential for different trapped charge (Single Gate and Double Gate)

Parameters used are $\phi_M = 4.6$ eV, $N_A = 1 \times 10^{16} \text{ cm}^{-3}$, $t_{Si} = 10$ nm, $L = 30, 50, 100$ nm, $t_{ox} = 2$ nm, $V_{DS} = 0.0$ V and $V_{GS} = 0.1$ V., $N_f = 0, 5e12, -5e12$.

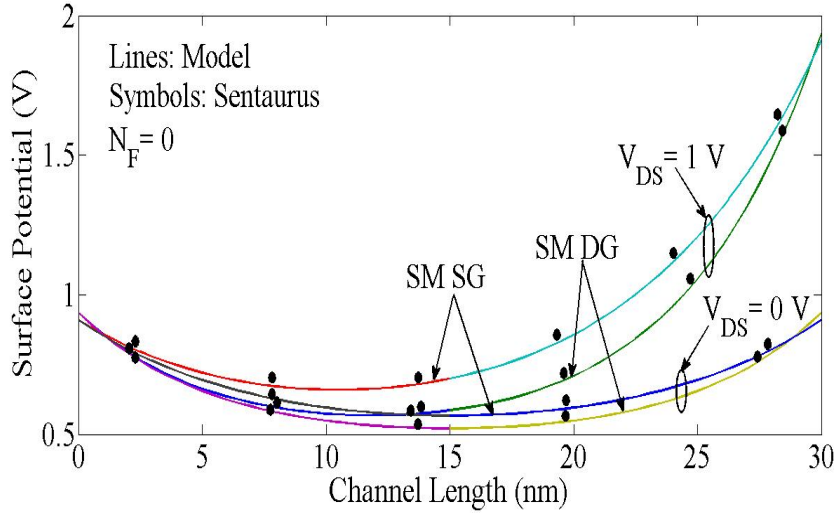


Fig 2.7 Variation of Surface potential for different V_{DS} (Single Gate and Double Gate)

Parameters used are $\phi_M = 4.6$ eV, $N_A = 1 \times 10^{16} \text{ cm}^{-3}$, $t_{Si} = 10$ nm, $L = 30, 50, 100$ nm, $t_{ox} = 2$ nm, $V_{DS} = 0.0, 1.0$ V and $V_{GS} = 0.1$ V., $N_F = 0$.

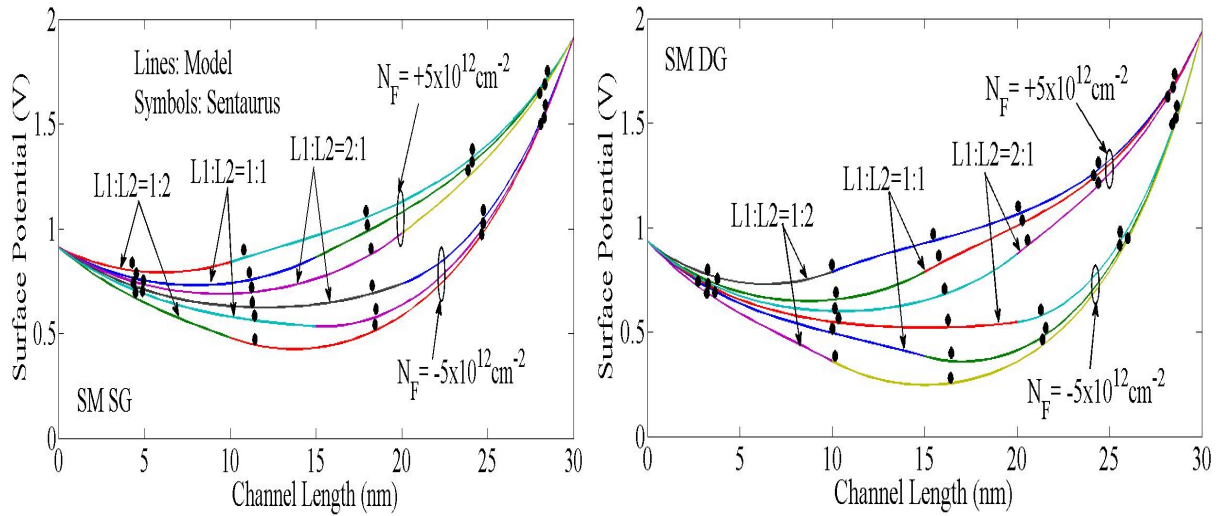


Fig 2.8 Surface Potential variation along the channel length for interface charge variations for different gate length ratios ($L1/L2 = 1:2, 1:1, 2:1$). Parameters used $X = 0.0$, $\phi_M = 4.6$ eV, $N_A = 1 \times 10^{16} \text{ cm}^{-3}$, $t_{Si} = 10$ nm, $L = 30$ nm, $t_{ox} = 2$ nm, $V_{DS} = 1$ V and $V_{GS} = 0.1$ V.

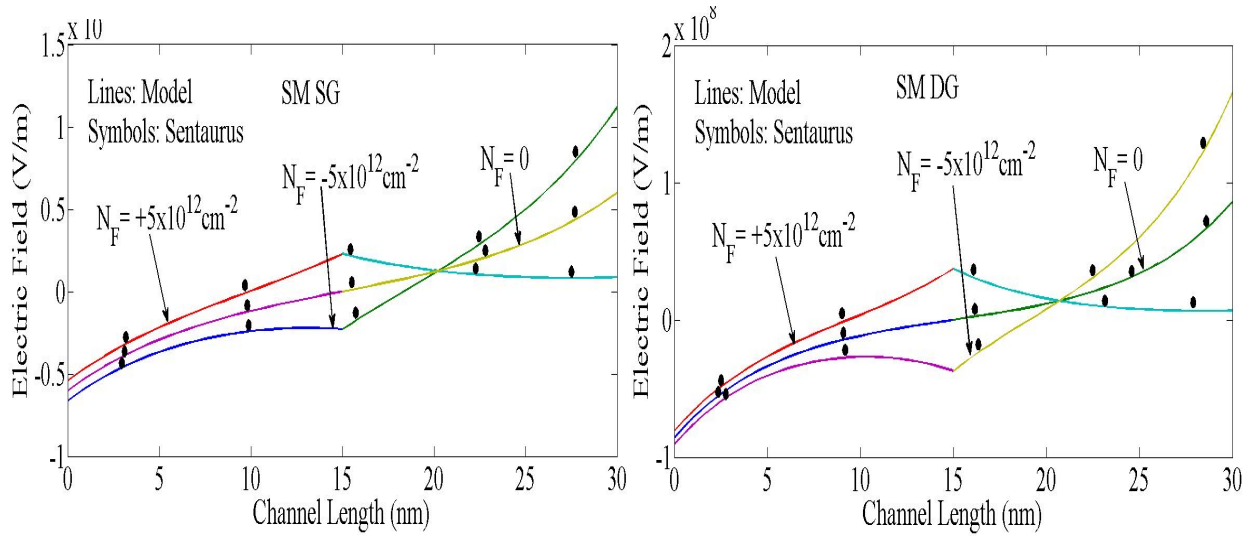


Fig 2.9 Electric Field variation along the channel length for interface charge variations. Parameters used $X=0.0$, $\phi_M = 4.6$ eV, $N_A = 1 \times 10^{16} \text{ cm}^{-3}$, $t_{si}=10$ nm, $L=30$ nm, $t_{ox}=2$ nm, $V_{DS}=1$ V and $V_{GS}=0.1$ V.

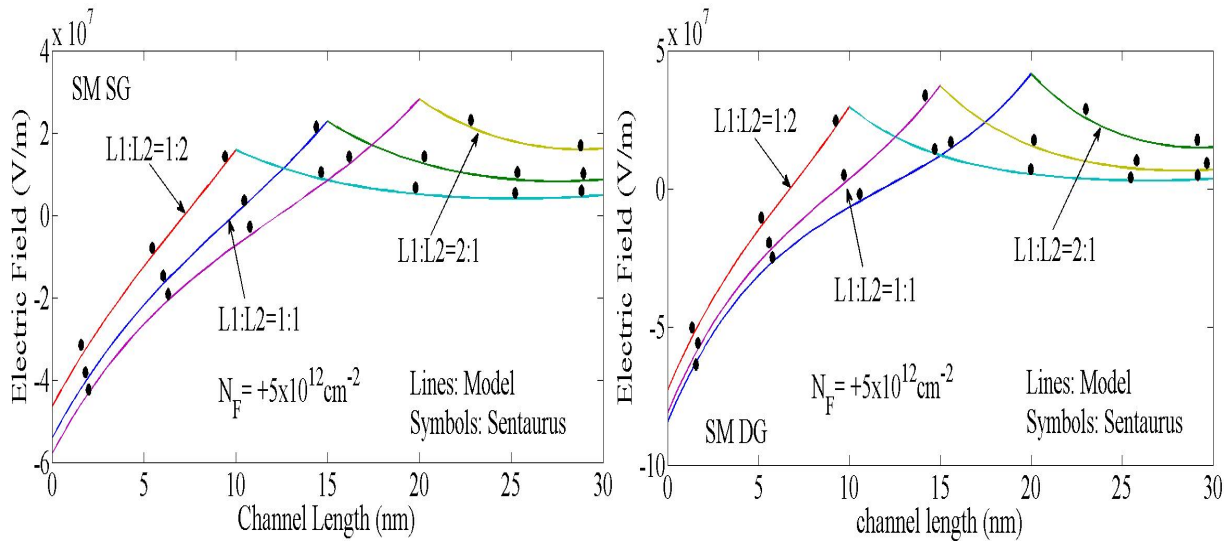


Fig 2.10 Electric Field variation along the channel length for different gate length ratios ($L1/L2=1:2$, $1:1$, $2:1$). Parameters used $X=0.0$, $\phi_M = 4.6$ eV, $N_A = 1 \times 10^{16} \text{ cm}^{-3}$, $t_{si}=10$ nm, $L=30$ nm, $t_{ox}=2$ nm, $V_{DS}=1$ V and $V_{GS}=0.1$ V.

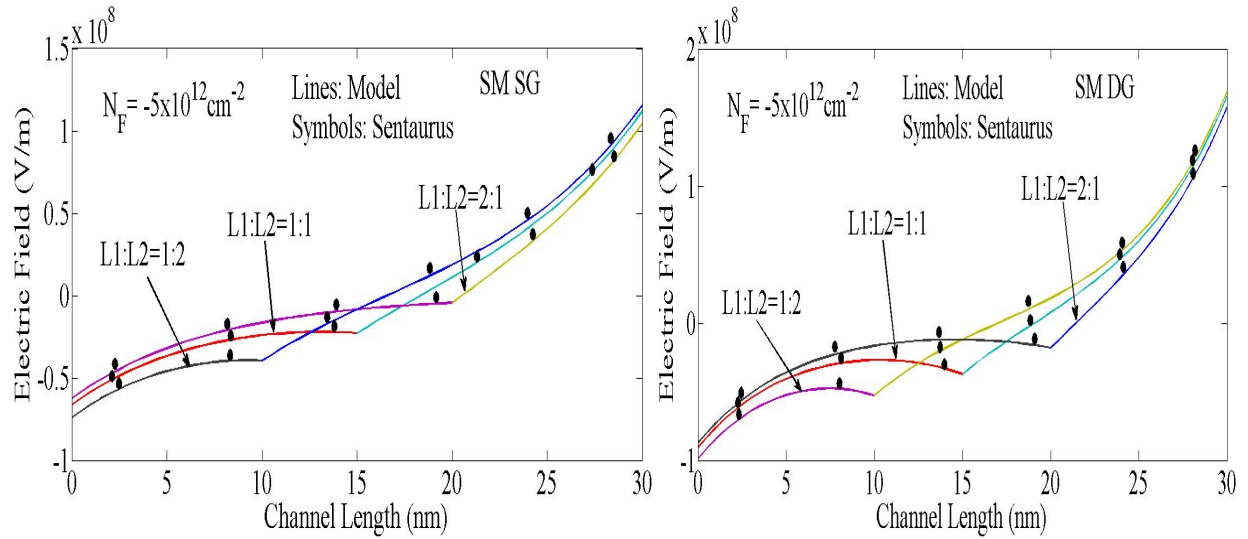
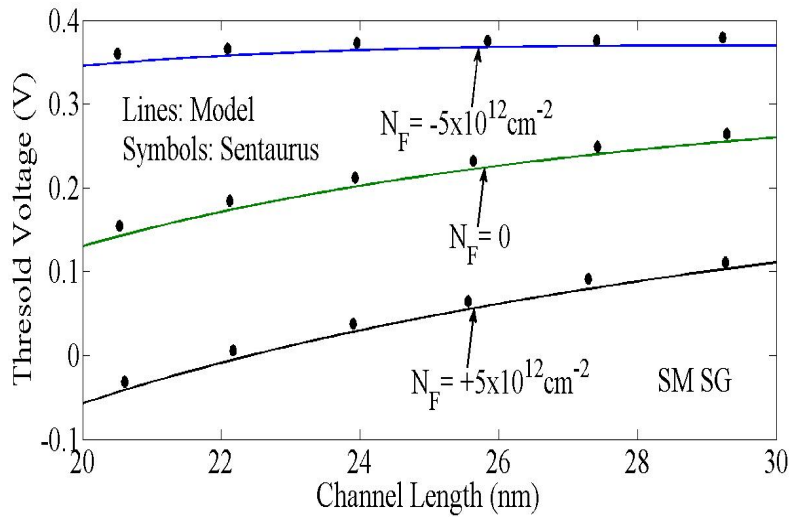


Fig 2.11 Electric Field variation along the channel length for different gate length ratios (L1/L2=1:2, 1:1, 2:1). Parameters used $X=0.0$, $\phi_M = 4.6 \text{ eV}$, $N_A = 1 \times 10^{16} \text{ cm}^{-3}$, $t_{si}=10 \text{ nm}$, $L=30 \text{ nm}$, $t_{ox}=2 \text{ nm}$, $V_{DS}=1 \text{ V}$ and $V_{GS}=0.1 \text{ V}$.

Threshold Voltage



.Fig 2.12 Threshold Voltage variation along the channel length for different gate trapped charges. Parameters used $X=0.2$, $\phi_M = 4.6 \text{ eV}$, $N_A = 1 \times 10^{16} \text{ cm}^{-3}$, $t_{si}=10 \text{ nm}$, $L=100 \text{ nm}$, $t_{ox}=2 \text{ nm}$, $V_{DS}=0.1 \text{ V}$ and $V_{GS}=0.1 \text{ V}$.

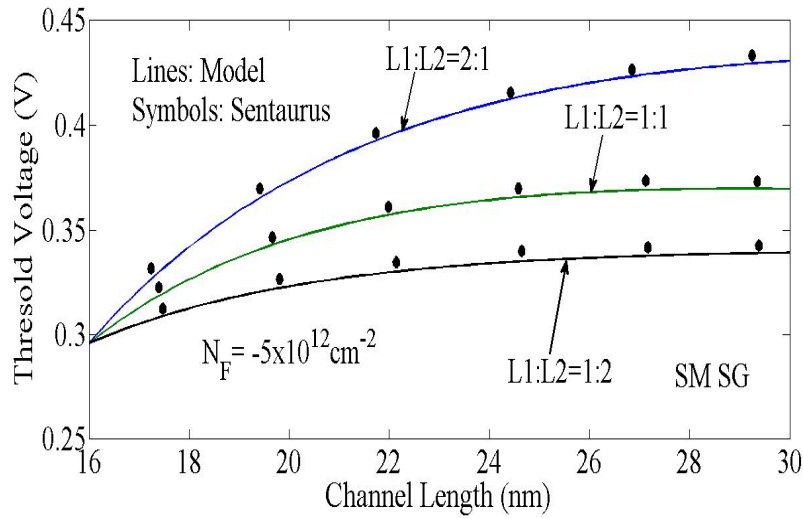


Fig 2.13 Threshold Voltage variation along the channel length for different gate length ratios (L1/L2=1:2, 1:1, 2:1). Parameters used $X=0.2$, $\phi_M=4.6$ eV, $N_A=1 \times 10^{16}$ cm⁻³, $t_{Si}=10$ nm, $L=100$ nm, $t_{ox}=2$ nm, $V_{DS}=0.1$ V and $V_{GS}=0.1$ V.

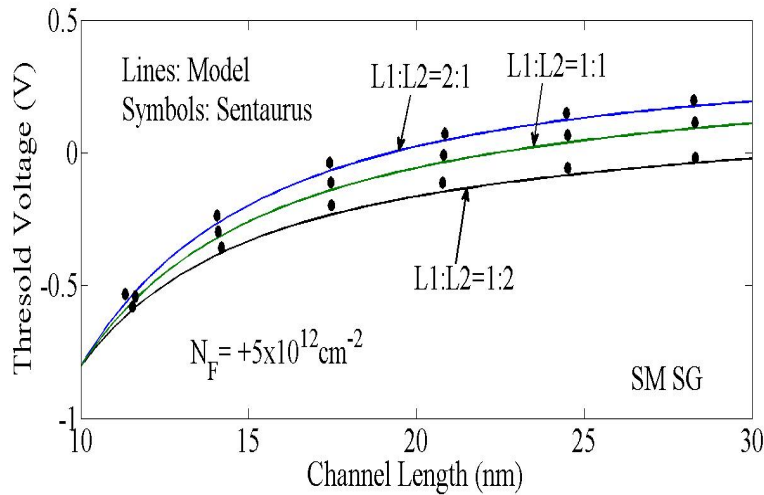


Fig 2.14 Threshold Voltage variation along the channel length for different gate length ratios (L1/L2=1:2, 1:1, 2:1). Parameters used $X=0.2$, $\phi_M=4.6$ eV, $N_A=1 \times 10^{16}$ cm⁻³, $t_{Si}=10$ nm, $L=100$ nm, $t_{ox}=2$ nm, $V_{DS}=0.1$ V and $V_{GS}=0.1$ V.

Chapter 3

Modeling of Dual Material Gate Fully Depleted Strained Silicon on Insulator (DMG-FD-S-SOI) MOSFET

3.1 INTRODUCTION

To minimize SCEs, a new structure called a dual material gate (DMG) MOSFET has been proposed. This structure has two different metals M1, M2 with different work function. This configuration provides instantaneous increase in transconductance and suppressed SCEs due to a step in the surface potential profile as equated to a single gate MOSFET. In the DMG structure the peak electric field at the drain end is reduced.

For the first time M. Jagadesh Kumar *et. al.* [22] proposed a simple analytical model of threshold voltage for single layer FD-S-SOI MOSFET in 2006. They had shown the dependency of various parameters like Ge mole fraction (X), strained silicon thickness (t_{si}) and doping concentration on the threshold voltage. Li Jin *et. al.* [23] proposed a two dimensional threshold voltage model for DMG strained SOI MOSFET. They have discussed how effectively the device was able to suppress the hot carrier effects (HCE) and threshold voltage roll-off. Similarly, the effect of double layer strain (i.e strained silicon on SiGe relaxed layer) is discussed by Shiv Bhusan *et. al.* [24]. They have also discussed about the improved short channel effects because of the DMG and strain silicon. However, no body have considered the effect of interface trap charges while solving the 2-D Poisson's equation.

In this work, the analytical model for surface potential, electric field, and threshold voltage for a DMG-FD-S-SOI is formulated including the effects of interface charges. The interface charges are considered both in magnitude and polarity with an assumption that the charge distribution is uniform along the channel. Parabolic approximation method is used for solving the 2-D Poisson's equation to formulate the surface potential and further virtual cathode potential method is used for modelling the threshold voltage. An extensive analysis is carried out to study the effect of various parameters like Ge mole fraction, drain bias, gate length ratio variation, and interface charge variation on surface potential, electric field, and threshold voltage.

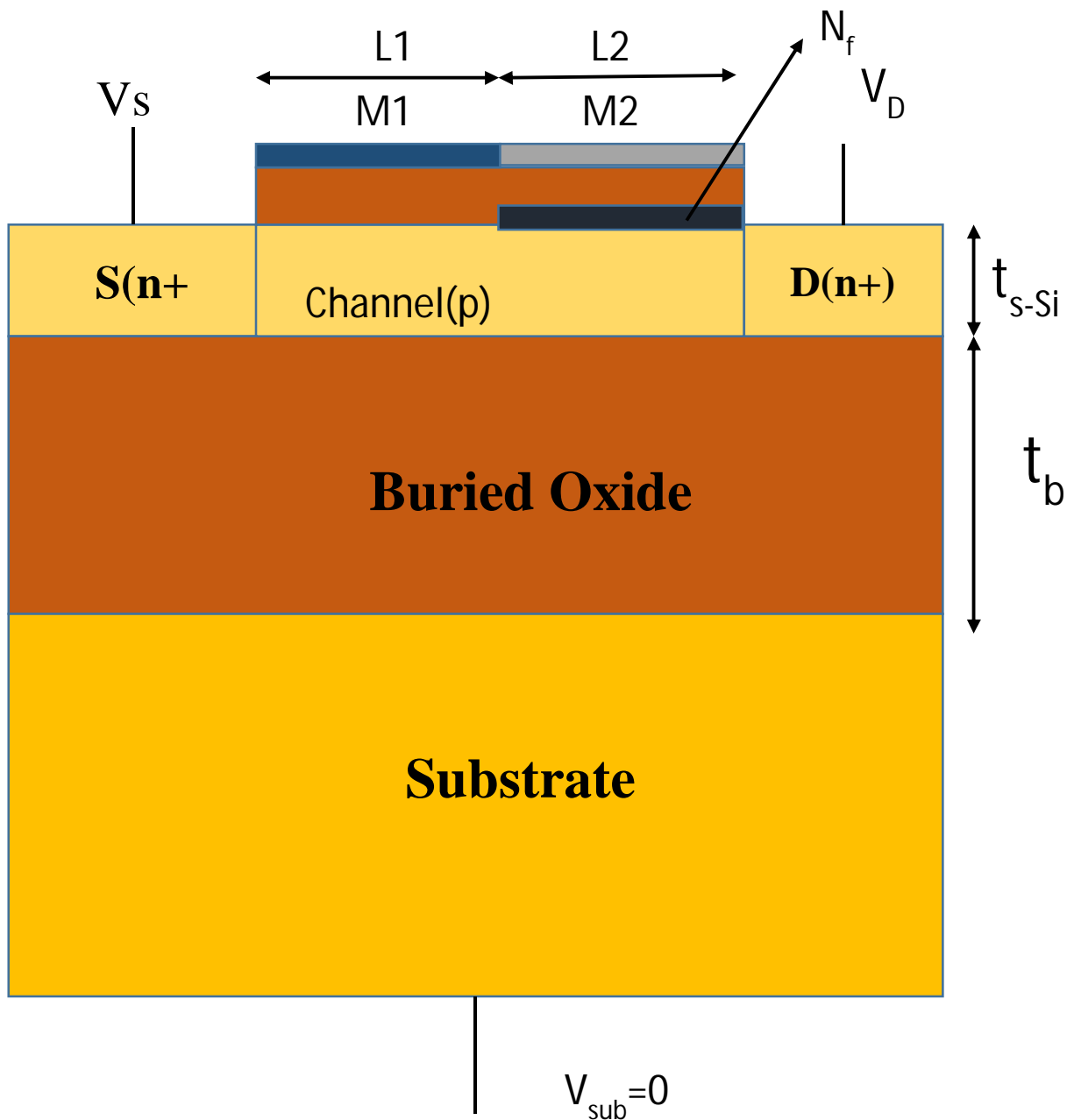


Fig 3.2 Schematic Diagram of DMG-FD-S-SOI MOSFET

3.2 Effect of Strain on Band Structure

The device simulator model library of Sentaurus™ has been modified according to the effects of strain on silicon band structure. Effects of strain in silicon band structure can be modelled as:

$$(\Delta E_c)_{s-Si} = 0.57 X \quad (3.1)$$

$$(\Delta E_g)_{s-Si} = 0.4 X \quad (3.2)$$

$$V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) = V_T \ln\left(\frac{m_{h,si}^*}{m_{h,s-Si}^*}\right)^{3/2} = 0.075 X \quad (3.3)$$

where $(\Delta E_c)_{s-Si}$ is the increase in electron affinity of silicon because of strain, $(\Delta E_g)_{s-Si}$ is the decrease in the band gap of silicon due to strain, V_T is the thermal voltage, $N_{V,Si}$ and $N_{V,s-Si}$ are the density of states in valence band in the unstrained and strained silicon respectively, $m_{h,si}^*$ and $m_{h,s-Si}^*$ are the hole density of states or effective masses in the unstrained and strained silicon.

The effect of strain on flat band voltage (front channel) can be modeled as:

$$(V_{FB,f})_{s-Si} = (V_{FB,f})_{si} + \Delta V_{FB,f} \quad (3.4)$$

Where

$$(V_{FB,f})_{si} = \phi_M - \phi_{si}$$

$$\Delta V_{FB,f} = -\frac{(\Delta E_c)_{s-Si}}{q} + \frac{(\Delta E_g)_{s-Si}}{q} - V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right)$$

ϕ_M and ϕ_{si} are the metal work function and Si work function respectively, q is the electronic charge of the Si, $(V_{FB,f})_{s-Si}$ and $(V_{FB,f})_{si}$ are the flat band voltage in the front channel of a bulk MOSFET and strained-Si MOSFET respectively. $\Delta V_{FB,f}$ represents the amount of change in flat band voltage due to strain.

$$\phi_{si} = \frac{\chi_{si}}{q} + \frac{E_{g,si}}{2q} + \phi_{f-si} \quad (3.5)$$

$$\phi_{f-si} = V_T \ln\left(\frac{N_a}{n_i}\right) \quad (3.6)$$

where, ϕ_{si} is the unstrained Si work function, χ_{si} is electron affinity of the silicon, $E_{g,si}$ represents the band gap of unstrained Si, ϕ_{f-si} is the Fermi potential in unstrained Si, N_a is the body doping concentration, and n_i represents the intrinsic carrier concentration in unstrained Si.

The effect of strain on flat band voltage (back channel) can be modeled as:

$$(V_{FB,b})_{s-Si} = (V_{FB,b})_{si} + \Delta V_{FB,b} \quad (3.7)$$

Where

$$(V_{FB,b})_{si} = \phi_{sub} - \phi_{si}$$

$$\Delta V_{FB,b} = -\frac{(\Delta E_c)_{s-Si}}{q} + \frac{(\Delta E_g)_{s-Si}}{q} - V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right)$$

$$\phi_{sub} = \frac{\chi_{si}}{q} + \frac{E_{g,Si}}{2q} + \phi_{f-sub}$$

$$\phi_{f-sub} = V_T \ln\left(\frac{N_{sub}}{n_i}\right)$$

$(V_{FB,b})_{si}$ And $(V_{FB,b})_{s-Si}$ are the flat band voltage in the back channel of a bulk MOSFET and strained-Si MOSFET respectively. $\Delta V_{FB,b}$ Represents the amount of change in back flat band voltage due to strain. $(\Delta E_c)_{s-Si}$ represents the change in conduction band of unstrained Si, ϕ_{f-Sub} is the substrate Fermi potential, N_{sub} is the substrate doping.

Due to the strained-Si thin film, the built-in voltage across the source-body and drain-body junctions are also affected and this can be modified as:

$$V_{bi,s-Si} = V_{bi,Si} + (\Delta V_{bi})_{s-Si} \quad (3.8)$$

Where

$$V_{bi,Si} = \frac{E_{g,Si}}{2q} + \phi_{f-Si}$$

$$(\Delta V_{bi})_{s-Si} = -\frac{(\Delta E_g)_{s-Si}}{q} - V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right)$$

Where $V_{bi,Si}$ and $(\Delta V_{bi})_{s-Si}$ are the unstrained Si built in potential and change in built in potential due to strain respectively

3.3 Analytical Model Formulation

3.3.1 Surface Potential Formulation

The front gate consists of dual material M1 (p+ poly) and M2 (n+ poly) of Lengths L1 and L2 respectively while the back gate is effectively an n+ poly gate. The impurity density is assumed to be uniform and neglecting the effect of fixed oxide charges has been neglected of the channel, the potential distribution in thin silicon film can be written as passion equation.

$$\frac{d^2\phi(x, y)}{dx^2} + \frac{d^2\phi(x, y)}{dy^2} = \frac{qN_a}{\epsilon_{si}}$$

$$\text{For } 0 \leq x \leq L, 0 \leq y \leq tsi \quad (3.9)$$

Where N_a =uniform film doping concentration independent of gate length, ϵ_{si} is dielectric strength of silicon, tsi is the film thickness, L is device channel length. The potential profile in the vertical direction can be approximated by a simple parabolic function.

$$\phi(x, y) = \phi_s(x) + a_1(x)y + a_2(x)y^2 \quad (3.10)$$

Where $\phi_s(x)$ is surface potential and the arbitrary coefficient $a_1(x)$ and $a_2(x)$ are function of x only. Since we have two regions in the front gate of the DMDG structure, the surface potential can be written as

$$\phi_1(x, y) = \phi_{s1}(x) + a_{11}(x)y + a_{12}(x)y^2 \quad \text{For } 0 \leq x \leq L1, 0 \leq y \leq tsi \quad (3.11)$$

$$\phi_2(x, y) = \phi_{s2}(x) + a_{12}(x)y + a_{22}(x)y^2 \quad \text{For } L1 \leq x \leq L, 0 \leq y \leq tsi \quad (3.12)$$

Where $\phi_{s1}(x)$, and $\phi_{s2}(x)$ are the surface potential under gate electrode M1 and M2 respectively. The coefficients of $a_{11}(x)$, $a_{12}(x)$, $a_{12}(x)$, and $a_{22}(x)$ are the functions of x only. The Poisson's equation can be solved by using the following boundary conditions.

The Poisson's equation is solved by using boundary condition.

1. Electric flux at the front gate oxide interface is continuous for DMG.

$$\frac{d\phi_1(x, y)}{dy} = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{\phi_{s1}(x) - V_{gs, f1}}{t_f} \quad (3.13)$$

$$(3.14) \quad \frac{d\phi_2(x,y)}{dy} = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{\phi_{s2}(x) - V_{gs,f2}}{t_f}$$

Where

$$V'_{GS1} = V_{GS} - (V_{FB1,f})_{s-Si}$$

$$V'_{GS2} = V_{GS} - (V_{FB2,f})_{s-Si}$$

Where the effect of trapped charges are to be considered

$$(V_{FB1,f})_{s-Si} = (V_{FB1,f})_{si} + \Delta V_{FB,f}$$

$$(V_{FB2,f})_{s-Si} = (V_{FB2,f})_{si} + \Delta V_{FB,f} - \frac{qN_f}{C_{ox}}$$

$$(V_{FB1,f})_{si} = \phi_{M1} - \phi_{si}$$

$$(V_{FB2,f})_{si} = \phi_{M2} - \phi_{si}$$

2. Electric field at the back gate oxide and back channel interface is continuous for both the materials of the front gate (p+ poly and n+ poly).

$$\frac{d\phi_1(x,y)}{dy} = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{V_{gs,b} - \phi_b(x)}{t_b} \quad (3.15)$$

$$\frac{d\phi_2(x,y)}{dy} = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{V_{gs,b} - \phi_b(x)}{t_b} \quad (3.16)$$

3. Surface potential at the interface of the two dissimilar gate materials of the front gate is continuous.

$$\phi_1(L_1, 0) = \phi_2(L_1, 0) \quad (3.17)$$

4. Electric flux at the interface of two materials of the front gate is continuous.

$$\frac{d\phi_1(x,y)}{dx} = \frac{d\phi_2(x,y)}{dx} \quad (3.18)$$

5. The potential at the source end is

$$\phi_1(0,0) = \phi_{s1}(0) = V_{bi} \quad (3.19)$$

6. The potential at the drain end is

$$\phi_{s2}(L1 + L2) = V_{bi} + V_{DS} \quad (3.20)$$

Using the boundary conditions equations (11)-(14) we obtain coefficients and obtain the expressions for $\phi_1(x, y)$ and $\phi_2(x, y)$. Substituting $\phi_1(x, y)$ and $\phi_2(x, y)$ into equation (7) and equation (8) respectively and subsisting $y=0$, we obtain:

$$\frac{d^2\phi_{s1}(x)}{dx^2} - \alpha\phi_{s1}(x) = \beta_1$$

$$\frac{d^2\phi_{s2}(x)}{dx^2} - \alpha\phi_{s2}(x) = \beta_2$$

Where

$$\alpha = \frac{2\left(1 + \frac{C_f}{C_b} + \frac{C_f}{C_{si}}\right)}{t_{si}^2\left(1 + \frac{2C_{si}}{C_b}\right)}$$

$$\beta_1 = \frac{qN_a}{\epsilon_{si}} - 2 * V_{gs,f1} * \frac{\left(\frac{C_f}{C_b} + \frac{C_f}{C_{si}}\right)}{t_{si}^2\left(1 + \frac{2C_{si}}{C_b}\right)} - 2 * V_{gs,b} * \frac{1}{t_{si}^2\left(1 + \frac{2C_{si}}{C_b}\right)}$$

$$\beta_2 = \frac{qN_a}{\epsilon_{si}} - 2 * V_{gs,f2} * \frac{\left(\frac{C_f}{C_b} + \frac{C_f}{C_{si}}\right)}{t_{si}^2\left(1 + \frac{2C_{si}}{C_b}\right)} - 2 * V_{gs,b} * \frac{1}{t_{si}^2\left(1 + \frac{2C_{si}}{C_b}\right)}$$

The above equations are second order differential equations with constant coefficients and the expressions are given by

$$\phi_{s1}(x) = A \exp(n * x) + B * \exp(-n * x) - p_1 \quad \text{for } 0 \leq x \leq L_1, 0 \leq y \leq t_{si} \quad (3.21)$$

$$\phi_{s2}(x) = C * \exp(n * (x - L_1)) + D * \exp(-n * (x - L_1)) - p_2 \quad \text{for } L_1 \leq x \leq L, 0 \leq y \leq t_{si} \quad (3.22)$$

Where

$$n = \sqrt{\alpha} \quad p_1 = \frac{\beta_1}{\alpha} \quad p_2 = \frac{\beta_2}{\alpha}$$

$$A = (V_{bi} * (1 - \exp(-n * L)) + V_{ds} + (p_1 - p_2) * \cosh(n * L_2) + p_2 - p_1 * \exp(-n * L)) * \exp(-n * L) / (1 - \exp(-2 * n * L))$$

$$B = (V_{bi} * (\exp(n * L) - 1) + p_1 * \exp(n * L) - V_{ds} - p_2 + (p_2 - p_1) * \cosh(n * L_2)) * \exp(-n * L) / (1 - \exp(-2 * n * L))$$

$$C = A * \exp(n * L_1) + (p_2 - p_1) / 2$$

$$D = B * \exp(-n * L_1) + (p_2 - p_1) / 2$$

3.3.2 Electric Field Formulation

Electric field horizontal component under metal gates $M1/M2$ can be calculated by differentiating the potential with respect to x .

$$E_1(x) = A n \exp(nx) - B n \exp(-nx) \quad (3.23)$$

$$E_2(x) = C n \exp(n(x - L_1)) - D n \exp(-n(x - L_1)) \quad (3.24)$$

The minimum potential of front channel can be expressed as:

$$x_{\min} = \frac{1}{2n} \ln \left(\frac{B}{A} \right) \quad (3.25)$$

$$\phi_{s,\min} = 2\sqrt{AB} - p_1 \quad (3.26)$$

3.3.3 Threshold Voltage Formulation

The threshold voltage (V_{th}) of the un-strained device can be found as follows [12]:

$$\phi_{s,\min} = \phi_{th} = 2\phi_{f,si} \quad (3.27)$$

$$\phi_f = KT \ln \frac{N_a}{n_i} \quad (3.28)$$

Where K is the Boltzmann's constant, T is the temperature, $\phi_{f,si}$ is the difference between the Fermi potential and the intrinsic Fermi level in the bulk region, ϕ_{th} is the value of surface potential at which the volumetric inversion electron charge density in the Si device is equal to the body doping.

For strained-Si SOI MOSFET the threshold condition under the front gate is modified as [13]

$$\phi_{s,\min} = \phi_{th} = 2\phi_{f,si} + \Delta\phi_{s,si} \quad (3.29)$$

Where

$$\Delta\phi_{s,si} = -\frac{\Delta E_{g,s-Si}}{q} + V_T \ln \left(\frac{N_{V,si}}{N_{V,s-Si}} \right)$$

In the case of the DMG-FD-S-SOI structure, due to different metal $M1$ and $M2$ having different work function, the minimum surface potential is purely dependent on metal gate with the higher work function. So the threshold voltage is calculated as the value of V_{GS} at which the minimum surface potential $\phi_{s,\min}$ equals to ϕ_{th} . Hence, one can determine the value of threshold voltage as the value of V_{GS} by solving equation (30).

$$V_{th} = \frac{-\eta + \sqrt{\eta^2 - 4\sigma\xi}}{2\sigma} \quad (3.30)$$

Where

$$\gamma = \exp(-nL)$$

$$\sigma = \frac{1}{\gamma} + \gamma - 2 - \sinh^2(nL)$$

$$V_{bi1} = V_{bi,s-Si}(1 - \gamma) + V_{DS} - (u - v) \cosh(nL_2) - v + u\gamma$$

$$V_{bi2} = V_{bi,s-Si} \left(\frac{1}{\gamma} - 1 \right) - V_{DS} + (u - v) \cosh(nL_2) + v - \frac{u}{\gamma}$$

$$u = \frac{C_b}{C_f} V_{SUB}' - \frac{qN_A t_{si}}{C_f} - V_{FB1,s-Si}$$

$$v = \frac{C_b}{C_f} V_{SUB}' - \frac{qN_A t_{si}}{C_f} - V_{FB2,s-Si}$$

$$\xi = V_{bi1} V_{bi2} - \sinh^2(nL) (\phi_{th} - u)^2$$

$$\eta = V_{bi1} \left(-\frac{1}{\gamma} + 1 \right) + 2 \sinh^2(nL) (\phi_{th} - u) - V_{bi2} (1 - \gamma)$$

3.4 Results and Discussion

In this section, results obtained from theoretical models of the surface potential, electric field and threshold voltage are compared with the numerical simulation results for DMG-FD-S-SOI MOSFET. Fig. 2 demonstrate the surface potential curve along the channel length at various values of the drain voltage. Because of the presence of dual metal, the variation of channel potential under metal gate 1 (*M1*) with respect to drain voltage is quite small. The drain voltage is not absorbed under *M1* as it is absorbed by metal gate 2 (*M2*), hence the channel under *M1* is screened from the changes of drain potential. As a consequence, V_{DS} has only a small influence on drain current after saturation. Also due to the dual metal gate, the variation of channel potential minima with respect to drain voltage is quite small which minimizes the DIBL (Drain Induced Barrier Lowering) effect.

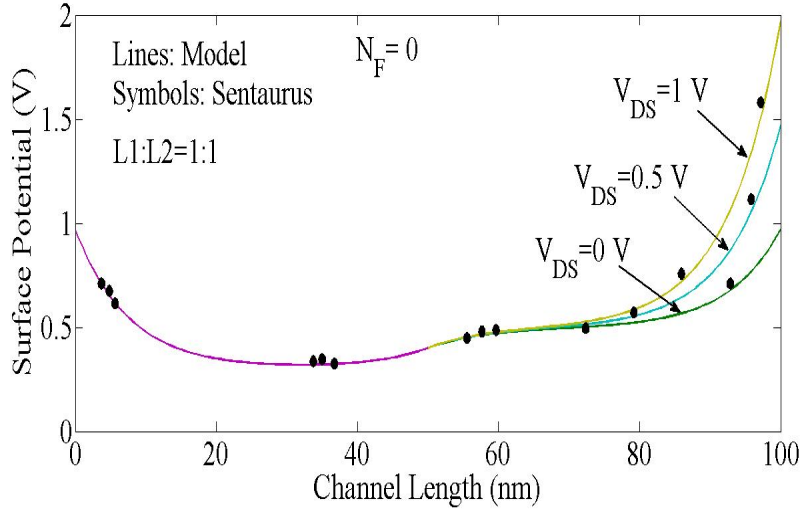


Fig.3.3. Variation of Surface Potential along the channel length for various Drain Voltages. Parameters used $X=0$, $\phi_{M1}=4.8$ eV, $\phi_{M2}=4.6$ eV, $N_A=1 \times 10^{16}$ cm $^{-3}$, $t_{Si}=10$ nm, $L=100$ nm, $t_{ox}=2$ nm, $V_{DS}=0.1$ V and $V_{GS}=0.1$ V.

In Fig. 3.3, the calculated and simulated values of surface potential are plotted against the horizontal distance x for $L = 100$ nm ($L1/L2 = 1:1$) at different values of effective Ge mole fraction (X) in the relaxed SiGe buffer. It can be seen that the potential barrier height is decreasing with increase in X . As the threshold voltage is calculated from the minimum surface potential and it is very important to choose the appropriate value of threshold voltage for a MOS device. The device having high threshold voltage is slower. Similarly, device having low threshold voltage have more leakage current. So, for our convenience from the Fig. 3, the middle one is considered i.e., $X = 0.2$ and the value is fixed to study the effect of other MOS parameters on surface potential for a DMG-FD-S-SOI MOSFET.

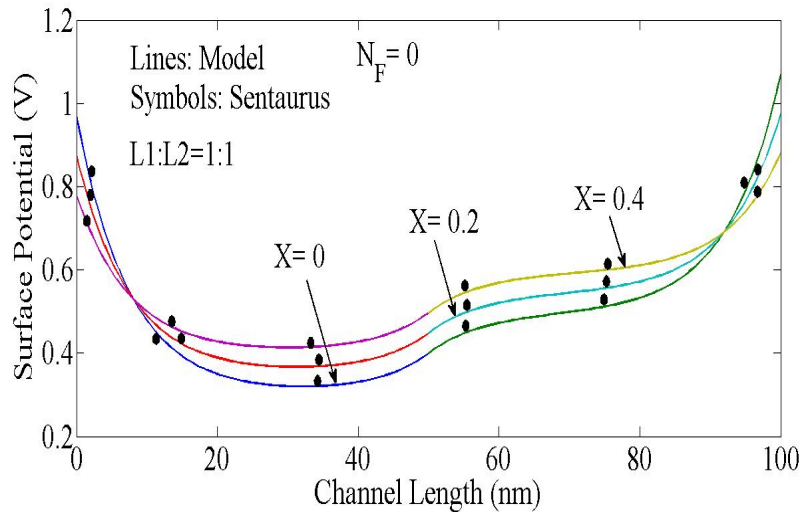


Fig.3.4. Variation of Surface Potential along the channel length for different Ge mole fraction (X). Parameters used $\phi_{M1}=4.8$ eV, $\phi_{M2}=4.6$ eV, $N_A=1 \times 10^{16}$ cm $^{-3}$, $t_{Si}=10$ nm, $L=100$ nm, $t_{ox}=2$ nm, $V_{DS}=0.1$ V and $V_{GS}=0.1$ V.

Fig. (3.5) shows the curve of surface potential of DMG-FD-S-SOI MOSFET for different gate length ratios ($L1/L2= 1:2, 1:1, 2:1$) against the horizontal distance x along the channel. The step profile due to DMG in the surface potential enhances the carrier transport efficiency from source to drain. From the figure it is observed that as the ratio of $M2$ increases, the minimum channel potential increases leads to a decrease in the barrier height and also the minimum potential shifted towards source side. So, we can say that the device having equal ratio of $M1$ and $M2$ will be the optimum one in terms of barrier height and V_{DS} immunity.

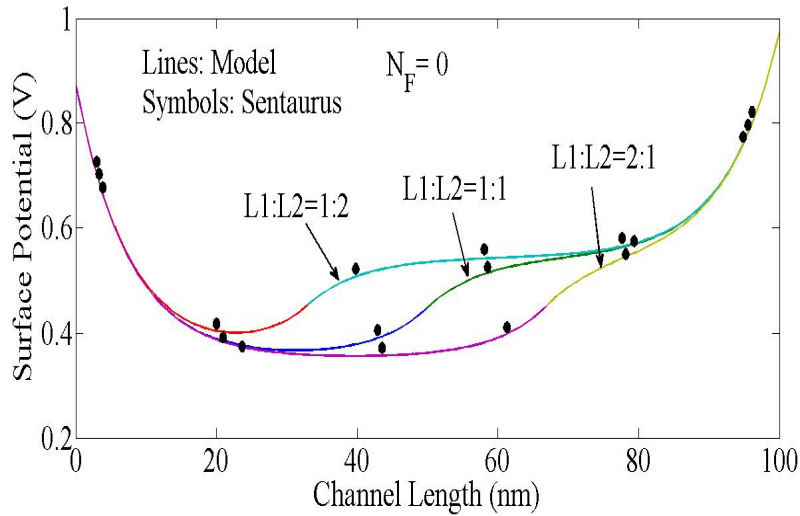


Fig.3.5. Variation of Surface Potential along the channel length for different gate length ratios ($L1/L2=1:2, 1:1, 2:1$). Parameters used $X=0.2$, $\phi_{M1}= 4.8$ eV, $\phi_{M2}= 4.6$ eV, $N_A=1 \times 10^{16} \text{ cm}^{-3}$, $t_{Si}=10$ nm, $L=100$ nm, $t_{ox}=2$ nm, $V_{DS}=0.1$ V and $V_{GS}=0.1$ V.

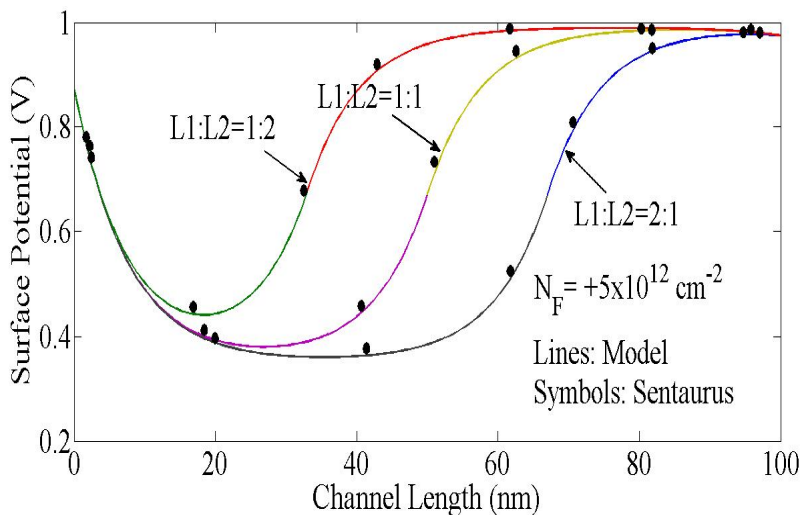


Fig.3.6. Variation of Surface Potential along the channel length considering positive interface charge for different gate length ratios ($L1/L2=1:2, 1:1, 2:1$). Parameters used $X=0.2$, $N_F= +5 \times 10^{12} \text{ cm}^{-2}$, $\phi_{M1}= 4.8$ eV, $\phi_{M2}= 4.6$ eV, $N_A=1 \times 10^{16} \text{ cm}^{-3}$, $t_{Si}=10$ nm, $L=100$ nm, $t_{ox}=2$ nm, $V_{DS}=0.1$ V and $V_{GS}=0.1$ V.

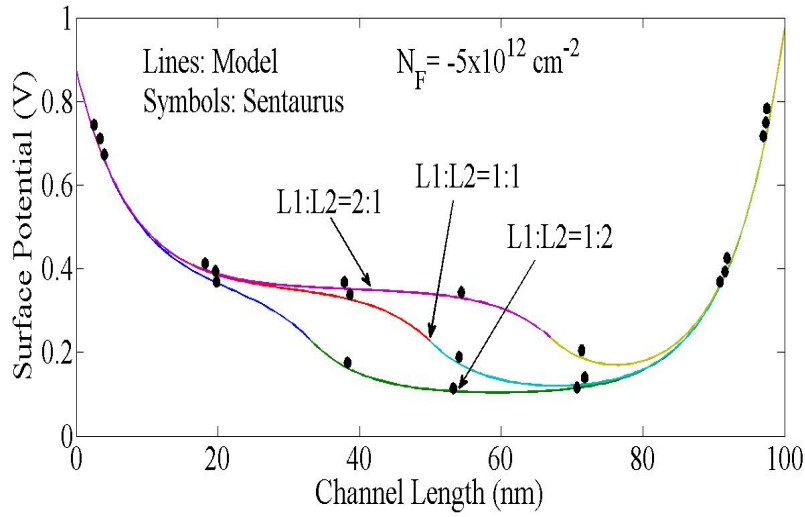


Fig.3.7. Variation of Surface Potential along the channel length considering negative interface charge for different gate length ratios ($L1/L2=1:2$, $1:1$, $2:1$). Parameters used $X=0.2$, $N_F= -5 \times 10^{12} \text{ cm}^{-2}$, $\phi_{M1}= 4.8 \text{ eV}$, $\phi_{M2}= 4.6 \text{ eV}$, $N_A=1 \times 10^{16} \text{ cm}^{-3}$, $t_{Si}=10 \text{ nm}$, $L=100 \text{ nm}$, $t_{ox}=2 \text{ nm}$, $V_{DS}=0.1 \text{ V}$ and $V_{GS}=0.1 \text{ V}$.

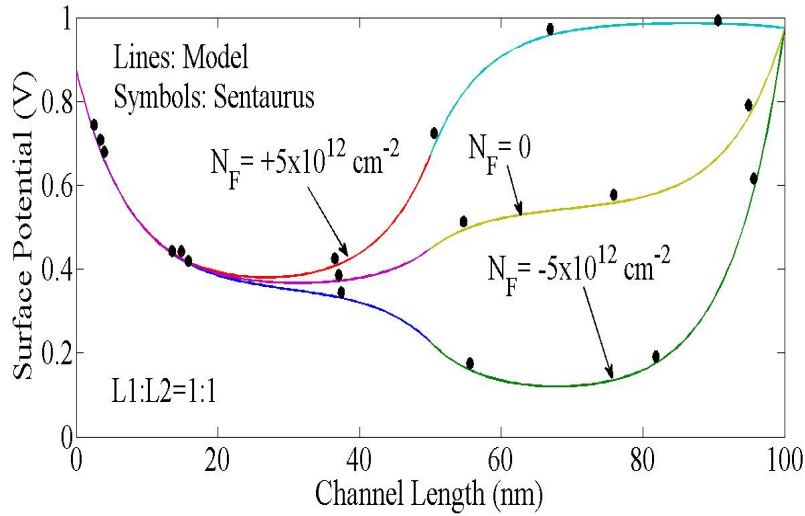


Fig.3.8. Surface Potential variation along the channel length for interface charge variations (in magnitude and polarity). Parameters used $X=0.2$, $\phi_{M1}= 4.8 \text{ eV}$, $\phi_{M2}= 4.6 \text{ eV}$, $N_A=1 \times 10^{16} \text{ cm}^{-3}$, $t_{Si}=10 \text{ nm}$, $L=100 \text{ nm}$, $t_{ox}=2 \text{ nm}$, $V_{DS}=0.1 \text{ V}$ and $V_{GS}=0.1 \text{ V}$.

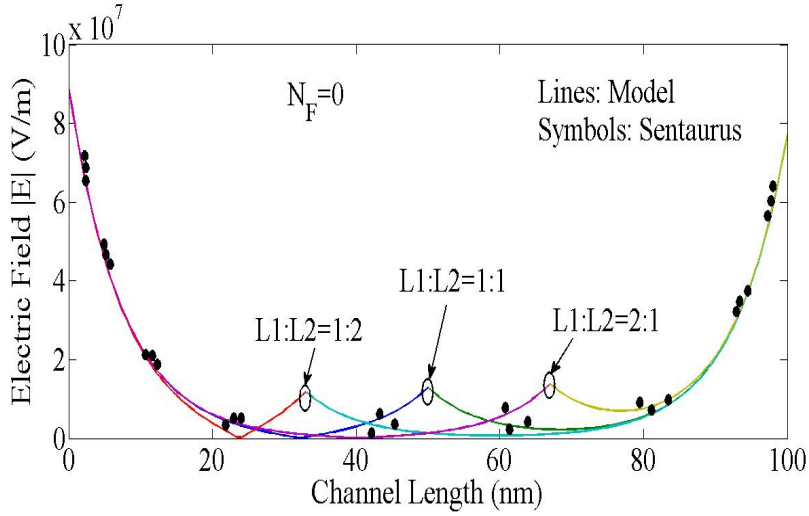


Fig.3.9. Electric Field variation along the channel length for different gate length ratios ($L1/L2=1:2$, $1:1$, $2:1$). Parameters used $X=0.2$, $\phi_{M1}=4.8\text{ eV}$, $\phi_{M2}=4.6\text{ eV}$, $N_A=1 \times 10^{16}\text{ cm}^{-3}$, $t_{Si}=10\text{ nm}$, $L=100\text{ nm}$, $t_{ox}=2\text{ nm}$, $V_{DS}=0.1\text{ V}$ and $V_{GS}=0.1\text{ V}$.

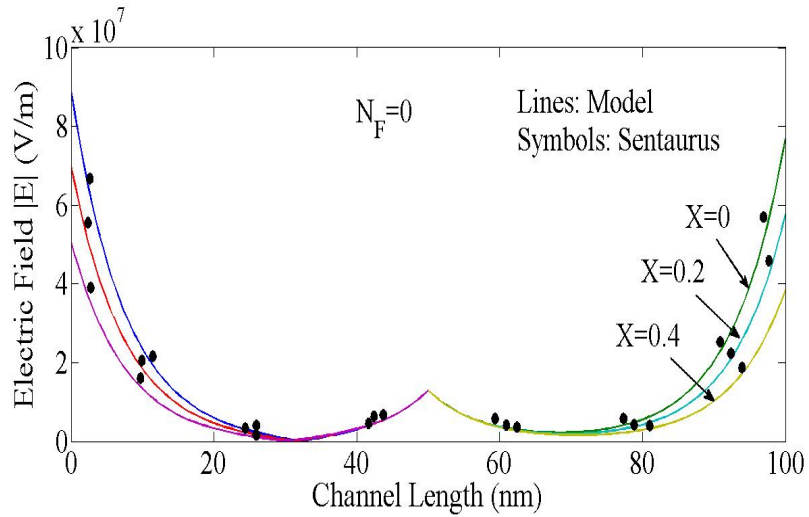


Fig.3.10. Variation of Electric Field along the channel length for different Ge mole fraction (X). Parameters used $\phi_{M1}=4.8\text{ eV}$, $\phi_{M2}=4.6\text{ eV}$, $N_A=1 \times 10^{16}\text{ cm}^{-3}$, $t_{Si}=10\text{ nm}$, $L=100\text{ nm}$, $t_{ox}=2\text{ nm}$, $V_{DS}=0.1\text{ V}$ and $V_{GS}=0.1\text{ V}$.

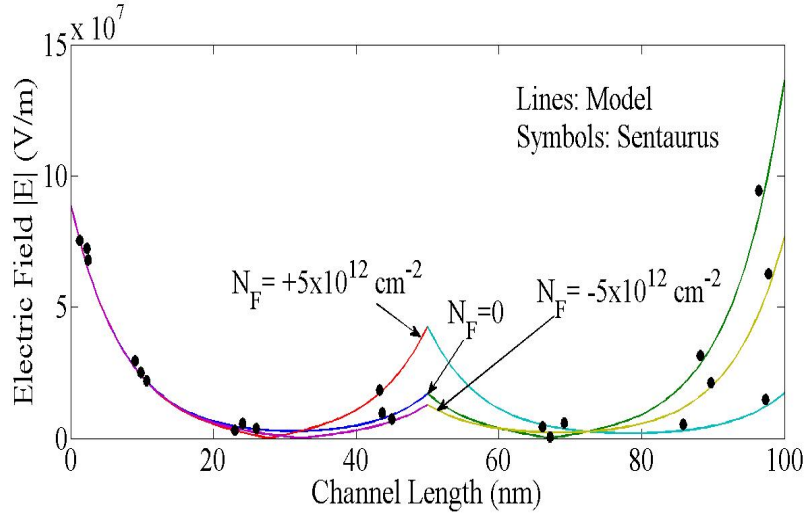


Fig 3.11. Electric Field variation along the channel length for interface charge variations (in magnitude and polarity). Parameters used $X=0.2$, $\phi_{M1}=4.8$ eV, $\phi_{M2}=4.6$ eV, $N_A=1 \times 10^{16} \text{ cm}^{-3}$, $t_{Si}=10$ nm, $L=100$ nm, $t_{ox}=2$ nm, $V_{DS}=0.1$ V and $V_{GS}=0.1$ V.

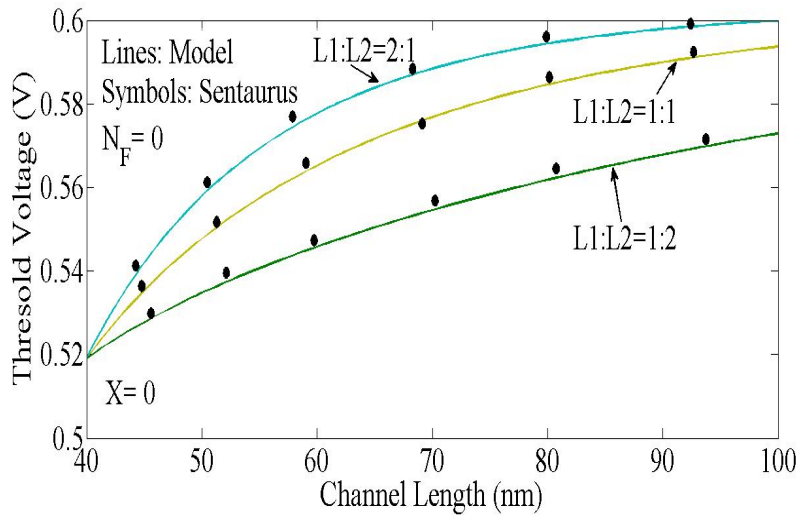


Fig 3.12. Threshold Voltage variation along the channel length for different gate length ratios ($L1/L2=1:2$, $1:1$, $2:1$). Parameters used $X=0.2$, $\phi_{M1}=4.8$ eV, $\phi_{M2}=4.6$ eV, $N_A=1 \times 10^{16} \text{ cm}^{-3}$, $t_{Si}=10$ nm, $L=100$ nm, $t_{ox}=2$ nm, $V_{DS}=0.1$ V and $V_{GS}=0.1$ V.

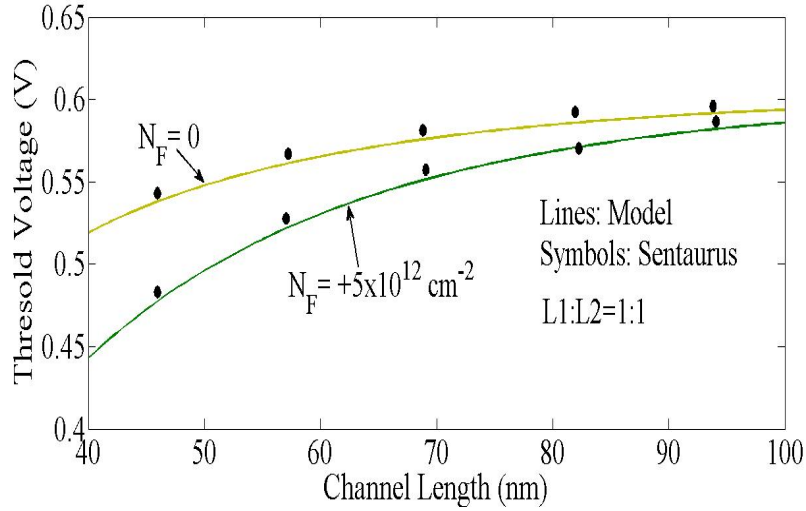


Fig .3.13. Threshold Voltage variation along the channel length for interface charge variations (in magnitude and polarity). Parameters used $X=0.2$, $\phi_{M1}= 4.8 \text{ eV}$, $\phi_{M2}= 4.6 \text{ eV}$, $N_A =1 \times 10^{16} \text{ cm}^{-3}$, $t_{Si}=10 \text{ nm}$, $L=100 \text{ nm}$, $t_{ox}=2 \text{ nm}$, $V_{DS}=0.1 \text{ V}$ and $V_{GS}=0.1 \text{ V}$.

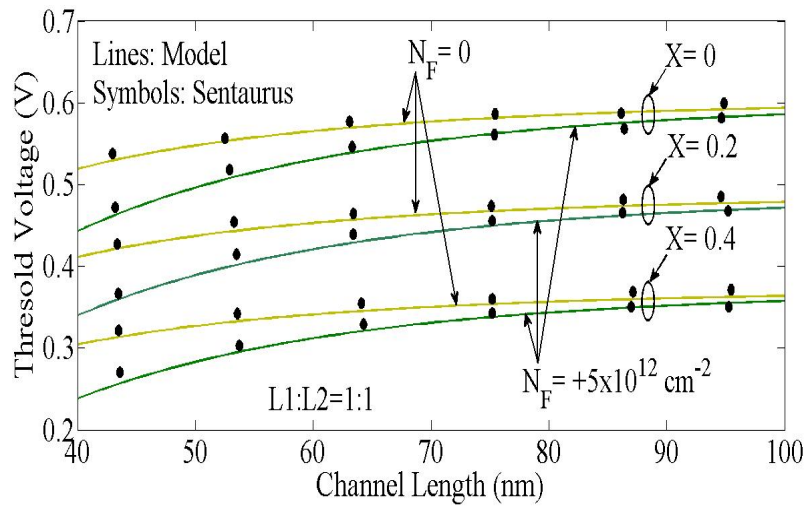


Fig 3.14. Threshold Voltage variation along the channel length with interface charge variations (in magnitude and polarity) for different Ge mole fraction (X). Parameters used $\phi_{M1}= 4.8 \text{ eV}$, $\phi_{M2}= 4.6 \text{ eV}$, $N_A =1 \times 10^{16} \text{ cm}^{-3}$, $t_{Si}=10 \text{ nm}$, $L=100 \text{ nm}$, $t_{ox}=2 \text{ nm}$, $V_{DS}=0.1 \text{ V}$ and $V_{GS}=0.1 \text{ V}$.

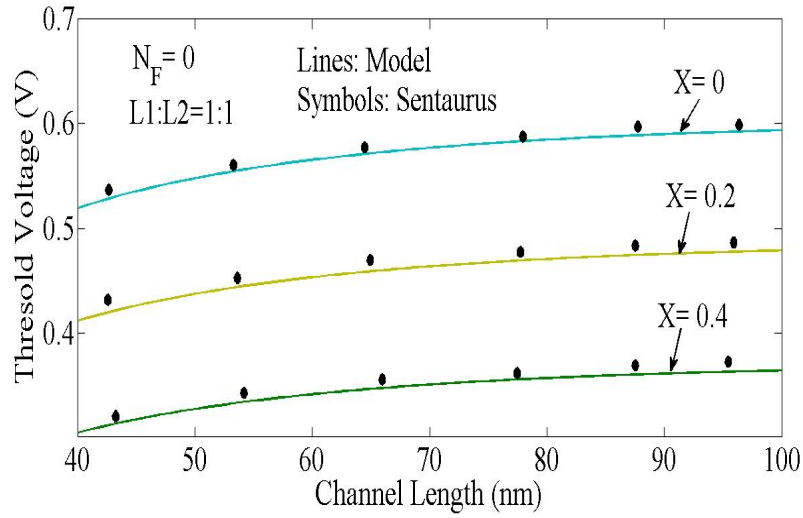


Fig 3.15. Variation of Threshold Voltage along the channel length for different Ge mole fraction (X). Parameters used $\phi_{M1}= 4.8$ eV, $\phi_{M2}= 4.6$ eV, $N_A =1 \times 10^{16}$ cm^{-3} , $t_{\text{Si}}=10$ nm, $L=100$ nm, $t_{\text{ox}}=2$ nm, $V_{\text{DS}}=0.1$ V and $V_{\text{GS}}=0.1$ V.

Chapter 4 Conclusion and future Work

4.1 Conclusions

- Continuous scaling in MOSFET devices degrade their performance as a result of leakage currents and short channel effects (SCEs) resulting from downscaling the device dimensions.
- To mitigate these short channel problems resulting from downscaling the device dimensions a device called Silicon-on-Insulator (SOI) MOSFET has been developed.
- The increase in strain i.e. equivalent Ge content, enhances the performance of SSOI MOSFETs due to improved trans-conductance and increase in the electron carrier mobility.
- However, as established by our results, there are still some detrimental side effects with increasing equivalent Ge content (more than 0.4) such as a roll-off in V_{th} , which may affect the device characteristics and performance.
- In this thesis, the analytical model for surface potential, electric field, and threshold voltage for a DMG-FD-S-SOI is formulated including the effects of interface charges. The interface charges are considered both in magnitude and polarity with an assumption that the charge distribution is uniform along the channel. Parabolic approximation method is used for solving the 2-D Poisson's equation to formulate the surface potential and further virtual cathode potential method is used for modelling the threshold voltage. An extensive analysis is carried out to study the effect of various parameters like Ge mole fraction, drain bias, gate length ratio variation, and interface charge variation on surface potential, electric field, and threshold voltage.
- From the result obtained from DMG-FD-S-SOI we can conclude that strained silicon up to some extent enhance the performance of the device.

4.2 Scope for Future Work

The research on carried on DMG-FD-S-SOI have shown results to reduce short channeling effect by using Double material gate, use of strain, effect of trapped charges, effect of high $-k$ material. The result shown in this thesis has been verified by simulation in SENTARURSTM and the results match with each other.

Some important direction in which this work can further be improved are

1. Use of Graded channel Gate stack structure
2. Use of Multi Gate (Double Gate, quadrature Gate, Gate All Around) structure.
3. The detailed AC analysis for RF applications of the optimized device DMG-FD-S-SOI MOSFET.
4. Possible fabrication of the different device structures considered.

4.3 List of Publication

1. M.R Kumar, K.P Pradhan, G.S. Pati, P.K.Sahu, S.K. Mohapatra, "An Accurate Analytical Threshold Voltage Model For Cylindrical Gate All Around (CGAA) MOSFET using Center Potential", Journal Of Computational Electronics, Springer(Communicated)
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