Analytical Modeling of Gate All Around (GAA) MOSFET in Nanoscale

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CERTIFICATE

This is to certify that the dissertation entitled ***"Analytical Modelling & Simulation Of Gate All Around (GAA) MOSFET in nanoscale "*** *submitted by* ***Mr. Madhu Raj Kumar*** *(Roll No.: 212EE1387), to the Department of Electrical Engineering, National Institute of Technology Rourkela, in partial fulfillment of the requirements for the award of the degree "****MASTER OF TECHNOLOGY" in Electrical Engineering (Electronic Systems & Communication)*** *is an authentic work carried out at Department of Electrical Engineering, National Institute of Technology, Rourkela by him under my supervision and guidance.*

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other University/ Institute for the award of any degree or diploma.

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CANDIDATE'S DECLARATION

I hereby declare that the work presented in this dissertation entitled ***"Analytical Modelling & Simulation Of Gate All Around (GAA) MOSFET in nanoscale",*** *is an authentic record of my own work carried out at Department of Electrical Engineering, National Institute of Technology, Rourkela as requirements for the award of degree of Master of Technology (M.Tech.) in Electrical Engineering (Electronic Systems & Communication), submitted in the National Institute of Technology, Rourkela for the session from June 2012 to June 2014 under supervision of* ***Prof. P.K Sahu****, Department of Electrical Engineering, National Institute of Technology, Rourkela.*

The matter embodied in the thesis has not been submitted to any other University/ Institute for the award of any degree or diploma.

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Dedicated
To
My Beloved
Family

Whose blessings, love and sacrifice brought me here up to ……….

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Abstract

The nano-scale devices face a major issue i.e. Short Channel Effects, as a result of which the performance of the devices degrade. To enhance the performance of such devices, the SCEs should be reduced.

This Thesis contributes to enhance the performance of nano-scaled Quadruple gate MOSFET by reducing the SCEs effects. In this work, an accurate analytical sub threshold models has been developed for an Undoped double gate MOSFET considering parabolic approximation of the channel. The Centre (axial) as well as the surface potential model is obtained by solving the 2-D Poisson's equation. Using two 2-D double gate MOSFETs and then using perimeter weighted sum method the center potential model of the Quadruple gate MOSFET has been developed. The developed Centre potential model is used further to develop the threshold voltage model. The Centre potential model was further applied to estimate the sub threshold drain current and the sub threshold swing of the device. An extensive analysis of the device parameters like the channel thickness, channel width, oxide thickness, channel length etc. on the sub threshold electrical parameters is demonstrated. This gives a highly accurate model which closely matches with the simulations. The models are verified by the simulations obtained from 3-D numerical device simulator Sentaurus from Synopsys.

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Chapter1

Introduction

1.1 Introduction

The revolution in the research of solid-state electronics in general and semiconductor device based electronic industry was started with the development of bipolar transistor, which is found one of the most revolutionary inventions of the 20th Century. In the past years, this invention has been showed an unprecedented impact on the development of the semiconductor science and technology [1]. The Bipolar transistor Shows delay nature when turn on and turn off and also Shows large base-storage times which limit it for high frequency switching application .So, the BJT has replaced by the CMOS technology in the design of digital integrated circuits. Therefore, in 1960, Kahng and Attalla proposed and fabricated one of the most important unipolar device which named as the metal-oxide-semiconductor field-effect transistor (MOSFET) [2]. The phrase "metal–oxide–semiconductor" is a reference to the physical structure of certain field-effect transistors, containing a silicon substrate on which an oxide layer is grown and an electrode of metal is placed on the top of oxide. Due to this gate voltage controllability, MOSFET is a transistor used for both digital and analog circuits. In MOSFETs, when a voltage applied on the gate electrode, some charge is induced and this induced charge make a channel between the two other contacts called Source and Drain. This is the device which took the leading role in the growth and development of the modern day's microprocessors and semiconductor memory.

The designing methodologies of modern ICs are established on the CMOS technology. The term "CMOS" refers to both a specific style of digital circuitry design, and the family of processes used to implement that circuitry on integrated circuits (chips). To design the digital circuits used in microprocessors, microcontrollers, Static RAM, and other digital logic circuits we have use CMOS circuit, an arrangement of p-type and n-type MOSFETs. For different analog circuits such as image sensors, data converters, and highly integrated transceivers which is used in analog communication technology, we also use CMOS technology. Typical the commercial

integrated circuits containing the CMOS composed of billions of MOS transistors of both n- and p- types MOSFETs on a rectangular piece of silicon of between 10 and 400 mm^2.

1.2 Motivation to the work

Due to the fast progress in the IC technology, ICs have consistently been migrating towards the smaller feature sizes for achieving the high packing density for reducing the cost per function along increasing functionality. However, the relentless demand for increasing more and more number of CMOS devices per unit area of an IC has forced the device dimensions to shrink from micrometer to the nanometer scale leading to several detrimental effects on the switching characteristics of the transistors. Although, the reduction in device dimensions during the change from one technology node to another is obtained by following certain scaling rules to minimize these effects, the severe degradation in the Subthreshold characteristics of CMOS devices in the nanometer scale has imposed a physical limit on further scaling of conventional MOS transistors. To continue with further scaling of ICs, it is urgently required to carry out research for the development and study of some alternative non-conventional CMOS devices such as ultra-thin body single and multiple-gate silicon-on-insulator (SOI) MOSFETs, Gate-All-Around (GAA) MOSFETs etc. [3].

Among all reported device architectures are facing few fabrication problems and also facing some mathematical problem when we find the analytical threshold voltage. Therefore, Due to these regions we have investigate a structure which is symmetrical in all respect as like width and height and hence quadruple gate MOSFET is found to be one of the most promising non-conventional CMOS devices for future generation IC technology []. The present dissertation deals with the modeling and simulation of quadruple gate MOSFETs for having the exact idea about this planner MOS structure.

1.3 MOSFET Scaling

The Semiconductor Industry Association (SIA) of the United States of America, a nonprofit organization that assesses the technology requirements of the future semiconductor industry and publishes the International Technology Roadmap for Semiconductors (ITRS), has recently stated

that it could be a “difficult task” to progress with CMOS beyond the 22nm technology generation [5]. The main reason behind the above prediction is the ultimate scaling limit of the conventional MOSFETs which has already been touched. Further scaling will result in excessive short-channel effects (SCEs) beyond the tolerable limit thereby increasing the standby power dissipation and deteriorating the switching characteristics of the CMOS transistors. Collectively, the variation in the threshold voltage and the variation in Subthreshold current is defined as a short-channel effects (SCEs). Higher SCE causes lower ON-to-OFF current ratio of the transistor which in turn imposes severe trade-off between circuit speed and standby power. Therefore, the suppression of the SCEs up to the acceptable level is of utmost importance of the MOSFET scaling to sustain the IC technology scaling trend.

The scaling approach of MOS transistor was first proposed by Dennard and his fellow workers in 1972 [6]. The work was later modified by Broers *et al*. and Dennard *et al.* in 1973 and 1974 respectively [7]. Their proposed scaling theory stated that, to avoid the short-channel effects of a transistor during scaling from larger to shorter geometrical configuration of the transistor, both the lateral and vertical dimensions and the supply voltages of the transistor are required to be scaled (down) by a constant scaling factor whereas the substrate doping concentration has to be scaled up (increased) by the same factor. The scaling of the gate length relies on the improvement of the resolution of lithography. The vertical dimension scaling includes thinning of the gate-oxide and making shallow-source/drain junctions. The work of Dennard *et al.* served as the basic reference to the semiconductor industry for almost two and half decades. However, scaling rules have become more and more sophisticated with the advancements in the MOSFET technology [8-9].

In conventional CMOS technologies, the suppression of SCEs can be obtained most effectively by (i) reducing the gate-oxide thickness, and (ii) increasing the channel doping concentration. The former is aimed to increase the gate capacitance thereby enhancing the electrostatic potential control of the gate over the entire channel region. The latter is desired to minimize the depletion depths of the source-channel and drain-channel junctions. It prevents the junction electric fields from penetrating too much into the channel and forming an undesired leakage path relatively at larger distance from the gate [10]. While these measures for controlling SCEs have been found successful for many technology generations in the past, they are expected to become less effective in the near future. Due to relentless scaling, as the bulk MOSFETs enter into the sub-

100 nm regime the gate-oxide thickness required for adequate SCEs suppression reaches at around 1.0-2.0 nm and below. Such a smaller gate-oxide thickness may lead to severe increase in the direct tunneling current through it thereby increasing the stand-by power consumption of the device [11].To reduce the leakage current, a potential solution under active investigation is the use of such dielectric material for the gate dielectric which have high dielectric strength, material is called high-k materials [12]. Further, the increased doping in the channel due to continuous scaling may severely reduce the speed of the device [ITRS (2004)]. Thus, in order to maintain the scaling trend of IC technology, it is of an utmost importance to study alternative non-classical CMOS device structures like multi gate MOSFETs, which are expected to push further the CMOS scaling beyond the limits foreseen by the conventional planar device structures as suggested by researchers in the ITRS-2007 [ITRS (2007)].

1.4 Non-Classical CMOS

It is previously discoursed in the earlier section that even high-k material is used with SiO_2 in place of simple SiO_2 gate, metal electrodes, novel annealing schemes, and the other material and processing type potential solutions[13], scaling will result in growing difficulties for planar bulk MOSFETs in meeting all of the transistor desires for future CMOS technology bulge. Key encounters are estimated to include trouble in controlling short-channel effects,negative influence of the high channel doping necessary for very small devices, struggle in procurement adequate ON-state drive current for transistors with very small gate-length, as well as other matters are also discussed. Alternatively, a number of non-classical MOSFETs devices with double-gate MOSFETs, cylindrical gate all around MOSFETs and quadruple gate MOSFET are being considered .In this section, we present brief metaphors about some important non-classical MOSFETs stated above.

1.5 Quadruple gate MOSFETs

The ultra-thin body SOI MOSFETs can be fabricated in different forms it may be a single or double gate (DG), a cylindrical MOSFET or quadruple gate MOSFET. One kind of quadruple gate MOSFET is alike to the SOI single-gate transistor, in addition of bottom, front and back

gate aligned with the front gate opposite side of the buried oxide (BOX). On the basis of application of gate voltages, quadruple MOSFETs may be grouped as symmetric, asymmetric MOSFETs. A symmetric Quadruple gate MOSFET results when all surrounded gates have the same metal work function, same thickness of oxide and a single input voltage is applied to all side of the gates as shown in the fig.(1).

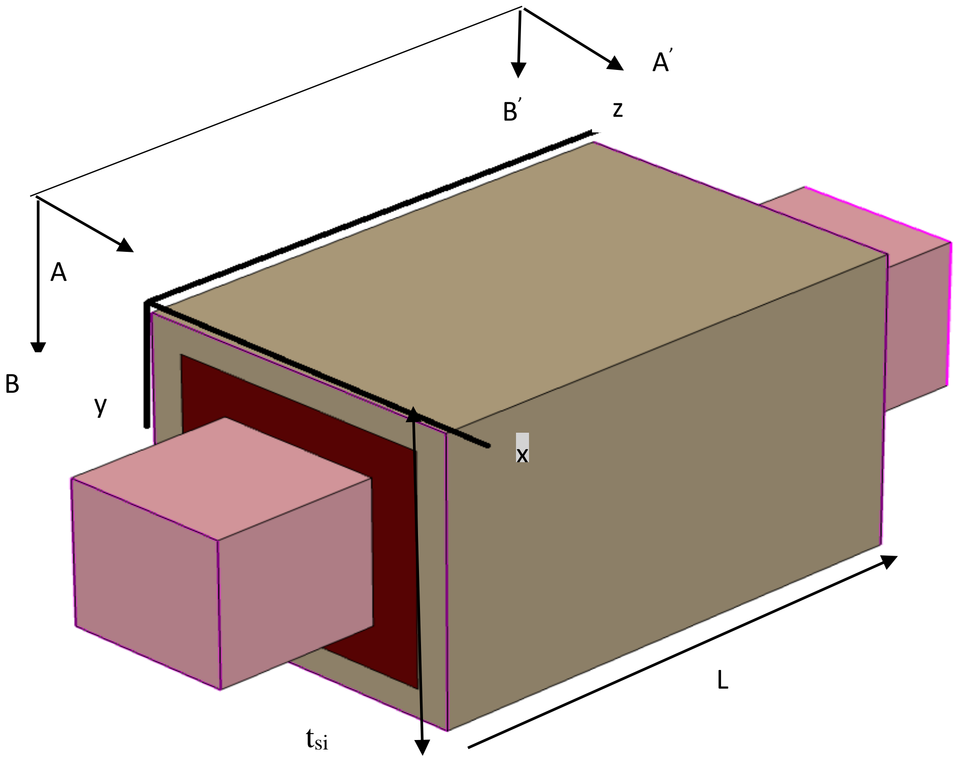

Figure 1 : Schematic diagram of Quadruple gate MOSFETs

An asymmetric Quadruple MOSFET either has synchronized but different input voltages to all side of quadruple gates, or applied the same input voltage to all gates that have distinct work functions. In short, the term symmetric and asymmetric principally reflect the appearance or nonappearance of symmetry of the electrostatic potential distributions at the $Si\text{-}SiO_2$ interfaces of the channel. Quadruple gate MOS devices have been presented with Undoped and doped channel

for different applications. Undoped channel Quadruple MOSFET is suitable for digital applications. Doped channel Quadruple MOSFETs have found places in varieties of applications like base-band analog applications, memory applications [14] etc. The DG MOSFETs are considered to be one of the most prominent non-classical CMOS devices for future generation Nano-scale IC technology.

1.6 Advantages of Quadruple gate MOSFETs

(a) Better scalability- The quadruple-gate MOSFET has higher scalability than the double-gate MOSFETs (i.e., better control of SCE).The reason behind that the surrounding gate creates an electrical sheltering action for lateral electrical fields creating due to the charges in the source and drain. The superior scalability of the device could make the quadruple gate MOSFET suitable for future generation CMOS technology with gate-length scaled below 25 nm.

(b) Better switching characteristics- An ideal Subthreshold swing of ~60mV/Decade could be expected in a Quadruple gate MOSFET. This may provide higher ON-to-OFF current ratio than that of the bulk MOSFET thereby providing better switching characteristics.

(c) Higher drive current- Since the current flow across all the top , bottom, front and back surface of the silicon body (not only just from the top edge as well as bottom edge in the ultra-thin body SOI DG MOSFET), the ON-state drive current can practically be double of that of the double-gate device.

(d) Higher trans-conductance and linearity- Higher trans-conductance and greater linearity of quadruple gate MOSFETs can be achieved by increasing the doping level in the channel region of device. It may be mentioned that the doped quadruple gate MOSFETs are important for many analog and RF applications [15].

1.7 Brief Review of Analytical Model of DG MOSFETs

1.7.1 Threshold Voltage Models

It is discussed in previous section that the Quadruple gate MOSFETs have all the potentialities to become alternative CMOS structures to meet the scaling challenges for designing future generation VLSI/ULSI based circuits and systems. Now, we discussed modeling of threshold voltage. In general, the minimum gate voltage required for generating an inversion layer in the channel near the interface of Si/SIO2, a MOS DEVICE with a mobile carrier concentration in the inversion region same as that of the carrier concentration in the neutral region of the bulk substrate of the device is called the threshold voltage of a MOSFET. The role of the threshold voltage is very important for the designing of VLSI circuits and systems targeting low-voltage, low-power and high-speed application [16].

To derive an analytical expression of surface potential of Undoped long-channel double gate MOSFETs, Udit Monga using conformal mapping techniques [17]. A physical drift-current based threshold voltage model of Undoped long-channel DG MOSFETs was proposed by Shih *et al.*[18] the channel potential was obtained by solving the 1-D poison's equation by considering only one type of mobile carriers and then the drift and diffusion currents were formulated separately to derive the analytical expressions of the threshold voltage.

Recently, Tiwari *et al.* reported a doping dependent threshold voltage model for the short-channel DG MOSFETs with a uniform channel doping. The sensitivity of the threshold voltage to acceptor doping and other device parameters was disused in this paper [19].

1.7.2 Subthreshold Swing Models

Subthreshold swing is one of the key parameters of the CMOS devices to determine their switching characteristics. It can be defined as the gate voltage required for changing the current

by one decade. Since the Subthreshold swing has significant implications in the CMOS device scaling, we present a brief review of the various modeling issues of the Sub-threshold swing characteristics of DG MOSFETs in the following.

The previous literatures have reported many numbers of analytical models dealing with the Sub-threshold swing of DG MOSFETs. Suzuki et al [20] suggested a scaling theory for lightly DG MOSFETs where they demonstrated that the punch through current in the devices would dominantly flow along the center of the channel of Undoped/lightly doped DG MOS devices. They observed that the devices would maintain an ideal Subthreshold swing (S) –factor even for very short gate length devices. Bhattacherjee *et al*. [Bhattacherjee *et al*.(2008)] proposed a subthreshold swing model of uniformly doped short-channel DG MOS device but did not throw any light on the doping dependency characteristics of the subthreshold swing parameter .They only show that the subthreshold swing of the double gate MOSFETs could be improved by decreasing the body thickness, (t_{si}) and gate oxide thickness,(t_{ox}).

1.7.3 Subthreshold Current Models

The Subthreshold current of any CMOS device acting as a significant role in describing the static power dissipation of the transistor acting as a switch. Thus, an accurate model of the Subthreshold current of Quadruple gate MOSFETs is an utmost concern of many researchers for the optimization of the power dissipation in Quadruple gate MOSFET based VLSI/ULSI circuits**.** The suggested model was based on the postulation that the drain current density of the device would flow principally in the lateral direction (from source to drain) and the electron quasi-Fermi potential would be constant in the direction of the thickness as well as in the direction of width . Besides constant mobility model, both the drift and diffusion current components of the device operating in the Subthreshold regime were included in the proposed model [21].

Qureshi *et al*. modeled the subthreshold current of DG MOSFETs. The Poisson's equation was solved by applying the Gauss's law around the silicon channel [22]. However, the model failed to be useful from compacting modeling point of view of the short-channel DG MOS devicez as it included a body-thickness-dependent parameter[23].

To assess the behavior of short-channel DG MOSFETs in the subthreshold regime, Tiwari *et al*. presented a subthreshold current model for uniformly doped devices. The parabolic potential approximation was used to obtain the channel potential of the device by the solving the 2-D Poisson's equation. The diffusion current equation was implemented to model the subthreshold current of the device [24] .The model also considered the effect of volume inversion in the relatively low doped DG MOS device. They expressed the subthreshold current as a function of various device parameters [25].

1.8 Scope of the Dissertation

The objective of this dissertation is to present a detailed analytical modeling and Numerical simulation based study of the Subthreshold characteristics of some short-channel Quadruple gate MOSFETs. We have modeled the device with the constant doping profile in channel. The analytical model is developed by using the parabolic approximation technique. This dissertation includes **Five Chapters** including the present one titled "Introduction", in which, some general aspects of IC technology, CMOS scaling and non-classical CMOS device structures have been briefly introduced. It also presents the schematic structure of Quadruple gate MOSFETs, which is used for modeling. For modeling, we used two symmetrical double gate MOSFETs ,in place of actual Quadruple gate MOSFETs, and individual double gate MOSFET is modeled and then by using weighted parameter sum method we have find the actual model of quadruple gate MOSFETs. The contents of the remaining chapters of this Dissertation are outlined as follows:

Chapter-2 presents an analytical 2-D channel potential and threshold voltage model for Undoped DG MOSFETs. The surface potential model was developed followed by the threshold voltage. To show the validity of the presented model a 2-D device simulation was done with the help of commercially available sentaurus.

Chapter-3 deals with the analytical modeling and simulation of the Sub-threshold current of symmetric DG MOSFETs as well as sub-threshold slope of DG MOSFETs with constant substrate doping. Subthreshold current expression is derived by assuming the diffusion phenomenon. Subthreshold Swing model is derived by using the effective conduction path effect concept of the quadruple MOS devices. The effects of channel thickness and channel width on the Sub-threshold current as well as Subthreshold swing are investigated in details. All the results are compared with the Numerical simulation results obtained by commercially Sentaurus.

Chapter-4 deals with the analytical modeling and simulation of threshold voltage, Sub-threshold current and Sub-threshold swing of short-channel symmetric Quadruple-gate MOSFETs with constant substrate doping. For modeling, we used two symmetrical double gate MOSFETs ,in place of actual Quadruple gate MOSFETs, and individual double gate MOSFET is modeled and then by using weighted parameter sum method we have find the actual model of quadruple gate MOSFETs.The effects of the doping and other device parameters like channel thickness and channel width on the sub-threshold current and sub-threshold swing are investigated in details. All the results obtained from analytical model are compared with the Numerical simulation results obtained by commercially Sentaurus

Chapter-5 includes the summary and conclusions of the thesis. The major findings of the present study are summarized in this chapter. Finally, a brief discussion on the future scope of research in related areas considered in the dissertation is also presented in this chapter.

Chapter 2

Modeling and Simulation of Channel Potential &Threshold Voltage Characteristics

2.1 **Introduction**

In Chapter-1, various features and advantages of uniformly doped Quadruple gate MOSFETs are highlighted. The present chapter deals with the 2-D modeling and simulation of the potential distribution and threshold voltage of ion-implemented quadruple gate MOSFETs. The doping profile of the channel is assumed to be constant .To simplify the mathematics the 3-D Quadruple gate device, device can be replaced with the 2-D equivalent symmetric double gate structure. For ignoring the coupling effects we take the channel length/channel width and channel length /channel thickness is larger than 2 which falls within the restriction required to obtain realistic and operational MOSFET. For obtain the Threshold voltage of the quadruple gate device .We use a method known as weighted parametric sum method. In this method the 3D device Structure is divided into two 2-D symmetric structure. For individual 2-D structure we find the threshold voltage individually and by using the above method we can get the threshold Voltage of 3-D structure device. In this chapter we have find the threshold voltage for the 3-D structure as shown in the figure (1).

2.2 **Channel Potential Derivation of the double gate MOSFET which is obtained by cutline (AA’)**

The schematic structure of Undoped Quadruple gate MOSFET device used for the modeling and Sentaurus simulation is shown in Fig. (1). where, L, t_{si} , t_h , t_{oxt} , t_{oxb} t_{oxf} and t_{oxb} are the gate-length, thickness of channel, channel width, top gate-oxide thickness, bottom gate-oxide thickness, front gate-oxide thickness and back gate-oxide thickness respectively. It should be noted that subscripts f and b are used for the front and back surface related parameters, respectively. The x- axes of the 2D structure are considered to be along the channel thickness and z-axes along the channel length which is shown in the figure (2). For the distinction of the two gates, we use the nomenclatures of the gates as top-gate and bottom-gate of the device.

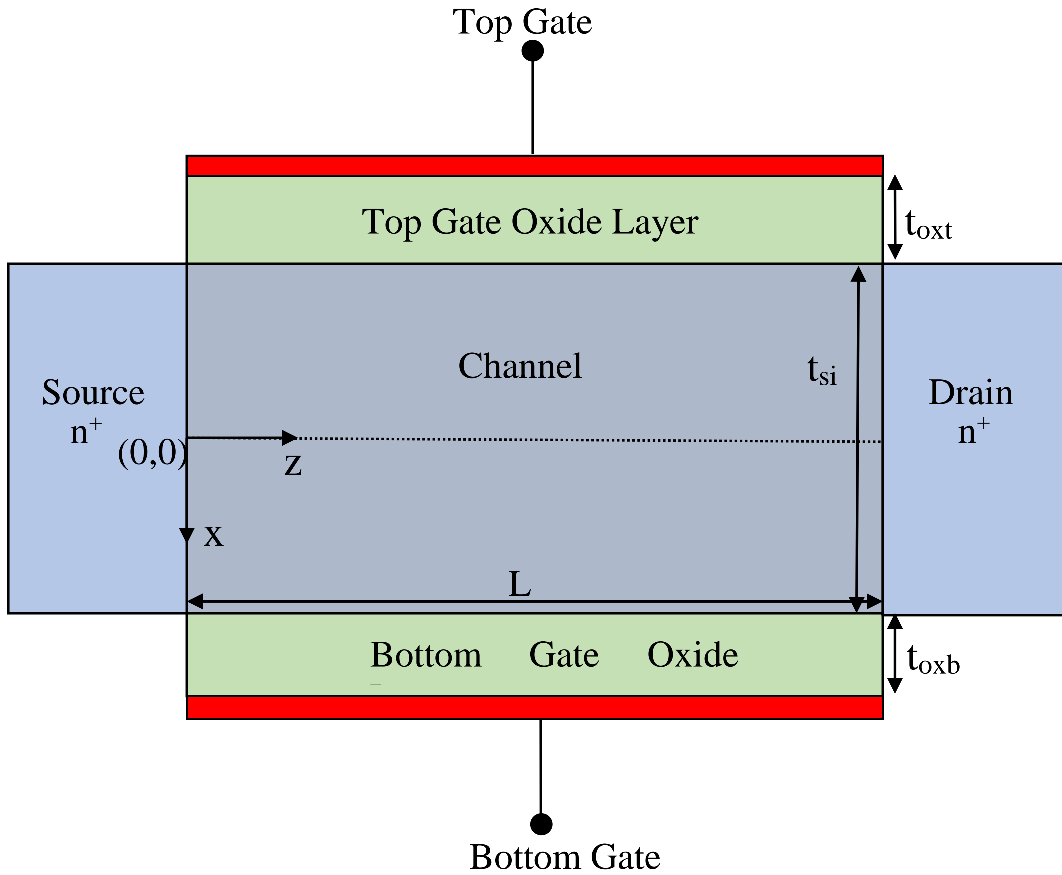

Figure 2: Schematic structure of the DG-MOSFET used in modeling and simulation

The channel potential distribution function is $\phi(x,z)$, According to the Poisson equation, the channel potential is written as eq. (2.1)

$$\frac{\partial^2\varphi(x,z)}{\partial x^2}+\frac{\partial^2\varphi(x,z)}{\partial z^2}=\frac{qN_a}{\varepsilon_{si}} \tag{2.1}$$

The Poisson equation expressed by eq. (2.1) can be solved by using the following boundary conditions:

$$\phi(x,z)\big|_{x=0}=\phi_0(x) \tag{2.2}$$

$$\left.\frac{\partial\phi(x,z)}{\partial x}\right|_{x=0}=0 \tag{2.3}$$

$$\frac{\varepsilon_{ox}}{t_{ox}}\left(V_{gs}-V_{fb}-\phi\left(-\frac{t_{si}}{2},z\right)\right)=-\varepsilon_{si}\left.\frac{\partial\phi(x,z)}{\partial x}\right|_{x=-\frac{t_{si}}{2}} \tag{2.4}$$

$$\frac{\varepsilon_{ox}}{t_{ox}}\left(V_{gs}-V_{fb}-\phi\left(\frac{t_{si}}{2},z\right)\right)=\varepsilon_{si}\left.\frac{\partial\phi(x,z)}{\partial x}\right|_{x=\frac{t_{si}}{2}} \tag{2.5}$$

$$\phi(x,0)=V_{bi} \tag{2.6}$$

$$\phi(x,L)=V_{bi}+V_{ds} \tag{2.7}$$

$$\phi(x,z)\big|_{x=-\frac{t_{si}}{2}}=\phi_{fg}(z) \tag{2.8}$$

$$\phi(x,z)\big|_{x=\frac{t_{si}}{2}}=\phi_{bg}(z) \tag{2.9}$$

Where, $\phi_0(x)$ is considered as the center potential along the channel, the permittivity of silicon is ε_{si}, the permittivity of the SiO_2. is $\varepsilon_{ox}.\phi_{tg}(x)$, Is the top surface potential, $\phi_{bg}(z)$ is the bottom surface potential, $V_{bi}=\frac{kT}{q}\ln\frac{N_{S(D)}N_a}{n_i^2}$ is potential built between source and drain, $N_{S(D)}$ is constant doping profile of n^+ source (drain) region, V_{DS} is biasing voltage applied across source-drain and $V_{fbf(fbb)}=\phi_{mf(mb)}-\left(\chi_s+\frac{E_g}{2}+\frac{kT}{q}\ln\left(\frac{N_{f(b)}}{n_i}\right)\right)$ is the flat-band voltage of the top (bottom) surface. where $\phi_{mf(mb)}$ is the top (bottom) metal work function, χ_s is electron affinity of

silicon, E_g is the energy band gap of the silicon material,T is absolute temperature ,q is the electron charge , k is Boltzmann constant and N_a is the channel doping concentration.

The 2-D channel potential function can be approximated as parabolic in nature and expressed as:

$$\phi(x,z) = c_0(z) + c_1(z)x + c_2(z)x^2 \tag{2.10}$$

Where, $c_0(z)$, $c_1(z)$ and $c_2(z)$ are the arbitrary function of z which are getting by applying the boundary condition in the above Poisson equation.

From Equation (2.2) and Equation (2.10), we get

$$c_0(z) = \phi_0(z) \tag{2.11}$$

Putting the value of Φ(x, z) from equation (2.10) to equation (2.4) and (2.5) and after solving we get the value of C_1 (z)

$$c_1(z) = \frac{\varepsilon_{ox}\left(V_{fbt} - V_{fbb}\right)}{t_{ox}\left(\varepsilon_{si} + \frac{\varepsilon_{ox}t_{si}}{2t_{ox}}\right)} \tag{2.12}$$

For Symmetrical DG MOSFETs,

$$c_1(z) = 0 \tag{2.13}$$

Further, by using the above Equation’s. (2.10)- (3.13) in Eq. (2.4), we get,

$$c_2(z) = \frac{V_{gs} - \frac{V_{fbt} - V_{fbb}}{2} - \phi_0(z)}{\left(\frac{1}{4} + \frac{t_{ox}\varepsilon_{si}}{\varepsilon_{ox}t_{si}}\right)t_{si}^2} \tag{2.14}$$

$$\lambda^2 = \frac{1}{\left(\frac{1}{4} + \frac{t_{ox}\varepsilon_{si}}{\varepsilon_{ox}t_{si}}\right)t_{si}^2} \tag{2.15}$$

Where λ^2, is known the natural length with the Centre channel potential.

Now, substituting the value of $c_0(z)$, $c_1(z)$ and $c_2(z)$ in Eq. (2.10) then, the 2D-potential of the channel is

$$\phi(x,z) = \phi_0(z)\left(1-\lambda^2 x^2\right) + \left(V_{gs} - V_{fb}\right)\lambda^2 x^2 \tag{2.16}$$

Since Eq. (2.1) is usable over the channel. So, we can write the Poisson's equation at the SOI center in the form as:

$$\left.\frac{\partial^2 \varphi(x,z)}{\partial x^2}\right|_{x=0} + \left.\frac{\partial^2 \varphi(x,z)}{\partial z^2}\right|_{x=0} = \frac{qN_a}{\varepsilon_{si}} \tag{2.17}$$

Using Eq. (2.16) in Eq. (2.17), we obtain

$$\frac{\partial^2 \varphi_0(z)}{\partial z^2} - 2\lambda^2 \phi_0(z) = \frac{qN_a}{\varepsilon_{si}} - 2\left(V_{gs} - V_{fb}\right)\lambda^2 \tag{2.18}$$

Above equation is a 2nd order differential equation and its solution having both complementary as well as particular integral part, which is given below

$$\phi_0(z) = Ae^{\sqrt{2}\lambda z} + Be^{-\sqrt{2}\lambda z} + \gamma \tag{2.19}$$

Where,

$$\gamma = \left(V_{gs} - V_{fb}\right) - \frac{qN_a}{2\lambda^2 \varepsilon_{si}} \tag{2.20}$$

By using Eq. (2.19) in Eq. (2.16), the 2D channel potential of the fully depleted doped symmetric DG MOSFETs is written as

$$\phi(x,z) = \left(Ae^{\sqrt{2}\lambda z} + Be^{-\sqrt{2}\lambda z} + \gamma\right)\left(1-\lambda^2 x^2\right) + \left(V_{gs} - V_{fb}\right)\lambda^2 x^2 \tag{2.21}$$

In the above equation A and B are arbitrary constant and it is obtained by using the above boundary conditions.

$$A=\frac{\left(V_{bi}-\left(V_{gs}-V_{fb}\right)+\frac{qN_a}{2\lambda^2\varepsilon_{si}}\right)\left(1-e^{-\sqrt{2}\lambda L}\right)+V_{ds}}{\left(e^{\sqrt{2}\lambda L}-e^{-\sqrt{2}\lambda L}\right)} \tag{2.22}$$

$$B=-\frac{\left(V_{bi}-\left(V_{gs}-V_{fb}\right)+\frac{qN_a}{2\lambda^2\varepsilon_{si}}\right)\left(1-e^{\sqrt{2}\lambda L}\right)+V_{ds}}{\left(e^{\sqrt{2}\lambda L}-e^{-\sqrt{2}\lambda L}\right)} \tag{2.23}$$

In the above equation if we have put the value of x =t_{si}/2 then we get the surface potential of the channel as:

$$\phi_s(z)=\phi\left(\frac{t_{si}}{2},z\right)=\phi_0(z)\left(1-\lambda^2\frac{t_{si}^2}{4}\right)+\left(V_{gs}-V_{fb}\right)\lambda^2\frac{t_{si}^2}{4} \tag{2.24}$$

2.3 **Threshold Voltage Derivation**

In this unit, we will use the 2D potential function $\phi(x,z)$ described above by Eq.(2.16) or Eq.(2.24) for analytical modeling of the threshold voltage of the device. Since minimum surface potential of a MOS device gives the source-channel barrier potential that an electron needs to overcome to enter into the channel from the source, the minimum value of the surface potential plays the important role in determining the threshold voltage of the CMOS devices. To determine the minimum surface potential of the symmetric DG MOSFETs, we may proceed as follows:

It may be noted from Eq. (2.24) that the surface potentials $\phi(x,z)\big|_{x=\frac{t_{si}}{2}}$ at the Si-SiO_2 interfaces (i.e. at $x=\frac{t_{si}}{2}$) of the constant doped symmetric DG MOSFET are same. Thus, if $\phi_s(z)$ denotes the surface potential of any of the two surfaces of the device, $\phi_s(z)$ can be written from Eq. (2.24) as

$$\phi_s(z)=\phi_0(z)\left(1-\lambda^2\frac{t_{si}^2}{4}\right)+\left(V_{gs}-V_{fb}\right)\lambda^2\frac{t_{si}^2}{4} \tag{2.25}$$

Now suppose that the minimum value of the surface potential $\phi_s(z)$ is denoted by $\phi_{s\min}$ which

occurs at $z = z_{0\min}$, that is, $\phi_s(z_{\min}) = \phi_{s\min}$. Clearly, the value of $z_{0\min}$ can be developed by solving the equation (2.25).

$$\left.\frac{d\varphi_s(z)}{dz}\right|_{z=z_{0\min}} = \left.\frac{d\varphi_0(z)}{dz}\right|_{z=z_{0\min}} - \lambda^2 \frac{t_{si}^{\;2}}{4} \left.\frac{d\varphi_0(z)}{dz}\right|_{z=z_{0\min}} = 0 \tag{2.26}$$

Eq. (2.26) shows that $\phi_s(z)$ will be minimum at $z = z_{0\min}$ if the channel center potential $\phi_0(z)$ is also minimum at $z = z_{0\min}$ since Eq. (2.26) will be satisfied if and only if

$$\left.\frac{d\varphi_0(z)}{dz}\right|_{z=z_{0\min}} = 0 \tag{2.27}$$

Now, suppose that $\phi_{0\min} = \phi_0(z_{0\min})$ represents the minimum value of $\phi_0(z)$ at $z = z_{0\min}$. Using Eq. (2.19) in Eq. (2.27) and solving the resultant equation for $z_{0\min}$, we can obtain

$$z_{0\min} = \frac{1}{2\sqrt{2}\lambda} \ln \frac{B}{A} \tag{2.28}$$

Using Eq. (2.28) in Eq. (2.19), the minimum value of the channel center potential is

$$\phi_{0\min} = 2\sqrt{AB} + \gamma \tag{2.29}$$

Substituting the value of $\phi_{0\min}$ in Eq. (2.25), the minimum surface potential can be written as

$$\phi_{s\min} = \phi_0(z_{\min})\left(1 - \lambda^2 \frac{t_{si}^2}{4}\right) + \left(V_{gs} - V_{fb}\right)\lambda^2 \frac{t_{si}^2}{4} \tag{2.30}$$

Substituting the value of $\phi_0(z_{\min})$ from Eq. (2.29) into Eq. (2.30), which finally express the minimum surface potential as follows:

$$\phi_{s\min} = \left(2\sqrt{AB} - \frac{qN_a}{2\lambda^2 \varepsilon_{si}}\right)\left(1 - \lambda^2 \frac{t_{si}^2}{4}\right) + \left(V_{gs} - V_{fb}\right) \tag{2.31}$$

Since any of two Si-SiO_2 interfaces of the DG-MOSFET is similar to the SOI MOSFET, we can define the threshold voltage of the symmetrical DG MOSFETs by using the methodology reported by Lee *et al.* [59] for SOI MOSFETs. The threshold voltage of the DG MOS device is

the gate voltage where the minimum surface potential becomes twice the Fermi –shift potential of Si channel and it is given by

$$\phi_{s\min}\Big|_{V_{gs}=V_{th}} = \phi_{s\min} = 2\varphi_F$$

Where, $\Phi_F = V_T \ln\left(\frac{N_a}{n_i}\right)$ is the Fermi-shift potential of silicon channel and Substituting $\phi_{s\min}$ in Eq. (2.31) and putting $V_{gs} = V_{th}$ in the resultant equation we can write the threshold voltage V_{th} in the polynomial form as :

$$V_{th} = 2\varphi_F + \frac{qN_a}{2\lambda^2\varepsilon_{si}}\left(1-\lambda^2\frac{t_{si}^2}{4}\right) + V_{fb} - 2\sqrt{AB}\left(1-\lambda^2\frac{t_{si}^2}{4}\right) \tag{2.32}$$

$$V_{th} = 2\varphi_F + \frac{qN_a}{2\lambda^2\varepsilon_{si}}\left(1-\lambda^2\frac{t_{si}^2}{4}\right) + V_{fb} - 2\sqrt{(a_1 - a_2V_{th})(a_3 - a_4V_{th})}\left(1-\lambda^2\frac{t_{si}^2}{4}\right) \tag{2.33}$$

Where,

$$a_1 = \frac{V_{ds} + \left(V_{bi} + \frac{qN_a}{2\lambda^2\varepsilon_{si}}\left(1-\lambda^2\frac{t_{si}^2}{4}\right) + V_{fb}\right)\left(1-e^{-\sqrt{2}\lambda L}\right)}{\left(e^{\sqrt{2}\lambda L} - e^{-\sqrt{2}\lambda L}\right)\left(1-\lambda^2x^2\right)} \tag{2.34}$$

$$a_2 = \frac{\left(1-e^{-\sqrt{2}\lambda L}\right)}{\left(e^{\sqrt{2}\lambda L} - e^{-\sqrt{2}\lambda L}\right)\left(1-\lambda^2x^2\right)} \tag{2.35}$$

$$a_3 = -\frac{V_{ds} + \left(V_{bi} + \frac{qN_a}{2\lambda^2\varepsilon_{si}}\left(1-\lambda^2\frac{t_{si}^2}{4}\right) + V_{fb}\right)\left(1-e^{\sqrt{2}\lambda L}\right)}{\left(e^{\sqrt{2}\lambda L} - e^{-\sqrt{2}\lambda L}\right)\left(1-\lambda^2x^2\right)} \tag{2.36}$$

$$a_4 = -\frac{\left(1-e^{\sqrt{2}\lambda L}\right)}{\left(e^{\sqrt{2}\lambda L} - e^{-\sqrt{2}\lambda L}\right)\left(1-\lambda^2x^2\right)} \tag{2.37}$$

$$a_5 = 4\left(1-\lambda^2 \frac{t_{si}^2}{4}\right)^2 \tag{2.38}$$

From the above equation it is clear that when the channel length of the device is large i.e $L \to \infty$,the last term of Eq. (2.33) tends to zero; and hence the threshold voltage, say V_{th-L} , can be obtained as

$$V_{th-L} = 2\varphi_F + \frac{qN_a}{2\lambda^2 \varepsilon_{si}}\left(1-\lambda^2 \frac{t_{si}^2}{4}\right) \tag{2.39}$$

With the help of Eq. (2.33) and (2.38), the threshold voltage of the symmetric DG MOSFETs is

$$X_1 V_{th}{}^2 + V_{th} X_2 + X_3 = 0 \tag{2.40}$$

$$V_{th} = \frac{-X_2 - \sqrt{X_2^2 - 4X_1X_3}}{2X_1} \tag{2.41}$$

Where,

$$X_1 = 1 - a_2a_4a_5 \tag{2.42}$$

$$X_2 = \left(a_2a_3a_5 + a_2a_4a_5 - 2V_{th-L}\right) \tag{2.43}$$

$$X_3 = \left(V_{th-L}{}^2 - a_1a_3a_5\right) \tag{2.44}$$

Since due to shortening of the channel length, the threshold voltage of the device is degraded and the difference between the threshold voltages of the short-channel -long-channel devices can be written as

$$\Delta V_{th} = V_{th-L} - V_{th} \tag{2.45}$$

Where, V_{th-L} and ΔV_{th} have been described by Eq.(2.39) and Eq.(2.45) respectively.

2.4 Channel Potential Derivation of the DG- MOSFET obtained by cutline (BB')

As we have find that the threshold voltage of the symmetrical double gate MOSFETs using the concept of center potential and surface potential of the schematic diagram shown in Fig (2). In the same way we can find the threshold voltage of the structure shown in Fig (3).

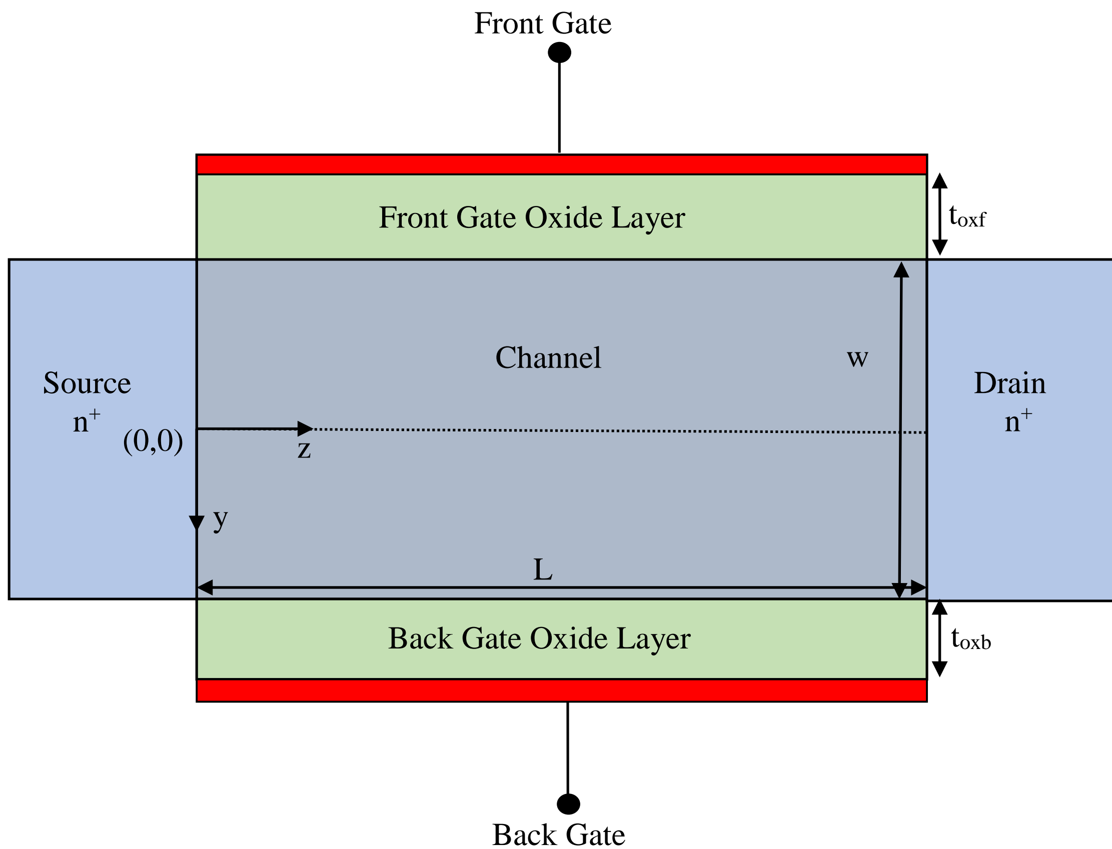

Figure 3 Schematic structure of the DG-MOSFET used for modeling and simulation

The y- axes and the z-axes are along the channel width and length respectively which is shown in the figure (3). For the distinction of the two gates, we use the nomenclatures of the gates as to front-gate and back-gate of the device.

The channel potential distribution is $\phi(y,z)$, According to the Poisson equation, the channel potential is expressed by eq. (2.46).

$$\frac{\partial^2\varphi(y,z)}{\partial y^2}+\frac{\partial^2\varphi(y,z)}{\partial z^2}=\frac{qN_a}{\varepsilon_{si}} \tag{2.46}$$

The Poisson equation expressed by eq. (2.46) is solved using the following boundary conditions:

$$\phi(y,z)\Big|_{y=0}=\phi_{01}(z) \tag{2.47}$$

$$\left.\frac{\partial\phi(y,z)}{\partial y}\right|_{y=0}=0 \tag{2.48}$$

$$\frac{\varepsilon_{ox}}{t_{ox}}\left(V_{gs}-V_{fb}-\phi\left(-\frac{w}{2},z\right)\right)=-\varepsilon_{si}\left.\frac{\partial\phi(y,z)}{\partial y}\right|_{y=-\frac{w}{2}} \tag{2.49}$$

$$\frac{\varepsilon_{ox}}{t_{ox}}\left(V_{gs}-V_{fb}-\phi\left(\frac{w}{2},z\right)\right)=\varepsilon_{si}\left.\frac{\partial\phi(y,z)}{\partial y}\right|_{y=\frac{w}{2}} \tag{2.50}$$

$$\phi(y,0)=V_{bi} \tag{2.51}$$

$$\phi(y,L)=V_{bi}+V_{ds} \tag{2.52}$$

According to Young *et al*., the 2-D channel potential function can be approximated as parabolic in nature and expressed as

$$\phi(y,z)=c_3(z)+c_4(z)y+c_5(z)y^2$$

Where, $c_3(z)$, $c_4(z)$ and $c_5(z)$ are arbitrary functions of z which are found by applying the boundary condition in the above Poisson equation.

After solving the above equation From), we get

$$\phi(y,z)=\phi_{01}(z)\left(1-\lambda_1^2 y^2\right)+\left(V_{gs}-V_{fb}\right)\lambda_1^2 y^2 \quad (2.53)$$

$$\lambda_1^2=\frac{1}{\left(\frac{1}{4}+\frac{t_{ox}\varepsilon_{si}}{\varepsilon_{ox}w}\right)w^2} \quad (2.54)$$

Where λ_1^2, is called the natural length with the Centre channel potential.

Since Eq. (2.46) is usable over all the channel region. So, we can write the Poisson's equation at the SOI center in the form as:

$$\left.\frac{\partial^2\varphi(y,z)}{\partial y^2}\right|_{y=0}+\left.\frac{\partial^2\varphi(y,z)}{\partial z^2}\right|_{y=0}=\frac{qN_a}{\varepsilon_{si}} \quad (2.55)$$

Using Eq. (2.16) in Eq. (2.17), we obtain

$$\frac{\partial^2\varphi_{01}(z)}{\partial z^2}-2\lambda_1^2\phi_{01}(z)=\frac{qN_a}{\varepsilon_{si}}-2\left(V_{gs}-V_{fb}\right)\lambda_1^2 \quad (2.56)$$

After solving above equation and using boundary value condition we get the surface potential as given below

$$\phi(y,z)=\left(A_1e^{\sqrt{2}\lambda_1 z}+B_1e^{-\sqrt{2}\lambda_1 z}+\gamma_1\right)\left(1-\lambda_1^2y^2\right)+\left(V_{gs}-V_{fb}\right)\lambda_1^2y^2 \quad (2.57)$$

In the above equation A_1 and B_1 are arbitrary constant and it is obtained by using the above boundary conditions.

$$A_1=\frac{\left(V_{bi}-\left(V_{gs}-V_{fb}\right)+\frac{qN_a}{2\lambda_1^2\varepsilon_{si}}\right)\left(1-e^{-\sqrt{2}\lambda_1 L}\right)+V_{ds}}{\left(e^{\sqrt{2}\lambda_1 L}-e^{-\sqrt{2}\lambda_1 L}\right)} \quad (2.58)$$

$$B_1=-\frac{\left(V_{bi}-\left(V_{gs}-V_{fb}\right)+\frac{qN_a}{2\lambda_1^2\varepsilon_{si}}\right)\left(1-e^{\sqrt{2}\lambda_1 L}\right)+V_{ds}}{\left(e^{\sqrt{2}\lambda_1 L}-e^{-\sqrt{2}\lambda_1 L}\right)} \quad (2.59)$$

In the above equation if we have put the value of y =w/2 then we get the surface potential of the channel as:

$$\phi_s(z) = \phi\left(\frac{w}{2}, z\right) = \phi_{01}(z)\left(1 - \lambda_1^2 \frac{w^2}{4}\right) + \left(V_{gs} - V_{fb}\right)\lambda_1^2 \frac{w^2}{4} \tag{2.60}$$

2.5 Threshold Voltage Derivation

In the same way as we have find the threshold voltage of the schematic diagram as shown in fig (2) we have find the threshold voltage of the schematic diagram as shown in figure (3).

We have got the threshold voltage as given below :

$$V_{th} = 2\varphi_F + \frac{qN_a}{2\lambda_1^2 \varepsilon_{si}}\left(1 - \lambda_1^2 \frac{w^2}{4}\right) + V_{fb} - 2\sqrt{A_1 B_1}\left(1 - \lambda_1^2 \frac{w^2}{4}\right) \tag{2.61}$$

$$V_{th} = 2\varphi_F + \frac{qN_a}{2\lambda_1^2 \varepsilon_{si}}\left(1 - \lambda_1^2 \frac{w^2}{4}\right) + V_{fb} - 2\sqrt{\left(a_5 - a_6 V_{th}\right)\left(a_7 - a_8 V_{th}\right)}\left(1 - \lambda_1^2 \frac{w^2}{4}\right) \tag{2.62}$$

Where,

$$a_6 = \frac{V_{ds} + \left(V_{bi} + \frac{qN_a}{2\lambda_1^2 \varepsilon_{si}}\left(1 - \lambda_1^2 \frac{w^2}{4}\right) + V_{fb}\right)\left(1 - e^{-\sqrt{2}\lambda_1 L}\right)}{\left(e^{\sqrt{2}\lambda_1 L} - e^{-\sqrt{2}\lambda_1 L}\right)\left(1 - \lambda_1^2 y^2\right)} \tag{2.63}$$

$$a_7 = \frac{\left(1 - e^{-\sqrt{2}\lambda_1 L}\right)}{\left(e^{\sqrt{2}\lambda_1 L} - e^{-\sqrt{2}\lambda_1 L}\right)\left(1 - \lambda_1^2 y^2\right)} \tag{2.64}$$

$$a_8 = -\frac{V_{ds} + \left(V_{bi} + \frac{qN_a}{2\lambda_1^2 \varepsilon_{si}}\left(1 - \lambda_1^2 \frac{w^2}{4}\right) + V_{fb}\right)\left(1 - e^{\sqrt{2}\lambda_1 L}\right)}{\left(e^{\sqrt{2}\lambda_1 L} - e^{-\sqrt{2}\lambda_1 L}\right)\left(1 - \lambda_1^2 y^2\right)} \tag{2.65}$$

$$a_9 = -\frac{\left(1 - e^{\sqrt{2}\lambda_1 L}\right)}{\left(e^{\sqrt{2}\lambda_1 L} - e^{-\sqrt{2}\lambda_1 L}\right)\left(1 - \lambda_1^2 y^2\right)} \tag{2.66}$$

$$a_{10} = 4\left(1 - \lambda_1^{\,2}\,\frac{w^2}{4}\right)^2 \tag{2.67}$$

From the above equation it is clear that when the channel length of the device is large i.e $L \rightarrow \infty$,the last term of Eq. (2.62) tends to zero; and hence the threshold voltage, say V_{th-L} , can be obtained as

$$V_{th-L} = 2\varphi_F + \frac{qN_a}{2\lambda_1^{\,2}\varepsilon_{si}}\left(1 - \lambda_1^{\,2}\,\frac{w^2}{4}\right) \tag{2.68}$$

With the help of Eq. (2.62) and (2.68), the threshold voltage of short-channel symmetric DG MOSFETs which is shown in figure(3) is denoted as

$$X_4 V_{th}^{\;2} + V_{th} X_5 + X_6 = 0 \tag{2.69}$$

$$V_{th} = \frac{-X_5 - \sqrt{X_5^2 - 4X_4X_6}}{2X_4} \tag{2.70}$$

Where,

$$X_4 = 1 - a_7 a_9 a_{10} \tag{2.71}$$

$$X_5 = \left(a_7 a_8 a_{10} + a_7 a_9 a_{10} - 2V_{th-L}\right) \tag{2.72}$$

$$X_6 = \left(V_{th-L}^{\;\;2} - a_6 a_8 a_{10}\right) \tag{2.73}$$

Since the threshold voltage roll-off ΔV_{th} represents the degradation of the threshold voltage due to shortening of the channel length, we may define ΔV_{th} as the difference between the threshold voltages of the long-channel and short-channel devices and can be written as

$$\Delta V_{th} = V_{th-L} - V_{th} \tag{2.74}$$

Where, V_{th-L} and ΔV_{th} have been described by Eq.(2.68) and Eq.(2.70) respectively.

2.6 List of parameter used

Table .1 List of parameters and its values used in simulation

Parameters	Values
t_{ox}	1nm-5nm
t_{si}	5nm-15nm
L	20nm-100nm
W	5nm-15nm
N_d	$10^{20} cm^{-3}$
N_a	$10^{17} cm^{-3}$
μ_n	$1076 cm^2 / (cm-s)$
V_{gs}	$0-1$ V
V_{ds}	$0.05-3$ V

2.7 **Results & Discussion**

A comparison has been done between analytical model and numerical simulation for threshold voltage,obtained by using the surface potential of DG MOSFETs. To getting the accurate results for MOSFET simulation, we needed to account for the mobility degradation that occurs inside inversion layers. The drift-diffusion model is the default carrier transport model in Sentaurus Device which is activated in our simulation. In the simulation basic mobility model is used, that

takes into account the effect of doping dependence, high-field saturation (velocity saturation), and transverse field dependence. The impact ionization effects are ignored in our device simulation. The silicon band gap narrowing model that determines the intrinsic carrier concentration is activated. The solution of the device equations are done self-consistently, on the discrete mesh, in an iterative fashion. For each iteration, an error is calculated and device attempts to converge on a solution that has an acceptably small error. The Poisson equation, continuity equations, and the different thermal and energy equations are included in simulation. All the structure junctions assumed as abrupt, and the biasing conditions considered at room temperature in the simulation.

The junctions formed between source and body , drain and body are supposed to be abrupt due to large doping concentration of the source/drain N_{DS} = 1e20 cm^{-3}.To make the device symmetrical, modeling done under the consideration of identical top and bottom gate structure having same thickness of oxide, the material we have used as electrodes for both the gate, top and bottom are same and material used for electrode is taken as tungsten because it is easily available and its deposition on oxide is not difficult. Therefore, the device will become a totally symmetric structure. Figure (4) shows the mesh-analysis of Double-Gate (DG) MOSFET which is obtained by Sentaurus software. Fig. (5) shows the schematic structure of Double-Gate (DG) MOSFET with channel doping profile. From Fig (6) It can be noted that source channel barrier height at channel center is lower than the surface and hence the V_{th} should be calculated by using the center potential minima. To validate the analytical surface potential model, The variation of surface potential with the channel length position for different gate biasing are given in Fig. (6). The analytical model results and the numerical simulator results are matched. It is found that the minimum surface potential found to be decrease with increase in gate voltage. Fig. (7) Shows the variation of surface potential with the channel length position for different channel thickness and we get a good agreement between analytical model results with the numerical simulator results.

The source to channel barrier increases with decreasing the channel thickness as shown in Fig. (7). When the channel thickness is decreases, the gate controllability on the channel is increases because the electric field in vertical direction is increased and hence potential of channel is also increases. The analytical model results and the numerical simulator results are matched.

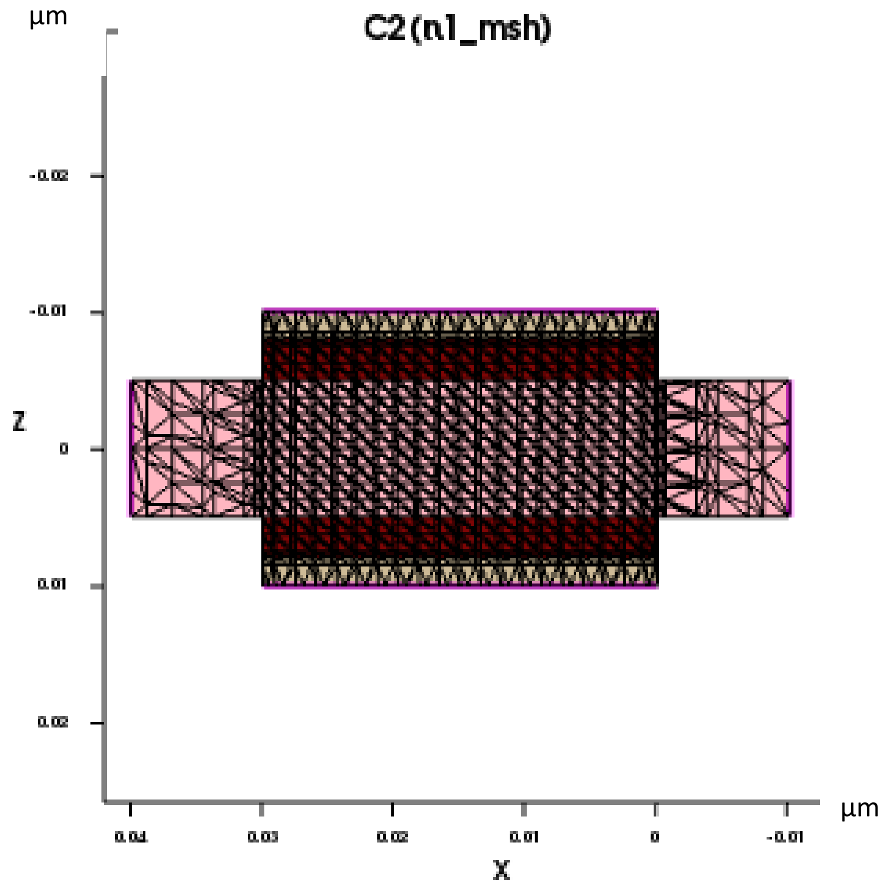

Figure 4 the mesh-analysis of Double-Gate (DG) MOSFET

From Fig. (7), it is observed that the source to channel barrier increases with decreasing the channel thickness . The source to channel barrier increases with decreasing the channel thickness as shown in Fig. (7). When the channel thickness is decreases, the gate controllability on the channel is increases because the electric field in vertical direction is increased and hence surface potential of channel is also increases. The analytical model results and the numerical simulator results are matched. Fig. (8) shows the variation of surface potential with the channel length position for different oxide thickness. We get a good agreement between analytical model results with the numerical simulator results. When the oxide thickness is decreases the control of gate on the channel is increases because the electric field in vertical direction is increased and hence

potential of channel is also increases. But the carrier in channel may have got the enough energy and it penetrate the oxide layer and these trap charge may be degrade the threshold voltage. So we cannot decrease the oxide thickness too much. We get a good agreement between analytical model results with the numerical simulator results. Fig (9) shows the threshold voltage roll-off variation against channel length for different thickness (t_{si}) of the channel. Note that, As the channel thickness (t_{si}) increases the threshold voltage decreased along the channel length. It is happened due to decrease quantum confinement. Note that threshold voltage of the device is increased with increase in (N_a) because of increase in overall doping level of the channel. The source-channel barrier increases with the increasing doping level and thereby increases the threshold voltage. Fig. (10) demonstrates the variation in the threshold voltage roll-off, against the device channel length for different oxide thicknesses. We have found that if channel oxide thickness decreased then, the roll-off increases.

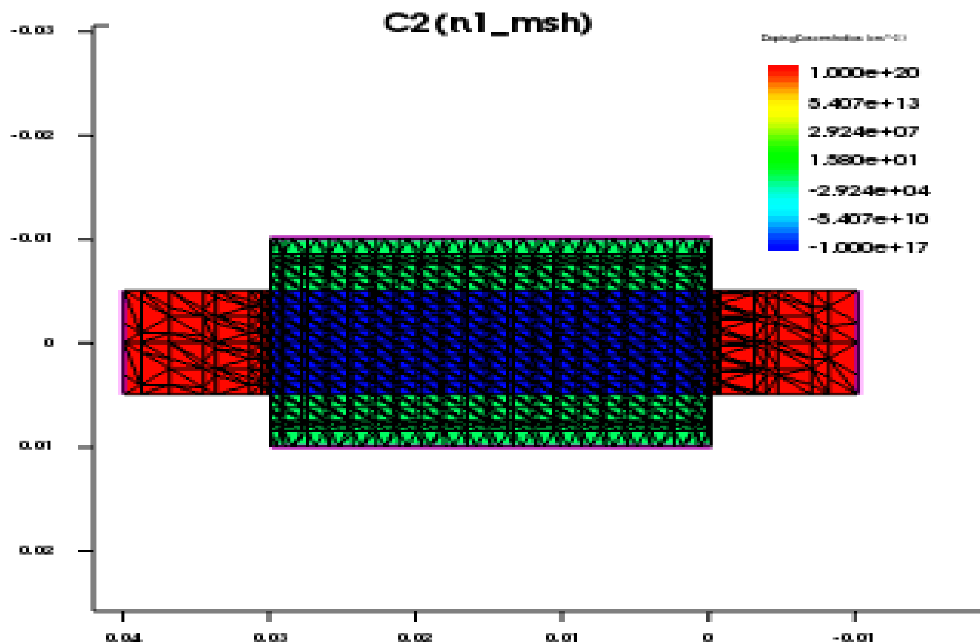

Figure 5 The schematic structure of DG-MOSFET with channel doping profile

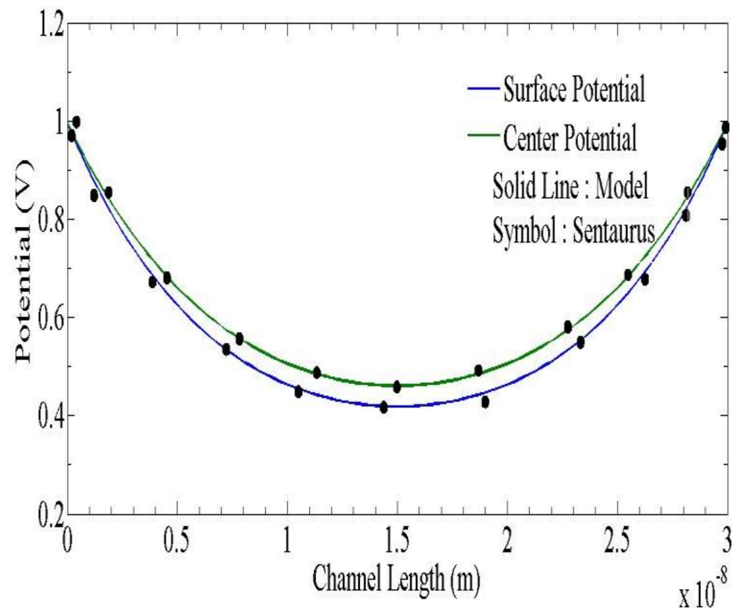

Figure 6 Potential distribution variation along the channel length. Parameter used are, tsi=3 nm, Vds=0 V , Vgs=0 V .

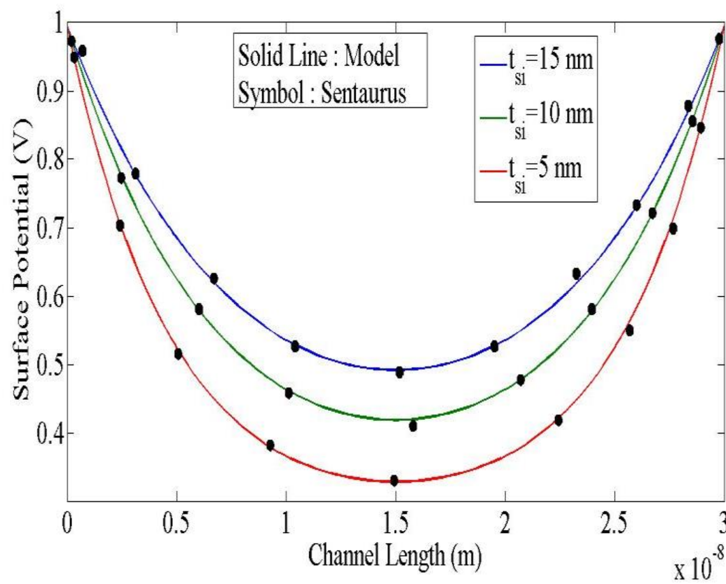

Figure 7 Surface Potential distribution variation along the channel length for different channel thickness. Parameter used are tsi=3 nm, Vds=0 V Vgs=0 V .

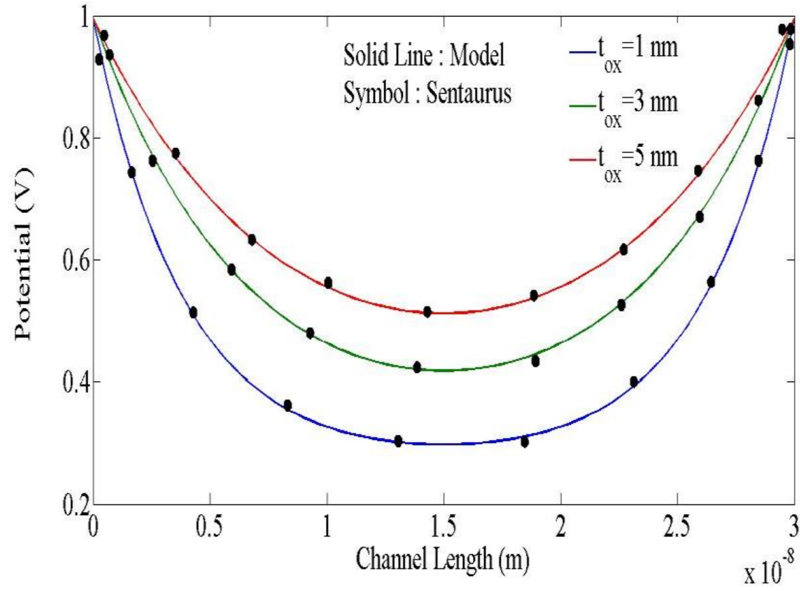

Figure 8 Distribution of Surface potential with channel length for different oxide thickness. Parameter used are tsi=10 nm, Vds=0 V, Vgs=0 V.

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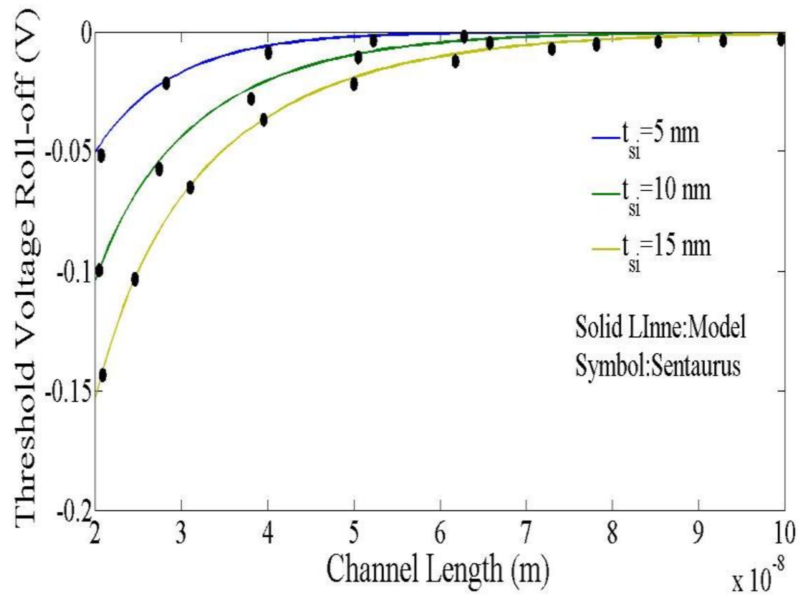

Figure 9 Distribution of threshold voltage roll-off with channel length for different channel thickness. Parameter used are tsi=10 nm, Vds=0 V, Vgs=0 V .

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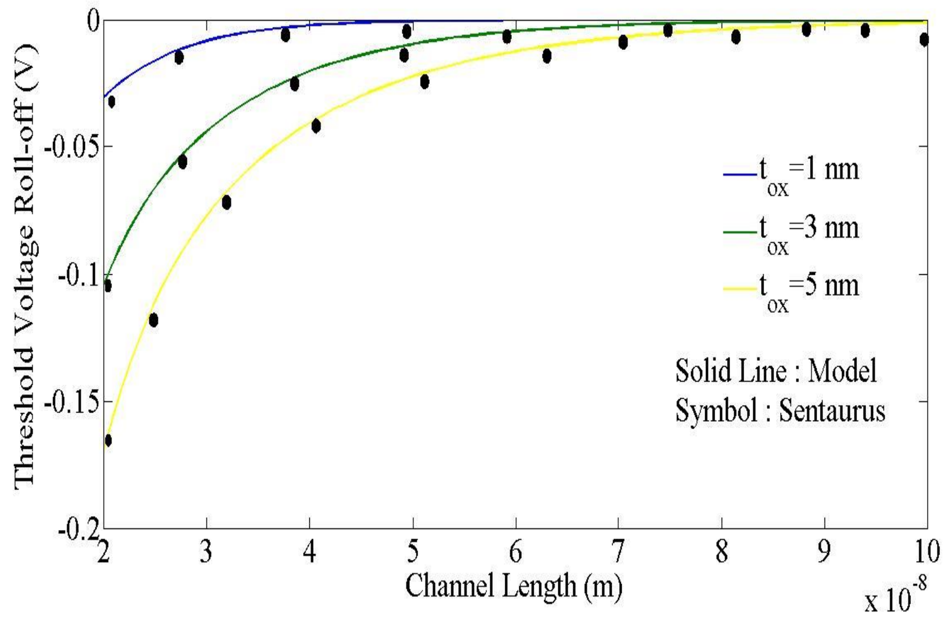

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Figure 10 Variation of threshold voltage roll-off with channel length for different oxide thickness. Parameter used are tsi=10 nm, Vds=0.05 V Vgs=0 V .

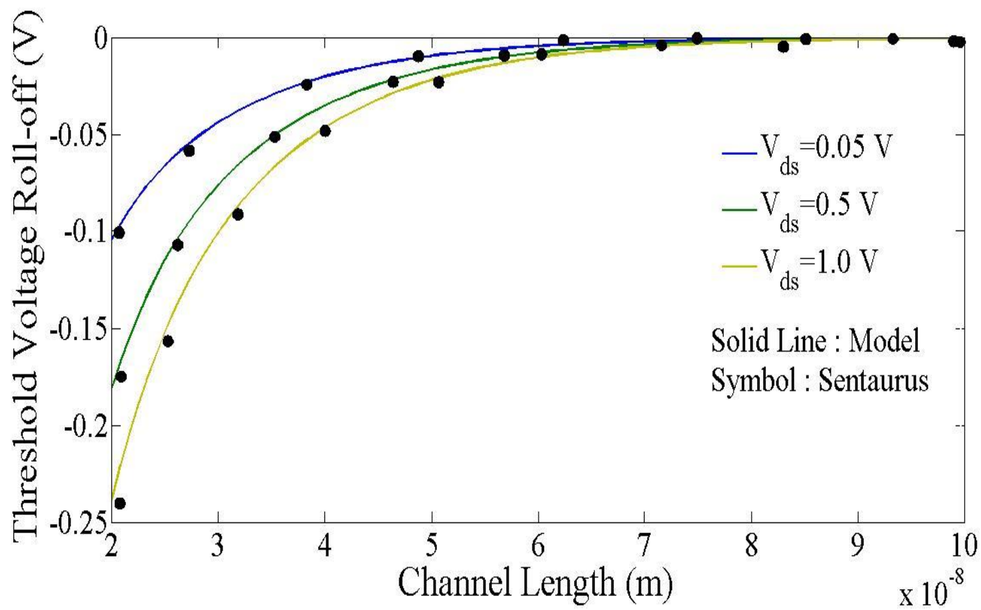

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Figure 11 Distribution of threshold voltage roll-off with variation of channel length for different biasing voltage. Parameter used are $t_{si} = 10nm$, $t_{ox} = 3nm$, $V_{ds} = 0.05V, V_{gs} = 0V$.

Chapter 3

Modeling and Simulation of Subthreshold Swing

3.1 Introduction

It is already discussed in chapter-1 that the threshold voltage of a MOSFET gives its switching characteristics, one other important characteristics of MOSFET is Subthreshold swing, discussion of this important characteristic is necessary because it gives the idea about the standby power dissipation and switching characteristics of the CMOS devices. The present chapter has been designed to carry out the modeling and simulation of the Subthreshold swing of the DG MOS devices with a constant doping profile considered in this dissertation. The solution of minimum surface potential obtained in the previous chapter has been employed in the present chapter to model the above characteristics of the CMOS device under considerations.

3.2 **Subthreshold Current Model Derivation of double gate MOSFETs obtained by cutline AA'**

The schematic structure of Undoped DG- MOSFET device used for the modeling and Sentaurus simulation is shown in Fig. (2). To estimate the Subthreshold current we consider that the subthreshold current flow due to the diffusion of carriers .

$$J_s = qD_n \frac{n_m}{L}\left(1-\exp\left(\frac{-V_{ds}}{V_T}\right)\right) \tag{3.1}$$

Where, n_m is the free electron density in weak inversion region and n_m is found by using the classical Boltzmann's equation and written as

$$n_m = \frac{n_i^2}{N_a}\exp\left(\frac{\phi_{\min}(z)}{V_T}\right) \tag{3.2}$$

Where, n_i is the intrinsic carrier concentration of the silicon channel, V_T is the thermal voltage and

$$\phi_{s\min}(z) = \phi_{0\min} + (\beta - \phi_{0\min})\lambda^2 x^2 \tag{3.3}$$

Where,

$$\beta = V_{gs} - V_{fb} \tag{3.4}$$

D_n ,Is the diffusion constant and $N_{DS} = 1\times10^{20}\,\mathrm{cm}^{-3}$, the drain/source doping density. By integrating Eq. (3.1) over the entire silicon channel thickness we have got the Subthreshold current and it is written as

$$I_D = \int_{-\frac{t_{si}}{2}}^{\frac{t_{si}}{2}} \int_{-\frac{w}{2}}^{\frac{w}{2}} qD_n \frac{n_m}{L}\left(1-\exp\left(\frac{-V_{ds}}{V_T}\right)\right) dydx \tag{3.5}$$

Using Eq. (3.2) for n_m in Eq. (3.5), we can write as,

$$I_D = qD_n \frac{n_i^2}{N_a L}\left(1-\exp\left(\frac{-V_{ds}}{V_T}\right)\right) w \int_{-\frac{t_{si}}{2}}^{\frac{t_{si}}{2}} \exp\left(\frac{\phi_{s\min}(z)}{V_T}\right) dx \tag{3.6}$$

By using Eq. (3.3) and Eq. (3.6) we get

$$I_D = D \int_{-\frac{t_{si}}{2}}^{\frac{t_{si}}{2}} \exp\left[\left(\frac{\beta - \phi_{0\min}}{V_T}\right)\lambda^2 x^2\right] dx \tag{3.7}$$

Where, $$D = qD_n \frac{n_i^2}{N_a L}\left(1-\exp\left(\frac{-V_{ds}}{V_T}\right)\right) w \times \exp\left(\frac{\phi_{0\min}}{V_T}\right) \tag{3.8}$$

Using the trapezoidal rule of the numerical integration Eq. (3.7) can be written as

$$I_D = D\frac{t_{si}}{2m}\left[\exp\left(\left(\frac{(\beta-\phi_{0\min})\lambda^2}{V_T}\right)\left(\frac{t_{si}}{2}\right)^2\right) + 2\sum_{k=1}^{m-1}\exp\left(\left(\frac{(\beta-\phi_{0\min})\lambda^2}{V_T}\right)\left(\frac{t_{si}}{2m}k\right)^2\right) + \exp\left(\left(\frac{(\beta-\beta_{0\min})\lambda^2}{V_T}\right)\left(-\frac{t_{si}}{2}\right)^2\right)\right] \quad (3.9)$$

Where, 'm' is the number of linear sections between intervals $\left[-\frac{t_{si}}{2},\frac{t_{si}}{2}\right]$. Considering $m=1$ for better physical insight and simplicity, Eq. (3.9) can be written as

$$I_D = D t_{si}\exp\left(\left(\frac{(\beta-\phi_{0\min})\lambda^2}{V_T}\right)\left(\frac{t_{si}}{2}\right)^2\right) \quad (3.10)$$

By putting the value of the constant D from the Eq. (3.8) into Eq. (3.10), an alternative for Subthreshold current can be given by

$$I_D = \frac{qD_n n_i^2}{N_a L}W\left(1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right)\exp\left(\frac{\phi_{0\min}}{V_T}\right)t_{si}\exp\left(\left(\frac{V_{gs}-V_{fb}-\phi_{0\min}}{\lambda^2 V_T}\right)\left(\frac{t_{si}}{2}\right)^2\right) \quad (3.11)$$

3.3 Subthreshold Swing Model Derivation of double gate MOSFETs obtained by cutline AA'

The Subthreshold swing of any CMOS device is defined as the reciprocal of the slope of the Subthreshold characteristic curve representing the variation of $\log(I_D)$ as a function of the gate voltage V_G, where I_D is the drain current in the Subthreshold regime of operation of the MOS device. Thus, if S represents the Subthreshold swing of the DG MOSFET under consideration, we can write

$$S = \frac{dV_{gs}}{d(\log I_{ds})} = \ln 10 \times \frac{dV_{gs}}{d\phi_{\min}}\frac{d\phi_{\min}}{dI_{ds}}I_{ds} \quad (3.12)$$

Where V_{gs} is the gate voltage, I_{ds} is the drain current, and $\phi_{\min}$ is the minimum surface potential, and the influence of interface trap charge is neglected. The Subthreshold slop is usually represented by the following classical expression.

$$S \approx \ln 10 \times V_T \times \left(\frac{\partial \phi_{\min}}{\partial V_{gs}} \right)^{-1} \tag{3.13}$$

Where, V_T is the thermal voltage in the normal atmospheric temperature.

From previous chapter we have find that the minimum surface potential is

$$\phi_{s\min} = \phi_0 \left(z_{\min} \right) \left(1 - \lambda^2 \frac{t_{si}^2}{4} \right) + \left(V_{gs} - V_{fb} \right) \lambda^2 \frac{t_{si}^2}{4} \tag{3.14}$$

Where,

$$\phi_{0\min} = 2\sqrt{AB} + \gamma \tag{3.15}$$

$$\frac{\partial \phi_{\min}}{\partial V_{gs}} = \left(1 - \lambda^2 x^2 \right) \frac{\partial \phi_{0\min}}{\partial V_{gs}} + \lambda^2 x^2 \tag{3.16}$$

$$S = \ln 10 \times V_T \left[\left(1 - x^2 \lambda^2 \right) \left(1 - \sqrt{\frac{B}{A}} \left(\frac{1 - e^{-\sqrt{2}\lambda L}}{e^{\sqrt{2}\lambda L} - e^{-\sqrt{2}\lambda L}} \right) + \sqrt{\frac{A}{B}} \left(\frac{1 - e^{\sqrt{2}\lambda L}}{e^{\sqrt{2}\lambda L} - e^{-\sqrt{2}\lambda L}} \right) \right) + \lambda^2 x^2 \right] \tag{3.17}$$

Where λ , A and B are given in previous chapter.

First term in the above expression states that the Subthreshold slope is $60 to 70 mV / decade$ for a long channel device. The latter term is due to the short channel effect.

3.4 Subthreshold Current Model Derivation of double gate MOSFETs obtained by cutline BB'

The schematic structure of Undoped DG- MOSFET device used for the modeling and Sentaurus simulation is shown in Fig. (2.2). To estimate the Subthreshold current we consider that the subthreshold current flow due to the diffusion of carriers

$$J_s = qD_n \frac{n_m}{L} \left(1 - \exp\left(\frac{-V_{ds}}{V_T} \right) \right) \tag{3.18}$$

Where, n_m is the free electron density in weak inversion region and n_m is found by using the classical Boltzmann's equation and written as

$$n_m = \frac{n_i^2}{N_a} \exp\left(\frac{\phi_{\min}(z)}{V_T}\right) \tag{3.19}$$

Where, n_i is the intrinsic carrier concentration of the silicon channel, V_T is the thermal voltage and

$$\phi_{s\min}(z) = \phi_{01\min} + (\beta - \phi_{01\min})\lambda_1^2 y^2 \tag{3.20}$$

Where,

$$\beta = V_{gs} - V_{fb} \tag{3.21}$$

D_n ,Is the diffusion constant and $N_{DS} = 1\times10^{20}\,\text{cm}^{-3}$, the drain/source doping density. By integrating Eq. (3.18) over the entire silicon body, we have got the Subthreshold current and it is written as

$$I_D = \int_{-\frac{t_{si}}{2}}^{\frac{t_{si}}{2}} \int_{-\frac{w}{2}}^{\frac{w}{2}} qD_n \frac{n_m}{L}\left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right) dydx \tag{3.22}$$

Using Eq. (3.19) for n_m in Eq. (3.22), we can write as,

$$I_D = qD_n \frac{n_i^2}{N_a L}\left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right) t_{si} \int_{-\frac{w}{2}}^{\frac{w}{2}} \exp\left(\frac{\phi_{s\min}(z)}{V_T}\right) dy \tag{3.23}$$

From Eq. (3.20) and Eq. (3.23), the Subthreshold current is written as

$$I_D = D \int_{-\frac{w}{2}}^{\frac{w}{2}} \exp\left[\left(\frac{\beta - \phi_{01\min}}{V_T}\right)\lambda_1^2 y^2\right] dy \tag{3.24}$$

Where,

$$D = qD_n \frac{n_i^2}{N_a L}\left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right) t_{si} \times \exp\left(\frac{\phi_{01\min}}{V_T}\right) \tag{3.25}$$

Using the trapezoidal rule of the numerical integration Eq. (3.24) can be written as

$$\begin{aligned} I_D = D\frac{t_{si}}{2m}\Bigg[\exp\left(\left(\frac{(\beta - \phi_{0\min})\lambda^2}{V_T}\right)\left(\frac{t_{si}}{2}\right)^2\right) + 2\sum_{k=1}^{m-1} \exp\left(\left(\frac{(\beta - \phi_{0\min})\lambda^2}{V_T}\right)\left(\frac{t_{si}}{2m}k\right)^2\right) \\ + \exp\left(\left(\frac{(\beta - \beta_{0\min})\lambda^2}{V_T}\right)\left(-\frac{t_{si}}{2}\right)^2\right)\Bigg] \end{aligned} \tag{3.26}$$

Where, 'm' is the number of linear sections between intervals $\left[-\frac{t_{si}}{2}, \frac{t_{si}}{2}\right]$. Considering $m = 1$ for better physical insight and simplicity, Eq. (3.26) can be written as

$$I_D = D t_{si} \exp\left(\left(\frac{(\beta - \phi_{01\min})\lambda_1^2}{V_T}\right)\left(\frac{w}{2}\right)^2\right) \tag{3.27}$$

By putting the value of the constant D from the Eq. (3.25) into Eq. (3.27), an alternative expression for Subthreshold current can be given by

$$I_D = \frac{qD_n n_i^2}{N_a L} t_{si}\left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right)\exp\left(\frac{\phi_{01\min}}{V_T}\right) w \exp\left(\left(\frac{V_{gs} - V_{fb} - \phi_{01\min}}{\lambda_1^2 V_T}\right)\left(\frac{w}{2}\right)^2\right) \tag{3.28}$$

3.5 Subthreshold Swing Model Derivation of double gate MOSFETs obtained by cutline BB'

The Subthreshold swing of any CMOS device is defined as the reciprocal of the slope of the Subthreshold characteristic curve representing the variation of $\log(I_D)$ as a function of the gate voltage V_G, where I_D is the drain current in the Subthreshold regime of operation of the MOS device. Thus, if S represents the Subthreshold swing of the DG MOSFET under consideration, we can write

$$S = \frac{dV_{gs}}{d\left(\log I_{ds}\right)} = \ln 10 \times \frac{dV_{gs}}{d\phi_{\min}} \frac{d\phi_{\min}}{dI_{ds}} I_{ds} \tag{3.29}$$

Where V_{gs} is the gate voltage, I_{ds} is the drain current, and $\phi_{\min}$ is the minimum surface potential, and the influence of interface trap charge is neglected. The Subthreshold slop is usually represented by the following classical expression.

$$S \approx \ln 10 \times V_T \times \left(\frac{\partial \phi_{\min}}{\partial V_{gs}} \right)^{-1} \tag{3.30}$$

Where, V_T is the thermal voltage in the normal atmospheric temperature.

From previous chapter we have find that the minimum surface potential is

$$\phi_{s\min} = \phi_{01}\left(z_{\min}\right)\left(1 - \lambda_1^2 \frac{w^2}{4}\right) + \left(V_{gs} - V_{fb}\right)\lambda_1^2 \frac{w^2}{4} \tag{3.31}$$

Where,

$$\phi_{01\min} = 2\sqrt{A_1 B_1} + \gamma \tag{3.32}$$

$$\frac{\partial \phi_{\min}}{\partial V_{gs}} = \left(1 - \lambda_1^2 y^2\right) \frac{\partial \phi_{01\min}}{\partial V_{gs}} + \lambda_1^2 y^2 \tag{3.33}$$

$$S = \ln 10 \times V_T \left[\left(1 - y^2 \lambda_1^2\right) \left(1 - \sqrt{\frac{B_1}{A_1}} \left(\frac{1 - e^{-\sqrt{2}\lambda_1 L}}{e^{\sqrt{2}\lambda_1 L} - e^{-\sqrt{2}\lambda_1 L}} \right) + \sqrt{\frac{A_1}{B_1}} \left(\frac{1 - e^{-\sqrt{2}\lambda_1 L}}{e^{\sqrt{2}\lambda_1 L} - e^{-\sqrt{2}\lambda_1 L}} \right) \right) + \lambda_1^2 y^2 \right] \tag{3.34}$$

Where λ_1, A_1 and B_1 are given in previous chapter.

First term in the above expression states that the Subthreshold slope is $60 to 70 mV / decade$ for a long channel device. The latter term is due to the short channel effect.

3.6 Results and Discussion

In this section, the results of the analytical model of uniformly doped DG MOSFETs are compare with the numerical simulation results getting from the 2-D device simulation tool. The modeling done with the assumption of identical top and bottom gate structure with the same oxide thicknesses and tungsten is used as a electrode material for both top and bottom gates of the device which is already discussed in the last chapter. The schematic diagram of DG MOSFET used for simulation is same as Fig. (3) in the previous chapter.

Fig. (12) plots the Subthreshold swing variation against the device channel length (*L*) for three different channel thickness (t_{si}). The plots shows that for thicker silicon films, the Subthreshold slop is more and for thinner the Subthreshold slop is less . The enhanced short-channel effects results in the increase in the Subthreshold swing, (*S*), of the device. It reveals that the degradation of subthreshold slop due to DIBL effect can be alleviated by the use of the thin silicon film.

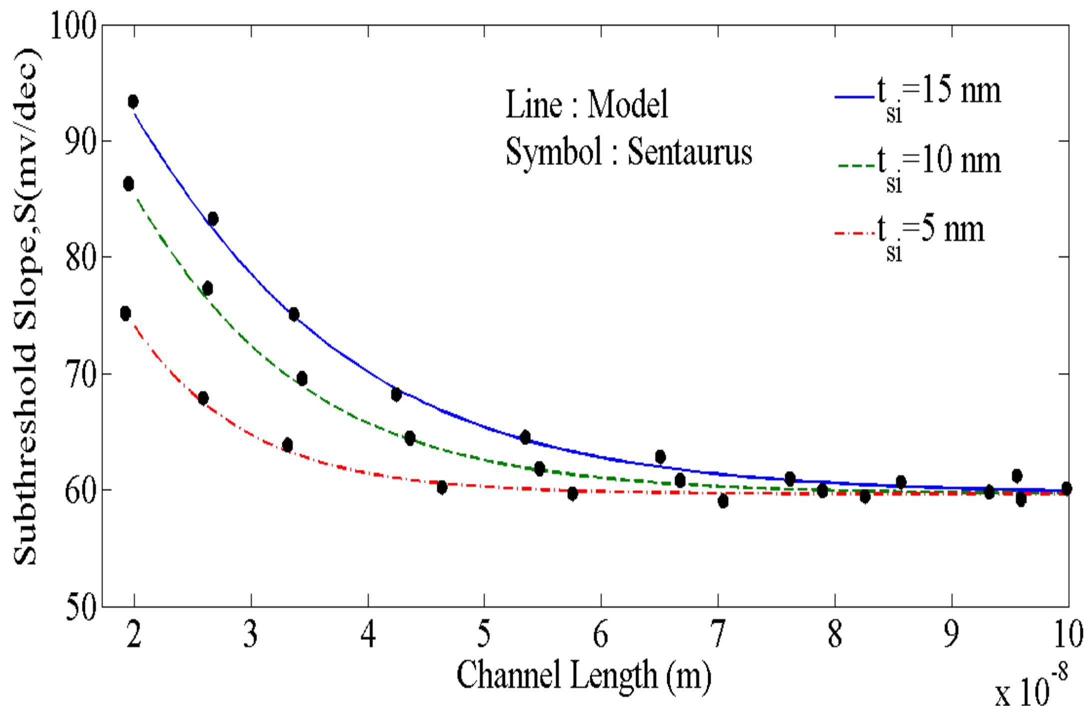

Figure 12 Subthreshold swing variation against the device channel length (L) for different channel thickness. Parameter used are tox=3nm, Vds=0.05 V ,Vgs=0 V .

On the other hand the subthreshold slop is also reduced by using small thickness of oxide. Fig. (13) shows variation of subthreshold slop as a function of device channel length for different gate oxide thickness and it shows the good agreement with the result found by numerical simulator. It also shows that the switching characteristics of the DG MOSFETs are declined very quickly with the decrease in channel length and increase in the gate oxide thickness provided other parameters of the devices remain unchanged.

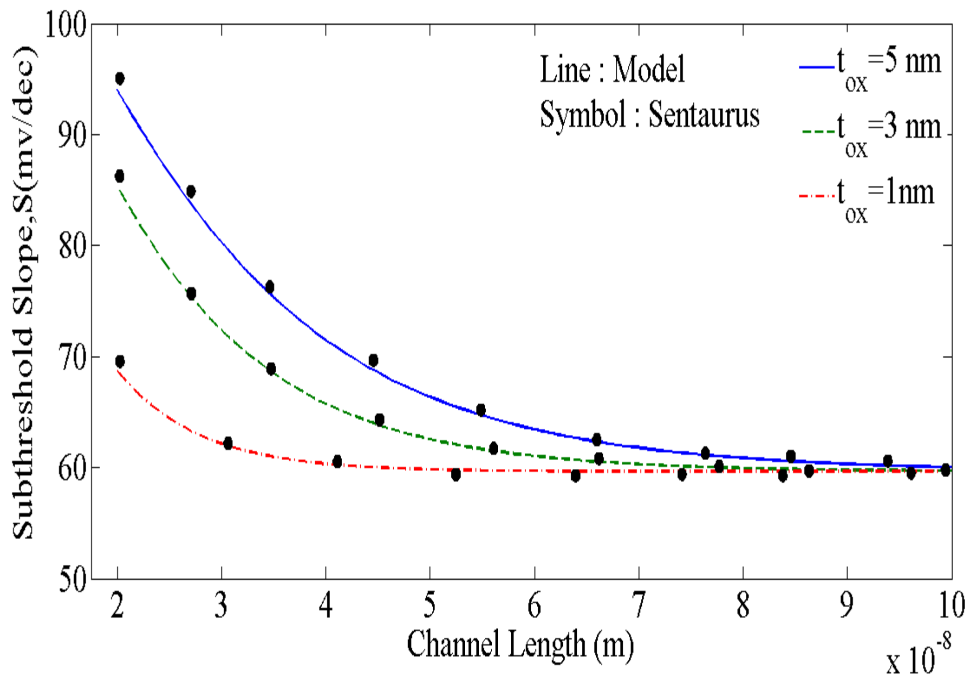

Figure 13 distribution of Subthreshold-swing variation against the device channel length (L) for different oxide thickness. Parameter used are tsi=10nm, Vds=0.05 V Vgs=0 V .

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The deterioration of the switching characteristics with the increase in the oxide thickness is due to fact that thicker gate oxides increased the gate capacitance due to this the electric field in the channel region thereby reducing the control gates over the channel and increasing the value of the subthreshold swing (*S*) of the device. Fig (14) presents the subthreshold swing variation with the doping concentration. subthreshold swing (*S*) value found to be decrease with the increasing channel doping due to reduced SCEs. It is also found that the double gate MOSFET reduces DIBL effects and keep swing of 60 decade/mV with long channel. Fig. 4.5 shows variation of

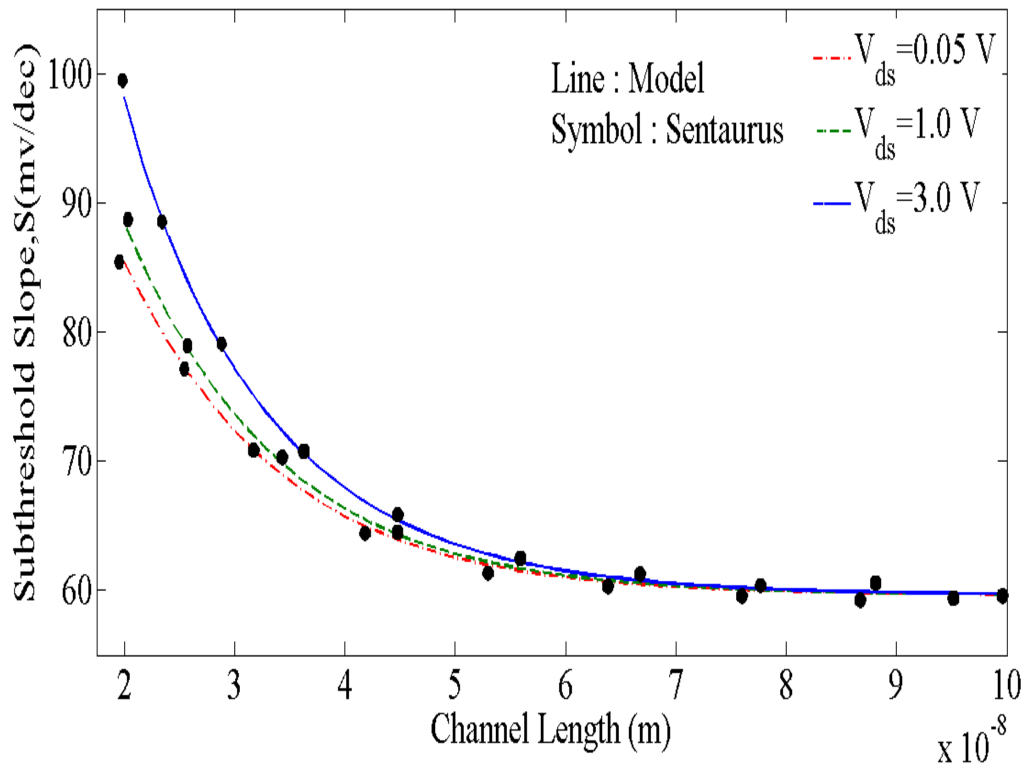

Figure 14 Subthreshold swing variation against the device channel length (L) for different biasing voltage . Parameter used are tsi=10nm, tox=3nm Vgs=0 V .

Subthreshold slop as a function of device channel length for different drain biasing and it is it shows the good agreement with the result found by numerical simulator. From fig it is clear that when drain voltage changes from o.o5 to 3V the Subthreshold slop value will not changes quickly until the channel length is scaled down to 40 nm.

Chapter 4

Modeling and Simulation of Channel Potential &Threshold Voltage Characteristics

4.1 Introduction

We have developed the analytical model of threshold voltage and Subthreshold slope in chapter-2 and in chapter-3 for DG-MOSFETs. Hence for getting the analytical model for Threshold voltage and Subthreshold slop of quadruple gate MOSFETs ,we can use the above developed model of DG-MOSFETs. By using perimeter-weighted-sum approach, an analytical model of quadruple gate MOSFETs is developed.

A schematic view of the three dimensional quadruple gate MOSFETs is shown in Fig(1) where W is the channel width, t_{si} is the silicon body thickness, and L is the cannel length. All four sides of the gate is surrounded with metal with a gate oxide thickness t_{ox}. Channel length is doped with acceptor concentration $N_a = 1\times10^{20} cm^{-3}$. To adjust the threshold voltage ,we have used metal for gate electrode with a proper work function .To avoid solving for $3-D$ Poisson equation that is too difficult to be derived, the $3-D$ quadruple gate device can be replaced by two $2-D$ equivalent symmetric double gate structure. To simplify the mathematical analysis for $3-D$ quadruple gate MOSFETs we consider that the device is consist of two independent double gate MOSFETs which is shown in figure.

4.2 3-D Generalized Potential Model

Due to fact that the leakiest path will be in the middle of the channel width as well as middle of the channel thickness for the quadruple gate device, the $3-D$ center potential of the device can be equivalently decomposed into two $2-D$ central potential for both symmetrical double gate device.

In chapter -3 the analytical potential model for both the $2-D$ symmetrical device is developed. By using the perimeter weighted sum method the analytical potential of the quadruple gate is expressed as

$$\phi(x,y,z)=\phi(x,z)\times\alpha+\phi(y,z)\times(1-\alpha) \tag{4.1}$$

Where,

$$\alpha=\frac{w}{w+t_{si}} \tag{4.2}$$

Where $\phi(x,y,z)$,is the analytical potential for quadruple gate device is, $\phi(x,z)$ is the analytical potential for symmetrical double gate MOSFETs shown in fig which is obtained from the quadruple gate structure, when cut line is taken along AA'. $\phi(y,z)$, is the analytical potential for symmetrical double gate MOSFETs shown in fig which is obtained by taking the cut line along BB'.and α is the ratio of symmetrical double gate MOSFETs device to the entire quadruple gate MOSFETs.

4.3 Threshold Voltage Roll-off Model

In order to determine the threshold voltage roll-off of the quadruple gate MOSFETs, numerical simulation have shown that the superposition principle cannot be applied in two separate Structures. Instead of using the superposition principal ,we have used the perimeter weighted sum method to get the threshold voltage roll off of quadruple gate MOSFETs and it is given as

$$\Delta V_{th}(x,y,z)=\Delta V_{th}(x,z)\times\alpha+\Delta V_{th}(y,z)\times(1-\alpha) \tag{4.3}$$

Where $\Delta V_{th}(x,y,z)$ is the threshold voltage roll-off of quadruple gate MOSFETs, $\Delta V_{th}(x,z)$ is the threshold voltage roll-off of symmetrical double gate MOSFETs shown in fig, which is obtained from the quadruple gate structure, when cut line is taken along AA'. $\Delta V_{th}(y,z)$, is the threshold voltage roll-off of symmetrical double gate MOSFETs shown in fig which is obtained

by taking the cut line along $BB^{'}$ and α is the ratio of symmetrical double gate MOSFETs device to the entire quadruple gate MOSFETs.

4.4 Subthreshold Current and Subthreshold slope Model

By using the perimeter weighted sum method, the subthreshold current of quadrature MOSFETs is easily obtained with the help of subthreshold current of symmetrical double gate MOSFETs which is given in previous chapter and it is given as

$$S_{QD} = S_{DG} \times \alpha + S_{DG} \times (1-\alpha) \tag{4.4}$$

Where S_{QD} the subthreshold current for is quadruple gate and S_{DG} is the Subthreshold current for symmetrical double gate which is shown by fig. And S_{DG} is Subthreshold current for symmetrical double gate which is shown in fig. 1.1. .

4.5 Result and discussion

Fig. (15) shows the variation of center potential with the channel length position .We get a good agreement between analytical model results with the numerical simulator results.

From fig (15) it can be noted that source channel barrier height at channel center is lower than that of the surface and hence the threshold voltage should be calculated by using the center potential minima. Fig. (16) shows the variation of surface potential with the channel length position for different channel thickness and we get a good agreement between analytical model results with the numerical simulator results. From Fig**.** (16), it is observed that the source to channel barrier increases with decreasing the channel thickness .when the channel thickness is decreases the control of gate on the channel is increases because the electric field in vertical direction is increased and hence potential of channel is also increases. We get a good agreement between analytical model results with the numerical simulator results.

Fig. (17) shows the variation of surface potential with the channel length position for different oxide thickness. We get a good agreement between analytical model results with the numerical simulator results. From Fig**.** (17), it is observed that the source to channel barrier increases when the thickness of the oxide layer is decreases.

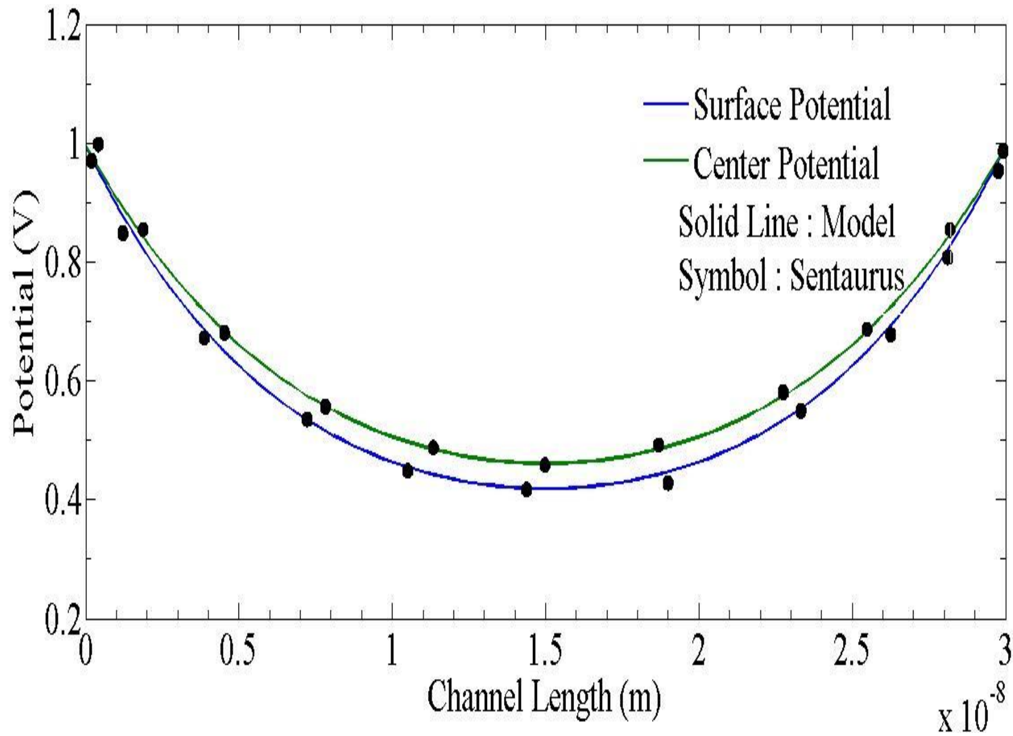

Figure 15 Potential distribution variation along the channel length. Parameter used are, tsi=10 nm, w=10nm ,Vds=0 V Vgs=0 V .

When the oxide thickness is decreases the control of gate on the channel is increases because the electric field in vertical direction is increased and hence potential of channel is also increases. But the carrier in channel may have got the enough energy and it penetrate the oxide layer and these trap charge may be degrade the threshold voltage. So we cannot decrease the oxide thickness too much. We get a good agreement between analytical model results with the numerical simulator results.

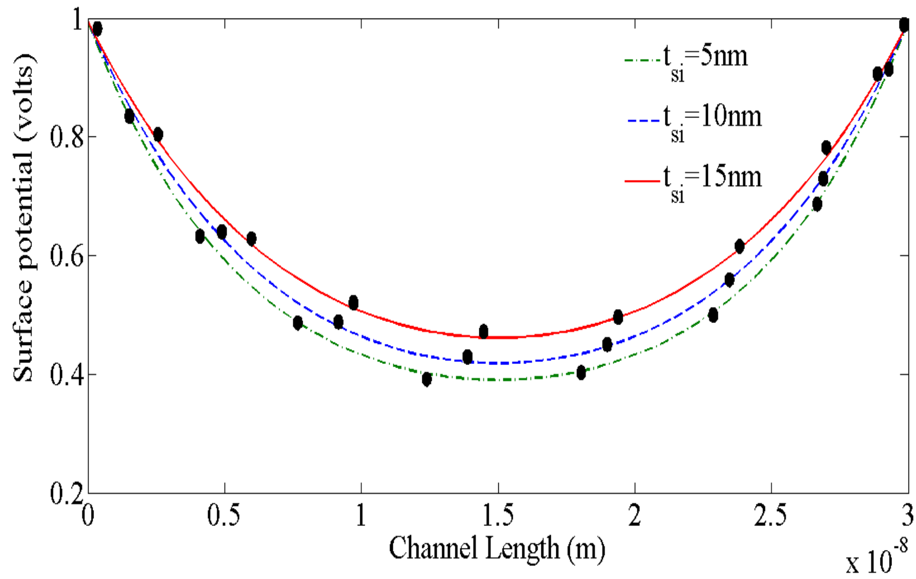

Figure 16 Channel Potential distribution variation along the channel length for different channel thickness. Parameter used are t_{ox}=3 nm, w=10 nm,Vds=0 V Vgs=0 V

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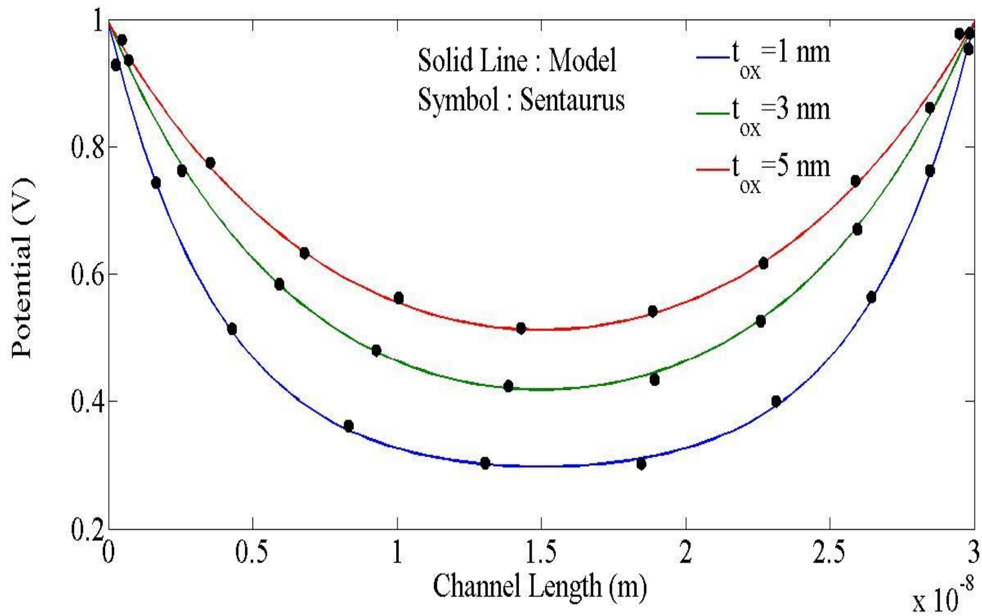

Figure 17 Surface Potential distribution variation along the channel length for different thickness of oxide. Parameter used are tsi=10 nm, w=10 nm,Vds=0 V Vgs=0 V

Fig (18) Shows the distribution of threshold voltage roll-off along the channel length for different thickness of gate-oxide. It is clearly shown in the figure that the threshold voltage roll-off increases when the channel length decreases, mainly when thickness of gate oxide is increased to 5 nm. This shows that the controllability of gate is gradually decreases inside the channel, which prevents the vertical electric field. We cannot reduce the oxide thickness too much ,due to very low oxide thickness the tunneling of carrier from the silicon and oxide interface may occurs and hence tunneling current will occur. For example, if the thickness of oxide reduced to 3 nm [30], quantum mechanical effects will arise and it degrades the performance of the model.

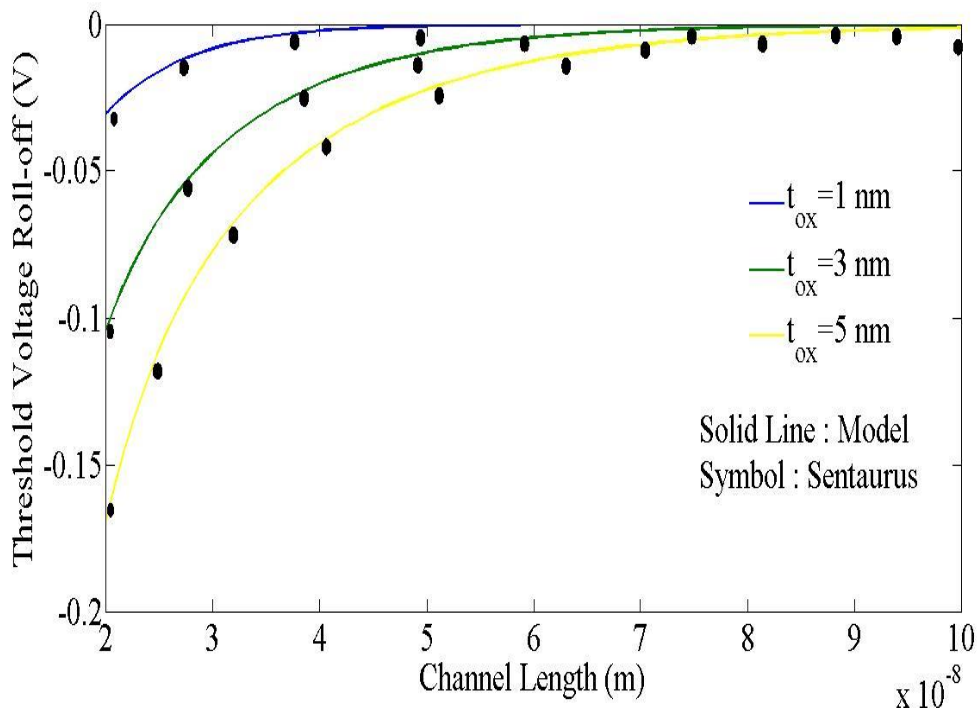

Figure 18 degradetion of threshold voltage along the channel length for different thickness of oxide. Parameter used are t_{si}=10 nm, w=10 nm,Vds=0 V Vgs=0 V

Fig (19) shows the threshold voltage roll off distribution along the channel length for different thickness of gate-oxide. As opposed to the gate oxide, the large channel width is preferred to suppress short channel effect when channel length L is increased. Although the large channel width is required to resist the short channel effect, it will increase the area of the active device and can make it difficult to be used in the tight packing density budget for manufacturing ULSI.

Another efficient method to improve the degradation of threshold voltage that is to make the silicon film thickness thinner as shown in fig.(19).

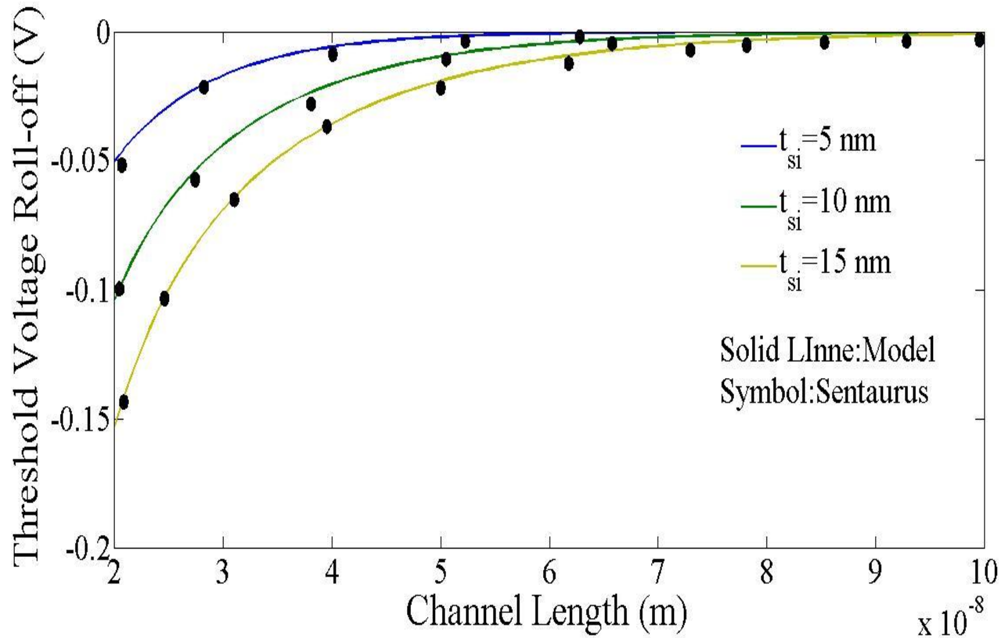

Figure 19 Variation of threshold voltage roll-off with channel length for different channel thickness. Parameter used are tox=3 nm, w=10 nm,Vds=0.05 V Vgs=0 V

Fig (20) shows the distibution of threshold-voltage roll-off along the channel length for various drain biasing. We have found that the threshold-voltage roll-off decreases with the channel length decreases, particularly when the drain biased is increased to 1v. This is happen due to the larger drain bias following the short channel length can greatly initiate DIBL and degrade the threshold behavior.

Fig. (21) shows the analytical solution of the Subthreshold slope for quadruple gate MOSFETs compared with 3D numerical simulation results with the silicon thickness as a varied parameter, and good agreements are obtained. The plot indicates that the thinner silicon film thickness has the smaller Subthreshold slope due to the DIBL effect alleviated by the use of thin silicon film.

Moreover, the subthreshold swing can also be substantially reduced by making use of thinner gate insulator. Fig (22) shows the dependency of subthreshold slope on the channel length with the gate oxide thickness as a variable parameter. To suppress the short channel effect more efficiently, much thinner oxides are preferred. Due to thinner oxide thickness, the vertical field in

the channel is increased and hence the gate controllability increased which reduces the Subthreshold degradation.

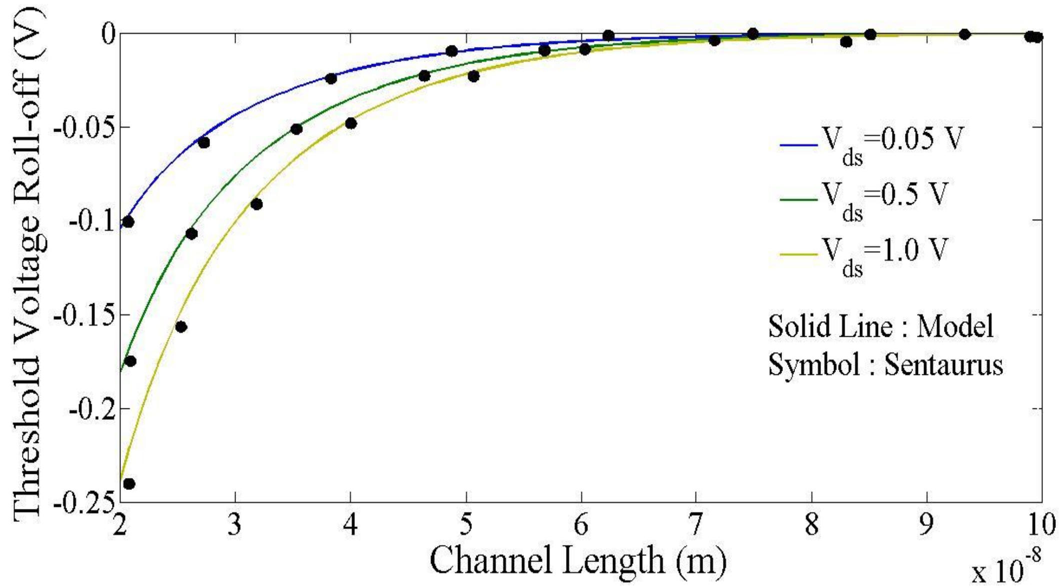

Figure 20 Distribution of threshold voltage roll-off with channel length for different biasing voltage. Parameter used are tox=3 nm, tsi=10nm,w=10 nm, Vgs=0 V

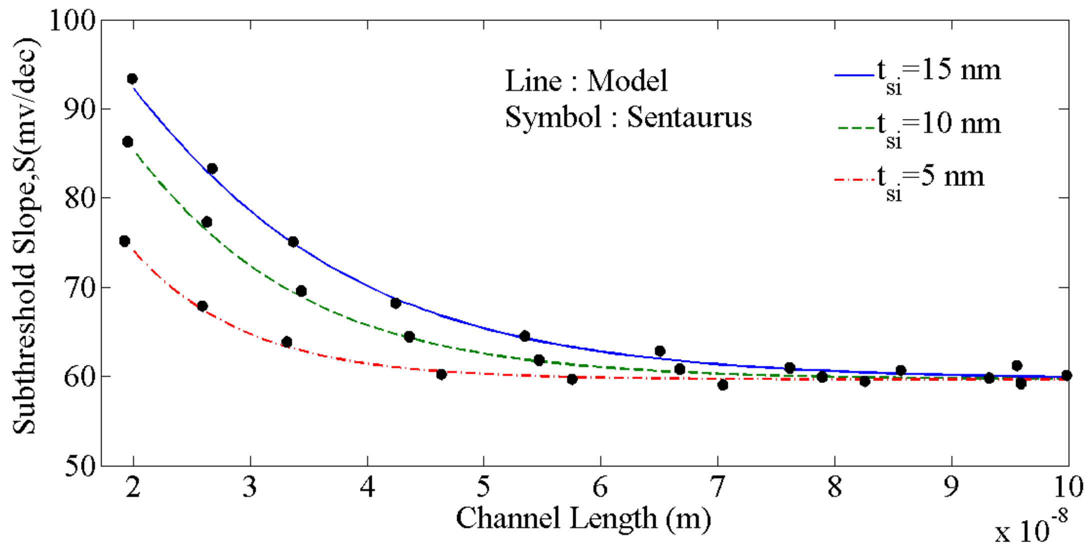

Figure 21 Distribution of Subthreshold slope with channel length for different channel thickness. Parameter used are tox=3 nm, w=10 nm, Vgs=0 V, Vds=0.05 V

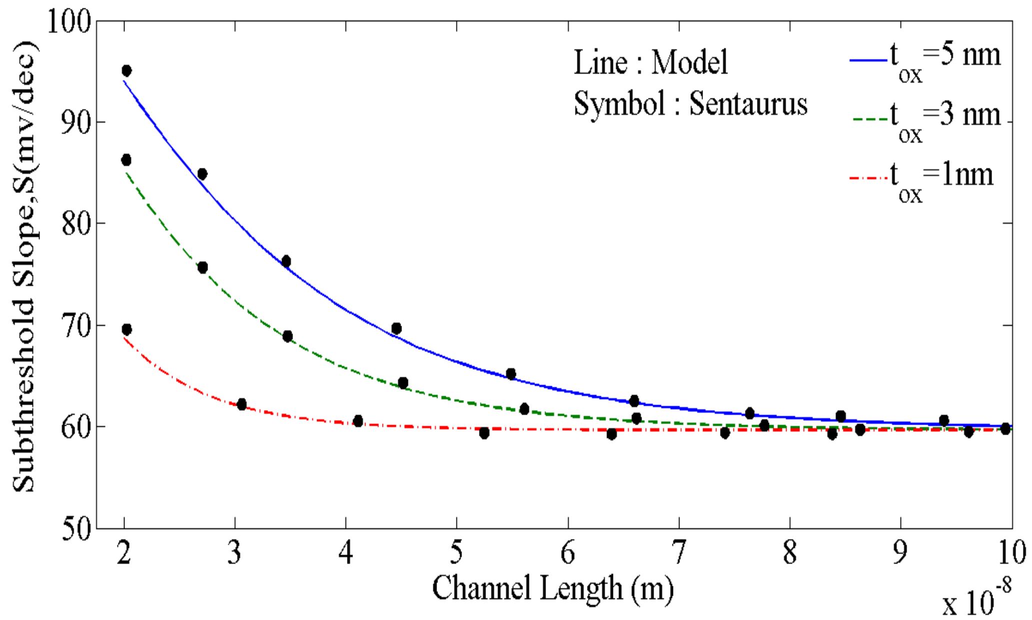

Figure 22 Variation of Subthreshold slope with variation of channel length when thickness of oxide changed. Parameter used are tsi=10 nm, w=10 nm, Vgs=0 V, Vds=0.05 V

Fig.(23) shows the analytical solution of the Subthreshold slope for quadruple gate MOSFETs compared with 3D numerical simulation results with the oxide thickness as a varied parameter, and good agreements are obtained. The plot indicates that the narrow oxide provide the more efficient suppression on short channel effects for the proposed device, which gives small Subthreshold-slope degradation. As a result the narrow width channel account as a key parameter, we can consider it for design the model for the Subthreshold operation.

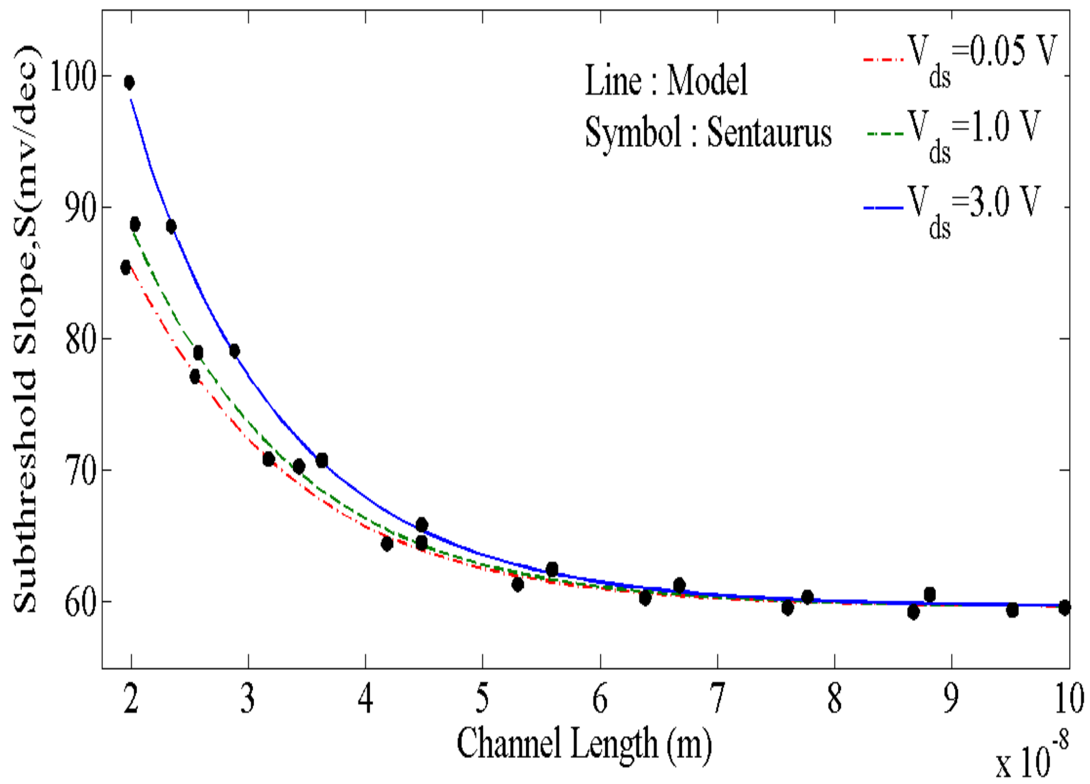

Figure 23 Variation of Subthreshold slope with channel length for different oxide thickness. Parameter used are tsi=10 nm, w=10 nm, Vgs=0 V, Vds=0.05 V

Chapter 5

Conclusion and Future Scope of Work

5.1 Introduction

The objective of this dissertation is to present a detailed theoretical and simulation based study of the threshold voltage, Subthreshold slope characteristics of short-channel Quadruple gate MOSFETs with a constant doping profile of the device. The present chapter has been devoted to summarize and conclude the major observations presented in the previous chapter of this dissertation. Since research is a continuous process of learning, we have also tried to outline some scopes of future works related to the area considered in this Dissertation.

5.2 Summary and Conclusion

Chapter-1 is devoted to discuss some general aspects of CMOS technology, CMOS scaling and double-gate CMOS structures. It is discussed that the dimension of conventional MOS transistors fabricated on a bulk silicon substrate has attained their physical limit owing to incessant technology scaling of CMOS devices. In view of the above, various CMOS device scaling issues as well as different novel non-classical CMOS structures for maintaining the desired pace with the current–edge technology trend has been discussed in this chapter. The various aspects of multi-gate MOS structure in general and Quadruple gate MOSFET in particular, has been presented in this chapter. With respect to the conventional single gate bulk CMOS transistor structures, the Quadruple gate MOSFETs are observed to be having (i) better control on the short channel effects because of their device geometry; (ii) ultimate potential for future technology scaling due to improved short-channel effects; (iii) better switching characteristics (iv) better on state drive current (which is nearly double of drain current of the single-gate gate device). The purpose of studying the Quadruple gate MOS devices in the Dissertation is thus clearly well justified. Finally, the scope of the dissertation has been outlined at the end of the chapter.

Chapter-2 presents an analytical modeling and simulation of the 2D potential distribution and threshold voltage of short-channel DG MOSFETs. The channel region is assumed to be Undoped. The parabolic mode analysis has been employed to determine the surface potential by the solving the 2D Poisson's equation in the channel region. Thus the obtained 2D surface potential is further utilized in defining the virtual cathode which represents the minimum surface potential along the channel. The important observations inferred from this chapter can be summarized as, the device surface potential minimum (the maximum channel barrier height) and therefore the threshold voltage is found to be a strong function of the channel thickness as well as oxide thickness. All the results have been found from analytical result is matched with device simulator Sentaurus.

Chapter-3 deals with modeling and simulation of Subthreshold-drain current and Subthreshold-swing of symmetric DG MOSFETs. It is assumed that diffusion is the dominant current flowing mechanism in subthreshold regime of device operation. The major points of this chapter can be outlined as follows.(i) the chapter presents an analytical modeling of the effective conduction path parameters of the two channels under two gates of the DG MOS device. All the results have been found from analytical result is matched with device simulator Sentaurus.

Chapter-4 deals with the analytical modeling and simulation of threshold voltage, Subthreshold-swing and Subthreshold-current of short-channel symmetric Quadruple gate MOSFETs with constant substrate doping. For modeling, we used two symmetrical double gate MOSFETs ,in place of actual Quadruple gate MOSFETs, and individual double gate MOSFET is modeled and then by using weighted parameter sum method we have find the actual model of quadruple gate MOSFETs.The effects of the doping and other device parameters like channel thickness and channel width on the subthreshold swing and subthreshold current are investigated in details. All the results have been certified with the Numerical simulation results getting from the commercially software Sentaurus.

5.3 Future Scope of Work

This dissertation is intended to present the theoretical modeling of the threshold voltage, sub-threshold slope and sub-threshold current of the Quadruple gate MOSFETs with a constant doping concenteration in the body. However, there are a few complicated issues which can be taken up as the future works. Some possible future woks may be described as follows.

a) A capacitance model of short-channel Quadruple gate MOSFETs could be very useful for many researchers working in the related areas.
b) An extensive study of Quadruple gate MOSFETs for analog and RF applications can be carried out.
c) At nanoscale (below 25nm gate length), the study of Quantum Mechanical Effects on Quadruple gate MOSFET becomes necessary.

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Publication List

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