Modeling & Performance Enhancement Analysis of Some Nanoscale MOSFET Structures

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Modeling & Performance Enhancement Analysis of Some Nanoscale MOSFET Structures

A dissertation submitted in partial fulfillment of the
requirement for the degree of

Master of Technology (Research)

by

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Dedicated

To

MY LOVING PARENTS AND MY BROTHER

Declaration

I certify that

- The work contained in this thesis is original and has been done by me under the guidance of my supervisor (s).
- The work has not been submitted to any other Institute for the award of any other degree or diploma.
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Rourkela, July 2013

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C E R T I F I C A T E

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Contents

List of Abbreviations

Abbreviation	Description
ITRS	International Technology Roadmap for Semiconductors
CMOS	Complementary Metal-Oxide Semiconductor
FET	Field Effect Transistor
SOI	Silicon on Insulator
FD-S-SOI	Fully Depleted Strained Silicon on Insulator
DG MOSFET	Double Gate Metal-Oxide Semiconductor Field Effect Transistor
SS	Sub-threshold Slope
DIBL	Drain Induced Barrier Lowering
EOT	Equivalent Oxide Thickness
SCEs	Short Channel Effects
GS	Gate Stack
FD-S-GS-DG	Fully Depleted Strained Gate Stack Double Gate
2-D	Two Dimensional
SiGe	Silicon Germanium
TFP	Silicon Germanium
GTFP	Gain Transconductance Frequency Product
GFP	Gain Frequency Product
FOM	Figure of Merits
TGF	Transconductance Generation Factor

List of Symbols

Symbols	Description
V_{th} or V_T	Threshold Voltage
V_{GS} or V_{gs}	Gate to Source Voltage
V_{DS} or V_{ds}	Drain to Source Voltage
I_{ds} or I_D	Drain Current
t_{ox} or T_{ox}	Gate-Oxide Thickness
t_b	Buried Oxide Thickness
L_g or L	Channel Length
W	Channel Width
N_A	Acceptor Doping Concentration
N_D	Donor Doping Concentration
t_{Si} or T_{Si}	Silicon Body Thickness
ε_{Si}	Permittivity of Silicon
ε_{ox}	Permittivity of Oxide
N_{Sub}	Substrate Doping
I_{on}	On-State Drive Current
I_{off}	Off-State Leakage Current
g_m	Transconductance
g_d	Output Conductance
E_v	Early Voltage
A_V	Intrinsic Gain
C_{gs}	Gate to Source Capacitance
C_{gd}	Gate to Drain Capacitance
f_T	Cut-off Frequency

C_T	Total Internal Capacitance
ϕ_M	Metal Work Function
ϕ_{Si}	Silicon Work Function
V_{bi}	Built-in Potential
X	Germanium Mole Fraction
$t_{s\text{-}Si}$	Strained Silicon Thickness
E_C	Electron Affinity
E_G	Energy Band Gap
η	Body Factor
SiO_2	Silicon Dioxide
Si_3N_4	Silicon Nitride
HfO_2	Hafnium Oxide
Ta_2O_5	Tantalum Pentoxide
TiO_2	Titanium Dioxide
T_K	Thickness of High-k Dielectric
φ_S	Surface Potential
v_{Sat}	Saturation Velocity
V_{FB}	Flat Band Voltage
η_i	Intrinsic Carrier Concentration

List of Useful Constants with their Values

Constants	Values
Electronic Charge (q)	$1.6 * 10^{-19}$ Coulomb
Electron Mass (m)	$9.1 * 10^{-31}$ Kg
Permeability of Vacuum (μ_0)	$4\pi * 10^{-7}$ H/m
Permittivity of Vacuum (ε_0)	$8.85 * 10^{-12}$ F/m
Boltzmann Constant (k_B)	$1.38 * 10^{-23}$ J/K
Permittivity of Silicon (ε_{Si})	11.68
Permittivity of SiO_2 (ε_{SiO2})	3.9
Permittivity of Si_3N_4 (ε_{Si3N4})	7.5
Permittivity of HfO_2 (ε_{HfO2})	24
Permittivity of Ta_2O_5 (ε_{Ta2O5})	30
Permittivity of TiO_2 (ε_{TiO2})	40
Room Temperature (T)	300 K
Thermal Voltage (V_T)	26 mV
Intrinsic Carrier Concentration (η_i)	$1.45 * 10^{10}$ cm^{-3}

List of Figures

List of Tables

Abstract

Silicon-on-Insulator (SOI) has been the forerunner of the CMOS technology in the last few decades offering superior CMOS devices with higher speed, higher density and reduced second order effects for submicron VLSI applications. Recent experimental studies invigorated interest in Fully Depleted (FD) SOI devices because of their potentially superior scalability relative to bulk silicon CMOS devices. Various new structures with different engineering concepts have been reported to reduce the SCEs in SOI platform. Among them Strain engineering and high-k gate dielectric with metal gate technology are very popular for enhancing the carrier mobility and reduction of gate leakage current.

In this thesis, first physics based 2-D model for surface potential, threshold voltage and electric field for a Fully Depleted Strained Silicon on Insulator (FD-S-SOI) MOSFET by solving the two dimensional Poisson's equation is presented. The model details the role of various MOS parameters like germanium concentration, body doping concentration, strained silicon thickness, oxide thickness and gate metal work function influencing the surface potential, threshold voltage and electric field. Then extensive numerical simulation is done to study the effect of device design engineering on the analog/RF performance of nanoscale DGMOSFET by varying the gate work function, channel length and gate oxide. Including the Short Channel Effects (SCEs) the important analog/RF figures of merit (FOMs) are also examined.

Finally one optimum device is presented with great immunization to SCEs and highly applicable to analog/RF applications.

Chapter 1

Challenges & Possible Solutions for Nanoscale Devices: A Review

1. 1. Introduction

The central component of semiconductor electronics is the integrated circuit (IC), which combines the basic elements of electronic circuits – such as transistors, diodes, capacitors, resistors and inductors on one semiconductor substrate. The two most important elements of silicon electronics are transistors and memory devices. For logic applications MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) are also used. [1]

The semiconductor industry has showcased a spectacular exponential growth in the number of transistors per integrated circuit for several decades, as predicted by Moore's law. The future technology trend predicted by ITRS (International Technology Roadmap for Semiconductors), physical dimensions and electrostatic limitations faced by conventional process and fabrication technologies will require the dimensional scaling of complementary metal-oxide-semiconductor (CMOS) devices within the next decade. To enable future technology scaling, new device structures for next-generation technology have been proposed. Some of the new technologies are Silicon On Insulator (SOI), Strained Silicon (S-Si) at the channel, inclusion of high-k dielectric materials in gate oxide and Multi gate MOSFETs. Many of these devices have been shown to have favorable device properties and new device characteristics, and require new fabrication techniques. These nanoscale devices have a significant potential to revolutionize the fabrication and integration of electronic systems and scale beyond the perceived scaling limitations of traditional CMOS. [2-3]

1.2. CMOS

Complementary Metal Oxide Semiconductor (CMOS) technology now a day is the backbone of the semiconductor industry worldwide and the enabler of the impressive number of

electronic applications that continue to revolutionize our daily life. The pace of growth of CMOS technology in the last 40 years is the key to success of CMOS technology and to the extraordinary scalability of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET).

MOSFETs are the building blocks of microprocessors, memory chips and telecommunications microcircuits. A modern microprocessor can contain more than 2 billion MOSFETs, and a 32-gigabyte memory card weighing only 0.5 g contains a staggering 256 billion transistors, which is comparable to the number of stars in the Milky Way. MOSFETs are mainly used as switches in logic microcircuits, although they can fulfill other purposes.

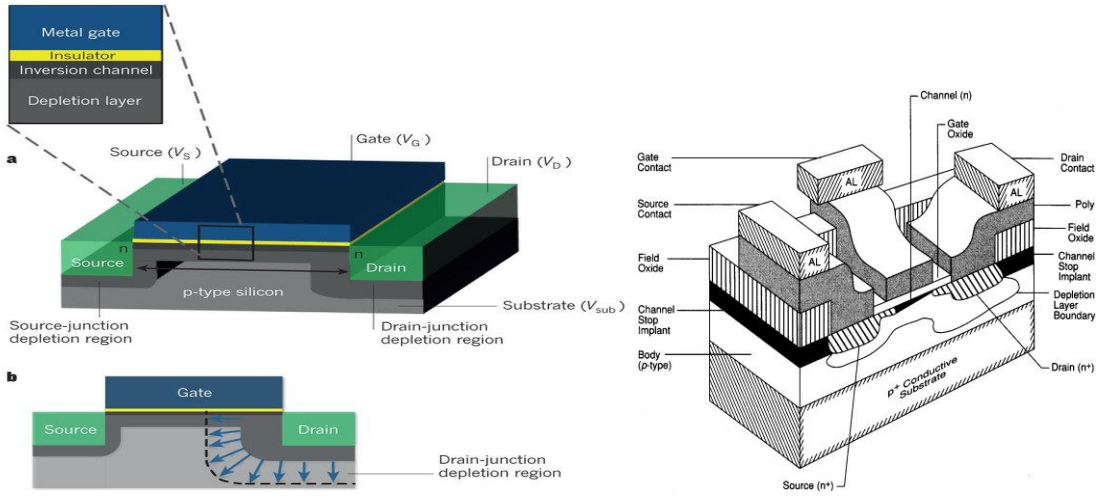

Figure 1.1 A schematic view of a classical bulk n-channel MOSFET. [4]

The device consists of two n-type semiconductor regions called the source and the drain, which are separated by a region of p-type semiconductor called the substrate. This description is for an n-channel MOSFET, or NMOS device. A p-type MOSFET, or PMOS device, would have the opposite doping in the source, drain and substrate regions. Typically, the semiconductor is silicon, although other semiconductor materials, with faster charge carriers, are being considered by the microelectronics industry. A thin layer of insulating material such as silicon dioxide covers the region between the source and the drain, and this layer is topped by a metal electrode called the gate. The insulator is referred to as the gate oxide. Under typical bias conditions, the source and the p-type substrate are grounded, and a positive voltage is applied to the drain. Under these conditions, the drain p–n junction is reverse biased and no current flows between the

drain and the substrate. Because the bias across the source p–n junction is zero, there is also no current flowing from the substrate to the source. As a result, there is no current flow between the source and the drain, and the transistor is turned off, playing the part of an open switch. If a large enough positive voltage is applied to the gate, then electrons 'spill out' of the n-type semiconductor source and drain regions, forming an electron-rich layer, called the channel, underneath the gate oxide. The channel forms a continuous electron bridge between the source and the drain, and current can flow between these two electrodes. The transistor is then turned on and behaves as a closed switch. Underneath the electron-rich channel is a region in which holes, which are the charge carriers in p-type semiconductors, have been repulsed and swept away by the positive voltage that has been applied to the gate. [4]

1.2.1. Requirements for Future Technology Nodes

For logic technologies, one usually distinguishes between several technology options:

- High performance (HP)
- Low operating power (LOP)
- Low stand-by power (LSTP).

High performance logic corresponds to high complexity integrated circuits that require high clock frequencies and can deal with high power consumption, such as for example microprocessor units for desktop computers. This intrinsic switching time τ is the time needed by a transistor supplying on-state current to make the gate of an identical transistor switching from the ground to the supply voltage:

$$\tau = C*V/ I \qquad (1.1)$$

with C the gate capacitance, V the supply voltage and I the on-state current of the device.The most efficient way to increase the performance is to scale aggressively the gate length of the transistor, since it allows reducing the gate capacitance while increasing the on-state current.

Low operating power technology option aims at relatively high performance mobile applications, such as notebook computers. The key issue is then to increase the circuit performance while reducing the power consumption as much as possible when the circuit is operating. At the device level, a relevant metric of this dynamic power consumption is the power-delay product, corresponding to the energy required for a single transistor switch. This power-delay product is simply:

$$P*\tau = C*V^2 \quad (1.2)$$

Where C is the gate capacitance and V is the supply voltage. The most efficient way to decrease the dynamic power consumption is thus reduce the supply voltage as far as possible.

Finally, low standby power option is used for lower performance, low cost consumer applications, such as cellular phones. For such applications, the main concern is to continue increasing performance while maintaining the power consumption as low as possible when the integrated circuit is idle. At the transistor level, this static power consumption is directly governed by the leakage current of the devices. Thus, this technology option requires very low transistor off-state currents, as well as very low parasitic currents (such as gate leakage). [5]

1.3. Reasons for MOSFET scaling

Smaller MOSFETs are desirable for several reasons. The main reason to make transistors smaller is to pack more and more devices in a given chip area. This results in a chip with the same functionality in a smaller area, or chips with more functionality in the same area. Since fabrication costs for a semiconductor wafer are relatively fixed, the cost per integrated circuits is mainly related to the number of chips that can be produced per wafer. Hence, smaller ICs allow more chips per wafer, reducing the price per chip. In fact, over the past 40 years the number of transistors per chip has been doubled every 2–3 years once a new technology node is introduced. For example the number of MOSFETs in a microprocessor fabricated in a 45 nm technology is twice as many as in a 65 nm chip. [5]

1.3.1. Scaling

It is desirable to scale the vertical as well as the lateral dimensions when decreasing the device sizes. The scaling affects both reliability and performance specifications of the process

- Constant field scaling strategy
  - ✓ Vertical dimension decreases with same lateral dimensions.
  - ✓ To maintain fixed electric field, operating voltage decreases.
- Constant voltage scaling strategy
  - ✓ Attractive due to electrical compatibility with existing circuit
  - ✓ Vertical dimensions decreases quadratically relative to the lateral dimensions.

Table1.1 MOS Scaling Theory [6]

Parameter	Symbol	Constant Field Scaling	Constant Voltage Scaling
Gate Length	L	1/α	1/α
Gate Width	W	1/α	1/α
Electric Field	E	1	α
Oxide Thickness	Tox	1/α	1/α
Substrate Doping	Na	α2	α2
Gate Capacitance	Cg	1/α	1/α
Oxide Capacitance	Cox	α	α
Voltage	V	1/α	1
Current	I	1/α	α
Power	P	1/α2	α

So a trade-off among performance, yield, and compatibility with existing technology, reliability, process complexity, device performance and impact of parasitic must be made when selecting a scaling strategy. [6-7]

1.4. MOS scaling theory

1.4.1. Moore's Law

It was the realization of scaling theory and its usage in practice which has made possible the better-known as "Moore's Law." Moore's Law is a phenomenological observation that the number of transistors on integrated circuits doubles every two years, as shown in Figure 1. It is intuitive that Moore's Law cannot be sustained forever. However, predictions of size reduction limits due to material or design constraints, or even the pace of size reduction, have proven to elude the most insightful scientists. The predicted 'limit' has been dropping at nearly the same rate as the size of the transistors.

Further technology scaling requires major changes in many areas, including: 1) improved lithography techniques and non-optical exposure technologies; 2) improved transistor design to achieve higher performance with smaller dimensions; 3) migration from current bulk CMOS devices to novel materials and structures, including silicon-on-insulator, strained Si and novel dielectric materials; 4) circuit sensitivity to soft errors from radiation; 5) smaller wiring for on-

chip interconnection of the circuits; 6) stable circuits; 7) more productive design automation tools; 8) denser memory cells, and 9) manageable capital costs. Metal gate and high-k gate dielectrics were introduced into production in 2007 to maintain technology scaling trends [5].

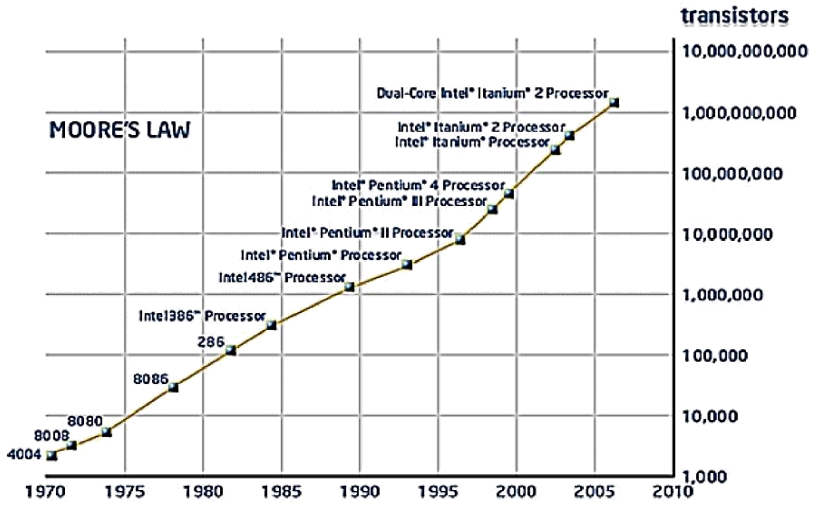

Figure 1.2 Moore's Law [5]

In addition, packaging technology need to progress at a rate consistent with the on-going CMOS technology scaling at sustainable cost/performance levels. This requires advances in I/O density, bandwidth, power distribution, and heat extraction. System architecture will also be required to maximize the performance gains achieved in advanced CMOS and packaging technologies.

1.4.2. Obstacles to Miniaturization of MOSFET's

Despite challenges, however, many of those in the research community and industry do conventional microelectronic transistors becoming miniaturized into the nanometer-scale regime. For example, the International Technology Roadmap for Semiconductors(ITRS) [3], published by the Semiconductor Industry Association, projects that chips will be made from transistors with major features (gate lengths) of 70 nm in the year 2010 Individual working transistors with 40 nm gate lengths have already been demonstrated in silicon. Transistors with gate lengths as small as 25 nm have been made using Strained Silicon (S-Si). [8]

However, to provide nanoelectronic devices with scaled-down MOSFET's, a few of the obstacles are below,

• **High electric fields**, due to a bias voltage being applied over very short distances, can cause "avalanche breakdown" by knocking large numbers of electrons out of the semiconductor at high energies, thus causing current surges and progressive damage to devices , This may remain a problem in nanoelectronic devices made from bulk semiconductors.

• **Heat dissipation** of transistors (and other switching devices), due to their necessarily limited thermodynamic efficiency, limits their density in circuits, since overheating can cause them to malfunction. This is likely to be a problem for any type of densely packed nanodevices.

• **Vanishing bulk properties** and non-uniformity of doped semiconductors on small scales. This can only be overcome either by not doping at all (accumulating electrons purely using gates, as has been demonstrated in a GaAs heterostructure) or by making the dopant atoms form a regular array. Molecular nanoelectronics is one path to the latter option.

• **Shrinkage of depletion regions** until they are too thin to prevent quantum mechanical tunneling of electrons from source to drain when the device supposedly is turned off. The function of nanoelectronic devices is not similarly impaired, because it depends on such tunneling of electrons through barriers. • Shrinkage and unevenness of the thin oxide layer beneath the gate that prevents electrons from leaking out of the gate to the drain. This leakage through thin spots in the oxide also involves electron tunneling. [9]

Long ago, MOSFETs were big and could be described via drift currents and carrier control via the gate capacitance. Now MOSFETs are small in order to increase their operation speed. Pushing the dimensions of the gate length down influences the electrostatics of the devices. In order to preserve the electrostatic integrity of the MOSFET scaling has proceeded in a controlled way:

$L_g\downarrow$ has to go together with $t_{ox}\downarrow$, $N_A\uparrow$, $t_j\downarrow$, $V_{DD}\downarrow$ and $W\downarrow$

But reducing these geometrical parameters not only increases fabrication complexity but also changes the physical processes in the device.

A MOSFET device is considered to be short when the channel length is the same order of magnitude as the depletion-layer widths (x_{dD}, x_{dS}) of the source and drain junction. As the channel length L is reduced to increase both the operating speed and the number of components per chip, the so-called short-channel effects arise.

1.5. Short-Channel Effects

The short-channel effects are attributed to two physical phenomena:

- The limitation imposed on electron drift characteristics in the channel,
- The modification of the threshold voltage due to the shortening channel length.

In particular five different short-channel effects can be distinguished: [5], [6], [10]

- Drain-induced barrier lowering and Punch through
- Surface scattering
- Velocity saturation
- Impact ionization
- Hot electrons
- Sub-threshold leakage current

1.5.1. Drain Induced Barrier Lowering and Punch Through

The expressions for the drain and source junction widths are:

$$X_{dD} = \sqrt{\left(\frac{2\varepsilon_{Si}}{qN_A}\right)\left(V_{DS} + \varphi_{Si} + V_{SB}\right)} \qquad \text{and} \qquad X_{dS} = \sqrt{\left(\frac{2\varepsilon_{Si}}{qN_A}\right)\left(\varphi_{Si} + V_{DB}\right)} \tag{1.3}$$

Where V_{SB} and V_{DB} are source-to-body and drain-to-body voltages. When the depletion regions surrounding the drain extends to the source, so that the two depletion layer merge (i.e., when $x_{dS} + x_{dD} = L$), punchthrough occurs. Punchthrough can be minimized with thinner oxides, larger substrate doping, shallower junctions, and obviously with longer channels. The current flow in the channel depends on creating and sustaining an inversion layer on the surface. If the gate bias voltage is not sufficient to invert the surface i.e. $V_{GS}<V_T$ (where V_T is the threshold voltage of the device), the carriers (electrons) in the channel face a potential barrier that blocks the flow. Increasing the gate voltage reduces this potential barrier and, eventually, allows the flow of carriers under the influence of the channel electric field. In small-geometry MOSFETs, the potential barrier is controlled by both the gate-to-source voltage V_{GS} and the drain-to-source voltage V_{DS}. If the drain voltage is increased, the potential barrier in the channel decreases, leading to drain-induced barrier lowering (DIBL). The reduction of the potential barrier eventually allows electron flow between the source and the drain, even if the gate-to-source

voltage is lower than the threshold voltage. The channel current that flows under this conditions ($V_{GS}<V_T$) is called the sub-threshold current.

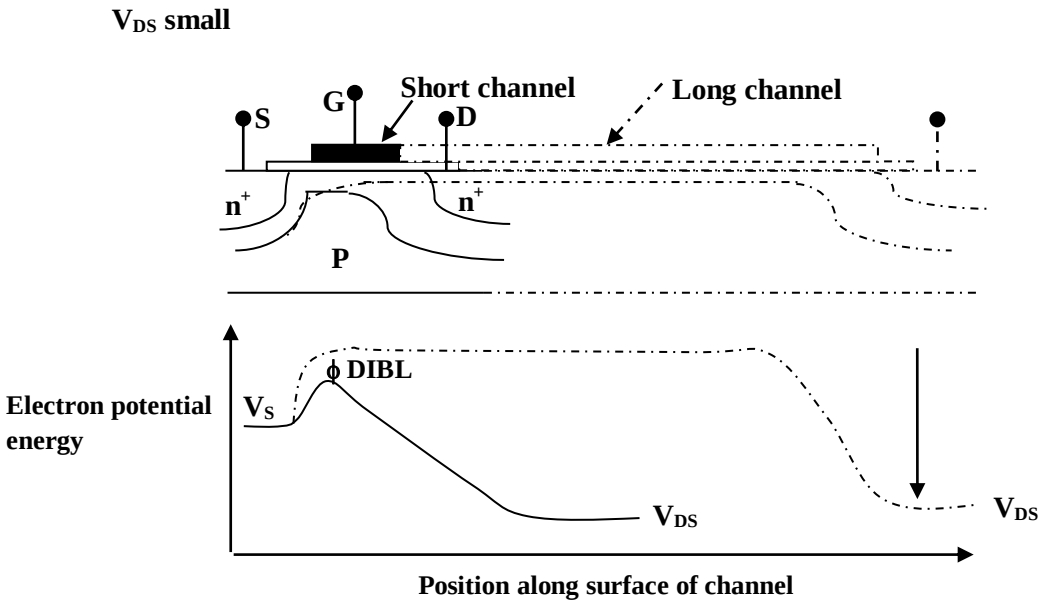

Figure 1.3 Electron Potential Energy Variations along the position in channel [6]

1.5.2. Surface Scattering

As the channel length becomes smaller due to the lateral extension of the depletion layer into the channel region, the longitudinal electric field component E_y increases, and the surface mobility becomes field-dependent.

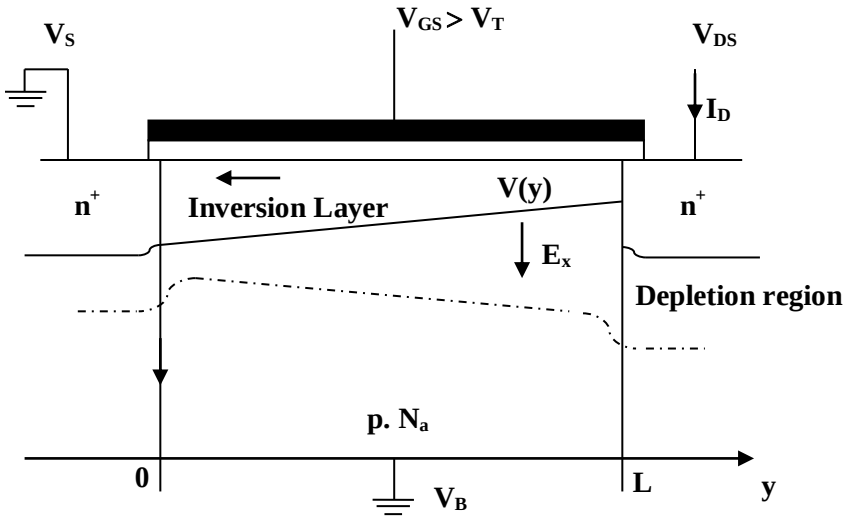

Figure 1.4 Electron Potential Energy Variations along the position in channel [6]

Since the carrier transport in a MOSFET is confined within the narrow inversion layer, and the surface scattering (that is the collisions suffered by the electrons that are accelerated toward the interface by E_x) causes reduction of the mobility, the electrons move with great difficulty parallel to the interface, so that the average surface mobility, even for small values of E_y, is about half as much as that of the bulk mobility.

1.5.3. Velocity Saturation

When the channel length is decreased, the electric field increases .The resulting high electric field affects the device parameters. In terms of the drain of the drain current under normal current device operation, the most significant effect that needs to be included is an effective reduction of mobility with increasing longitudinal field. Let E_x be the value of the longitudinal field component. We have assumed that all the points in the inversion layer $|E_x|$ is small enough so that the magnitude of the carrier velocity $|V_d|$ is proportional to $|E_x|$, In devices with small channel lengths this assumption is not accurate, and the I_{ds} -V_{ds} relation is not valid. The velocity of the carriers in the inversion layer tends to saturate at high $|E_x|$ values. The effects arising due to the lack of proportionality between $|V_d|$ and $|E_x|$ on device characteristics are often referred to as velocity saturation effects.

$$E_c = \frac{|V_d|max}{\mu} \tag{1.4}$$

In some treatments, the same value of $|V_d|_{max}$ is used for both electrons and holes ($5*10^6$ to $2*10^7$ cm/s), which results in E_c values of about $8*10^3$ to $3*10^4$ V/cm for electrons and $2*10^4$ to 10^5 V/cm for holes.

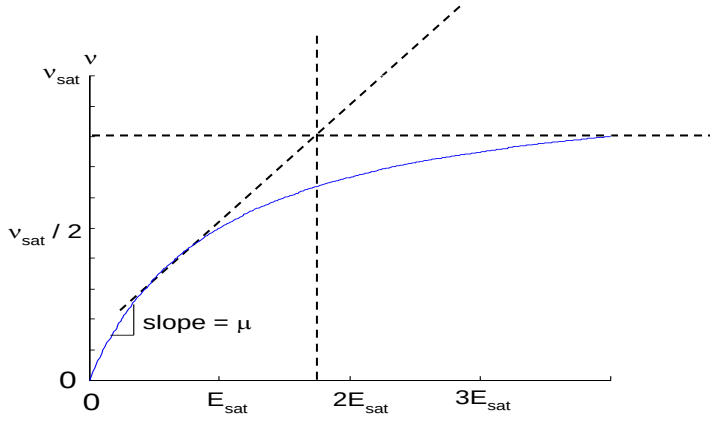

Figure 1.5 Variation of Drift Velocity and Electric Field [11]

1.5.4. Impact Ionization

Another undesirable short-channel effect, especially in NMOS, occurs due to the high velocity of electrons in presence of high longitudinal fields that can generate electron-hole (e-h) pairs by impact ionization, that is, by impacting on silicon atoms and ionizing them.

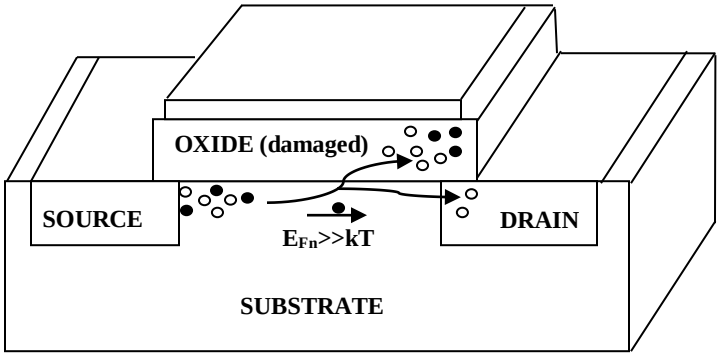

Figure 1.6 Electrons entering into oxide region [6]

It happens as follow: normally, most of the electrons are attracted by the drain, while the holes enter the substrate to form part of the parasitic substrate current. Moreover, the region between the source and the drain can act like the base of an npn transistor, with the source playing the role of the emitter and the drain that of the collector. If the aforementioned holes are collected by the source, and the corresponding hole current creates a voltage drop in the substrate material of the order of .6V, the normally reversed-biased substrate-source pn junction will conduct appreciably resulting in injection of the electrons from the source to the substrate, similar to the injection of electrons from the emitter to the base. These electrons can then enough energy as they travel toward the drain to create new electron-hole pairs. The situation can worsen if some electrons generated due to high fields escape the drain field to travel into the substrate, thereby affecting other devices on a chip.

1.5.5. Hot Electrons

Another problem, related to high electric fields, is caused by so-called hot electrons. These high energy electrons can enter the oxide, where they can be trapped, giving rise to oxide charging that can accumulate with time and degrade the device performance by increasing V_T and affect adversely the gate control on the drain current.

During the last decades transistors dimensions were scaled down, but not the power supply.

- The resulting increase in the electric field strength causes an increase in energy of the electrons.
- Some electrons are able to leave the silicon and tunnel into the gate oxide.
- Such electrons are called “Hot carriers”.
- Electrons trapped in the oxide change the V_T of the transistors.
- This leads to a long term reliability problem.
- For an electron to become hot, an electric field of the order of 10^4 V/cm is necessary.
- This condition can be easily met with channel lengths below 1μm.

1.5.6. Sub-threshold leakage current:

The Sub-threshold leakage current is the weak inversion conduction current, which is dominated by the diffusion current flowing between the drain and source when $|V_{GS}| < |V_{th}|$. It is considered as one of the non-ideal characteristics of MOSFET as a switching device and contributes major portions of the standby leakage power dissipation. This weak inversion conduction current can be expressed based on the Eq. (1.5), [12]

$$I_{subth} = \mu C_{dep} \left(\frac{W}{L}\right) V_T^2 \left(\exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right)\right)\left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right) \tag{1.5}$$

Where $C_{dep} = \sqrt{\varepsilon_{Si} q N_{sub} / 4\varphi_B}$ denotes the capacitance of the depletion region under the gate region under the gate area, V_T is the thermal voltage which equals to kT/q, and n is sub-threshold parameter and expressed as $1 + C_{dep} / C_{ox}$

Since from Eq. (1), I_{subth} increases exponentially with increasing V_{GS} and decreasing V_{th}. The partial derivative of $\log_{10} I_{subth}$ with respect to V_{GS} yields a constant slope called sub-threshold slope (SS) and equals to

$$SS = \left[\frac{\partial \log_{10}(I_{subth})}{\partial V_{GS}}\right]^{-1} \tag{1.6}$$

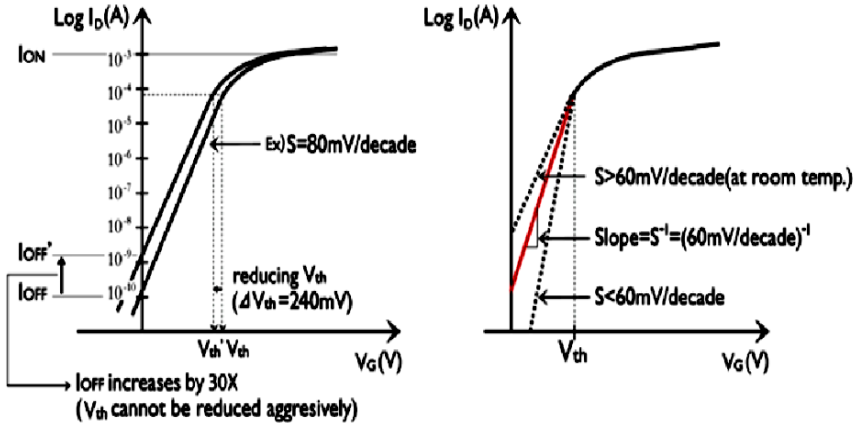

Figure 1.7 Characteristics of sub-threshold conduction [13]

This parameter shows how abruptly the transistor turns off with decreasing gate voltage. In order to turn off the transistor effectively, SS must be designed to be as small as possible. Fig. 1.7 shows that SS is always greater than 2.3 V_T (~60 mV/dec) at room temperature and shows how well the channel surface potential can be controlled by the gate contact. SS can be made smaller (close to ~60 mV/dec) by using a thinner gate oxide thickness (resulting in larger Cox) or a lower substrate doping concentration (resulting in the larger depletion width beneath the channel, hence reduced C_{dep}). In addition, under low temperature operation, SS can be reduced since SS is a function of T. For MOS a transistor built on SOI technology, the sub-threshold swing is usually better than in bulk technology. In fact, the sub-threshold swing of SOI devices can even reach the optimum value (2.3 V_T) depending on whether their bulk is fully depleted or partially depleted. This makes SOI a promising candidate for ultra-low-power CMOS applications though a lot of improvements to the current process technologies still have to be made until this new technique can be applied to commercial products on a large scale. [12], [14]

1.6. The modification of the threshold voltage due to SCEs

The equation giving the threshold voltage at zero-bias is accurate in describing large MOS transistors, but it collapses when applied to small-geometry MOSFETs.

$$V_T = V_{FB} + \varphi_0 + \gamma\sqrt{\varphi_0 + V_{SB}} \qquad \text{----------For long channel} \qquad (1.7)$$

$$V'_T = V_{FB} + \varphi_0 + \gamma\frac{Q'_B}{Q_B}\sqrt{\varphi_0 + V_{SB}} \qquad \text{----------For short channel} \qquad (1.8)$$

$$V'_T = V_T + \Delta V_{TL} \quad \text{where} \tag{1.9}$$

$$\Delta V_{TL} = -(1 - \frac{Q'_B}{Q_B})\gamma\sqrt{\varphi_0 + V_{SB}} \tag{1.10}$$

In fact that equation assumes that the bulk depletion charge is only due to the electric field created by the gate voltage, while the depletion charge near n+ source and drain region is actually induced by p-n junction band bending. Therefore, the amount of bulk charge the gate voltage supports is overestimated, leading to a larger V_T than the actual value.

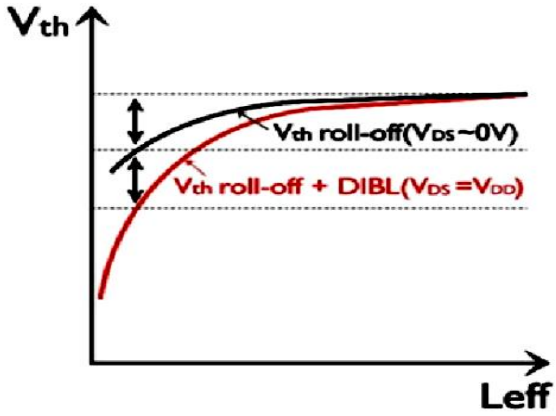

Figure 1.8 Threshold voltage roll-off and DIBL [13]

The transistors with a different channel length (L) on the same wafer, even in the same die, yield different V_{th}. The threshold voltage reduction due to the reduced channel length represents V_{th} roll-off. Further V_{th} reduction caused by increasing drain voltage describes DIBL as shown in Fig. 1.8. The electric flux lines generated by the charge on the MOS capacitor gate electrode terminate on the induced mobile carriers in the depletion region just under the gate. For short-channel MOSFETs, on the other hand, some of the field lines originating from the source and the drain electrodes terminate on charges in the channel region. Thus, less gate voltage is required to cause inversion. This implies that the fraction of the bulk depletion charge originating from the p-n junction depletion and hence requires no gate voltage to be subtracted from the V_T expression [10-11].

1.7. To Overcome the SCEs

To overcome all the short channel effects several innovative techniques have been introduced. These are

- High-k Dielectric Material Gate
- Silicon On Insulator (SOI) Structure
- Strained Silicon Technique (S-Si) Structures

1.7.1. High-k + Metal Gate Benefits

The dielectric constant, k, is a parameter defining ability of material to store charge. Consequently, it also defines capacitance, C of any capacitor comprising of a layer of dielectric sandwiched between two metal plates. In the figure below size of the upper plate defines area of the capacitor contact (A).

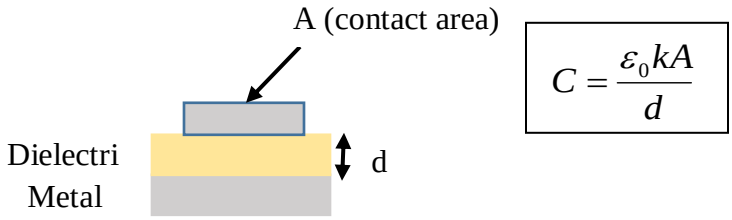

Figure 1.9 High-k + Metal Gate [15]

All other parameters equal, k would determine capacitance of the above structure, or in other words, it would define the extent of capacitive coupling between two conducting plates – with high-k dielectric such coupling would be strong, and with low-k dielectric being obviously weak. In Si technology, the reference value of k is taken that of silicon dioxide, SiO2, which is 3.9. Dielectrics featuring k>3.9 are referred to as high-k dielectric while dielectric featuring k<3.9 are defined as low-k dielectrics. In cutting edge silicon nanoelectronics both high-k and low-k dielectrics are needed to implement fully functional very high-density integrated circuit, although, for drastically different reasons. High-k dielectrics are needed in MOS gate stacks to maintain sufficiently high capacitance of the metal (gate) - dielectric-Si structure in MOS/CMOS transistors. Due to the continued scaling of the channel length (L), and hence reduced gate area A, the need to maintain sufficient capacitance of the MOS gate stack was met by gradual decrease of the thickness of SiO_2 gate oxide.

Obviously such scaling cannot continue indefinitely as at certain point gate oxide will become so thin (thinner than about 1 nm) that, due to excessive tunneling current, it would stop playing role of an insulator. Hence, dielectric featuring k higher than 3.9, i.e. one assuring same capacitive coupling but at the larger physical thickness of the film, must be used instead of SiO_2

as a gate dielectric in advanced MOS/CMOS integrated circuits. On the opposite end of the spectrum finds itself a multi-layer metallization scheme in which inter-layer-dielectric (ILD) is used to electrically insulate metal lines. In this case it is of critical importance that the capacitive coupling between adjacent interconnects lines is as limited as possible. Hence, a low-k dielectric must be used to assure as little capacitive coupling between interconnect lines as possible. Whether the problem is with high-k dielectrics for MOS gates or low-k dielectrics for ILDs, lack of viable technical solutions in either of these areas will bring any future progress in mainstream silicon technology. [15]

1.7.2. Silicon-on-Insulator (SOI)

With physical separation between individual devices in ultra-high density CMOS integrated circuits measured in nanometers, proper electrical isolation between them is a key challenge. The SOI substrate wafers, as opposed to conventional bulk wafers, not only solve the problem of electrical isolation between adjacent devices but also allow innovative device layouts resulting insignificantly better than in the case of bulk substrates performance of CMOS circuitry. Hence, SOI substrates rapidly became an important element of the advanced silicon IC technology.

The figure 1.10 shows cross-section of a bulk wafer in which individual devices (e.g. PMOSFETs and NMOSFETs in CMOS cell) are isolated by LOCOS isolation or shallow trench isolation (regions in red). By creating a substrate in which very thin layer of oxide is buried underneath the surface, superior isolation between devices is possible. It is accomplished by etching off Si between devices and refilling created narrow trenches with oxide. As a result, each among millions of devices comprising a circuit is literally embedded in the oxide.

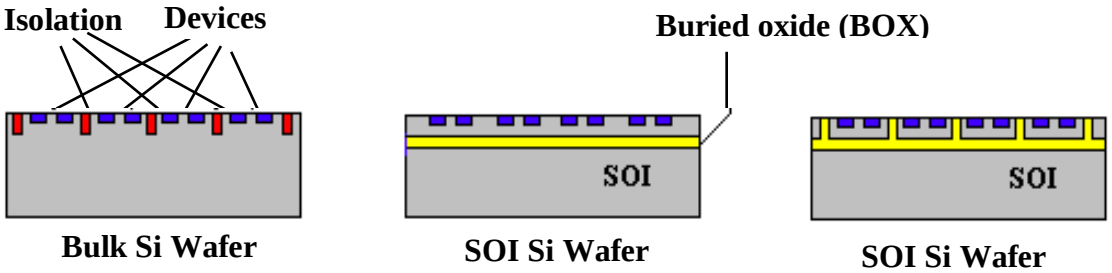

Figure 1.10 SOI wafers [15]

This not only eliminates leakage current between devices but also reduces parasitic capacitances associated with source and drain regions and results in the faster switching device.

Further improvement in the performance of CMOS circuit on SOI substrate can be accomplished by reducing thickness of the Si active layer, i.e. layer of Si on top of buried oxide. In the above figure same MOSFET structure is formed in the thicker and thinner active layer. In the latter case the layer is so thin that both source (S) and drain (D) regions, as well as channel, expand across the active layer to the buried oxide. Significant performance gains result from implementation of such Fully Depleted SOI (FD-SOI).

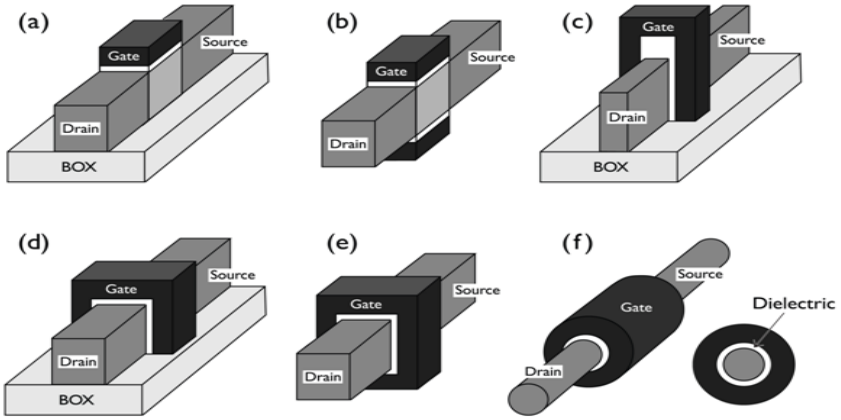

Figure 1.11 Various SOI device: (a) Single gate SOI transistor, (b) DG planar SOI transistor, (c) DG on-planar FinFET, (d) trigate FET, (e) quadruple-gate (or gate-all-around) FET, and gate-all around (or surrounding gate) FET (nanowire FET). [13]

Most notably leakage currents of source and drain junctions are drastically reduced. Hence, less power is dissipated into the substrate and premature destruction of device from overheating is prevented. Also, parasitic capacitances associated with source, drain and channel regions are essentially eliminated with increase in the device switching speed. Yet additional gain in performance of fully depleted SOI CMOS can be achieved by using strained silicon as an active layer on top of buried oxide. In this case channel is induced in the strained Si in which electrons feature higher mobility as compared to mobility in standard (relaxed) Si. This obviously leads to the faster switching CMOS cell. [13], [16]

1.7.3. Strained Semiconductor Films

The strain in crystalline solid is due to the relative displacement of atoms in the lattice. The strain creates proportional distortion of key material properties of semiconductor including energy gap and effective mass of an electron in the strained region is reduced, hence, its mobility

is increased. Consequently, creation of strain in the region of transistor in which mobility of electrons has an effect determining its performance will result in the faster switching transistor.

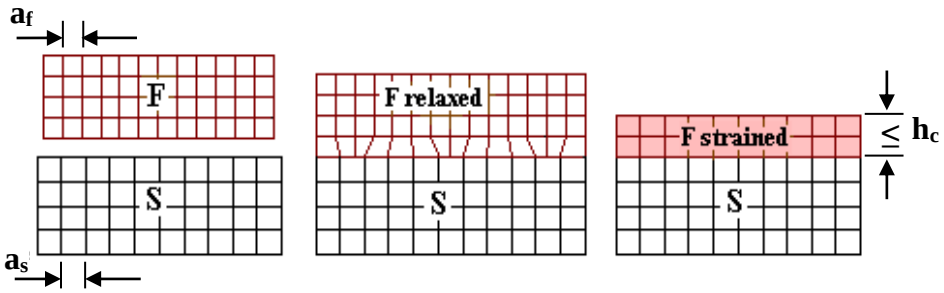

Figure 1.12 Formation of strain on Silicon wafer [17]

Due to the performance enhancing properties, the lattice-mismatched semiconductor heterostructures containing strained films are rapidly growing in importance in semiconductor device technology. To explain the concept of strained semiconductor films consider single crystal materials S and F featuring different lattice constants a_s and a_f. If S is a substrate upon which F is formed by epitaxial deposition this lattice mismatch will cause a build-up of the strain in the film as its thickness increases. Eventually, the strain energy will have to be completely or partially relieved by generation of dislocations at the interface (misfit dislocations). At this point, lattice constant of the film will relax toward the unstrained value. However, if the film growth will be stopped below critical thickness h_c, i.e. in the thickness regime in which lattice mismatch is still accommodated by strain in the film (such film is called a pseudomorphic film) then a defect-free, highly strained single-crystal F film will be formed on the substrate S. Critical thickness h_c decreases as the lattice mismatch f increases. In practical strained-layer heterostructures, the lattice mismatch typically does not exceed 5 % and typical thickness of the film ranges from 1 to 20 nm.

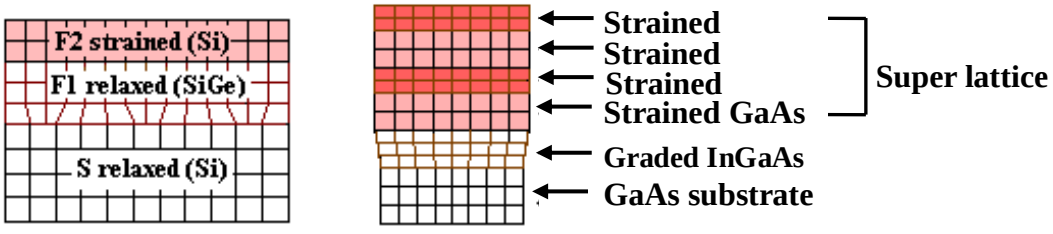

Figure 1.13 Formation of strain on various semiconductor surface [17]

As stated earlier strained films are used to enhance performance of both silicon- and GaAs-based transistors. Formation of the layer of strained silicon on silicon substrate requires a

buffer layer of SiGe as shown in the figure. Strained SiGe itself formed on Si substrate also finds applications in very high-frequency transistors manufacturing. In the case of GaAs-based devices strained films are incorporated in the device structure in the form of strained layer superlattices (SLS). The SLS structures display unusual properties that can be used to design high performance electronic (e.g. quantum well) and photonic (e.g. novel photo detectors and lasers) devices. As the figure shows SLS is a multilayer structure comprising of alternating epitaxial layers (formed on GaAs substrate) of two lattice mismatched materials each having a thickness below h_c (often AlGaAs is used in conjunction with GaAs). The key to the fabrication of super lattice is very precise (atomic scale) control of chemical composition and thickness of the film. Both are possible using Molecular Beam Epitaxy (MBE). [17-18]

1.8. Standard MOSFET models

Some semiconductor industry standard compact models, such as charge, potential and conductance based models are reviewed here. [19]

1.8.1. Charge based MOSFET model

The charge based modeling approach is one of the basic and primitive modeling approaches. It is based on the computation of the inversion charge density in the MOSFET channel in terms of the terminal voltages, i.e. gate and drain voltages. This model is a regional model because it explains the behavior of the MOSFET separately in all regions of its operation. So, these models require smoothing parameters, they are somewhat empirical in the interfacing regions and, thus the device is not described accurately.

The prominent charge based models are level 1, level 2, and level 3, BSIM 1, HSPICE level 28, BSIM 2, BSIM 3, BSIM 4, and BSIM 5. BSIM 5 is used for sub-100nm CMOS circuit simulation. This model is applicable to deep sub-micron region, and attempts have been made to include the modeling of strained silicon technology in the latest spice models. BSIM 4 considers the influence of stress of mobility, velocity saturation, threshold voltage, body effect and DIBL effect. But the equations expressed are mostly empirical and no analytical models have been given.

1.8.2. Potential based MOSFET model

This model approach is more accurate than the charge based models. It is based on the calculation of the potential in the channel of a MOSFET to determine the I-V and C-V characteristics. Some of the models based on the approach are SP models by penn-state university, USA, HISIM (Hiroshima-University, STARC IGFET model) valid down to sub-100nm MOSFETs. This model is applicable to the sub-micron region and attempts have been made to include the modelling of strained silicon technology.

1.8.3. Conductance based MOSFET model

This modeling approach is suitable for low power, short channel applications for analog design. It is known as the EKV (Enz-Krummenachar-Vittoz) model, which has been developed by the Swiss Federal Institute of Technology, Switzerland. This model keeps the substrate as the reference rather than the source, as observed in the potential based and charge based models. Due to its complexity, it is much less used for modeling purposes. Moreover, no stress modeling has been done in this model.

In all the approaches mentioned above, attempts have been made to model MOSFETs. But most of the models that have been proposed are either empirical in nature. Therefore, there is a need for a more physics based approach to accurately explain the behavior of the device.

1.9. Multi-gate MOSFET — the Future CMOS Transistor

1.9.1. Advantages of Multi-gate MOSFETs

The main advantage of the multi-gate devices is the improved short channel effects. Since the channel (body) is controlled electro statically by the gate from multiple sides, the channel is better-controlled by the gate than in the conventional transistor structure. Unwanted leakage components are reduced and a small transistor can be used to continue the cost reduction through miniaturization. Improved gate control also provides lower output conductance, i.e., smaller dI_{ds}/dV_{ds} in the current saturation region. This provides greater voltage gain, which is beneficial to analog circuits as well as to the noise tolerance of digital circuits.

A second advantage of the multi-gate devices is the improved on-state drive current (I_{on}) and therefore faster circuit speed. Ion improvement arises from several reasons [5]. Reduction of

channel doping reduces impurity Columbic scattering. Reduced channel doping reduces the electric field normal to the SiO_2 interface and therefore reduces the surface roughness scattering. Finally, a promising multi-gate structure, the FinFET, provides a larger channel width with a small footprint in area. This raises Ion, which is handy for driving a large capacitive load such as long interconnect.

A third advantage is the reduced manufacturing variation. In the absence of channel dopants, the effect of random dopant fluctuation (RDF) is minimized. Lower SRAM supply voltage for the FinFET multi-gate technology compared to traditional bulk MOSFET technology has been experimentally demonstrated [20]. The advantages of multi-gate devices are well known and demonstrated in many FinFET technologies.

1.9.2. Various Flavors of Multi-gate MOSFET

There are different flavors of multi-gate MOSFETs. Several examples are shown in Figure below. The FinFET consists of a thin silicon body (the fin) and a gate wrapping around its top and two sides. FinFETs can be made on either bulk or SOI substrates, creating the bulk FinFET or the SOI FinFETs. In some FinFET processes, the oxide hard mask on top of the fin is not removed, creating the double-gate FinFET. In double-gate FinFETs, the top surface of the fin does not conduct current, whereas in triple-gate FinFETs the side surfaces and the top surface all conduct current. Another example of multi-gate MOSFET is the all-around gate device. It consists of a pillar-like body surrounded by the gate dielectric and the gate. The nanowire MOSFET is one example of all-around gate devices. Depending on the fabrication process, the channel may be either vertically or horizontally oriented. Optionally, a FinFET can have two separate gates that are independently biased. This can be achieved by removing the top portion of the gate of a regular FinFET using chemical mechanical polishing, forming the independent double-gate FinFET. Independent double-gate MOSFETs may also be made as a planar device. The planar DG SOI is essentially a planar SOI MOSFET with a thin buried oxide (labeled as BOX).

A heavily-doped region in silicon under the buried oxide acts as the back-gate. Unlike the front-gate, the back-gate is primarily used for tuning the device threshold (V_{th}). The buried oxide is usually thick such that the back-gate cannot induce an inversion layer at the back surface. V_{th} tuning can be used to compensate for variability in IC manufacturing from chip to chip or even

circuit to circuit within the same chip. Doing so improves the IC speed and power consumption. It can also be used to dynamically rise or lower V_{th} circuit by circuit within a chip in response to the need for less leakage or more speed. This is a very effective means of managing power consumption. [4]

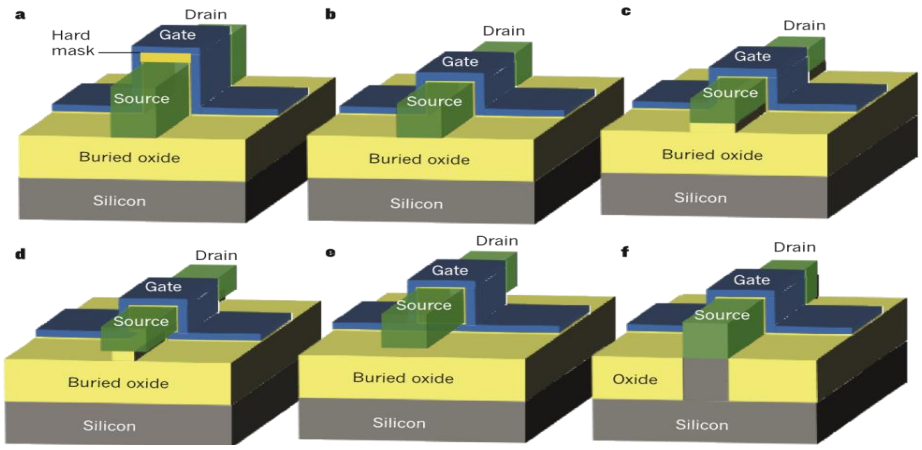

Figure 1.14 Types of multigate MOSFET. The different ways in which the gate electrode can be wrapped around the channel region of a transistor are shown. **a**, A silicon-on-insulator (SOI) fin field-effect transistor (FinFET). The 'hard mask' is a thick dielectric that prevents the formation of an inversion channel at the top of the silicon 'fin'. **b**, SOI triple-gate (or tri-gate) MOSFET. Gate control is exerted on the channel from three sides of the device (the top, as well as the left and right sides). **c**, SOI Π-gate MOSFET. Gate control is improved over the tri-gate MOSFET shown in **b. d**, SOI Ω-gate MOSFET. Gate control of the bottom of the channel region is better than in the SOI Π-gate MOSFET. The names Π gate and Ω gate reflect the shape of the gates. **e**, SOI gate-all-around MOSFET. Gate control is exerted on the channel from all four sides of the device. **f**, A bulk tri-gate MOSFET. Gate control is exerted on the channel from three sides of the device (the top, the left and the right). In this case, there is no buried oxide underneath the device. [4]

1.10. Objectives

The salient objectives of the thesis are:

i. To develop a physics based 2-D model for surface potential, threshold voltage and electric field for a Fully Depleted Strained Silicon on Insulator (FD-S-SOI) MOSFET by solving the two dimensional Poisson's equation. The model details the role of various MOS parameters like germanium concentration (X), body doping concentration (N_A), strained silicon thickness (t_{Si}),

oxide thickness (t_{ox}) and gate metal work function (φ_M) influencing the surface potential, threshold voltage and electric field.

ii. To analyze the effect of gate work function (φ_M), channel length (L) and high-k gate dielectric materials (both single layer and double layer) on various electrostatic parameters as well as Analog/RF figures of merit (FOMs) for a Double Gate (DG) MOSFET. By comparing the extracted values, the optimum device parameters are chosen for further design.

iii. Finally one optimum device (Fully Depleted Strained Gate Stack DG MOSFET with optimized device parameters) is designed and simulated for both low power and high frequency applications.

1.11. Thesis Organization

The dissertation is divided into five chapters and its outline is described as follows:

- **Chapter 1: Introduction**

  Fundamental concepts related to technology scaling, the origin and consequences of the SCEs in nanoscale MOSFETs. Various methods like SOI, S-Si, high-k gate dielectric and Multigate MOSFETs are employed to overcome the SCEs are summarized. Objectives of the work and outline of the thesis are also presented.

- **Chapter 2: Modeling and Simulation of Fully Depleted Strained Silicon on Insulator (FD-S-SOI) MOSFET**

  This chapter deals with the physics based 2-D model and simulation for surface potential, threshold voltage and electric field for a Fully Depleted Strained Silicon on Insulator (FD-S-SOI) MOSFET by solving the two dimensional Poisson's equation. The model details the role of various MOS parameters like germanium concentration, body doping concentration, strained silicon thickness, oxide thickness and gate metal work function influencing the surface potential, threshold voltage and electric field.

- **Chapter 3: Analysis of various SCEs & Analog/RF FOMs of DG MOSFET**

  This chapter deals with the simulation both DC & AC performance of the DG MOSFET by varying the gate work function, channel length and gate dielectric materials. First to calibrate the device, a study is made for various important electrostatic parameters by varying the gate work function to maintain a constant threshold voltage irrespective of

drain bias. By taking three different variables as gate work function, channel length and gate oxide, the effect of device design engineering on the analog/RF performance of nanoscale DG MOSFET is investigated. Including the SCEs like SS, DIBL, the important analog/RF figures of merits (FOMs) like transconductance generation factor ($TGF=g_m/I_{ds}$), intrinsic gain ($A_v=g_m/g_d$), Early voltage ($E_v=I_{ds}/g_d$), cutoff frequency ($f_T = g_m/2\pi C_T$) and transconductance frequency product ($TFP= g_m/I_{ds}*f_T$), gain frequency product ($GFP=A_v*f_T$) and gain transconductance frequency product ($GTFP= A_v*g_m/I_{ds}*f_T$) are also examined. C_T stands for the sum of source-to-gate capacitance (C_{GS}) and source-to-drain capacitance (C_{GD}) of the device.

- **Chapter 4: Analysis of Fully Depleted Strained Gate Stack (FD-S-GS) DG MOSFET**

  This chapter deals with the design of an optimized device, i.e. FD-S-GS-DG MOSFET and some electrostatic parameters as well as analog parameters are studied by varying the Ge concentration (X).

- **Chapter 5: Conclusion and Scope for Future Work**

1.12. Motivation

Continuous scaling in MOSFET devices degrades the performance. As a result of scaling, severe problems like leakage currents and SCEs comes into play. To mitigate these problems, a device called Silicon-on-Insulator (SOI) MOSFET has been developed. For higher current drive, faster and smaller chips, the bulk MOSFET scaling is a traditional process. By reducing the channel lengths in each next technology node the improvement in performance and reduction of cost is achieved. But in recent years, the MOSFET scaling is slowed down; hence people are searching for new technologies /methodologies. The new methodologies give rise to two paths; one is the introduction of new materials into the classical single gate MOSFETs like develop uniaxial/biaxial strain in the channel region to enhance the carrier mobility in the channel region and implementation of high-k dielectric material as gate oxide to minimize the gate leakage current. Basic idea of strained MOSEFET is that it Changes the lattice constant of the material and also changes energy band structure (Because lattice constant of Silicon is 5.431 Angstrom and Germanium is 5.658 Angstrom). Germanium has higher mobility (3900 cm^2/V-sec) than silicon (1500 cm^2/V-sec), so, the strain concept is used to enhance the carrier mobility by adding

some amount of germanium with silicon in the channel region. Second is the development of non-classical Multigate MOSFETs (Mug-FETs) which is very good concept for further scaling of the device dimensions.

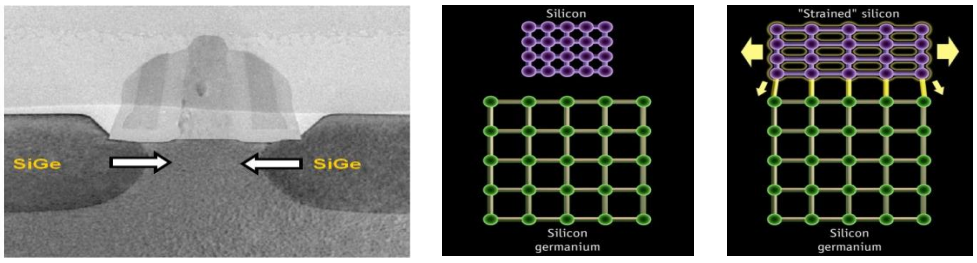

Figure 1.15 Concept of developing strain [8], [18]

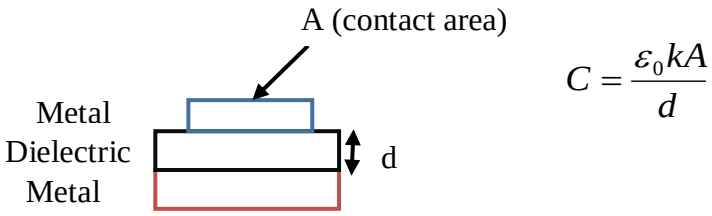

Figure 1.16 Concept of high-k +Metal Gate [15]

So, it is required to design a device and study the electrical/short channel parameters like Electric Field, Surface Potential, Electron Velocity, Current Density, Transconductance (g_m), Output Conductance (g_d), Sub-threshold Swing (SS), Drain Induced Barrier Lowering (DIBL) and also AC performances like cut off frequency (f_t), and the figures of merits (FOMs) like transconductance generation factor (TGF), Early voltage (E_v), intrinsic gain (A_v), transconductance frequency product (TFP), gain frequency product (GFP) and gain transconductance frequency product (GTFP).

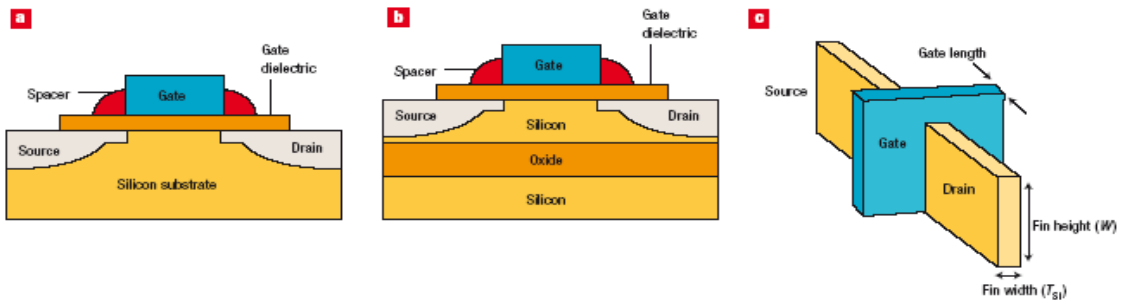

Figure 1.17 Different type of MOSFET structures [21]

a. A traditional n-channel MOSFET uses a highly doped n-type polysilicon gate electrode, a highly doped n-type source/drain, a p-type substrate, and a silicon dioxide or oxynitride gate dielectric.

b. A SOI MOSFET is similar to the traditional MOSFET except the active silicon is on a thick layer of silicon dioxide. This electrical isolation of the silicon reduces parasitic junction capacitance and improves device performance.

c. A FinFET is a three-dimensional version of a MOSFET. The gate electrode wraps around a confined silicon channel providing improved electrostatic control of the channel electrons.

1.13. Summary

Continuous scaling in MOSFET devices degrade the performance of the device resulting in major problems such as leakage currents and short channel effects (SCEs) are major problems. To overcome these problems, a device called SOI MOSFET has been developed. To increase the density and enhance the performance of CMOS technology new materials are introduced into the classical single gate MOSFET and non-classical multi gate MOSFETs are developed. For higher current drive, faster and smaller chips, the bulk MOSFET scaling is a traditional process. By reducing the channel lengths in each next technology node, the improvement in performance and reduction of cost is achieved. But in recent years, the MOSFET scaling is slowed down; hence people are searching for new technologies /methodologies. The new methodologies give rise to two paths; one is the introduction of new materials into the classical single gate MOSFETs like develop uniaxial/biaxial strain in the channel region to enhance the carrier mobility in the channel region and implementation of high-k dielectric material as gate oxide to minimize the gate leakage current. Second is the development of non-classical Multigate MOSFETs (Mug-FETs), which is very good concept for further scaling of the device dimensions.

Chapter 2

Modeling and Simulation of FD-S-SOI MOSFET

2.1 Introduction

Since last four decades silicon technology is ruling the integrated circuit (IC) market but main issue of silicon technology is the effects occurring due to reduction of the dimensions. Continuous shrinking of the device is strongly required to achieve high packing density and better performance. The reduction of the device dimensions in all aspects degrades the performance and the resulting SCEs heavily affect the device. In order to mitigate these effects, SOI engineering came into picture well suppressing the SCEs when compared to bulk MOSFETs. While scaling the planar bulk MOSFET into nanometer regime, significant challenges and difficulties came forward like the control of SCEs [22-24]. Therefore, various new structures with different engineering concepts have been reported to reduce the SCEs in SOI platform. Among them, Strain engineering is very popular for enhancing the carrier mobility [25] [26]. Since strained Si provides device performance enhancements through changes in material properties rather than changing in device geometry and doping, strained Si is a promising candidate for improving the performance of Si CMOS technology without compromising the control of short channel effects. The conventional method of producing strained-Si is by growing pseudomorphic Si epitaxial layer on relaxed SiGe alloys. By increasing the Ge content of the relaxed SiGe alloy, the amount of biaxial strain, and therefore, the magnitude of the mobility enhancement, can be enhanced [27-31]. However, as the Ge content is increased, the critical thickness (the thickness to which the strained-silicon can be grown without inducing misfit dislocations to alleviate the strain) is reduced. Single layer strained-silicon-on-insulator (S-SOI) is a new SiGe-free material system that combines the carrier transport advantages of strained-Si with the reduced parasitic capacitance and improved MOSFET scalability of thin-film SOI. The single layer S-SOI is less susceptible to misfit dislocation induced leakage current while maintaining increased carrier mobility [32-34]. A number of applications have been reported for

the strained-silicon MOSFETs. Earlier works have concentrated on modeling and simulating the electron transport in strained-silicon MOSFETs [28-35]

In this chapter, the main aim is to develop a physics based 2-D model for surface potential, threshold voltage and electric field for a Fully Depleted Strained Silicon on Insulator (FD-S-SOI) MOSFET by solving the two dimensional Poisson's equation. The model details the role of various MOS parameters like germanium concentration, body doping concentration, strained silicon thickness, oxide thickness and gate metal work function influencing the surface potential, threshold voltage and electric field. It is simple in its functional form and lends itself to efficient computation.

2.2 Single-Layer S-SOI MOSFETs

SSOI MOSFETs are of two types: 1) single-layer S-SOI (S-SOI substrates) and 2) strained-Si on SiGe-on-insulator (SGOI substrates). In this chapter, one single-layer S-SOI MOSFET has been considered as shown in Figure 2.1.

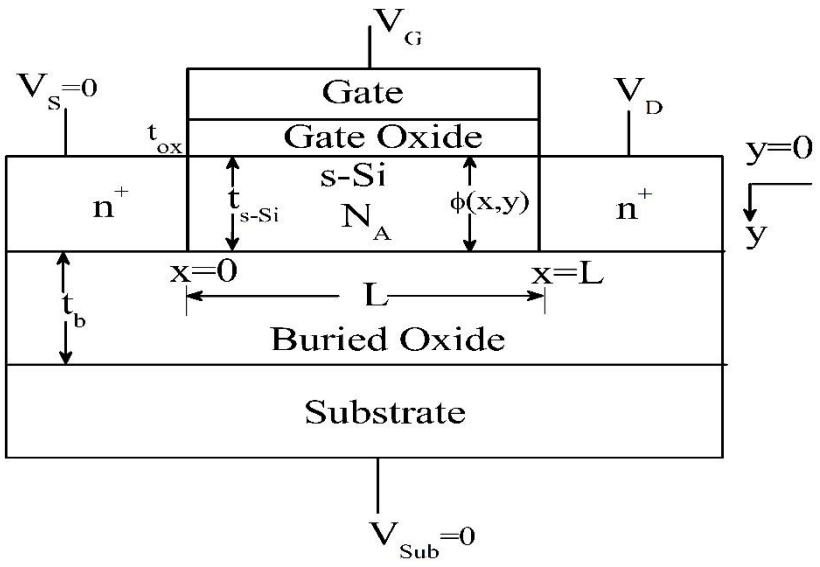

Figure 2.1 Cross-sectional view of the single-layer FD-S-SOI MOSFET

This structure is particularly useful for body thickness scaling when compared to Si/SiGe bi-layer or Si/SiGe/Si tri-layer on oxide structures [32-33]. The Smart Cut™ technology is a layer transfer technique; it allows producing a variety of engineered wafers, with a layer of one material placed on a substrate of a different material. For example, biaxial strained Si layers or

relaxed layers of SiGe alloys can be bonded to Si handle wafers with SiO_2 in between and compound semiconductor layers on oxidized [26-28].

This compact model will be used for the design and characterization of high-performance single-layer S-SOI nanoscale MOSFETs including the short-channel effects and the effect of varying device parameters.

2.2.1 Effect of Strain on Band gap

In the presence of strain, the silicon thin film experiences biaxial tension that changes its band structure. The strain causes the electron affinity of silicon to increase and the band gap, the effective mass of carriers to decrease. The above strain-related effects on the silicon band structure are modeled as follows [31-35]

$$(\Delta E_C)_{s-Si} = 0.57X \qquad \text{and} \qquad \left(\Delta E_g\right)_{s-Si} = 0.4X$$

$$V_T Ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) = V_T Ln\left(\frac{m^*_{h,Si}}{m^*_{h,s-Si}}\right)^{\frac{3}{2}} \approx 0.075X \tag{2.1}$$

Effect of Strain on Flat band Voltage

The effect of strain on the front-channel flat band voltage of FD-SOI MOSFET can be modeled as follows [32]:

$$\left(V_{FB,f}\right)_{s-Si} = \left(V_{FB,f}\right)_{Si} + \Delta V_{FB,f} \tag{2.2}$$

$$\text{Where } \left(V_{FB,f}\right)_{Si} = \varphi_M - \varphi_{Si}$$

$$\Delta V_{FB,f} = \frac{-(\Delta E_C)_{s-Si}}{q} + \frac{\left(\Delta E_g\right)_{s-Si}}{q} - V_T Ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right)$$

$$\varphi_{Si} = \frac{\chi_{Si}}{q} + \frac{E_{g,Si}}{2q} + \varphi_{F,Si}\ ,\ \varphi_{F,Si} = V_T Ln\left(\frac{N_A}{n_{i,Si}}\right)$$

In a similar way, the effect of strain on the back-channel flat band voltage of FD-SOI MOSFET is modeled as follows:

$$(V_{FB})_{s-Si} = (V_{FB})_{Si} + \Delta V_{FB,b} \tag{2.3}$$

$$\text{Where } (V_{FB})_{Si} = \varphi_{sub} - \varphi_{Si} \text{ and}$$

$$\Delta V_{FB,b} = \frac{-(\Delta E_C)_{s-Si}}{q} + \frac{\left(\Delta E_g\right)_{s-Si}}{q} - V_T Ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right)$$

It is also important to consider the effect of strain on the built-in voltage across the source –body and drain-body junctions in the strained-Si thin film, i.e.

$$V_{bi,s-Si} = V_{bi,si} + (\Delta V_{bi})_{s-Si} \tag{2.4}$$

$$\text{Where} \quad V_{bi,si} = \frac{E_{g,Si}}{2q} + \varphi_{F,Si} \ ,$$

$$(\Delta V_{bi})_{s-Si} = \frac{-(\Delta E_g)_{s-Si}}{q} + V_T Ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right)$$

2.2.2 Surface Potential & Electric Field Model

Before the onset of strong inversion, the 2-D Poisson equation in the strained-silicon thin film of an FD-SSOI MOSFET, shown in Figure 1, can be written as follows [31-32]:

$$\frac{d^2\varphi(x,y)}{dx^2} + \frac{d^2\varphi(x,y)}{dy^2} = \frac{qN_A}{\epsilon_{Si}} \qquad for\ 0 \le x \le L, 0 \le y \le t_{S-Si} \tag{2.5}$$

The potential profile in the vertical direction in the strained-Si film (y-direction in Fig. 1) can be approximated by a parabolic function, as done in [31-32], i.e.

$$\varphi(x,y) = \varphi_s(x) + C_1(x)y + C_2(x)y^2 \qquad for\ 0 \le x \le L, 0 \le y \le t_{S-Si} \tag{2.6}$$

Where the coefficients $c_1(x)$ and $c_2(x)$ are functions of x only. Equation (2.5) can be solved using the following boundary conditions:

Boundary conditions

1) Electric flux (displacement) at the gate oxide/strained-Si film interface is continuous, i.e.

$$\left[\frac{d\varphi(x,y)}{dy}\right]_{y=0} = \frac{\epsilon_{ox}}{\epsilon_{Si}}\left(\frac{\varphi_{s(x)} - V'_{GS}}{t_f}\right) \tag{2.7}$$

2) Electric flux at the interface of buried oxide and the back channel is continuous, i.e.

$$\left[\frac{d\varphi(x,y)}{dy}\right]_{y=t_{s-Si}} = \frac{\epsilon_{ox}}{\epsilon_{Si}}\left(\frac{V'_{sub} - \varphi(x,t_{s-Si})}{t_b}\right) \tag{2.8}$$

3) The substrate potential at the source end is

$$\varphi(0,0) = \varphi_s(0) = V_{bi,s-Si} \tag{2.9}$$

4) The surface potential at the drain end is

$$\varphi(L,0) = \varphi_s(L) = V_{bi,s-Si} + V_{DS} \tag{2.10}$$

Using the boundary conditions, one can obtain the coefficients $C_1(x)$ and $C_2(x)$ leading to an expression for $\varphi(x,y)$ and setting $y = 0$, we obtain

$$\frac{d^2\varphi_s(x)}{dx^2} - \alpha\varphi_s(x) = \beta \tag{2.11}$$

Where$\propto = \frac{C_b}{t_{s-Si}\epsilon_{Si}}\left(\frac{2C_{Si}+C_f}{2C_{Si}+C_b}\right) + \frac{C_f}{t_{s-Si}\epsilon_{Si}}$

$$\beta = \frac{qN_A}{\epsilon_{Si}} - \left(\frac{C_b}{t_{s-Si}\epsilon_{Si}} + \frac{C^2{}_b}{(2C_{Si}+C_b)t_{s-Si}\epsilon_{Si}}\right)V'_{sub} - \left[\frac{C_b}{t_{s-Si}\epsilon_{Si}}\left(\frac{C_f}{2C_{Si}+C_b}\right) + \frac{C_f}{t_{s-Si}\epsilon_{Si}}\right]V'_{GS}$$

Where $C_f = \frac{\epsilon_{ox}}{t_f}$, $C_{Si} = \frac{\epsilon_{Si}}{t_{s-Si}}$ and $C_b = \frac{\epsilon_{ox}}{t_b}$.

The above equation (2.11) with constant coefficients, can be written as

$$\varphi_s(x) = Aexp(\lambda x) + Bexp(-\lambda x) - \sigma \tag{2.12}$$

Where $\lambda = \sqrt{\alpha}$ and $\sigma = \frac{\beta}{\alpha}$ .Now using boundary conditions to solve for A and B, we obtain

$$A = \frac{[1-\exp(-\lambda l)]\left(V_{bi,s-Si}+\sigma\right)+V_{DS}}{exp(\lambda l)-exp(-\lambda l)}$$

$$B = \frac{[1-\exp(\lambda l)]\left(V_{bi,s-Si}+\sigma\right)+V_{DS}}{exp(-\lambda l)-exp(\lambda l)}$$

Thus Electric Field can be calculated as

$$E = \frac{d\varphi_s(x)}{dx} = A\lambda exp(\lambda x) - B\lambda exp\,(-\lambda x)$$

2.2.3 Threshold Equation Model

To obtain a model for the threshold voltage, we need to find the minimum surface potential from equation (2.12) by substituting

$$\frac{d\varphi_s(x)}{dx} = 0 \tag{2.13}$$

This will be the minimum surface potential as

$$\varphi_{s,min} = 2\sqrt{AB} - \sigma \tag{2.14}$$

The threshold voltage V_{th} is that value of the gate voltage V_{GS} at which a conducting channel is induced under the gate oxide at the surface of SOI MOSFET. In an FD thin-film SOI MOSFET, it is desirable that the front channel turns on before the back channel and that only the front channel contributes to the current conduction. Therefore, in a conventional unstrained silicon MOSFET, the threshold voltage is taken to be that value of gate–source voltage for which the front-channel surface potential $\varphi_{s,min} = 2\varphi_{F,Si}$, where $\varphi_{F,Si}$ is the difference between the

extrinsic Fermi level in the bulk region and the intrinsic Fermi level [31-35]. For the single-layer SSOI MOSFET, the condition for threshold under the front gate is modified as

$$\varphi_{s,min} = 2\varphi_{F,Si} + \Delta\varphi_{s-Si} = \varphi_{th} \tag{2.15}$$

$$\text{Where} \quad \Delta\varphi_{s-Si} = \frac{-(\Delta E_g)_{s-Si}}{q} + V_T Ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right)$$

and φ_{th} is that value of surface potential at which the volumetric inversion electron charge density in the strained-Si device is the same as that in the unstrained-Si at threshold, i.e., equal to the body doping. Thus, the threshold voltage is defined as the value of V_{GS} at which the minimum surface potential $\varphi_{s,min}$ equals φ_{th}. Hence, we can determine the value of threshold voltage by substituting (2.14) into (2.15) and solving for V_{GS} as [32-35].

$$V_{th} = \frac{-K_2 + \sqrt{K^2{}_2 - 4K_1K_3}}{2K_1} \tag{2.16}$$

Where $K_1 = b^2[4(N - N^2) - 1]$

$K_2 = b\{4(NV_{bi,s-Si} + M - 2MN) - 2\varphi_{th}\} + 2ab\{4(N - N^2) - 1\}$

$K_3 = a\{4(NV_{bi,s-Si} + M - 2MN) - 2\varphi_{th}\} - \varphi^2{}_{th} - 4(M^2 - MV_{bi,s-Si}) + a^2\{4(N - N^2) - 1\}$

$M = \frac{[1-exp(-\lambda l)]V_{bi,s-Si}+V_{DS}}{2sinhx}$, $N = \frac{1-exp(-\lambda l)}{2sinhx}$

$$a = \frac{1}{\alpha}\left[\frac{qN_A}{\varepsilon_{Si}} - \left\{\frac{C_b}{t_{s-Si}\varepsilon_{Si}} + \frac{C^2{}_b}{(2C_{Si}+C_b)t_{s-Si}\varepsilon_{Si}}\right\}V'_{sub} + \left\{\frac{C_bC_f}{t_{s-Si}\varepsilon_{Si}(2C_{Si}+C_b)} + \frac{C_f}{t_{s-Si}\varepsilon_{Si}}\right\}(V_{FB,f})_{s-Si}\right]$$

$$b = -\frac{1}{\alpha}\left[\frac{C_bC_f}{t_{s-Si}\varepsilon_{Si}(2C_{Si}+C_b)} + \frac{C_f}{t_{s-Si}\varepsilon_{Si}}\right]$$

2.3 Results and Discussion

2.3.1 Surface Potential

To verify the proposed analytical model, the 2-D device simulator ATLAS [36] was used to simulate the surface potential distribution within the silicon thin film and threshold voltage variation are compared with the results predicted by the analytical model.

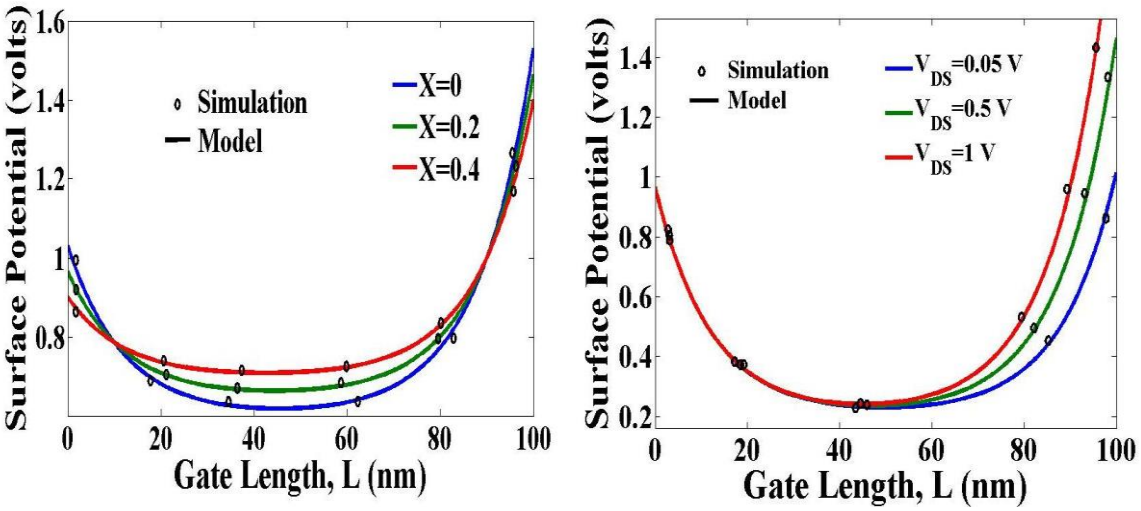

Figure 2.2 The parameters used are as follows: V_{sub} = 0 V, $N_A = 1 \times 10^{18}$ cm^{-3}, $t_{s\text{-}Si}$ = 25 nm, t_{ox} = 2 nm, t_b = 100 nm, and φ_M = 4.35 eV. (a) Surface Potential versus L for different values of X with constant V_{DS} = 0.5 V. (b) Surface Potential versus L for different values of V_{DS} with constant X= 0.2.

In Fig. 2.2 (a), the calculated and simulated values of surface potential are plotted against the horizontal distance x for L = 100 nm at different values of effective Ge mole fraction (X) in the relaxed SiGe buffer. It can be seen that the potential barrier is increasing with increase in X but decreases at source and drain end. As the threshold voltage is calculated from the minimum surface potential and it is very important to choose the appropriate value of threshold voltage for a MOS device. The device having high threshold voltage is slower. Similarly, device having low threshold voltage have more leakage current. So, for our convenience from the Fig. 2.2 (a), the middle one is considered i.e., X=0.2 and the value is fixed to study the effect of other MOS parameters on surface potential for a strained MOSFET. Fig. 2.2 (b) shows the variation of surface potential along the channel length for different values of drain bias. It is seen from the figure that due to presence of Ge mole fraction there is no significant change in the potential at the source end and a very minute change at the drain end. As a consequence, V_{DS} has only a very small influence on drain current after saturation and it is evident from the figure that there is a negligible shift in the point of minimum potential irrespective of the applied drain bias. Therefore, DIBL is considerably reduced for the FD-S-SOI MOSFET. The model predictions correlate well with the simulation results [36] proving the accuracy of our proposed analytical model.

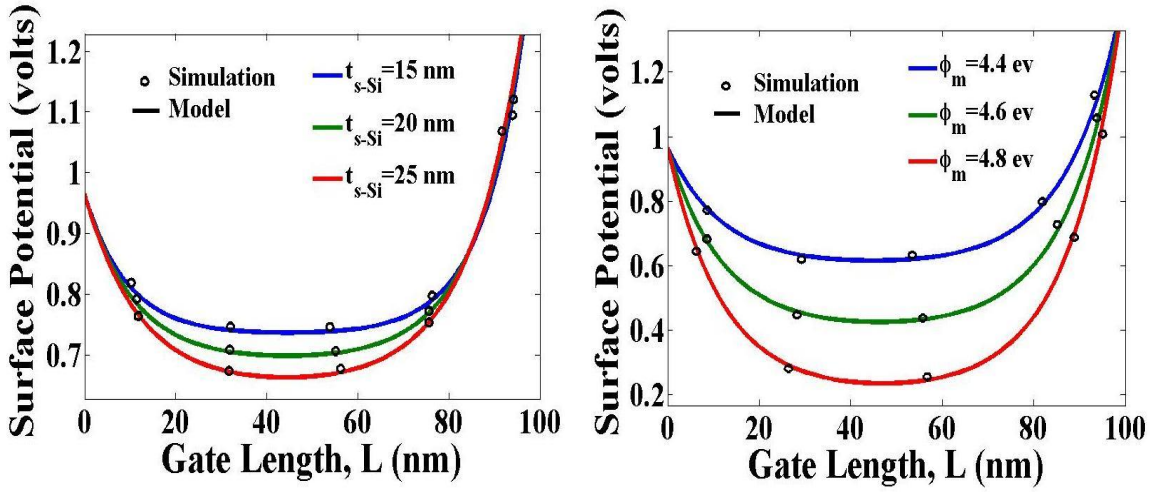

Figure 2.3 The parameters used are as follows: V_{DS} = 0.5 V, V_{sub} = 0 V, N_A = 1 × 1018 cm−3, X=0.2, t_{ox} = 2 nm and t_b = 100 nm. (a) Surface Potential versus L for different values of t_{s-Si} with constant φ_M = 4.35 eV. (b) Surface Potential versus L for different values of φ_M with constant t_{s-Si}= 25 nm.

Fig. 2.3 (a) shows the variation of the surface potential along the channel for three different strained-Si thin film thicknesses. When the thin film thickness is reduced, the controllability of the front gate over the surface channel becomes stronger in comparison to the influence exerted by the source/drain. Fig. 2.3 (b) shows the variation of the surface potential along the channel for three different work function values of gate metal M. As it can be seen from figure, choosing a gate metal M with a higher work function leads to a better control of the channel potential minima by M.

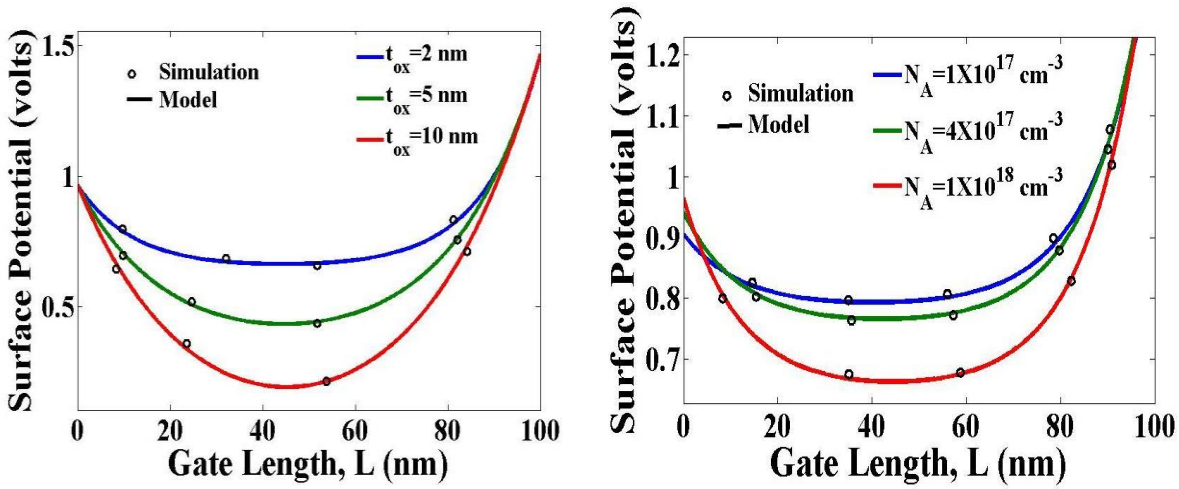

Figure 2.4 The parameters used are as follows: V_{DS} = 0.5 V, V_{sub} = 0 V, φ_M = 4.35 eV, t_{s-Si}= 25 nm, X=0.2, and t_b = 100 nm. (a) Surface Potential versus L for different values of t_{ox} with constant N_A = 1 × 10^{18} cm^{-3}. (b) Surface Potential versus L for different values of N_A with constant t_{ox}= 2 nm.

Fig. 2.4 (a) shows the variation of the surface potential along the channel for different oxide thickness. When the oxide thickness is reduced, the controllability of the front gate over the channel potential increases, but at the same time it becomes more prominent to SCEs. Therefore, continuous scaling down of the oxide thickness reduces SCEs. Also oxide thickness cannot be scaled down to very small values because tunneling through the thin oxide and hot-carrier effects become prominent. Fig. 2.4 (b) shows the variation of the surface potential along the channel for different body doping concentration. It can be seen from the figure that as the doping concentration increases the surface potential minimum decreases in the channel region but it is quite constant in drain side. Hence DIBL decreases and the immunity to control the SCEs are increased.

2.3.2 Electric Field Profile

Fig. 2.5 (a) shows the variation of the electric distribution along the channel at different values of effective Ge mole fraction (X). It is evident from the figure that the electric field at the drain side considerably reduces with increase in X value. This reduction of the electric field experienced by the carriers in the channel can be interpreted as the reduction of the hot-carrier effect at the drain end.

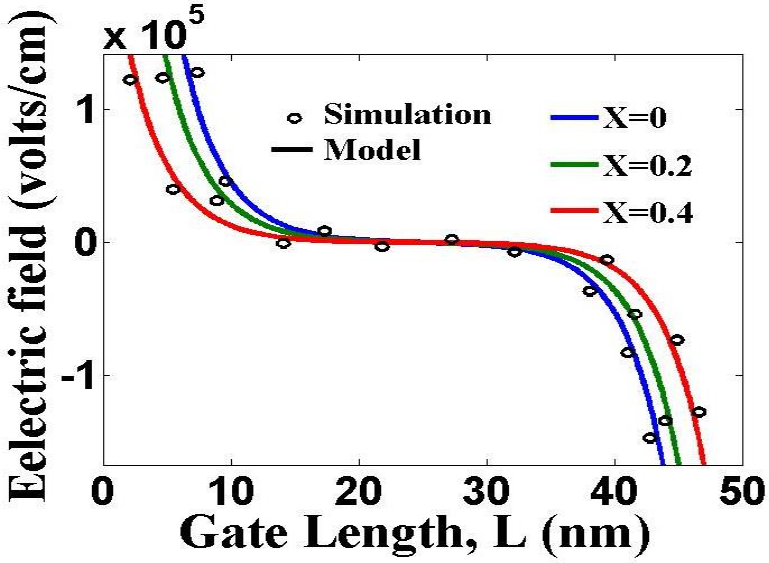

Figure 2.5 Variation of Electric Field along the channel for different values of X. The parameters used are as follows: V_{DS} = 0.5 V, V_{sub} = 0 V, φ_M = 4.35 eV, $t_{s\text{-}Si}$= 25 nm, N_A=1X10^{18} cm^{-3}, t_{ox}=2 nm and t_b = 100 nm.

Therefore, further scaling of oxide thickness is possible in the FD-S-SOI structure. As shown in the figure, the results from the analytical model are in close proximity with the

simulation results. Similarly, we can make a study of the electric field dependence on other MOS parameters.

2.3.3 Threshold Voltage

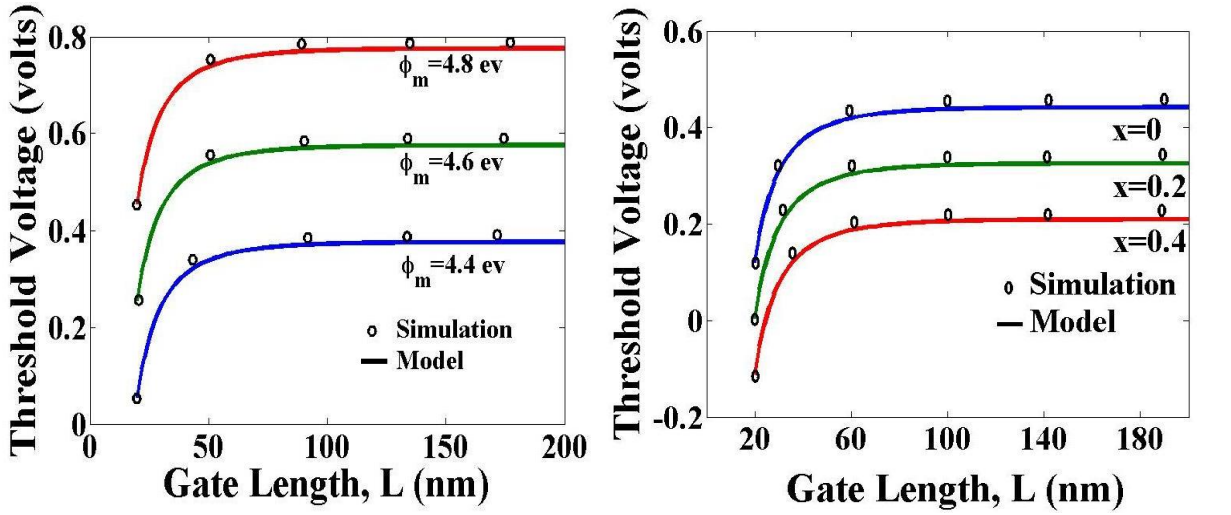

Figure 2.6 The parameters used are as follows: V_{DS} = 0.5 V, V_{sub} = 0 V, $t_{s\text{-}Si}$= 25 nm, t_{ox}= 2 nm, N_A=1X10^{18} cm^{-3} and t_b = 100 nm. (a) Threshold Voltage versus L for different values of φ_M with constant X=0.2. (b) Threshold Voltage versus L for different values of X with constant φ_M = 4.35 eV.

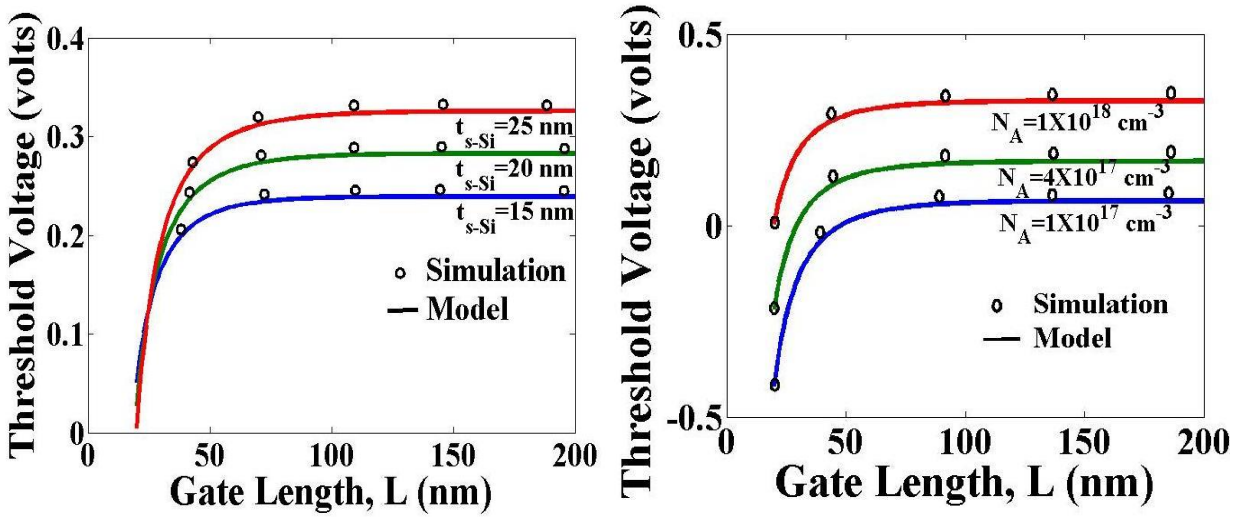

Figure 2.7 The parameters used are as follows: V_{DS} = 0.5 V, V_{sub} = 0 V, φ_M = 4.35 eV, t_{ox}= 2 nm, X=0.2 and t_b = 100 nm. (a) Threshold Voltage versus L for different values of $t_{s\text{-}Si}$ with constant N_A=1X10^{18} cm^{-3}. (b) Threshold Voltage versus L for different values of N_A with constant $t_{s\text{-}Si}$= 25 nm.

Fig. 2.6 (a) shows the variation of the threshold voltage along the channel for three different work function values of gate metal M. As it can be seen from figure, choosing a gate metal M with a higher work function leads to a better control of the V_{th} value. Fig.2.6 (b) shows the variation of threshold voltage with gate length for different values of effective Ge mole fraction in the relaxed SiGe buffer. It is observed that short channel effects become apparent when the channel length is below 50-60 nm and is marked by sharp decrease in the V_{th} value. The gate-source/drain (S/D) charge sharing and source-body/drain-body built in potential barrier lowering due to overlap of the lateral source-body and drain-body depletion regions becomes significant for such short channel lengths. The V_{th} values from the analytical model are in close proximity with the simulation results.

Fig. 2.7 (a) shows the variation of the threshold voltage along the channel for different strained-Si thin film thicknesses. It can be seen that V_{th} also reduces as strained-Si thin film thickness decreases. This is because of the decrease in the total depletion charge under the gate with decrease in the strained-Si thin-film thickness, leading to an early onset of inversion. Thus, a higher thickness of the strained-Si thin film leads to higher V_{th}. Fig. 2.7 (b) shows the variation of the threshold voltage along the channel for different body doping concentration. As shown in the figure, threshold voltage increases with increased body doping and a "roll-up" in the characteristics is observed at lower channel lengths. Hence the scaling of the device can go to some more extent without any further increase in SCEs by increasing the body doping concentration. The threshold voltage obtained from the model tracks the simulation result very well.

Fig. 2.8 (a) shows the threshold voltage variation with strain (equivalent Ge mole fraction, X in the SiGe buffer) for different body doping concentration. It is evident from the figure that the threshold voltage of the FD-S-SOI MOSFET can be controlled by using appropriate channel doping concentration and X value. Thus, by using a suitable gate material, we can achieve higher mobility of charge carriers due to larger strain and lower doping concentration and, consequently, higher transconductance. Fig. 2.8 (b) shows the variation of the threshold voltage along the channel for different gate oxide thicknesses. When the gate oxide thickness is reduced, the threshold voltage is also reduced which is the requirement for a faster device. Therefore, continuous scaling down of the oxide thickness gives rise to faster devices but on the other hand, oxide thickness cannot be scaled down to very small values because tunneling

through the thin oxide and hot-carrier effects become prominent. It is clear that there is a close match between the analytical results and the 2-D simulation results.

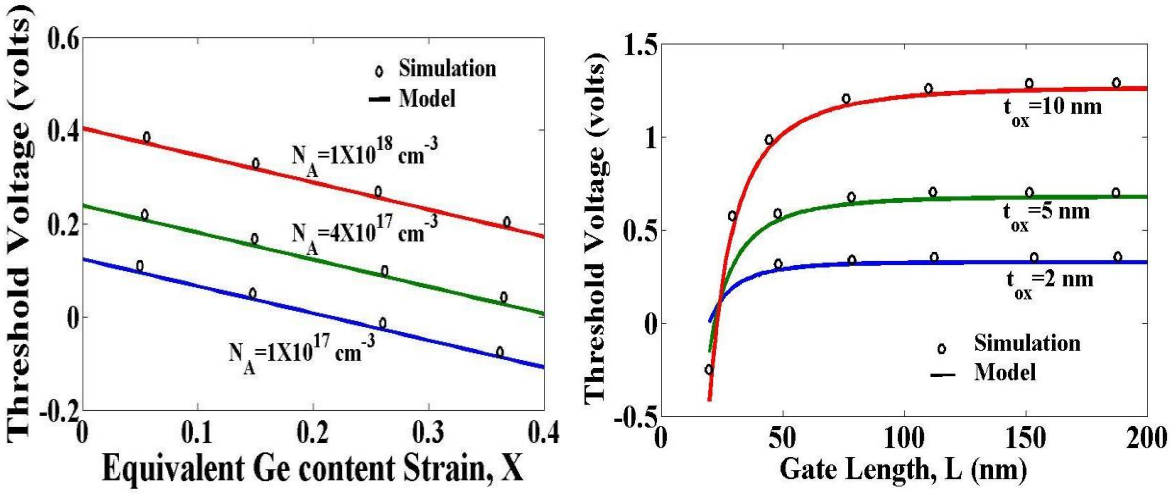

Figure 2.8 The parameters used are as follows: V_{DS} = 0.5 V, V_{sub} = 0 V, φ_M = 4.35 eV, $t_{s\text{-}Si}$= 25 nm, and t_b = 100 nm. (a) Threshold Voltage versus strain X (equivalent Ge content in the relaxed SiGe buffer) for different values of N_A with constant t_{ox}= 2 (b) Thresh Voltage versus L for different values of t_{ox} with constant N_A=1X10^{18} cm^{-3} and X=0.2.

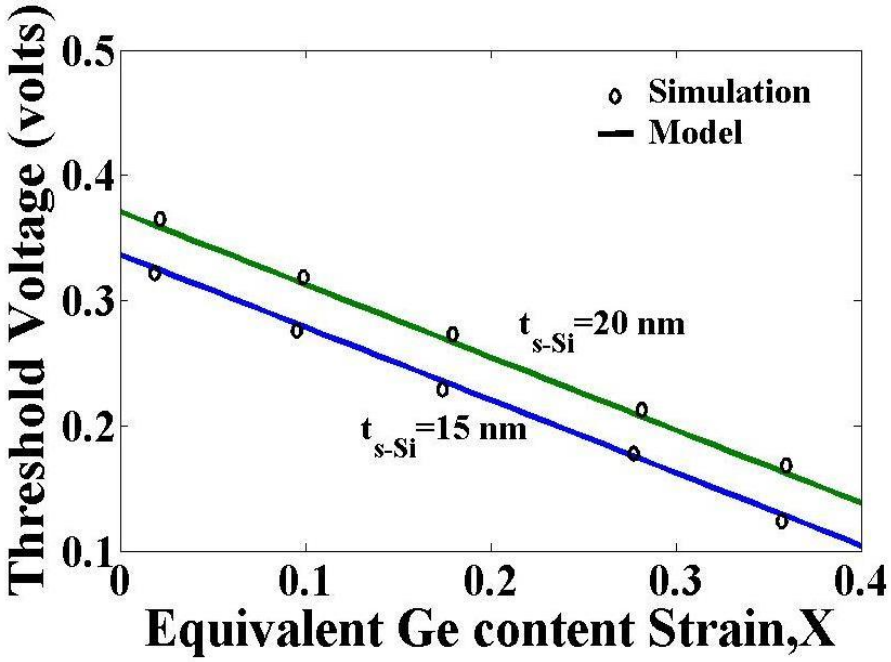

Figure 2.9 Variation of Threshold Voltage along X for different values of $t_{s\text{-}Si}$. The parameters used are as follows: V_{DS} = 0.5 V, V_{sub} = 0 V, φ_M = 4.35 eV, $t_{s\text{-}Si}$= 25 nm, N_A=1X10^{18} cm^{-3}, t_{ox}=2 nm and t_b = 100 nm.

Fig. 2.9 shows the threshold voltage variation with strain (equivalent Ge mole fraction, X in the SiGe buffer) for different strained silicon thickness. It is evident from the figure that there is a significant fall in the threshold voltage with increasing strain, even becoming negative for a

Ge content of 0.4-0.5, and the decrease of threshold voltage is almost linear. This reduction in the threshold voltage with increasing Ge content X is due to a decrease in the flat band voltage, decrease in the source-body/drain-body built in potential barrier, and an early onset of inversion due to a decrease $\varphi_{th.}$ As shown in the figure, the results from the analytical model are in close proximity with the simulation results.

2.4 Summary

An analytical expression of surface potential, electric field and threshold voltage for fully depleted strained silicon on insulator (FD-S-SOI) MOSFET is formulated based on the 2-D physical model of surface potential developed earlier. The effect of various device parameters like strain (equivalent Ge mole fraction in the relaxed SiGe buffer), gate length scaling, body doping density, gate metal work function, strained silicon thickness, gate oxide thickness on the surface potential, electric field and threshold voltage is studied. The results predicted by the model are compared with 2-D simulations performed. There is a significant drop in threshold voltage with increasing strain and decreasing channel length. The increase in strain, i.e., equivalent Ge content, enhances the performance of S-SOI MOSFETs in terms of improved transconductance and speed because of an increase in the carrier mobility. However, as demonstrated by our results, there are undesirable side effects with increasing equivalent Ge content such as a roll off in V_{th}, which may affect the device characteristics and performance significantly. The compact model accurately predicts the threshold voltage over a large range of device parameters and can be effectively used to design and characterize the nanoscale single-layer FD-S-SOI MOSFETs with the desired performance.

Chapter 3

Analysis of DC & Analog/RF Performance of DG MOSFET by varying Work Function, Gate Length and High-k Gate Dielectric

3.1. Introduction

Double Gate (DG) structures fabricated on Silicon-on-Insulator (SOI) wafers have been utilized in Complementary Metal Oxide Semiconductor (CMOS) technology due to their excellent scaling capability, outstanding Short Channel Effects (SCEs) immunity and high current drivability owing to excellent control of both top/bottom through coupling. DG structure shows better SCE suppression, higher on current and trans-conductance, lower leakage current and better scaling capability compared with the bulk MOSFET. As conventional silicon MOSFETs are scaled into nanometer regime, maintaining performance enhancement beyond 100 nm technology node becomes extremely difficult due to increased SCEs [37-39].

According to ITRS roadmap, a precisely controlled process flow for the incorporation of new technologies is becoming crucial for deep sub-micron devices. Among the possible solutions, unconventional MOS structures employing asymmetric structures have been proposed to overcome the SCEs. DG MOSFET is one of the most promising candidates in nanoscale design for providing a scalability option. Excellent SCEs immunity, high transconductance and nearly ideal subthreshold slope have been reported by many theoretical and experimental studies on the device [40-41]. Continuous scaling of MOSFET devices has been successfully propelled by the rapid advancement of device engineering and fabrication technologies for gaining better performance and higher packing density. As CMOS scaling approaches the limit imposed by gate oxide tunneling, the DG MOSFET is becoming the subject of intense VLSI research, owing to its ability to be scaled to the shortest channel lengths possible for a given gate oxide thickness. Excellent SCE immunity, improved threshold voltage roll off, higher drain current, higher transconductance and an ideal subthreshold slope have been reported by various studies on this

device. As MOSFET dimensions are scaled down to sub 100 nm regimes, threshold voltage reduction with decreasing channel lengths and DIBL become important issues that should be addressed while providing immunity against SCEs [40-43]. Now days, more emphasis is given to the study of analog, RF performance of the nanoscale devices [44-50].

In this chapter, first to calibrate the device a study is made for various important electrostatic parameters by varying the gate work function to maintain a constant threshold voltage irrespective of drain bias. By taking three different variables as gate work function, channel length and gate oxide, the effect of device design engineering on the analog/RF performance of nanoscale DG MOSFET is investigated. Including the SCEs like SS, DIBL, we also examined important analog/RF figures of merit (FOMs) like transconductance generation factor (g_m/I_d), intrinsic gain ($A_v=g_m/g_d$), cutoff frequency ($f_T = g_m/2\pi C_T$) and transconductance frequency product (TFP= g_m/I_d*f_T), gain frequency product (GFP=A_v*f_T) and gain transconductance frequency product (GTFP= A_v*g_m/I_d*f_T). C_T stands for the total source-to-gate capacitance (C_{GS}) and source-to-drain capacitance (C_{GD}) of the device.

3.2 Device Design

The schematic structure of DG MOSFET is shown in Fig. 3.1. The source and drain doping density (N_D) is fixed as 10^{20} cm^{-3} and the channel is doped with (N_A) 10^{16} cm^{-3} except in case of work function variation.

3.2.1 Varying Work Function

First to calibrate the device, various electrostatic parameters are studied by considering four different gate work functions as 4.52 eV, 4.6 eV and 4.7 eV to maintain a constant threshold voltage irrespective of the drain bias [51]. Threshold voltage (V_{th}) is maintained constant at 0.2 V by adjusting channel doping and source/drain doping for analog/RF performances.

3.2.2 Varying Gate Length

Both the DC and AC analysis are done by considering five different gate lengths as 60 nm, 50 nm, 40 nm and 30 nm to optimize the gate length [52-53]. By tuning the gate work function between 4.6 eV to 4.7 eV, V_{th} is achieved a constant value for all channel length cases.

3.2.3 Considering high-k dielectrics as gate oxide

Two different types of structural models have been considered. The first model is structured considering single oxide layer and the second with double oxide layer or gate stack (i.e. gate oxides). In each case, the effective oxide thickness is fixed at 1.1 nm. To maintain a constant capacitance while varying the dielectric permittivity from 3.9 to 40, the thickness of the high-k dielectric is calculated by $T_k=k*(T_{SiO2}/3.9)$, where k is the permittivity of high-k dielectric and T_{SiO2} is the equivalent SiO_2 thickness. According to the above relation, for k=7.5, k=24, k=30 and k=40 the corresponding high-k thicknesses are 2.1 nm, 6.8 nm, and 8.5 nm respectively in order to maintain a constant EOT=1.1 nm for single layer configurations. Further for double layer/gate stack configurations SiO_2 layer thickness is fixed at 0.6 nm and above this layer 0.5 nm equivalent thickness of high-k layer is deposited, so that the EOT reaches 1.1 nm. In all the cases the gate work function is tuned between 4.5eV - 4.7eV to obtain the threshold voltage (V_{th}) of 0.2V at drain to source voltage V_{DS} of 0.1V. This work considers the high-k dielectrics as Si_3N_4, HfO_2, and Ta_2O_5 [54-59].

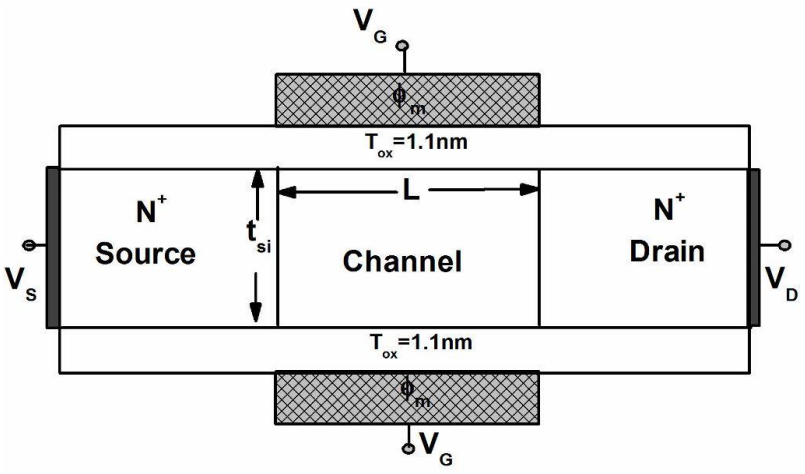

Figure 3.1 Schematic structure of Double Gate N-MOSFET

3.3 Simulation

To obtain accurate results for MOSFET simulation we need to account for the mobility degradation that occurs inside inversion layers. The degradation normally occurs as a result of higher surface scattering near the semiconductor to insulator interface. Therefore, in the simulation, the inversion-layer Lombardi constant voltage and temperature (CVT) mobility

model is taken, that takes into account the effect of transverse fields, along with doping and temperature dependent parts of the mobility.

The Shockley–Read–Hall (SRH) model simulates the leakage currents that exist due to thermal generation. Electrons in thermal equilibrium at given temperature with a semiconductor lattice obey Fermi-Dirac statistics. The use of Boltzmann statistics is normally justified in semiconductor device theory, but Fermi-Dirac statistics are necessary to account for certain properties of very highly doped (degenerate) materials. The model Fermi-Dirac uses a Rational Chebyshev approximation that gives results close to the exact values. The Auger recombination models for minority carrier recombination have been used. In SOI technology the potential in the channel is commonly referred to as "floating". Furthermore, we chose Gummel's method (or the decoupled method) which performs a Gummel iteration for Newton solution [36].

3.4 Results and Discussion

3.4.1 Variation of Work Function

In order to maintain the appropriate threshold voltages for short channel CMOS devices, it is necessary to achieve two gate work functions similar to those of n^+ and p^+ poly-Si. For novel structure such as the double gate MOSFET, an intermediate work function corresponding to mid gap in Si is required. An ideal metal gate technology should achieve separately optimized work functions for NMOSFETs. This will require a means to adjust the work function of the metal. With further optimization, this single metal gate technology may potentially replace conventional poly-Si gate technology for CMOS and can also be used for multiple V_{th} technologies. Hence, in this sub section, we have outlined a detailed analysis of various SCEs as well as Analog/RF parameter fluctuations consisting of metal gate work function fluctuation by maintaining a constant V_{th} for all cases.

Fig.3.2 (a) shows drain current (I_D) in both linear and log scale as a function of gate to source voltage (V_{GS}) for different gate work function at drain bias (V_{DS}) of 0.5V with a constant channel length of L=40 nm. To achieve a constant V_{th}, the channel doping (N_A) and source/drain doping (N_D) is considered $1.5*10^{18}$ cc^{-3} and $1*10^{20}$ cc^{-3} respectively in case of 4.52 eV device case. Similarly $N_A=1*10^{16}$ cc^{-3}, $N_D=1*10^{20}$ cc^{-3} for 4.6 eV device case and $N_A=1*10^{15}$ cc^{-3}, $N_D=9*10^{21}$ cc^{-3} for 4.7 eV device case.

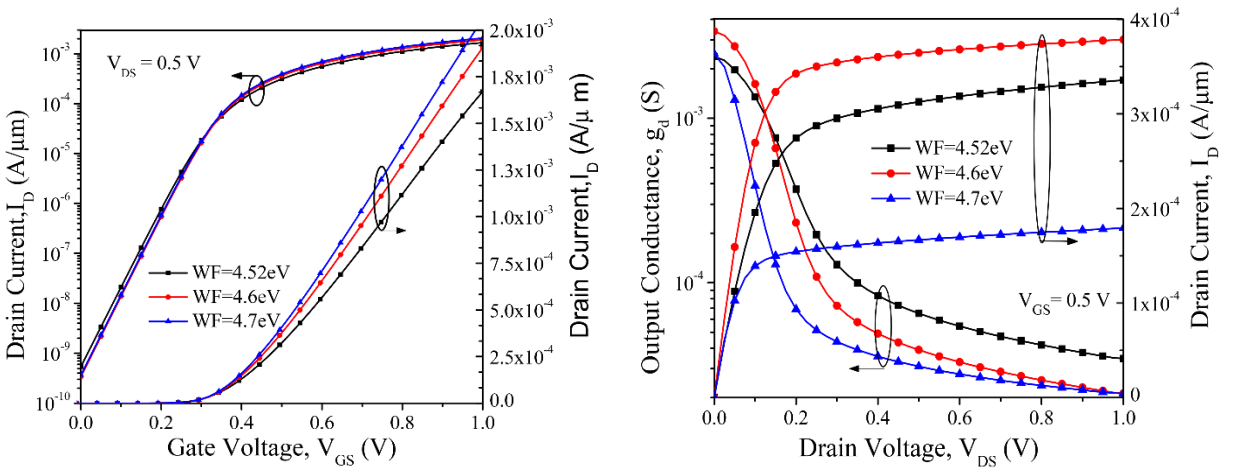

Figure 3.2 (a) Drain current (I_D) in both linear and log scale as a function of gate to source voltage (V_{GS}) (b) Output conductance (g_d) and drain current (I_D) with respect to drain to source voltage (V_{DS}) for different work functions.

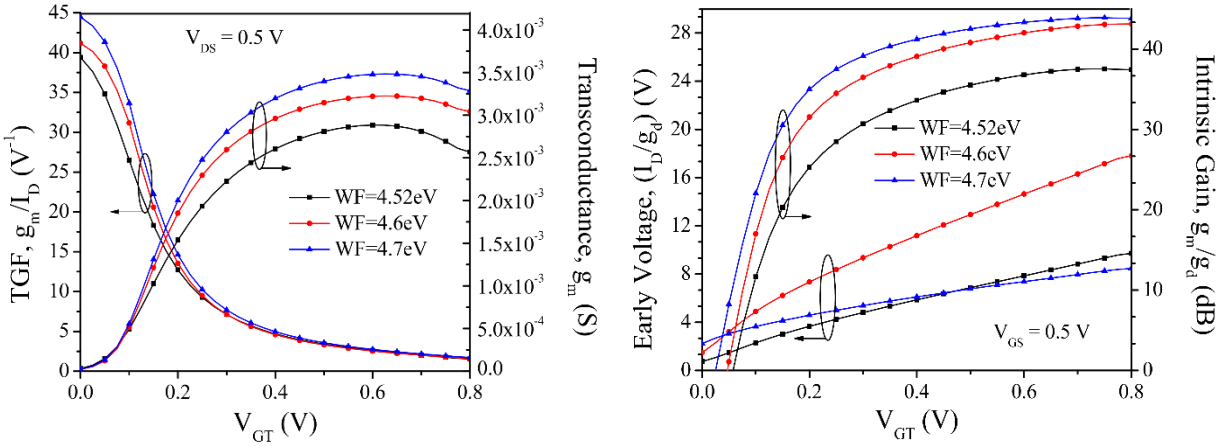

Figure 3.3 (a) Transconductance generation factor (TGF) and transconductance (g_m) as a function of gate over drive voltage (V_{GT}) (b) Early voltage (V_{EA}) and intrinsic gain (A_V) as a function of gate over drive voltage (V_{GT}) for different work functions.

The Sub threshold Slope (SS) is the major parameter for calculating the off state current. Furthermore, SS is calculated as:

$$SS(mV/dec) = \frac{\partial V_{GS}}{\partial(\log I_{DS})} \tag{3.2}$$

The SS value is extracted by calculating the inverse of maximum slope of V_G versus log (I_{DS}) curve. The value of DIBL is calculated as per the relation: $DIBL = \frac{\Delta V_{th}}{\Delta V_{ds}}$.

Where the logarithm is in base 10, I_{DS} is the drain current and V_{GS} is the gate voltage. The SS is always expressed in millivolts per decade. The typical value for the SS of Multigate MOSFET is 60 mV /decade, i.e. a 60 mV change in gate voltage brings about a tenfold change in drain current. The DIBL calculation is performed for V_{th} at V_{DS}=0.1 V and V_{DS}=1.0 V. Both the extracted value of SS and calculated value of DIBL for different work function is tabulated in Table 3.1. From the Fig. 3.2 (a), the on current increases as work function of the device increases and maximum for 4.7 eV. The off current is quiet constant for all device cases as V_{th} is maintained constant. Output conductance (g_d) and drain current (I_D) with respect to drain to source voltage (V_{DS}) for different work functions are plotted in Fig. 3.2 (b). From the figure, output current is maximum for 4.6 eV device case and lowest for 4.7 eV device case.

As far as analog circuits are concerned, the most important parameters are the transconductance g_m, output conductance g_{ds}, early voltage V_{EA}, transconductance-to-drain current ratio g_m/I_{ds}, intrinsic gain g_m/g_{ds}, terminal capacitances, i.e., gate-to-source capacitance C_{GS} and gate-to-drain capacitance C_{GD}, and cutoff frequency f_T. The g_m-V_{GT} and TGF-V_{GT} characteristics have been compared for various work functions in Fig.3.3 (a).

$$\text{As we know: } g_m = \frac{\partial I_{DS}}{\partial V_{GS}}, \quad \text{TGF}=g_m/I_D \tag{3.1}$$

The g_m/I_{DS} ratio demonstrates how efficiently the current is used to achieve a certain value of transconductance. The advantage of high transconductance-to-drain ratio is the realization of circuits operating at low supply voltage. From previous analysis, structures having 4.7 eV shows high drain current. According to the above relation it is clear that both g_m and TGF are directly dependent on the drain current. So, the structure having work function 4.7 eV give rise to higher values of transconductance and TGF when compared with others. Early voltage (V_{EA}) and intrinsic gain (A_V) as a function of gate over drive voltage (V_{GT}) for different work functions are presented in Fig.3.3 (b). An enormous improvement is observed in V_{EA} for work function 4.6 eV when compared to others. The intrinsic gain of the device, which is a ratio of transconductance and output conductance for various gate work functions is also displayed against gate over drive voltage (V_{GT}) for V_{DS}=0.5 V in Fig.3.3 (b). The intrinsic gain g_m/g_{ds} is a valuable figure of merit for operational transconductance amplifier. From the figure, the device having work function of 4.7 eV gives highest gain from others.

The simulated results for subthrshold slope (SS), maximum value of transconductance (g_m (max)) and maximum value of output conductance (g_d (max)) are outlined in Table 3.1. By comparing these values while work function varying from 4.52 eV to 4.6 eV, SS value is decreased by 0.83%, and g_d is decreased by 62.73%. Analog/RF figures of merit like transconductance (g_m), transconductance-to-drain-current ratio g_m/I_{DS}, intrinsic gain g_m/g_{ds}, early voltage V_{EA} are calculated and tabulated in Table 3.1. By comparing these devices having 4.6 eV provides better values in case of V_{EA}, gain and TGF as compared to 4.52 eV case and nearly equal values with 4.7 eV case.

Table 3.1 Electrostatic & Analog performances for different values of work function

Work Function (eV)	DIBL (mV/V)	SS (mV/decade)	g_m (S)	g_d (S)	V_{EA} (V)	Gain, A_V (dB)	TGF (V^{-1})
		V_{DS}=0.5V					
4.52	20.43	62.58	2.56E-03	3.45E-05	9.71	37.42	39.395
4.6	19.96	62.06	3.04E-03	2.12E-05	17.81	43.12	41.173
4.7	21.48	63.23	3.28E-03	2.11E-05	8.46	43.81	41.186

Fig. 3.4 shows the intrinsic capacitances (C_{gs} & C_{gd}) as a function of V_{GT} for both subthreshold or weak inversion and superthreshold or strong inversion regions. As shown in figure, in the subthreshold regime, the intrinsic capacitance parameters have low values which increase slowly; however, in the superthreshold region, they increase swiftly. This is because of the increase in the fringing field lines emanating from the gate edges. Thus, the total capacitance $C_{gg} = C_{gs} + C_{gd}$ follows the same nature as the intrinsic capacitances. The device having work function 4.7 eV shows high value for C_{gs} & device having 4.52 eV gives high C_{gd} when compared to others. However, in case of 4.6 eV, both the intrinsic capacitance values are minimum which in turns to high cutoff frequency. Cutoff frequency f_T is one of the most important parameters for evaluating the RF performance of the device. Generally, f_T is the frequency when the current gain is unity.

$$f_T = \frac{g_m}{2\pi\left(C_{GS} + C_{GD}\right)} = \frac{g_m}{2\pi C_{GG}} \tag{3.2}$$

Where g_m is the transconductance; C_{GG}, C_{Gs}, and C_{GD} are the total gate capacitance, gate-to-source capacitance, and gate-to-drain capacitance respectively.

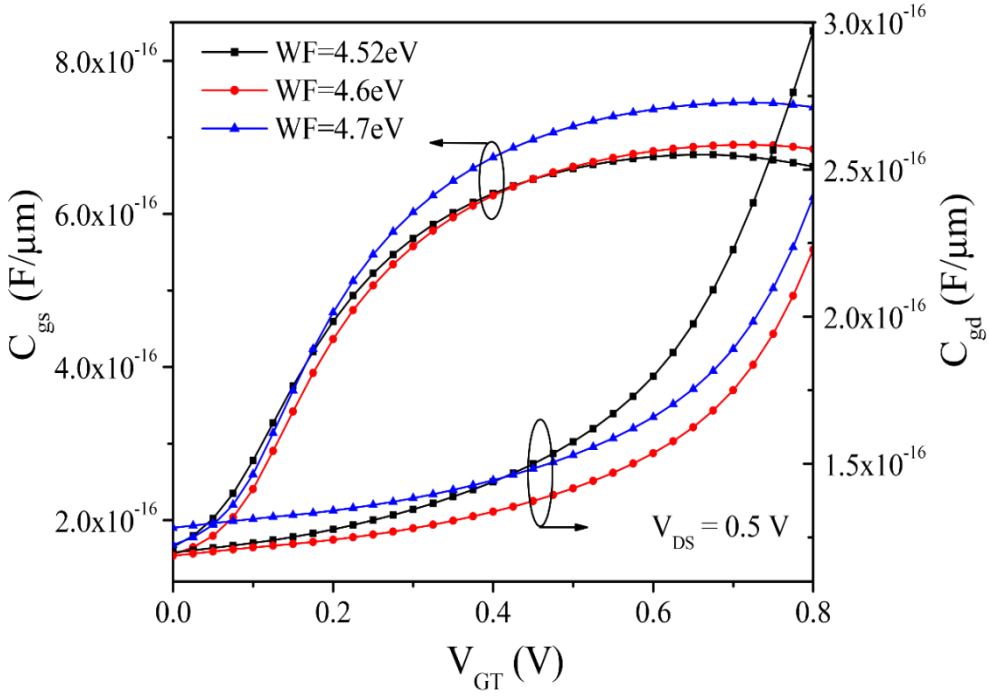

Figure 3.4 Gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) as a function of gate over drive voltage (V_{GT}) for different work functions.

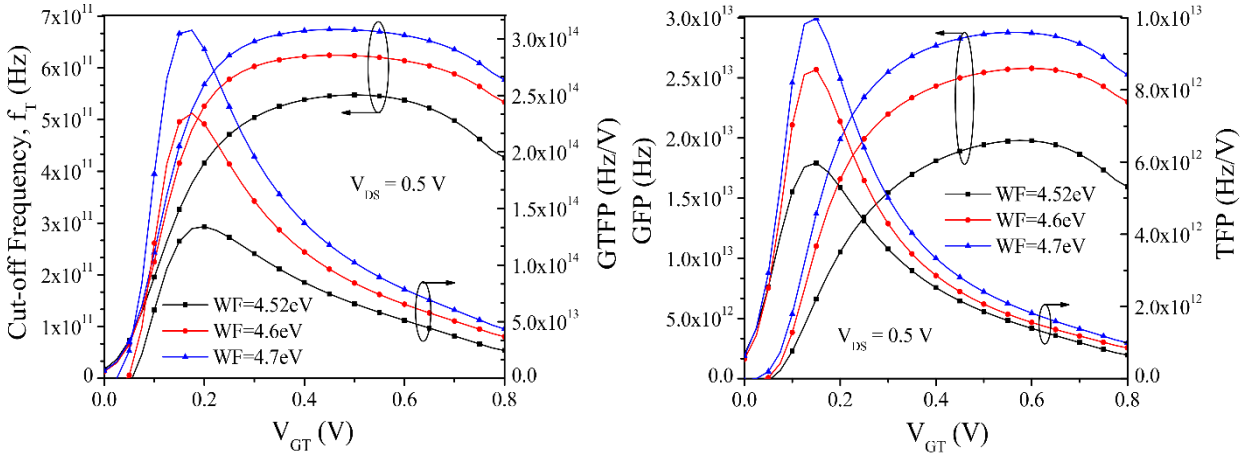

Figure 3.5 (a) Cut off frequency (f_T) and gain trans-conductance frequency product (GTFP) as a function of gate over drive voltage (V_{GT}) (b) Gain frequency product (GFP) and trans-conductance frequency product (TFP) as a function of gate over drive voltage (V_{GT}) for different work functions.

From Fig. 3.5 (a), the variations of f_T and GTFP can be observed with respect to V_{GT} for different values of work functions. Here, the value of f_T obtained for the device having high

work function i.e. 4.7 eV is higher as compare to its counterparts. This is because, the g_m value is high for work function 4.7 eV and is low for 4.52 eV case. To comprise these aspects of analog/RF circuit design, a unique figure of merit, GTFP (GTFP= g_m/g_{ds}* g_m/I_{DS}* f_T) is proposed. The variation of GTFP with gate voltage (V_{GT}) for different work functions is also shown in Fig. 3.5 (a). It is interesting to see that as the gate work function increases, the GTFP also increases and it is highest for the device having work function 4.7 eV. This is due to the reduction in peak electric field, lower output conductance of the device having work function 4.7 eV.

In Fig. 3.5 (b) gives the gain frequency product (GFP) i.e. g_m/g_{ds}*f_T against gate voltage (V_{GS}) for different values of work functions. From the figure, the value of GFP increases as work function increases and reaches utmost for the device having work function 4.7 eV. The product of g_m/I_{DS} and f_T represents a trade-off between power and bandwidth and is utilized in moderate to high speed designs. Transconductance frequency product (TFP) as a function of V_{GS} for different values of work function is also plotted in Fig. 3.5 (b). From the figure, it is clear that the device having higher work function gives higher TFP values from others. This is due to the high frequency values for higher work function devices.

These simulated results may be slightly higher than those of the experimental results, since, some considered parasitic parameters may be smaller than those of the real case, such as gate-to-source/drain capacitance, source/drain contact resistance. Cutoff frequency f_T, maximum oscillation frequency f_{max}, transconductance frequency product TFP= g_m/I_{DS}* f_T, and GTFP (GTFP= g_m/g_{ds}* g_m/I_{DS}* f_T) are compared for various gate work function.

Table 3.2 RF FOMs for different values of work functions

Work Function (eV)	C_{gs} (fF)	C_{gd} (fF)	f_t (GHz)	GFP (GHz)	TFP (GHz/V)	GTFP (GHz/V)
4.52	0.673	0.297	547.262	1.98E+04	5.98E+03	1.32E+05
4.6	0.690	0.222	624.471	2.58E+04	8.56E+03	2.34E+05
4.7	0.745	0.240	674.428	2.87E+04	9.98E+03	3.08E+05

All the extracted values for analog/RF FOMs are tabulated in Table 3.2. Similarly, as work function increases from 4.52 eV to 4.6 eV, gain of the device increases by 15.23% and cut off

frequency (f_T) increases by 14.10%. Due to all these advantages we fixed the work function as 4.6 eV for further simulations.

3.4.2 Variation of Channel Length

In order to optimize the channel length of the device, we did the same analysis as done in the work function section for four different channel lengths as 60 nm, 50 nm, 40 nm, and 30 nm. However, for analog/RF performance comparison among all the channel length cases, V_{th} kept constant by adjusting work function between 4.6 eV and 4.7 eV.

The I_D-V_{GS} transfer characteristics both in linear and log scales have been shown in Fig. 3.6 (a) for different configurations at V_{DS}=0.5V. The V_{th} is maintained a constant value for all the device cases at V_{DS}=0.1V as a consequence of the leakage current is quite constant. Here, different channel lengths are considered and have been compared for V_{DS}=0.5V at a fixed V_t. As channel length decreases, it gives rise to high drain current because of the relation $I_D \propto 1/L$. However, from the log scale, the leakage current is also prominent for lower channel lengths.

Drain current (I_D) and output conductance (g_d) against drain to source voltage (V_{DS}) for different cases at V_{GS}=0.5V are presented in Fig.3.6 (b). As per the Fig.3.6 (b), the drain current is increasing with decrease in channel length which in turn makes; the g_d high for lower L devices as $g_d=\partial I_D/\partial V_{DS}$. As we know from the literatures that gain and early voltage are inversely proportional to output conductance, so the device having lower L gives higher gd which comprises lower gain and early voltage of the device.

Transconductance generation factor (TGF) and transconductance (g_m) as a function of gate over drive voltage ($V_{GT}=V_{GS}-V_{th}$) are presented in Fig.3.7 (a). From the figure, it is clear that as the channel length decreases the g_m value is increasing because of high drain current.

$$I_{DS}(nA) = 100.\frac{W}{L}.e^{q(V_{GS}-V_T)/\eta kT} \tag{3.3}$$

where W : width of the channel, L: Channel Length, q: Electronic Charge, V_{GS}: Gate to Source Voltage, V_T: Threshold Voltage,

k: Boltzman Constant, T: Temperarure in Kelvin, η: Body factor and is proportional to the change in gate voltage with a change in channel potential: i.e $\eta = \frac{\partial V_{GS}}{\partial \varphi_S}$

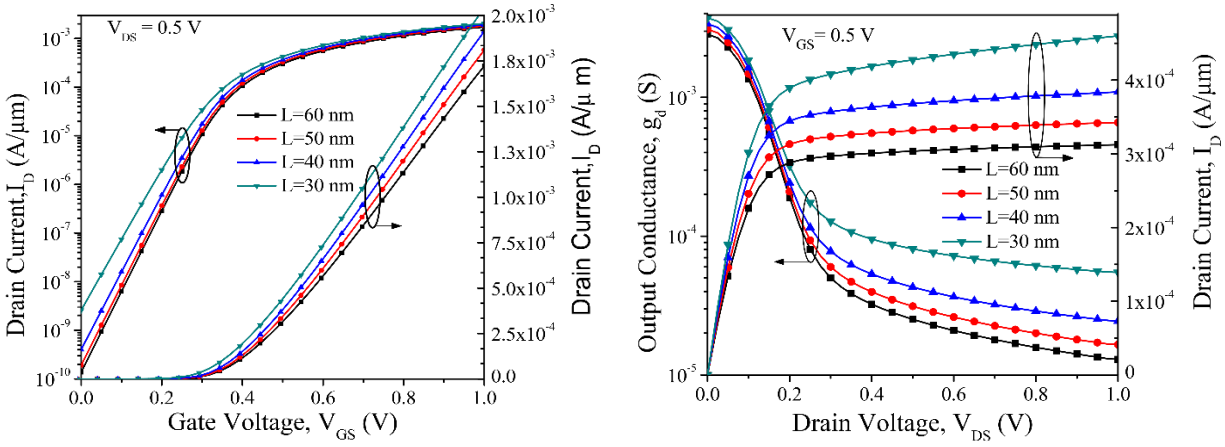

Figure 3.6 (a) Drain current (I_D) in both linear and log scale as a function of gate to source voltage (V_{GS}) (b) Output conductance (g_d) and drain current (I_D) with respect to drain to source voltage (V_{DS}) for different channel lengths.

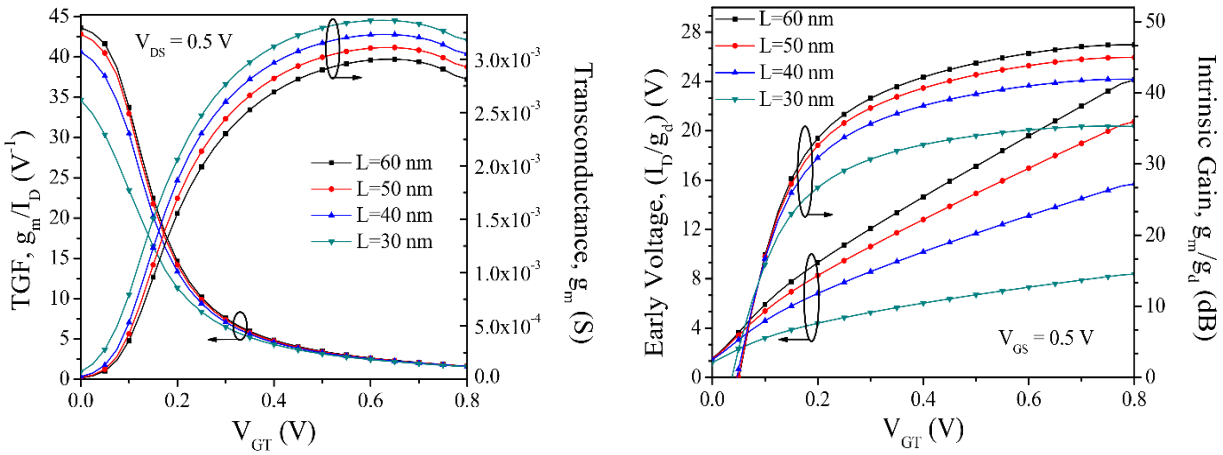

Figure 3.7 (a) Transconductance generation factor (TGF) and transconductance (g_m) as a function of gate over drive voltage (V_{GT}) (b) Early voltage (V_{EA}) and intrinsic gain (A_V) as a function of gate over drive voltage (V_{GT}) for different channel lengths.

According to equation (3.3), the drain current is inversely proportional to the channel length. So, as the channel length decreases then drain current increases and because of this both g_m and g_d is increased for lower channel lengths. The g_m/I_{DS} ratio demonstrates how efficiently the current is used to achieve a certain value of transconductance. The advantage of high transconductance-to-drain ratio is the realization of circuits operating at low supply voltage. As shown in the figure, g_m/I_{DS} is maximized in the subthreshold region of device operation. From the Fig. 3.7 (a), it is clear that the structure having channel length 60 nm shows higher g_m/I_{DS} ratio as compare to others and it decreases as channel length decreases.

Fig. 3.7 (b) shows the variation of the Early voltage (V_{EA}) and intrinsic gain (A_V) as a function of gate over drive voltage (V_{GT}) for different channel lengths. For better analog performance the V_{EA} and A_V should be as high as possible. An enormous improvement is observed in V_{EA} for channel length L=60 nm as compared to others.

The intrinsic gain of the device, which is a ratio of transconductance and output conductance for various channel lengths is plotted against gate voltage (V_{GS}) for V_{DS}=0.5 V is shown in Fig.3.7 (a). The intrinsic gain g_m/g_{ds} is a valuable figure of merit for operational transconductance amplifier. From the figure, the device having channel length 60 nm gives highest gain from others and it decreases as the channel length decreases.

Table 3.3 Electrostatic & Analog performances for different values of channel lengths

Channel Length (nm)	DIBL (mV/V)	SS (mV/decade)	g_m (S)	g_d (S)	V_{EA} (V)	Gain, A_V (dB)	TGF (V^{-1})
		V_{DS}=0.5V					
L=60	20.71	62.31	2.81E-03	1.29E-05	24.130	46.742	43.637
L=50	21.12	63.12	2.93E-03	1.65E-05	20.737	44.969	42.840
L=40	37.24	65.95	3.05E-03	2.45E-05	15.787	41.921	40.639
L=30	49.88	68.35	3.18E-03	5.48E-05	8.499	35.458	34.669

Both the extracted values of SS and calculated values of DIBL for different channel lengths are tabulated in Table 3.3. The DIBL calculation is performed for V_{th} at V_{DS}=0.1 V and V_{DS}=1.0 V. From the table, it is clear that the SS value increases as channel length decreases and it is very high for channel length 30 nm. Similarly, the DIBL value also increases as channel length decreases and it gives a maximum value for channel length of 30 nm. These two parameters are very important for short channel effects, which should be minimized. Hence, the SCEs are heavily affecting the lower dimension devices. The methods of calculating SS and DIBL are already discussed in the work function section. The maximum values for g_m, g_d, V_{EA}, A_V, TGF are also tabulated in Table 3.3. As the drain current (I_D) is increasing for lower channel length devices, which consequently increases g_m values for these devices. However, because of high g_d, the V_{EA}, and A_V becomes lower as L decreases. Coming from L=60 nm to 30 nm, the DIBL and SS values are more prominent for lower channel length devices and also the TGF and Gain are decreases as L decreases.

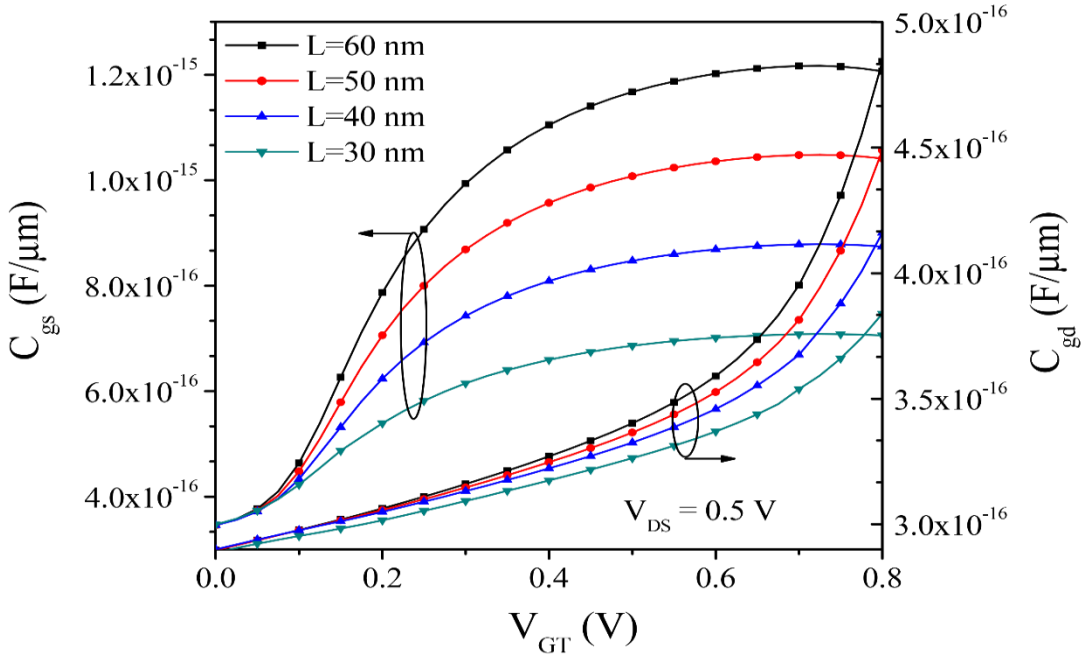

Figure 3.8 Gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) as a function of gate over drive voltage (V_{GT}) for different channel lengths.

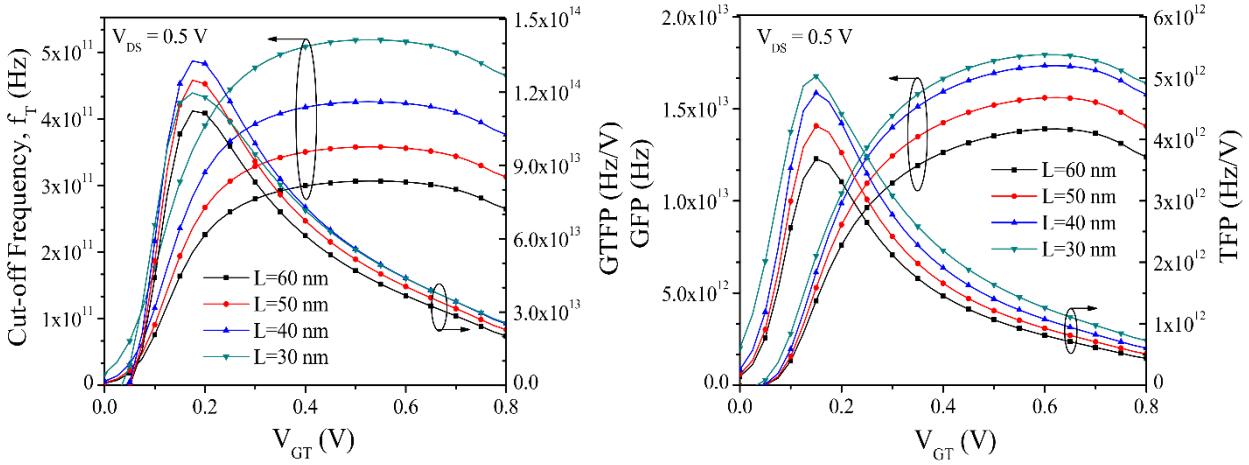

Figure 3.9 (a) Cut off frequency (f_T) and gain trans-conductance frequency product (GTFP) as a function of gate over drive voltage (V_{GT}) (b) Gain frequency product (GFP) and trans-conductance frequency product (TFP) as a function of gate over drive voltage (V_{GT}).

Fig. 3.8 shows the intrinsic capacitances (C_{gs} & C_{gd}) as a function of V_{GT} for both subthreshold or weak inversion and superthreshold or strong inversion regions. As shown in figure, in the subthreshold regime, the intrinsic capacitance parameters have low values which increase slowly; however, in the superthreshold region, they increase swiftly. This is because of the increase in the fringing field lines emanating from the gate edges. The device having channel

length 60 nm shows higher values of intrinsic capacitances (both C_{gs} & C_{gd}) and it decreases as channel length decreases. From Fig. 3.9 (a), the variations of f_T and GTFP can be observed with respect to V_{GT} for different values of channel lengths. Here, the value of f_T obtained for the device having low channel length is higher and it gradually decreases as the channel length decreases. In the work function section it is already discussed that f_T is inversely proportional to the intrinsic capacitances (C_{gs} & C_{gd}). So, f_T value is low due to high capacitance values for higher channel length devices. The variation of GTFP with gate voltage (V_{GS}) for different work functions is shown in Fig. 3.9 (a). It is interesting to see that the device having channel length 40 nm shows a higher GTFP value as comparison to others. This is due to the reduction in peak electric field, lower output conductance of the device having channel length 40 nm. The GTFP value is very low for L=30 nm. The product of g_m/I_{DS} and f_T represents a trade-off between power and bandwidth and is utilized in moderate to high speed designs.

Fig. 3.9 (b) gives the gain frequency product (GFP) i.e. $g_m/g_{ds}*f_T$ and TFP against gate over drive voltage (V_{GT}) for different values of channel lengths. From the figure, the value of GFP increases as channel length decreases and reaches utmost for the device having channel length 30 nm. The same figure also shows transconductance frequency product (TFP) as a function of V_{GT} for different values of channel lengths. From the figure it is clear that the device having channel lengths 40 nm and 30 nm gives higher TFP values as comparison to others.

Table 3.4 RF performances for different values of channel lengths

Channel Length (nm)	C_{gs} (fF)	C_{gd} (fF)	f_t (GHz)	GFP (GHz)	TFP(GHz/V)	GTFP (GHz/V)
L=60	1.207	0.484	306.78	4.57E+03	3.69E+03	1.12E+05
L=50	1.041	0.449	358.00	5.27E+03	4.22E+03	1.25E+05
L=40	0.874	0.416	425.80	6.12E+03	4.76E+03	1.33E+05
L=30	0.706	0.384	518.79	7.02E+03	5.03E+03	1.37E+05

All the extracted values for analog/RF FOMs are plotted in Table 3.4 for different values of channel lengths. As we have already seen from Table 3.3, the short channel effects are heavily affecting the device while channel length decreases. So, by comparing all the DC and AC parameters the channel length is fixed as 40 nm for further simulations.

3.4.3 High-k dielectrics in DG MOSFETs

In order to study the effect of different high-k dielectric materials on various parameters, we did the same analysis as in the work function and channel length section for four different high-k dielectrics as k=7.5, k=24, and k=30 by taking direct and gate stack configuration. Here different dielectric materials are considered as gate oxide for both single and double layer configurations and have been compared for V_{DS}=0.5 V. Different device structural cases are maintained with electrical oxide thickness (EOT) as 1.1nm as shown in Table 3.5.

Table 3.5 Structural cases considered in simulation

Device	Interfacial layer		High-k Layer		EOT (nm)
	T_{ox} (nm)	ε_{ox}	T_{hk} (nm)	k	
D1	1.1	3.9	0.0	n/a	1.1
D2	2.1	7.5			
D3	6.8	24			
D4	8.5	30			
D5	0.6	3.9	0.96	7.5	
D6			3.08	24	
D7			3.85	30	

Here different dielectric materials are considered and have been compared for V_{DS}=0.5V at a fixed channel length, L=40 nm. The work function is tuned between 4.6 eV and 4.7 eV to achieve a constant V_{th}=0.2 V. The I_D-V_{GS} transfer characteristics both in linear and log scales have been shown in Fig. 3.10 (a) for different configurations at V_{DS}=0.5V. The V_{th} is maintained a constant value for all the device cases at V_{DS}=0.1V as a consequence of the leakage current is quite constant. One can notice from the Fig.3.10 (a), leakage current (I_{off}) is varying in between 10^{-8} A/µm and 10^{-10} A/µm for all cases. From the figure it is clear that with increasing high-k dielectric permittivity for single layer, the on current increases but simultaneously it gives high leakage current. In the device cases of high-k with interfacial oxide (SiO_2) layer, the gate leakage current reduces. The capacitive coupling due to gate increases that decreases the leakage current.

Drain current (I_D) and output conductance (g_d) against drain to source voltage (V_{DS}) for different cases at V_{GS}=0.5V are presented in Fig.3.10 (b). As per the Fig.3.10 (b), the drain current is increasing with increase in high-k dielectric permittivity for single layer configurations which in turn makes; the g_d high for these configurations. CMOS Analog circuits require transistors with low output conductance (g_d) in order to achieve high gain. High g_d means, low output resistance which resulting an increase in I_D with V_{DS} in saturation regime. The components are associated with this increase, namely channel length modulation (CLM) and

DIBL. Also a low g_d propagates a higher drain current to output conductance ratio, which is nothing but the early voltage of the device. So, from Fig.3.10 (b), the device D5 has a good control over CLM and DIBL owing to low g_d value.

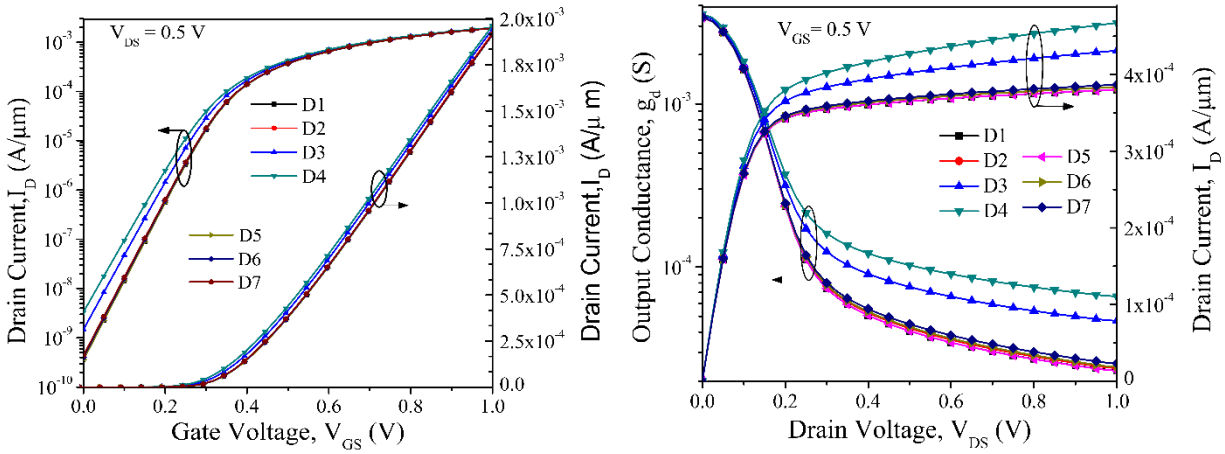

Figure 3.10 (a) Drain current (I_D) in both linear and log scale as a function of gate to source voltage (V_{GS}) (b) Output conductance (g_d) and drain current (I_D) with respect to drain to source voltage (V_{DS}) for different device cases.

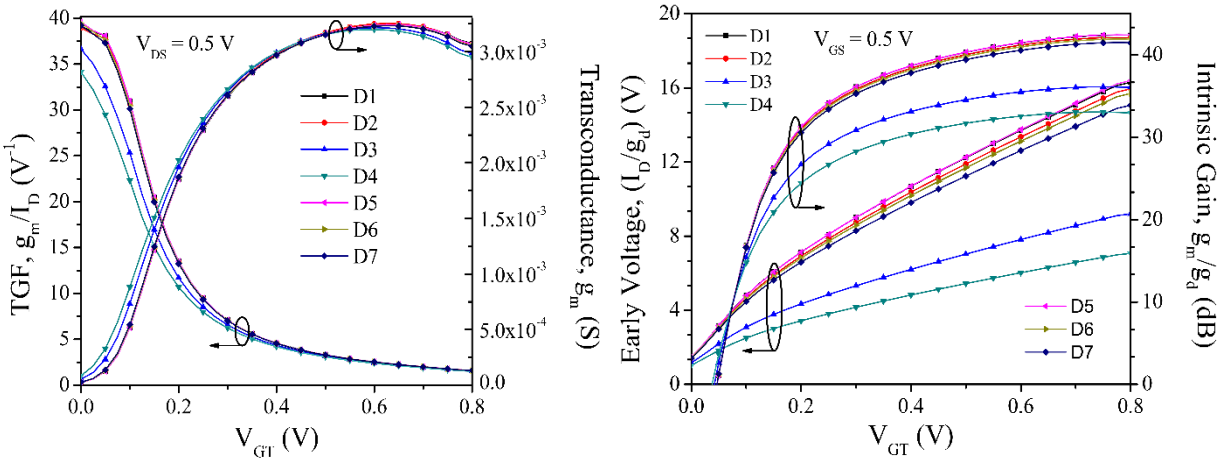

Figure 3.11 (a) Transconductance generation factor (TGF) and transconductance (g_m) as a function of gate over drive voltage (V_{GT}) (b) Early voltage (V_{EA}) and intrinsic gain (A_V) as a function of gate over drive voltage (V_{GT}) for different device cases.

A combined plot for transconductance generation factor (TGF) and transconductance (g_m) as a function of gate over drive voltage ($V_{GT}=V_{GS}-V_{th}$) presented in Fig.3.11 (a). Transconductance of the MOSFET which determines the gain of the amplifier is formulated as $g_m = \partial I_D / \partial V_{GS}$. The higher carrier transport efficiency in an improved transconductance for the gate stack configurations is preferred for analog applications. TGF demonstrates the effective use

of the current to achieve a desired value of transconductance. The high value of TGF is advantageous to realize analog circuits which are operating at low supply voltage. The ideal value of TGF is limited to ≈40V^{-1} at minimum SS of 60 mV/decade of the device. The variation of TGF occurs at subthreshold region of operation for all devices under study. All most same TGF achieved in strong inversion. From Fig. 3.11 (a), it is clear that the double layer structures with high dielectric materials exhibits higher TGF as compared to single layer structures. In single layer structures, as the dielectric permittivity increases the g_m/I_D ratio decreases and it becomes worst at k=30. Higher TGF is not good for high linearity microwave systems as lower TGF is not drawback since the power consumption in subthreshold region is very less.

Fig. 3.11 (b) shows the variation of the Early voltage (V_{EA}) and intrinsic gain (A_V) as a function of gate over drive voltage (V_{GT}). For better analog performance the V_{EA} and A_V should be as high as possible. As per Fig. 3.11 (b), the GS configuration exhibits higher early voltage as compared to their corresponding single layer configuration. Again, among from all the GS structures the high-k (k=7.5, i.e. D5 device case) shows the optimum result. This is due to improved SCEs. The intrinsic gain is a valuable figure of merit for operational transconductance amplifier. The results from Fig.3.11 (b), it is observed that with increase in dielectric permittivity for single oxide layer structures, the gain of the device becoming worst. The maximum value of g_m, g_d, V_{EA}, A_V, TGF were tabulated in Table 3.6. By comparing all the extracted parameters in Table 3.6, the device with high-k gate dielectric as Si_3N_4 i.e. device D5 shows a better result in terms of gain, V_{EA} and TGF.

Table 3.6 Electrostatic & Analog performances for different values of dielectric materials

Device	DIBL (mV/V)	SS (mV/decade)	g_m (S)	g_d (S)	V_{EA} (V)	Gain, A_V (dB)	TGF (V^{-1})
		V_{DS}=0.5V					
D1	20.71	62.31	3.07E-03	2.33E-05	16.304	42.402	39.092
D2	21.12	62.47	3.06E-03	2.40E-05	15.954	42.105	38.957
D3	37.24	65.81	2.98E-03	4.69E-05	9.205	36.077	36.650
D4	49.88	68.03	2.95E-03	6.61E-05	7.069	32.984	34.148
D5	19.69	61.32	3.17E-03	2.27E-05	16.897	43.436	39.589
D6	20.28	62.56	3.05E-03	2.45E-05	15.698	41.921	39.439
D7	21.65	62.76	3.05E-03	2.57E-05	15.065	41.489	39.220

The important high frequency or RF circuit parameter includes cut off frequency (f_T), transconductance frequency product (TFP), gain frequency product (GFP) and gain

transconductance frequency product (GTFP). The intrinsic capacitances are shown in Fig. 3.12 (gate to source capacitance, C_{gs} & gate to drain capacitance, C_{gd}) as a function of V_{GT} for both sub-threshold and super-threshold or strong inversion regions. The extraction of intrinsic capacitances C_{gs} and C_{gd} are done through AC small signal analysis after post-processing operation of DC solution. The capacitances between each pair of electrode are calculated by single AC frequency (1MHz) solution during a DC ramp voltage from 0V to 1V with a step of 0.025V. To obtain the convergence in the inversion/deep depletion region, the DIRECT parameter is added for more robust solution. The C_{gs} & C_{gd} values of the device increase with k. This is caused by the increased fringing field density in the single layer high-k devices. However, GS configurations demonstrate better values for intrinsic capacitances. It is observed that both the C_{gs} & C_{gd} starts increasing as V_{GT} increases until saturation. After saturation, both the values become constant, as expected, as the additional V_{DS} can't affect the junction. Cut-off frequency f_T is one of the most important parameters for evaluating the RF performance of the device. Generally, f_T is the frequency when the current gain is unity.

From Fig.3.13 (a), the variations of f_T can be observed with respect to V_{GT} for different proposed structures with high-k dielectric materials as gate oxide. It can be seen from the figure that f_T decreases as 'k' increases in case of single layer structures. However, it displays required values for GS configurations. The difference in f_T is mainly due to the difference in g_m, as observed in Fig.3.11 (a), and partially due to the higher value of total capacitance (C_{gs}+C_{gd}), as observed in Fig.3.12. The peak point of f_T corresponds to the point between the minimum gate-drain/source capacitance and peak of transconductance. It is also clear from Fig.3.13 (a) that f_T is highest for the device D5 reflecting superior gate controllability, and hence higher transconductance and lower parasitic gate capacitances as compared to other devices considered in our study. A unique figure of merit for analog/RF performances is the gain transconductance frequency product (GTFP) is also plotted in Fig.3.13 (a) for both the switching speed and the intrinsic gain. The peak value of GTFP is achieved at V_{GS}=0.375V for all the configurations, where the level of drain current (I_D) is quite low, i.e. $I_D \approx 10^{-5}$A/μm. It is interesting that the voltage corresponds to V_{GS} just above 175mV of the threshold voltage of the device. This allows the circuit designer to determine the best region of operation by trading off among gain, transconductance and speed. Here also device D5 shows higher GTFP as compared to other configurations. This is because of higher f_T, g_m and low g_d value of D5 device.

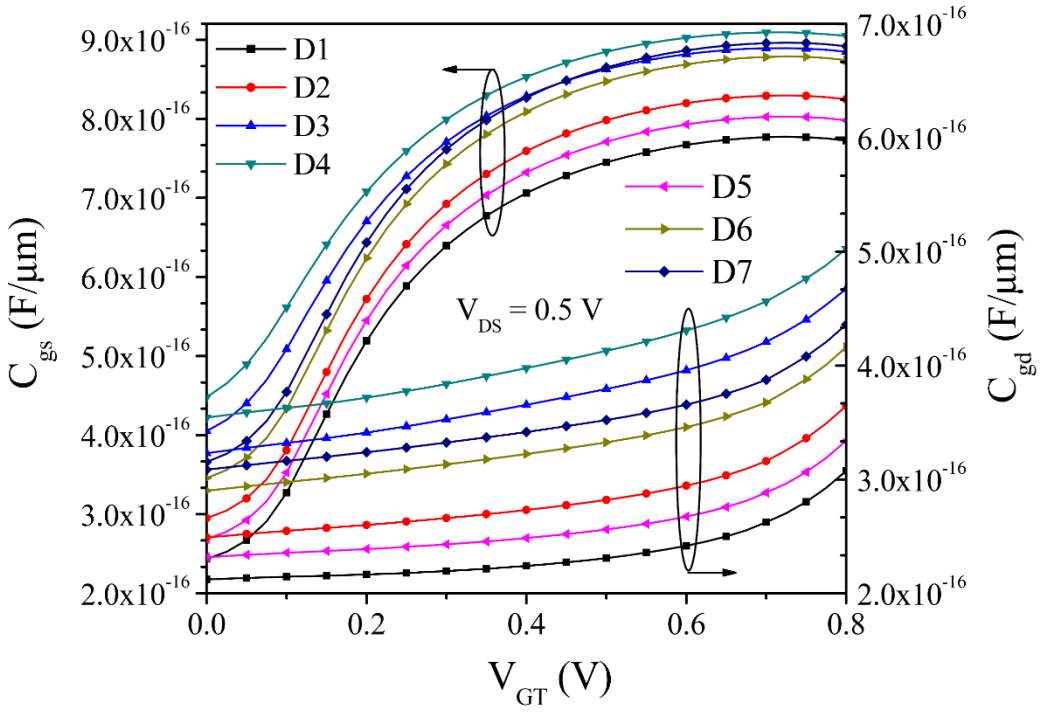

Figure 3.12 Gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) as a function of gate over drive voltage (V_{GT}) for different device cases.

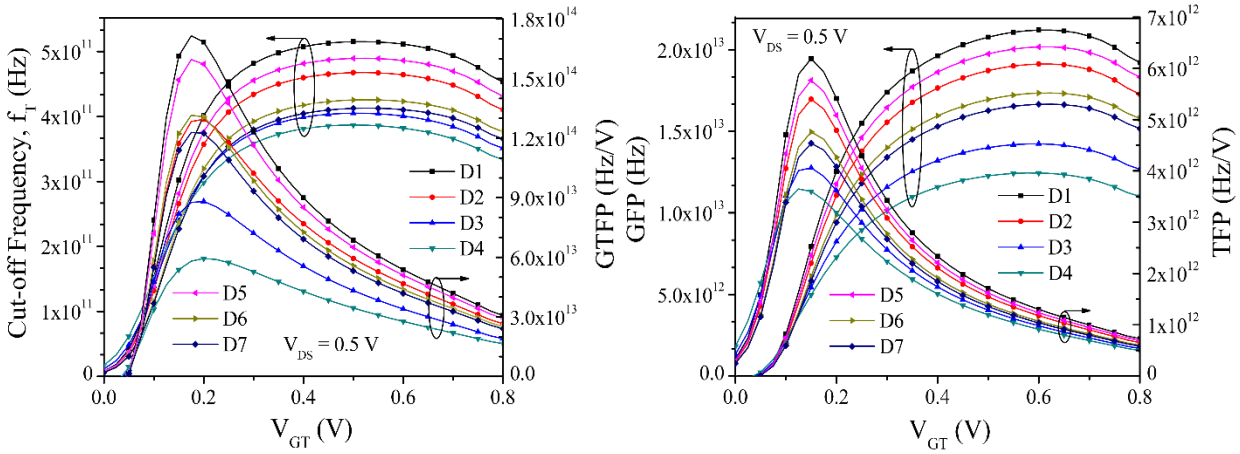

Figure 3.13 (a) Cut off frequency (f_T) and gain trans-conductance frequency product (GTFP) as a function of gate over drive voltage (V_{GT}) (b) Gain frequency product (GFP) and trans-conductance frequency product (TFP) as a function of gate over drive voltage (V_{GT}).

The product of g_m/I_D and f_T i.e. TFP represents a tradeoff between power and bandwidth and is utilized in moderate to high speed designs. Similarly, gain frequency product i.e. GFP, is also very important parameter for operational amplifiers in high frequency application. Both the GFP and TFP against V_{GT} for V_{DS}=0.5 V are plotted in Fig.13 (b). From the figure, the GFP and TFP are started linearly increasing as V_{GT} increases in subthreshold region and hold an optimum

value then start decreasing in saturation region. By comparing between different configurations, the GS structures are showing better GFP and TFP values as compare to single layer structures. This is due to the high g_m and f_T values of GS structures.

The maximum value of RF FOMs like f_T, GFP, TFP and GTFP are compared for various DG configurations at V_{DS}=0.5 V in Table 3.7. By comparing the data given in both the tables, the GFP and GTFP values are better in case of V_{DS}=0.1 V i.e. in the subthreshold mode of operation. If we compare between different device cases, the configuration having Si_3N_4 gate oxide as gate stack i.e. D5 shows optimum results than its counterparts in terms of f_T, GFP, TFP and GTFP. By comparing the above said parameters with the variation of gate dielectrics, it is concluded that GS configurations with high-k dielectric materials as Silicon Nitride (i.e D5 device) exhibit better performance as compare to other configurations. So the proposed nanoscale DG-MOSFET structure D5 may be considered as a suitable candidate for the design of Analog and RF circuits.

Table 3.7 RF performances for different values of dielectric materials

Device	C_{gs} (fF)	C_{gd} (fF)	f_t (GHz)	GFP (GHz)	TFP(GHz/V)	GTFP (GHz/V)
D1	0.798	0.334	489.18	2.02E+04	5.54E+03	1.60E+05
D2	0.825	0.365	467.63	1.91E+04	5.21E+03	1.28E+05
D3	0.885	0.467	404.92	1.42E+04	3.89E+03	0.87E+05
D4	0.905	0.502	386.65	1.24E+04	3.43E+03	0.58E+05
D5	0.772	0.308	515.55	2.12E+04	5.93E+03	1.72E+05
D6	0.874	0.416	425.80	1.73E+04	4.62E+03	1.32E+05
D7	0.892	0.436	412.89	1.67E+04	4.41E+03	1.23E+05

3.5 Summary

Here the calibration and optimization of the device has been examined through extensive device simulation. Both static and dynamic performances of DG silicon-on-insulator (SOI) MOSFET has been analyzed by varying gate work function (φ_m), channel length (L) and gate dielectric materials. However, for better comparison between all analog/RF performances we adjusted threshold voltage as a constant value for all cases. While varying work function, the V_{th} kept constant by adjusting the doping concentration of channel and source/drain. Similarly, for other two technology parameter variation i.e., channel length and high-k dielectric material, the constant V_{th} is achieved by tuning the work function of the device. First a study is made for the

SCEs like SS, DIBL and also for important analog/RF figures of merit (FOMs) like transconductance generation factor (g_m/I_d), intrinsic gain ($A_v=g_m/g_d$), cutoff frequency ($f_T = g_m/2\pi C_T$) and transconductance frequency product (TFP= g_m/I_d*f_T), gain frequency product (GFP=A_v*f_T) and gain transconductance frequency product (GTFP= A_v*g_m/I_d*f_T) by varying the gate work function as 4.52 eV, 4.6 eV and 4.7 eV at a constant V_{th}. By comparing the above said parameters with the variation of work function, we conclude that the device having work function 4.6 eV shows better results as compared to its counterparts. Similar studies and comparisons are made between the parameters by varying channel length as 60 nm, 50 nm, 40 nm, and 30 nm with a fixed work function as 4.6 eV. From the study, the device having 40 nm channel length is the optimum among other considered channel lengths. Finally to study the effect of various gate dielectric materials, we fixed the work function as 4.6 eV and channel length as 40 nm and varying the permittivity as k=7.5, k=24, and k=30 for both single layer and double layer/gate stack configurations. Similarly, by comparing all the parameters and varying the gate dielectrics for both single layer and double layer structures, finally, it is concluded that the double layer structure with k=7.5 shows better results among all others. Therefore, for the next chapter to get an optimum device the parameters are fixed as L=40 nm, φ_m=4.6 eV and k=7.5 (Gate Stack configuration).

Chapter 4

Analysis of DC & Analog/RF Performance of FD-S-GS-DG MOSFET

4.1. Introduction

The objective of this chapter is to design a optimized structure based on previous chapters and study its performance. Up till now we have studied the role of various MOS parameters like germanium concentration (X), body doping concentration (N_A), strained silicon thickness (t_{Si}), oxide thickness (t_{ox}) and gate metal work function (φ_M) influencing the surface potential, threshold voltage and electric field for a Fully Depleted Strained Silicon on Insulator (FDSSOI) MOSFET in chapter 2 and the effect of device design engineering on the analog/RF performance of nanoscale DG MOSFET by taking three different variables as gate work function, channel length and gate oxide in chapter 3. In addition, including the SCEs like SS, DIBL, I_{on}/I_{off} ratio we examined important analog/RF figures of merits (FOMs) like transconductance generation factor (g_m/I_d), early voltage ($E_v=I_{ds}/g_d$), intrinsic gain ($A_v=g_m/g_d$), cutoff frequency ($f_T = g_m/2\pi C_T$) and transconductance frequency product (TFP= g_m/I_d*f_T), gain frequency product (GFP=A_v*f_T) and gain transconductance frequency product (GTFP= A_v*g_m/I_d*f_T) in chapter 3.

In this chapter an optimum device is designed by considering all the best device parameters from chapter 2 and chapter 3. A fully depleted strained gate stack double gate (FD-S-GS-DG) MOSFET is designed and some parameters are studied by varying the germanium concentration (X).

4.2. Device Design

The schematic structure of FD-S-GS-DG MOSFET is shown in Fig. 4.1. In this structure the channel length (L) and Source/Drain length (L_S/L_D) is fixed as 40nm, the silicon thickness (t_{Si}) as 10nm and a uniform density of N_D as 10^{20} cm^{-3} is taken. The channel is doped with (N_A)

10^{16} cm^{-3}. Gate stack configuration is designed by considering SiO_2 layer thickness is fixed at 0.6nm and above this layer 0.5nm equivalent thickness of high-k layer, HfO_2 (k=24) is deposited, so that the EOT reaches 1.1nm. The work function of the gate material is fixed at 4.6 eV. The Ge composition (X) in the layer SiGe is varied from 0 to 0.4 [60-66]

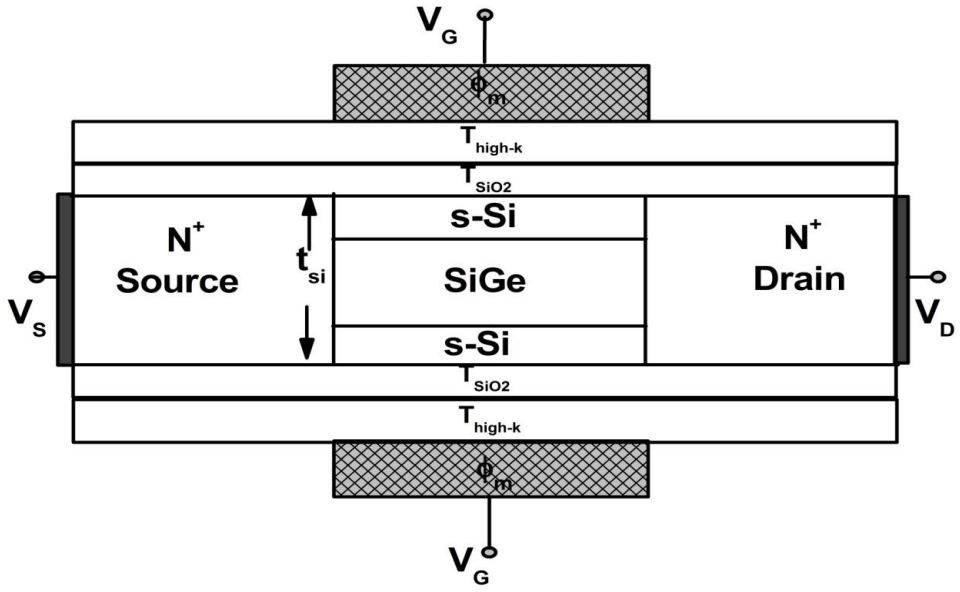

Figure 4.1 Schematic structure of FD-S-GS-Double Gate N-MOSFET

4.3. Simulation

All the models and method cosidered in chapter3 for simulation are also incorporated in chapter 4 .

4.4. Results and Discussion

Fig.4.2 (a) shows the variation of drain current (I_D) and transconductance (g_m) with respect to gate voltage (V_{GS}) for various Ge concentrations (X). From the figure, as the Ge concentration is increased, drain current and transconductance is also increased because of the enhancement of carrier mobility caused by the strained silicon and a decrease of surface roughness scattering. The output characteristic (I_D-V_{DS}) and output conductance (g_d) as a function of drain bias (V_{DS}) is plotted in Fig.4.2 (b). Here also, both the current and output conductance is more for strained silicon as compare to unstrained (X=0) silicon due to the same mobility effect.

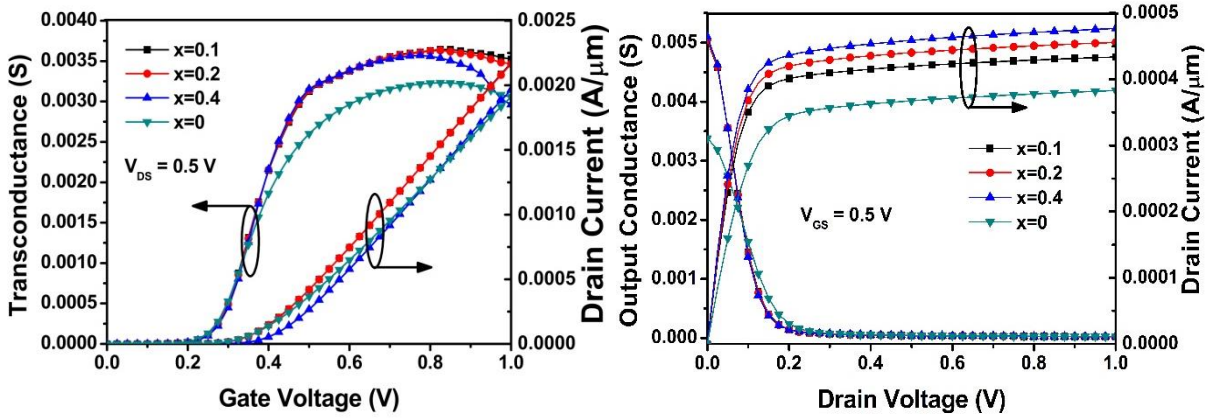

Figure 4.2 (a) Drain current (I_D) and transconductance (g_m) variation with Gate voltage (V_{GS}) for different Ge concentration (X) (b) Drain current (I_{DS}) and output conductance (gd) as a function of Drain voltage (V_{DS}) for different Ge concentration (X).

Table 4.1 Electrostatic parameters for different values of Ge Concentration

Ge Concentration (X)	V_{th} (V)	SS (mV/decade)	I_{DS} (max) (mA)	I_{off} (A)	Ion/Ioff
X=0.1	0.213	62.6723	2.11603	3.40E-10	6.22E+09
X=0.2	0.208	62.8793	2.16636	3.459E-10	6.26E+09
X=0.4	0.202	63.2893	2.17332	9.02E-10	2.40E+09
X=0	0.219	62.5057	1.91026	3.19E-10	5.99E+09

The simulated results for threshold voltage (V_{th}), subthrshold slope (SS), maximum value of on current (I_{on} (max)), off current (I_{off}), on-off ratio (I_{on}/I_{off}) are tabulated in Table 4.1. By comparing those values with Ge concentration (X) varying from 0 (unstrained) to 0.2 (strained), I_{on} is raised up to 13.4 %, and Ion/I_{off} is improved by 4.6 %. The SS value increases as x value increases and reaches its maximum for X=0.4.

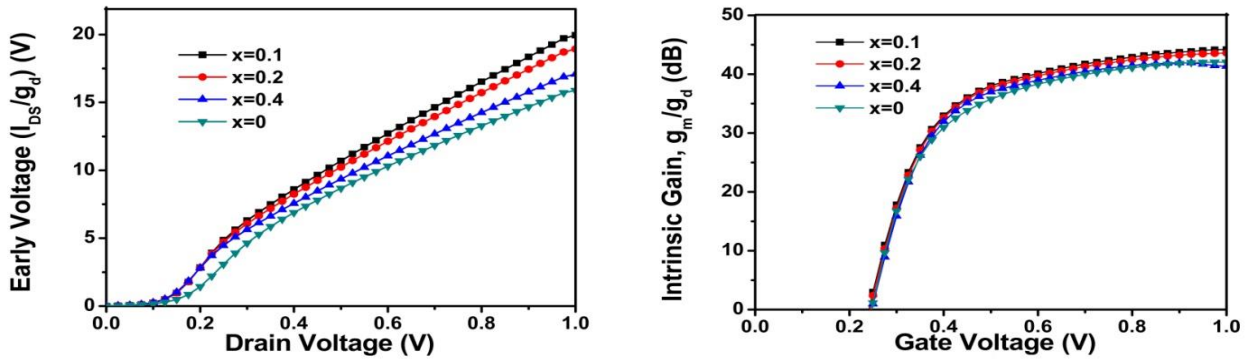

Figure 4.3 (a) Early voltage (E_v) variation with Drain voltage (V_{DS}) for different Ge concentration (X). (b) Intrinsic gain (A_V) as a function of Gate voltage (V_{GS}) for different Ge concentration (X).

Fig. 4.3 (a) shows the variation of the Early voltage E_v with drain bias for various Ge mole fractions (X) at a gate voltage of 0.5 V. The E_v is more for strained silicon as compare to unstrained silicon. It depicts highest value for X=0.1 and starts decreasing as x value increases. The intrinsic gain of the device, which is a ratio of transconductance and output conductance for various Ge concentrations is plotted against gate voltage (V_{GS}) for V_{DS}=0.5 V is shown in Fig.4.3 (b). The intrinsic gain g_m/g_{ds} is a valuable figure of merit for operational transconductance amplifier. Similarly, from the figure, the gain is high for strained silicon from its counterpart unstrained silicon and reaches its maximum value for X=0.1. It then starts decreasing as X value increases.

Table 4.2 Analog parameters for different values of of Ge Concentration

Ge concentration (X)	g_m (max) (mA)	g_d (max) (mA)	V_{EA} (V)	Gain (dB)	TGF (V^{-1})
X=0.1	3.57203	5.02637	19.947	41.344	40.87
X=0.2	3.63325	5.04749	18.933	43.599	41.98
X=0.4	3.64959	5.09755	17.081	44.194	42.08
X=0	3.2323	3.38049	15.882	42.046	39.62

All the extracted values for analog performance are tabulated in Table 4.2. Similarly, as Ge concentration (X) varies from 0 (unstrained) to 0.2 (strained), transconductance (g_m) of the device increases by 12.40%, output conductance (g_d) is increased by 49.31%, early voltage (E_v) is raised by 19.21%, gain of the device is increased by 3.6% and TGF is raised by 5.96%.

4.5. Summary

In this chapter, one optimum device, i.e. fully depleted strained gate stack double gate (FD-S-GS-DG) mosfet is designed and simulated to study some aspect of its performance. Both DC and Analog performances are studied by varying the Ge mole fraction (X). The increase in strain, i.e., equivalent Ge content, enhances the performance of FD-S-GS-MOSFET in terms of electrostatic parameters as well as in terms of analog parameters because of an increase in the carrier mobility. However, as demonstrated by our results, there are undesirable side effects with increasing equivalent Ge content (X=0.4) such as an increase in SS value and a decrease in I_{on}, g_m, E_v and Gain (A_v) which may affect the device characteristics and performance significantly. Therefore, from the results predicted in this chapter, we conclude that strained silicon up to some extent of Ge mole fraction shows better results in device performances.

Chapter 5

Conclusion & Scope for Future Work

5.1 Conclusions

- Continuous scaling in MOSFET devices degrade their performance as a result of leakage currents and short channel effects (SCEs) resulting from downscaling the device dimensions.
- To mitigate these short channel problems resulting from downscaling the device dimensions a device called Silicon-on-Insulator (SOI) MOSFET has been developed.
- To increase the density and enhance the performance of CMOS technology new materials into the classical single gate MOSFET like development of uniaxial/biaxial strain in the channel region to enhance the carrier mobility in the channel region and implementation of high-k dielectric material as gate oxide to minimize the gate leakage current and non-classical multi gate MOSFETs are developed.
- The increase in strain i.e. equivalent Ge content, enhances the performance of SSOI MOSFETs in terms of improved trans-conductance and speed because of an increase in the carrier mobility.
- However, as demonstrated by our results, there are still some undesirable side effects with increasing equivalent Ge content (more than 0.4) such as a roll-off in V_{th}, which may affect the device characteristics and performance significantly.
- Our analytical model accurately predicts the threshold voltage over a large range of device parameters and can be effectively used to design and characterize the nanoscale single-layer FD-SSOI MOSFETs with the desired performance.
- All SCEs like SS, DIBL and important analog/RF figures of merit (FOMs) like transconductance generation factor (g_m/I_{ds}), Early voltage ($E_v=I_{ds}/g_d$), intrinsic gain ($A_v=g_m/g_d$), cutoff frequency ($f_T = g_m/2\pi C_T$) and transconductance frequency product

(TFP= $g_m/I_{ds}*f_T$), gain frequency product (GFP=A_v*f_T) and gain transconductance frequency product (GTFP= $A_v*g_m/I_{ds}*f_T$) are studied by varying work function, channel length and high-k gate dielectric material for DG MOSFET.

- By comparing the above said parameters, we conclude that the device having work function 4.6 eV, channel length 40 nm and double layer structure with k=7.5 predicts better results among all others.
- One optimum device FD-S-GS-DG MOSFET is designed and simulated to study some aspect of its performance.
- The increase in strain, i.e., equivalent Ge content, enhances the performance of FD-S-GS-MOSFET in terms of electrostatic parameters as well as in analog parameters because of an increase in the carrier mobility.
- Therefore, from the results shown previously in the respective chapters we conclude that strained silicon up to some extent of Ge mole fraction shows better results in device performances.

5.2 Scope for Future Work

The research work carried out in this thesis has proved the ability of reducing short channel effects and improving the device performance in terms of Analog/RF applications by choosing appropriate device dimensions with suitable materials. It also explains the effect of strain engineering and high-k gate dielectrics on various device parameters. The same framework can now be used to improve the understanding of existing structures and develop new structures for high performance, low power and high speed applications that can be of interests for certain applicative scenarios. The results presented are expected to provide incentive for further experimental exploration. Some important directions for further research in the following areas can be:

1. The detailed AC analysis for RF applications of the optimized device FD-S-GS-MOSFET.
2. Comparing the simulated results with the experimental results.
3. Possible fabrication of the different device structures considered.

List of Publications

1. **K P Pradhan**, S K Mohapatra, P K Sahu, D K Behera, "Impact of High-k Gate Dielectric on Analog & RF Performance of Nanoscale DG-MOSFET", *Microelectronics Journal*, Elsevier (Accepted).
2. P. K. Sahu, **K. P. Pradhan**, S. K. Mohapatra, "A Study on SCEs of FD-S-SOI MOSFET in Nanoscale", *Universal Journal of Electrical and Electronic Engineering*, Vol. 2, No. 1, pp. 37-43, 2014.
3. S. K. Mohapatra, **K. P. Pradhan**, P. K. Sahu, "Some Device Design Consideration to Enhance the Performance of DG-MOSFETs", *Transactions on Electrical and Electronic Materials*, (Accepted).
4. **K P Pradhan**, P K Agarwal, S K Mohapatra, P K Sahu, "Role of High-k Materials in Nanoscale TM-DG MOSFET: A Simulation Study", *Invertis Journal of Science and Technology*, Vol. 6, No. 4, pp. 1-5, 2013.
5. P K Sahu, S K Mohapatra, **K P Pradhan**, "A study of SCEs and Analog FOMs in GS-DG-MOSFET with lateral Asymmetric Channel Doping", *Journal of Semiconductor Technology and Science*, Vol. 13, No. 6, Dec., 2013.
6. **K P Pradhan**, S K Mohapatra, P K Agarwal, P K Sahu, D K Behera, Jyotismita Mishra, "Symmetric DG-MOSFET with Gate and Channel Engineering: A 2-D Simulation Study", *Microelectronics and Solid State Electronics*, Vol. 2, pp. 1-9, Feb, 2013.
7. S. K. Mohapatra, **K. P. Pradhan**, P. K. Sahu, "Investigation of Prefabrication Models of Double Gate MOSFETs in Nanoscale for High Performance Circuit Application", *Nano Trends: A Journal of Nanotechnology and its Applications*, Vol. 13, Issue 2, pp. 40-44, Oct., 2012.
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