PHASE ESTIMATION FOR GRID SYNCHRONIZATION OF DG SYSTEM USING CORDIC ALGORITHM

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PHASE ESTIMATION FOR GRID SYNCHRONIZATION OF DG SYSTEM USING CORDIC ALGORITHM

A Thesis submitted in partial fulfillment of the requirements for the degree of

Bachelor of Technology in "Electrical Engineering"

By

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CERTIFICATE

This is to certify that the thesis entitled "**Phase Estimation for Grid Synchronization of DG system using CORDIC Algorithm**", submitted by **Mr. Smruti Ranjan Panda (Roll No: 109EE0291)**in partial fulfilment of the requirements for the award of **Bachelor of Technology** in **Electrical Engineering** during session 2012-2013 at National Institute of Technology, Rourkela. A bonafide record of research work carried out by them under my supervision and guidance.

The candidates have fulfilled all the prescribed requirements.

The Thesis which is based on candidates' own work, have not submitted elsewhere for a degree/diploma.

In my opinion, the thesis is of standard required for the award of a bachelor of technology degree in Electrical Engineering.

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Smruti Ranjan Panda

Dedicated to

My parents

ABSTRACT

The proper operation of grid connected inverter system is determined by grid voltage conditions such as phase, amplitude and frequency. In such applications, an accurate and fast detection of the phase angle, amplitude and frequency of the grid voltage is essential for reference current generation. Phase angle plays an important role in control being used to transform the feedback variables to a suitable reference frame in which the control structure is implemented. Hence grid synchronization has a significant role in the control of grid connected inverter system. However, accurate on-line tracking of phase angle of the grid voltages under distorted grid condition is critical especially; during line notching, voltage unbalance, voltage dips, frequency variations etc. This project work involves development of phase estimation technique for grid synchronization using CORDIC algorithm during unbalanced three-phase grid voltage conditions. By proposing CORDIC algorithm, we can largely reduce the computational time while it will be implemented in real time platform using FPGA or DSP. Computer simulations have been carried out using MATLAB-Simulink package for feasibility of the study.

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ABBREVIATIONS AND ACRONYMS

PLL – Phase Locked Loop

STATCOM – Static synchronous Compensators

AC – Alternating Current

DC – Direct Current

VCO – Voltage Controlled Oscillator

CORDIC – Coordinate Rotation DIgital Computer

SRF – Synchronous Reference Frame

FPGA – Field Programmable Gate Array

LPF – Low Pass Filter

LF – Loop filter

VHDL – VHSlC Hardware Description Language

VHSIC – Very High Speed Integrated Circuits

EPLL – Enhanced Phase Locked Loop

CPLL – Conventional Phase Locked Loop

NRF – Natural Reference Frame

StRF – Stationary Reference Frame

VM – Vectoring Mode

RM – Rotation Mode

IP – Intellectual Property

DSP – Digital Signal Processing

CHAPTER 1

Introduction

1.1 MOTIVATION

With the advancement technology, the requirements of modern power systems is no longer limited to just uninterrupted supply of power, but the demand for quality and consistency is more than ever. On the other hand introduction of new methods of power generation (e.g. Wind power, Photovoltaic cells and other renewable sources) in which the generation parameters (e.g. wind speed, light intensity etc.) are natural variations that can't be regulated perfectly, are putting forward new challenges like controlling frequency variations, checking amplitude distortions, eliminating harmonics etc. Hence the need for sophisticated methods that can guarantee quality in power supply is growing every day. Exact estimation of utility phase angle is critical for maintaining quality in power supply especially when the grid involves apparatuses like controlled AC-DC converters, static synchronous compensators (STATCOMs), cycloconverters, active harmonic filters etc.

The very first proposed phase estimation schemes were zero cross detectors [1], but due to the power quality phenomena present in the grids, especially in weak-grids, caused malfunctioning in zero-cross based controllers. Use of voltage controlled oscillators (VCOs) resulted in more rigid controllers such as the Phase Locked Oscillator [1] systems and the Charge-Pump PLLs [2]. However with the development of discrete devices such as microcontrollers, numbers of high performance synchronization methods have been introduced. The CORDIC algorithm method is one of such methods. Although the conventional SRF-PLL measures the phase quite accurately even under distorted condition [3], the CORDIC algorithm method provides less complications and the processing time involved in field programmable gate array (FPGA) environment is quite less [4].

1.2 NECESSITY OF ESTIMATING THE PHASE ANGLE

In order to meet standard specifications in terms of power quality and safety for grid-connected systems the phase angle and the frequency of the grid voltage are crucial pieces of information. The safe and efficient operation of Distributed Generation systems requires proper synchronization with power grids by using power electronics converters. The operational condition of grid connected inverter system is determined by grid voltage

parameters such as phase, amplitude and frequency. An accurate and fast detection of the phase angle, amplitude and frequency of the grid voltage is thus essential for determination of grid condition. Hence on-line tracking of phase angle of the grid voltages during distorted grid condition becomes critical especially; during line notching, voltage unbalance, voltage dips, frequency variations etc. That's where phase estimation schemes like Phase locked loop (PLL) comes into picture

1.3 BASIC PHASE ESTIMATION SCHEMES

The very first proposed zero cross detectors for phase estimation were not quite robust due to the power quality phenomena present in the weak grids. Another was the feed forward method presented in [3][4]. In the basic feed forward scheme the phase angle$\varphi_1(t)$ has the frequency information of the fundamental component in the original voltage signal. However, the phase error θ_{LPF} due to the low pass filter (LPF) is introduced, which can be compensated by the second stage of phase estimation, similar to the operation of first stage. The second stage of phase angle estimation is based on inverse tangent operation of the filtered voltages $u_3(t)$and $u_4(t)$ which are obtained by the multiplication of the input grid voltage $v_{sa}(t)$ with two sinusoidal signals $\sin\varphi_1(t)$and$\cos\varphi_1(t)$. It was suggested that the same cut-off frequencies and DC gains are selected in the low pass filters of both the stages.

However, it has a serious drawback, i.e., the dynamic performance and estimation accuracy is highly dependent on the selection of the low pass filters (LPFs). Higher cutoff frequency of the LPFs results in a faster dynamic response but poorer estimation accuracy. In order to improve the accuracy, lower cutoff frequency should be adopted, whereas, the dynamic response becomes sluggish. Moreover, this feed-forward estimation scheme has poor immunity to line disturbances, such as phase angle jump and frequency deviations in grid voltages. Therefore, this method can only be applied to the situations when the grid voltages are almost sinusoidal waveforms and free of abrupt disturbances. Besides, it does not provide implicit frequency information of the grid voltage. These drawbacks can be overcome by using a phase-locked loop (PLL), which keeps an output signal synchronized with a reference input signal in frequency as well as in phase and with the development of discrete devices such as microcontrollers, numbers of high performance synchronization methods using Phase Locked Loops have been introduced.

1.4 OVERVIEW OF PROPOSED WORKDONE

Rigorous literature review is carried out on the projects which include notes on Phase Locked Loops, modern phase estimation methods, CORDIC algorithm for different purposes Synchronous Reference Frame applications etc. The whole CORDIC algorithm incorporated model as well as the SRF-Phase locked Loop model is first designed in MATLAB-Simulink environment. The performance of both the methods to estimate the phase angle accurately have been compared under numerous unbalanced conditions like voltage sag, voltage swell, harmonics injection, phase angle jump, single phase fault etc. After the feasibility of the proposed model is checked, a preliminary attempt to model the CORDIC algorithm based phase estimator in VHDL environment has been made using Xilinx 10.1 and ISim simulator.

1.5 THESIS OBJECTIVES

The objectives of the undertaken project work involve

- Investigation of one of the state of the art technologies for estimation of phase angle, the CORDIC algorithm method.
- Formulation and Implementation of the CORDIC algorithm in MATLAB-Simulink environment to study the feasibility and compare its performance with normal SRF-PLL phase estimator.
- Primary attempt towards implementing this algorithm in VHDL in order to realize the proposed model in FPGA environment.

1.6 ORGANISATION OF THESIS

The thesis is organised into six chapters including the chapter of introduction. Each chapter is different from the other and is described along with the necessary theory required to comprehend it.

Chapter 2 includes the basic literature review of the research work done. Various phase estimation methods used until now have been reviewed and utilization of Phase Locked Loop scheme for estimating phase angle is studied. The fundamentals and applications of a phase locked loop at its most basic structure is understood. From the various discussed schemes Synchronous Reference Frame topology has been chosen for modelling and comparing with the proposed structure.

Chapter 3 describes the design of synchronous reference frame PLL in Simulink environment and its analysis to realise practical feasibility. The whole scheme is modelled in MATLAB-Simulink and its behaviour under balanced as well as unbalanced (voltage swell, voltage sag, harmonics injection, phase angle jump etc.) condition is observed.

Chapter 4 explains elaborately about the proposed model. The CORDIC algorithm in its most basic form is explained in detail. The conversion of complicated and time taking trigonometric calculations into faster shift additions has been observed. Apart from the theoretical analysis, practical implementation of the model is also studied. CORDIC methods are encoded in two separate blocks for two separate purposes (Vector mode for normalisation and Rotation mode for delay compensation) and the scheme is then modelled in Simulink to study its response to different unbalanced conditions (voltage sag, swell, harmonics etc.).

Chapter 5 presents the modelling of the PLL scheme in VHDL environment, so that practical FPGA implementation can be done in future for development of hardware prototype. The minute yet important details of VHDL coding and the different problems faced during software interfacing have been discussed. Finally the designed model and its primitive responses are included at the end of the chapter.

Chapter 6 concludes the work performed so far. The limitations in proceeding research towards this work are discussed. The possible scope of future in improving the current scenario is mentioned. The potential and future application of the undertaken work has also been presented.

CHAPTER 2

Phase Locked Loops

2.1 INTRODUCTION

A Phase Locked Loop is a nonlinear circuit whose basic function is to synchronize its output signal (v_o) with a reference or input signal (v_i) in frequency as well as in phase. The simplified block diagram of a PLL is shown in fig. 2.1.

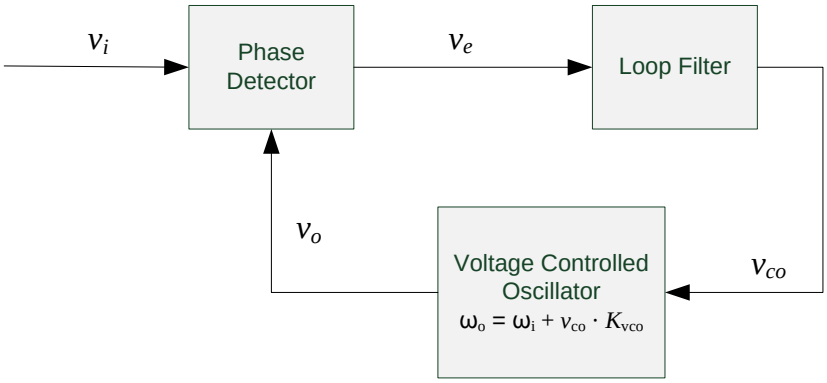


Fig. 2.1 Basic Structure of the Phase Locked Loop

The Phase Detector (PD) block, which can be as simple as a multiplier, responds to the phase angle of both the inputs and provides an output whose average value, averaged each cycle of the fundamental component of the input, is zero only when the input signals are in-phase, that is, they are synchronized both in phase ($\theta_0 = \theta_0$) and frequency ($\omega_0 = \omega_0$).The Loop Filter (LF), which is usually a low pass filter to pass the low frequency error signal, supplies a filtered control signal (V_{co}) to the Voltage Controlled Oscillator and sets the dynamics of the system. Voltage Controlled Oscillator generates a signal whose frequency depends on its input V_{co} . Thus if there is an error between the frequency of input and output signal, the phase detector detects it and provides input to VCO through the LF, VCO adjusts the frequency and locks it to the input frequency value.

As we've mentioned earlier, with the development of discrete devices numbers of high performance synchronization methods using PLLs have been introduced. Out of all those methods, some of the popular and state-of-the-art single-phase PLL topologies are

A) Power PLL
B) Enhanced PLL
C) SRF-PLL

These schemes are discusses briefly in the following subsections.

2.2 POWER PLL

The Power-PLL scheme is based on instantaneous power theory (active, reactive or both). The operation can be understood as follows

Assuming a sinusoidal input of $v_{sa} = V\cos\theta$, if the fictitious average power P is zero, then the fictitious current is would be in quadrature with the fundamental component of grid voltage v_{sa}. Hence estimated phase angle exactly tracks the actual phase angle, thus concluding the job of PLL.

If $V\cos\theta$ is the input voltage with instantaneous phase angle θ and θ' be the measured phase angle, then we've fictitious power

$$P = V\cos\theta\sin\theta'$$

$$P = \frac{V}{2}\sin(\theta' - \theta) + \frac{V}{2}\sin(\theta' + \theta)$$

Now $(\theta' - \theta)$ is nothing but the error in estimated phase, assuming small error we can consider

$$\sin(\theta' - \theta) \approx (\theta' - \theta)$$

Thus $$P = \frac{V}{2}(\theta' - \theta) + \frac{V}{2}\sin(\theta' + \theta)$$

Here $\frac{V}{2}(\theta' - \theta)$is the DC component of the fictitious power P. If this DC value (or average value) of P is filtered out and reduced to zero by the control system, then $\theta' = \theta$ thus output phase angle follows the input.

The major drawback of this method is, a DC component or a 2nd order harmonic component present in the input signal will produce a fundamental order frequency

component, which needs to be filtered out, thus the LPF needs to have lower cut off frequency, which degrades the system dynamic response.

[**NOTE**: *Dynamic response can be improved for a particular cut off frequency by increasing the order of the filter; however it involves increased complexity of the system*]

2.3 ENHANCED PLL

An Enhanced PLL (EPLL) system was introduced in Refs. [3][4]. The major improvement introduced by the EPLL is in the phase detection mechanism, which is replaced by a new strategy allowing more flexibility and provides more information such as amplitude and phase angle. The mechanism of this EPLL is based on estimating in-phase and quadrature-phase amplitudes of the desired signal, hence, has potential application in communication systems which employ quadrature modulation techniques. This scheme provided high level of noise and external disturbance rejection.

But the gain for the frequency estimation (k_i) should be very small to ensure stability. However, it would result in slow dynamic performance under frequency deviation in the grid voltage. If the frequency estimation is disabled by setting k_i to be zero, steady-state error may appear or the algorithm may even diverge under large deviations in the input. Therefore, this EPLL scheme is difficult to be practically implemented, especially for the grid-connected converters which has demanding requirements for tracking accuracy, stability and reliability of the synchronization algorithm.

2.4 SYNCHRONOUS REFERENCE FRAME PLL (SRF-PLL)

At present Synchronous Reference Frame PLL (SRF-PLL) is the one of the most employed PLL topology.

If $V_\propto$ is the single-phase voltage input, $V_\beta$is an internally generated signal that is a 90 degrees shifted version of $V_\propto$.The Park transformation block changes the reference frame, bringing the voltages system from an α-β stationary reference frame to a d-q rotating synchronous reference frame.

The feedback loop controls the angular position of this d-q reference frame. In particular the utility voltage vector is totally lined up to the d-axis. In this way it coincides with all its d-component; consequently the q-component is made equal to zero. The d-component describes the voltage vector amplitude course.

2.5 CONCLUSION

After studying the various Phase Locked Loop schemes used today in modern power system, we observe that the Synchronous Reference Frame PLL method provides a simple yet effective way to measure phase angle. In case of a single phase system we obtain the quadrature signal by delaying the available sinusoid or adopting some other similar structure, however in 3 phase system this problem is greatly reduced due to the availability of three phase shifted signals. Hence just by applying arithmetic manipulation we obtain the required orthogonal signal necessary for SRF-PLL implementation. Modelling and realisation of a three phase SRF-PLL system has been discussed in the next chapter.

CHAPTER 3

The Three Phase SRF-PLL System

3.1 INTRODUCTION

The SRF-PLL method discussed in the previous chapter has the capability of tracking the phase angle of the input sinusoid when provided with another signal in quadrature with the available one. In case of a three phase signal (with three time shifted sinusoids) this orthogonal signals are generated by simple arithmetic manipulations (discussed later in this chapter). After that the scheme follows the SRF- topology to measure the phase angle (by converting orthogonal v_α, v_β to constant valued $v_d$and v_q). This method of estimating phase of a three phase signal is elaborated, implemented (in MATLAB-Simulink environment) and analysed in this chapter.

3.2 THREE PHASE SRF-PLL

By transforming the time-varying three phase sinusoidal voltages to the synchronous reference frame using coordinate transformation, the three phase signals become dc quantities in steady state, which can significantly alleviate the difficulty in closed-loop controller design and synthesis [5]. Fig. 3.1 shows the basic SRF-PLL, proposed in [3]. The main feature of the SRF-PLL is that it estimates the phase-angle of the fundamental positive-sequence($V_{abc} = (v_a v_b v_c)$ the estimated phase-angle (θ_o) corresponds with v_a phase angle.

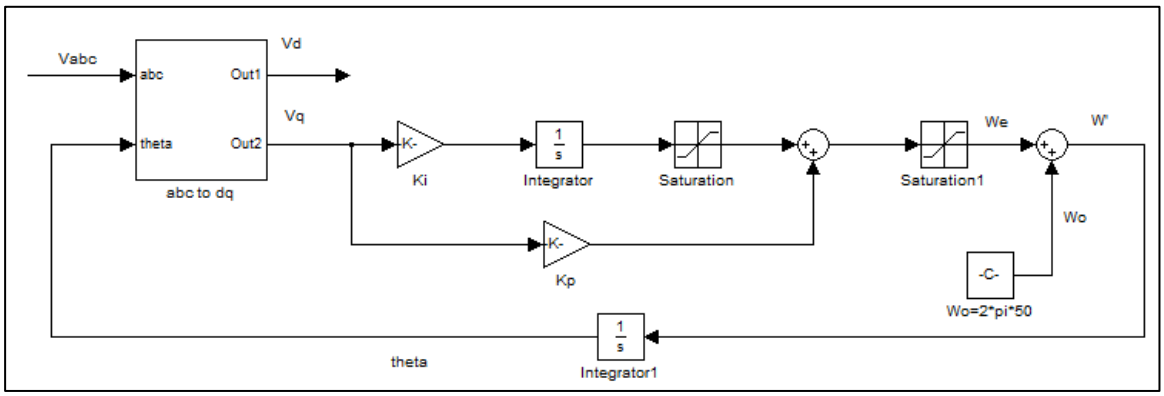


Fig. 3.1. The Matlab/Simulink diagram for the conventional three-phase PLL (CPLL)

The Park's transformation is employed as PD:

$$\begin{pmatrix} v_d \\ v_q \end{pmatrix} = \begin{pmatrix} -\sin\delta & \cos\delta \\ \cos\delta & \sin\delta \end{pmatrix} \cdot \begin{pmatrix} v_\alpha \\ v_\beta \end{pmatrix} \tag{3.1}$$

where

$$\begin{pmatrix} v_\alpha \\ v_\beta \end{pmatrix} = \frac{2}{3}\begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \cdot \begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} \tag{3.2}$$

The voltage of interest is the q-axis component and derived as

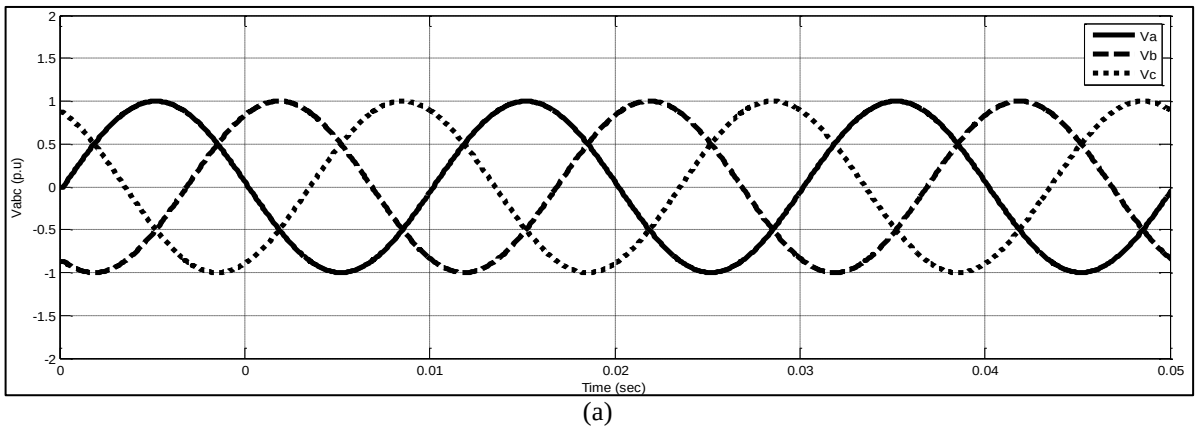
$$v_q = (v_a)_{max} \sin(\theta_i - \theta_o) = (v_a)_{max} \sin(\delta) \approx (v_a)_{max}.\delta$$

where $(v_a)_{max} = (v_b)_{max} = (v_c)_{max}$ is the peak value of three phase input, which is usually rearranged so that v_a =1 p.u. to ease the tuning. Under steady state condition v_q is expected to be zero, which represents the phase errorδ. Hence the PLL phase can track the utility phase angle by the proper design of the loop filter.

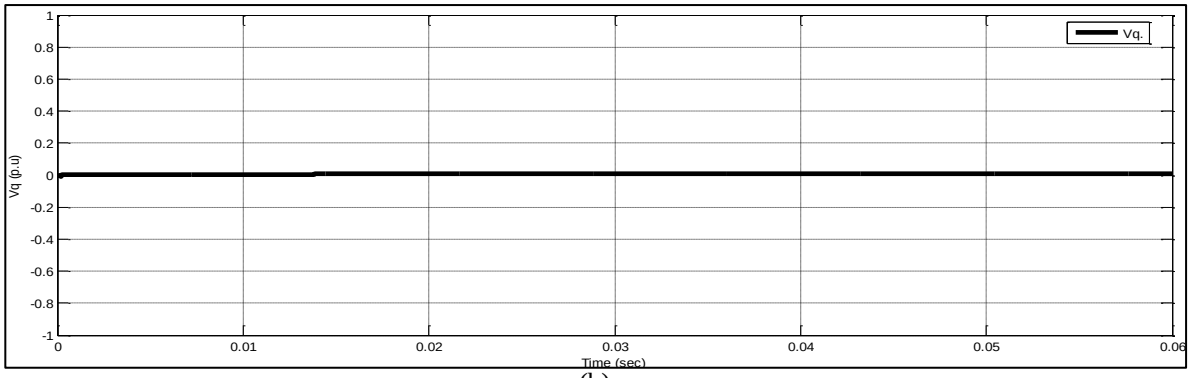
To test the Conventional three phase SRF-PLL operation under different conditions it is realized in the MATLAB/SIMULINK environment as shown in Fig.6. The abc to dq unit transforms the time varying three phase sinusoidal voltage to constant quantities by projecting them on a synchronously rotating reference frame. The CPLL has been studied at different unbalanced conditions and the simulation results are given in figures below.

3.3 SIMULATTION RESULTS

Fig. 3.2 shows the 3 phase grid voltage, the quadrature component of SRF projected voltage and the estimated phase when the grid is under balanced condition.



(a)



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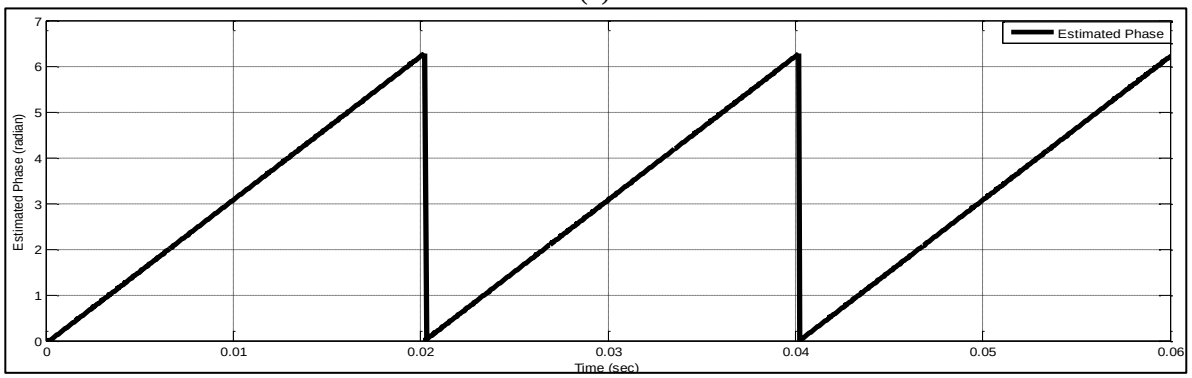
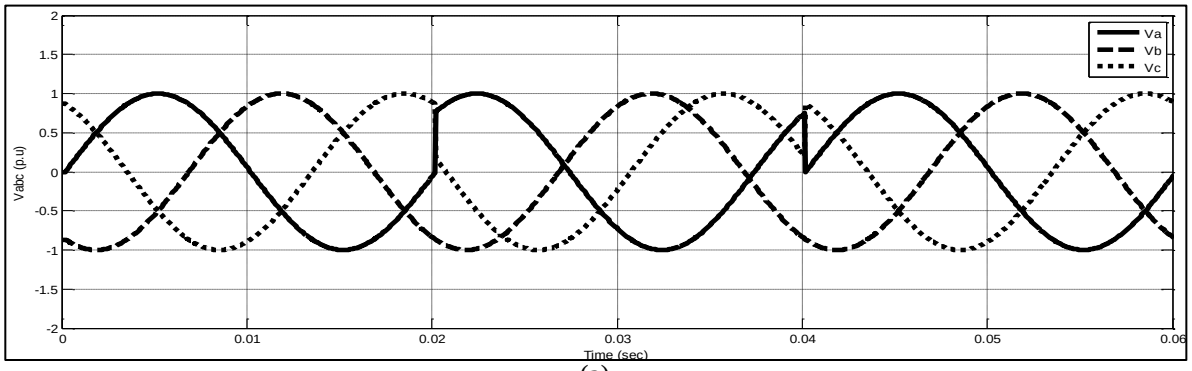


(c)

Fig. 3.2 (a) Balanced and Undistorted 3 phase grid (b) V_q in Balanced grid condition (c) Estimated Phase at balanced grid condition

Fig. 3.3 shows the grid voltages, V_q and estimated phase angle under 50º phase jump.



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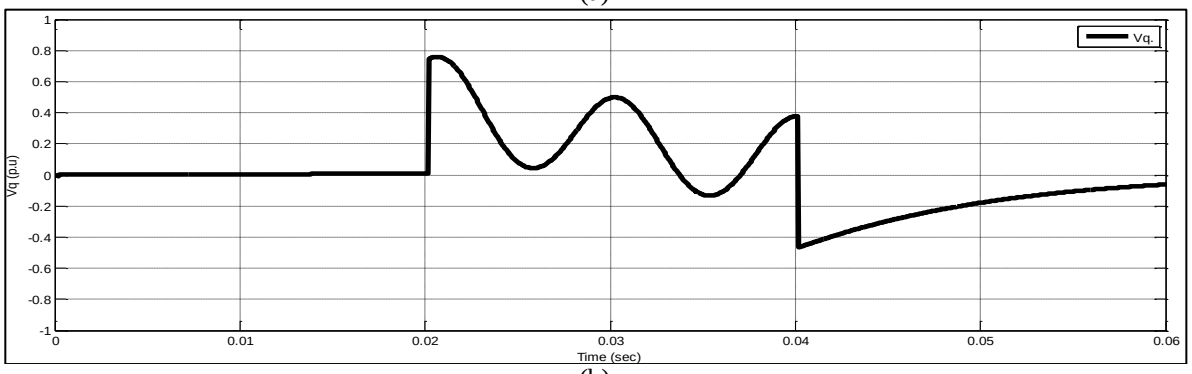

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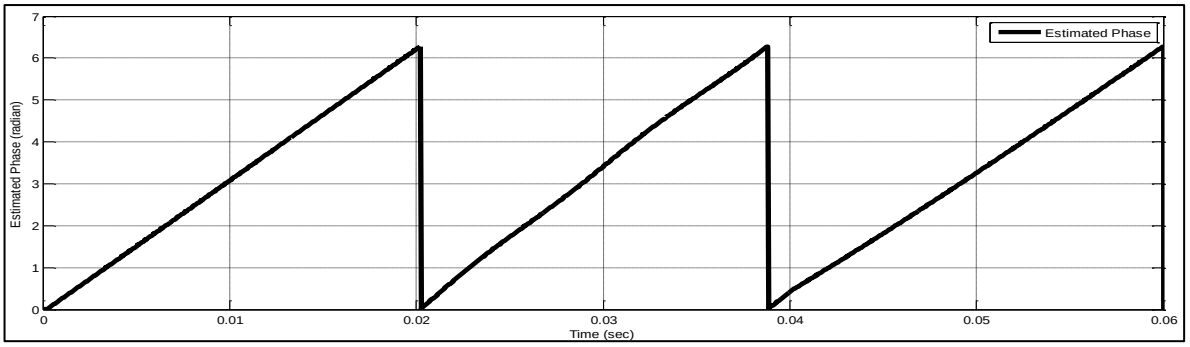
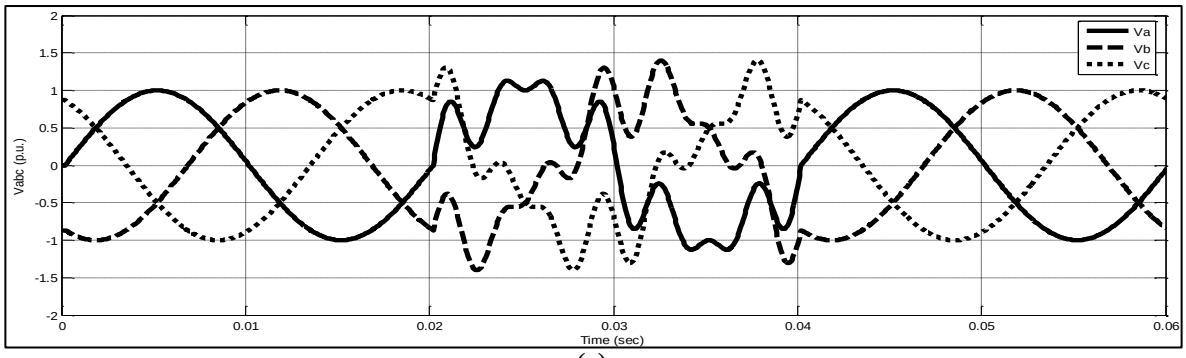


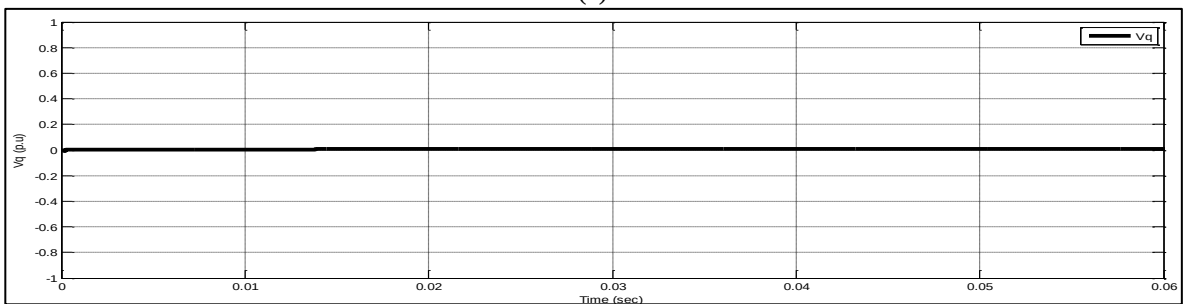
(c)

Fig. 3.3 (a) 3 Phase grid voltages with 50º phase jump (b) V_q during 50º phase jump (c) Estimated Phase during 50º phase jump

Fig. 3.4 shows the different CPLL parameters when 0.3 p.u. of 5th and 6th harmonics are injected into the grid.



(a)



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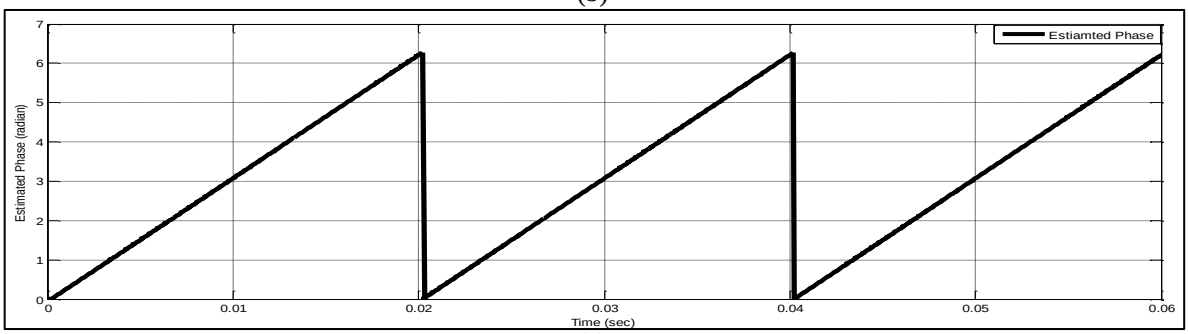
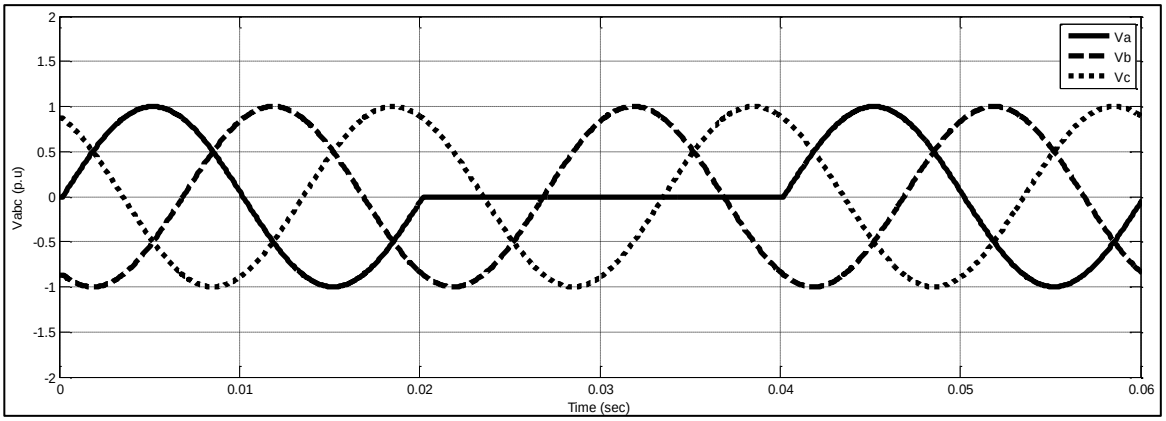


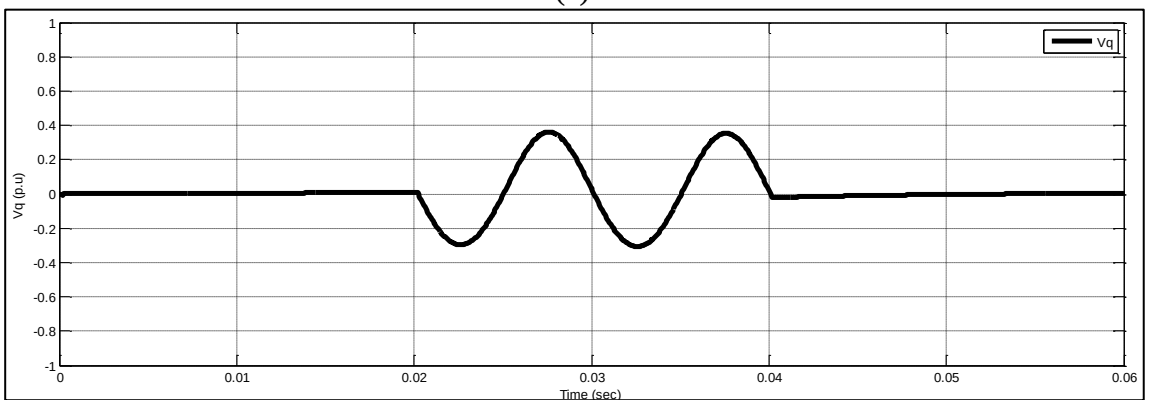
(c)

Fig. 3.4(a) 3 Phase grid voltages with harmonic injection (b) V_q with harmonic injection (c) Estimated Phase with harmonic injection

Fig. 3.5 shows the grid voltages, V_q and estimated phase angle during single phase fault condition.



(a)



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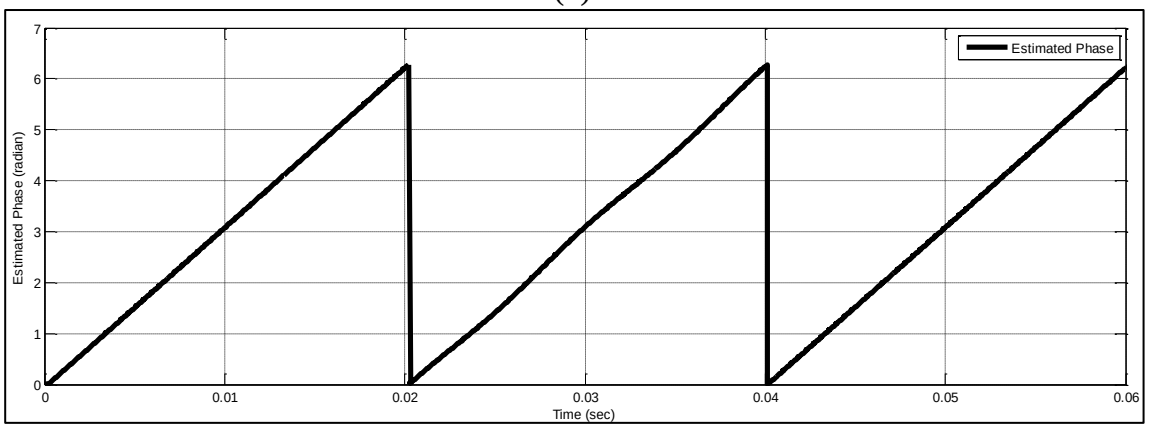


(c)

Fig.3.5(a) 3 Phase grid voltages with phase fault (b) V_q during phase fault (c) Estimated Phase during phase fault

3.4 CONCLUSION

The practical aspects and feasibility of designing a three phase PLL utilizing SRF topology has been discussed in this chapter. After modelling in Simulink, its behaviour is observed under different practical environments (ideal as well as unbalanced). However the block by block analysis reveals that the $\alpha\beta - dq$block is going to be complex and sluggish while realizing it practically due to the multiple trigonometric calculations involved. The delay brings in a danger of losing the capability of tracking phase angle in real time systems. Hence the need of a fast phase estimating algorithm that makes use of minimum number of trigonometric manipulations becomes conspicuous now. This is when CORDIC method comes into picture. CORDIC algorithm ideally converts all the trigonometric calculations into shift additions (which are much faster) thus improving the time complexity manifold. The details of which are explained in the further chapters.

CHAPTER 4

CORDIC Algorithm Method

4.1 INTRODUCTION

The coordinate rotation digital computer (CORDIC) technique is an effective algorithm which is capable of iteratively evaluating trigonometric, exponential or logarithmic functions (among others) as well as to make vector rotations, by means of a shift-adder structure, which assure an optimum use of the computation resources while obtaining better performance than the multiplication and accumulation (MAC) arithmetic unit [6],[7].

4.2 THE BASIC StRF SYSTEM

Another successful grid synchronization technique is the Stationary Reference Frame (StRF) filtering method which is based on the projection of the grid voltages from the Natural Reference Frame (NRF) to the stationary reference frame (StRF). This projection is carried out by means of the matrix transformation described in (2), where the undistorted and unbalanced electric grid voltages are described by (1), thus obtaining the α, β and γ components of the StRF voltage.

4.3 EQUATIONS

$$v_{abc} = \begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} = V \begin{pmatrix} \cos(\theta_i) \\ \cos\left(\theta_i - \frac{2\pi}{3}\right) \\ \cos\left(\theta_i + \frac{2\pi}{3}\right) \end{pmatrix} \tag{4.1}$$

$$T_{abc} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix} \tag{4.2}$$

$$v_{\alpha\beta\gamma} = \begin{pmatrix} v_\alpha \\ v_\beta \\ v_\gamma \end{pmatrix} = T_{abc/\alpha\beta\gamma} . v_{abc} \tag{4.3}$$

Once v_α and v_β is known, the phase angle θ_i can be easily estimated as

$$\theta_i = \tan^{-1}\left(\frac{v_\beta}{v_\alpha}\right) \quad (4.4)$$

However it should be noted that (4.4) is only true if v_α and v_β are sinusoidal and orthogonal, i.e. they are not contaminated by harmonics different from fundamental and are 90º phase apart from each other. This is not usually the case in practice due to the unbalanced and distorted grid; hence phase estimation becomes far from accurate.

Nevertheless this problem of inaccurate phase estimation of unbalanced grids can be solved by adding filtering and normalization stages to the StRF phase estimator scheme.

4.4 THE CORDIC ALGORITHM IMPLEMENTED SYSTEM

The CORDIC arithmetic unit is based on the use of conditional additions or subtractions along with the shift operation in such a way that it can be controlled to solve either (4.5), (4.6) or (4.7).

$$X_o = K(X_i \cos\delta - Y_i \sin\delta)$$

$$Y_o = K(X_i \sin\delta - Y_i \cos\delta) \quad (4.5)$$

$$R = K\sqrt{X_i^2 + Y_i^2} \quad (4.6)$$

$$\theta = \tan^{-1}\left(\frac{Y_i}{X_i}\right) \quad (4.7)$$

Now the CORDIC arithmetic unit can be operated either in the rotation mode (RM CORDIC) or in the vectoring mode (VM CORDIC) depending of the desired operation to be solved. The CORDIC algorithm can rotate a given vector $P_i = (I_1 I_2)$ through an angle *ai*, when operated in the rotation mode. The objective of this mode of operation is to diminish the resulting angle in each iteration by applying the pseudo-rotation method described in [4]. The RM CORDIC algorithm [4] is given by

$$d_i = sign[a_o(i)]$$

$$X'_o(i+1) = X'_o(i) - d_i 2^{-i} Y'_o(i)$$

$$Y'_o(i+1) = Y'_o(i) + d_i 2^{-i} X'_o(i) \quad (4.8)$$

$$a_o(i+1) = a_o(i) - d_i \sigma_i$$

$$X_o = K X'_o$$

$$Y_o = K Y'_o \quad (4.9)$$

Where 2^{-i} is the shift operator and a_o is the output angle. $\sigma_o$is the discrete elementary angles which is related to the number of iterations of algorithm (*i*) according to (12).

$$\sigma_i = \tan^{-1}\left(2^{-i}\right) \quad (4.10)$$

Similarly in the vectoring mode, the input vector, $P_i = (I_1 \quad I_2)$is rotated until it reaches a zero angle, by diminishing the Y'_o value in each iteration, thus obtaining the vector $P_0 = (R_o \quad 0 \quad \theta)$ at the output of the VM CORDIC arithmetic unit. The VM CORDIC algorithm [4] is given by

$$d_i = -sign[a_o(i)]$$

$$X'_o(i+1) = X'_o(i) - d_i 2^{-i} Y'_o(i)$$

$$Y'_o(i+1) = Y'_o(i) + d_i 2^{-i} X'_o(i)$$

$$a_o(i+1) = a_o(i) - d_i \sigma_i \quad (4.11)$$

The StRF phase estimator using CORDIC arithmetic unit is shown in fig. 4.1.

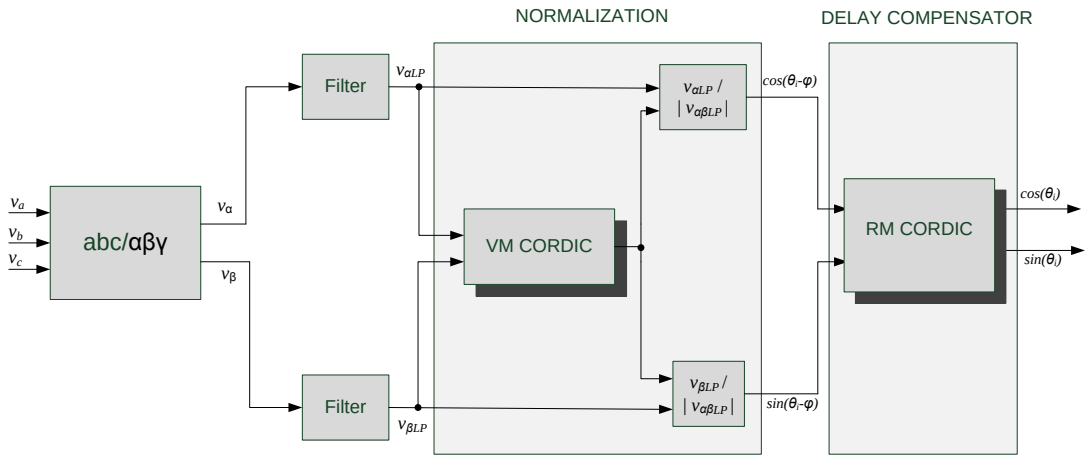
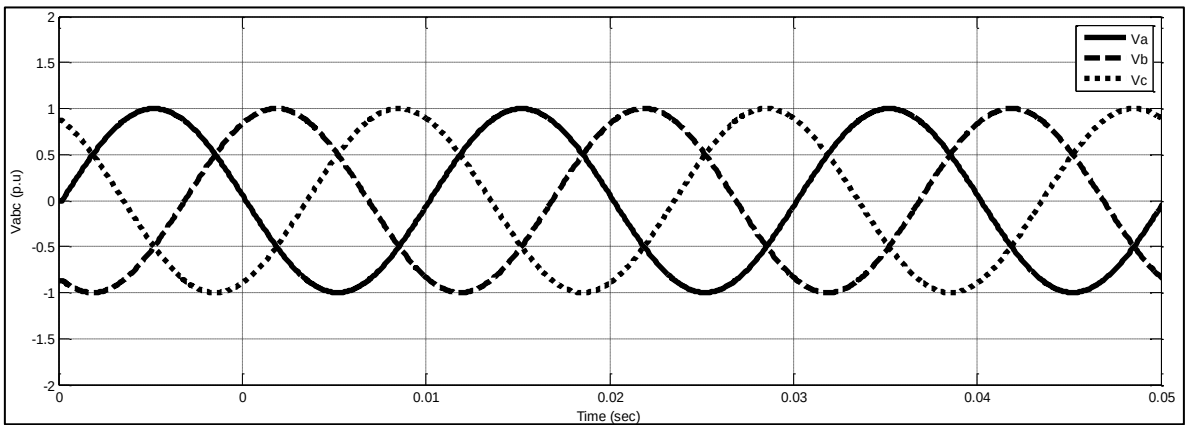


Fig. 4.1 StRF Phase estimator using VM CORDIC and RM CORDIC

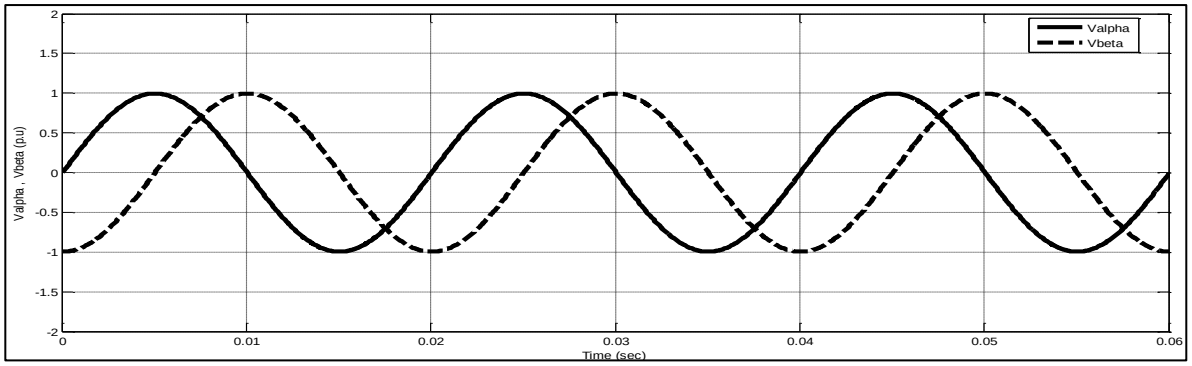
The CORDIC arithmetic unit has been tested and implemented in MATLAB/SIMULINK environment; Fig.11 shows the corresponding block diagram. The VM CORDIC unit is used for Normalization and the RM CORDIC unit acts as the phase shifter to compensate the delay introduced by the filtering units. The CORDIC StRF Phase Estimator has been studied under unbalanced conditions and the simulation results are given below.

In the following figures balanced 3 phase grid, v_α andv_β and CORDIC estimated phase angle is shown.

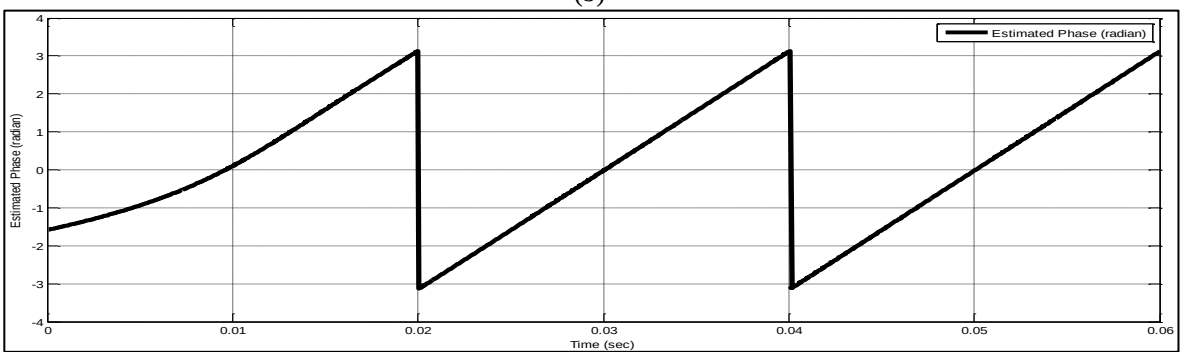
4.5 SIMULATION RESULTS



(a)



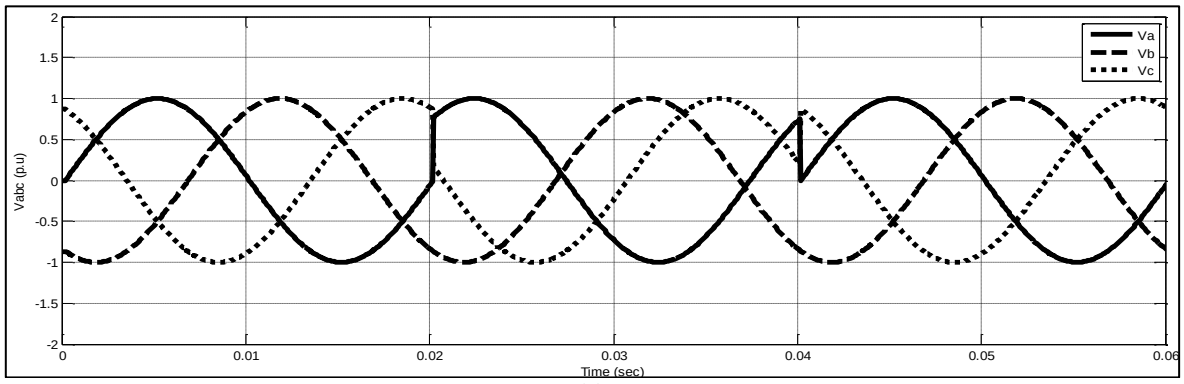
(b)



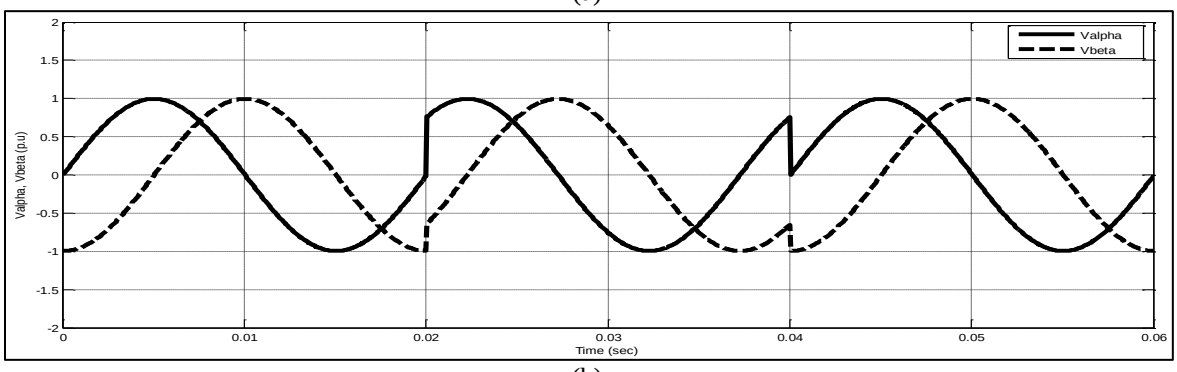
(c)

Fig. 4.2 (a) Balanced and Undistorted 3 phase grid (b)v_α and$v_\beta$under balanced grid condition (c) Estimated Phase under balanced grid condition

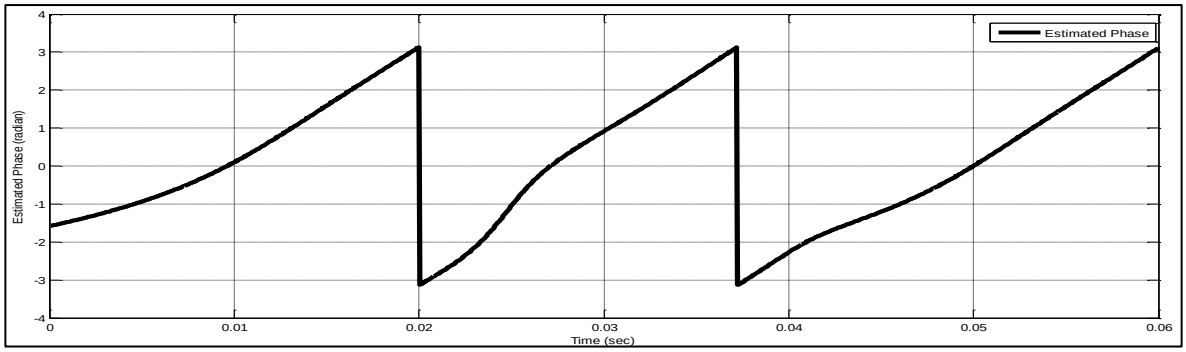
Fig. 4.3 shows the grid voltages v_α andv_β and phase angle estimated by the CORDIC based StRF-Estimator when 50º phase jump is introduced.



(a)



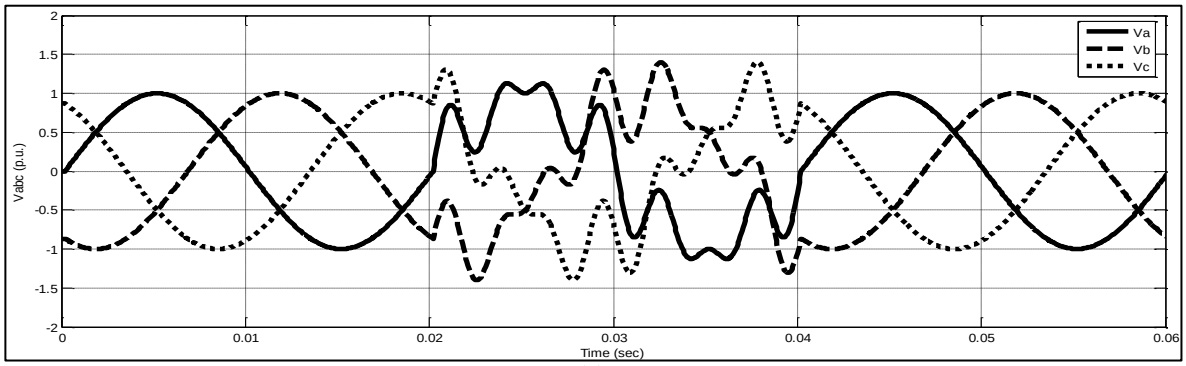
(b)



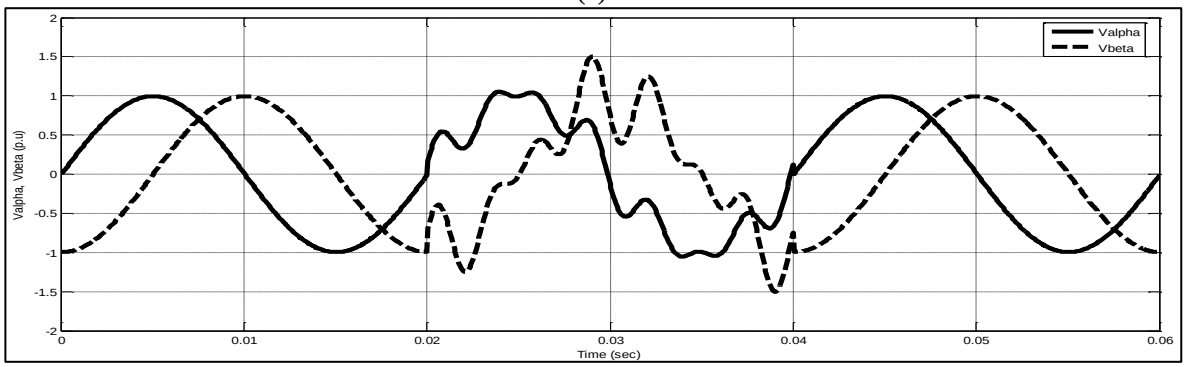
(c)

Fig. 4.3 (a) 3 Phase grid voltages with 50º phase angle jump (b)v_α and $v_\beta$under 50º phase angle jump (c) Estimated Phase under 50º phase angle jump

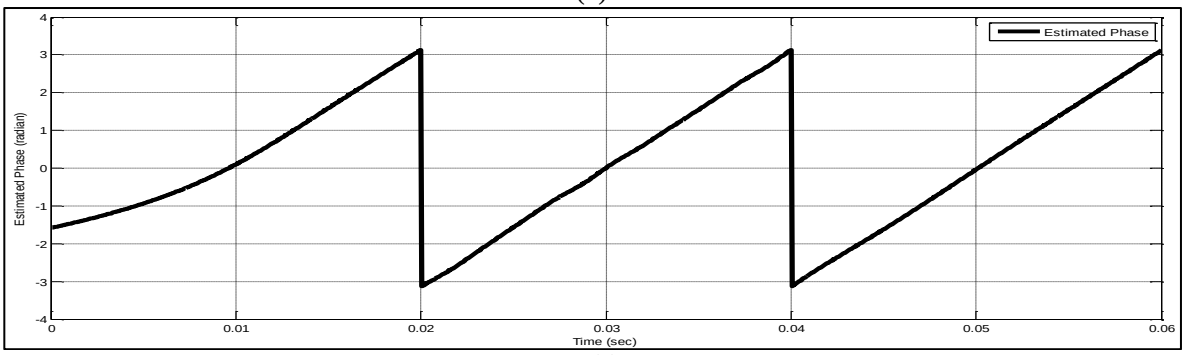
Fig. 4.4 shows the different parameters of CORDIC based StRF Phase estimator when 0.3 p.u. of 5^{th} and 6^{th} harmonics are injected into the grid.



(a)



(b)



(c)

Fig. 4.4 (a) 3 Phase grid voltages with harmonic injection (b) v_α and $v_\beta$under harmonic injection (c) Estimated Phase under harmonic injection

Fig. 4.5 shows the 3 phase grid voltage, v_α,v_β and the estimated phase when the grid is under balanced condition.

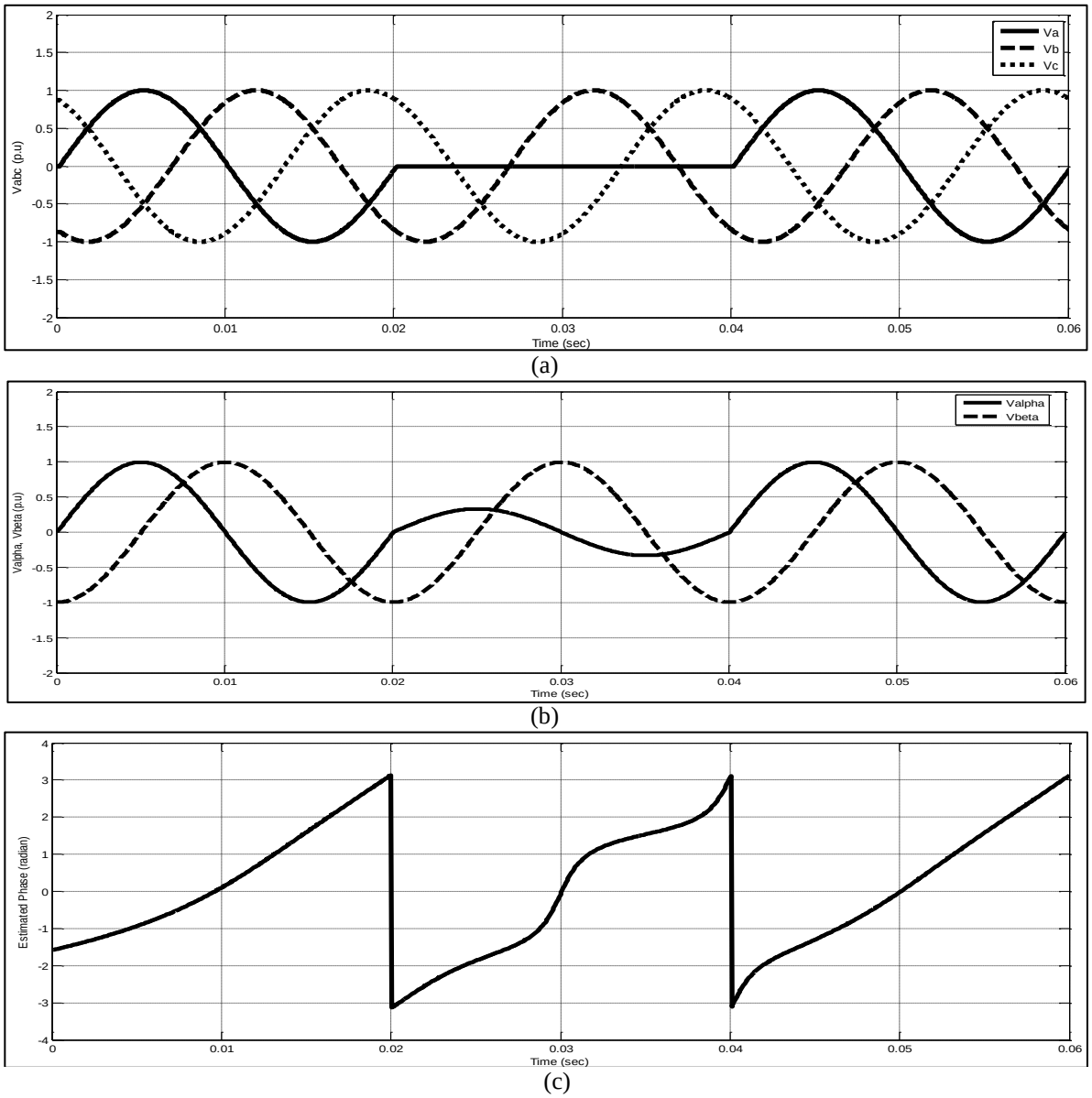


Fig. 4.5. (a) 3 Phase grid voltages with single phase fault (b) v_α and v_β under single phase fault (c) Estimated Phase under single phase fault

4.6 CONCLUSIONS

As we have discussed earlier the CORDIC based StRF phase estimator uses simple shift adders to calculate complex trigonometric and exponential functions thus reduces the computational efforts greatly. This improves speed of estimation and online tracking of phase angle is possible. As part of this project work we will try to implement this model in FPGA environment and test it during different unbalanced conditions. FPGA implementation requires VHDL coding, details of which has been described below.

CHAPTER 5

VHDL Coding and Modelling

5.1 INTRODUCTION

VHDL is an acronym for VHSlC Hardware Description Language (VHSIC is an acronym for Very High Speed Integrated Circuits). It is a hardware description language that can be used to model a digital system at many levels of abstraction ranging from the algorithmic level to the gate level. The complexity of the digital system being modeled could vary from that of a simple gate to a complete digital electronic system, or anything in between.

5.2 IP CORES IN XILINX

Intellectual Property (IP) refers to preconfigured logic functions that can be used in your design. Xilinx® provides a wide selection of IP that is optimized for Xilinx FPGAs. These can include functions delivered through the Xilinx CORE Generator™ tool, through the Xilinx Architecture Wizard, as standalone archives, from third parties, through Xilinx Platform Studio (XPS), or through System Generator. Xilinx and its partner companies produce IP ranging in complexity from simple arithmetic operators and delay elements to complex system-level building blocks, such as Digital Signal Processing (DSP) filters, multiplexers, transformers, and memory. Xilinx IP is delivered through the following tools and mechanisms.

The Xilinx LogiCORE™ IP CORDIC core implements a generalized coordinate rotational digital computer (CORDIC) algorithm.

Features

- Drop-in module for Virtex®-7 and Kintex™-7, Virtex®-6, Virtex-5, Virtex-4, Spartan®-6, Spartan-3/XA, Spartan-3A/XA/AN/3A DSP and Spartan-3E/XA FPGAs
- Functional configurations
- Vector rotation (polar to rectangular)
- Vector translation (rectangular to polar)
- Sin and Cos
- Sinh and Cosh
- Atan and Atanh
- Square root

The CORDIC core implements the following equation types:

- Rectangular to Polar Conversion (and vice-versa)
- Trigonometric
- Hyperbolic
- Square Root

Two architectural configurations are available for the CORDIC core:

- A fully parallel configuration with single-cycle data throughput at the expense of silicon area
- A word serial implementation with multiple-cycle throughput but occupying a small silicon area

A coarse rotation is performed to rotate the input sample from the full circle into the first quadrant. (The coarse rotation stage is required as the CORDIC algorithm is only valid over the first quadrant). An inverse coarse rotation stage rotates the output sample into the correct quadrant. The CORDIC algorithm introduces a scale factor to the amplitude of the result, and the CORDIC core provides the option of automatically compensating for the CORDIC scale factor.

As we discussed above about IP Cores can be used to model our system, the whole PLL system was coded and port mapped one by one Xilinx as shown below.

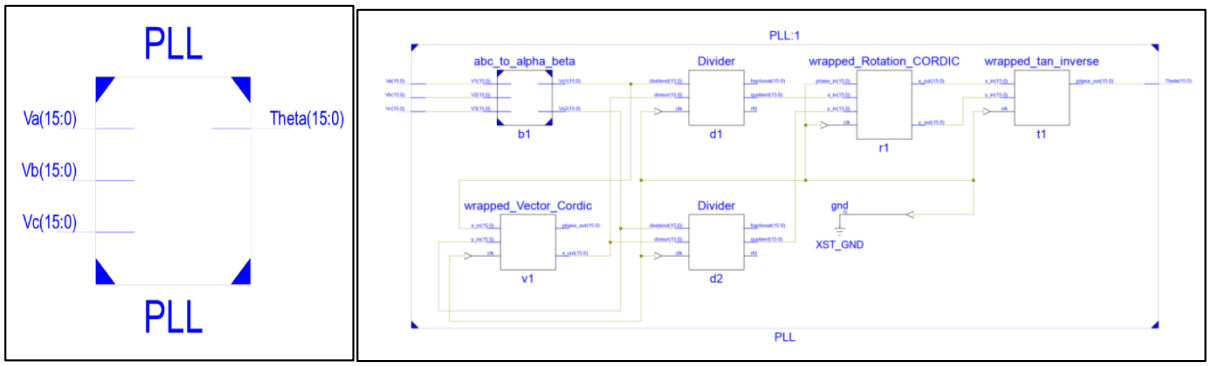
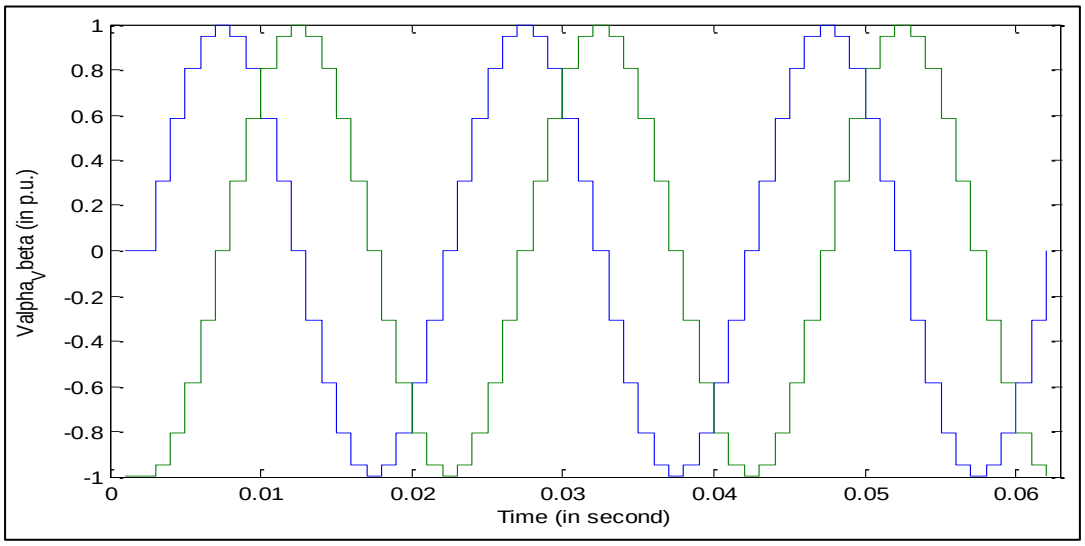


Fig. 5.1 PLL system modeled in Xilinx 14.2

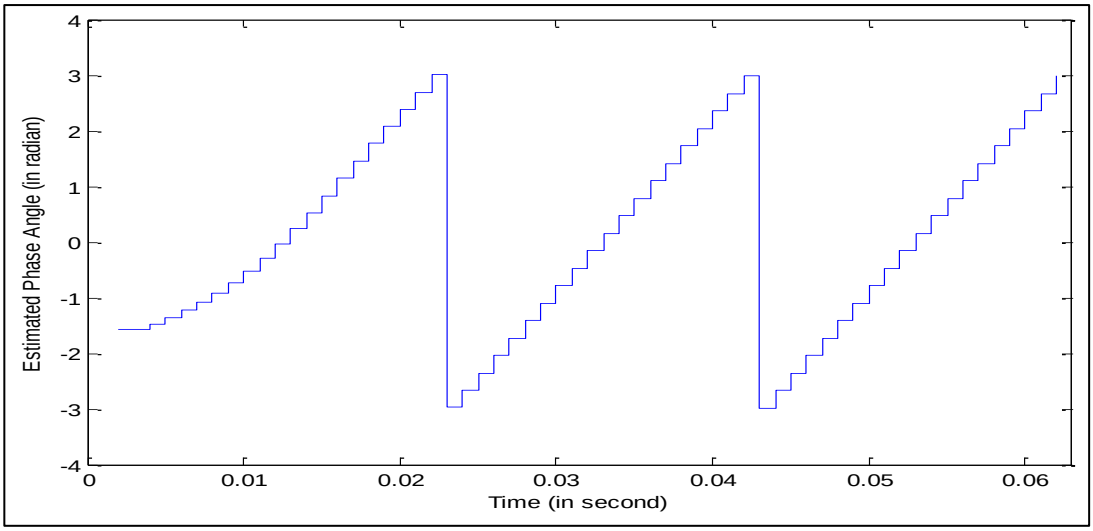
However there was one big drawback throughout the time that we have ignored, i.e. ISim simulator does not support digital to analog conversion of output data. In other words even though we get outputs from the designed model it will be in digital format and unless

converted into analog and shown in terms of figures it's meaningless for interpretation. ModelSim was first chosen to solve this problem; but due to interfacing problems ModelSim could not be incorporated into our model. Instead manual recording of digital inputs and outputs were done, and after converting those into equivalent analog values the graphs were plotted.Figure 13 shows v_α and $v_\beta$under ideal circumstances and the phase angle estimated by the CORDIC model in Xilinx.

5.3 SIMULATION RESULTS



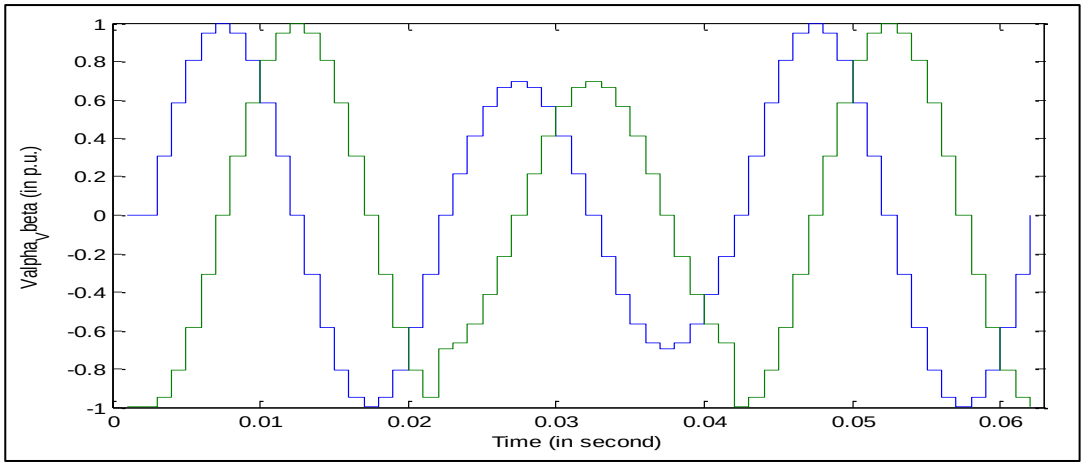
(a)



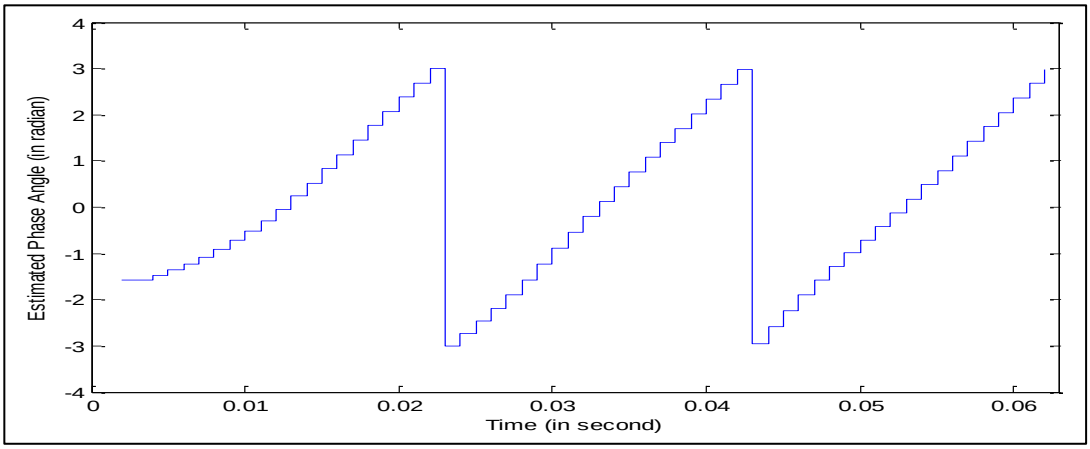
(b)

Fig. 5.2 (a) v_α and $v_\beta$under ideal condition (b) Estimated phase angle under ideal condition

Figure 5.3 shows v_α and v_β and the phase angle estimated by the CORDIC model under 0.3 p.u. voltage sag.



(a)



(b)

Fig. 5.3 (a) v_α and v_β under 0.3 p.u. voltage sag (b) Estimated phase angle under 0.3 p,.u. voltage sag

5.4 CONCLUSIONS

The CORDIC algorithm method developed first in MATLAB-Simulink environment is coded into a VHDL system. Note that the proposed structure is modeled in Xilinx with manual recording of the output data under different conditions. Interfacing this model with ModelSim(that has an digital to analog conversion algorithm already in build) can provide finer results and better resolution. VHDL modeling requires rigorous coding of blocks from simple adders and multipliers to the CORDIC block itself, thus the window for further optimization of the code is also large. FPGA implementation of the model can be done to analyze practicality of the proposed model and the code can be altered as required in future. The CORDIC block codes (both Vector and Rotation modes) have been included in the appendix for this purpose.

CHAPTER 6

Conclusion and Future work

6.1 CONCLUSION

The correct estimation of phase has become essential for quality power supply and smooth operation of the grid connected devices. However as we all know the grid voltages of any typical electrical system is rarely ideal. Line disturbances like phase jump, presence of harmonics, phase fault etc. pose a serious problem for stable grid operation. Therefore the phase estimator tools are becoming indispensable parts of modern grid connected converter applications for control purposes.

Note that the reason behind choosing FPGA was the control we get over our design. VHDL is a powerful language that allows us to design a digital system from the very fundamental levels i.e. gates and transistors. We have modeled the required components in VHDL environment and then have implemented it in the Xilinx ISim simulator. The CORDIC arithmetic unit based StRF phase estimator seems to greatly reduce the computational efforts (since it uses only additions and shift operations to carry out complex arithmetical operations). So with the introduction of CORDIC algorithm, the model is predicted to take less time for estimation of phase.

6.2 FUTURE WORK

VHDL coding of the proposed algorithm has been executed as a part of this project, FPGA implementation of this code can be made and a hardware prototype of the proposed PLL can be realised. Since the algorithm improves time response, it can be checked for reliability by ModelSim simulations (ModelSim provides in build digital to analog conversions to interpret the data in a better way. Further CORDIC compensator can be incorporated in existing PLL system for response improvement. However rigorous coding and response comparison in VHDL environment is necessary before implementing in digital processors in order to avoid unexpected hardware malfunctioning.

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APPENDIX

A. CORDIC Vector Mode (MATLAB Code):

```
function [O1,O2,ao] = srp_trial2(i1,i2)
xa=0;
ya=0;
   d=0;
i=0;
ao=0;
   s=1;
xp=abs(i1);
yp=abs(i2);
xa=xp;
ya=yp;
while((yp>0.000001)||(yp<-0.000001))
if(yp>0)
            d=-1;
end
if (yp<0)
            d=1;
end
            p=i;
            k=(2^(-p));
xa=xp-(d*k*yp);
ya=yp+(d*k*xp);
      l1=1+k^2;
      l=l1^0.5;
      s=s*l;
ao=ao-(d*atan(k));
i=i+1;
yp=ya;
xp=xa;
end
      O1=xa/s;
      O2=ya/s;
End
```

B. CORDIC Rotation Mode (MATLAB Code):

```
        function [O1,O2]=srp_trial2(i1,i2,ao)
xa=0;
ya=0;
   d=0;
i=0;
   s=1;
xp=i1;
yp=i2;
xa=xp;
ya=yp;
while((ao>0.000001)||(ao<-0.000001))
if(ao>0)
            d=1;
end
if (ao<0)
            d=-1;
end
            p=i;
            k=(2^(-p));
xa=xp-(d*k*yp);
ya=yp+(d*k*xp);
        l1=1+k^2;
        l=l1^0.5;
        s=s*l;
ao=ao-(d*atan(k));
i=i+1;
yp=ya;
xp=xa;
end
        O1=xa/s;
        O2=ya/s;
End
```

PAPERS PUBLISHED

1. **Smruti Ranjan Panda**, B.Chitti Babu, " Phase estimation for grid synchronization using CORDIC algorithm with SRF-PLL", In Proc. IEEE Students' Conference on *Electrical, Electronics and Computer Science (SCEECS), 2012* ,MANIT, Bhopal, Mar/2012.