Modeling & Simulation of High Performance Nanoscale MOSFETs

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Modeling & Simulation of High Performance Nanoscale MOSFETs

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in

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by

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Dedicated

to

My Loving Parents, Brothers, Sisters,

Brother-In-Laws, And My Sweet Nephew Soham.

Declaration

I certify that

- The work contained in this thesis is original and has been done by me under the guidance of my supervisor.
- The work has not been submitted to any other Institute for any other degree or diploma.
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Rourkela, May 2013

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C E R T I F I C A T E

This is to certify that the thesis entitled ***"Modeling & Simulation of High Performance Nanoscale MOSFETs"*** *by* ***Mr. Pramod Kumar Agarwal****, submitted to the National Institute of Technology, Rourkela (Deemed University) for the award of Master of Technology in* ***Electrical Engineering*** *with the specialization of* ***"Electronic Systems and Communication"****, is a record of bonafide research work carried out by him in the* ***Department of Electrical Engineering****, under my supervision. I believe that this thesis fulfills part of the requirements for the award of degree of Master of Technology. The results embodied in the thesis have not been submitted for the award of any other degree elsewhere.*

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Abstract

***S**ilicon-on-insulator (SOI) has been the forerunner of the CMOS technology in the last few decades offering superior CMOS devices with higher speed, higher density and reduced second order effects for submicron VLSI applications. A new type of transistor without junctions and no doping concentration gradients is analysed and demonstrated. These device structures address the challenge of short channel effects (SCEs) resulting with scaling of transistor dimensions and higher performance for deep submicron VLSI integration.*

Recent experimental studies have invigorated interest in partially depleted (PD) SOI devices because of their potentially superior scalability relative to bulk silicon CMOS devices. SELBOX structure offer an alternative way of suppressing kink effect and self heating effects in PD-SOI devices with a proper selection of oxide gap length. Also in order to mitigate the difficulties in fabrication of ultra thin devices for the semiconductor industry, resulting from scaling of gate length in MOSFET, a new device structure called junctionless (JL) transistors have recently been reported as an alternative device.

In conclusion, extensive numerical simulation studies were used to explore and compare the electrical characteristics of SELBOX SOI MOSFET with a conventional single-material gate (SMG) bulk MOSFET. The proposed work investigates the DC and AC characteristics of the junctionless transistors. Also the performance analysis of JL transistors is compared and presented with the conventional DG MOSFET structure. The results presented in this work are expected to provide incentive for further experimental exploration.

Contents

List of Abbreviations

Abbreviation	Description
ITRS	International Technology Roadmap for Semiconductors
CMOS	Complementary Metal-Oxide Semiconductor
FET	Field Effect Transistor
GaAs	Gallium Arsenide
SOI	Silicon-On- Insulator
SS	Subthreshold Slope
PD-SOI	Partially-Depleted Silicon-On- Insulator
FD-SOI	Fully-Depleted Silicon-On- Insulator
EOT	Effective Oxide Thickness
DT	Direct Tunneling
GIDL	Gate Induced Drain Lowering
DIBL	Drain Induced Barrier Lowering
BTBT	Band-to-Band Tuneling Current
DG-MOSFET	Double-Gate Metal-Oxide Field Effect Transistor
DG-JL MOSFET	Double-Gate Junctionless Metal-Oxide Field Effect Transistor
SCEs	Short Channel Effects
FBEs	Floating Body Effects
SELBOX	Selective Buried Oxide

List of Symbols

Symbols	Description
V_{dd} or V_{DD}	Power Supply Voltage
V_{th} or V_T	Threshold Voltage
I_{ds} or I_D	Drain Current
SiO_2	Silicon dioxide
t_{ox} or T_{ox}	Gate-Oxide Thickness
t_b	Buried-Oxide Thickness
L_g or L	Channel Length
W	Channel Width
N_A	Acceptor Doping Concentration
N_D	Donor Doping Concentration
t_{Si} or T_{Si}	Silicon-body Thickness
G_m	Transconductance
t_b	Buried-Oxide Thickness
ε_{si}	permittivity of Silicon
N_{sub}	Substrate Doping
I_{on}	On-State drive Current
I_{off}	Off-State Leakage Current
v_{sat}	Carriers Velocity Saturation
C_G	gate Capacitance
C_{dep}	Depletion Capacitance
C_{ox}	Oxide Capacitance
k_B	Boltzman Constant

List of Useful Constants with their Values

Constants	Values
Electronic Charge(q)	1.6×10^{-19} Coulomb
Electron mass(m)	$9.1 \times 10^{-31} Kg$
Permeability of Vaccum(μ_o)	$4\Pi \times 10^{-7}$H/m
Permittivity of Vaccum(ε_o)	$10^{-9}/36\Pi$=8.85×10^{-12}F/m
Boltzman Constant(k_B)	1.38×10^{-23}J/K
Permittivity of Silicon(ε_{si})	11.68$\simeq$12
Permittivity of SiO_2(ε_{SiO_2})	3.9
Permittivity of HfO_2(ε_{HfO_2})	$20 \sim 24$
Room Temperature(T)	300K
Thermal Voltage($V_T = k_BT/q$)	0.0259V$\simeq$26mV

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Chapter 1

INTRODUCTION

1.1 Background

The central component of semiconductor electronics is the integrated circuit (IC), which combines the basic elements of electronic circuits - such as transistors, diodes, capacitors, resistors and inductors - on one semiconductor substrate. The two most important elements of silicon electronics are transistors and memory devices. For logic applications MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) are used. MOSFETs have been the major device for ICs over the past two decades. With technology advancement and the high scalability of the device structure, silicon MOSFET-based VLSI circuits have continually delivered performance gain and/or cost reduction to semiconductor chips for data processing and memory functions.

The semiconductor industry has showcased a spectacular exponential growth in the number of transistors per integrated circuit for several decades, as predicted by Moore's law. The relentless evolution of electronics, information technology(IT), and communications has been mainly enabled by continuous progress in silicon-based CMOS technology. This continuous progress has been achieved particularly by its dimensional scaling. CMOS scaling has been the main driving force of Si technology advancement to improve both device density and performance. The reduction in cost-per-function has been steadily increasing the economic productivity with every new technol-

ogy generation. Besides scalability, the other unique device properties such as input resistance, self isolation, zero static power dissipation, simple layout and process steps have made CMOS transistors as the main components of the current integrated circuits(ICs). Today CMOS ICs are found everywhere and indespensible in our daily life, ranging from portable electronics to telecommunications and transportation.

A lot of research has gone into device design over the last thirty years, but the evolution of process technologies brings new obstacles as well as new opportunities to device designers. The future technology trend predicted by ITRS (International Technology Roadmap for Semiconductors), physical dimensions and electrostatic limitations faced by conventional process and fabrication technologies will require the dimensional scaling of complementary metal-oxide-semiconductor (CMOS) devices within the next decade. However, as the device scaling continues for the 21st century, it turns out that the historical growth, doubled circuit density and increased performance by about 40% every technology generation, followed by Moore's Law cannot be maintained only by the conventional scaling theory.

As the CMOS technology scaling enters the nanometer regime, many serious problems called the small geometry effects or short channel effects(SCEs) comes into play. Some of these effects are such as increased laekage currents, diffulty on increase of on-current, large parameter variations, low reliability and yield, increase in manufacturing cost, and etc. In order to sustain the historical improvements, future technology scaling and to mitigate these small geometry effects to a considerable level, several strategies and new device structures have been researched and introduced. A few examples of those are; increasing electrostatic control over the channel by means of the continuous EOT scaling with high-k/metal gate stack, Multi-gate MOSFET structures, silicon-on-insulator(SOI), Strained Silicon (S-Si), Si nanowire/carbon nanotube FETs, etc. Many of these devices have been shown to have favorable device properties and new device characteristics, and require new fabrication

techniques. These nanoscale devices have a significant potential to revolutionize the fabrication and integration of electronic systems and scale beyond the perceived scaling limitations of traditional CMOS.

1.2 Future Technology Node Requirements

The factors or features to be distinguished between several logic technology options are:

a) High performance (HP):

The high performance corresponds to high complexity ICs that require high clock frequencies and at the same time can deal with high power consumption. The increase in clock frequency from one technology node to the next can be achieved at the device level by an improvement of the intrinsic switching time of a transistor of 17% per year, while maintaining the transistor off-state current to a value acceptable from a power consumption point of view. The intrinsic switching time (τ) is the time needed by a transistor supplying on-state current to make the gate of an identical transistor switching from ground to the supply voltage.

$$I = \frac{Q}{t} = \frac{CV}{\tau}$$

$$\tau = \frac{Q}{I} = \frac{CV}{I} \tag{1.1}$$

where,

$C \rightarrow$ Gate capacitance $V \rightarrow$ Supply voltage $I \rightarrow$ On-state current of the device

Therefore, the most efficient way to achieve enhanced performance is to scale the gate length of the transistor aggressively. Consequently, this will result in reduced gate capacitance while increasing the on-state current.

b) Low operating power (LOP):

The low operating power technology option mainly aims at relatively high

performance mobile applications such as notebook computers. The key challenge is to increase the circuit performance while decreasing the dynamic power consumption as much as possible when the device is operating. The dynamic power consumption at the device level is a measure of power-delay product given by

$$P\tau = \frac{CV}{I}P = \frac{CV}{I}VI$$

$$P\tau = CV^2$$

$$P\tau \propto V^2 \tag{1.2}$$

Therefore, the most efficient way to reduce the dynamic power consumption is thus to reduce the supply voltage as far as possible i.e. $V \Downarrow \Rightarrow P\tau \Downarrow \Rightarrow$ Dynamic Power Consumption (given by $0.5CV^2f$) decreases.

c) Low stand-by power dissipation (LSTPD):

The low stand-by power option is used for lower performance, low-cost consumer applications such as cellular phones. For such applications, the main concern or key issue is to continue increasing circuit performance while maintaining the power consumption as low as possible when the IC is idle. This static power consumption at the transistor level is governed by the leakage current of the devices. Therefore, low stand-by power technology option requires very low transistor-off state currents as well as very low parasitic currents such as gate leakage.

1.3 Technology Scaling

The lateral geometric dimensions of devices and interconnects are reduced. This reduction in size is referred to as "scaling" of the geometric dimensions of the integrated circuits(IC). The minimum feature size is smaller size of object (e.g. gate length or interconnect linewidth) on IC. Over the past

decades, the MOSFET has continually been scaled down in size; typical MOSFET channel lengths were once several micrometres, but modern integrated circuits are incorporating MOSFETs with channel lengths of tens of nanometers. As a consequence of this minimum feature size of ICs, the number of transistors have increased over time. The semiconductor industry maintains a "roadmap", the ITRS, which sets the pace for MOSFET development. Historically, the difficulties with decreasing the size of the MOSFET have been associated with the semiconductor device fabrication process, the need to use very low voltages, and with poorer electrical performance necessitating circuit redesign and innovation (small MOSFETs exhibit higher leakage currents, lower output resistance, lower transconductance, interconnect capacitance, process variations, etc.

1.3.1 Why MOSFET Scaling ?

Smaller size of MOSFETs is highly desirable for several reasons. The primary reason to make transistors smaller in size is to integrate more and more number of devices in a given chip area. This results in a chip with the same functionality in a smaller area, or chips with more functionality in the same area. Since fabrication costs for a semiconductor wafer are relatively fixed, the cost per integrated circuits is mainly related to the number of chips that can be produced per wafer. Hence, smaller ICs allow more chips per wafer, reducing the price per chip. In fact, over the past 30 years the number of transistors per chip has been doubled every 23 years once a new technology node is introduced. For example the number of MOSFETs in a microprocessor fabricated in a 45 nm technology can well be twice as many as in a 65 nm chip. This doubling of transistor density was first observed by Gordon Moore in 1965 and is commonly referred to as Moore's law.

It is also expected that smaller transistors switch faster. For example, one approach to size reduction is a scaling of the MOSFET that requires all device dimensions to reduce proportionally. The main device dimensions are the channel length, channel width, and oxide thickness. When they are scaled

down by equal factors, the transistor channel resistance does not change, while gate capacitance is cut by that factor. Hence, the RC delay of the transistor scales with a similar factor. However, this has been traditionally the case for the older technologies, for the state-of-the-art MOSFETs reduction of the transistor dimensions does not necessarily translate to higher chip speed because the delay due to interconnections is more significant.

1.3.2 Moore's Law

In the last forty-five years since 1965, the price of one bit of semiconductor memory has been dropped 100 million times. The primary engine that powered the proliferation of electronics is "miniaturization". By making the transistors and interconnects smaller, more circuits can be fabricated on each silicon wafer and therefore each circuit becomes smaller. Miniaturization has also been responsible to the improvements in speed and power consumption in ICs.

Gordon Moore made an empirical observation in 1965 that the number of devices on a chip doubles every 18 or 24 months or so as shown in Figure 1.1 [3].

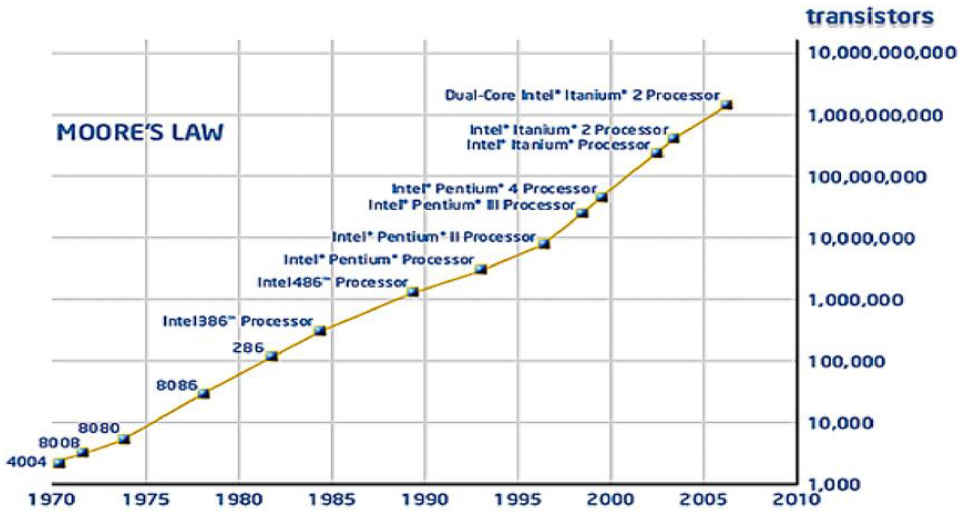

Figure 1.1: Moore's Law

This Moore's law is a succint description of the rapid and persistent trend

of miniaturization. Each time the minimum line width is reduced , we say that a new technology generation or technology node is introduced. Examples of technology generations is shown in Table 1.1 :

Table 1.1: Improvements in Technology Node over the years

Year	2004	2006	2008	2010	2011	2013	2016	2022
$Technology\ Node:$	$90nm$	$65nm$	$45nm$	$32nm$	$22nm$	$16nm$	$14nm$	$10nm$

The numbers shown in the table refers to the minimum metal line width. Poly-Si lengths may be even smaller. At each new node, all the features in the circuit layout, such as the contact holes, are reduced in size to 70% of the previous node. Historically, a new technology node is introduced every two to three years. The main reward for introducing a new technology node is the reduction of circuit size by half. (70% of previous line width means 50% reduction in area i.e., 0.7*0.7=0.49). Since nearly twice as many circuits can be fabricated on each wafer with each new technology node, the cost per circuit is reduced significantly which drives down the cost of ICs.

It is intuitive that Moore's Law cannot be sustained forever. However, predictions of size reduction limits due to material or design constraints, or even the pace of size reduction, have proven to elude the most insightful scientists. The predicted 'limit' has been dropping at nearly the same rate as the size of the transistors. Further technology scaling requires major changes in many areas, including: 1) improved lithography techniques and non-optical exposure technologies; 2) improved transistor design to achieve higher performance with smaller dimensions; 3) migration from current bulk CMOS devices to novel materials and structures, including silicon-on-insulator, strained Si and novel dielectric materials; 4) circuit sensitivity to soft errors from radiation; 5) smaller wiring for on-chip interconnection of the circuits; 6) stable circuits; 7) more productive design automation tools; 8) denser memory cells, and 9) manageable capital costs. Metal gate and high-k gate dielectrics were introduced into production in 2007 to maintain technology scaling trends.

In addition, packaging technology needs to progress at a rate consistent with on-going CMOS technology scaling at sustainable cost/performance levels. This requires advances in I/O density, bandwidth, power distribution, and heat extraction. System architecture will also be required to maximize the performance gains achieved in advanced CMOS and packaging technologies.

1.3.3 CMOS Scaling Trends

For many years now, the shrinking of MOSFETs has been governed by the ideas of scaling. The basic idea is illustrated in the Figure 1.2 [4]: a large FET is scaled down by factor α to produce a smaller FET with similar behavior.

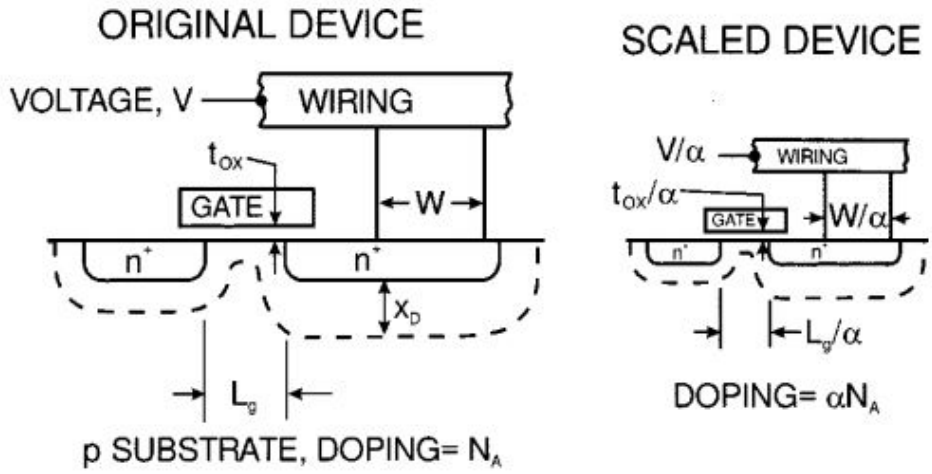

Figure 1.2: Schematic illustration of the scaling of Si technology by a factor α

Device scaling is based upon simple principles; by reducing the sizes of devices and interconnects, density, and power, the speed and performance of transistors can be improved. Device scaling mainly focusses on

a) scaling of threshold voltage with feature size

b) scaling of gate oxide thickness with feature size

c) scaling of supply voltage with feature size

With technology scaling, the MOS device channel length is reduced. When

the dimensions of a MOSFET are scaled down, both the voltage level and the gate-oxide thickness are also reduced. The supply voltage V_{dd} has to be scaled down in order to keep the power consumption under control. The transistor V_{th} also had to be scaled down to maintain a high drive current and achieve performance improvement. In a given technology node, since the source-body and drain-body depletion widths are predefined based on the doping, the rate at which the barrier height increases as a function of distance from the source into the channel is constant. Therefore, when the channel length is reduced, the barrier for the majority carriers to enter the channel is also reduced as shown in Figure 1.3 [5]. As a result threshold voltage is reduced. In short channel transistor, the barrier height and therefore the threshold voltage are a strong function of the drain voltage. Figure 1.3 [5] indicates, the barrier reduces as the drain voltage is increased.

Aggressive scaling of CMOS technology in recent years has reduced the silicon dioxide(SiO_2) gate dielectric thickness below 20Å. In 90 nm, the gate oxide consists of about 5 atomic layers equivalent to 1.2 nm in thickness. The thinner the gate oxide, the higher the transistor current and consequently the switching speed. The scaling trend of power supply voltage (V_{dd}), threshold voltage (V_{th}), and gate-oxide thickness (T_{ox}) as a function of CMOS channel length is shown in Figure 1.4 [6].

When V_{dd} is reduced towards shorter channel lengths, it becomes increasingly difficult to satisfy both the performance and the off current requirements. Trade-off between leakage current and circuit speed stems due to subthreshold nonscalability. For this reason and for compatibility with the standardized power supply voltage of earlier generation systems, the general trend is that V_{dd} has not been scaled down in proportion to L and V_{th} has not been scaled down in proportion to V_{dd} as shown in Figure 1.4 [6].

When all of the voltages and dimensions are reduced by the scaling factor α and the doping and charge densities are increased by the same factor, the electric field configurations inside the FET remains the same as it was in the

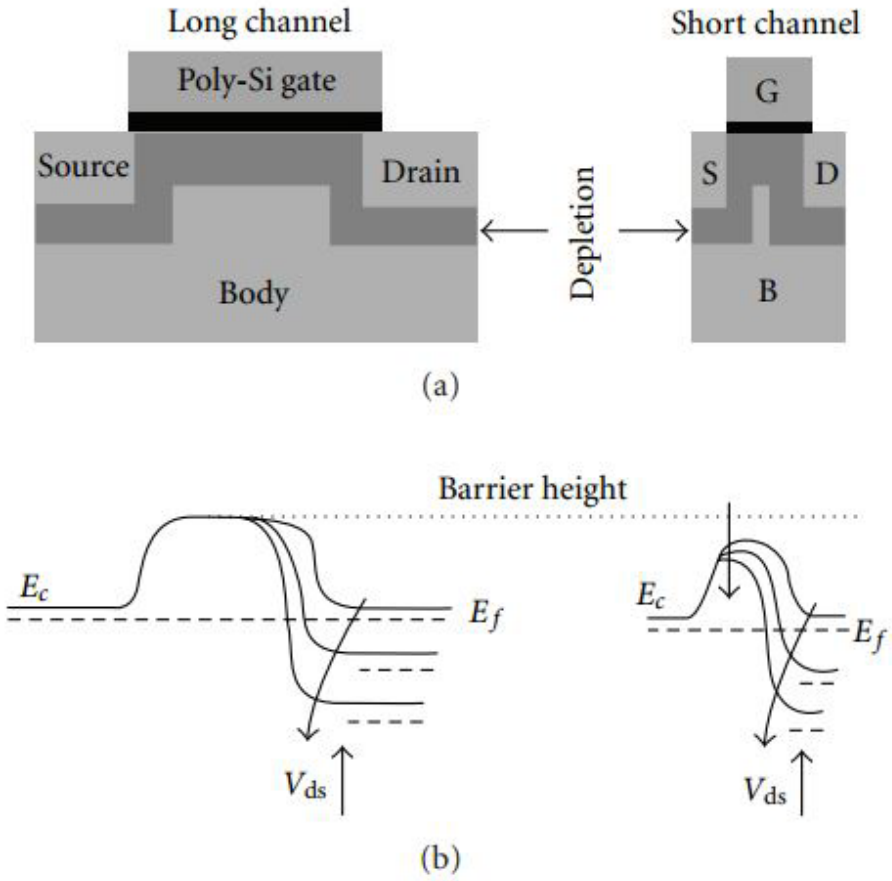

Figure 1.3: Channel length reduces the barrier for the majority of carriers to enter the channel

original device. This is called constant field scaling, which results in circuit speed increasing in proportion to the factor α and circuit density increasing as α^2. These scaling relations are shown in the second column of Table 1.2 along with the scaling behavior of some of the other important physical parameters.

α is the dimensional scaling parameter, ε is the electric field scaling parameter, and α_d and α_w are separate dimensional scaling parameters for the selective scaling case. α_d is applied to the device vertical dimensions and gate length, while α_w applies to the device width and the wiring.

1.3.4 Challenges to Miniaturization of MOSFETs

Despite formidable challenges, however, many of those in the research community and industry do envision close variants of conventional microelec-

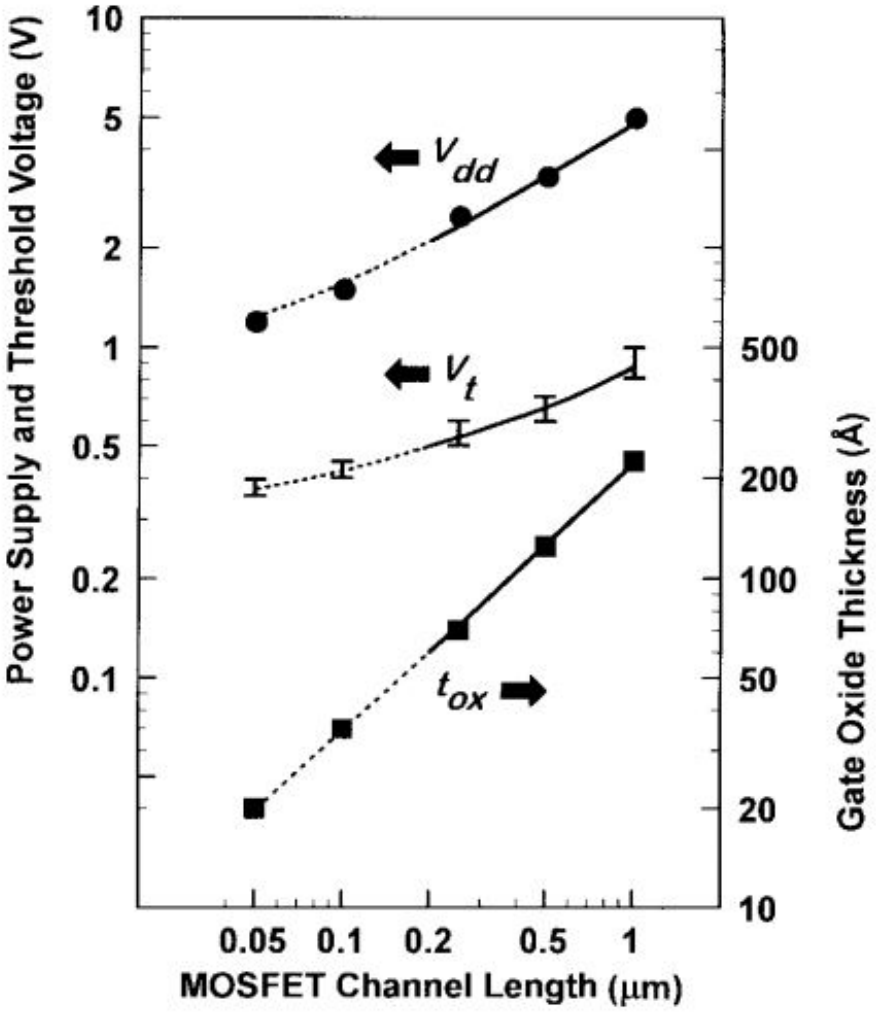

Figure 1.4: Scaling trend of power supply voltage (V_{dd}), threshold voltage (V_{th}), and gate-oxide thickness (T_{ox}) as a function of CMOS channel length

tronic transistors becoming miniaturized into the nanometer-scale regime. For example, the International Technology Roadmap for Semiconductors(ITRS), published by the Semiconductor Industry Association, projects that chips will be made from transistors with major features (gate lengths) of 70 nm in the year 2010. Individual working transistors with 40 nm gate lengths have already been demonstrated in silicon. Transistors with gate lengths as small as 25 nm have been made using Strained Silicon (S-Si). However, to provide points of reference for contrasting nanoelectronic devices with scaled-down FETs, a few of the obstacles to FET scaling are simply enumerated below,

Table 1.2: Technology Scaling Rules for Three Cases

Physical Parameter	$ConstantElectricField\ ScalingFactor$	$GeneralizedScaling\ Factor$	$GeneralizedSelective\ ScalingFactor$
$ChannelLength$, $InsulatorThickness$	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
$WiringWidth$, $ChannelWidth$	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
$ElectricFieldindevice$	1	ε	ε
$Voltage$	$1/\alpha$	ε/α	ε/α_d
$On-Currentperdevice$	$1/\alpha$	ε/α	ε/α_w
$Doping$	α	$\varepsilon\alpha$	$\varepsilon\alpha_d$
$Area$	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha_w^2$
$Capacitance$	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
$GateDelay$	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
$Powerdissipation$	$1/\alpha^2$	ε^2/α^2	$\varepsilon^2/\alpha_w\alpha_d$
$PowerDensity$	1	ε^2	$\varepsilon^2/\alpha_w\alpha_d$

in increasing order of their intractability.

a) High electric fields:

Due to a bias voltage being applied over very short distances, can cause avalanche breakdown by knocking large numbers of electrons out of the semiconductor at high energies, thus causing current surges and progressive damage to devices. This may remain a problem in nanoelectronic devices made from bulk semiconductors.

b) Heat dissipation:

Heat dissipation of transistors (and other switching devices), due to their necessarily limited thermodynamic efficiency, limits their density in circuits, since overheating can cause them to malfunction. This is likely to be a problem for any type of densely packed nanodevices.

c) Vanishing bulk properties and non-uniformity of doped semiconductors on small scales:

This can only be overcome either by not doping at all (accumulating electrons purely using gates, as has been demonstrated in a GaAs heterostructure) or by making the dopant atoms form a regular array. Molecular nano-electronics is one path to the latter option.

d) Shrinkage of depletion regions:
Shrinkage of depletion regions until they are too thin to prevent quantum mechanical tunneling of electrons from source to drain when the device supposedly is turned off. The function of nanoelectronic devices is not similarly impaired, because it depends on such tunneling of electrons through barriers.

e) Shrinkage and unevenness of the thin oxide layer beneath the gate:
This prevents electrons from leaking out of the gate to the drain. This leakage through thin spots in the oxide also involves electron tunneling.

Long ago, MOSFETs were big and could be described via drift currents and carrier control via the gate capacitance. Now MOSFETs are small in order to increase their operation speed. Pushing the dimensions of the gate length down influences the electrostatics of the devices. In order to preserve the electrostatic integrity of the MOSFET scaling has proceeded in a controlled way: $L_g \downarrow$ has to go together with $t_{ox} \downarrow$, $N_A \downarrow$, $t_{si} \downarrow$, $V_{dd} \downarrow$ and $W \downarrow$.

1.4 Motivation

In a conventional, bulk-silicon micro-circuit, the active elements are located in a thin surface layer (less than 0.5 μm of thickness) and are isolated from the silicon body with a depletion layer of a p-n junction. The leakage current of this p-n junction exponentially increases with temperature, and is responsible for several serious reliability problems. Excessive leakage currents and high power dissipation limit the operation of micro-circuits at high temperatures. Parasitic n-p-n and p-n-p transistors formed in neighboring insulating tubs can cause latch-up failures and significantly degrade circuit performance.

Silicon-on-insulator (SOI) technology employs a thin layer of silicon (tens of nanometers) isolated from a silicon substrate by a relatively thick (hundreds of nanometers) layer of silicon oxide. The SOI technology dielectrically isolates components and in conjunction with the lateral isolation, reduces various parasitic circuit capacitances, and thus, eliminates the possibility of latch-up failures. Figure 1.5 [7] shows the cross-section of the bulk and SOI

MOS devices. As shown in the Figure 1.5 [7], owing to the buried oxide isolation structure, SOI technology offers superior devices with excellent radiation hardness and high device density. SOI devices are more suitable with their steeper subthreshold slope(SS) which facilitates scaling of the threshold

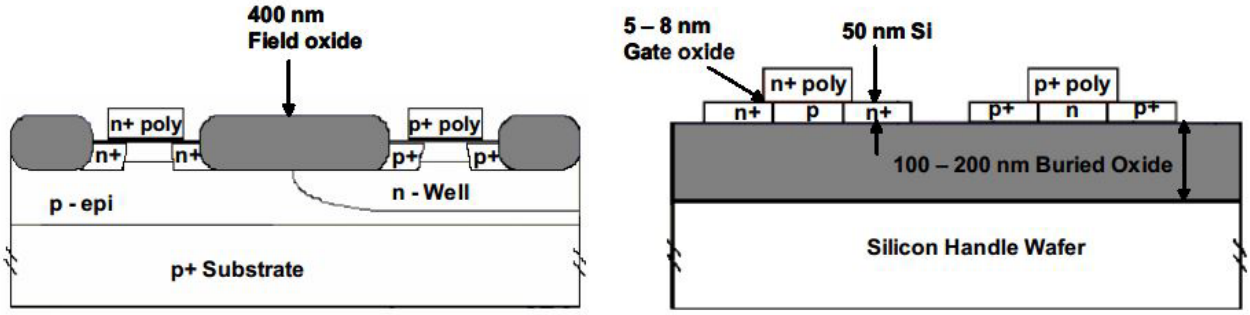

Figure 1.5: Cross-sectional view of the bulk-Si (left) and SOI (right) CMOS devices

voltage for low-voltage low-power applications. Depending on the thickness of the silicon layer, MOSFETs will operate in fully depleted (FD) or partially depleted (PD) regimes. When the channel depletion region extends through the entire thickness of the silicon layer, the transistor operates in a FD mode. PD transistors are built on relatively thick silicon layers with the depletion depths of the fully powered MOS channel shallower than the thickness of the silicon layer. The PD-SOI devices have many advantages like the fabrication process of PD-SOI devices is totally compatible with bulk silicon technology while fabrication of FD-SOI devices require development of ultra thin body, and, therefore needs more sophisticated technology. Hence, the design of bulk Si devices can be easily transferred to PD-SOI technology. Also V_T in PD-SOI is relatively less sensitive to the uniformity in the Si-film thickness while in FD-SOI device, V_T depends on Si film thickness and it is difficult to control the thickness of the ultra thin film body. As a result the film thickness becomes non-uniform across the surface. In spite of so many benefits, PD-SOI devices exhibit certain undesirable effect known as “kink effect”.

During the past few decades, excellent high-speed and performance have

been achieved through improved design, use of high quality material and shrinking device dimensions. However, with the reduction of channel length, control of short-channel effects is one of the biggest challenges in further down-scaling of the technology. The predominating short-channel effects are a lack of pinch-off and a shift in threshold voltage with decreasing channel length as well as drain induced barrier lowering (DIBL) and hot-carrier effect at increasing drain voltage. Therefore, to reduce this short channel effects to a greater extent a new device structure called Junctionless (JL) Transistors have been demostrated. Junctionless devices with a uniform doping concentration and type throughout the channel and source/drain extensions overcomes the challenges faced by the conventional nano devices. The schematic diagram of DG-JL MOSFET is shown in the Figure 1.6 [8]. JL MOSFETs

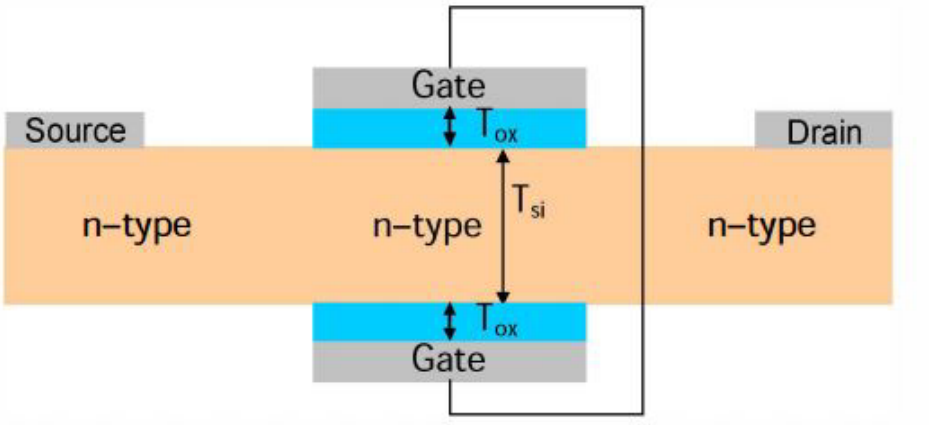

Figure 1.6: Schematic diagram of Double Gate(DG) JL MOSFET.

have extremely low leakage current and simple fabrication process and are less susceptible to SCEs when compared with classical inversion-mode devices. However, the high doping concentration in the channel reduces carrier mobility which results in lower drive current and transconductance (G_m) of JL MOSFETs.

1.5 Objectives

The salient objectives of the thesis are:

i. To study the "kink effect" visible in the output drain current-voltage characteristics of the PD-SOI MOSFET. The SELBOX structure is being proposed to minimize this non-linear effect so that it can be used for practical linear applications. The effect of dual insulator(DI) on the kink effect is also presented.

ii. To analyze the elctrical behavior of the recently newly developed structure called Junctionless transistors which offers excellent advantages over the conventional nano devices. These JL MOSFETs reduces SCEs to a much grater extent than conventional devices. Therefore, the DC and AC characteristics of DG JL MOSFETs are simulated and compared with those of the conventional DG MOSFETs.

1.6 Thesis Organisation

The dissertation is divided into five chapters and its outline is described as given below:

- **chapter 1: Introduction**
  Fundamental concepts related to technology scaling, SOI devices and its advantages and disadvantages, objectives of the project and outline of the thesis.

- **chapter 2: Short Channel Effects in Nanoscale MOSFETs: A Review**
  This chapter analyzes the origin and effect of the short-channel effects in nanoscale MOSFETs. Various methods employed to overcome short-channel effects are also summarized and the feasibility of various MOSFET structures in suppressing short-channel effects is discussed.

- **chapter 3: Analysis & Minimization of Kink Effect in PD-SOI MOSFETs**

  This chapter demonstrates the development of SELBOX structure in PD-SOI SOI MOSFET and illustrates the role of SELBOX structure in suppressing short-channel effects. The use of dual insulator (DI) for the minimization of kink effect is also presented.

- **chapter 4: Analysis of DC & AC Performance of DG Junctionless(JL) MOSFETs**

  This chapter deals with the simulation of DC and AC characteristics of junctionless MOSFETs and compared to those of conventional DG MOSFETs. The various AC parameters of DG JL MOSFETs are extracted and a comparison is being made with conventional DG MOSFETs.

- **chapter 5: Conclusion & Scope for Future Work**

Chapter 2

Short Channel Effects in Nanoscale MOSFETs: A Review

2.1 Introduction

In order to realize higher-speed and higher-packing density MOS integrated circuits, the dimensions of MOSFETs have continued to shrink according to the scaling law proposed by Dennard et al. [9]. However, the power consumption of modern VLSIs has become rather significant as a result of extremely large integration. Reducing this power is strongly desired. Choosing a lower power supply voltage is an effective method. However, it leads to the degradation of MOSFET current driving capability. Consequently, scaling of MOS dimensions is important in order to improve the drivability, and to achieve higher-performance and higher-functional VLSIs.

We can say that the story of MOSFET scaling is the history of how to prevent short-channel effects (SCE) [10]. SCE causes the dependence of device characteristics, such as threshold voltage, upon channel length. This leads to the scatter of device characteristics because of the scatter of gate length produced during the fabrication process. Moreover, SCE degrades the controllability of the gate voltage to drain current, which leads to the degradation of the subthreshold slope and the increase in drain off-current. Thinning gate oxide and using shallow source/drain junctions are known to

be effective ways of preventing SCE.

The detrimental short-channel effects occur when the gate length is reduced to the same order as the channel depth. When the channel length shrinks, the absolute value of threshold voltage becomes smaller due to the reduced controllability of the gate over the channel depletion region by the increased charge sharing from source/drain. The predominating features of SCE are a lack of pinch off and a shift in threshold voltage with decreasing channel length as well as drain induced barrier lowering (DIBL) and hot-carrier effects at increasing drain voltage. Increased charge sharing from source/drain degrades the controllability of gate voltage over channel current. This degradation is described as charge sharing by the gate and drain electric fields in the channel depletion layer in Poon and Yaus model [11], which was reported as the first SCE model.

This description can be applied to conventional MOSFETs fabricated in a bulk silicon wafer. What about the thin-film SOI MOSFETs ?. They are attractive devices for low-power high-speed VLSI applications because of their small parasitic capacitance [12]. Young [13] analyzed the SCE using a device simulator, and concluded that SCE is well suppressed in thin-film SOI MOSFETs when compared to bulk MOSFETs. In general, it is believed that thin-film SOI MOSFETs have a higher immunity to SCE compared to bulk MOSFETs. This may be due to the difference in source/drain junction depths between the two kinds of devices. For instance, the thickness of the silicon film, which corresponds to the source/drain junction depth of 50-100 nm, is common in 0.25-0.35 μm SOI MOSFETs. It is extremely shallow compared with the junction depth of 100-200 nm in 0.25-0.35 μm gate bulk MOSFETs. However, to take advantage of the ameliorated SCEs in deep-submicron fully-depleted SOI, t_{Si} must be considerably smaller than the source/drain junction depth (t_{Si} $\sim$10-15 nm). Moreover, there exits a strong coupling through the buried oxide in thin-film devices consequently, very thin buried oxides (t_b $\sim$100 nm) are needed which trade-offs with junction

capacitance considerations. Hence, for small-geometry SOI CMOS devices, short-channel effects are important [14, 15, 16, 17, 18].

2.2 Issues for Nanoscale MOSFETs

The various issues for nanoscale MOSFETs are categorized based on where the problems occur :

2.2.1 Channel

a) Sub-threshold leakage current:

The Sub-threshold leakage current is the weak inversion conduction current, which is dominated by the diffusion current flowing between the drain and source when $|V_{GS}|<|V_{th}|$. It is considered as one of non-ideal characteristics of MOSFET as a switching device and contributes major portions of the standby leakage power dissipation. This weak inversion conduction current can be expressed based on the Eq.(2.1) [19],

$$I_{subth}=\mu C_{dep}\left(\frac{W}{L}\right)V_T^2\left(\exp\left(\frac{V_{GS}-V_{th}}{nV_T}\right)\right)\left(1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right) \tag{2.1}$$

where $C_{dep}=\sqrt{\varepsilon_{Si}qN_{sub}/4\varphi_B}$ denotes the capacitance of the depletion region under the gate area, V_T is the thermal voltage which equals to k_BT/q, and n is the sub-threshold parameter and expressed as $1+C_{dep}/C_{ox}$.

Since, from Eq.(2.1), I_{subth} increases exponentially with both increasing V_{GS} and decreasing V_{th}, the partial derivative of $log_{10}I_{subth}$ with respect to V_{GS} yields a constant slope called sub-threshold slope (SS) and equals to

$$SS=\frac{\partial\left(\log_{10}\mathrm{I}_{subth}\right)}{\partial\mathrm{V}_{GS}}=\frac{1}{\ln 10\cdot\mathrm{I}_{subth}}\times\frac{\partial\mathrm{I}_{subth}}{\partial\mathrm{V}_{GS}} \tag{2.2}$$

This parameter shows how abruptly the transistor turns off with decreasing gate voltage. In order to turn off the transistor effectively, SS must be designed to be as small as possible. Figure 2.1 [5] shows that SS is always greater than 2.3 V_T ($\sim$60 mV/dec) at room temperature and shows how well the channel surface potential can be controlled by the gate contact. SS can be made smaller (close to $\sim$60 mV/dec) by using a thinner gate oxide thickness

(resulting in larger C_{ox}) or a lower substrate doping concentration (resulting in the larger depletion width beneath the channel, hence reduced C_{dep}).

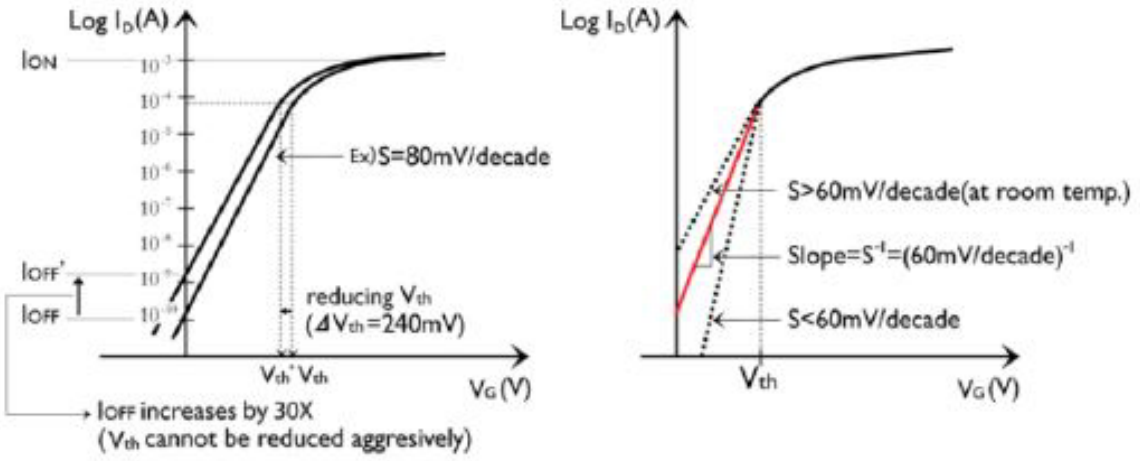

Figure 2.1: Characteristics of sub-threshold conduction.

In addition, under lower temperature operation, SS can be reduced since SS is a function of T. For MOS a transistor built in SOI technology, the sub-threshold swing is usually better than in bulk technology. In fact the sub-threshold swing of SOI devices can even reach the optimum value (2.3 V_T) depending on whether their bulk is fully depleted or partially depleted. This makes SOI a promising candidate for ultra low power CMOS applications [19].

b)Threshold Voltage Variations and Drain-Induced Barrier Lowering:

Since the threshold voltage (V_{th}) is directly related to the device speed and sub-threshold leakage current, it has to be minimized. It is generally explained in terms of a) V_{th} roll-off(or falloff) and b) Drain induced barrier lowering (DIBL).

The transistors with a different channel length (L) in the same wafer, even in the same die, yield different V_{th}. The threshold voltage reduction due to the reduced channel length represents V_{th} roll-off. Further V_{th} reduction

caused by increasing drain voltage describes DIBL as shown in Figure 2.2 [5]. Both phenomena stem from the lowered potential barrier between the drain and source due to the relatively increased charge-sharing effect between the channel depletion region and source/drain depletion regions comparing to long-channel device case. This charge-sharing effect makes a transistor require less gate voltage to deplete the substrate beneath the gate dielectric and makes V_{th} decrease [20].

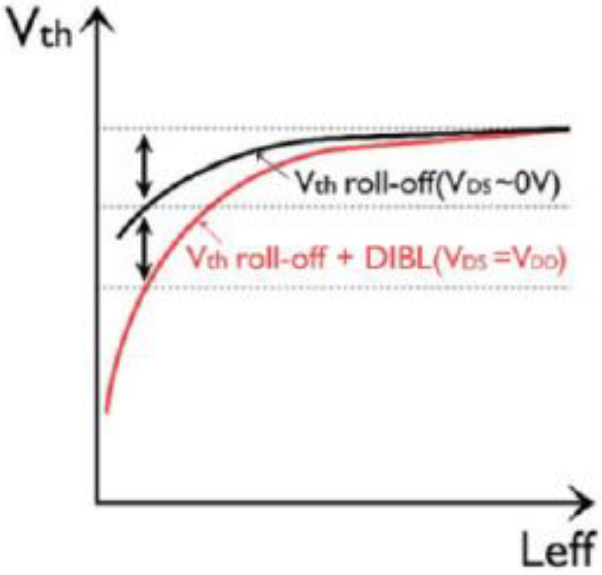

Figure 2.2: Threshold voltage roll-off and drain induced barrier lowering (DIBL).

The expressions for the drain and source junction widths are:

$$X_{dD}=\sqrt{\left(\frac{2\varepsilon_{Si}}{qN_A}\right)(V_{DS}+\varphi_{Si}+V_{SB})}, \quad X_{dS}=\sqrt{\left(\frac{2\varepsilon_{Si}}{qN_A}\right)(\varphi_{Si}+V_{Si})} \qquad (2.3)$$

where V_{SB} and V_{DB} are source-to-body and drain-to-body voltages. When the depletion regions surrounding the drain extends to the source, so that the two depletion layer merge (i.e., when $x_{dS} + x_{dD} = \mathrm{L}$), punchthrough occurs. Punchthrough can be minimized with thinner oxides, larger substrate doping, shallower junctions, and obviously with longer channels.

The current flow in the channel depends on creating and sustaining an inversion layer on the surface. If the gate bias voltage is not sufficient to

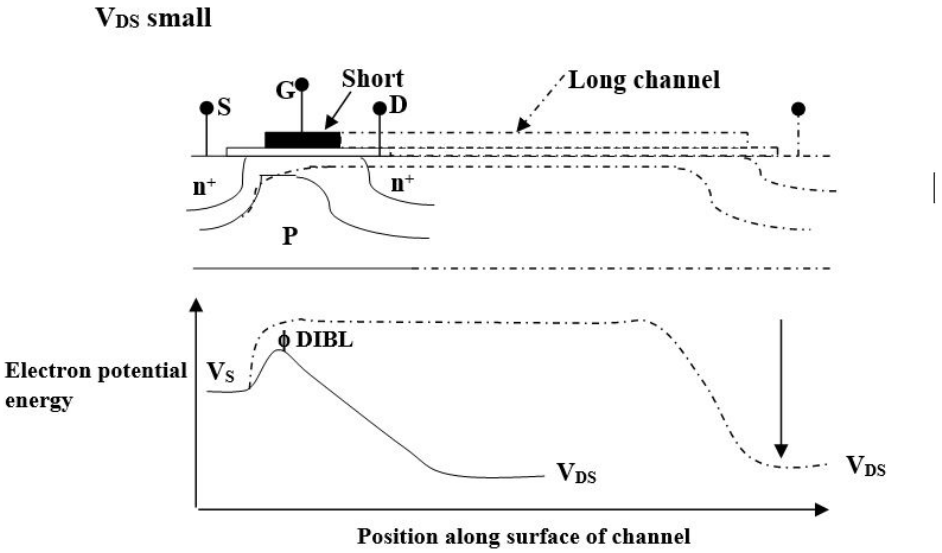

Figure 2.3: Electron Potential Energy Variations along the position in channel

invert the surface ($V_{GS} < V_{TO}$), the carriers (electrons) in the channel face a potential barrier that blocks the flow. Increasing the gate voltage reduces this potential barrier and, eventually, allows the flow of carriers under the influence of the channel electric field. In the weak inversion regime there is a potential barrier between the source and the channel region. The height of this barrier is a result of the balance between drift and diffusion current between these two regions. The barrier height for channel carriers should ideally be controlled by the gate voltage to maximize transconductance. However, in small-geometry MOSFETs, the potential barrier is controlled by both the gate-to-source voltage V_{GS} and the drain-to-source voltage V_{DS}. As indicated in Figure 2.3, drain-induced barrier lowering (DIBL) effect [20] occurs when the barrier height for channel carriers at the edge of the source reduces due to the influence of drain electric field, upon application of a high drain voltage. The reduction of the potential barrier eventually allows electron flow between the source and the drain, even if the gate-to-source voltage is lower than the threshold voltage. This increases the number of carriers injected into the channel from the source leading to an increased drain off-current. The channel current that flows under this conditions ($V_{GS} < V_{TO}$) is called

the sub-threshold current. Thus the drain current is controlled not only by the gate voltage, but also by the drain voltage.

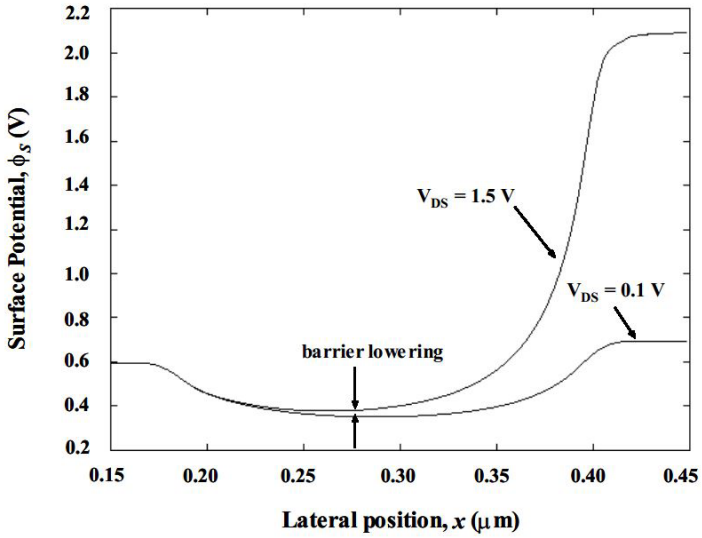

Figure 2.4: Surface potential variation along the position in channel for 0.1 V and 1.5 V drain voltages (linear and saturated case).

For device modeling purposes this parasitic effect can be accounted for by a threshold voltage reduction depending on the drain voltage [21]. In addition to the surface DIBL, there are two unique features determining SCEs in thin-film SOI devices viz.(a) positive bias effect to the body due to the accumulation of holes generated by impact ionization near the drain and (b) the DIBL effect on the barrier height for holes at the edge of the source near the bottom,as illustrated in Figure 2.4 [10].

Holes generated near the drain due to impact ionization accumulate in the body region, and then positively bias the body, reducing V_T as shown in the Figure 2.5. This positive bias effect leads to V_T lowering for all gate lengths, including rather long gates such as 2 μm. The hole generation rate due to impact ionization increases as gate length decreases under a fixed value of V_D. This effect is predominant in PD SOI nMOSFETs and results in so-called floating body effects(FBE) [22, 23].

The DIBL effect on the barrier height for holes reduces the positive bias

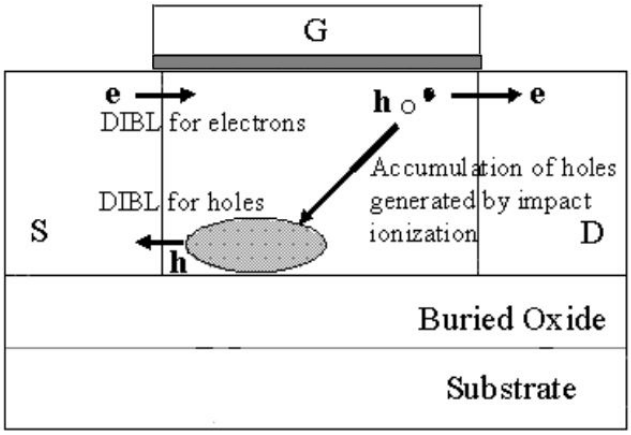

Figure 2.5: Three mechanisms determining SCE in SOI MOSFETs

effect to the body because the accumulated holes in the body can more easily surmount the barrier and flow to the source. As a result fewer number of accumulated holes remain which weakens the V_T lowering. The potential near the bottom in the thin-film increases as gate length decreases due to the drain electric field. This leads to the lowering of the barrier height for holes at the source edge near the bottom with shorter gate lengths. Figure 2.6 [10] compares the schematic energy band diagrams at threshold condition between short and long channels MOSFETs. The comparison is done near the bottom of the thin-film from the source to the drain. With shorter gate lengths, the barrier height for holes near the bottom is lowered by the influence of the drain electric field, and holes accumulated in the body region can more easily flow into the source.

Due to these three mechanisms, V_T dependence upon gate length in FD nMOSFETs becomes small, as illustrated in Figure 2.7 [10].

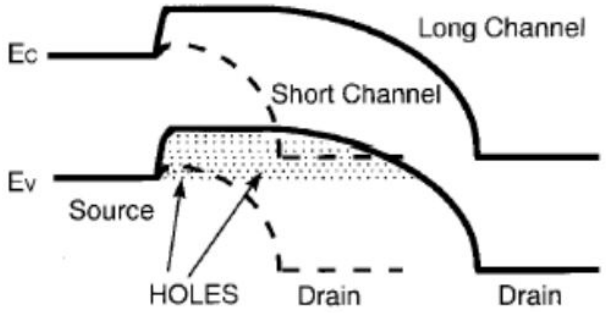

Figure 2.6: Comparison of schematic energy band diagrams near the bottom of the body between the long and short-channel fully depleted (FD) nMOSFETs

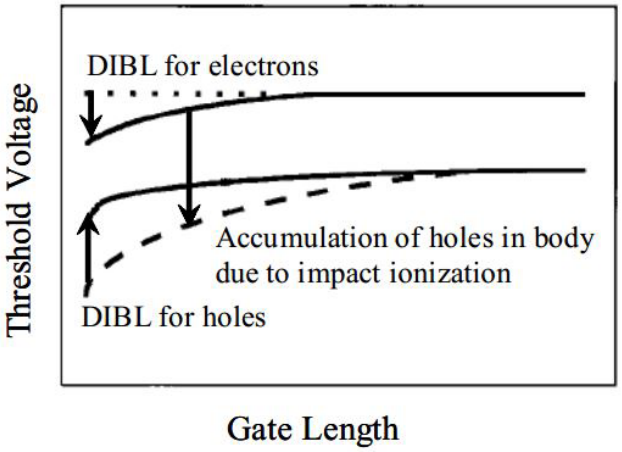

Figure 2.7: Effects of the three mechanisms on threshold voltage dependence on gate length

c) Carrier mobility degradation:

Since the rate of the supply voltage scaling has been reduced while the geometric scaling keeps the same historical rate, the electric fields inside the MOSFETs keep on increasing. The drift velocity of the carriers is proportional to the longitudinal electric field across the channel at low field ($<10^3$ V/cm). After that point, however, the increasing rate of the carriers velocity decreases with the increasing longitudinal field in Si at room temperature. Finally, the carriers reach their maximum velocity of $v_{sat} \sim 10^7$ cm/sec when the electric field exceeds $\sim 3 \times 10^4$V/cm for electrons and $\sim 10^5$V/cm for

holes (here the channel length (L) is assumed to be much greater than the average distance (l) between scattering events such as L≫10 nm.) This carrier mobility degradation is called "Velocity Saturation," and originates from various scattering mechanisms such as optical phonon scattering, phonon dispersion, phonon absorption as well as emission, and the energy band non-parabolicity [24, 25].

Another high electric field is developed between the gate and the channel due to the aggressive gate oxide thickness scaling with relatively constant supply voltage, which limits the charge carriers to a narrower region below the oxide-silicon interface, leading to more carrier scattering and hence lower mobility. Furthermore, the increased body doping by means of suppressing SCEs degrades the carrier mobility [25].

d) Hot carrier effects (HCEs):

The high electric fields in a device also cause reliability problems such as threshold voltage shifts and trans-conductance degradation due to "Hot Carrier Effects (HCEs)." As the average velocity of carriers in the channel saturates by the increased scattering rate at the high electric fields, the carriers can attain high kinetic energy. Once those hot carriers obtain sufficient energy to overcome barriers, they might migrate into the unwanted area such as the gate dielectric, gate, or substrate of a transistor. Particularly, the highly accelerated hot carriers near the drain region can generate new electron-hole pairs by collision with the silicon atoms, which is called "impact ionization." Impact ionization can cause significant increase in substrate current or carrier injection into the gate dielectric, which causes charges to get trapped in the gate oxide. This causes threshold voltage shifts and therefore the device becomes unstable and even can fail [25, 26].

e) Direct source to drain tunneling:

The ultimate physical scaling limit of MOSFETs is direct source-to-drain

tunneling. If the barrier width (transistor channel length) between source and drain becomes small enough for electrons to tunnel through the barrier without any additional gate bias, MOSFETs no longer can be used as a switch. When we consider only over-barrier transition of electrons but the direct tunneling, from the well-known Shannon-von Neumann-Landauer (SNL) expression, the minimum energy barrier to separate two different states of electrons is E_{SNL}= k_BT(ln2) = 0.017 eV at room temperature (T = 300 K), where k_B is the Boltzmann constant and T is the temperature. Therefore, the smallest energy required to process a bit is E_{bit}>E_{SNL}= k_BT(ln2) = 0.017 eV. Also, according to quantum mechanics the minimum channel length (barrier width) able to resist E_{bit}, not to allow tunneling, is about 5 nm. In order to achieve a smaller channel length, it is necessary to increase the E_{bit}. However this, in turn, tradeoffs with the growth of total power dissipation in a chip. Therefore, enhanced cooling techniques become the critical issues to achieve this goal.

2.2.2 Gate

a) Direct tunneling gate leakage current:

With the continuous device scaling, the gate oxide thickness has been accordingly reduced to maintain the gate controllability over the channel. However, as the gate oxide thickness scales below 2 nm, the direct tunneling (DT) gate leakage increases exponentially due to quantum mechanical tunneling. The DT gate leakage current can not only increase standby power dissipation but also limit the proper device operation. These serious problems can be solved by replacing SiO_2 with higher permittivity (high-k) gate dielectrics, which allows a physically thicker dielectric layer to have an EOT [27].

b) Gate depletion:

Polycrystalline silicon (poly-Si) has been widely used as the gate electrode material of MOSFETs since it replaced aluminum on account of its superior thermal stability to higher processing temperature. In addition, the use of

poly-Si as gate electrode has reduced the overall number of processing steps by means of self-aligned processing, where the gate itself is used as a hard mask during ion implantation for the source and drain junction formation. This technique allows tighter overlap between gate and source/drain regions and results in lower parasitic capacitance.

However, even heavily doped poly-Si gate electrode has a certain resistance which contributes to a considerable RC time delay. Furthermore, when the doping concentration of the polySi is not sufficient, at high gate bias during inversion, a region in the poly-Si gate electrode adjacent to the poly-Si/SiO_2 interface becomes depleted with carriers, which is called "Poly-depletion Effect." This results in increased EOT and hence significant decrease in the drive capability of transistor. For these reasons poly-Si is not suitable for the future gate electrode and new materials are required. Fortunately, metal gate electrode with a suitable work function (WF) shows many advantages such as lower gate sheet resistance and no boron penetration and poly depletion effect. However, the selection of metal gate substitutes for poly-Si, which are compatible with the new high-k gate dielectrics, is not as advanced [28].

2.2.3 Drain/source

a) Parasitic resistance (suppress on-current):

As the device gets smaller, the influence of parasitic resistance on on-current increases significantly. Therefore, proper control of parasitic resistance in a MOSFET becomes more important to achieve further performance improvement. The total parasitic resistance, which accounts for the voltage drop between channel and S/D contacts, can be divided into the four components such as overlap resistance, extension resistance, deep resistance, and silicide-diffusion contact resistance. Shallower S/D junction depths are desired to suppress SCEs effectively; however, since the shallower junction also increases the sheet resistance, the S/D doping must be increased accordingly to keep the sheet resistance constant. In addition, the ultra-shallow junctions

are difficult to form and also cause significant increase in BTBT leakage current [29].

b) Parasitic capacitance:

In digital switching applications, lower capacitance, along with higher drive current, is the main factor for high performance CMOS circuit design, because the conventional CMOS inverter delay model is given by $C_G V_{DD}/I_D$, where C_G is gate capacitance, V_{DD} is supply voltage, and I_D is drain on-current. Thus, with geometry scaling, the performance improvement has been achieved because the gate capacitance consisting of both intrinsic gate capacitance (C_{int}=$C_{GC} + 2C_{OV}$) and parasitic capacitance ($C_{para} \sim C_{fringe} + C_{gco}$) decreases in proportion to the gate length reduction in micro MOSFET, where C_{GC} is gate-to channel capacitance, C_{OV} is drain/source-to-gate electrode overlap capacitance, C_{fringe} is inner/outer fringing capacitance, and C_{gco} is gate-to-contact capacitance. However, as MOSFET enters into nano regime, gate capacitance does not decrease in proportion to the gate length reduction due to relatively increased parasitic capacitance. Therefore, in order to sustain performance improvement from scaling, parasitic capacitance reduction technique is required [30].

2.2.4 Substrate (bulk)

a) Reverse-biased junction leakage current(reverse-biased BTBT current):

Reverse-biased junction leakage current (I_{REV}) is the current flowing between the source/drain(S/D) and the substrate through the parasitic reverse-biased pn-junction diode in the off-state MOSFET. I_{REV} mainly consists of the diffusion and drift of minority carriers near the depletion region edge and the generation of electron-hole pairs in the depletion region of the reverse-biased pn-junction. If both S/D and substrate regions are heavily doped, BTBT dominates the I_{REV} since the electric field across the junction depletion region increases. If the high electric field ($>10^6$V/cm), so that the volt-

age drop across the junction is bigger than the band gap of silicon, is formed across the reverse-biased junctions of the source/drain (S/D) regions, especially with increasing S/D voltage or reverse body bias, significant amount of BTBT current flows through the S/D to substrate junctions. In nanometer devices, higher channel and S/D doping with shallow junction depths are required to minimize SCEs, there is significant increase in BTBT current.

Recently high-mobility channel materials, such as Ge, strained-Ge(s-Ge), s-SiGe, and III-V materials (GaAs, InAs, InSb, and InGaAs), are actively being researched as candidates for future channel materials of highly scaled MOSFETs. However, since most of high-mobility materials have lower band gaps than Si, BTBT leakage currents increase significantly. Therefore, various device structures to minimize BTBT currents are being developed. The various leakage mechanisms in a MOSFET are illustrated in Figure 2.8.

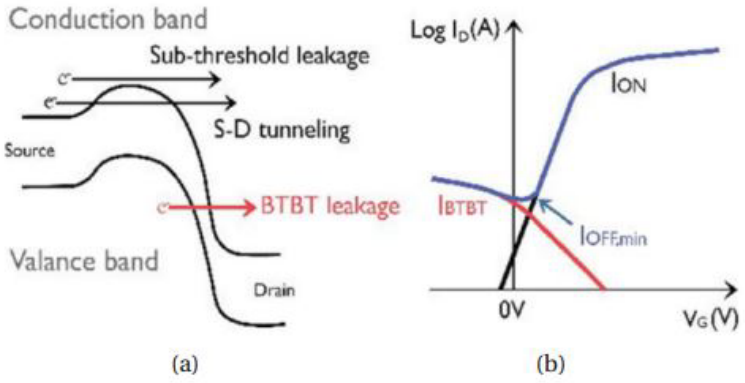

Figure 2.8: (a) Various leakage mechanisms in a MOSFET (left), (b) I_{OFF},min is the minimum achievable leakage current in a MOSFET. In low E_G materials it is generally limited by I_{BTBT}.

b) GIDL current (Surface BTBT current):

GIDL current, also called surface BTBT current, has become one of the major off-state leakage current components in state-of-the-art MOSFETs. When the drain of n-MOSFET is biased at the supply voltage(V_{DD}) and the gate is biased at either zero or negative voltage, a depletion region is formed

under the gate and drain overlap region. In the same way as the BTBT current, if the high electric field is formed in the narrower depletion region as a result of the reverse-bias between channel and drain, a significant amount of surface BTBT current flows through drain to substrate junctions due to twisting of bandgaps.

2.3 Solutions to Short Channel Effects

As the gate length of the MOSFET is scaled into the sub-100-nm regime for improved performance and density, the requirements for body-doping concentration, gate oxide thickness, and source/drain (S/D) doping profiles to control short-channel effects become increasingly difficult to meet when conventional device structures based on bulk silicon substrates are employed. The heavy channel doping required to provide adequate suppression of SCE results in degraded mobility and enhanced junction leakage. The aggressive reduction of the gate dielectric thickness for reduced SCE and improved drive current leads to increased direct tunneling gate leakage current and standby power consumption, and also raises concerns regarding the gate oxide reliability.

Figure 2.9 [1]schematically shows the electric field lines from the drain encroaching on the channel region.

As shown in the Figure 2.9 , the gate electrode shields the channel region from those lines at the top of the device, but electric field lines penetrate the device laterally and from underneath, through the buried oxide and the silicon wafer substrate causing the undesirable DIBL for the charge carriers. To overcome all the short channel effects several innovative techniques have been introduced. These are:

2.3.1 High-k Dielectric Material Gate

One of the key innovation enablers for 45 nm process technology and beyond is the high-k/metal gate transistor, which is regarded as one of the biggest

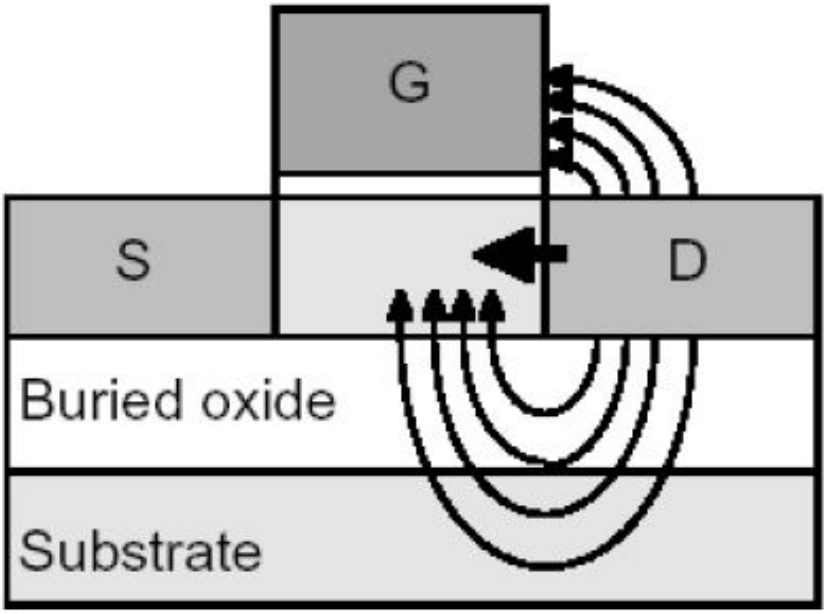

Figure 2.9: Electric field lines from the drain [1]

developments in transistor design in 40 years. High-k/metal gate have enabled the continuous EOT scaling. The dielectric constant, k, is a parameter defining ability of material to store charge. Consequently, it also defines capacitance, C of any capacitor comprising of a layer of dielectric sandwiched between two metal plates. In the figure below size of the upper plate defines area of the capacitor contact (A).

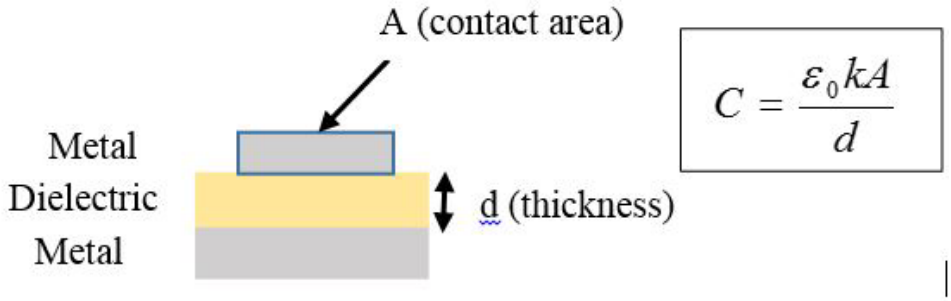

Figure 2.10: High-k Metal Gate Structure

All other parameters equal, k would determine capacitance of the above structure, or in other words, it would define the extent of capacitive cou-

pling between two conducting plates - with high-k dielectric such coupling would be strong, and with low-k dielectric being obviously weak. In Si technology the reference is a value of k of silicon dioxide, SiO_2, which is 3.9. Dielectrics featuring k>3.9 are referred to as high-k dielectric while dielectric featuring k<3.9 are defined as low-k dielectrics. In cutting edge silicon nanoelectronics, both high-k and low-k dielectrics are needed to implement fully functional very high-density integrated circuit, although, for drastically different reasons. High-k dielectrics are needed in MOS gate stacks to maintain sufficiently high capacitance of the metal (gate) - dielectric-Si structure in MOS/CMOS transistors. Due to the continued scaling of the channel length (L), and hence reduced gate area A, the need to maintain sufficient capacitance of the MOS gate stack was met by gradual decrease of the thickness of SiO_2 gate oxide. Recently, high-k dielectric based on Hafnium and dual metal gate has been introduced to increase transistor performance while also reducing gate leakage as gate dielectric thickness actually increased while also the gate capacitance increased.

However, such scaling cannot continue indefinitely as at certain point gate oxide will become so thin (thinner than about 1 nm) that, due to excessive tunnelling current, it would stop playing role of an insulator. Hence, dielectric featuring k higher than 3.9, i.e. one assuring same capacitive coupling but at the larger physical thickness of the film, must be used instead of SiO_2 as a gate dielectric in advanced MOS/CMOS integrated circuits. On the opposite end of the spectrum finds itself a multi-layer metallization scheme in which inter-layer-dielectric (ILD) is used to electrically insulate metal lines. In this case it is of critical importance that the capacitive coupling between adjacent interconnects lines is as limited as possible. Hence, a low-k dielectric must be used to assure as little capacitive coupling between interconnect lines as possible. Whether the problem is with high-k dielectrics for MOS gates or low-k dielectrics for ILDs, lack of viable technical solutions in either of these areas will bring any future progress in mainstream silicon technology [31].

2.3.2 Silicon-on-Insulator (SOI)

With physical separation between individual devices in ultra-high density CMOS integrated circuits measured in nanometers, proper electrical isolation between them is a key challenge. The SOI (Silicon-On-Insulator) substrate wafers, as opposed to conventional bulk wafers, not only solve the problem of electrical isolation between adjacent devices but also allow innovative device layouts resulting insignificantly better than in the case of bulk substrates performance of CMOS circuitry. Hence, SOI substrates rapidly become an important element of the advanced silicon IC technology. The advantages of SOI technology come from its buried oxide (BOX) layer as shown in Figure 2.11. With the reduction of the parasitic capacitances, mostly as a result of the reduced drain/source junction capacitances, SOI devices yield improved switching speed and reduced power consumption. The operating speed is also improved since the isolated channel from substrate bias prevents the increase in a threshold voltage of stacked SOI transistors. In addition, the perfect lateral and vertical isolation from substrate provides latchup and inter-device leakage free CMOS technology, reduction in various interferences, and better soft error immunity. Moreover, SOI technology offers tighter transistor packing density and simplified processing [2].

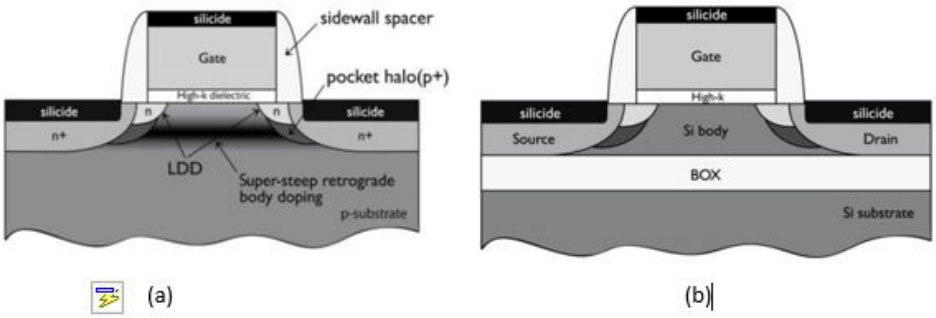

Figure 2.11: a) Cross-section of an advanced MOSFET. b) Cross-section of a SOI MOSFET [2].

SOI transistors are classified into two types; “partially depleted(PD) SOI,”

if the silicon film (typically 100 nm or more) on the BOX layer is thicker than the depletion region depth beneath the gate oxide, and "fully depleted (FD) SOI," if the body (silicon film) thickness is thin enough (typically 50 nm or less) or the doping concentration of the body is low enough to be fully depleted. FDSOI transistors have superior advantages over PD SOI transistors in terms of extremely low sub-threshold swing (<65 mV/decade), no floating-body effects, and low threshold voltage variation with temperature (2-3 times less). However, since FD SOI transistors are even more sensitive to process variation such as the silicon film layer variation resulting in threshold voltage fluctuation, PD SOI devices were commercially introduced first.

Another important merit of SOI technology is that it provides the cornerstone for new device structures such as multi gate field-effect transistors (MuGFETs), which includes more than one gate into a single device. The double-gate (DG) FET shown in Figure 2.12(b) is the first step for those multi gate devices. Since the transverse electric field induced by V_{DS} is shared by both top and bottom channels, it mitigates SCEs.

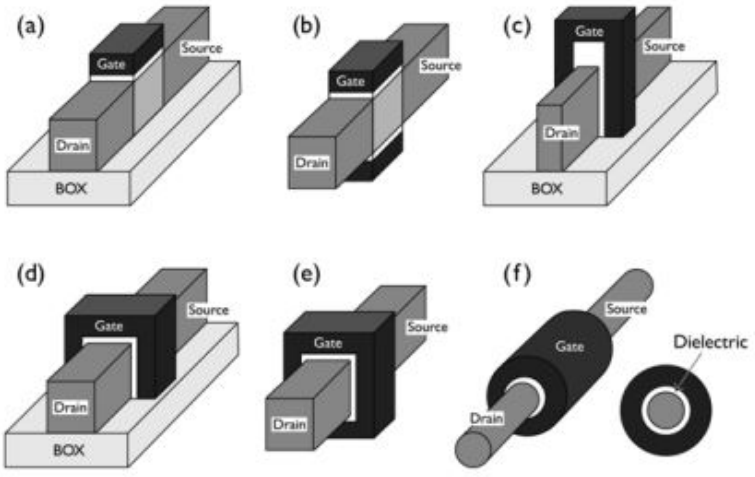

Figure 2.12: Various SOI device: (a) Single gate SOI transistor, (b) double gate planar SOI transistor, (c) double gatenon-planar FinFET, (d) trigate FET, (e) quadruple-gate (or gate-all-around) FET, and gate-allaround (or surrounding gate) FET (nanowire FET).

On the other hand there is a significant drawback in SOI technology. Since the BOX, which has approximately 100 times lower thermal conductivity

than that of silicon, prevents thermal conduction path from SOI transistors to the substrate, SOI transistors are easily affected by the thermal heating generated in the channel, which is called Self-Heating Effects. Consequently, the self-heating degrades the mobility of carriers and causes the threshold voltage shift. These effects get worse with FD structures because they use thinner silicon films.

2.3.3 Strained Silicon Technique (S-Si) Structures

Mobility loss resulted from higher channel doping and scaled gate dielectrics should be compensated to meet the performance targets of the future technologies. In parallel with SOI technology, there has been more straight forward and cost effective way to improve device performance and scalability. That is mobility-enhancement technology. Both the high mobility channel materials (such as Ge and GaAs) and the strained channel by means of stress offer mobility enhancement. Various CMOS fabrication processes can be used to induce appropriate strain to the channel region of the MOSFETs.

The strain in crystalline solid results from the relative displacement of atoms in the lattice. The strain creates proportional distortion of key material properties of semiconductor including energy gap and effective mass of an electron in the strained region is reduced, hence, its mobility is increased. Consequently, creation of strain in the region of transistor in which mobility of electrons has an effect determining its performance will result in the faster switching transistor. Due to the performance enhancing properties, the lattice-mismatched semiconductor heterostructures containing strained films are rapidly growing in importance in semiconductor device technology. The most innovative way on strained-Si was focused on biaxial global strain generated by depositing a thin layer of silicon on a relaxed SiGe virtual substrate. This results in enhanced carrier transport in the strained Si layer, and mobility enhancements of 110% for electrons and 45% for holes. A cross-sectional view of transistors fabricated with strained Si-channel is shown in Figure 2.13.

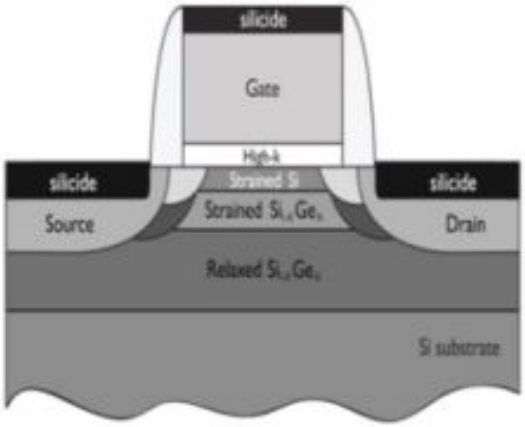

Figure 2.13: MOSFET with a strained-silicon channel [2].

Appropriately applied strain to the MOSFET channel can significantly improve the device performance by means of modifying energy bands and increasing mobility of carriers in silicon. Strain is expected to continue CMOS technology scaling for the time being [2].

2.4 Standard MOSFET models

Some semiconductor industry standard compact models, such as charge, potential and conductance based models are reviewed here.

2.4.1 Charge based MOSFET model

The charge based modeling approach is one of the basic and primitive modeling approaches. It is based on the computation of the inversion charge density in the MOSFET channel in terms of the terminal voltages, i.e. gate and drain voltages. This model is a regional model because it explains the behavior of the MOSFET separately in all regions of its operation. So, these models require smoothing parameters, they are somewhat empirical in the interfacing regions and, thus the device is not described accurately.

The prominent charge based models are level 1, level 2, and level 3, BSIM 1, HSPICE level 28, BSIM 2, BSIM 3, BSIM 4, and BSIM 5. BSIM 5 is used for sub-100nm CMOS circuit simulation. This model is applicable to deep

sub-micron region, and attempts have been made to include the modeling of strained silicon technology in the latest spice models. BSIM 4 considers the influence of stress of mobility, velocity saturation, threshold voltage, body effect and DIBL effect. But the equations expressed are mostly empirical and no analytical models have been given.

2.4.2 Potential based MOSFET model

This model approach is more accurate than the charge based models. It is based on the calculation of the potential in the channel of a MOSFET to determine the I-V and C-V characteristics. Some of the models based on the approach are SP models by penn-state university, USA, HISIM (Hiroshima-University, STARC IGFET model) valid down to sub-100nm MOSFETs. This model is applicable to the sub micron region and attempts have been made to include the modeling of strained silicon technology.

2.4.3 Conductance based MOSFET model

This modeling approach is suitable for low power, short channel applications for analog design. It is known as the EKV (Enz-Krummenachar-Vittoz) model, which has been developed by the Swiss Federal Institute of Technology, Switzerland. This model keeps the substrate as the reference rather than the source, as observed in the potential based and charge based models. Due to its complexity, it is much less used for modeling purposes. Moreover, no stress modeling has been done in this model. In all the approaches mentioned above, attempts have been made to model MOSFETs. But most of the models that have been proposed are either empirical in nature. Therefore, there is a need for a more physics based approach to accurately explain the behavior of the device [32].

2.5 Multi-gate MOSFET: The Future CMOS Transistor

2.5.1 Advantages of Multi-gate MOSFETs

The main advantage of the multi-gate devices is to improve the short channel effects. Since the channel (body) is controlled electrostatically by the

gate from multiple sides, the channel is better-controlled by the gate than in the conventional transistor structure. Unwanted leakage components are reduced and a small transistor can be used to continue the cost reduction through miniaturization. Improved gate control also provides lower output conductance, i.e., smaller dI_{ds}/V_{ds} in the current saturation region. This provides greater voltage gain, which is beneficial to analog circuits as well as to the noise tolerance of digital circuits.

A second advantage of the multi-gate devices is the improved on-state drive current (I_{on}) and therefore faster circuit speed. I_{on} improvement arises from several reasons. Reduction of channel doping reduces impurity Columbic scattering. Reduced channel doping reduces the electric field normal to the SiO_2 interface and therefore reduces the surface roughness scattering. Finally, a promising multi-gate structure, the FinFET, provides a larger channel width with a small footprint in area. This raises I_{on}, which is handy for driving a large capacitive load such as long interconnect.

A third advantage is the reduced manufacturing variation. In the absence of channel dopants, the effect of random dopant fluctuation (RDF) is minimized. Lower SRAM supply voltage for the FinFET multi-gate technology compared to traditional bulk MOSFET technology has been experimentally demonstrated. The advantages of multi-gate devices are well known and demonstrated in many FinFET technologies.

2.5.2 Different Multi-gate MOSFET Structures

There are different flavors of multi-gate MOSFETs. Several examples are shown in Figure 2.14 and Figure 2.15 respectively. The FinFET consists of a thin silicon body (the fin) and a gate wrapping around its top and two sides. FinFETs can be made on either bulk or SOI substrates, creating the bulk FinFET or the SOI FinFETs. In some FinFET processes the oxide hard mask on top of the fin is not removed, creating the double-gate FinFET. In double-gate FinFETs the top surface of the fin does not conduct current, whereas in triple-gate FinFETs the side surfaces and the top surface all con-

duct current. Another example of multi-gate MOSFET is the all-around gate device. It consists of a pillar-like body surrounded by the gate dielectric and the gate. The nanowire MOSFET is one example of all-around gate devices. Depending on the fabrication process, the channel may be either vertically or horizontally oriented. Optionally, a FinFET can have two separated gates that are independently biased. This can be achieved by removing the top portion of the gate of a regular FinFET using chemical mechanical polishing, forming the independent double-gate FinFET. Independent double-gate MOSFETs may also be made as a planar device. The planar double-gate SOI is essentially a planar SOI MOSFET with a thin buried oxide (labeled as BOX).

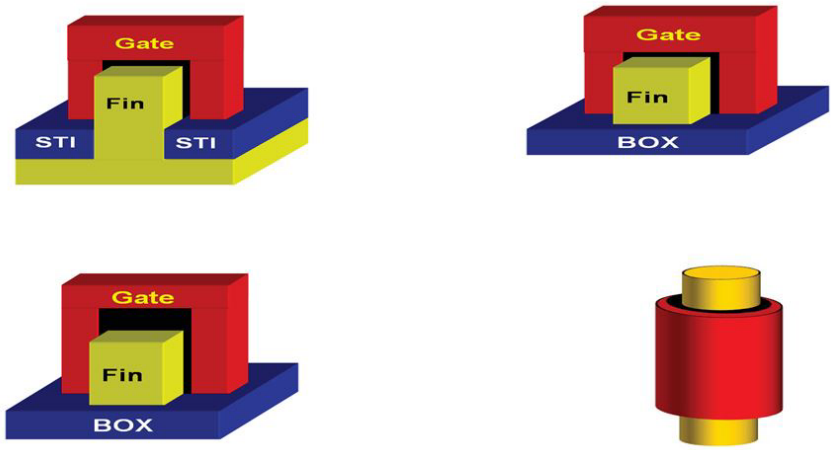

Figure 2.14: Multigate MOSFETs: a) Triple-Gate FinFET on Bulk Si b) Triple-Gate FinFET on SOI c)Double-Gate FinFET on SOI d) All-Around Gate

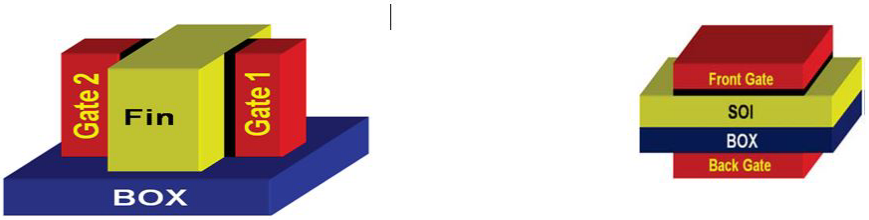

Figure 2.15: Multigate MOSFETs: a) Independent Double-Gate FinFET on SOI b) Planar Double-Gate SOI

A heavily-doped region in silicon under the buried oxide acts as the back-gate. Unlike the front-gate, the back-gate is primarily used for tuning the device threshold (V_{th}). The buried oxide is usually thick such that the back-gate cannot induce an inversion layer at the back surface. V_{th} tuning can be used to compensate for variability in IC manufacturing from chip to chip or even circuit to circuit within the same chip. Doing so improves the IC speed and power consumption. It can also be used to dynamically rise or lower V_{th} circuit by circuit within a chip in response to the need for less leakage or more speed. This is a very effective means of managing power consumption.

2.6 Summary

As dimensional scaling of CMOS transistors is reaching its fundamental limits, various researches have been actively carried out to find an alternative way to continue to follow Moores law. Among these efforts, SOI devices have been well recognized for their advantages in integrating deep sub-micron CMOS devices. However, with the reduction of channel length, short-channel effects are becoming increasingly important. SCE degrades the controllability of the gate voltage over drain current due to increased charge-sharing from the drain/source regions, which leads to the degradation of the sub-threshold slope and the increase in drain off-current. The last decade has seen increasing amount of effort focused to circumvent the undesirable short-channel effects (SCE). Engineering channel doping in a controlled way is prohibitively difficult with extremely thin-films and scarce and randomly positioned dopant atoms, implying yield and reliability problems. Therefore, an additional constraint, 'reliability,' has to be added to the conventional low-power, high-speed and high-density design consideration. On the other hand, buried oxides thinner than 100 nm are needed to avoid coupling, which trades-off with junction capacitance considerations. Multiple gate SOIs offer a better immunity against SCE but they are difficult to integrate in the current CMOS fabrication technology. Selective buried oxide(Selbox) SOI MOSFETs structure promise simultaneous suppression of FBE and keeping

intact the associated advantages with SOI devices. Also recently proposed junctionless MOSFETs as an alternative solution to suppressing SCEs better than conventional inversion-mode devices is discussed. Therefore, a systematic analysis of the effect of Selbox structure on SOI and multigate junctionless MOSFETs is required to aid in understanding its efficacy in suppressing SCE in deep sub-micron CMOS devices.

Chapter 3

Analysis & Minimization of Kink Effect in PD-SOI MOSFETs

3.1 Introduction

The MOS transistors fabricated on silicon on insulator (SOI) devices has been an area of great research from the past several years .The MOSFET devices on SOI offer several advantages over bulk MOSFETs such as improved lateral and vertical isolation, improved latch free operation, better threshold swing, lower parasitic capacitances resulting in lower power consumption, better switching speeds leading to faster operation of the circuits [33, 34].

The Silicon-On-Insulator (SOI) devices are basically classified into two types i.e. partially-depleted silicon-on-insulator (PD-SOI) and fully depleted silicon-on-insulator (FD-SOI). However, in spite of several advantages offered, the SOI devices are affected by certain undesirable effects such as floating body effects, the suppression of which has been an area of great challenge [35, 36, 37]. A MOSFET fabricated on SOI structure shows some incomparable characteristics inherent in the floating body substrates and one such effect is the kink effect. But, this kink effect is observed in the drain current-voltage characteristics of PD-SOI MOSFET devices as shown in the Figure 3.4. As a result, the device is not suitable for linear applications because of the non-linearity presented by the kink effect [38, 39, 40, 41].

In this chapter, method of elimination of kink effect with the use of SELBOX structure has been presented. The SELBOX structure provides increased performance by taking into account SELBOX gap length (g) and BOX thickness (w) as parameters for device optimization. This chapter also presents the variation of the kink voltage with respect to gate oxide thickness. The simulated results show that the kink can be minimized up to a certain extent using a dual insulator of equal length in PD-SOI devices below the gate electrode. All the simulated results have been carried out using the 2-D ATLAS simulator. The details of the simulation parameters has been described and displayed in the next section. The device characteristics obtained using the SELBOX structure particularly with the variation of different SELBOX parameters (i.e. gap length (g) and gap width(w)) has been presented and a comparison study has been made with the PD-SOI and bulk MOSFET devices. The analysis of output device characteristics of PD-SOI devices using single and dual insulator has also been carried out. The variation of kink voltage with varying gate oxide thickness has also been analyzed.

3.2 Device Structures

The schematic structures of PD-SOI, SELBOX structure and PD-SOI with double insulator (DI) MOSFETs are shown in Figure 3.1, Figure 3.2 and Figure 3.3 respectively. In these structures the channel length (L) and Source/Drain length (L_S/L_D) is fixed as 200 nm, 750 nm respectively. The silicon thickness (t_{Si}) is kept as 490 nm and a uniform doping density of source/ drain (N_D) and channel/body (N_A) is selected as $1 \times 10^{19} cm^{-3}$, $2 \times 10^{17} cm^{-3}$ respectively. The oxide thickness is maintained at t_{ox}=10 nm for the structures in Figure 3.2 and Figure 3.3 and a plot of electrical output characteristics between drain current V_S. voltage is analyzed for varying gate oxide thickness (t_{ox}) for Figure 3.1. The work function for the gate material is assumed to be M1=4.8ev. In Figure 3.3 the device structure with dual insulator (DI) having permittivity of 3.9 and 20 is considered respectively.

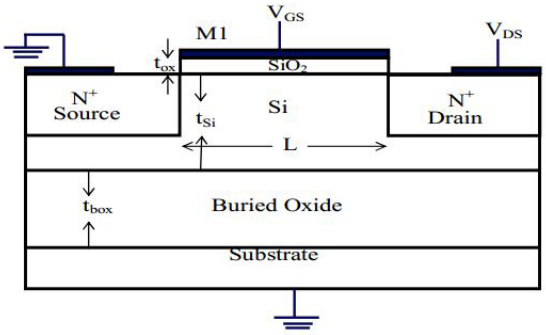

Figure 3.1: Device structure of PD-SOI

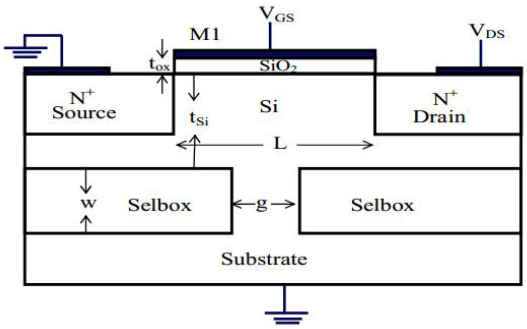

Figure 3.2: Device structure of Selbox

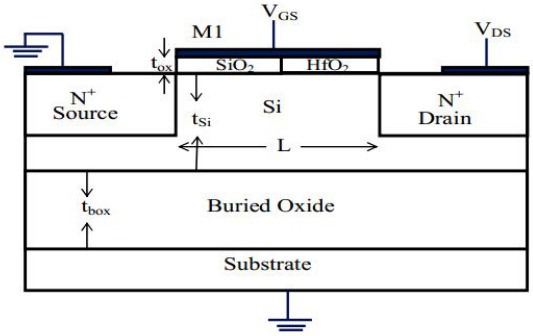

Figure 3.3: Device structure of PD-SOI using Dual Insulator

3.3 Simulation

In this chapter, ATLASTM (SILVACO) tools are used for device simulation. Silvaco atlas is used to simulate the electrical output characteristics of the semiconductor device under study. Numerical simulation is being carried out using the atlas tools from Silvaco. Depending upon the literature of SOI

devices the models activated in the simulation are field dependent mobility model (FLDMOB), Shockley Read Hall recombination (SRH), and impact ionization model from Selberherr. The field dependent mobility model provides a smooth transition between low field and high field. This model is required to consider any type velocity saturation effects. We choose Gummels method (or the decoupled method) along with Newtons method (or the fully coupled method) to solve the equations included in the FLDMOB and SRH model.

3.4 Results and Discussion

Figure 3.4 illustrates the typical output characteristics between I_D V_S. V_{DS} obtained for PD-SOI device using atlas simulations. As can be seen from the figure, the onset of kink takes place at a kink voltage of 1V for gate-source voltage (V_{GS}) of 2.2V. The simulated output characteristics of bulk MOSFET with identical device dimension and doping concentration along with PD-SOI characteristics is illustrated and compared in Figure 3.5 . From Figure 3.5, presence of kink is clearly visible in PD-SOI device while the same is not present in bulk MOSFETs.

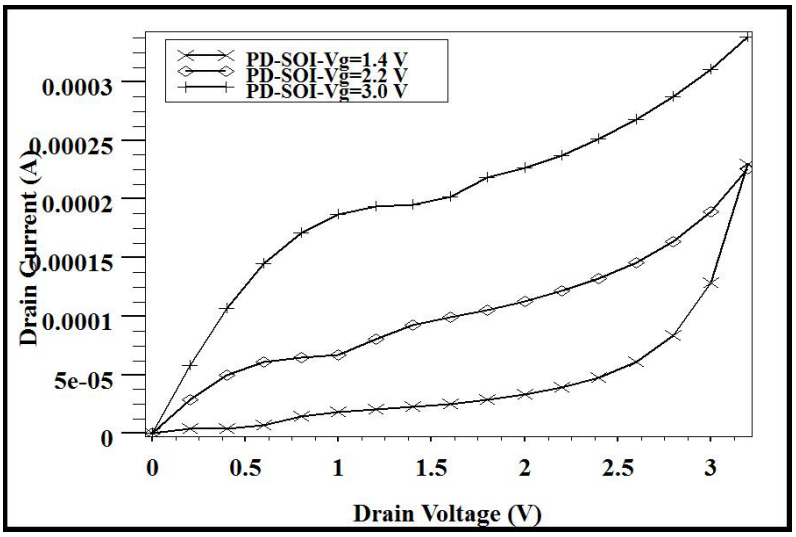

Figure 3.4: Simulation of Drain Current (I_D) as a function of Drain Voltage (V_{DS}) for PD-SOI MOSFET

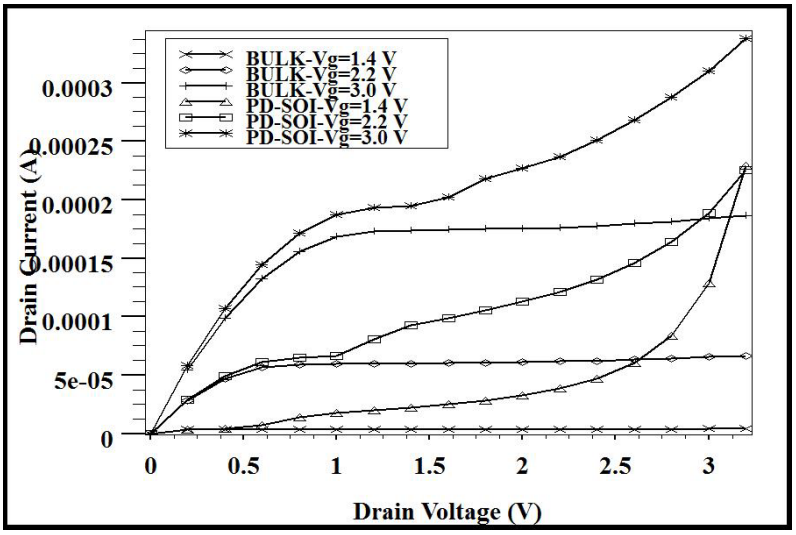

Figure 3.5: Simulation of Drain Current (I_D) as a function of Drain Voltage (V_{DS}) for both BULK and PD-SOI MOSFET

In order to minimize the kink in the output characteristics of PD-SOI device selbox structure is designed as shown previously in Figure 3.2.

The simulated output characteristics of selbox device, the structure of which is explained with the help of Figure 3.2 is illustrated in Figure 3.6 and Figure 3.7 respectively. The selbox structure is very much similar to the bulk MOSFET device except the presence of back oxide partially covering the channel. Figure 3.6 gives the output characteristics of the selbox device with varying gap length. In this figure, the oxide thickness has been maintained at 0.4μm. The gap length(g) is increased from 0.004μm to 0.010μm. The increase in gap length results in an increase in the kink voltage because with increased gap length the kink occurs at a higher drain voltages. Consequently, for larger values of gap length the kink will completely disappear and eventually coincides with the output characteristics of the bulk MOSFET. For very narrow gap length, it is noticed that selbox device still behaves like an SOI device and marks the presence of kink in the output characteristics. Therefore, to minimize the kink in the output characteristics, the gap length is varied until the kink disappears. Figure 3.6 shows that the kink voltage becomes larger than the 3.5 V for a gap length of 0.010μm. Hereafter, any

further increase in gap length will result in the output characteristics of bulk MOSFET and is thus less likely to have the other advantages associated with an SOI device.

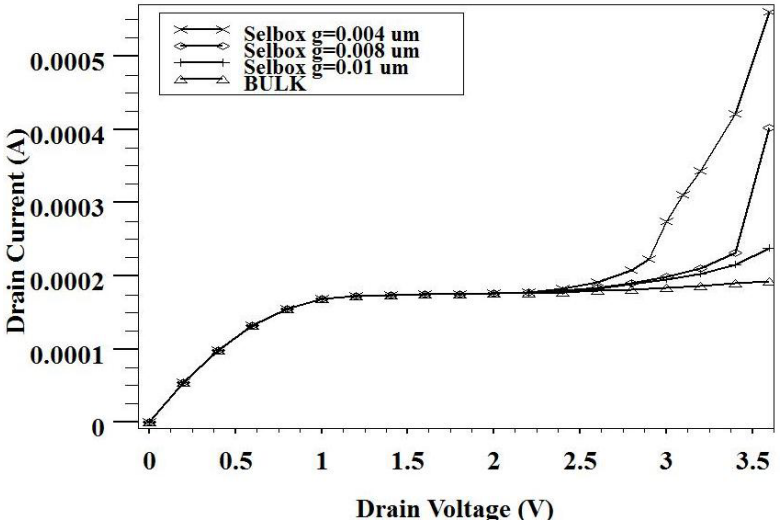

Figure 3.6: Simulation of Drain Current (I_D) as a function of Drain Voltage (V_{DS}) for SelBox structure with varying gap length (g)

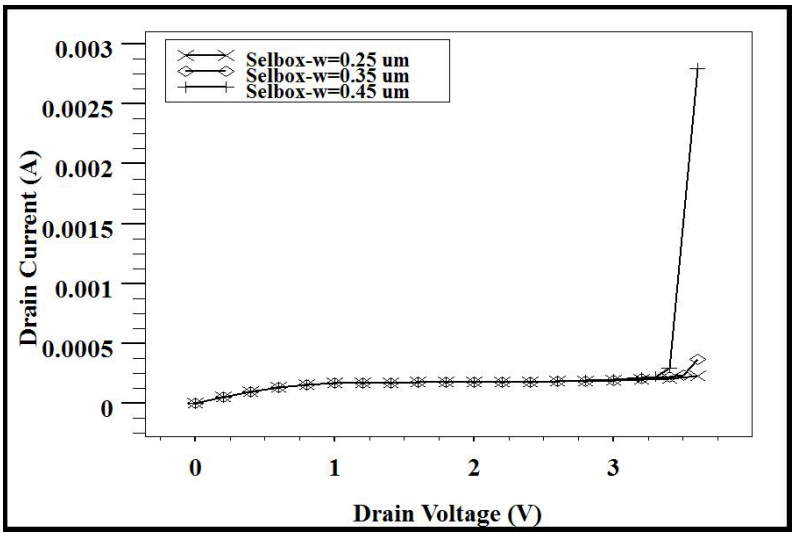

Figure 3.7: Simulation of Drain Current (I_D) as a function of Drain Voltage (V_{DS}) for SelBox structure with varying gap width (w)

It is found that the kink voltage have a significant dependence with respect to the thickness of the buried oxide. The kink can also be effectively reduced with a small gap in the buried oxide. Figure 3.7 gives the variation of kink

voltage with buried oxide for a fixed gap length of 0.009μm. In this figure, the back oxide thickness is varied from 0.25μm to 0.45μm for a fixed gap length of 0.009μm. Keeping the gap length constant, variation in the buried oxide thickness (w) gives a change in the kink voltage. As can be seen from the figure, increase in the back oxide thickness for a fixed gap length, kink occurs at a lower drain voltage. However, with reduced back oxide thickness kink occurs at a higher drain voltage and hence the kink voltage will be higher. Therefore, a selbox device with thinner back oxide thickness is more likely to behave as bulk MOSFET and is less susceptible to the kink effect.

However, the kink effect can be minimized up to a certain extent using a dual insulator below the gate electrode while preserving the necessary advantages of the SOI device at the same time. The structure of PD-SOI device using a dual insulator has been shown in Figure 3.3. The two insulators having the permittivity of 3.9 and 20 respectively are taken in the ratio of 1:1. The simulated electrical output characteristics of PD-SOI device using dual insulator is illustrated in Figure 3.8. In this figure, a comparison has been made between the output characteristics of PD-SOI device using single and dual insulator. From the figure it can be seen that in simple PD-SOI the onset of kink takes place at a kink voltage of around 1V for a gate to source voltage of 2.2V while in PD-SOI using dual insulator (DI) the kink occurs at a higher value of drain voltage for the same value of V_{GS}.

The influence of gate oxide thickness (t_{ox}) on drain current has also been analyzed. It is found that the scaling of gate oxide thickness is desirable for better drain current. Therefore, it is feasible to consider the effect of oxide thickness variation on the device performance. Figure 3.9 illustrates the output characteristics of PD-SOI device at different oxide thickness the structure of which is shown previously in Figure 3.1. From Figure 3.9, it can be analyzed that at shorter gate oxide thickness, the drain saturation current increases strongly. Thinner gate oxide thickness leads to higher drain currents and a better pinch-off voltage. Therefore, the PD-SOI device with

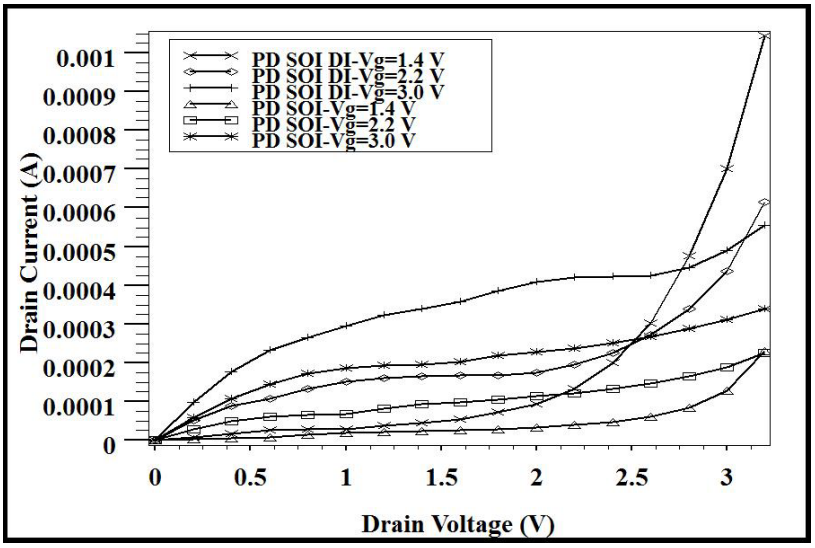

Figure 3.8: Simulation of Drain Current (I_D) as a function of Drain Voltage (V_{DS}) for PD-SOI MOSFET with Dual Insulator (DI)

the lowest possible oxide thickness leads to C_{ox} increasing and consequently to threshold voltage is decreasing. This leads to increase in drain current and less susceptance to kink phenomenon. Hence we can then conclude that gate oxide thickness has a very big effect on the threshold voltage.

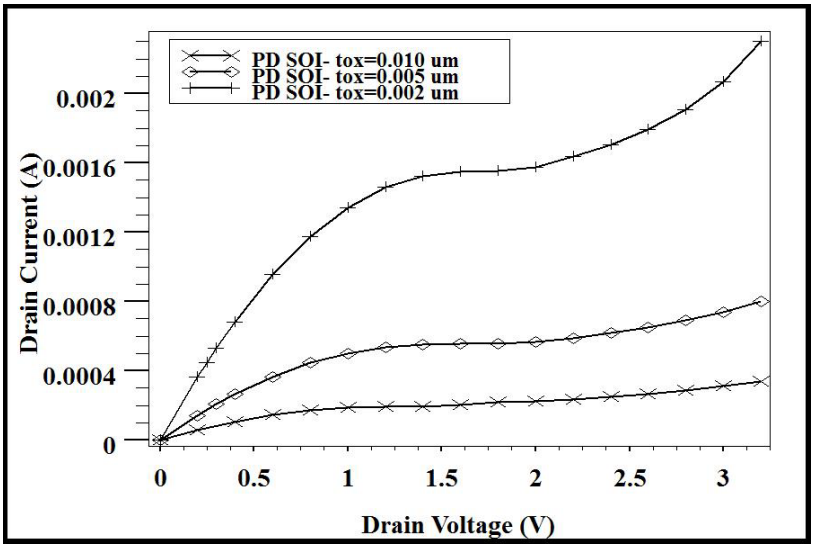

Figure 3.9: Simulation of Drain Current (I_D) as a function of Drain Voltage (V_{DS}) for PD-SOI MOSFET with varying gate oxide thickness (t_{ox})

3.5 Summary

The SOI MOSFETs according to the International Technology Roadmap for Semiconductors allow reducing short channel effects that appears under 50 nm node. In order to study these new structures numerical simulations are carried out. PD-SOI MOSFET devices exhibit nonlinearities due to the occurrence of kink in the output current voltage characteristics. The selbox structure is used to eliminate the kink in the output characteristic of a PD-SOI MOSFET device. Simulation of PD-SOI and selbox structures is carried out using Atlas Silvaco software. Variations of these different structures parameters have been carried out to study their effect on the device performance. The Selbox device offers several advantages over the bulk and PD-SOI MOSFET devices. In this chapter, it has been verified that the kink can be suppressed using a selbox device in the output characteristic of PD-SOI devices. However, the selbox device has its limitations too that is with increasing gap length the device tends to behave more like bulk MOSFET and tends to lose the associated advantages of SOI. In this chapter, with the use of dual insulator and varying oxide thickness keeping other parameters constant, the minimization of kink in the output characteristics of PD-SOI device has been investigated. At the end, based on the simulation results obtained using Silvaco software, the adequate parameters can be chosen allowing structure optimization with a good reduction of kink phenomenon.

Chapter 4

Analysis of DC & AC Performance of DG Junctionless(JL) MOSFETs

4.1 Introduction

Up till now all the existing transistors are based on the formation of semiconductor junctions formed by placing two semiconductor regions with opposite polarities into contact with one another. The semiconductor junctions are capable of both blocking current and allowing it to flow, which depends on the applied bias. The most common junction is the p-n junction consisting of a contact between a p-type silicon, rich in holes, and an n-type silicon, rich in electrons. Other types of junctions include metal-silicon 'Schottky' junction and the heterojunction, which is a p-n junction consisting of two different semiconductor materials. The bipolar junction transistor(BJT) and metal-oxide-semiconductor field-effect transistor(MOSFET) comprises two p-n junctions. The junction field-effect transistor(JFET) has only one p-n junction and the metal-semiconductor field-effect transistor(MESFET) consists of a Schottky junction [42].

As the distance between junctions in modern devices drops below 10 nm, extraordinarily high doping concentration gradients become necessary. Because of the laws of diffusion and statistical nature of the distribution of dopant atoms, such junctions encounter an increasingly difficult fabrication

challenge for the semiconductor industry. One such parameter limiting the scaling is the abruptness of source/drain(S/D) junctions as it impacts short channel effects and parasitic series resistance. To overcome the technological difficulties in the formation of ultra-steep S/D profiles, the concept of the Junctionless(JL) MOS transistor in silicon-on-insulator(SOI) and bulk technologies have recently been reported and extensively investigated as an alternative device as shown in the Figure 4.1 [8]. As the channel doping is the same as that of the S/D regions in JL devices, the need for steep S/D profile is alleviated. JL MOSFETs are different from accumulation mode devices as the channel region of accumulation-mode MOSFETs is lightly doped and, therefore, has a high resistance. A large gate voltage must be applied to create an accumulation layer and carriers are confined to a very thin layer 'squeezed' along the silicon/gate oxide interface. In a JL MOSFET, the channel region is neutral in the centre of the nanowire and, because the carriers are located in neutral silicon (that is, not depleted silicon), they see a zero electric field in the directions perpendicular to the current flow.

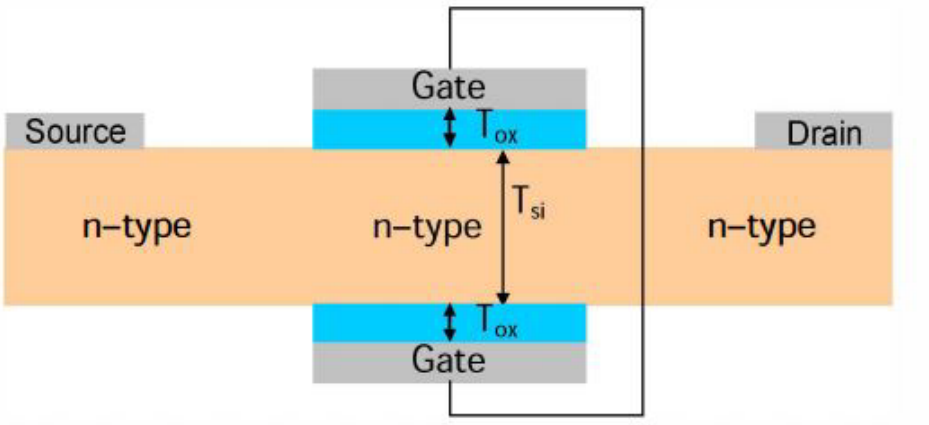

Figure 4.1: Schematic diagram of Double Gate(DG) JL MOSFET.

Junctionless MOSFETs in principle is immune to many of the challenges related to the formation of source/drain junctions and hence presents a very promising candidate for future decananometer applications. In addition, short channel effects (SCEs) are more effectively suppressed in comparison to

their counterpart enclosing conventional MOSFETs. Also the JL MOSFETs have extremely low leakage current and simple fabrication process and are less susceptible to SCEs when compared with classical inversion-mode devices. However, the high doping concentration in the channel reduces carrier mobility which results in lower drive current and transconductance (G_m) of JL MOSFETs [43]. DG-JL-MOSFETs have basically the same structure as standard DG-FETs. However, in the examined JL transistor, its channel, its source, and its drain have a homogenous doping polarity and a uniform doping concentration. The operating principle of an n-channel DG-JL-FETs is different from that of a standard n-channel conventional DG-MOSFETs.

4.2 Device Structures

Both double-gate(DG) junctionless and conventional nMOSFETs are simulated. The simulations were performed at gate lengths(L_g) of 30nm, 50nm and 100nm respectively. For comparison with junctionless nMOSFET, conventional p-n junction source/drain nMOSFETs with similar geometrical parameters are also performed. The physical gate length(L_g) is kept to be 50nm unless otherwise stated. Detailed geometrical parameters can be found from the Figure 4.1 for DG junctionless MOSFET. The simulated DG junctionless and conventional nMOSFETs are shown in the Figure 4.2.

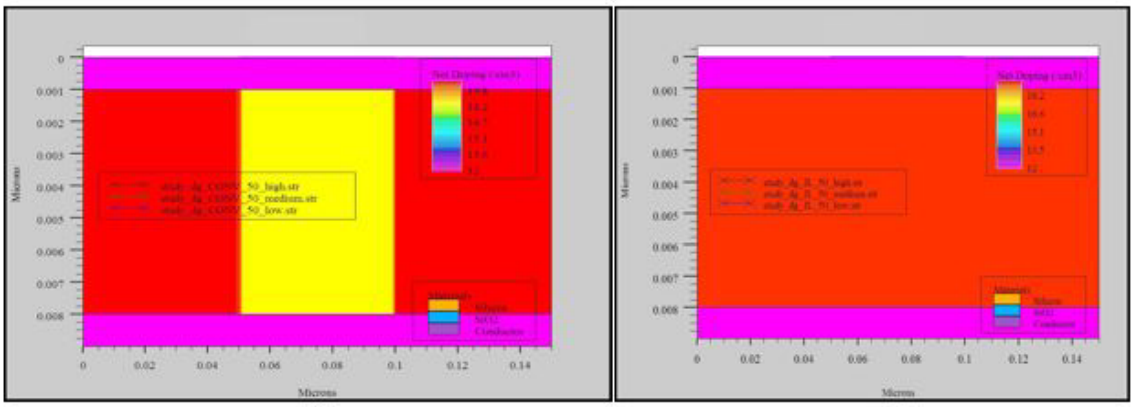

Figure 4.2: Simulated Structures of DG Conventional & Junctionless nMOSFETs.

In order to achieve comparable threshold voltage(V_T) values, the work function of the simulated metal gates for junctionless and conventional nMOSFETs are set to be φ_{m1}=4.97eV and φ_{m2}=4.8eV respectively [44] as shown in Figure 4.1. As shown in Table 4.1, parameters including gate oxide thickness(T_{ox}), channel doping concentration, gate length(L_g) and silicon channel thickness(T_{Si}) are varied in order to evaluate their effects on the variability of the simulated devices. The values in the middle of the Table 4.1 represents the default settings for the simulated transistors.

Table 4.1: Parameters for the simulated Double-Gate nMOSFETs

	Channel Doping(cm^{-3})	*Channel Length*(L_g)(nm)	*GateOxide Thickness*(T_{ox})(nm)	*S_iChannel Thickness*(T_{Si})(nm)
Junctionless	1.1e19	100	3	8
	1.0e19	50	2	7
	0.9e19	30	1	6
Conventional	2.20e18	100	3	8
	2.00e18	50	2	7
	1.80e18	30	1	6

Table 4.2: V_T and SS of the simulated Double-Gate junctionless and Conventional nMOSFETs with varied parameters shown in Table 4.1

		Channel Doping (cm^{-3})	*Channel Length* (L_g)	*Oxide Thickness* (T_{ox})	*S_iChannel Thickness* (T_{Si})
Junctionless	$V_T(V)$	0.36	0.43	0.10	0.32
		0.37	0.38	0.21	0.37
		0.40	0.36	0.31	0.40
	$SS(mV/dec)$	61.02	61.04	70.20	62.00
		60.01	60.55	61.73	60.80
		60.01	61.30	60.10	60.80
Conventional	$V_T(V)$	0.60	0.62	0.63	0.60
		0.59	0.59	0.62	0.59
		0.59	0.57	0.60	0.59
	$SS(mV/dec)$	72.70	71.20	72.8	74.7
		72.90	72.80	72.8	72.8
		72.80	75.30	72.8	71.4

Table 4.3: DIBL values for the simulated Double-Gate Junctionless and Conventional nMOSFETs with varying Gate length(L_g)

	$Channel\ Length(L_g)nm$	$DIBL\ (mV/V)$
$Junctionless$	100	51.96
	50	102.78
	30	195.2
$Conventional$	100	67.8
	50	38.66
	30	63.72

4.3 Simulation

Atlas Silvaco software package is used to construct the various device structures and perform the relevant simulations corresponding to different device structures. Both the double-gate(DG) junctionalless and conventional inversion-mode nMOSFETs are simulated. The models activated in the simulation comprises the inversion-layer Lombardi constant voltage and temperature (CVT) mobility model that takes into account the effect of parallel and perpendicular fields, along with doping and temperature-dependent parts of the mobility. The Shockley-Read-Hall(SRH) and Auger recombination models for minority carriers'combination have been used. The Fermi-Dirac carrier statistics, along with standard recombination models is used in the simulation. Furthermore, we choose Gummel's method (or the decoupled method), along with Newton's method (or the fully coupled method), to solve the equations included in the CVT model. Therefore, all the simulated MOSFET structures use the same un-calibrated mobility models in order to make reasonable and straightforward comparison among different devices. As a result, the resultant absolute drain current values may differ from other simulation and experimental results.

4.4 Results and Discussion

Table 4.2 summarizes the corresponding V_T and SS values for the simulated Double-Gate conventional and junctionless nMOSFETs with respect to the

parameters listed in Table 4.1. These values assist in evaluating and comparing between conventional and junctionless MOSFETs in a double gate environment.

4.4.1 DC Characteristics

In Figure 4.3, $I_D - V_{GS}$ transfer characteristics on linear scale for double gate (DG) junctionless and conventional MOSFETs with different gate lengths is outlined. The $I_D - V_{GS}$ curve of the junctionless DG-MOSFET is similar to that of the conventional DG MOSFETs. However, the drain current(I_D) of conventional MOSFETs is much higher than that of the junctionless MOSFET at the same gate overdrive($V_{GS} - V_T$). Figure 4.4 shows the $I_D - V_{GS}$ transfer characteristics for double gate (DG) junctionless MOSFET with reference to the current shown in the Figure 4.3. As can be seen from Figure 4.4, JL transistors show a relatively small change in V_T and subthreshold slope (SS), indicating a reasonable control of the short channel effects compared to conventional DG-MOSFETs.

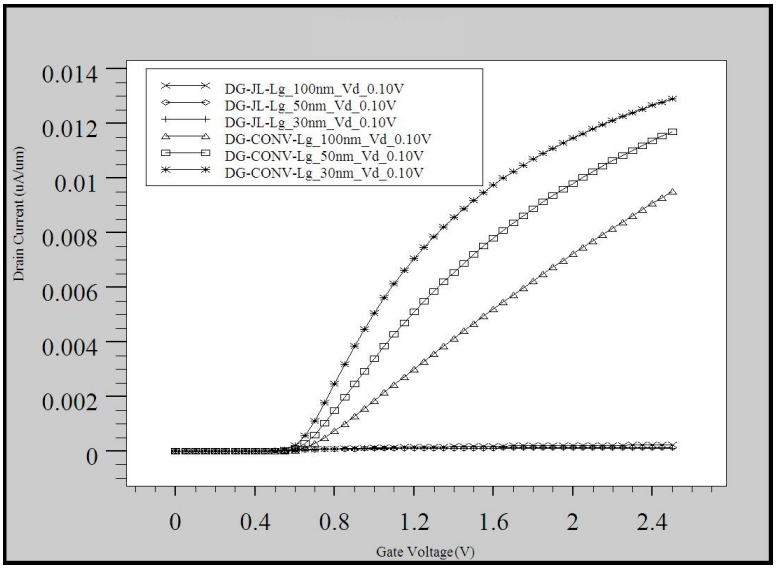

Figure 4.3: $I_D - V_{GS}$ characteristics for the Double-Gate Junctionless & Conventional nMOSFETs with various gate lengths(L_g) at V_D=0.1V.

The main reason for low driving current in case of junctionless transistors is mainly due to the degraded electron mobility because of the unavoidable

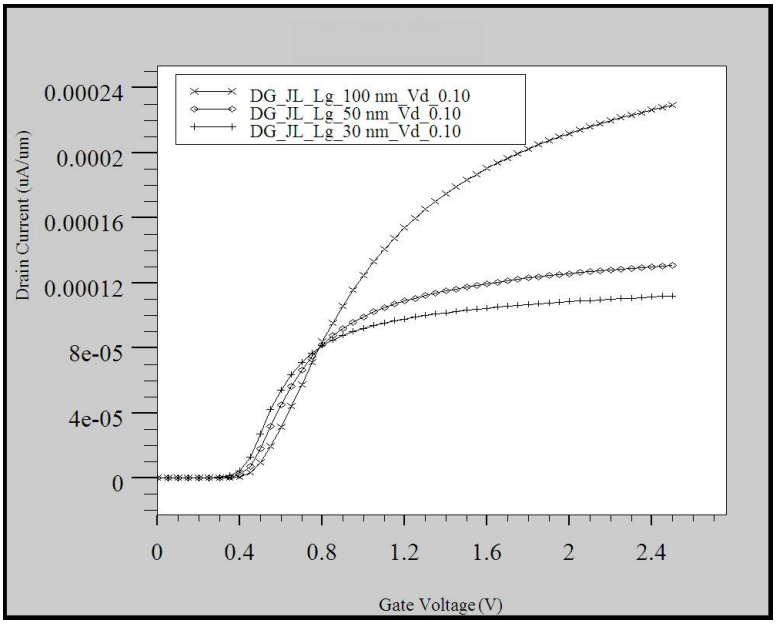

Figure 4.4: $I_D - V_{GS}$ characteristics for the Double-Gate Junctionless nMOSFETs with various gate lengths(L_g) at V_D=0.1V.

high channel doping concentration. The drift velocity of electrons along the channel is linearly related to the electron mobility. The Figure 4.5 clearly represents the difference in electron velocity along the lateral position between conventional and junctionless DG-MOSFETs indicating very low values of drain current in junctionless transistor compared to conventional transistors.

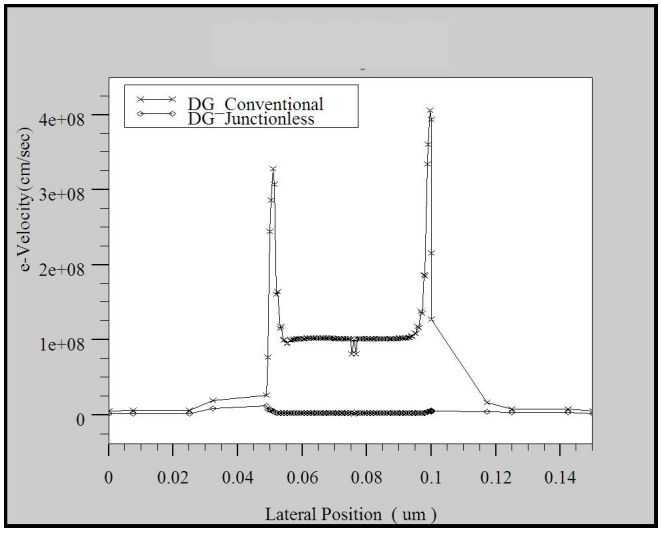

Figure 4.5: Electron Velocity along the channel position for the Double-Gate Junctionless & Conventional nMOSFETs at V_D=0.1V.

Consequently, as shown in Figure 4.6, the transconductance(G_m) of the junctionless nMOSFET is also significantly lower than that of the conventional DG-MOSFET for the same gate overdrive(V_{GS}-V_T). Figure 4.7 represents the transconductance(G_m) of the junctionless transistor with reference to the G_m shown in Figure 4.6. Interestingly, a slower degradation of transconductance with V_{GS}-V_T is observed for the junctionless transistor.

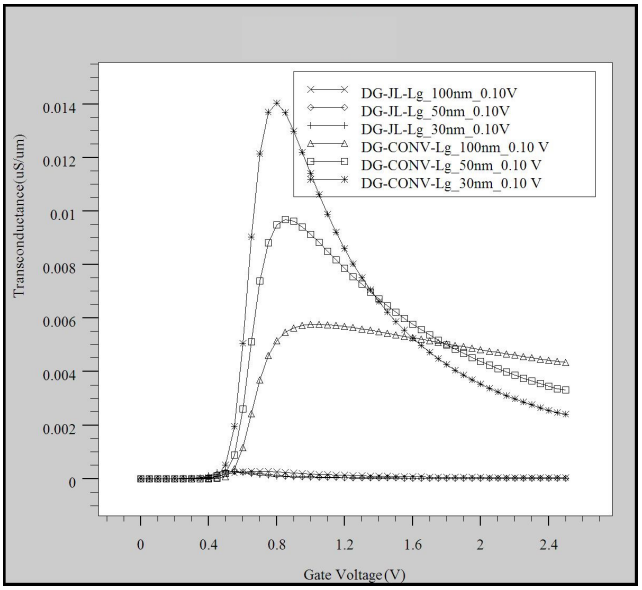

Figure 4.6: Transconductances(G_m) for the Double-Gate Junctionless & Conventional nMOSFETs at V_D=0.1V.

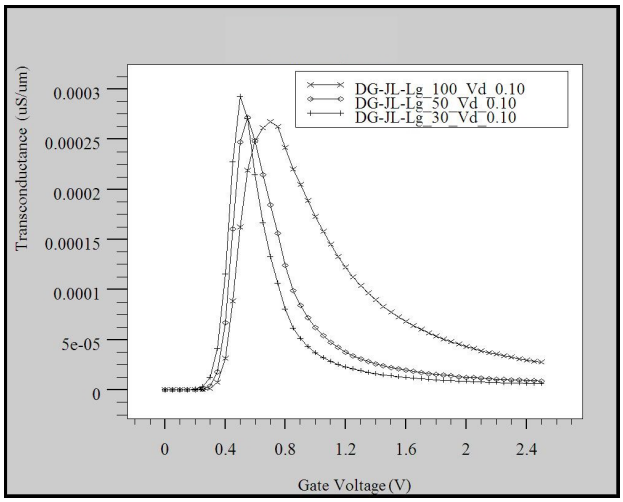

Figure 4.7: Transconductances(G_m) for the Double-Gate Junctionless nMOSFETs at V_D=0.1V.

Junctionless MOSFETs exhibits slower degradation of G_m compared to conventional MOSFET which can be well explained by the fact that the reduction in mobility with gate voltage is much less pronounced in junctionless transistor compared with the conventional transistor as a consequence of the lower electric field perpendicular to the current flow as shown in the Figure 4.8.

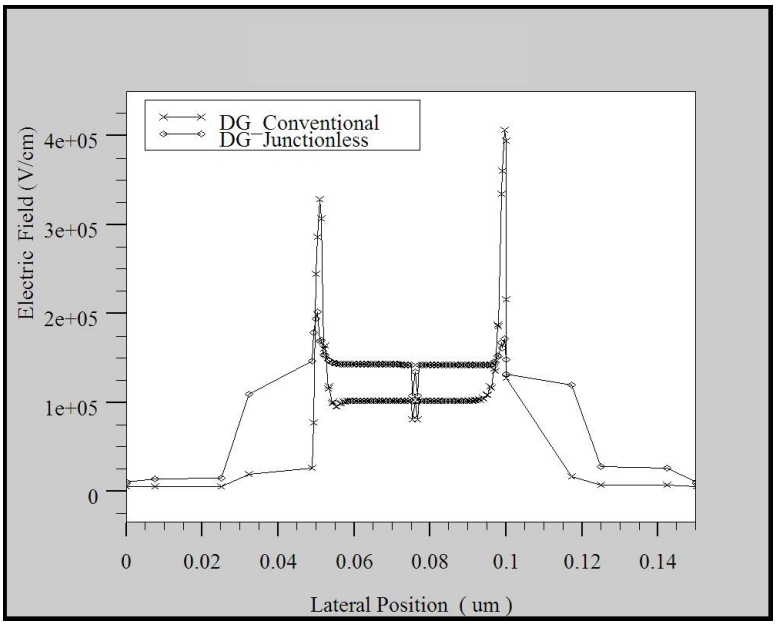

Figure 4.8: Electric Field for the Double-Gate Junctionless & Conventional nMOSFETs at V_D=0.1V.

The $I_D - V_{GS}$ transfer characteristics on linear scale for double gate (DG) junctionless and conventional MOSFETs with different channel dopings levels depicted in Table 4.1 is shown in the Figure 4.9. As it was expected, the conventional MOSFETs shows very little change in the $I_D - V_{GS}$ characteristics as a result of the low channel doping level and an ultra-thin S_i channel compared to junctionaless nMOSFETs. However, a high sensitivity of V_T to the channel doping level is observed for the junctionless nMOSFETs as shown in the Figure 4.10. The Figure 4.10 represents the drain current in junctionless transistors with various channel doping levels with reference to the drive current for junctionless nMOSFETs shown in the Figure 4.9 .

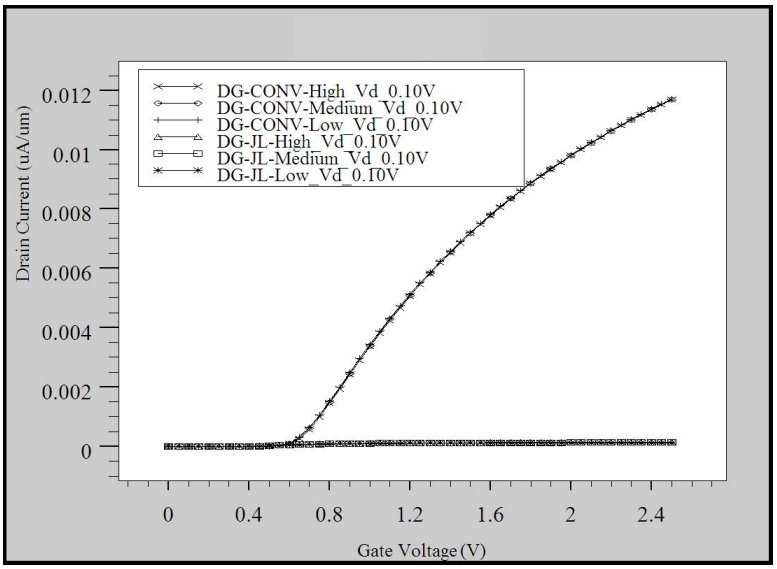

Figure 4.9: $I_D - V_{GS}$ characteristics for the Double-Gate Junctionless & Conventional nMOSFETs with various channel doping levels at V_D=0.1V.

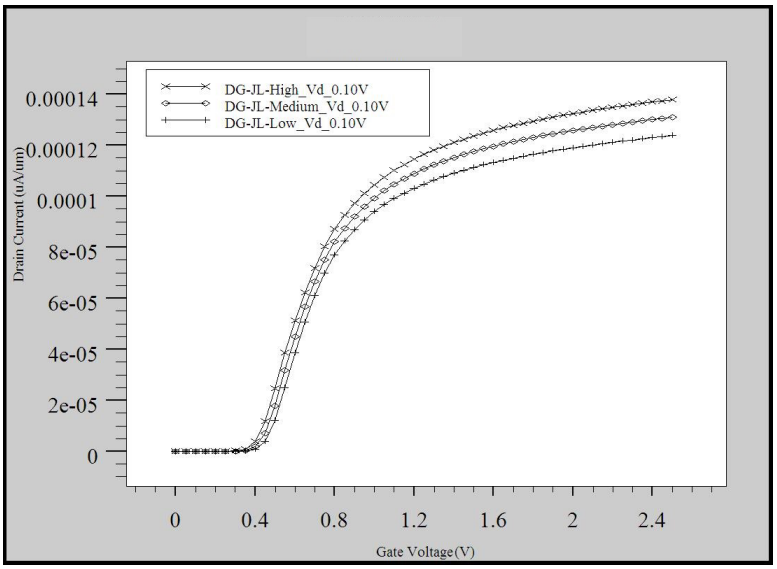

Figure 4.10: $I_D - V_{GS}$ characteristics for the Double-Gate Junctionless nMOSFETs with various channel doping levels at V_D=0.1V.

The $I_D - V_{GS}$ transfer characteristics curve for double gate (DG) junctionless and conventional MOSFETs with different gate oxide thickness(T_{ox}) as depicted in Table 4.1 is shown in the Figure 4.11. As can be seen from Table 4.2 and Figure 4.11, the conventional MOSFET do not show much sensitivity of V_T to variations of gate oxide thickness though their I_D at higher

V_{GS}-V_T seems to be highly impacted. Figure 4.12 represents the drain current in junctionless transistors with various gate oxide thickness(T_{ox}) with reference to the drive current for junctionless nMOSFETs shown in the Figure 4.11. From the Figure 4.12, it is clearly visible that compared to conventional MOSFETs, the junctionless MOSFETs exhibits a much higher sensitivity of V_T to variations of gate oxide thickness. However, their I_D at higher V_{GS}-V_T seems to be less impacted compared to conventional MOSFETs.

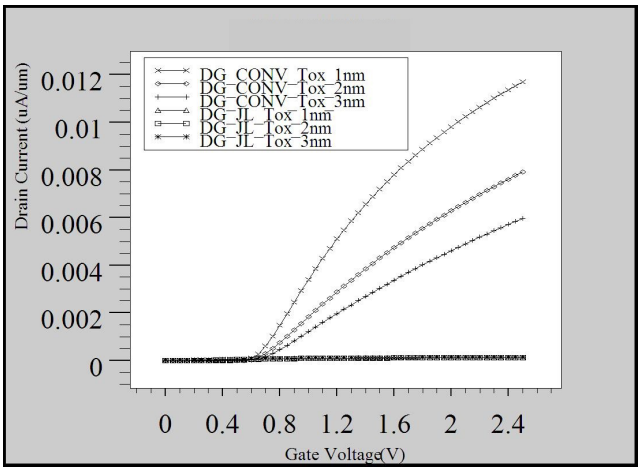

Figure 4.11: $I_D - V_{GS}$ characteristics for the Double-Gate Junctionless & Conventional nMOSFETs with various gate oxide thickness(T_{ox}) at V_D=0.1V.

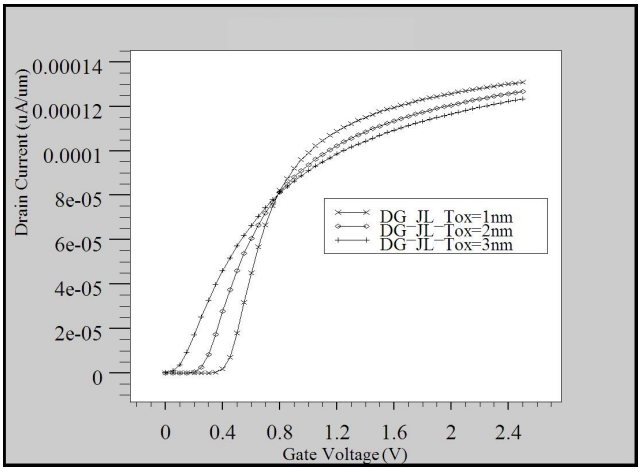

Figure 4.12: $I_D - V_{GS}$ characteristics for the Double-Gate Junctionless nMOSFET with various gate oxide thickness(T_{ox}) at V_D=0.1V.

The $I_D - V_{GS}$ transfer characteristics curve for double gate (DG) junctionless and conventional MOSFETs with different silicon channel thickness(T_{Si}) as depicted in Table 4.1 is shown in the Figure 4.13. Figure 4.14 represents the drain current in junctionless transistors with various silicon channel thickness(T_{Si}) with reference to the drive current for junctionless nMOSFETs shown in the Figure 4.13. As can be seen from Table 4.2 and Figures 4.13 and 4.14 respectively, the V_T and SS of the conventional nMOSFETs are found to be insensitive to the variations of the Si channel thickness. However, a large variation of V_T is still observable for the junctionless nMOSFETs as the Si channel thickness varies. A change of around 50mV in V_T can be found when the Si channel thickness varies by 1 nm.

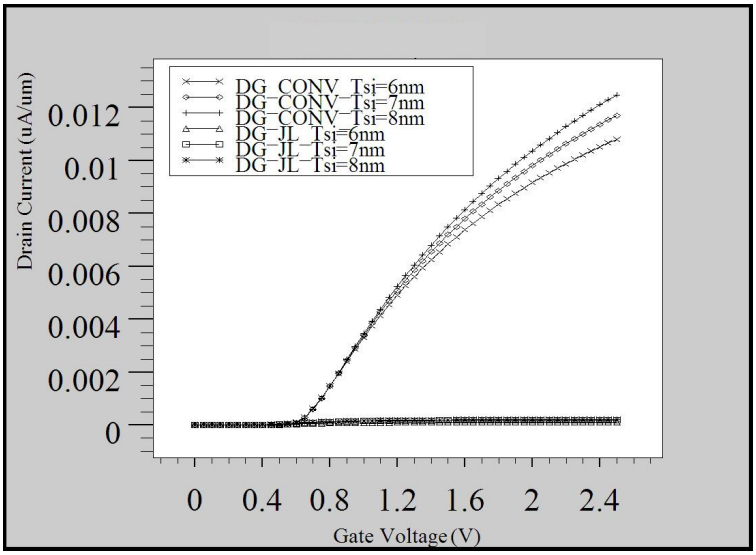

Figure 4.13: $I_D - V_{GS}$ characteristics for the Double-Gate Junctionless & Conventional nMOSFETs with various silicon channel thickness(T_{si}) at V_D=0.1V.

4.4.2 AC Characteristics

The simulated gate-to-source(C_{gs}) and gate-to-drain(C_{gd}) capacitances of the conventional and junctionless nMOSFETs are depicted in the Figure 4.15 and Figure 4.16 respectively. Interestingly, C_{gs} of the junctionless nMOSFET is clearly quite smaller than that of the conventional nMOSFET for the same V_{GS}. However, the peak value of C_{gs} of the junctionless nMOSFET occurs

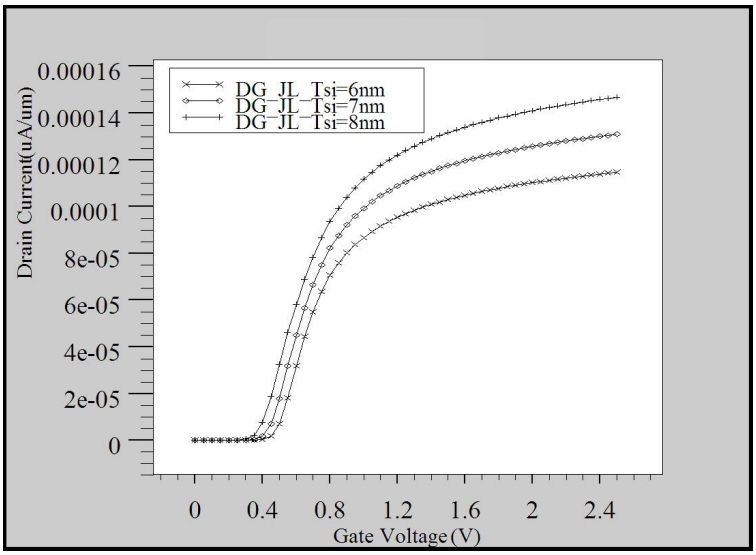

Figure 4.14: $I_D - V_{GS}$ characteristics for the Double-Gate Junctionless nMOSFET with various silicon channel thickness(T_{si}) at V_D=0.1V.

at the same gate overdrive($V_{GS} - V_T$). Also as can be seen from the Figure 4.16, the C_{gd} of the junctionless nMOSFET is also lower than that of the conventional nMOSFET for V_{GS}<1.4V.

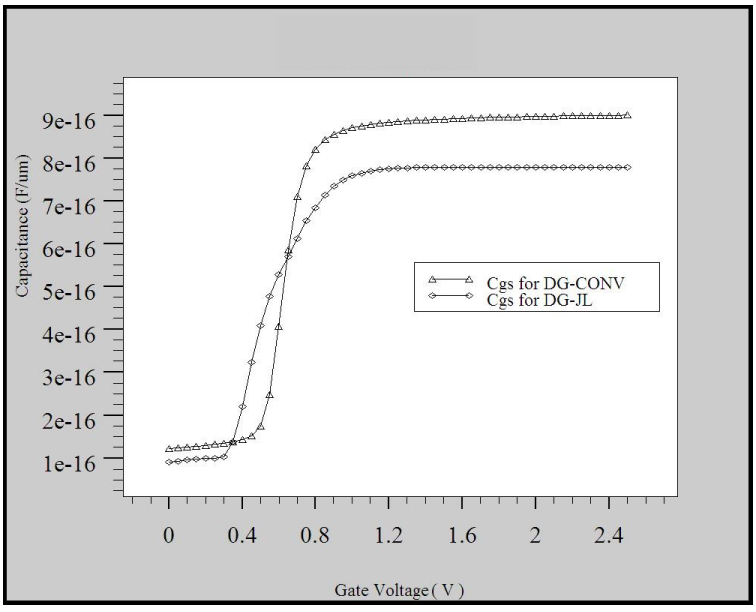

Figure 4.15: Simulated C_{gs} for Double-Gate Junctionless & Conventional nMOSFETs.

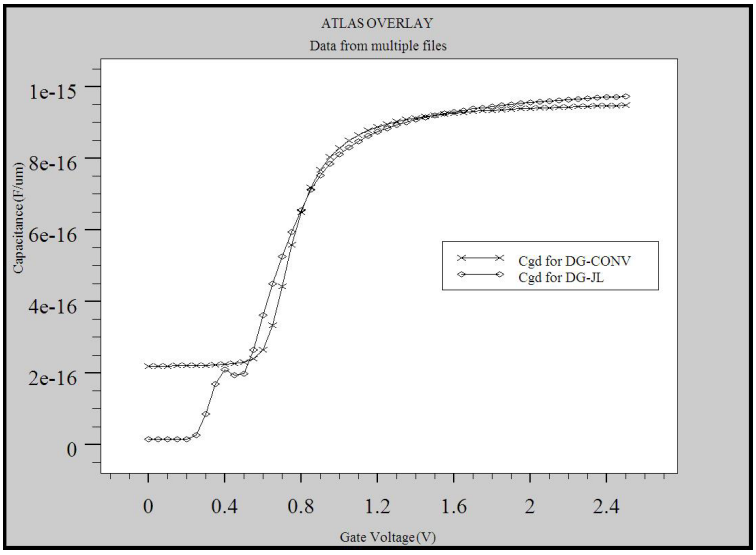

Figure 4.16: Simulated C_{gd} for Double-Gate Junctionless & Conventional nMOSFETs.

4.5 Summary

Single-gate is unable to properly turn off the channel at the off-state for the junctionless MOSFETs that usually require a uniform channel doping of no less than $2 \times 10^{20} cm^{-3}$. Double or multi-gate structures are necessary for junctionless MOSFETs to suppress the off-state source-to-drain leakage current even for an extremely thin Si channel at 7 nm thickness. In comparison with conventional double-gate MOSFETs, double-gate junctionless MOSFETs with a gate length of 50 nm exhibit significantly lower drive current and peak transconductance, but a comparable low subthreshold slope around 62 mV/dec. For the junctionless MOSFETs, their V_T is significantly more sensitive to variations of Si channel thickness and channel doping concentration. Preferably, junctionless MOSFETs demonstrate significantly lower gate capacitances at saturation and a slower degradation of transconductance with a gate overdrive. With its unique advantage of elimination of the source/drain junctions, junctionless MOSFETs could be a promising candidate for future sub-10 nm technologies where a 3-D gate structure is most likely expected.

Chapter 5

Conclusion & Scope for Future Work

5.1 Conclusions

As dimensional scaling of CMOS transistors is reaching its fundamental limits, various researches have been actively carried out to find an alternative way to continue to follow Moores law. Among these efforts, the SOI MOSFETs according to ITRS allow reducing short channel effects that appears under 50nm node. PD-SOI MOSFET devices exhibit nonlinearities due to the occurrence of kink in the output current voltage characteristics. The selbox structure is used to eliminate the kink in the output characteristic of a PD-SOI MOSFET device. The Selbox device offers several advantages over the bulk and PD-SOI MOSFET devices. It has been verified that the kink can be suppressed using a selbox device in the output characteristic of PD-SOI devices. In addition, in order to mitigate the difficulties in fabrication of ultra thin devices for the semiconductor industry, resulting from scaling of gate length in MOSFET, a new device structure called junctionless(JL) transistors have recently been reported as an alternative device. Junctionless MOSFETs using double or multi gate structures are necessary to suppress the off-state source-to-drain leakage current even for an extremely thin channel Si at 7 nm thickness. Preferably, junctionless MOSFETs demonstrate significantly lower gate capacitances at saturation and a slower degradation of transcon-

ductance with a gate overdrive. With its unique advantages, junctionless MOSFETs could be a promising candidate for future sub-10 nm technologies where a 3-D gate structure is most likely expected.

5.2 Scope for Future Work

The research work carried out in this thesis has proved the ability of reducing short channel effects in PD-SOI devices and the efficiency of multi-gate junctionless transistors over the conventional multi-gate structures. The same framework can now be used to improve the understanding of existing structures and develop new structures for high performance, low power and high speed applications that can be of interests for certain applicative scenarios. The results presented are expected to provide incentive for further experimental exploration. Some important directions for further research in the following areas can be:

1. Optimization of Device parameters using some efficient algorithms techniques.
2. Possible fabrication of the different device structures considered.
3. Comparing the simulated results with the experimental results.

5.3 List of Publications

1. K P Pradhan, S K Mohapatra, **P K Agarwal**, P K Sahu, D K Behera, Jyotismita Mishra, "Symmetric DG-MOSFET with Gate and Channel Engineering: A 2-D Simulation Study", *Microelectronics and Solid State Electronics (Scientific & Academic Publishing)*, vol.2, issue.1, pp.1-9, February 2013.

2. **P K Agarwal**, K P Pradhan, S K Mohapatra, P K Sahu, "Insulating layer parameters are still in reduction of kink", *IEEE International Conference on Engineering*, Ahmedabad, pp.1-4, December 6-8, 2012.

3. K P Pradhan, **P K Agarwal**, P K Sahu, S K Mohapatra, "Role of high-k materials in Nanoscale TM-DG MOSFET: A simulation study", *First National Conference on Recent Developments in Electronics (NCRDE)*, New Delhi, January 18-20, 2013.

4. K P Pradhan, **P K Agarwal**, S K Mohapatra, P K Sahu, "The Impact of High-k Gate Dielectric Materials over Short Channel Parameters on Sub-100 nm MOSFET", $XVII^{th}$ *National Seminar on Ferroelectrics & Dielectrics (NSFD)*, Bhubaneswar, December 17-19, 2012.

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