STUDY AND ANALYSIS OF DIFFERENT TYPES

OF COMPARATORS

A Thesis submitted in partial fulfillment of the requirements for the degree of

Bachelor of Technology
In
Electronics and Communication Engineering

Submitted by:

Lalit Madhab Dhal (109EI0267)

&

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C E R T I F I C A T E

This is to certify that the Thesis entitled, '**Study and Analysis of different types of comparators**' submitted by **Lalit Madhab Dhal & Anshuman Pradhan** in partial fulfillment of the requirements for the award of **Bachelor of Technology Degree** in **Electronics and Communication Engineering** at the **National Institute of Technology, Rourkela** is a bonafide work carried out by them under my supervision. To the best of my knowledge and belief the matter embodied in the Thesis has not been submitted by them to any other University/Institute for the award of any Degree/Diploma.

Prof. K.K. Mahapatra

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ACKNOWLEDGEMENT

ABSTRACT

Different types of comparators are studied and the circuits are simulated in Cadence® Virtuoso Analog Design Environment using GPDK 90nm technology. The circuits are simulated with 1.8 Volt DC supply voltage. The clock has a frequency of 250 MHz. All the respective DC responses and transient responses are plotted and analyzed. Layouts of all the comparators have been done in Cadence® Virtuoso Layout XL Design Environment.

Different static and dynamic characteristics of all the comparators are studied and compared. Their advantages and disadvantages were also discussed.

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CHAPTER 1

INTRODUCTION TO COMPARATORS

1.1 INTRODUCTION

In electronics, Operational amplifier is designed to be used with negative feedback. It can be also used as comparator in open loop configuration. On the other hand, Comparator is especially designed for open loop configuration without any feedback. Hence it is the second most widely used device in electronic circuits after Opamp. Comparators are mostly used in analog-to-digital converter (ADCs). In the conversion process, first the input signal is sampled. Then the sampled signal is applied to a number of comparators to determine the digital equivalent of the analog value. Apart from that, comparators are used in peak detectors, zero crossing detectors, BLDC operating motors, switching power regulators.

DEFINITION

Comparators is the device that compares two analog voltages or currents and switches it output to indicate which one is larger.
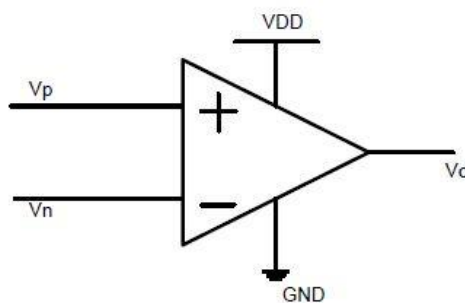
(Fig 1.1 -- Schematic of comparator)

If V_P is at a greater potential than V_P, then the output V_o of the comparator is logic 1 and when V_P is at a potential less than V_n, then the output is at logic 0.

If we apply a pulse voltage at V_P and a DC reference voltage at V_n, the output is logic 1 when the pulse amplitude is greater than the reference voltage. The figure is shown below.

(Fig 1.2 -- Voltage transfer characteristics of ideal comparator)

Thus a comparator compares two input analog value and gives binary output. In ideal case, binary signals can have two values at any point. But actually there is a transition region between the two binary states. F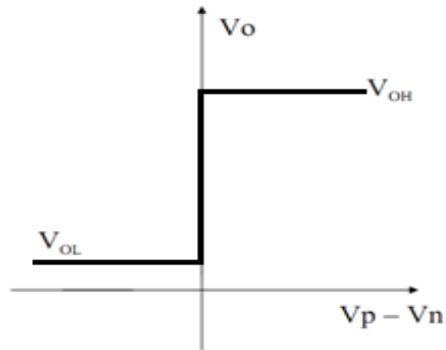or a comparator, it is important to pass quickly through that transition region. Basically comparators can be divided into two types. First is the Open loop comparators, which are nothing but OPamps. The second type is regenerative comparators. Regenerative comparators use positive feedback for the comparison of magnitude between two signals.

1.2 MOTIVATION

Nowadays, where demand for portable battery operated devices is increasing, a major importance is given towards low power methodologies for high speed applications. Also we have to minimize the power consumption by using smaller feature size processes. However when we move towards power consumption minimization, the process variations and other parameters will greatly affect the overall performance of the device. Now comparators are used in ADCs and ADCs

require less power dissipation, high speed, less delay, less offset voltage, low noise, better slew rate, less hysteresis etc. In order to achieve these specification, the building block of ADC i.e. comparator must be tightly constrained. Nowadays dynamic comparators are used in ADCs because these comparators have high speed, less power dissipation, zero static power consumption. Also back-to-back inverters are used in dynamic comparators to provide positive feedback mechanism which converts a smaller voltage difference to full scale digital level output. However parasitic node capacitance, output load capacitance limits the accuracy of such comparators.

1.3 THESIS ORGANIZATION

The thesis can be organized as follows. Chapter 2 provides the comparator characteristics. Chapter 3 provides the literature review of different types of comparators. Chapter 4 describes latched comparator in brief. Chapter 5 provides the results and simulations of different comparators studied. Chapter 6 gives the conclusion and describes the future work that can be done.

CHAPTER-2

COMPARATOR CHARACTERISTICS

In this section, we will discuss about static and dynamic characteristics of comparator.

2.1 STATIC CHARACTERISTICS

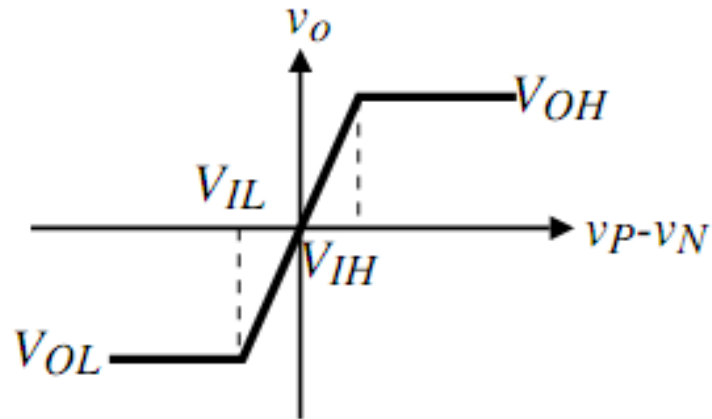The static characteristics of a comparator are

   i.   Gain

  ii.   Offset voltage

 iii.   Input resolution

 iv.   Noise

  v.   Input common mode range (ICMR)

GAIN

Gain of a comparator can be expressed as

$$\text{Gain } (A_V) = \lim_{\Delta V \to 0} \frac{V_{OH} - V_{OL}}{\Delta V}$$

Where ΔV = input voltage range

(Fig 2.1 -- First order model of a comparator)

V_{IH}= Smallest input voltage for which the output voltage is V_{OH}

V_{IL}= Largest input voltage for which the output voltage is V_{OL}

OFFSET

It can be classified into two types. 1. Systematic offset 2. Random offset. Offset in the comparators are generated due to input transistor mismatches. (Mismatch in threshold voltages and mismatch in trans-conductance parameter $\beta=\mu Cox\ W/L$)

INPUT OFFSET VOLTAGE

The input offset voltage is the voltage which must be applied between the two input terminals to balance the amplifier.

OUTPUT OFFSET VOLTAGE

The output offset voltage is defined as the dc voltage present at the output terminal of the comparator when the two input terminals are grounded.

INPUT OFFSET CURRENT

The input offset current is defined as the difference between the two separate currents entering into the input terminals of a balanced amplifier.

INPUT RESOLUTION

It is the input voltage change which is sufficient to make output swing to valid binary states.

NOISE

Noise of a comparator is modeled if the comparator were biased in the transition region. Noise leads to an uncertainty in the transition region which causes jitter.
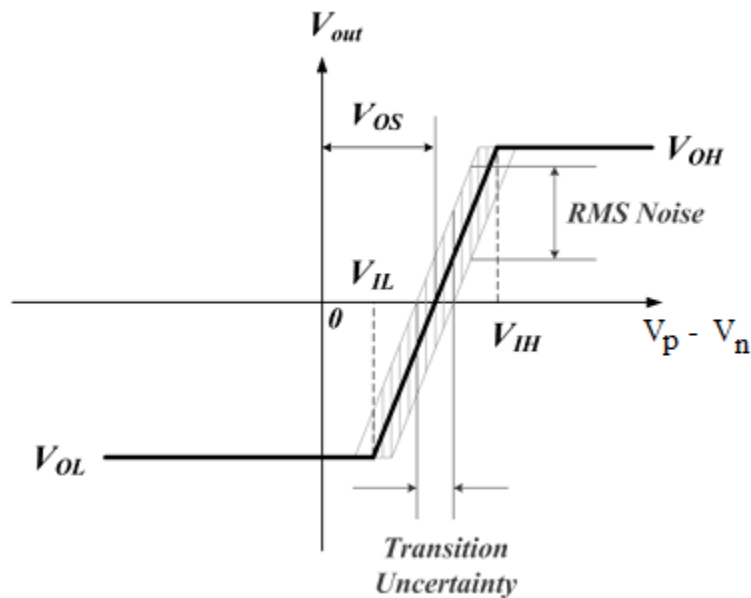
(Fig 2.2 --First order model of a comparator with input voltage and noise)

INPUT COMMON MODE RANGE

ICMR can be defined as the range of input voltage for which the comparator functions normally & meets all required specifications.

2.2 DYNAMIC CHARACTERISTICS

The dynamic characteristics of a comparator are

   i.   Propagation delay

   ii.   Slew rate

   iii. Speed

PROPAGATION DELAY

Propagation delay is defined as at how much speed the amplifier responds with applied input. Simply speaking it is the delay between output and input.
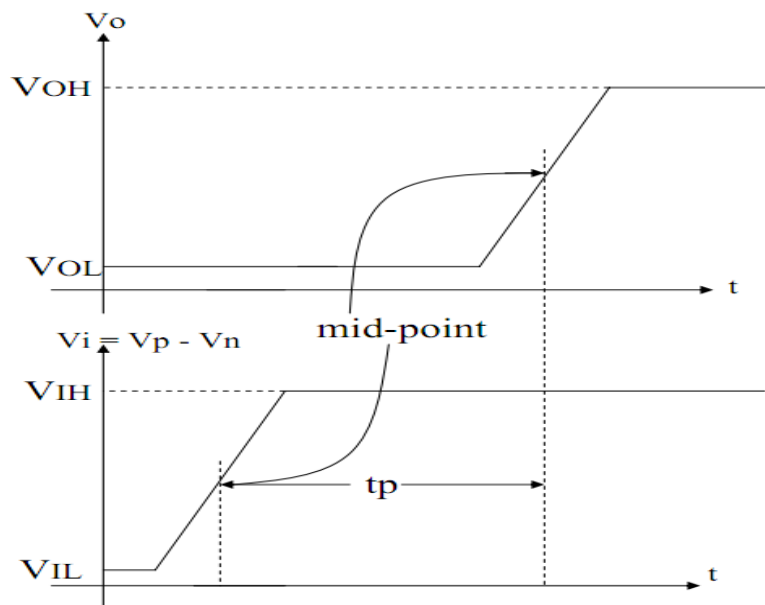
(Fig 2.3 -- Propagation delay of a comparator)

It can be calculated as

Propagation time delay= (Rising Propagation Delay time +Falling Propagation Delay Time) /2

SPEED

It is the inverse of the Propagation delay.

$$\text{Speed} = \frac{1}{propagation\ delay}$$

CHAPTER –3

LITERATURE REVIEW

In this literature review, we will discuss about various type of comparator architecture. The static and dynamic characteristics & advantages and disadvantages of pre-amplifier based comparator are analyzed.

3.1 PRE-AMPLIFIER BASED COMPARATOR

(Fig 3.1 -- Pre-amplifier based comparator)

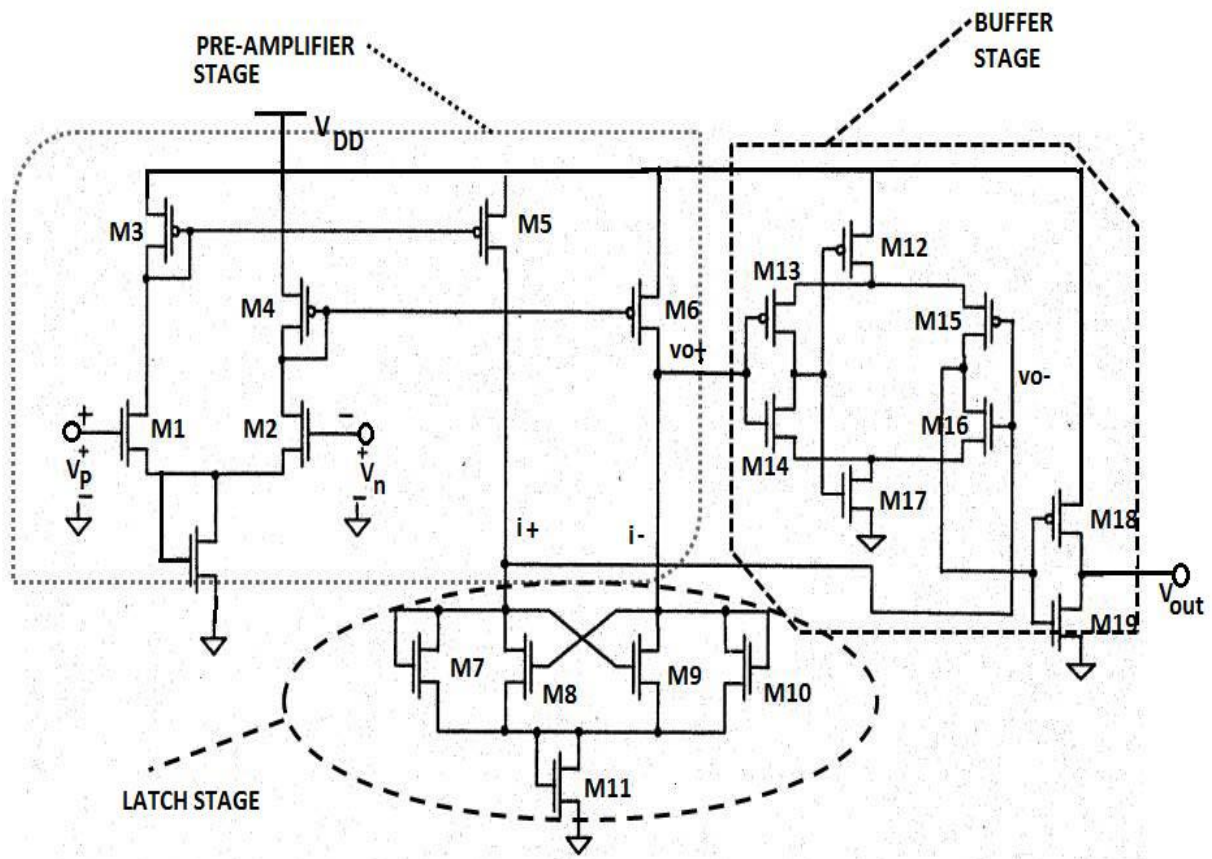The comparator consists of three stages

   i.   input preamplifier stage

  ii.   latch stage

 iii.   output buffer stage

The preamplifier stage consists a differential amplifier with active loads. The preamp stage amplifies the input signal to improve the comparator sensitivity. It increases the minimum input signal with which the comparator can make a decision and isolates the input of the comparator from switching noise (often called kickback noise) coming from the positive feedback stage. It also can reduce the input referred latch offset voltage. The sizes of Ml and M2 are set by taking into consideration the input capacitance and the diff-amp trans-conductance. The trans-conductance sets the gain of the stage, while the size of Ml and M2 mosfets determines the input capacitance of the comparator. Here $gm1 = gm2$.

The positive feedback latch stage is used to determine which of the input signals is larger and amplifies their difference. The output buffer stage consists of a self-biased differential amplifier followed by an inverter which gives the digital output. It converts the output of the latch stage to a full scale digital level output (logic 1 or logic 0). The output buffer stage should accept a differential input signal and not have slew-rate limitations.

3.2 DOUBLE-TAIL LATCH TYPE VOLTAGE SENSE AMPLIFIER

Figure 3.2 shows the schematic diagram of the Double-Tail latch type voltage sense amplifier. Double-Tail is derived from the fact that the comparator uses one tail for input stage and another tail for latching stage. It has less stacking and therefore it can operate at lower supply voltages. Large size of the Transistor M14 draws large current at latching stage which is completely independent of common mode voltages at inputs. Also small size of M1 offers lower supply voltages resulting lower offset.
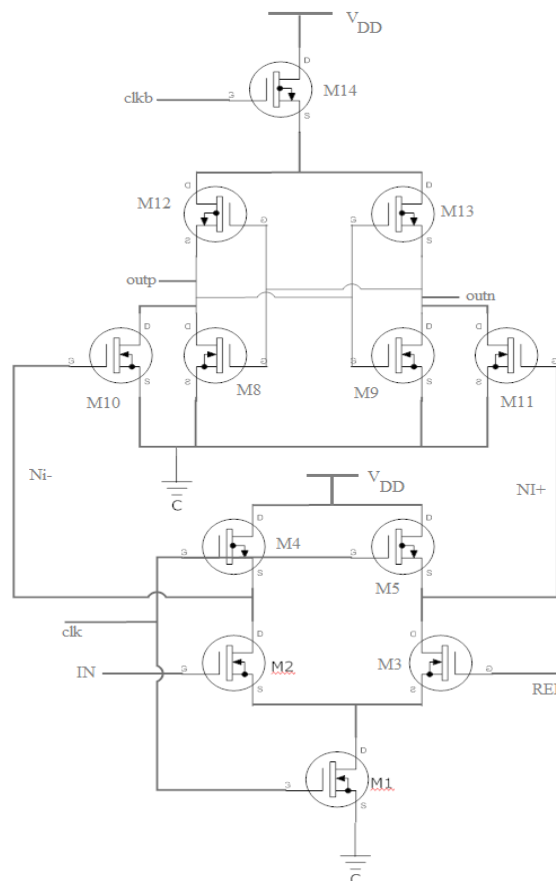
(Fig 3.2 -- Double-tail latch type voltage sense amplifier)

OPERATION

During reset phase (clk=0V), M4 and M5 charges to VDD which in turn charges Ni (regenerative nodes) nodes to VDD. Then M10 and M11 turns on and discharges output nodes to GND. During evaluation phase (clk=VDD), the transistors M1 and M14 turns ON. So Ni nodes common mode voltage decreases gradually and one input dependent differential mode voltage generates. M10 and M11 pass this differential node voltage to latch stage. The inverters start to regenerate the voltage difference as soon as the common-mode voltage at the Di nodes is no longer high enough for M10 and M11 to clamp the outputs to ground. M10 and M11 also provide additional shielding which reduces kickback noise.

DISADVANTAGES

clk and clkb requires high accuracy timing. The reason is that the latch stage has to regenerate the differential input voltage coming from input stage at very short period of time. Now if we replace the clkb with the inverter whose input is clk signal then clk has to drive heavier load in order to drive largest transistor M14 in a smallest possible delay. Now if clkb leads clk, then comparator will undergo increased power dissipation and if clkb lags clk, it results in increased delay means less speed of operation due to short circuit current path from M14 to M10/M11 through M12/M13.
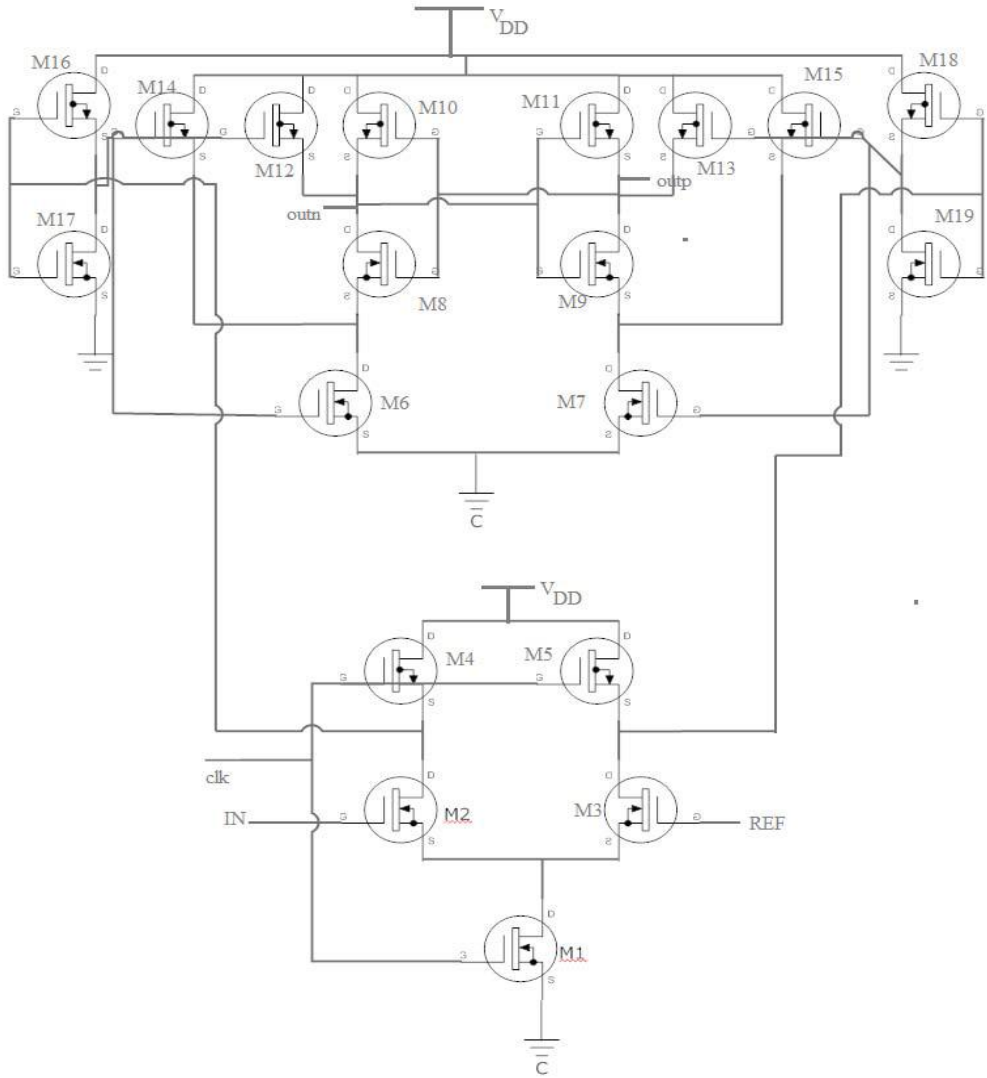
3.3 DYNAMIC COMPARATOR
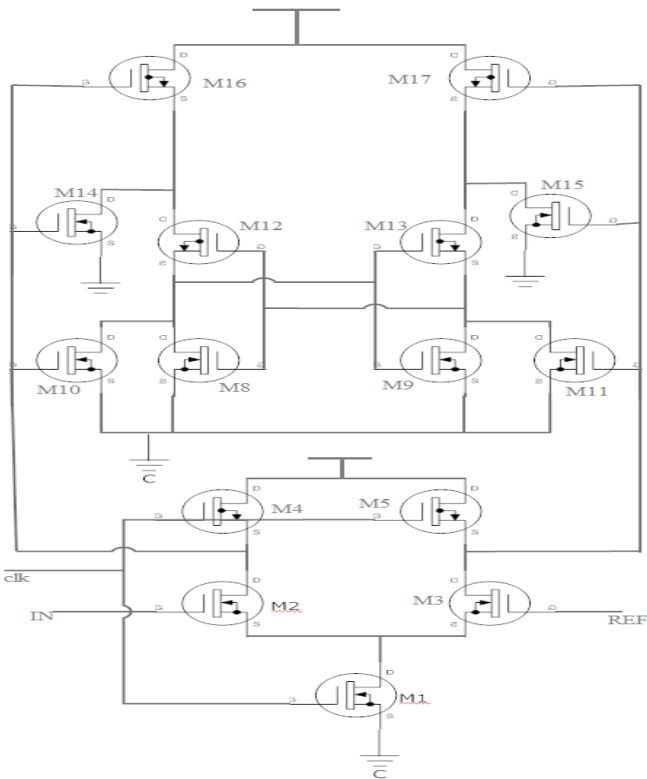
(Fig 3.3 -- Dynamic comparator)

Figure 3.3 shows the Self-Calibrating Dynamic Comparator. This comparator resolved the high accuracy timing between clk and clkb problem by replacing clkb signal with Ni nodes. But it results in increased delay because the transistor M16 and M17 use Ni node voltages as their input signal. Also due to this, the current drivability of the output node decreases. The input referred latch offset is also reduced in this circuit since the output latch stage takes load from the M10, M11 and M16, M17. Maximum drive current of the output node also decreased to half since the supply voltage VDD has been divided into two transistors.

3.4 DOUBLE TAIL DUAL RAIL DYNAMIC LATCHED COMPARATOR

(Fig 3.4 -- Double-tail dual rail dynamic latched comparator)

Figure 3.4 shows the schematic of the Double-Tail Dual-Rail Dynamic Comparator. This comparator eliminated the weakened regenerating nodes by inserting an inverter between input and output stages. This comparator shows faster operation and lesser power dissipation than the previous comparators.
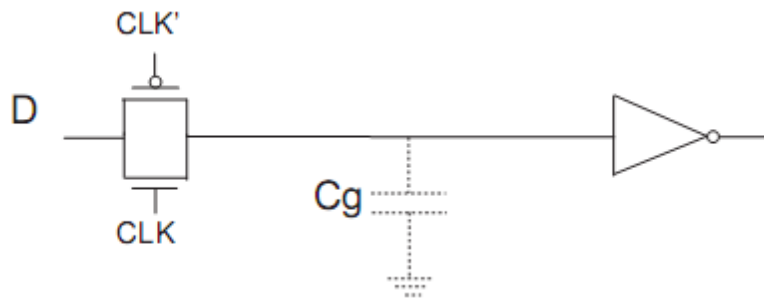
CHAPTER 4

LATCHED COMPARATORS

4.1 DYNAMIC LATCH

A dynamic latch is a memory unit that stores charge on the gate capacitance of the inverter.

Shown below is a simple dynamic latch.

A clock drives the circuit. When clk=1, the transmission gate is closed, the latch acts transparent, and hence the inverter is directly connected to the input. When clk=0, the transmission gate opens and the inverter's output is determined by the node. We must take into consideration the setup and hold times determined by the transmission to ensure proper operation of the latch i.e sufficient level of voltage is stored on the gate capacitance of the latch.

4.2 PRE-AMPLIFIER

The pre-amplifier used in the design is a simple common source differential amplifier connected with active loads. Pre-amplifier is followed by a small circuit which is used for two main functions. First it is used to avoid "kick back effect" from the latch to the input signal. Kick back is the noise detected at the input signal which is produced due to high voltage variations at the regenerative nodes of the latches and is coupled to the input through the parasitic capacitances of the transistors. The other purpose of using the kick back protection circuit is to create a charge imbalance in the latch when it switches from reset mode to the regeneration mode.

4.3 SPEED OF THE COMPARATOR

Speed of the comparator is heavily dependent on the regenerative time constant of the latch. The latch can be modeled with two inverters connected in a loop with positive feedback configuration as shown in figure
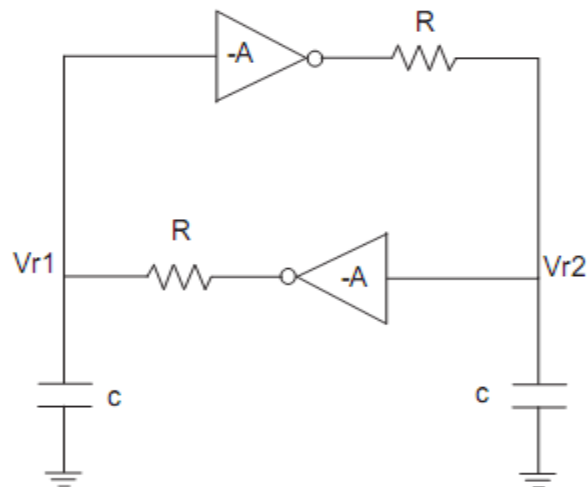
(Fig 4.1 -- Model for a comparator)

The regenerative nodes are marked 'Vr1' and 'Vr2'. These nodes convert the small voltage difference to full logic level. The time required for amplification is dependent on the initial voltage difference "V-diff" produced by the pre-amplifier in the form of slight charge disturbance during the reset phase.

The time required for regeneration is given by:

$$t_{comp} = \frac{(RC)}{A-1}\ln\left(\frac{(Vdiff)}{Vdd}\right)$$

"A" is the small signal gain of the inverters. From this equation, it can be seen that the time for comparison depends upon the time constant RC, gain of the inverter and the initial voltage difference.

CHAPTER 5

COMPARATOR ANALYSIS

Table 1: Input Specifications

Supply voltage	1.8 V
Technology	CADENCE GPDK 90nm
Clock Voltage Range	0V – 0.9V
Clock Frequency	2.5 MHz
Clock Rise Time	100 ps
Clock Fall Time	100ps
Clock Delay	1ns
Clock Pulse Width	2ns
Temperature	27 ºC
Reference Voltage	0.2V – 0.6V

Table 2: Transistor Dimension (µm)

| TRANSISTOR	3.1		3.2		3.3		3.4	
	W	L	W	L	W	L	W	L
M1	8	0.1	8	0.1	8	0.1	8	0.1
M2	4	0.1	4	0.1	4	0.1	4	0.1
M3	4	0.1	4	0.1	4	0.1	4	0.1
M4	X	X	2	0.1	2	0.1	2	0.1
M5	X	X	2	0.1	2	0.1	2	0.1
M6	X	X	X	X	2	0.1	2	0.1
M7	X	X	X	X	2	0.1	2	0.1
M8	2	0.1	2	0.1	2	0.1	2	0.1
M9	2	0.1	2	0.1	2	0.1	2	0.1
M10	2	0.1	4	0.1	4	0.1	2	0.1
M11	2	0.1	4	0.1	4	0.1	2	0.1
M12	2	0.1	2	0.1	2	0.1	4	0.1
M13	2	0.1	2	0.1	2	0.1	4	0.1
M14	4	0.1	4	0.1	4	0.1	4	0.1
M15	4	0.1	X	X	4	0.1	4	0.1
M16	X	X	0.18	0.1	4	0.1	0.18	0.1
M17	X	X	0.18	0.1	4	0.1	0.18	0.1
M18	X	X	X	X	X	X	0.18	0.1
M19	X	X	X	X	X	X	0.18	0.1

In this section the existing comparators are analyzed that were discussed in the literature review. Their advantages and disadvantages are compared in respect of their speed, delay, power dissipation and offset voltage. Cadence Virtuoso® Analog Design Environment, Virtuoso® XL Layout Editing Software are used for analyzing the circuits.

5.1 PREAMPLIFER BASED COMPARATOR

Circuit Diagram

Figure 5.1 shows the schematic (designed in Cadence) of the Preamplifier based comparator circuit. The supply voltage to this comparator is 1.8 V. Reference voltage is .5 V.
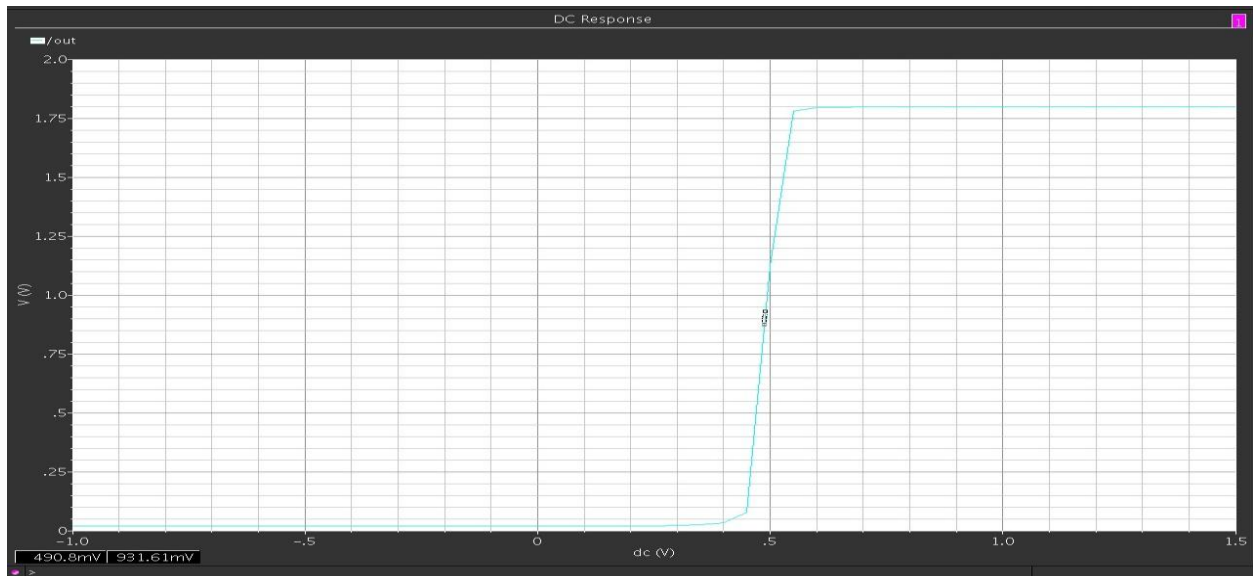
The input specifications are specified in detail in Table 1.
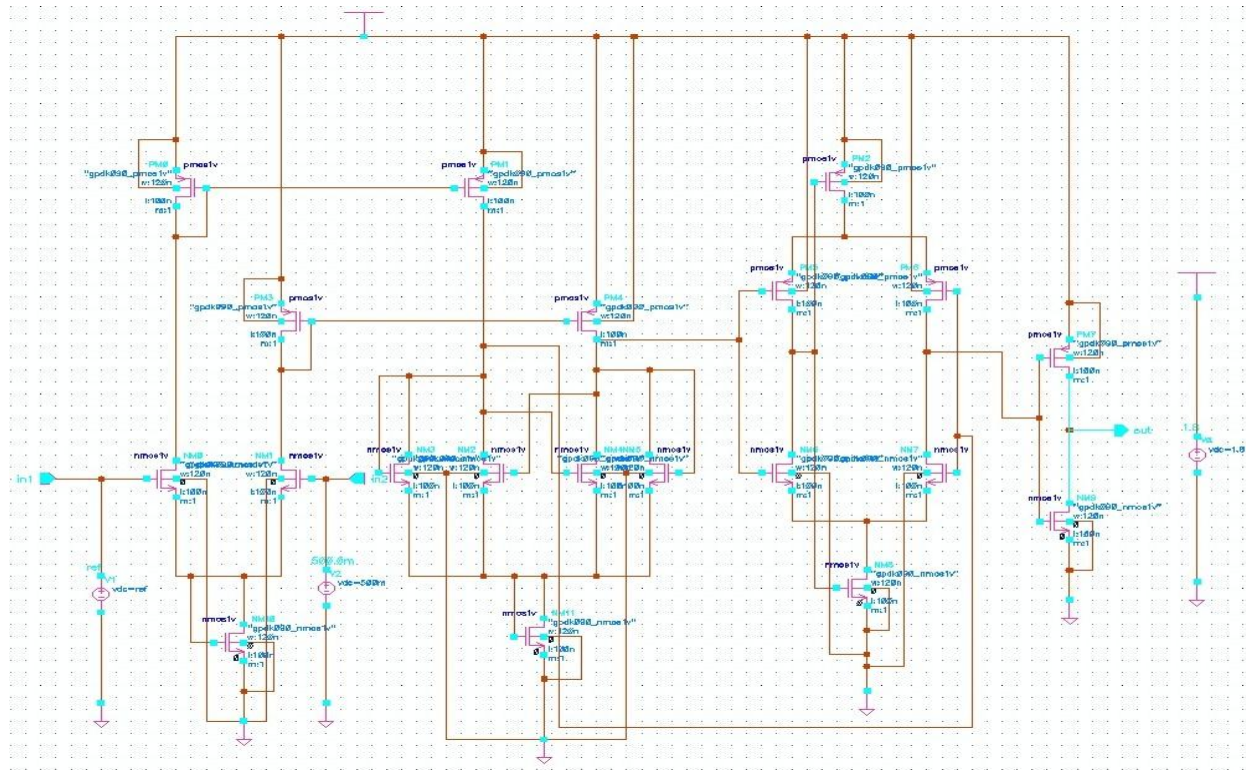
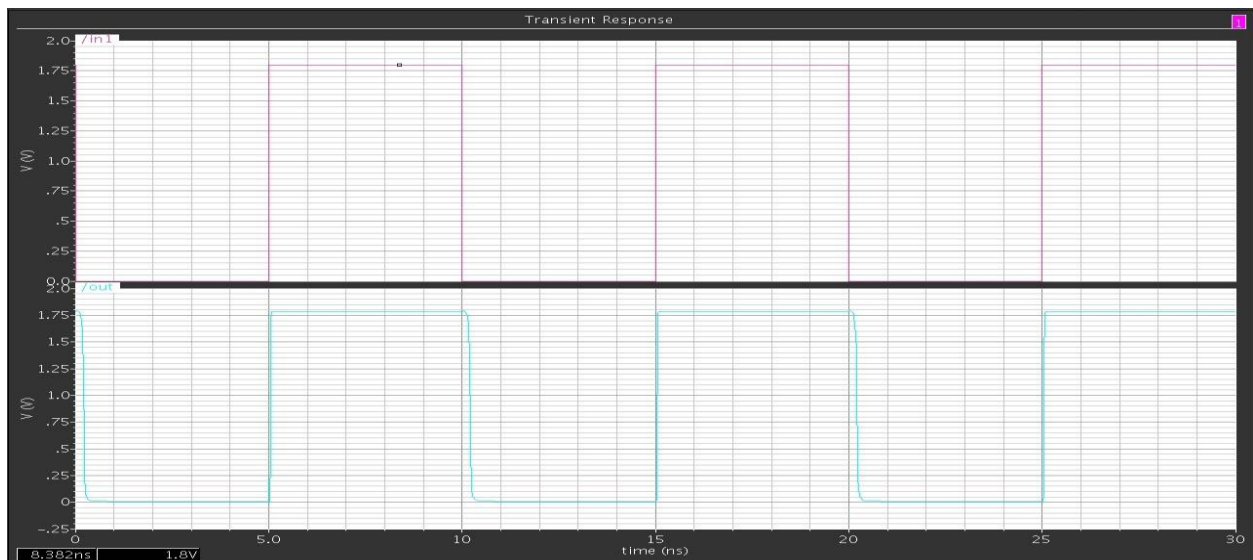(Fig 5.1 – Pre-amplifier based comparator circuit diagram)

DC Analysis:

Figure shows the DC analysis of the preamplifier based comparator. For the DC analysis, both

input and reference voltage are taken as DC voltage source.

Transient Analysis

The above figure shows the transient response of the preamplifier based comparator. For the

transient response the input voltage source is a pulse voltage source and the reference voltage

source is a DC voltage source.

Results

Input Offset Voltage: 16.6 mV

Dynamic Power Dissipation: 102.5 μW

Propagation Delay: 104.1 ps

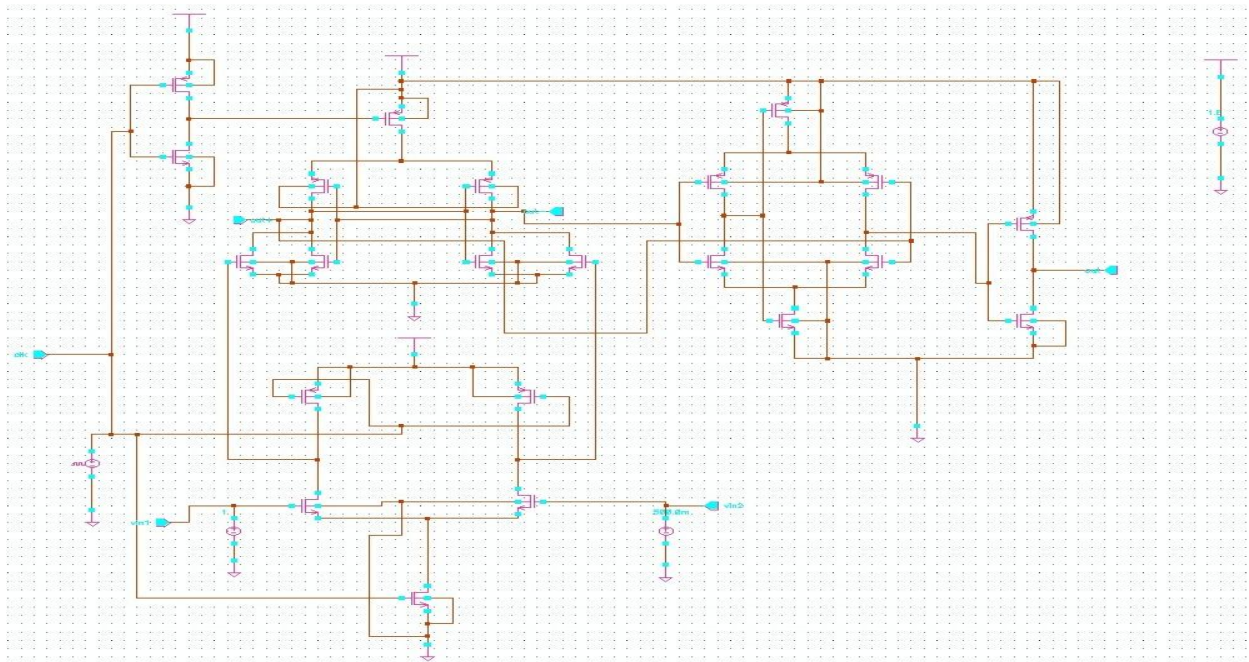Speed: 9.6 GHz

# 5.2 DOUBLE TAIL LATCH TYPE VOLTAGE SENSE AMPLIFIER

Circuit Diagram

Figure 5.2 shows the schematic (designed in Cadence) of the Double Tail Latch Type Voltage Sense Amplifier circuit. The supply voltage is 1.8 V. Reference voltage is .4 V. The input specifications are specified in detail in Table 1.

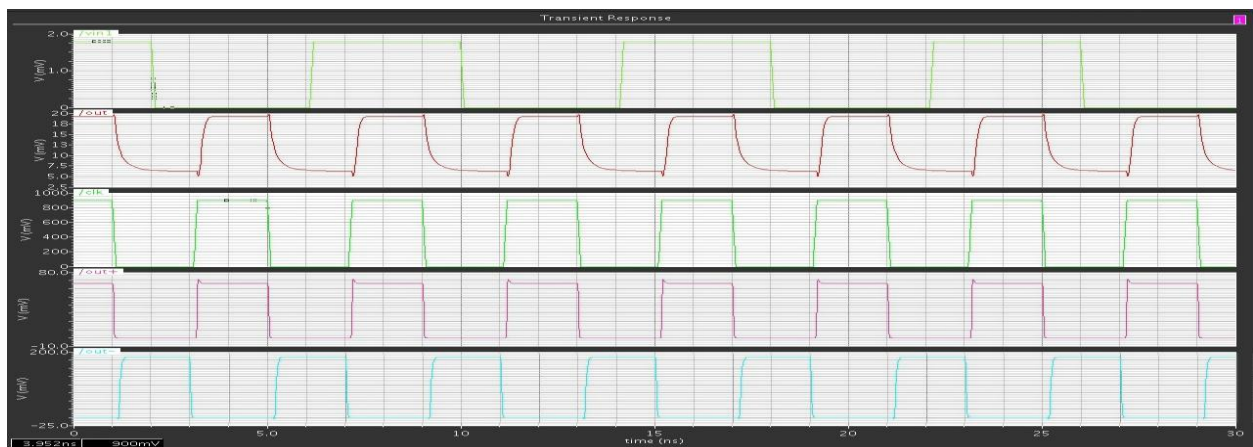(Fig 5.2 – Double Tail Latch Type Voltage Sense Amplifier circuit diagram)

DC Analysis:

Figure shows the DC analysis of the preamplifier based comparator. For the DC analysis, both input and reference voltage are taken as DC voltage source. Input voltage is swept from -1V to 1.8V. We observe that the amplifier is working fine.
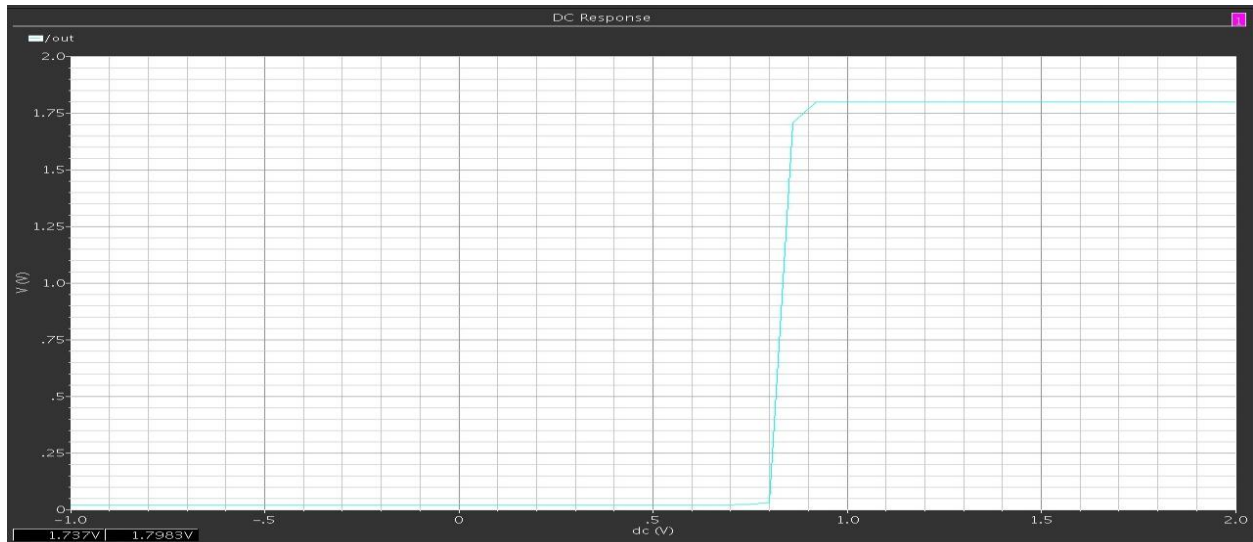
Transient Analysis

Figure shows the transient response of the preamplifier based comparator. For the transient response the input voltage source is a pulse voltage source and the reference voltage source is a DC voltage source.

Results

Input Offset Voltage: 30.3 mV

Dynamic Power Dissipation: 64.7 μW
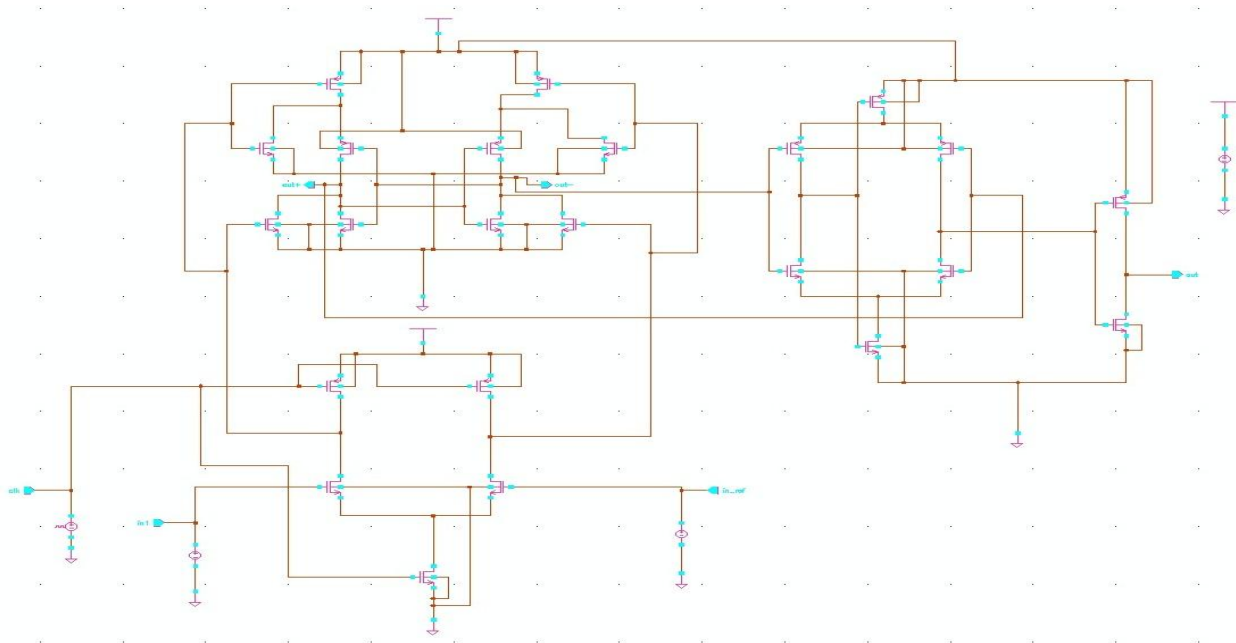
Propagation Delay: 996.8 ps

Speed: 1.003 GHz

5.3 DYNAMIC COMPARATOR

Circuit Diagram

Figure 5.3 shows the schematic (designed in Cadence) of the Dynamic comparator circuit. The supply voltage is 1.8 V. Reference voltage is .4 V. The input specifications are specified in detail in Table 1. Transistor sizes are specified in Table 2.
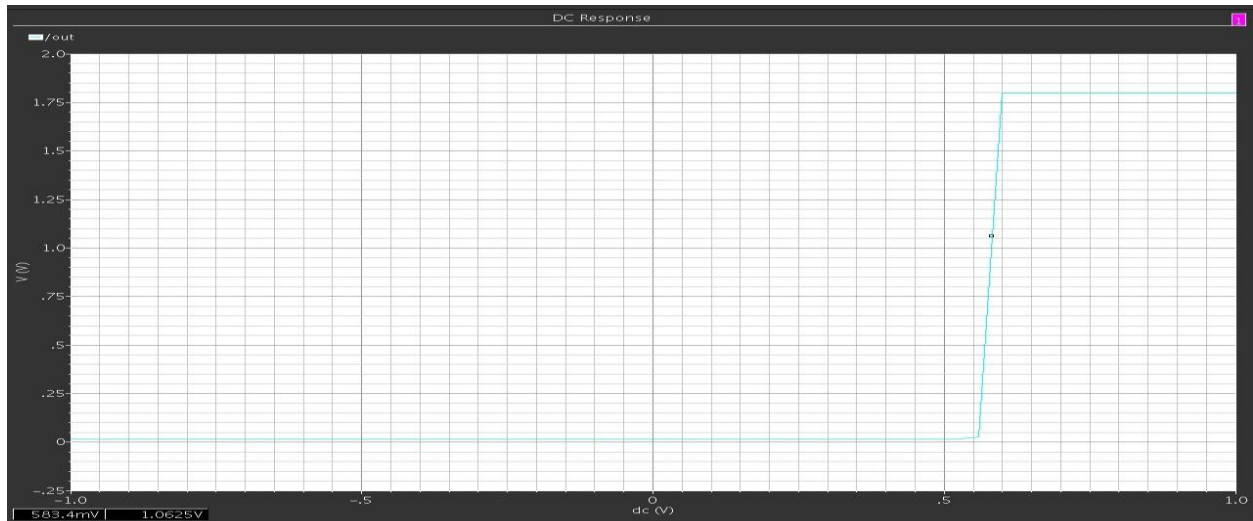

(Fig 5.3 – Dynamic Comparator circuit diagram)

DC Analysis:

Figure shows the DC analysis of the dynamic comparator. For the DC analysis, both input and reference voltage are taken as DC voltage source. Input voltage is swept from -1V to 1.8V. We conclude that the circuit is working fine.

Transient Analysis:

Figure shows the transient response of the dynamic comparator. For the transient response the input voltage source is a pulse voltage source and the reference voltage source is a DC voltage source.

Results:

Input Offset Voltage: 13 mV

Dynamic Power Dissipation: 19 µW
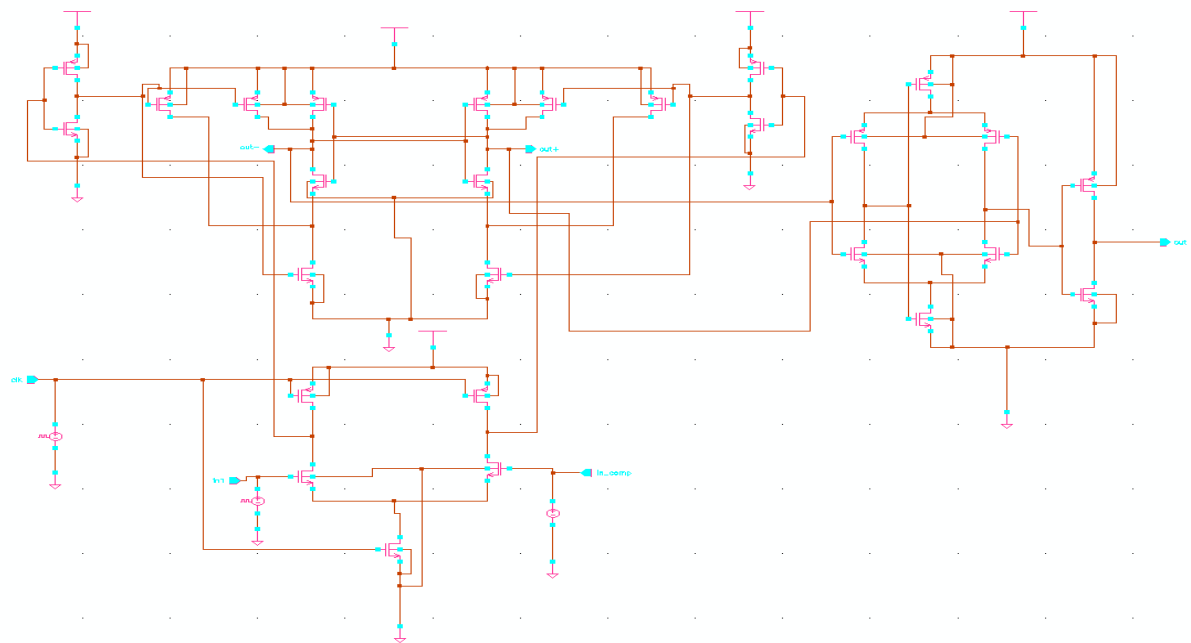
Propagation Delay: 987.5 ps

Speed: 1.012 GHz

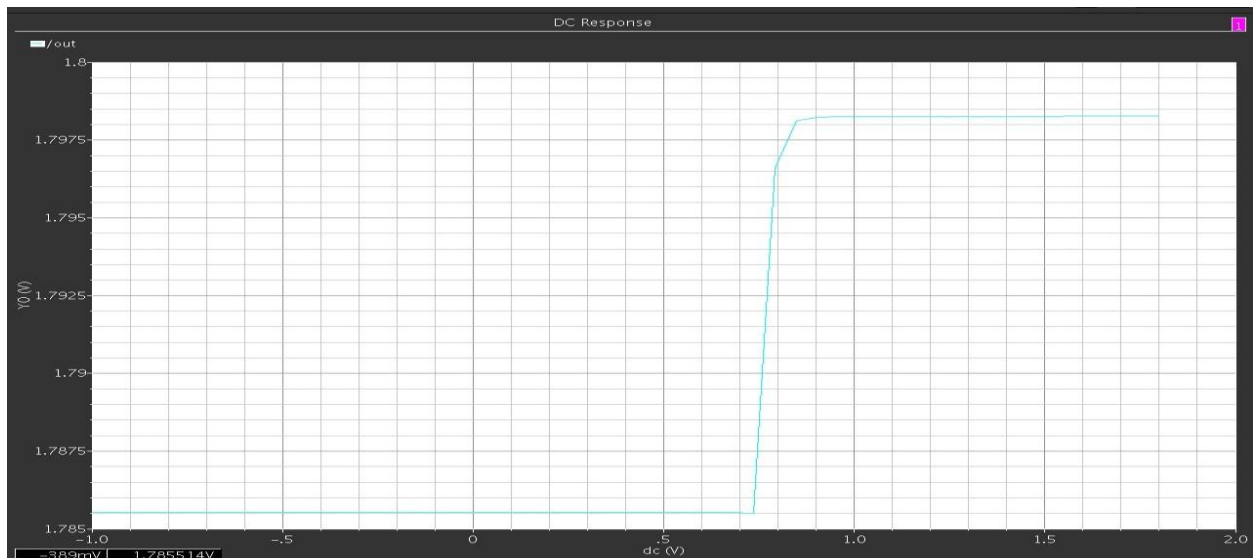# 5.4 DOUBLE TAIL DUAL RAIL DYNAMIC LATCHED COMPARATOR

Circuit Diagram

Figure 5.4 shows the schematic (designed in Cadence) of the Dynamic comparator circuit. The supply voltage is 1.8 V. Reference voltage is .4 V. The input specifications are specified in detail in Table 1. Transistor sizes are specified in Table 2.

(Fig 5.4 – Double Tail Dual Rail Latched Type Dynamic Comparator Circuit Diagram)

DC Analysis:

Figure shows the DC analysis of the dynamic comparator. For the DC analysis, both input and reference voltage are taken as DC voltage source. Input voltage is swept from -1V to 1.8V. We conclude that the circuit is working fine.

Transient Analysis:

Figure shows the transient response of the dynamic comparator. For the transient response the input voltage source is a pulse voltage source and the reference voltage source is a DC voltage source.
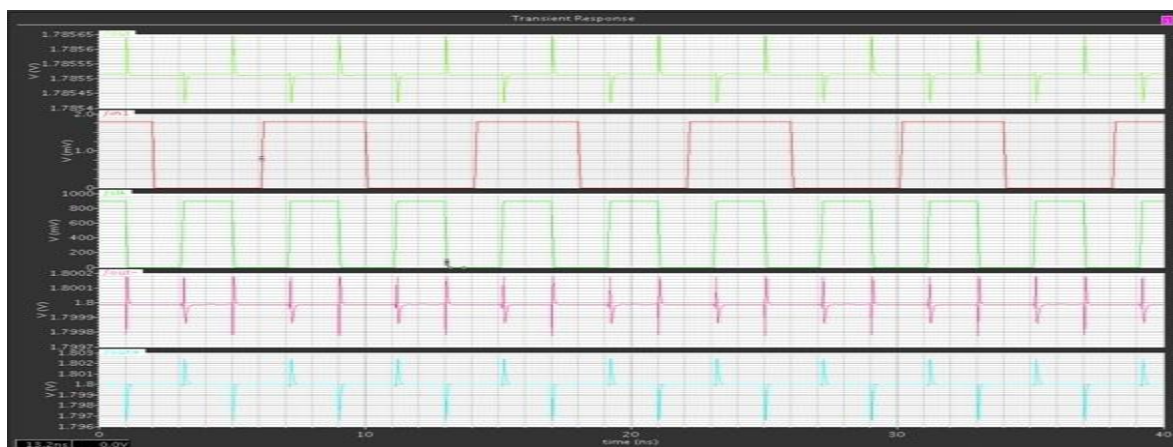
Results:

Input Offset Voltage: 13 mV

Dynamic Power Dissipation: 10.2 μW

Propagation Delay: 1012.3 ps

Speed: 0.98 GHz

5.5 Result Summary

Comparator	Transistor Count	Input Offset Voltage (mV)	Dynamic Power Dissipation (μW)	Propagation Delay (ps)	Speed (GHz)
Preamplifier based comparator	20	16.6	102.5	104.1	9.6
Double Tail Latch Type Voltage Sense Amplifier	22	30.3	64.7	996.8	1.003
Dynamic Comparator	23	13	19	987.5	1.012
Double Tail Dual Rail Dynamic Latched Comparator	27	13	10.2	1012.3	0.98

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 CONCLUSION

Among the comparators studied the double-tail dual-rail latch comparator which has a back to back latch stage has the lowest power dissipation. Dynamic comparators have less dynamic power dissipation and input offset voltage compared to the pre-amplifier based comparator. But their speed is the latter due to the parasitic capacitances. The layout for the different comparators are given in Appendix.

6.2 SCOPE FOR FUTURE WORK

Offset voltage optimization and optimization of the circuits after layout can be one topic. Finding application specific comparators can be another topic.

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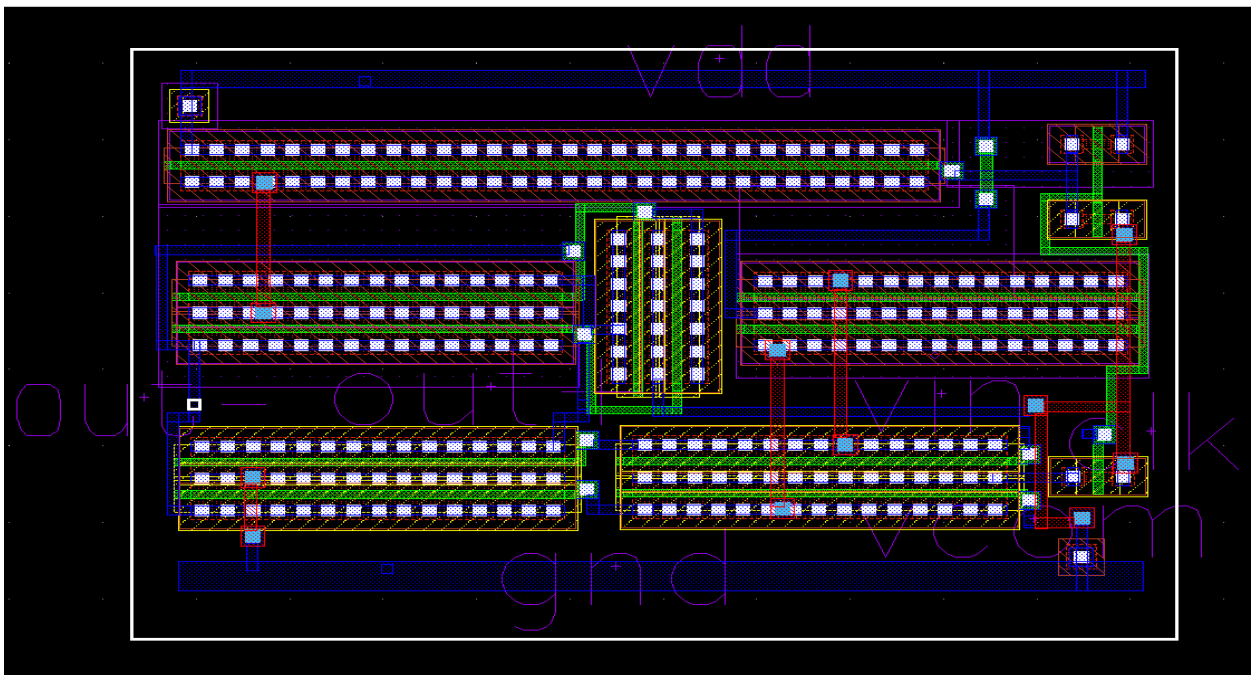[8] Cadence Online Documentation. Avilable: http://www.cadence.com

APPENDIX

CIRCUIT LAYOUTS
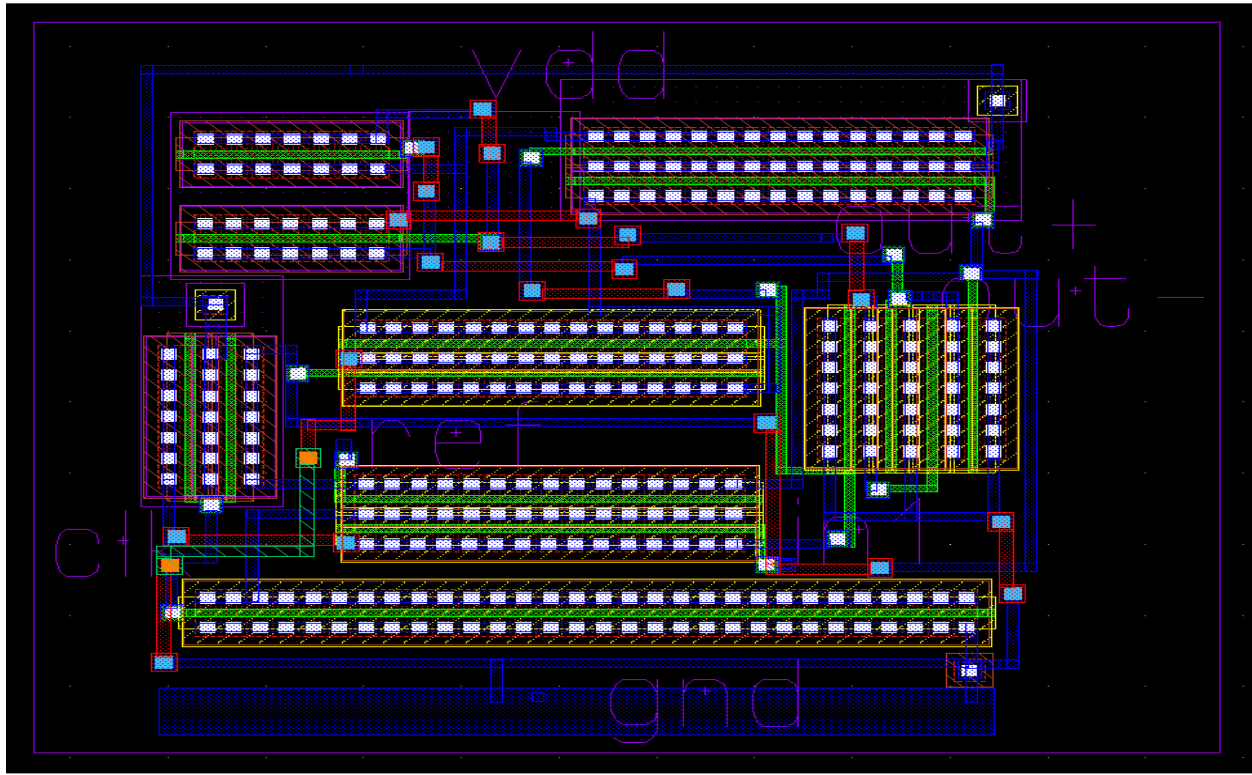
Pre-amplifier based comparator
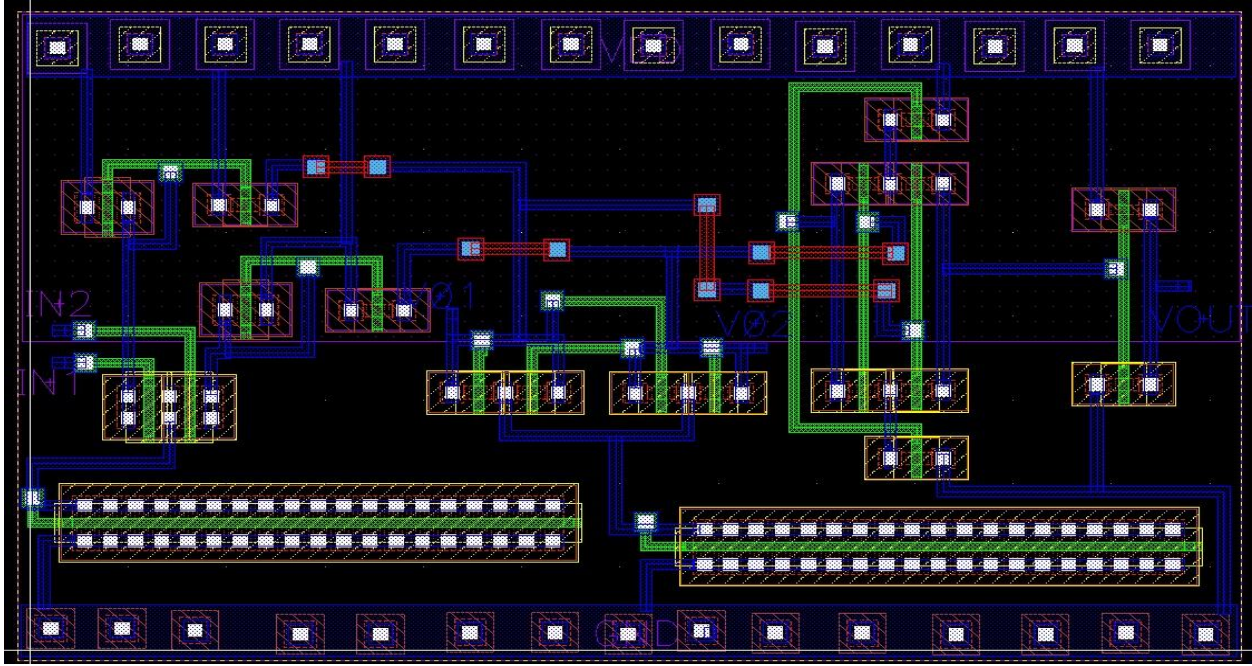
Double Tail Latch Type Voltage Sense Amplifier

Dynamic Comparator

Double Tail Dual Rail Dynamic Latched Comparator