IMPLEMENTATION OF WiMAX PHYSICAL LAYER BASEBAND PROCESSING BLOCKS IN FPGA

A Thesis Submitted In Partial Fulfillment of the Requirements for the Degree of

MASTER OF TECHNOLOGY

IN

VLSI DESIGN AND EMBEDDED SYSTEM

By

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National Institute Of Technology

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Under The Guidance Of

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ROURKELA

CERTIFICATE

This is to certify that the thesis titled, "**IMPLEMENTATION OF WiMAX PHYSICAL LAYER BASEBAND PROCESSING BLOCKS IN FPGA"** submitted by **Bineeta Soreng, Roll No-211EC2303** in partial fulfillment of the requirements for the award of Master of Technology Degree in **Electronics & Communication Engineering** with specialization in **VLSI Design and Embedded System** during **2011-2013** at the National Institute of Technology, Rourkela is an authentic work carried out by her under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other University / Institute for the award of any Degree or Diploma.

PLACE-NIT Rourkela

DATE-24/05/2013

Prof. D.P ACHARYA

Associate Professor

Dept. of Electronics & Communication Engg.

National Institute of Technology

Dedicated To My Family

And

My Teachers

ACKNOWLEGEMENT

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ABSTRACT

This project thesis elaborates on designing a baseband processing blocks for Worldwide Interoperability for Microwave Access (WiMAX) physical layer using an FPGA. WiMAX provides broadband wireless access and uses OFDM as the essential modulation technique. The channel performance is badly affected due to synchronization mismatches between the transmitter and receiver ends so the transmitted signal received is not reliable as the OFDM deals with high data rate. This thesis includes the theory and concepts behind OFDM, WiMAX IEEE 802.16d standard and other blocks algorithms, its architectures used for designing as well as a presentation of how they are implemented. Here Altera's FPGA has been used for targeting to the EP4SGX70HF35C2 device of the Stratix IV family. WiMAX use sophisticated digital signal processing techniques, which typically require a large number of mathematical computations. Here Stratix IV devices are ideally suited for these kinds of complex tasks because the DSP blocks have a combination of dedicated elements that perform multiplication, addition, subtraction, accumulation, summation, and dynamic shift operations. The WiMAX physical layer baseband processing architecture consists of various major modules which were simulated block wise in order to check its giving the correct output as required. The coding style used here is VHDL. The sub-blocks have been synthesized using Altera Quartus II v11. 0 and simulated using ModelSim Altera Edition 6.6d.

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LIST OF ACRONYMS

WiMAX- Worldwide Interoperability for Microwave Access

BWA- Broadband Wireless Access

LAN- Local Area Network

MAN- metropolitan area network

OFDM- Orthogonal Frequency Division Multiplexing

DMT- Discrete Multi-tone Modulation

BPSK- binary phase-shift keying

QPSK- Quadrature phase- shift keying

QAM- Quadrature Amplitude Modulation

DSL- Digital Subscriber Loop

MIMO- Multi Input and Multi Output

IFFT- Inverse Fast Fourier Transform

WDM- Wavelength-Division Multiplexing

ISI- Inter symbol interference

LTE- Long-Term Evolution

DAB- Digital Audio Broadcasting

DVB- Digital Video Broadcasting

Chapter 1

INTRODUCTION

1. INTRODUCTION

In recent years due to the immense demand for internet access and cellular services has led to the demand of communication standard which provides high data rate, coverage and mobility. Broadband wireless access (BWA) is increasingly gaining popularity as an option for the last-mile connection replacing cable modems and DSL connections [1]. To be specific, WiMAX, the IEEE 802.16 standard, came as a follow-up to the successful 802.11 wireless local area network (LAN) standard; with deployments of the IEEE 802.16 wireless metropolitan area network (MAN) standard. The standard offers both fixed broadband wireless access for rural as well as remote areas, and also provides mobility for users to support portable devices.

1.1 Motivation

- WiMAX, like DSL/cable is standards based and enables vendors to interoperate with one another. The Worldwide Interoperability for Microwave Access (WiMAX) is specified for the IEEE 802.16 standard. This standard has been further revised for 2-11GHz fixed (802.16.a-2004) and 2-6GHz portable (802.16e) wireless solutions.
- Typical WiMAX equipment would contain a baseband-PHY processor and the MAC network processor besides memory and other peripherals. In physical layer, WiMAX uses Orthogonal Frequency Division Multiplexing (OFDM) for modulation which divides a portion of the data over narrowband carriers transmitted in parallel at different frequencies. The same technique has been used as Discrete Multi-tone Modulation (DMT) in ADSL. OFDM makes WiMAX scalable for a fluctuating user base, since the spectrum can be dynamically reallocated (range: 1.25-20 MHz) with variations in the number of subscribers. In addition, OFDM improves resilience to interference and outdoor environment, and improves the signal to noise ratio at the terminals.

1.2 Literature Review

Forward error correction is provided through the use of a rate 1/2 convolution code with puncturing to provide rates of 2/3, 3/4, and 5/6. The coded bits are interleaved to avoid error bursts and grouped together to form the symbols, which are mapped to one of binary phase-shift keying (BPSK), Quadrature PSK (QPSK), 16 Quadrature amplitude modulation (QAM), and

64QAM. The modulated symbols are encoded by the MIMO encoder which performs SFBC or SDM encoding. The MIMO encoded symbols are OFDM-modulated by 64-point inverse fast Fourier transforms (IFFT). Each output of the IFFT is converted to a serial sequence and a cyclic prefix (CP) is added. After the CP is added, each OFDM symbol is clipped.[1]

In recent years, Internet traffic in the core network has been doubling almost every two years, and predictions indicate that it will continue to exhibit exponential growth due to emerging applications such as high-definition and real-time video communications [1] [2]. As a result of this rapid increase in traffic demands, large-capacity and cost effective optical fiber transmission systems are required for realizing future optical networks. So far, Wavelength-Division Multiplexing (WDM) systems with up to 40 Gb/s capacity per channel have been deployed in backbone networks, while 100 Gb/s interfaces are now commercially available and 100 Gb/s deployment is expected soon. Moreover, it is foreseen that optical networks will be required to support Tb/s class transmission in the near future [2] [3]. However, scaling to the growing traffic demands is challenging for conventional optical transmission technology as it suffers from the electrical bandwidth bottleneck limitation, and the physical impairments become more severe as the transmission speed increases [3].

Recently, OFDM (Orthogonal Frequency-Division Multiplexing) has been considered a promising candidate for future high-speed optical transmission technology. OFDM is a multicarrier transmission technology that transmits a high-speed data stream by splitting it into multiple parallel low-speed data channels. OFDM first emerged as a leading physical layer technology in wireless communications, as it provides an effective solution to inter-symbol interference (ISI) caused by the delay spread of wireless channels. It is now widely adopted in broadband wireless and wire-line networking standards, such as 802.11a/g WiFi, 802.16 WiMAX, LTE (Long-Term Evolution), DAB and DVB (Digital Audio and Video Broadcasting), and DSL (Digital Subscriber Loop) around the world [3].

Because of the great success of OFDM in wireless and wireline systems, it is currently being considered for optical transmission and networking. With the intrinsic flexibility and scalability characteristics of optical OFDM technology, novel elastic optical network architecture, possessing the capability to manage signals with different data rate and variable bandwidth, can be built to meet the requirements of future optical networks [6].

1.3 Objective

The objective is to implement WiMAX physical layer baseband processing blocks in an FPGA using STRATIX IV family targeting to EP4SGX70HF35C2 device which will support the IEEE 802.16 standard.

Implementation of WiMAX physical layer baseband processing blocks efficiently in FPGA so that it can be used further for integrating together in the baseband processor for communication purpose. The implemented blocks are scrambler, descrambler, RS encoder and decoder, convolution encoder and Viterbi decoder, mapper, IFFT/FFT.

WiMAX uses OFDM as modulation technique. The OFDM has one primary advantage as it deals with high data rate and can handle multi-carriers frequencies than over single-carrier schemes as it has the ability to cope with severe channel conditions like attenuation, narrowband interference and frequency-selective fading due to multipath and has the liability to work without complex equalization filters. Channel equalization is simplified because OFDM may be viewed as using many slowly modulated narrowband signals rather than one rapidly modulated wideband signal. The low symbol rate makes the use of a guard interval between symbols affordable, making it possible to eliminate inter symbol interference (ISI) and utilize echoes and time-spreading (on analogue TV these are visible as ghosting and blurring, respectively) to achieve a diversity gain, i.e. a signal-to-noise ratio improvement. This mechanism also facilitates the design of a single frequency (SFNs), where several adjacent transmitters send the same signal simultaneously at the same frequency, as the signals from multiple distant transmitters may be combined constructively, rather than interfering as would typically occur in a traditional single-carrier system.

1.4 Thesis Organization

This section shows how the contents have been distributed according to the chapters. There are total five chapters.

- **Chapter 2- INTRODUCTION TO WIMAX**

This chapter describes about the meaning of WiMAX, its history and reasons of choosing it over others, its features. WiMAX is based on IEEE 802.16 so the detail about the standard

specification has been given. As WiMAX uses the OFDM modulation technique so its basic function has been discussed. Advantages and disadvantages of OFDM have been shown. Application of WiMAX and about the Stratix IV FPGA has also been discussed.

- **Chapter 3- WIMAX PHYSICAL LAYER**

This chapter describes about the architecture of WiMAX PHY Layer Baseband processor. Individually, WiMAX PHY Layer Transmitter and WiMAX PHY Layer Receiver chain blocks have been shown. Each side consists of many blocks like scrambler, descrambler, RS encoder and decoder, mapper, demapper and other blocks. Each block function and its architecture have been discussed clearly.

- **Chapter 4-IMPLEMENTATION OF DIFFERENT BLOCKS OF WIMAX PHY LAYER BASEBAND PROCESSOR**

This chapter shows the implementation of WiMAX PHY Layer transmitter's and receiver's blocks individually. Implemented blocks on transmitter side are scrambler, RS encoder, convolution encoder, 16-QAM mapper and in the receiver side–RS decoder, Viterbi decoder, 16-QAM demapper. The Stratix IV GX FPGA has been used, targeting to the device EP4SGX70HF35C2. For each block following have been shown:

- I/O signals
- RTL schematic
- Simulation result
- I/O signal description
- Device utilization summary

- **Chapter 5-CONCLUSION AND FUTURE WORK**

This chapter shows the conclusion and future work of the project. It was concluded from the device utilization summary that the processing time of decoder is more and complex than encoder. The block memory usage is more in decoder and lookup tables have been replaced instead of complex multiplication and addition.

1.5 Summary

This chapter describes about the introduction for increasing demand for the broadband wireless access and the need for different evolving standards. It also provides the reason for motivating in choosing WiMAX and its technology behind it. The different modulation schemes and literature review have been given. The brief about the study of WiMAX and physical layers has been discussed. Overview of research work and how the thesis has been organizing the whole chapters are given briefly. This chapter also describes about the overall work and the objective of the project.

Chapter 2

INTRODUCTION TO WiMAX

2 INTRODUCTION TO WiMAX

Before we start to read about Wimax, let us first discuss the related concepts that help in better understanding of WiMAX. Wireless refers to transmitting signals using radio waves as the medium as an alternative of wires. Wireless operations allow working in long-range communications that are not possible to implement with the use of wires. The term “Wireless” refer to telecommunications systems which use some form of energy to transfer information without the use of wires. Wireless technology has turned out to be part of everyday life. The whole thing, from phones and satellites, to computer equipment and the Internet, no longer requires long, bulky wires to work correctly. Wireless technologies are used for tasks as simple as switching off the television or as complex as supplying the sales force with information from an automated enterprise application while in the field. Now cordless keyboards and mice, PDAs, pagers and digital and cellular phones have become part of our daily life.

2.1 Overview of WiMAX

WiMAX (Worldwide Interoperability for Microwave Access) is one of the broadband wireless technologies around today. WiMAX systems are most widely expected to deliver broadband access services to residential and enterprise customers in an economical way. Loosely, WiMax is a standardized wireless version of Ethernet intended primarily as an alternative to wire technologies (such as Cable Modems, DSL and T1/E1 links) to provide broadband access to customer premises. More strictly, WiMAX is an industry trade organization formed by leading communications component and equipment companies to promote and certify compatibility and interoperability of broadband wireless access equipment that conforms to the IEEE 802.16 and ETSI HIPERMAN standards. WiMAX would operate similar to WiFi but at higher speeds, over greater distances and for a greater number of users.

WiMAX has the ability to provide service even in areas that are difficult for wired infrastructure to reach and the ability to overcome the physical limitations of traditional wired infrastructure. WiMAX was formed in April 2001, in anticipation of the publication of the original 10-66 GHz IEEE 802.16 specifications. WiMAX is to 802.16 as the WiFi Alliance is to 802.11. A certification that denotes interoperability of equipment built to the IEEE 802.16 or

compatible standard. The IEEE 802.16 Working Group develops standards that address two types of usage models:

- A fixed usage model (IEEE 802.16-2004).
- A portable usage model (IEEE 802.16e).

2.2 History of WiMAX

Most researchers are familiar with the technical features of WiMAX technology but the evolution that WiMAX went through, in terms of standardization and certification, is missing and unknown to most people. Knowledge of this historical process would however aid to understand how WiMAX has become the widespread technology that it is today. Furthermore, it would give insight into the steps to undertake for anyone aiming at introducing a new wireless technology on a worldwide scale. Therefore, this article presents a survey on all relevant activities that took place within three important organizations: the 802.16 Working Group of the IEEE (Institute of Electrical and Electronics Engineers) for technology development and standardization, the WiMAX Forum for product certification and the ITU (International Telecommunication Union) for international recognition.

An elaborated and comprehensive overview of all those activities is given, which reveals the importance of the willingness to innovate and to continually incorporate new ideas in the IEEE standardization process and the importance of the WiMAX Forum certification label granting process to ensure interoperability. We also emphasize the steps that were taken in cooperating with the ITU to improve the international esteem of the technology. Finally, a WiMAX trend analysis is made. We showed how industry interest has fluctuated over time and quantified the evolution in the WiMAX product certification and deployments. It is shown that most interest went to the 2.5GHz and 3.5GHz frequencies, that most deployments are in geographic regions with a lot of developing countries and that the higher people coverage is achieved in Asia Pacific. This elaborated description of all standardization and certification activities, from the very start up to now, will make the reader comprehend how past and future steps are taken in the development process of new WiMAX features.(taken from 06042387.pdf)

2.3 Reasons for Choosing WiMAX

- WiMAX satisfies a variety of access needs. Potential applications include extending broadband capabilities to bring them closer to subscribers, filling gaps in cable, DSL and T1 services, WiFi and cellular backhaul, providing last-100 meter access from fiber to the curb and giving service providers another cost-effective option for supporting broadband services.
- WiMAX supports very high bandwidth solutions where large spectrum deployments (i.e. >10 MHz) are desired using existing infrastructure keeping costs down while delivering the bandwidth needed to support a full range of high-value, multimedia services.
- WiMAX helps service providers to meet many of the challenges they face due to increasing customer demands without discarding their existing infrastructure investments because it has the ability to seamlessly interoperate across various network types.
- WiMAX provides wide area coverage and quality of service capabilities for applications ranging from real-time delay-sensitive voice-over-IP (VoIP) to real-time streaming video and non-real-time downloads which ensures that subscribers obtain the performance they expect for all types of communications.
- WiMAX, which is an IP-based wireless broadband technology, can be integrated into both wide-area third-generation (3G) mobile and wireless and wire line networks, allowing it to become part of a seamless anytime, anywhere broadband access solution.
- WiMAX has the following advantages: cheaper implementation costs, less monthly ongoing maintenance costs, quicker and easier setup/ deployment/ reconfiguration/ disassembly, less impact on the environment, more scalability for future network expanding, and more flexibility. The distance of a WiMAX connection can be up to 30 miles (50 km) at data rates up to 75 Mbps using both the unlicensed and licensed spectrums.

Ultimately, WiMAX is intended to serve as the next step in the evolution of 3G mobile phones, via a potential combination of WiMAX and CDMA standards called 4G.

2.4 Salient Features of WiMAX

WiMAX is a wireless broadband solution that offers a rich set of features with a lot of flexibility in terms of deployment options and potential service offerings. Some of the more salient features that deserve highlighting are as follows:

2.4.1 Two type of services

WiMAX can provide two forms of wireless service:

- **Non-line-of-sight:** service is a WiFi sort of service. Here a small antenna on your computer connects to the WiMAX tower. In this mode, WiMAX uses a lower frequency range -- 2 GHz to 11 GHz (similar to WiFi).
- **Line-of-sight:** service, where a fixed dish antenna points straight at the WiMAX tower from a rooftop or pole. The line-of-sight connection is stronger and more stable, so it's able to send a lot of data with fewer errors. Line-of-sight transmissions use higher frequencies, with ranges reaching a possible 66 GHz.

2.4.2 Very high peak data rates

WiMAX is capable of supporting very high peak data rates. In fact, the peak PHY data rate can be as high as 74Mbps when operating using a 20MHz wide spectrum.
More typically, using a 10MHz spectrum operating using TDD scheme with a 3:1 downlink-to-uplink ratio, the peak PHY data rate is about 25Mbps and 6.7Mbps in the downlink and the uplink, respectively.

2.4.3 Scalable bandwidth and data rate support

WiMAX has a scalable physical-layer architecture that allows for the data rate to scale easily with available channel bandwidth.

For example, a WiMAX system may use 128, 512, or 1,048-bit FFTs (Fast Fourier transforms) based on whether the channel bandwidth is 1.25MHz, 5MHz, or 10MHz, respectively. This scaling may be done dynamically to support user roaming across different networks that may have different bandwidth allocations.

2.4.4 OFDM-based physical layer

The WiMAX physical layer (PHY) is based on orthogonal frequency division multiplexing, a scheme that offers good resistance to multipath, and allows WiMAX to operate in NLOS conditions.

2.4.5 Link-layer retransmissions

WiMAX supports automatic retransmission requests (ARQ) at the link layer for connections that require enhanced reliability. ARQ-enabled connections require each transmitted packet to be acknowledged by the receiver; unacknowledged packets are assumed to be lost and are retransmitted.

2.4.6 Adaptive modulation and coding (AMC)

WiMAX supports a number of modulation and forward error correction (FEC) coding schemes and allows the scheme to be changed on a per user and per frame basis, based on channel conditions.

AMC is an effective mechanism to maximize throughput in a time-varying channel.

2.4.7 Support for TDD and FDD

IEEE 802.16-2004 and IEEE 802.16e-2005 supports both time division duplexing and frequency division duplexing, as well as a half-duplex FDD, which allows for a low-cost system implementation.

2.4.8 WiMAX uses OFDM

Mobile WiMAX uses orthogonal frequency division multiple access (OFDM) as a multiple-access technique, whereby different users can be allocated different subsets of the OFDM tones.

2.4.9 Quality-of-service support

The WiMAX MAC layer has a connection-oriented architecture that is designed to support a variety of applications, including voice and multimedia services.

The WiMAX system offers support for constant bit rate, variable bit rate, real-time, and non-real-time traffic flows, in addition to best-effort data traffic.

WiMAX MAC is designed to support a large number of users, with multiple connections per terminal, each with its own QoS requirement.

2.4.10 Flexible and dynamic per user resource allocation

Both uplink and downlink resource allocation are controlled by a scheduler in the base station. Capacity is shared among multiple users on a demand basis, using a burst TDM scheme.

2.4.11 Robust security

WiMAX supports strong encryption, using Advanced Encryption Standard (AES), and has a robust privacy and key-management protocol.

The system also offers a very flexible authentication architecture based on Extensible Authentication Protocol (EAP), which allows for a variety of user credentials, including username/password, digital certificates, and smart cards.

2.4.12 Support for mobility

The mobile WiMAX variant of the system has mechanisms to support secure seamless handovers for delay-tolerant full-mobility applications, such as VoIP.

2.4.13 Support for advanced antenna techniques

The WiMAX solution has a number of hooks built into the physical-layer design, which allows for the use of multiple-antenna techniques, such as beam forming, space-time coding, and spatial multiplexing.

2.4.14 IP-based architecture

The WiMAX Forum has defined a reference network architecture that is based on an all-IP platform. All end-to-end services are delivered over an IP architecture relying on IP-based protocols for end-to-end transport, QoS, session management, security, and mobility.

2.5 IEEE 802.16 Standard

The main features of IEEE 802.16/WiMAX technology are the following:

- (Carrier) frequency <11 GHz. For the moment, the frequency bands considered are 2.5 GHz, 3.5 GHz and 5.7GHz.
- OFDM. The 802.16 is (mainly) built with the Orthogonal Frequency Division Multiplexing (OFDM) transmission technique known for its high radio resource use efficiency.
- Data rates. A reasonable number is 10 Mb/s. Reports have given more ambitious figures going up to 70 Mb/s or even 100 Mb/s. These values would be in a very good state of the radio channel and for a very small cell capacity, making these values too optimistic for the moment.
- Distance. Up to 20 km, a little less for indoor equipments.

The IEEE 802.16 standard is the network technology used for WiMAX. The IEEE 802.16 working group for BWA was created in 1999. It was divided into two working groups:

- 802.16a, center frequency within the interval 2–11 GHz. This technology will then be used for WiMAX.
- 802.16, with a frequency value interval of 10–66 GHz

2.6 Applications of WiMAX

The WiMAX network provides the ability for service provider to deploy new era broadband service. WiMAX applications are more effective than today. It provides a broad customer base, while adding up a mobility feature to those services. WiMAX technology applications are a mean of service providers to present data, video, voice, mobile and internet access. There are various benefits of WiMAX technology such as it provides simple based prospective cost saving and service efficiency but to be capable to allow VoIP calling, mobile devices, video making and high speed data transfer.

WiMAX technology brings a new ingredient to today's mobile community. The most important application offered by Wimax Technology is business, consumer connectivity, and

backhaul. WiMAX Technology carries real augmentation to communications through which you can get the benefit not only for voice but also video and data transmission to get quick responses to the situation. Through WiMAX a client can deploy a temporary communication service and speed up their network to support events and circumstances. WIMAX technology applications enable us to get temporary access to media, visitors and employees. If we are existing in tower range then we can get easy access to premises equipment for such events. The basic strength behind the Wimax Technology applications are high bandwidth, high quality services, security, deployment, full duplex including DSL and versus cable, and its cost.

2.7 OFDM Basics

An OFDM signal consists of a number of closely spaced modulated carriers. When modulation of any form - voice, data, etc. is applied to a carrier, then sidebands spread out either side. It is necessary for a receiver to be able to receive the whole signal to be able to successfully demodulate the data. As a result when signals are transmitted close to one another they must be spaced so that the receiver can separate them using a filter and there must be a guard band between them. This is not the case with OFDM. Although the sidebands from each carrier overlap, they can still be received without the interference that might be expected because they are orthogonal to each other. This is achieved by having the carrier spacing equal to the reciprocal of the symbol period.

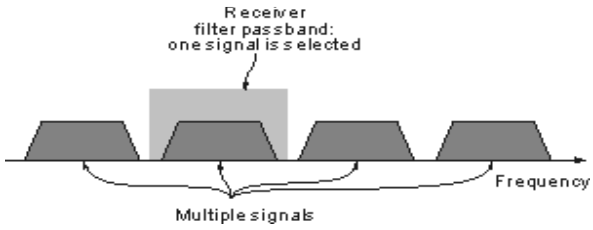

Figure 2.1: Traditional view of receiving signals carrying modulation

To see how OFDM works, it is necessary to look at the receiver. This acts as a bank of demodulators, translating each carrier down to DC. The resulting signal is integrated over the symbol period to regenerate the data from that carrier. The same demodulator also demodulates the other carriers. As the carrier spacing equal to the reciprocal of the symbol period means that

they will have a whole number of cycles in the symbol period and their contribution will sum to zero - in other words there is no interference contribution.

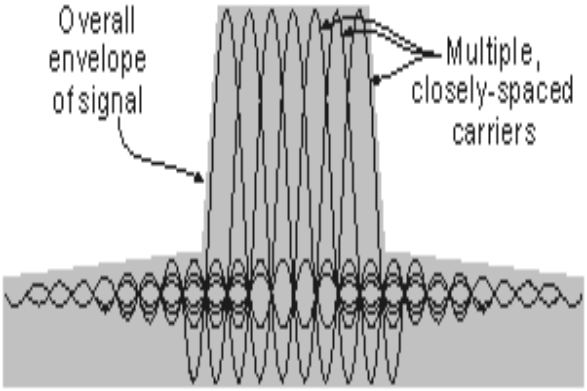

Figure 2.2: OFDM Spectrum

One requirement of the OFDM transmitting and receiving systems is that they must be linear. Any non-linearity will cause interference between the carriers as a result of inter-modulation distortion. This will introduce unwanted signals that would cause interference and impair the orthogonality of the transmission.

In terms of the equipment to be used the high peak to average ratio of multi-carrier systems such as OFDM requires the RF final amplifier on the output of the transmitter to be able to handle the peaks whilst the average power is much lower and this leads to inefficiency. In some systems the peaks are limited. Although this introduces distortion that results in a higher level of data errors, the system can rely on the error correction to remove them.

The data to be transmitted on an OFDM signal is spread across the carriers of the signal, each carrier taking part of the payload. This reduces the data rate taken by each carrier. The low data rate has the advantage that interference from reflections is much less critical. This is achieved by adding a guard band time or guard interval into the system. This ensures that the data is only sampled when the signal is stable and no new delayed signals arrive that would alter the timing and phase of the signal.

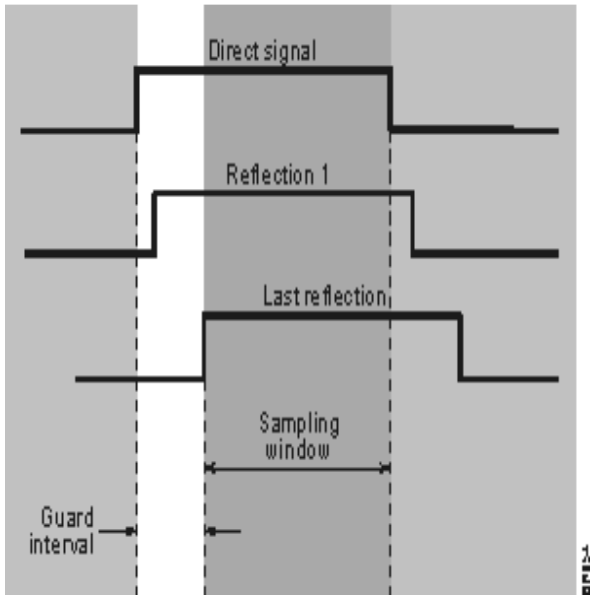

Figure 2.3: Guard Interval

The distribution of the data across a large number of carriers in the OFDM signal has some further advantages. Nulls caused by multi-path effects or interference on a given frequency only affect a small number of the carriers, the remaining ones being received correctly. By using error-coding techniques, which does mean adding further data to the transmitted signal, it enables many or all of the corrupted data to be reconstructed within the receiver. This can be done because the error correction code is transmitted in a different part of the signal.

2.8 FPGA

The field-programmable gate array (FPGA) is a semiconductor device that can be programmed after manufacturing. Instead of being restricted to any predetermined hardware function, an FPGA allows you to program product features and functions, adapt to new standards, and reconfigure hardware for specific applications even after the product has been installed in the field—hence the name "field-programmable". You can use an FPGA to implement any logical function that an application-specific integrated circuit (ASIC) could perform, but the ability to update the functionality after shipping offers advantages for many applications.

Unlike previous generation FPGAs using I/Os with programmable logic and interconnects, today’s FPGAs consist of various mixes of configurable embedded SRAM, high-

speed transceivers, high-speed I/Os, logic blocks, and routing. Specifically, an FPGA contains programmable logic components called logic elements (LEs) and a hierarchy of reconfigurable interconnects that allow the LEs to be physically connected. You can configure LEs to perform complex combinational functions, or merely simple logic gates like AND, XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip- flops or more complete blocks of memory shown in figure 2.4.

As FPGAs continue to evolve, the devices have become more integrated. Hard intellectual property (IP) blocks built into the FPGA fabric provide rich functions while lowering power and cost and freeing up logic resources for product differentiation. Newer FPGA families are being developed with hard embedded processors, transforming the devices into systems on a chip (SoC).

Compared to ASICs or ASSPs, FPGAs offer many design advantages, including:

- Rapid prototyping
- Shorter time to market
- The ability to re-program in the field for debugging
- Lower NRE costs
- Long product life cycle to mitigate obsolescence risk

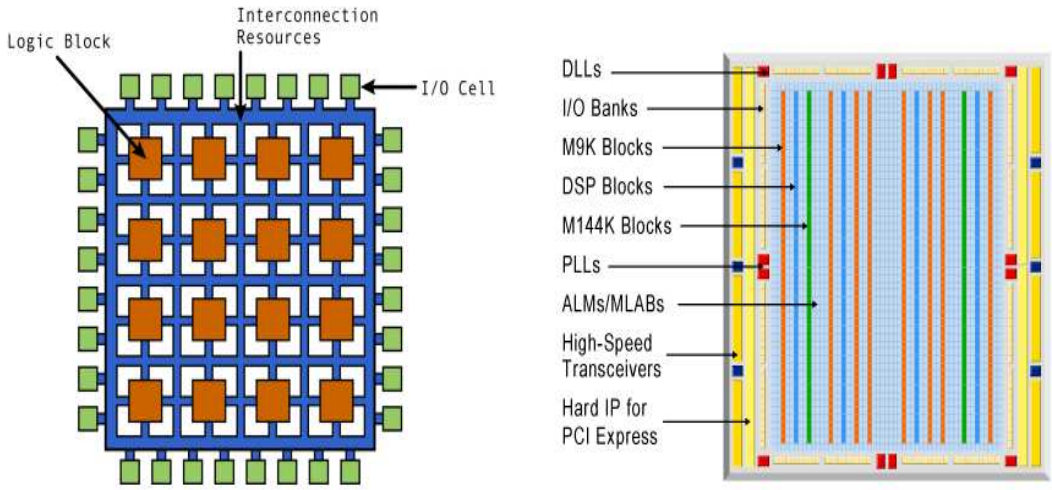

Figure 2.4: Showing previous FPGA and with additional blocks

The 40-nm Stratix IV FPGA family delivers the highest density, the highest performance, and the lowest power. Leveraging 40-nm benefits and proven transceiver and memory interface technology, the Stratix IV FPGA family provides an unprecedented level of system bandwidth with superior signal integrity. Key benefits include:

- The Stratix IV GX FPGA is fully PCI-SIG compliant for PCI Express Gen1 and Gen2 (x1, x4, and x8) and is on the PCI-SIG integrators list
- The Stratix IV GT FPGA is the only FPGA with integrated 11.3-Gbps transceivers.
- Highest density with up to 820K logic elements (LEs), 23.1 Mbits of embedded memory, and up to 1,288 18 x 18 multipliers
- Highest FPGA performance with a 2 speed grade advantage and the industry's most advanced logic and routing architecture
- Unprecedented system bandwidth with up to 48 high-speed transceivers at up to 8.5 Gbps, or up to 24 transceivers at up to 11.3 Gbps optimized for 100G applications and 1,067-Mbps (533 MHz) DDR3 memory interfaces
- Lowest power with up to 50 percent lower power than any other high-end FPGA in the market enabled by 40-nm benefits and Programmable Power Technology
- Hard intellectual property (IP) for PCI Express Gen1 (2.5 Gbps) and Gen2 (5.0 Gbps) with up to four x8 blocks delivering a full endpoint or root-port function
- Superior signal integrity with the ability to drive a 50" backplane at 6.375 Gbps with Plug & Play Signal Integrity

Altera's 40-nm Stratix IV FPGA family is ideal for your high-end digital applications in wireless, wireline, military, broadcast, and many other end markets.

A Stratix IV FPGA, when coupled with a Hardcopy IV ASIC, provides the benefits of both an FPGA and the benefits of an ASIC. FPGA offers logic utilization and shortest compile times. Large FPGA designs require efficient design methodology and tool support.

2.9 Summary

In this chapter, history of WiMAX, reasons for choosing WiMAX, its salient features, and IEEE 802.16 standard, application of WiMAX, OFDM basics and about FPGA have been presented.

WiMAX supports both line of sight and non line of sight. WiMAX would operate similar to WiFi but at higher speeds, over greater distances and for a greater number of users. WiMAX has the ability to provide service even in areas that are difficult for wired infrastructure to reach and the ability to overcome the physical limitations of traditional wired infrastructure. The WiMAX physical layer (PHY) is based on orthogonal frequency division multiplexing, a scheme that offers good resistance to multipath, and allows WiMAX to operate in NLOS conditions. The field-programmable gate array (FPGA) is a semiconductor device that can be programmed after manufacturing.

Chapter 3

WiMAX PHYSICAL LAYER

3 WiMAX PHYSICAL LAYER

The physical (PHY) layer of WiMAX is based on the IEEE 802.16-2004 and IEEE 802.16e-2005 standards and was designed with much influence from WiFi, especially IEEE 802.11a. Although many aspects of the two technologies are different due to the inherent difference in their purpose and applications, some of their basic constructs are very similar. Like WiFi, WiMAX is based on the principles of orthogonal frequency division multiplexing (OFDM) as previously introduced in Chapter 2, which is a suitable modulation/access technique for non–line-of-sight (NLOS) conditions with high data rates.

3.1 Introduction

In WiMAX, the various parameters pertaining to the physical layer, such as number of subcarriers, pilots, guard band and so on, are quite different from WiFi, since the two technologies are expected to function in very different environments. The IEEE 802.16 suite of standards (IEEE 802.16-2004/IEEE 802-16e-2005) [3, 4] is defined within its scope four PHY layers , any of which can be used with the media access control (MAC) layer to develop a broadband wireless system. The PHY layers defined in IEEE 802.16 are

- Wireless MAN SC, a single-carrier PHY layer intended for frequencies beyond 11GHz requiring a LOS condition. This PHY layer is part of the original 802.16 specifications.
- Wireless MAN SCa, a single-carrier PHY for frequencies between 2GHz and 11GHz for point-to-multipoint operations.
- Wireless MAN OFDM, a 256-point FFT-based OFDM PHY layer for point-to-multipoint operations in non-LOS conditions at frequencies between 2GHz and 11GHz. This PHY layer, finalized in the IEEE 802.16-2004 specifications, has been accepted by WiMAX for fixed operations and is often referred to as fixed WiMAX
- Wireless MAN OFDMA, a 2,048-point FFT-based OFDMA PHY for point-to-multipoint operations in NLOS conditions on frequencies between 2GHz and 11GHz. In the IEEE 02.16e-2005 specifications, this PHY layer has been modified to SOFDMA (scalable OFDMA), where the FFT size is variable and can take any one of the following values: 128, 512, 1,024, and 2,048. The variable FFT size allows for optimum operation/implementation of the system over a wide range of channel bandwidths and

radio conditions. This PHY layer has been accepted by WiMAX for mobile and portable operations and is also referred to as mobile WiMAX.

3.2 Architecture of WiMAX PHY Layer Baseband Processor

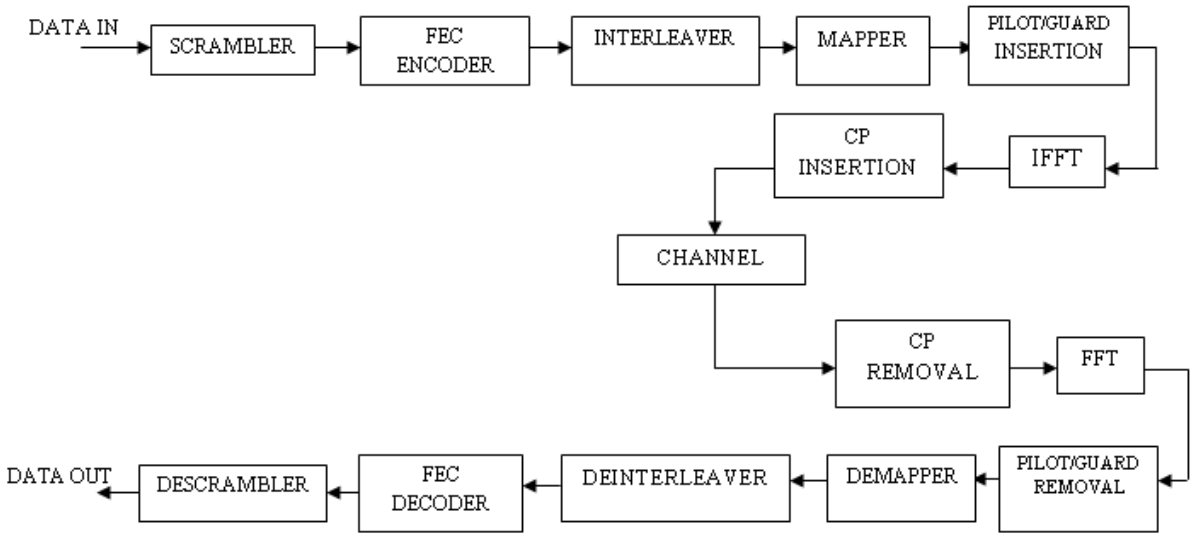

Figure 3.1: WiMAX PHY Layer Baseband processor

3.3 WiMAX PHY Layer Transmitter

The data input is sent to scrambler block where data are randomized on each burst to avoid the long sequence of 0's and 1's. The block changes the data at the bit level, where it processes the input data bytes bit by bit. The randomized output is sent to forward error correction (FEC) block. It adds redundant data to the message. The redundancy allows the receiver to detect and correct a limited number of errors occurring anywhere in the message without the need to ask the sender for additional data. FEC offers the receiver an ability to correct errors without needing a reverse channel to request retransmission of data, but this advantage is at the cost of a fixed higher forward channel bandwidth.

The output from FEC is fed to interleaver. The interleaving is a two step permutation process. The first step ensures that adjacent coded bits are mapped onto a non-adjacent subcarriers. The second step ensures that adjacent coded bits are mapped onto LSB or LSB of the constellation map alternatively to avoid long runs of low reliable bits. Pilot/Guard Insertion:

Adds the values for pilot and guard subcarriers. The subcarrier indices are protocol-specific. Both protocols use scramblers to generate values for the pilots and use null values for the guard subcarriers. IFFT: Converts symbols from the frequency domain to the Pilot/Guard Insertion: Converts symbols from the frequency domain to the time domain.

The size of the IFFT is determined by the number of subcarriers used by the given OFDM protocol. CP Insertion: Copies some samples from the end of the symbol to the front to add some redundancy to the symbols. These duplicated samples are known as a cyclic prefix (CP). The purpose of the cyclic prefix is to avoid Inter-Symbol Interference (ISI) caused by multipath propagation. This block also adds a preamble before the first transmitted symbol. A preamble is a collection of predefined complex numbers known by the receiver so that it can detect the start of new transmission. The preambles for the two protocols have similar structure. After CP insertion, the symbol is converted into analog signals by D/A converter and transmitted through the air.

3.3.1 Channel coding

When the errors introduced by the information channel are unacceptable then the channel coding is needed. The use of channel coders with source coders provides the efficient and reliable transmission in the presence of noise. Our concern is the binary block codes, that is, both the channel coder inputs and outputs will be binary and fixed-length. The channel used is a binary channel (BSC), thus the source coder will encode the source to a binary code and channel coder will encode the binary message to binary codes.

3.3.1.1 Scrambler

The scrambler is used to randomize the data stream before transmitting. The application of scrambling is in satellite, radio relay communications and PSTN modems. A scrambler can be placed just before an FEC coder, or it can be placed after the FEC, just before the modulation.

A Scrambler (or Randomizer) can be either:

- An algorithm that converts an input string into a seemingly random output string of the same length (e.g., by pseudo-randomly selecting bits to invert), thus avoiding long sequences of bits of the same value; in this context, a Randomizer is also referred to as a scrambler.

- An analog or digital source of unpredictable (i.e., high entropy), unbiased, and usually independent (i.e., random) output bits. A "truly" random generator may be used to feed a (more practical) deterministic pseudo-random number generator, which extends the random seed value.

There are two main reasons why scrambling is used:

- To enable accurate timing recovery on receiver equipment without resorting to redundant line coding. It facilitates the work of a timing recovery circuit, an automatic gain control and other adaptive circuits of the receiver (eliminating long sequences consisting of '0' or '1' only).
- For energy dispersal on the carrier, reducing inter-carrier signal interference. It eliminates the dependence of a signal's power spectrum upon the actual transmitted data, making it more dispersed to meet maximum power spectral density requirements (because if the power is concentrated in a narrow frequency band, it can interfere with adjacent channels due to the cross modulation and the intermodulation caused by non-linearities of the receiving tract).

Scramblers are essential components of physical layer system standards besides interleaved coding and modulation. They are usually defined based on linear feedback shift registers (LFSRs) due to their good statistical properties and ease of implementation in hardware.

3.3.1.2 Forward error correction (FEC)

The key idea of FEC is to transmit enough redundant data to allow the receiver to recover from errors all by itself. No sender retransmission required. In telecommunication, information theory, and coding theory, forward error correction (FEC) or channel coding is a technique used for controlling errors in data transmission over unreliable or noisy communication channels. The central idea is the sender encodes their message in a redundant way by using an error-correcting code (ECC).

The redundancy allows the receiver to detect a limited number of errors that may occur anywhere in the message, and often to correct these errors without retransmission. FEC gives the receiver the ability to correct errors without needing a reverse channel to request retransmission

of data, but at the cost of a fixed, higher forward channel bandwidth. FEC is therefore applied in situations where retransmissions are costly or impossible, such as one-way communication links and when transmitting to multiple receivers in the multicast. FEC information is usually added to mass storage devices to enable recovery of corrupted data, and is widely used in modems.

FEC processing in a receiver may be applied to a digital bit stream or in the demodulation of a digitally modulated carrier. For the latter, FEC is an integral part of the initial analog-to-digital conversion in the receiver. The Viterbi decoder implements a soft-decision algorithm to demodulate digital data from an analog signal corrupted by noise. Many FEC coders can also generate a bit-error rate (BER) signal which can be used as feedback to fine-tune the analog receiving electronics.

The maximum fractions of errors or of missing bits that can be corrected is determined by the design of the FEC code, so different forward error correcting codes are suitable for different conditions.

3.3.1.2.1 RS encoder

Reed-Solomon codes are based on a specialized area of mathematics known as Galois fields or finite fields. A finite field has the property that arithmetic operations (+,-, x, / etc.) on field elements always have a result in the field. A Reed-Solomon encoder or decoder needs to carry out these arithmetic operations. These operations require special hardware or software functions to be implemented.

A Reed-Solomon codeword is generated using a special polynomial. All valid code words are exactly divisible by the generator polynomial. The general form of the generator polynomial is g(x) =$(x-\alpha^{i})(x-\alpha^{i+1})\dots(x-\alpha^{i+2t})$, and the codeword is constructed using c(x) = g(x).i(x) Where g(x) is the generator polynomial, i(x) is the information data and c(x) is the code word. To support variable block size and therefore configurable error correction capability, puncturing and shortened codes are supported. Finally, in the IEEE802.16-2004 standard the redundant bits are sent first, while leaving the trailing byte at the end to flush the convolutional encoder stage. The architecture of RS Encoder is shown in the figure.

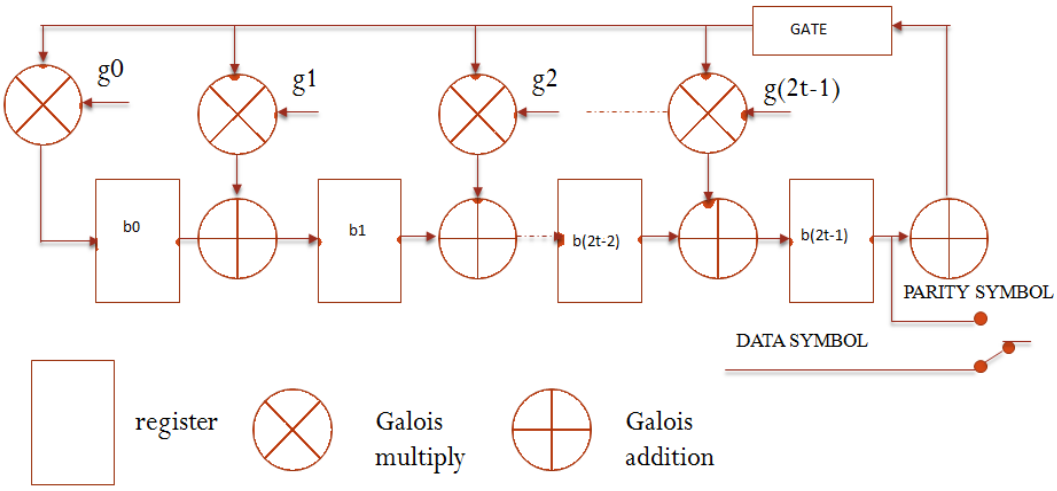

Figure 3.2: Architecture of RS Encoder

3.3.1.2.2 Convolution encoder

A convolutional code is a type of error-correcting code in which Each *m*-bit information symbol (each *m*-bit string) to be encoded is transformed into a *n*-bit symbol, where *m*/*n* is the code *rate* ($n \geq m$) and the transformation is a function of the last *k* information symbols, where *k* is the constraint length of the code.

To convolutionally encode data, start with *k* memory registers, each holding 1 input bit. Unless otherwise specified, all memory registers start with a value of 0. The encoder has *n* modulo-2 adders (a modulo 2 adder can be implemented with a single Boolean XOR gate, where the logic is: 0+0 = 0, 0+1 = 1, 1+0 = 1, 1+1 = 0), and *n* generator polynomials — one for each adder (see figure below). An input bit m_1 are fed into the leftmost register. Using the generator polynomials and the existing values in the remaining registers, the encoder outputs *n* bits. Now bit shifts all register values to the right (m_1 moves to m_0, m_0 moves to m_{-1}) and wait for the next input bit. If there are no remaining input bits, the encoder continues output until all registers have returned to the zero state.

3.3.1.3 Interleaver

Interleaving is a technique commonly used in communication systems to overcome correlated channel noise such as burst error or fading. The interleaver rearranges input data such that consecutive data are spaced apart. At the receiver end, the interleaved data are arranged back into the original sequence by the de-interleaver. As a result of interleaving, correlated noise

introduced in the transmission channel appears to be statistically independent of the receiver and thus allows better error correction.

The interleaving is a 2 step permutation process. The first step ensures that adjacent coded bits are mapped onto non-adjacent subcarriers. The second step ensures that adjacent coded bits are mapped onto LSB or LSB of the constellation map alternatively to avoid long runs of low reliable bits.

The first permutation is given by the equation:

$$m_k = \left(\frac{N_{cbps}}{d}\right).k_{mod(d)} + floor\left(\frac{k}{d}\right)$$

$$k = 0,1 \ldots \ldots N_{cbps} - 1 \qquad d = 16$$

The second permutation is given by the equation:

$$j_k = s.floor\left(\frac{m_k}{s}\right) + (m_k) + N_{cbps} - floor\left(d.\frac{m_k}{N_{cbps}}\right) mod(s)$$

$$k = 0,1 \ldots \ldots N_{cbps} - 1 \qquad d = 16$$

where,

s = $N_{cpc}/2$, N_{cpc} denotes the number of coded bits per sub-carrier (2, 4 and 6 for QPSK, 16-QAM and 64-QAM respectively.)

De-interleaving at the receiver:

Here, the first de-permutation is the reverse of the second permutation.

$$m_j = s.floor\left(\frac{j}{s}\right) + \left(j + floor\left(d.\frac{j}{N_{cbps}}\right)\right) mod(s)$$

$$j = 0,1 \ldots \ldots N_{cbps} - 1 \qquad d = 16$$

The second de-permutation is the reverse of the first permutation.

$$k_j = d.m_j - \left(N_{cbps} - 1\right).floor\left(d.\frac{mj}{N_{cbps}}\right)$$

$$j = 0,1 \ldots \ldots N_{cbps} - 1 \qquad d = 16$$

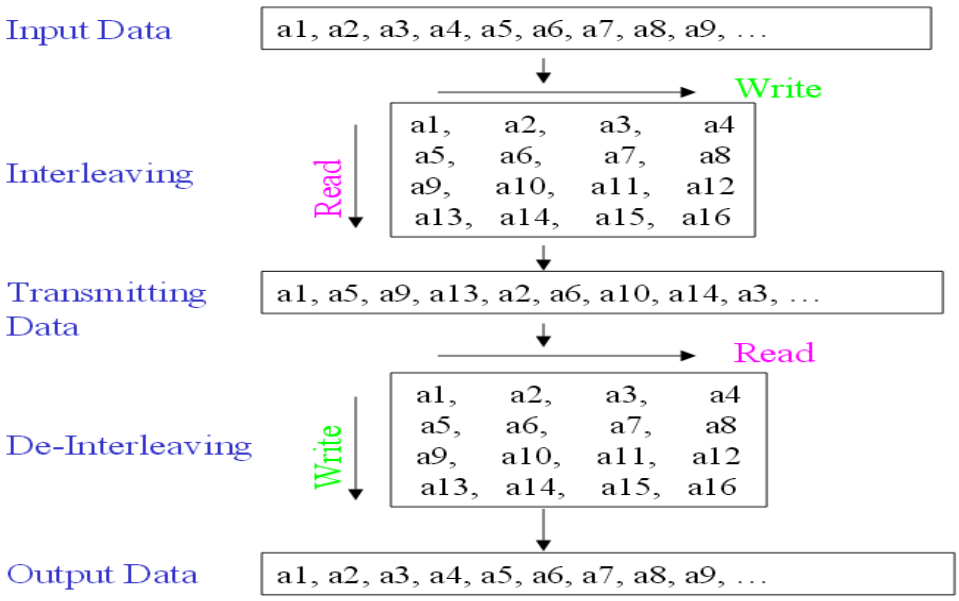

Figure 3.3: Interleaver algorithm

3.3.2 Mapper

A signal constellation is the physical diagram used to describe all the possible symbols used by a signaling system to transmit data and is an aid to designing better communications systems. They help you design a transmission system that is less prone to errors and can possibly recover from transmission problems without relying on higher level protocols.

They also help you visually understand how a particular modulation mechanism works. If you make a chart of all the possible values (symbols) that a modulation system can create during transmission, you end up with what is called a constellation map. When a communications device transmits, it modulates a pattern into the signal being transmitted. That pattern represents information and is called a symbol. Symbols are used to represent sets of zeroes and ones-binary data. Between the transmission point and the reception point, signals can get corrupted. A signal's original output power can be reduced or attenuated by the environment or the signal can get shifted out of phase. The signal can become so corrupted that it becomes unrecognizable, unless the design of the transmission system and the modulation technique take this into account. Designing a modulation system that spreads the symbols apart in such a way that they are not easily confused for one another is just part of designing a communications system. Both the

selection of signal values and the selection of the bits those signal patterns represent are important to the design of the constellation map. The analysis of a transmission systems' constellation map allows the development of error detection and error correction schemes that can detect transmission problems. Below is a constellation map for an eight symbol, three bit system. The green dots represent the values the signal should produce when transmitting the bit patterns shown in black text.

The mapper supports the BPSK, QPSK, 16-QAM and 64-QAM modulation schemes. The constellation mapped data are assigned to the allocated data subcarriers of the OFDM symbol in the order of the increasing frequency offset, where the first mapped data is allocated to the subcarrier with the lowest frequency offset index. In 16-QAM, the symbol rate is one fourth of the bit rate. So this modulation format produces a more spectrally efficient transmission. It is more efficient than BPSK, QPSK, or 8PSK.

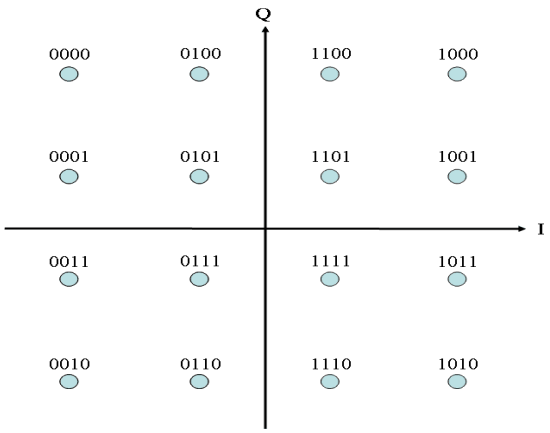

Figure 3.4: Constellation diagram of 16-QAM

3.3.3 Pilot/Guard insertion

The mobile WiMAX frame consists of 48 OFDM symbols. Each symbol time contains actual user data and guard time. The guard time [also known as cyclic prefix (CP)] duration is selected based on the conditions of the wireless channel. As long as the length of CP is longer than the multipath channel delay spread, ISI associated with the fading channel may be eliminated. The basic TDD frame structure as outlined in IEEE 802.16e is partitioned into two subframes: the DL subframe and the UL subframe. The subframes are separated by transmit/receive gaps (TTG) and

receive/transmit gaps (RTG), which are inserted to ensure that the device has an adequate amount of time to switch between transmit and receive modes.

Each subframe begins with control information that indicates how all constituents synchronize and if and when reception and transmission should occur in the given frame. After the control information is transmitted, the BS transmits to the MS in the DL subframe, or the MS transmits to the BS in the UL subframe.

The first OFDM symbol in the DL subframe begins with a preamble. Mobile stations use the preamble to perform synchronization and channel estimation. The frame control header (FCH) follows the preamble, and it specifies to the MS the DL-medium access protocol (MAP) message length, the DL-MAP message coding scheme, and available subchannels. The DL-MAP and the UL-MAP relay information pertaining to channel allocation and other pertinent control information relevant to their respective subframes.

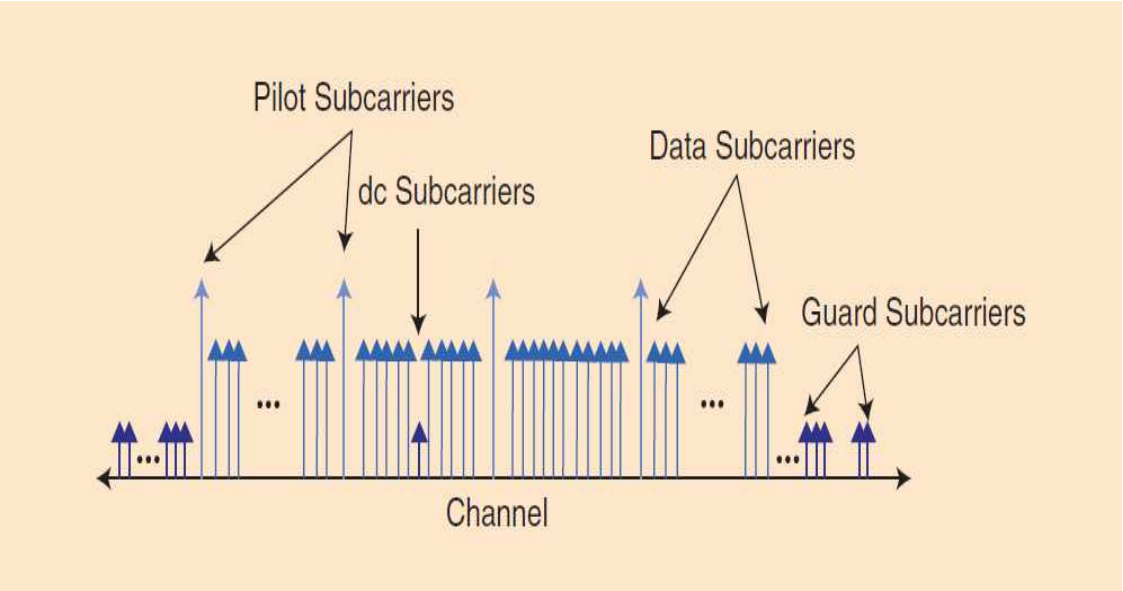

Figure 3.5: OFDMA spectrum division and subcarriers position

3.3.4 IFFT

The OFDM symbol threats the source symbols to perform frequency-domain into time-domain. If we chose the N number of subcarriers for the system to evaluate the performance of WiMAX the basic function of IFFT receives the N number of sinusoidal and N symbols at a time. The output of IFFT is the total N sinusoidal signals and makes a single OFDM symbol. The

mathematical model of OFDM symbol defined by IFFT which would be transmitted during our simulation as given bellow:

$$x_n = \left(\frac{1}{N}\right)\sum_{k=0}^{N-1} x_k \, e^{2\pi.jnk/N} \qquad N = 0,1,2 \ldots \ldots . N-1$$

3.3.5 Cyclic prefix insertion

To maintain the frequency orthogonality and reduce the delay due to multipath propagation, cyclic prefix is added in OFDM signals. To do so, before transmitting the signal, it is added at the beginning of the signal. In wireless transmission the transmitted signals might be distorted by the effect of echo signals due to the presence of multipath delay. The ISI is totally eliminated by the design when the CP length L is greater than the multipath delay. After performing Inverse Fast Fourier Transform (IFFT) the CP will be added with each OFDM symbol.

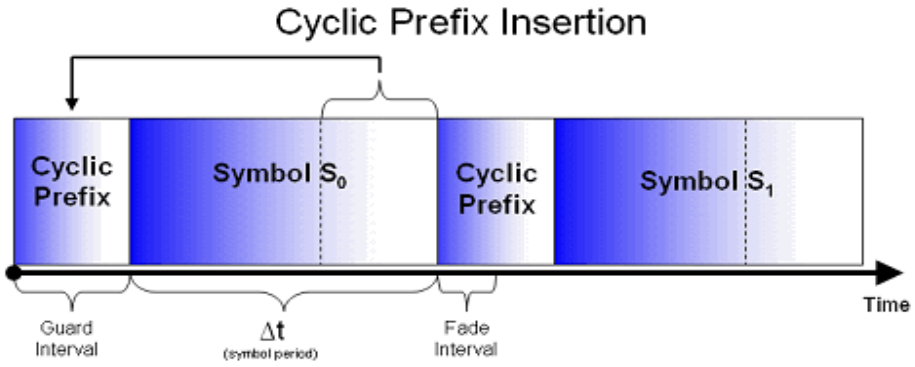

Figure 3.6: Cyclic prefix insertion

3.4 WiMAX PHY Layer Receiver

We can say that the operation of the blocks on the receiver side is somewhat the same but functions in reverse to their corresponding blocks in the transmitter. However, since the receiver has to recover data from a degraded signal so some blocks require more implementation effort, some receiver blocks have to do more processing and consequently. When the antenna detects the signal, it amplifies the signal and passes it to the A/D converter to generate baseband digital samples. Synchronizer: Detects the starting position of an incoming packet based on preambles.

It is extremely important for the synchronize to correctly estimate the OFDM symbol boundaries so that subsequent blocks process an appropriate collection of samples together.

In many implementations, the synchronizer also detects and corrects carrier frequency offset that is caused by the difference in the oscillator frequencies at transmitter and receiver or due to the Doppler Effect. The synchronizer uses the preamble to perform timing and frequency synchronization. There are many different implementations of the synchronizer, most of which involve auto-correlation and cross-correlation. For the synchronizer to support different protocols, it needs to know the preamble structure, the symbol size and the CP size of the protocol. Serial to Parallel (S/P): Removes the cyclic prefix (CP) and then aggregates samples into symbols before passing them to the FFT.

It also propagates the control information from the RX Controller to subsequent blocks. FFT: Converts OFDM symbols from the time domain back into the frequency domain. Channel Estimator: Uses the information from pilots to estimate and compensate for frequency-dependent signal degradation. The channel estimator estimates and corrects the errors caused by multipath interference. Similar to the synchronizer, there are many different algorithms for channel estimation. Many of them use either the preambles or the pilots to estimate the effect of the interference on each data subcarrier. We parameterize the channel estimator by protocol-specific preamble and pilot values. Demapper: Demodulates data and converts samples to encoded bits, which are used by the FEC decoder.

The number of encoded bits generated per sample is determined by the specific modulation scheme. The parameters of this block are modulation schemes supported and the functions for converting the samples to decisions. Deinterleaver: Reverses the interleaving performed by transmitter and restores the original arrangement of bits. FEC Decoder: Uses the redundant information that was introduced at the transmitter to detect and correct any errors that may have occurred during transmission. Both 802.11a and 802.16 uses the Viterbi algorithm [13] to decode convolutionally encoded data. To support multiple protocols, the decoder uses the same parameter settings as the convolutional encoder at the transmitter side. Since 802.16 also uses Reed-Solomon encoding, corresponding Reed-Solomon decoder that supports appropriate profiles is used on the receiver side. Descrambler: Reverses the scrambling performed by the transmitter.

Here only two blocks have been discussed in detail below and rest all are the same as in transmitter side but operate in reverse way.

3.4.1 Reed Solomon decoder

The Reed-Solomon Decoder performs detection and correction of encoded data available at the receiver after demodulation. The RS encoded data is then processed to determine whether any errors have occurred during transmission. Once the number of errors is determined, the decoder decides if they are within the range of correction. After determining this, the decoder corrects the errors in the received data. The figure below illustrates the operation of a Reed-Solomon Decoder.

3.4.2 Viterbi decoder

The function of Viterbi decoder is to decode the bit stream using Viterbi algorithm which has been encoded using a convolutional code. The Viterbi Decoding algorithm is broadly used in Radio communication, Digital TV, Radio relay, Satellite communication and many more applications [4]. The figure 3.7 shows the major components of Viterbi Decoder which are branch metric units (BMU) , add compare select unit (ACSU), survivor-path memory unit (SMU), and path metric unit (PMU).

The branch metrics are calculated from the received channel symbols in BMU which are distances between all the possible symbol codes and data received. Branch matrices are fed into ACS which performs add compare and select operation for all the states. The decision bits produced in ACS are stored and regained from the SMU in order to finally decode the source bits along the final survivor path [4, 5]. The decoded output sequence is determined by tracing back the information from the recorded survivor paths. The core elements of the PMU are ACS units. The path metrics of the current iteration are stored in the path metric unit (PMU) and are read out for use in next iteration [7–9].

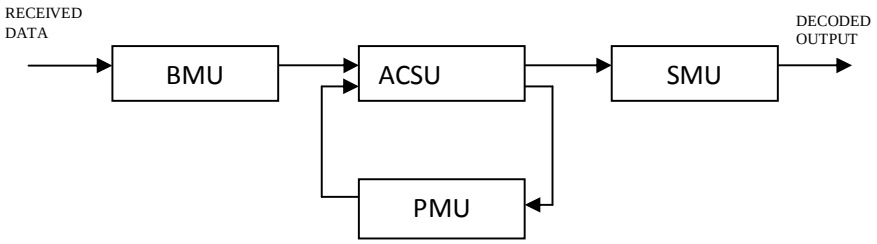

Figure 3.7: Functional diagram of Viterbi Decoder [14]

3.5 Summary

In this chapter, the architecture of the WiMAX physical layer transmitter and receiver has been discussed block wise in detail. The function of each block has been explained briefly with its appropriate diagram wherever necessary.

Chapter 4

IMPLEMENTATION OF DIFFERENT BLOCKS OF WiMAX PHY LAYER BASEBAND PROCESSOR

4 IMPLEMENTATION OF DIFFERENT BLOCKS OF WiMAX PHY LAYER BASEBAND PROCESSOR

WiMAX physical layer transmitter and receiver consist of various essential blocks which have been discussed in this chapter with its detailed theory for better understanding.

4.1 Introduction

The implementation of each block is done according to WiMAX IEEE 802.16-2004 standard. To make it into synthesizable core, a hardware description language known as VHDL is used to translate each block. Here Altera's FPGA has been used for targeting to the EP4SGX70HF35C2 device of the Stratix IV family. The Quartus II 11.0 tool was used for synthesis and for simulating purpose ModelSim Altera Edition 6.6d. The figure 4.1 shows WiMAX PHY Layer baseband processor.

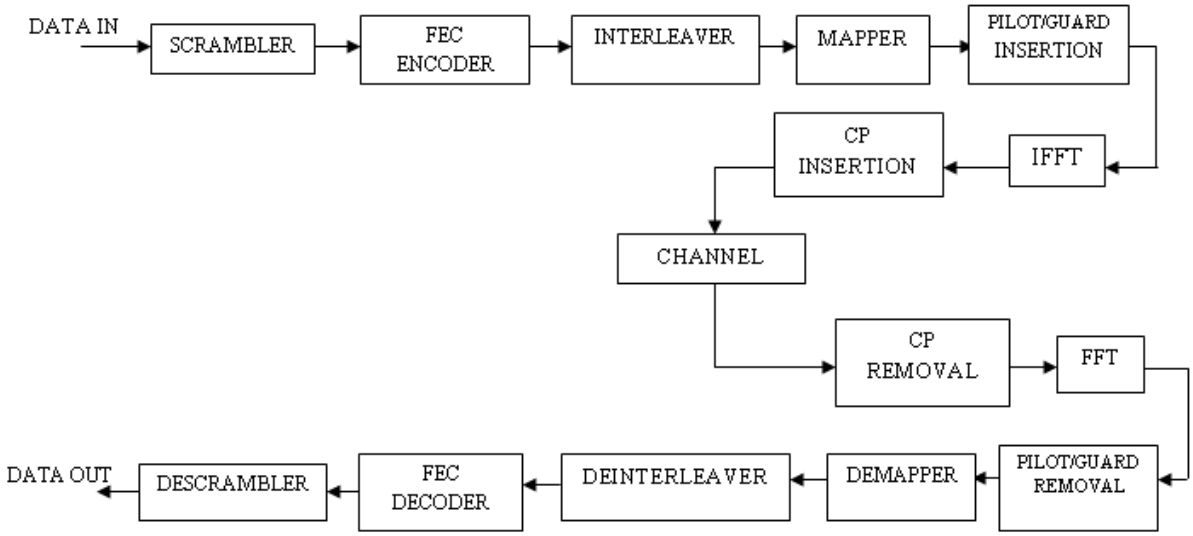

Figure 4.1: WiMAX PHY Layer Baseband processor

4.2 WiMAX PHY Layer Transmitter

In the following section, each block of the transmitting chain will be presented, and the main design features will be highlighted. The transmitter and receiver chain blocks follow the below WiMAX physical layer standard shown in Table 1.

Table 1: WiMAX physical layer standard

	802.16
SCRAMBLER	
shift register size	15 bits
linear function	$x^{15} + x^{14} + 1$
throughput	26.2Mbps
FEC ENCODER(Reed Solomon)	
encoder profile(n, k, t)	(255,239,8)
supported profiles(n, k, t)	(12, 12, 0), (32, 24, 4), (40, 36, 2), (64, 48, 8)
throughput	29.1Mbps
FEC ENCODER(Convolution)	
constraint length	7
supported rates	½, 2/3, ¾, 5/6
generator polynomials	171oct, 133oct
throughput	35Mbps
INTERLEAVER	
block size	192, 384, 768, 1152
throughput	1 block per 33µs
MAPPER	
modulations	BPSK, QPSK, 16-QAM, 64-QAM
throughput	192 samples per 33µs
PILOT/GUARD INSERTION	
pilot indices	-88, -63, -38, -13,13, 38,63, 88
guard indices	-128 to -101, 0, 101 to 127
throughput	256 samples per 33µs
IFFT	
size	256
throughput	256 samples per 33µs
CP INSERTION	
CP size	8,16,32,64
short preamble	4 64-sample symbols
long preamble	2 128-sample symbols
throughput	264 samples per 33µs

The main components of WiMAX transmitter are shown in Figure 4.2. The transmitter chain has a major function of the channel coding block consisting of three blocks: Randomizer, FEC (Forward error correction), and interleave which have been discussed in one subsection and mapper, pilot/guard insertion, IFFT, parallel to serial converter, cyclic prefix insertion is shown in another subsection.

4.3 Channel Coding

The channel coding consists of three blocks-Randomizer, FEC, interleave. The figure 3 shown below presents the components of the channel encoding mechanism for the IEEE 802.16 standard.

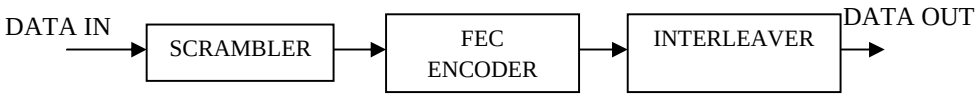

Figure 4.3: Channel Coding

4.3.1 Scrambler/Randomizer

The work of randomization is to randomize the input data on each burst to avoid a long sequence of zeros and ones. The block changes the data at the bit level, where it processes the input data bytes bit by bit, MSB first. The implementation is done with a Pseudo Random Binary Sequence (PRBS) generator that uses a 15 bit linear feedback shift register (LFSR) to represent the generator polynomial of $X^{15} + X^{14} + 1$.

Further in the feedback branch to 2-input XOR gates are used as shown in figure 4.4. This is the required architecture for randomizing the input data according to the IEEE 802.16d.

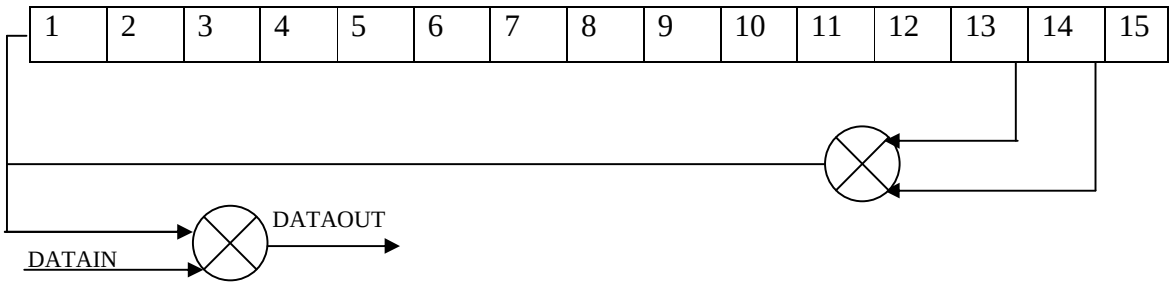

Figure 4.4: Architecture of Randomizer of generator polynomial X^15+X^14+1

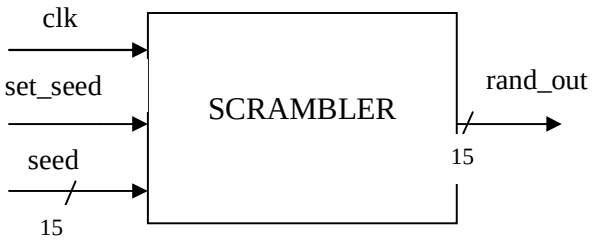

Figure 4.5: I/O Signals of Scrambler

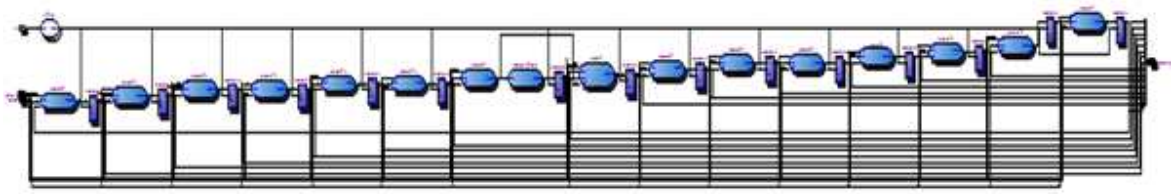

Figure 4.6: RTL Schematic of Scrambler

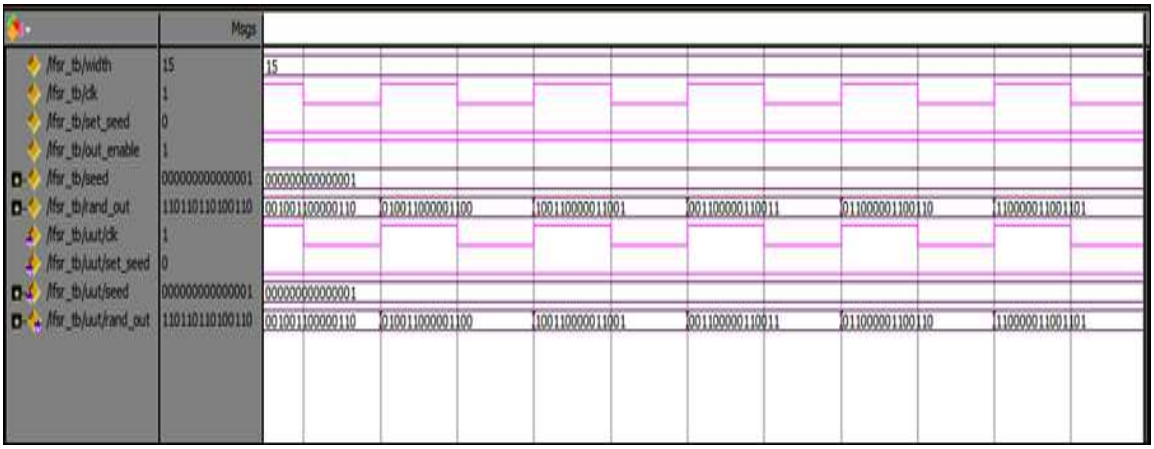

Figure 4.7: Simulation result of Scrambler

Table 2: I/O Signals Description of Scrambler

clk	Input Clock is the main system clock
set_seed	Input signal, when set_seed=1, then register is initialized with the seed value
Seed[14:0]	Data input signal of 15 bits
rand_out[14:0]	Data output signal, the final output after xoring and shifting

4.3.2 Forward Error Correction (FEC)

In a data communication system, forward error correction which is also called channel coding is a process of controlling errors during transmission of data, where the sender adds systematically generated redundant data to its messages, also known as an error-correcting code. This is named as such because it does not require reverse channel for re-transmission of data.

4.3.2.1 RS encoder

The RS-encoder is derived from the RS (N=255, K=239, T=8) code using a Galois Field GF (2^8). N is the number of bytes after encoding, K refers to the number of bytes before encoding and T refers to the number of correctable errors.

The encoder architecture is made using the Linear Feedback Shift Register Design,. The coefficients, $0 \leq i \leq 15$ are derived as each message is accompanied by a pulse signal, which indicates the beginning of a message. The encoder starts concatenating the 16 calculated parities to the message to make a codeword of 255 symbols, after 239 clock cycles.

When the encoder receives data symbols, it generates check symbols for a given codeword and sends the input codeword together with the check symbols to the output interface. The encoder backpressures the upstream component when it generates the check symbols. The field generator polynomial is $p(x) = x^8 + x^4 + x^3 + x^2 + 1$.

And the code generator polynomial is g(x) =$(x - \alpha^i)(x - \alpha^{i+1})$ ... $(x - \alpha^{i+2t})$, where $\propto$ is the primitive element of GF (2^8), its corresponding values can be seen from lookup table.

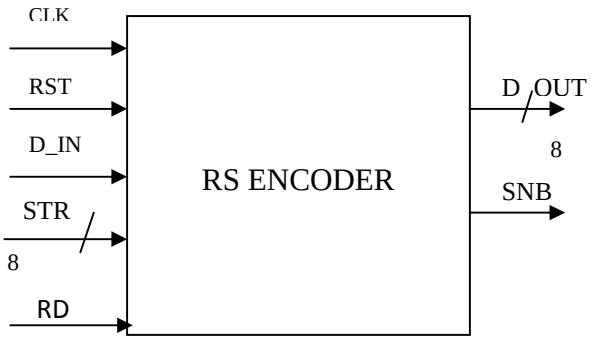

Figure 4.8: I/O Signals of Reed Solomon Encoder

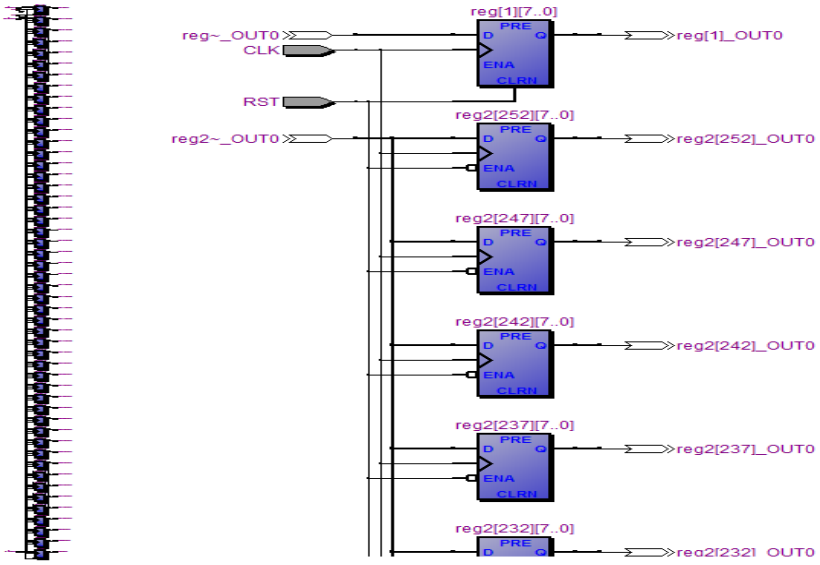

Figure 4.9: RTL of Reed Solomon Encoder

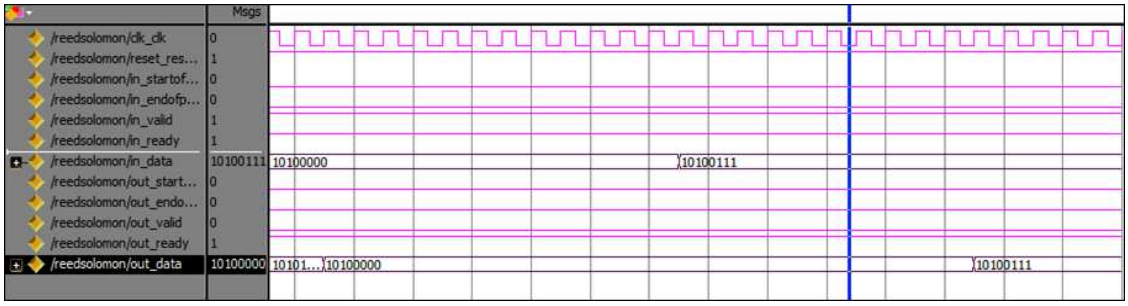

Figure 4.10: Simulation result of Reed Solomon Encoder

Table 3: I/O Signals Description of Reed Solomon Encoder

CLK	Input CLK signal of the module
RST	Input signal, RST=1, it resets all registers
D_IN [7:0]	Input data of 8 bits
STR	Input data start signal
RD	Input Read signal, when RD=1, input data are read
D_OUT [7:0]	Output data of 8 bits
SNB	Output Impulse when the decoding is finished

4.3.2.2 Convolution encoder

The mandatory type of FEC is Tail biting Convolution Coding i.e. the CC register is initialized to the last k-bits of the data in the FEC's input. Here k denotes the constraint length.

Convolution Coding Block:

G1: 171 (octal) for X,

G2: 133 (octal) for Y

The generator sequences G1 and G2 can be derived as below:

Paths which are chosen for binary summation are designated by '1' and those which are not chosen are designated by '0'. Moving from right to left, for X output, the generated sequence will be 1001111. Appending 2 '0' to the right, we get, 100111100. Reading this from right to left, G1 = 171 (octal). Similarly, we can derive G2 = 133 (octal).

The default rate of Convolution Encoding is ½, since for a given input; we get 2 outputs, X and Y. Here u1 and u2 is branch code words.

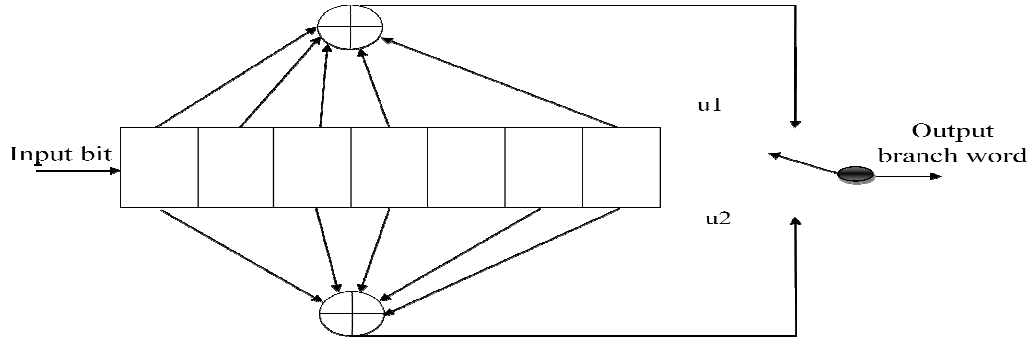

Figure 4.11: Architecture of Convolution Encoder of generator polynomial (171Oct, 133Oct) of code rate ½

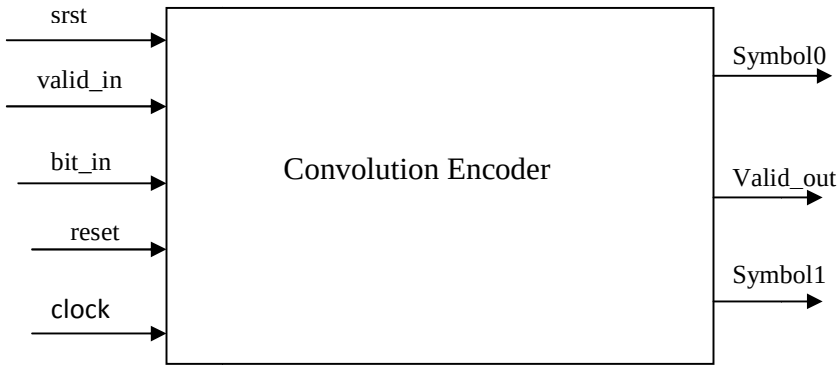

Figure 4.12: I/O Signals of Convolution Encoder

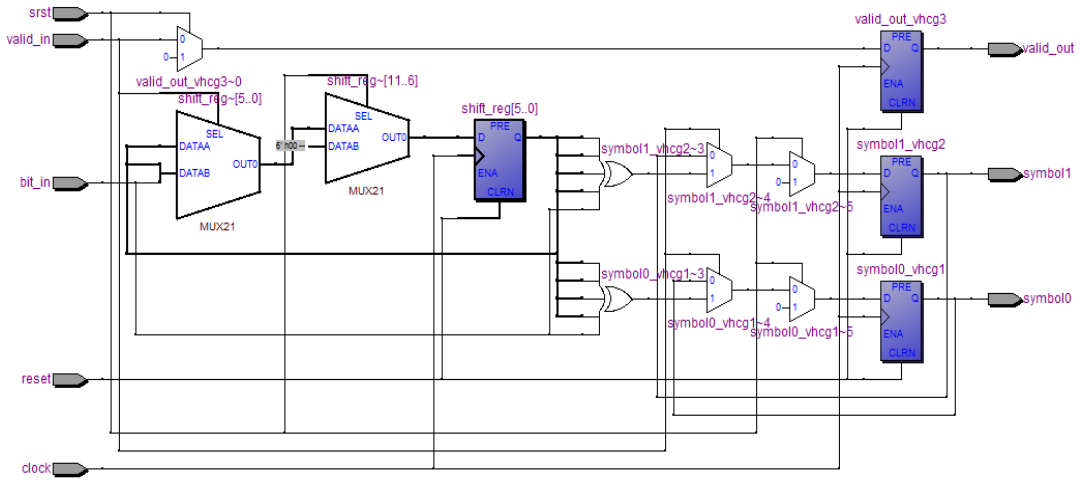

Figure 4.13: RTL Schematic of Convolution Encoder

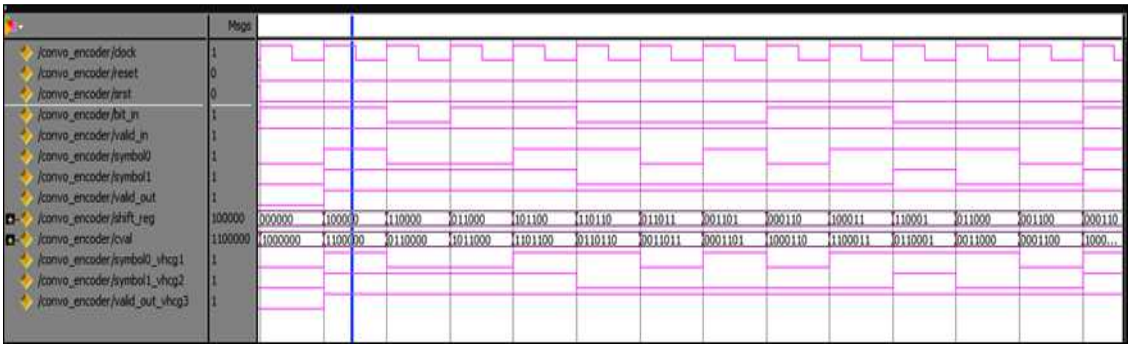

Figure 4.14: Simulation result of Convolution Encoder

srst	Input synchronous reset signal
valid_in	Input signal, which is high when reading input data
bit_in	Input data
reset	Input signal, reset=1 then all contents are 0
clock	Input clock signal
Symbol0 [2:0]	Output signal, 1st codeword
Symbol1 [2:0]	Output signal, 2nd codeword
valid_out	Output signal, it is high when input data are read correctly

Figure 4.15: I/O Signals Description of Convolution Encoder

4.3.3 Mapper

The interleaved bits are serially fed to the constellation mapper to produce the corresponding In phase and Quadrature (I/Q) pairs.

Here 16-QAM mapping scheme has been implemented where 4 bits are mapped into the corresponding I/Q pairs, the mapper receives the serial input stream and groups them into symbol of 4 bits. These bits are used to index a ROM based look-up table that contains the corresponding I/Q pair values. To facilitate the design, each chunk of Ncpc is divided into two parts to address two separate ROMs, one contains the I values while the other contains the Q values. The normalized values are stored in a signed fixed point representation of 16 bits and decimal point at 14. This was selected since all values are less than zero, except the BPSK values that could be either 1 or -1. Thus, to represent the fractional part 14 bits are required and only two bits are required to represent the sign. The 128 mapped I/Q pairs are allocated later to the data subcarriers in the 256 subcarriers forming the OFDM symbol.

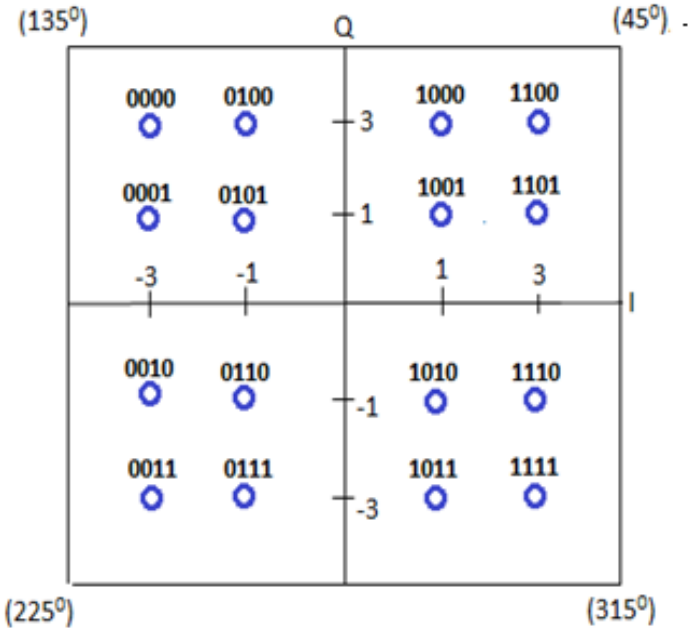

Figure 4.16: 16-QAM Constellation Diagram

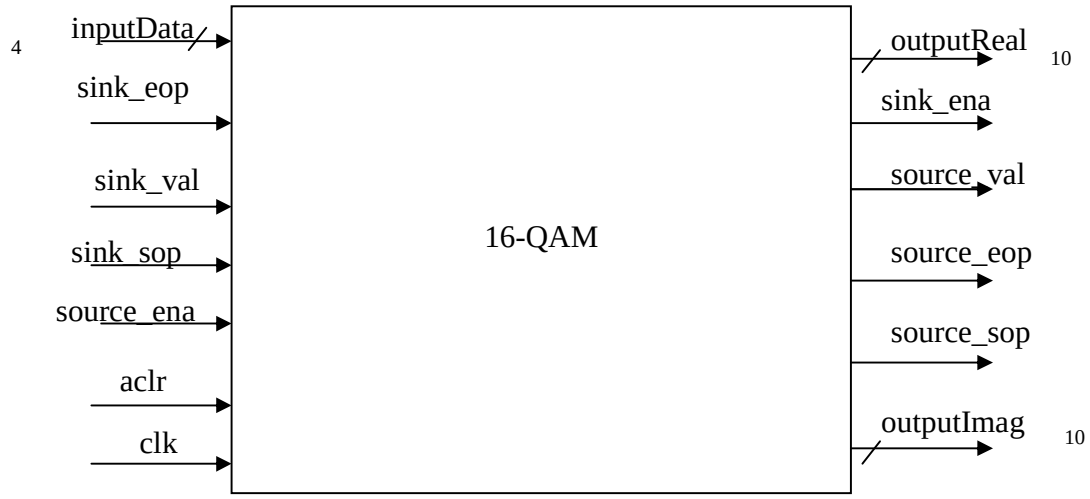

Figure 4.17: I/O Signals of 16-QAM Mapper

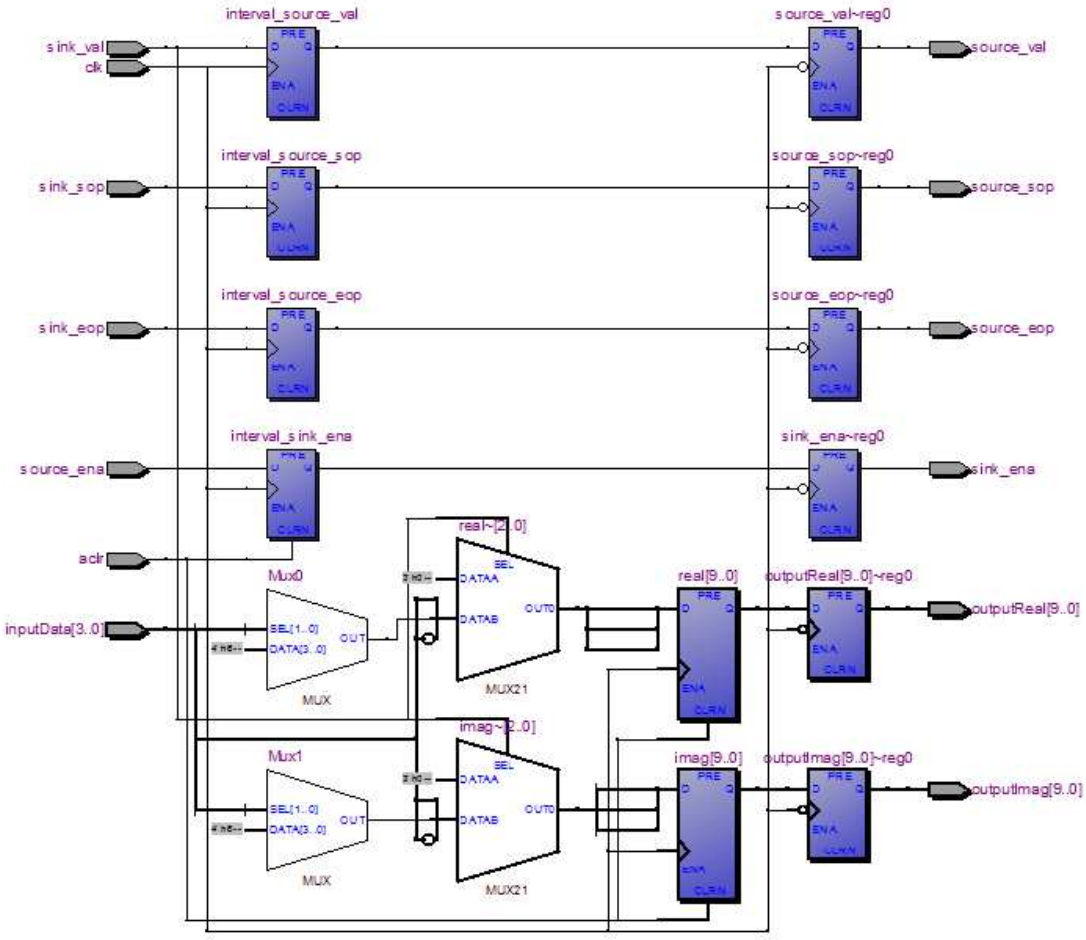

Figure 4.18: RTL Schematic of 16-QAM Mapper

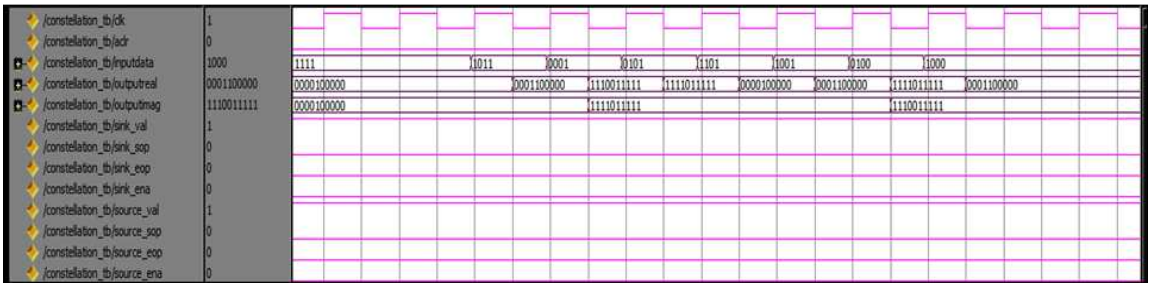

Figure 4.19: Simulation result of 16-QAM Mapper

Table 4: I/O Signals Description of 16-QAM mapper

inputData [3:0]	4bit width input data ports
sink_eop	Input signal showing the end of packet
sink_val	Input signal which is high when reading data
sink_sop	Input signal which shows the start of the packet
outputImag [9:0]	Imaginary output signal
aclr	Asynchronous clear input signal
clk	Clock input signal
outputReal [9:0]	Real output signal
sink_ena	Output enable signal
source_val	The output valid signal is high when reading output data
source_eop	Output signal showing the end of the packet
source_sop	Output signal showing the start of the signal
source_ena	Enable input signal

4.4 WiMAX PHY Layer Receiver

On the receiver side, implementation of Reed Solomon Decoder, Viterbi Decoder and the 16-QAM damper have been done.

4.4.1 Reed Solomon decoder

- Decodes Reed-Solomon code (255, 239) encoded bits.

  - Code word length (n) = 255 symbols
  - Data word length (k) = 239 symbols

- Parity length (2t) = 16 symbols

- Supports shortened codes.
- Symbol size= 8 bits
- Error correcting capability= 8 symbols
- Field generator polynomial p (x) = $p(x) = x^8 + x^4 + x^3 + x^2 + 1$
- Code generator polynomial g (x) =$(x - \alpha^i)(x - \alpha^{i+1})$ ... $(x - \alpha^{i+2t})$, where $\propto$ is the primitive element of GF (2^8), its corresponding values can be seen from lookup table.

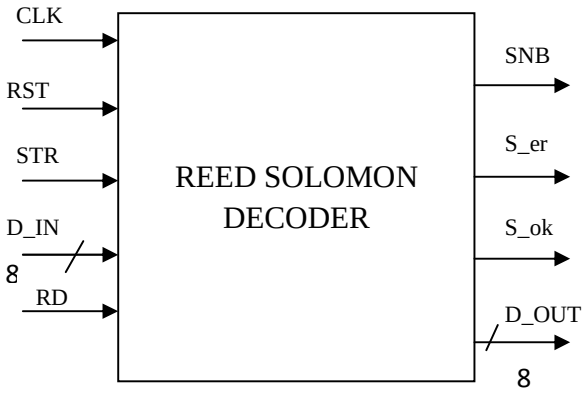

Figure 4.20: I/O Signals of Reed Solomon Decoder

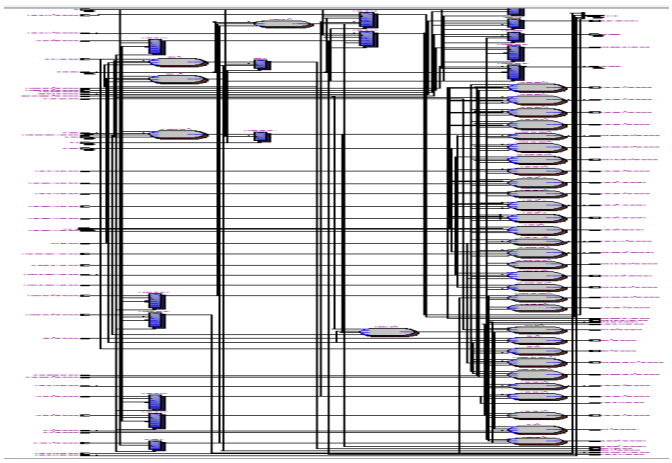

Figure 4.21: RTL Schematic of Reed Solomon Decoder

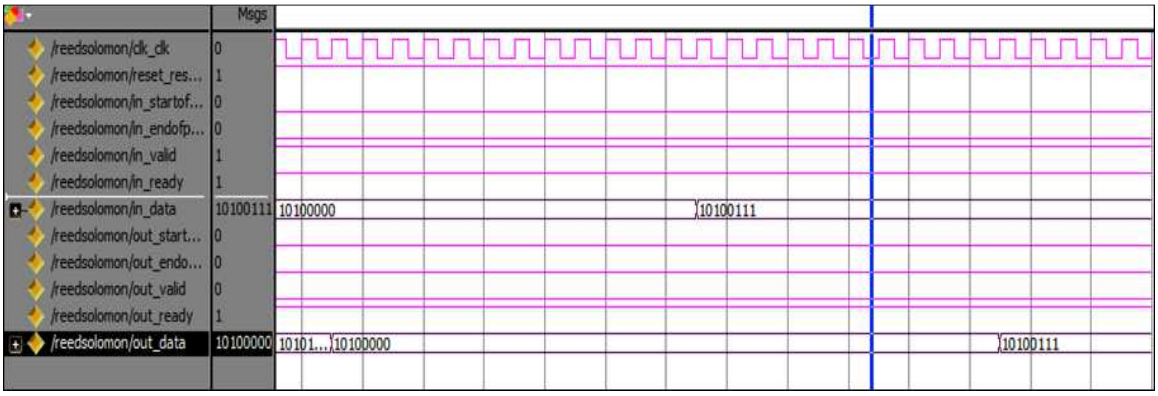

Figure 4.22: Simulation result of Reed Solomon Decoder

Table 5: I/O Signals description of Reed Solomon Decoder

CLK	Input clock signal
RST	Input reset signal, active low
STR	Input start signal
D_IN[7:0]	Input data of 8 bits
RD	Input read signal, high input data is coming
D_OUT[7:0]	Output signal of 8 bits
S_er	Output signal, high when there is an error while reading data
S_ok	Output signal, high when data is read correctly
SNB	Input signal when the decoding is finished

4.4.2 Viterbi decoder

Hardware Viterbi decoder for basic code usually consists of three major blocks:

- Branch Metric Unit (BMU) - used to calculate branch metrics or normed distances between every possible symbol in the code alphabet and the received symbol. This block determines if the decoder is a hard decision or soft decision decoder. A hard decision decoder receives a simple bitstream file on its input and a Hamming distance is used as a metric. Information about the reliability of each received symbol is known when a soft decision decoder receives a bitstream.
- Path Metric Unit (PMU) - used to summarize the branch metrics to get metrics for

2^(k-1) paths where one of the paths will be chosen as the optimal. It is here that the trellis diagram of the code is referenced.

- Traceback Unit (TBU) - used to restore, as close as possible, the maximum likelihood path from the decisions made in the PMU.

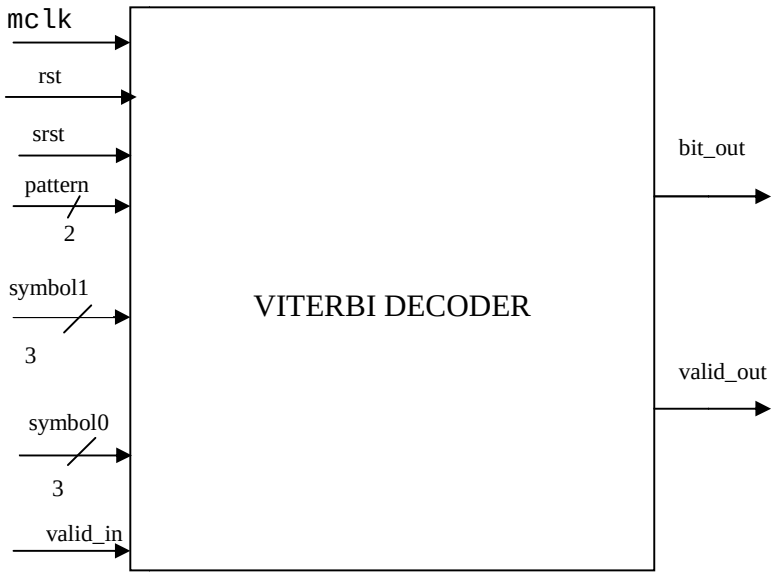

Figure 4.23: I/O Signals of Viterbi Decoder

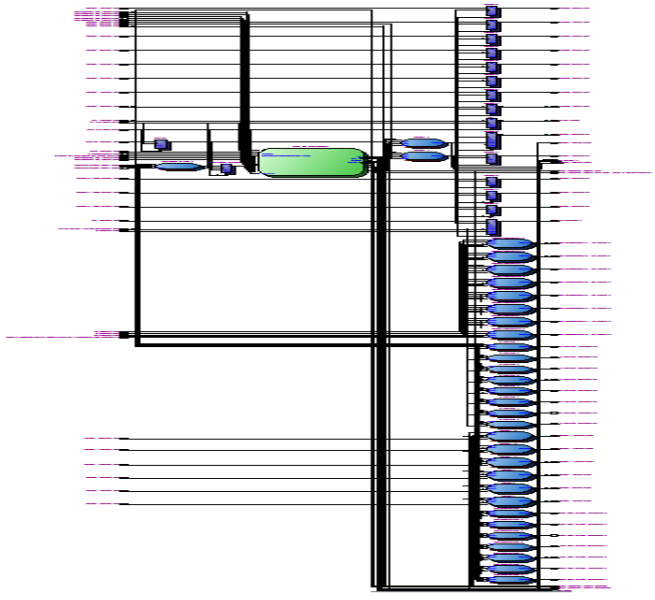

Figure 4.24: RTL Schematic of Viterbi Decoder

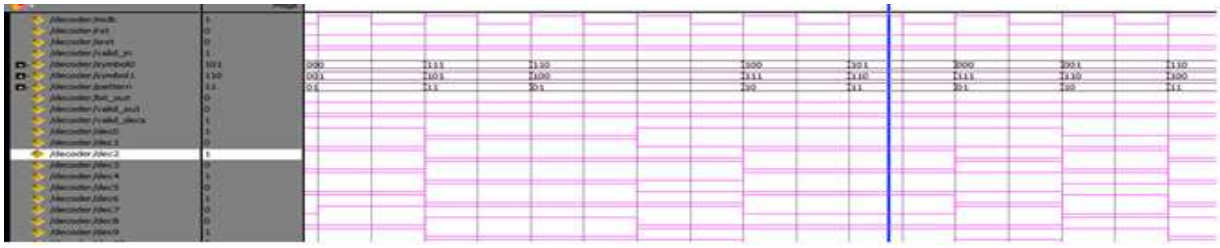

Figure 4.25: Simulation Result Of Viterbi Decoder

Table 6: I/O Signals Description of Viterbi Decoder

mclk	Input clock signal
rst	Input reset, when rst=1, registers are initialized to 0
srst	Input Synchronous reset
valid_in	Input valid signal, high when reads the data
symbol0 [2:0]	Input signals of 3 bits
symbol1 [2:0]	Input symbol of 3 bits
Pattern [1:0]	Input bit pattern
bit_out	Output data signal
valid_out	Output valid signal, high when data is correct

4.4.3 DEMAPPER

The 16-QAM Demmaper has been implemented here. This does the reverse operation as a mapper that is the 4 bits mapped symbol are demapped to bits of streams.

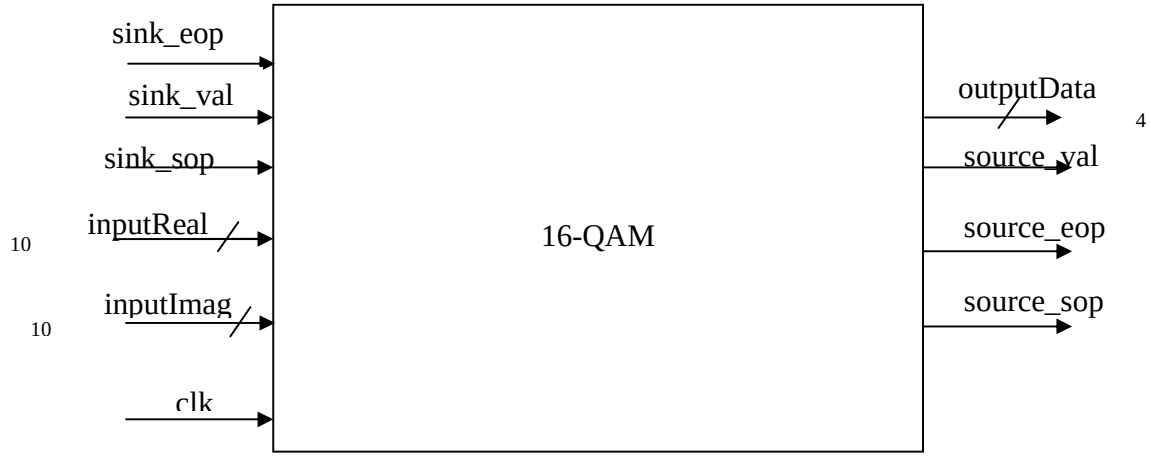

Figure 4.26: I/O Signal of 16-QAM Demapper

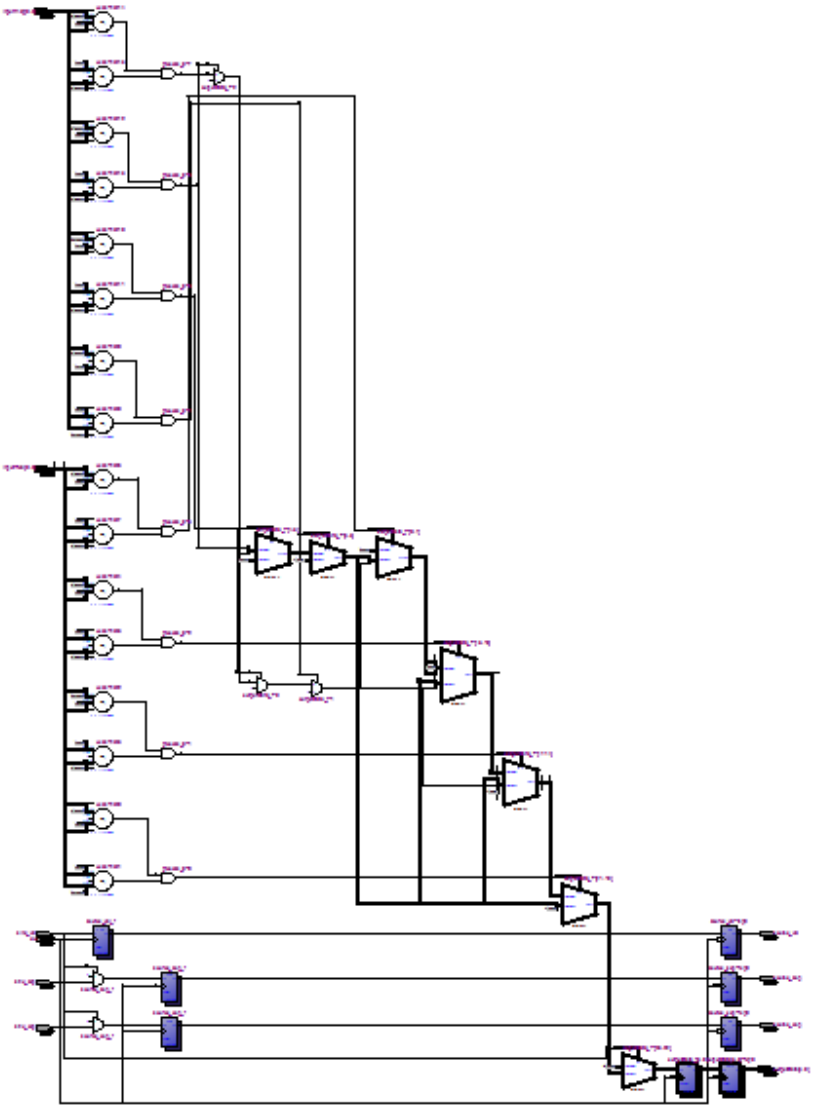

Figure 4.27: RTL Schematic of 16-QAM Demapper

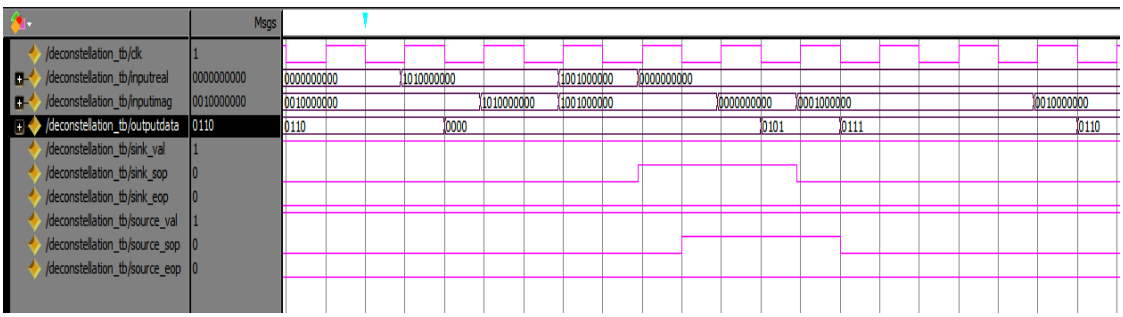

Figure 4.28: Simulation result of 16-QAM Demapper

Table 7: I/O Signals Description of 16-QAM Demapper

clk	Clock input signal
inputReal[9:0]	Input real signal of 9 bits
inputImag[9:0]	Input imaginary signal of 9 bits
outputData[3:0]	Output data signal of 4 bits
sink_val	Input signal which is high when reading data
sink_sop	Input signal showing the start of packet
sink_eop	Input signal showing the end of packet
source_val	Output signal which is high when reading data
source_sop	Output signal showing the start of the packet
source_eop	Output signal showing the end of packet

The following Tables show the Device utilization summary of various blocks implemented on device EP4SGX70HF35C2 of Stratix IV family.

Table 8: (a) Results of Scrambler in Terms of Hardware Utilized,

(b) Results of Reed Solomon Encoder in Terms of Hardware Utilized

Device EP4SGX70HF35C2	Used	Available	Utilization
Nos. of ALUTS	10	58080	<1%
Nos. of dedicated logic register	8	58080	<1%
Total pins	18	584	3%
Nos. of block memory bits	0	6617088	0%

(a)

Device EP4SGX70HF35C2	Used	Avaliable	Utilization
Nos. of ALUTS	2076	58080	4%
Nos. of dedicated logic register	2098	58080	4%
Total pins	21	584	4%
Nos. of block memory bits	0	6617088	0%

(b)

Table 9: (c) Results of Convolution Encoder in Terms of Hardware Utilized,
(d) Results of 16-QAM Mapper in Terms of Hardware Utilized

Device EP4SGX70HF35C2	Used	Available	Utilization
Nos. of ALUTS	10	58080	<1%
Nos. of dedicated logic register	8	58080	<1%
Total pins	18	584	3%
Nos. of block memory bits	0	6617088	0%

(c)

Device EP4SGX70HF35C2	Used	Available	Utilization
Nos. of ALUTS	6	58080	<1%
Nos. of dedicated logic register	34	58080	<1%
Total pins	34	584	6%
Nos. of block memory bits	0	6617088	0%

(d)

Table 10: (e) Results of Reed Solomon Decoder in Terms of Hardware Utilized
(f) Results of Viterbi Decoder in Terms of Hardware Utilized

Device EP4SGX70HF35C2	Used	Available	Utilization
Nos. of ALUTS	11714	58080	20%
Nos. of dedicated logic register	16980	58080	29%
Total pins	23	584	4%
Nos. of block memory bits	2560	6617088	<1%

(e)

Device EP4SGX70HF35C2	Used	Available	Utilization
Nos. of ALUTS	7991	58080	14%
Nos. of dedicated logic register	2523	58080	4%
Total pins	14	584	2%
Nos. of block memory bits	131072	6617088	2%

(f)

Table 11: Results of 16-QAM Demmaper in Terms of Hardware Utilized

Device EP4SGX70HF35C2	Used	Available	Utilization
Nos. of ALUTS	**12**	58080	<1%
Nos. of dedicated logic register	**14**	58080	<1%
Total pins	**31**	584	5%
Nos. of block memory bits	**0**	6617088	0%

4.5 Summary

In this chapter, implementation of scrambler and descrambler, RS encoder and decoder, convolution encoder and Viterbi decoder, 16-QAM mapper and demapper have been implemented showing for each block:

- I/O signals
- RTL schematic
- Simulation result
- I/O signal description
- Device utilization summary

Chapter 5

CONCLUSION AND FUTURE WORK

5 CONCLUSION

- Scrambling and descrambling logic can easily be implemented using very little logic resources.
- This work showed that the STRATIX IV FPGA is efficient in creating complex systems like RS Decoder and Viterbi Decoder and block memory bits used here is much as compared to other encoder.
- Lookup table used in the blocks is very much as compared to complex multiplication and addition in RS Encoder and Decoder logic utilization.

5.1 Future Work

This project is based WiMAX PHY Layer baseband processing blocks which contain transmitter chain blocks and transmitter chain blocks for data communication purpose. As the future work, some of the remaining blocks from both the chain blocks can be implemented according to IEEE 802.16 standards, and then the complete system can be integrated to make the complete system.

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