“GROWTH AND CHARACTERIZATIONS OF SILICON NITRIDE THIN FILM ON SILICON SUBSTRATES”

A Dissertation submitted in partial fulfillment of the requirements for the degree of

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in

PHYSICS

By

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CERTIFICATE

This to certify that the work in the report entitled ***"Growth and Characterizations of Silicon nitride thin films on Silicon substrates"*** by ***Miss Priyambada Pradhan***, in partial fulfilment of Master of Science degree in PHYSICS at the National Institute of Technology, Rourkela, is an authentic work carried out by her under my supervision and guidance. The work is satisfactory to the best of my knowledge.

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Abstract

Silicon nitride thin films were prepared on Silicon p-type substrates using chemical vapor deposition method. Three Silicon nitride samples were taken. One was not annealed while the rest two were annealed at different temperatures. The films are of 250 nm. Two Si_3N_4 samples were annealed at 800 ^oC and 1000 ^oC in a furnace in the presence of N_2. The samples morphological characterizations are done using XRD and SEM. And electrical characterizations are done using C-V. XRD and SEM confirmed its amorphous nature. Electrical properties were found out by capacitance-voltage measurement (C-V).

Keywords: silicon nitride, thin film, chemical vapor deposition, MIS structure, Gate voltage

Introduction

Chapter-1

1.1. Motivation and background

The competitive pressure to produce “smaller, faster, cheaper” microelectronic devices means that reliability must be achieved using only the minimum amount of material, and also the minimum amount of testing. Actual testing of complete devices is the most definitive means to find out whether a design is reliable, and also the slowest and most expensive. Device designer’s use modeling and simulation to substitute for actual testing whenever possible. It seems evident that simulations based on an accurate understanding of the physics and mechanics of the materials involved, and carried out using accurate values of material properties, are more valuable than simulations based on ad hoc schemes and using guessed or estimated properties. The International SEMATECH roadmap has for years included the need for accurate modeling based on actual material properties. The 2003 version includes the statement [1]: Cost effective first pass design success requires computer-aided design (CAD) tools that incorporate contextual reliability considerations in the design of new products and technologies. It is essential that advances in failure mechanism understanding and modeling, which result from the use of improved modelling and test methodologies, be used to provide input data for these new CAD tools. With these data and smart reliability CAD tools, the impact on product reliability of design selections can be evaluated.

Progress is driven by improvements, which are measured by either a more efficient functionality of a technological product or the process of its manufacture. In the semiconductor industry, better performance is marked by higher device speed as well as an increase in the packing density. This increase in density leads to higher circuit complexity, requiring a greater number of interconnects, leading to smaller wire width and spacing. the interconnect delay caused by RC coupling becomes significant. As the feature size decreases, the interconnect delay comes to be the major part of the total delay. The time delay depends on the capacitance between them. The capacitance depends on the metal pitch, which is the sum of the metal width and the spacing in between, the metal thickness and length, and the dielectric constant of the space in between the metal. Other properties of the new interlayer dielectric (ILD) of importance are the dielectric loss, the breakdown voltage, the thermal

stability, thermomechanical characteristics, good adhesion and gap filling ability, low moisture uptake, high thermal conductivity, low leakage current, and finally, low cost.

1.2. Thin film

Thin films of various types are a key component of modern microelectronic and photonic products. Conducting films form the interconnect layers in all chips, and dielectric films provide electrical insulation. With silicon-on-insulator (SOI) and strained silicon, semiconductor films have entered commercial design practice. The term thin films as used here refers to material layers deposited by vapor- or electro deposition, with thicknesses too small to permit characterization by conventional mechanical testing procedures for bulk materials as described in, e.g., ASTM standards. Accordingly, our upper limit of thickness is taken as around 20 μm. Layers in this thickness range formed by other special processes, such as SOI (silicon on insulator) layers, also fall outside the standard mechanical test methods, and require thin-film characterization methods. Copper traces within multi-chip packages may be thicker than the definition given above, but some package designs include films within the present scope. Interconnect layers on die are included in a book on packaging because these layers are often considered to be "Level 0 packaging," since they are part of the packaging chain that connects the active devices to the outside environment electrically, mechanically, and thermally. Thin films of a material set different from those in microelectronic devices are used for MEMS; polycrystalline silicon (poly Si), designed for mechanical functions, is an important MEMS material. The dimensions of films commonly used in microelectronic products have progressed well into the nanoscale at present; and MEMS technology is evolving the ability to produce nano electromechanical systems (NEMS). The elements of these products that are well below 1 μm in thickness challenge the current leading edge of mechanical characterization of thin films.

1.3. Literature Survey

The two main techniques for depositing thin films in wide use today are physical vapor deposition, the category under which methods such as evaporation and sputtering fall, and chemical vapor deposition (CVD). CVD offers many advantages most important of which are low cost and excellent step coverage and uniformity, and has thus become the dominant technique in industry.

The first CVD techniques were employed in the late 1880's to coat thin metallic films onto incandescent filaments [2-4]. The formation of high purity metallic thin films made by chemical transport first received interest at about the same time period, but progress in the CVD field progressed little until the 1930's, when deposition of refractory compounds gained technological importance [5]. In 1960, the replacement of Ge with Si as the main semiconducting material and the development of the planar technology by Hoerni caused a rapid expansion of interest in CVD technology [6]. Further research into chemical vapor deposition processes led to the development of polycrystalline semiconducting films as well as doped amorphous semiconductors, important for the optoelectronics field. Due to technological driving forces, most of the emphasis has been on the evolution of deposition techniques leading to better film quality, less so on the understanding of the basic sciences behind the processes such as thermodynamics, kinetics, or growth and nucleation. Another technique of significance is plasma enhanced CVD (PECVD), which uses plasma instead of thermal activation to impart the necessary energy for the reaction to occur and was first reported in 1965 by Sterling and Swan for the deposition of amorphous silicon, SiO_2, and Si_3N_4 [7]. Desu and Kalidindi addressed the problem of determining the rate controlling step in a CVD process from deposition rate profiles. A regime can be either gas-phase controlled and surface controlled, and knowing which regime is dominant is essential for optimization [8].

1.4. MATERIALS

Materials selection plays a crucial role in the operation and capabilities of a fabricated device. Among the material properties that must be considered: the morphology and crystal structure of each material; thermal and electrical compatibility between materials; and ability to withstand processing conditions without unacceptable degradation. Even after a material has been selected, there is the possibility that a new deposition method or material processing step could result in better device performance. This chapter examines the material properties of the two most significant materials such as silicon and silicon nitride

1.4.1 Silicon

Silicon, a tetravalent metalloid, is a chemical element with the symbol Si and atomic number 14. It is less reactive than its chemical anolog carbon, the non-metal directly above it in the periodic table, but more reactive than germanium. Silicon and gallium arsenide with its related III-V compounds form the basis of the most commonly used semiconductor materials.

Silicon is a semiconductor material with the band gap of 1.12eV. Silicon possesses two of the most outstanding natural dielectrics, silicon dioxide (SiO_2) and silicon nitride (Si_3N_4), which are essential for device formation. In particular, Si_3N_4, which is the basis of the metal–oxide – semiconductor devices (MOS) can be grown thermally on a silicon wafer; it is chemically very stable and can achieve a very high breakdown voltage. Silicon is non-toxic, relatively inexpensive (silicon comprises about 26% of the earth's crust which makes it second in abundance only to oxygen), easy to process (a very well established industrial infrastructure in silicon processing exists around the world), and has quite good mechanical properties (strength, hardness, thermal conductivity, etc.). In a semiconductor with an indirect fundamental energy bandgap, the maximum of the valence band and the minimum of the conduction band are found at different locations in the k-space, therefore energy required for transition is actually more than the bandgap. Recombination by a single photon – which possesses negligible momentum – is not allowed, because of momentum conservation. The properties of silicon and silicon nitride are listed in the table 1.1. The Silicon exhibits a different kind of face-centered cubic structure known as the diamond lattice which is a combination of two face centered cubic unit cells in which one cell has been slide along the main diagonal of the cube one-forth of the distance along the diagonal shown in fig 1.1

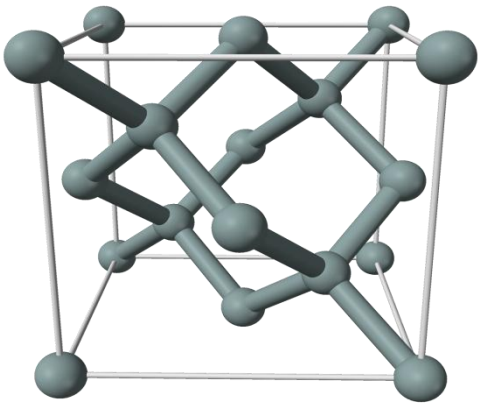


Fig1.1. Silicon crystallizes in a diamond cubic crystal structure

1.4.2. Silicon nitride

Silicon nitride has physical properties desirable to both MEMS designers and the larger research community. A III–V semiconductor, many of its material properties are a result of its close–packed crystal structure. There exist three crystallographic structures of silicon

nitride (Si_3N_4), designated as α, β and γ phases, which are shown in the fig 1.2.and fig 1.3. respectively [9]. The α and β phases are the most common forms of Si_3N_4, and can be produced under normal pressure condition. The γ phase can only be synthesized under high pressures and temperatures and has a hardness of 35 GPa.

The α- and β-Si_3N_4 have trigonal (Pearson symbol hP28, space group P31c, No. 159) and hexagonal (hP14, P63, No. 173) structures, respectively. They can be regarded as consisting of layers of silicon and nitrogen atoms in the sequence ABAB... or ABCDABCD... in β-Si3N4 and α-Si3N4, respectively. The AB layer is the same in the α and β phases, and the CD layer in the α phase is related to AB by a c-glide plane.

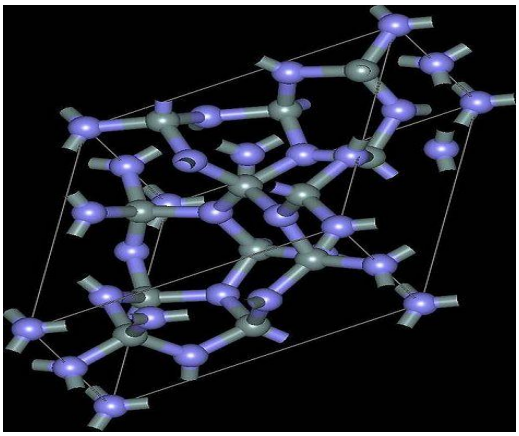


Fig1.2. trigonal α-Si_3N_4.

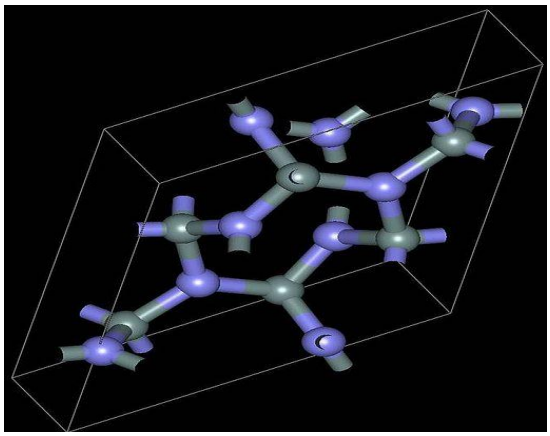


Fig1.3. hexagonal β-Si_3N_4

One of the major applications of sintered silicon nitride is in automobile industry as a material for engine parts. Silicon nitride bearings are both full ceramic bearings and ceramic hybrid bearings with balls in ceramics and races in steel. Silicon nitride ceramics have good shock resistance compared to other ceramics. Therefore, ball bearings made of silicon nitride ceramic are used in performance bearings. A representative example is use of silicon nitride bearings in the main engines of the NASA's Space Shuttle [10-11]. The table 1.1 shows the important material properties of silicon, and silicon nitrides. The robust growth of native oxide on silicon and the strong contrasts in resistivity, dielectric contrast, and thermal conductivity have resulted in the development of a wide variety of MEMS.

Silicon nitride is a man-made compound synthesized through several different chemical reaction methods. The material is dark gray in colour and can be polished to a very smooth

reflective surface. The material is an electrical insulator and is not wet by nonferrous alloys. It is generally amorphous, but the material is much more constrained than the oxide.

Silicon nitride can be obtained by direct reaction between Silicon and Nitrogen at temperatures between 1300 and 1400 °C.

$$3\ Si(s) + 2\ N2\ (g) \rightarrow Si3N4(s)$$

properties	silicon	Silicon nitride
Density (kg m^{-3})	2330	3440
Resistivity (Ω m)	3.2×10^{3}	2.82×10^{6}
Thermal conductivity (W cm^{-1} $°C^{-1}$)	1.24	29
Thermal expansion (°C-1)	2.6×10^{-6}	8.0×10^{-6}
Young′s modulus (GPa)	170	300
Fracture toughness (MPa $m^{-1/2}$)	0.8	0.6

Table 1.1 Material properties of silicon and silicon nitride

1.4.3. Application

The applications of silicon nitrides are given as

1. Silicon nitride used as an insulator and chemical barrier in manufacturing integrated circuit
2. It is also used as a dielectric between polysilicon layers in capacitors in anolog chips. Sintered silicon nitride is used in automobile industry as a material for engine parts.
3. The major application of silicon nitride was abrasive and cutting tools.
4. Bulk, monolithic silicon nitride is used as a material for cutting tools, due to its hardness, thermal stability, and resistance to wear.
5. Sintered silicon nitride can cut cast iron, hard steel and nickel based alloys with surface speeds up to 25 times quicker than tungsten carbide

1.4.4. The Metal-Insulator-Semiconductor (MIS) Structure

A MIS capacitor is a capacitor formed from a layer of metal, a layer of insulating material and a layer of semiconductor material. It gets its name from the initials of the metal-insulator-semiconductor structure. As with the MOS field-effect transistor structure, for historical reasons, this layer is also often referred to as a MOS capacitor, but this specifically refers to

an oxide insulator material. The MOS capacitor consists of a thin film Si_3N_4 layer sandwiched between a Silicon substrates and a metallic field plates, shown in the fig1.4 . The most common field plate materials are Aluminium and heavily doped polycrystalline Silicon. A second metallic layer present along the back or bottom side of the semiconductor provides an electrical contact to the Silicon substrate.

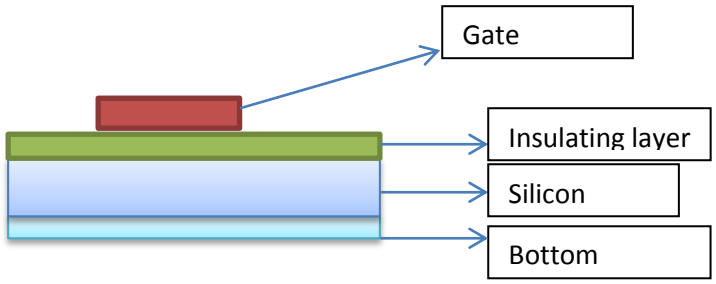


Fig1.4 cross section view of MIS structure

CHAPTER-2

2.1. Fabrication Technology of Silicon Nitride Thin Film

The formation of films on surfaces encompasses an entire field of science and engineering. For the sake of brevity, the discussion below will focus on the deposition methods used in electronic and photonic circuit fabrication, as these are the technologies that are commonly used for MEMS thin film deposition. These methods can be separated into two distinct processes: The two main techniques for depositing thin films in wide use today are physical vapor deposition, the category under which methods such as evaporation and sputtering fall, and chemical vapor deposition (CVD). CVD offers many advantages most important of which are low cost and excellent step coverage and uniformity, and has thus become the dominant technique in industry. So we follow the chemical vapor deposition method (CVD).

2.2. Chemical Vapor Deposition

Chemical vapor deposition (CVD) is a technique used in thin film manufacturing. It is used for depositing materials like amorphous silicon, polysilicon, silicon nitride or silicon dioxide. CVD is also used for depositing different metal such as tungsten (W). The common factor for deposition of these different materials by CVD is that the coating are conformal, can coat a large number of wafers at the same time and good step coverage. The method is based on thermal decomposition and/or reaction of gaseous compounds, and the desire material is deposited directly from the gas phase onto the surface of a substrate.

There is uniform distribution over large area, no compositional gradients across substrate, no need to break vacuum for source changes and more selective area deposition because of higher activation energy for reaction with foreign substances

For depositing these thin films there are number of CVD variation. Three of the most common deposition methods are

2.2.1 Low Pressure CVD

2.2.2 Plasma Enhanced CVD

2.2.3 Atmospheric Pressure CVD

When making the choice between these different deposition methods several things have to be considered; the deposition rate and film uniformity, the electrical and mechanical properties, the substrate temperature, and the chemical composition of the films.

2.2.1 Low Pressure CVD

LPCVD is used to deposit a wide range of possible film compositions with good conformal step coverage. These films include a variety of materials including polysilicon for gate

contacts, thick oxides used for isolation, doped oxides for global planarization, nitrides and other dielectrics. The pressure for LPCVD is usually around 10-1000 Pa while standard atmospheric pressure is 101,325 Pa. If the pressure is lowered from atmospheric pressure to about 100 Pa the diffusion will decrease by almost 1000. That means the velocity of mass transport will decrease meaning the substrates can approach more closely and the deposited films show better uniformity and homogeneity.

Fig.2.1 shows the schematic diagram of the LPCVD. The LPCVD process has a quartz tube placed in a spiral heater that starts with at very low pressure around 0.1 Pa. The tube is then heated to the desired temperature and the gaseous species ("working gas") is applied into the tube at the pressure between 10-1000 Pa. This working gas consists of dilution gas and the reactive gas that will react with the substrate and create a solid phase material on the substrate. After the working gas enters the tube it spreads out around the hot substrates that are already in the tube at the same temperature. The substrate temperature is extremely important and influences what reactions take place. This working gas reacts with the substrates and forms the solid phase material and the excess material is pumped out of the tube. The LPCVD process produces layers with excellent uniformity of thickness and material characteristics. The main problems with the process are the high deposition temperature (higher than 600 °C) and the relatively slow deposition rate.

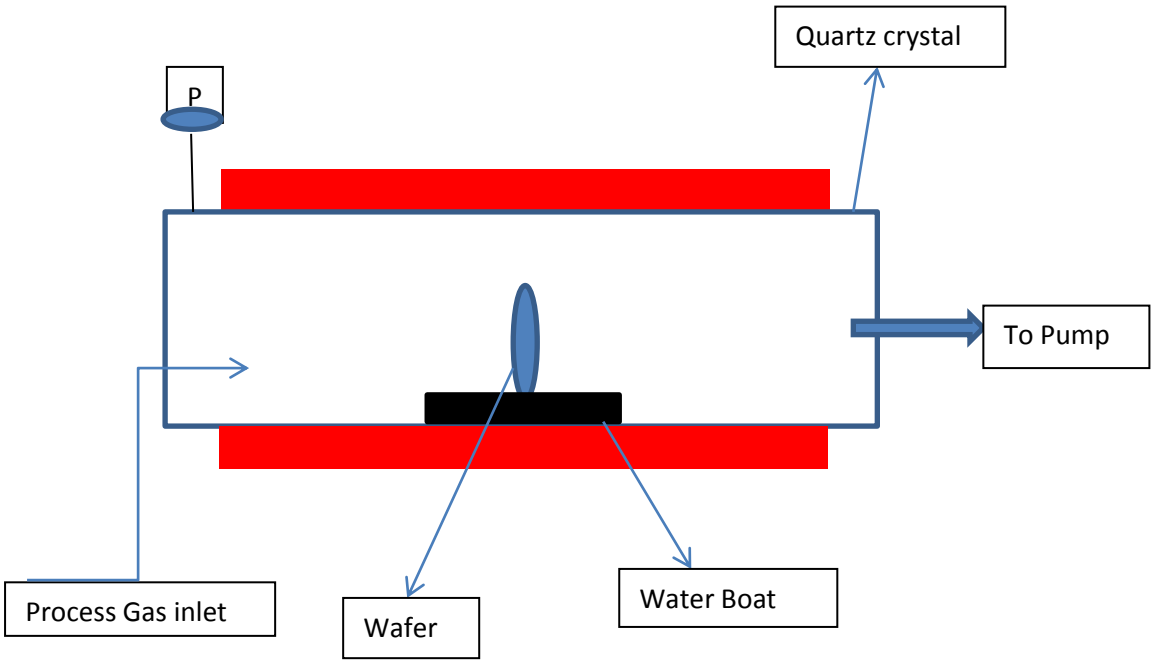


Fig2.1. Schematic diagram of LPCVD

2.2.2 Plasma Enhanced CVD

Fig2.2 shows the schematic diagram of a plasma enhanced chemical vapor deposition. Chemical vapour deposition can take place in a plasma reactor. Because of the formation of plasma, the reaction is take place at low temperatures, typically between 250 ^{o}C to 400 ^{o}C. This is because the plasma is an alternative energy source for the gaseous atom or molecules. In this process, radio frequency (RF) is used to induce plasma in the deposition gas. This results in a higher deposition rate at relatively low temperatures. Plasma is a partially ionized gas with high free electron content (about 50%). Plasmas are divided into two groups; cold and thermal. In thermal plasmas, electrons and particles in the gas are at the same temperature. But in cold plasmas the electrons have a much higher temperature than the neutral particles and ions. Therefore, cold plasmas can utilize the energy of the electrons by changing just the pressure. This allows a PECVD system to operate at low temperatures (between 100 and 400 degree Celsius).

This chemical vapour deposition is an excellent alternative for depositing a variety of thin films at lower temperatures than those utilized in CVD reactors without settling for a lesser film quality.

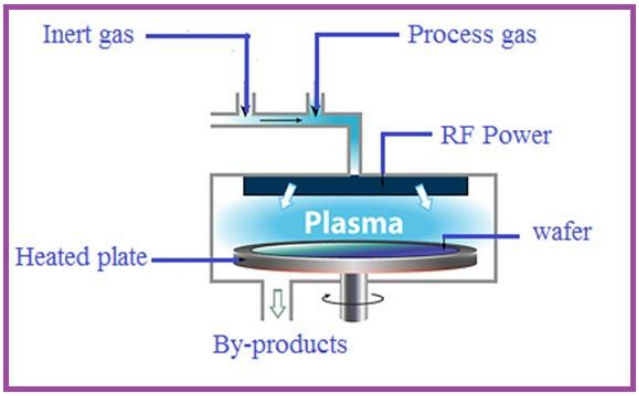


Fig2.2 Schematic Diagram of PE CVD

PECVD systems must contain two electrodes (in a parallel plate configuration), plasma gas, and reactive gas in a chamber. To begin the PECVD process, a wafer is placed on the bottom electrode and reactive gas with the deposition elements is introduced into the chamber. Plasma is then introduced into the chamber between the two electrodes, and voltage is

applied to excite the plasma. The excited state plasma then bombards the reactive gas causing. This dissociation deposits the desired element onto the wafer.

2.2.3 Atmospheric Pressure CVD

APCVD is a simple and high reaction rates process, particularly for the deposition of dielectrics. Because of high deposition rates, it is now most commonly used for deposition of thick dielectrics. For thin layers, LPCVD systems are preferred since they provide much uniformity of the deposited films

APCVD continues reactor is used for deposition of a silicon dioxide passivation layer. In this reactor reactant gases flow through the center section of the reactor and are confined by nitrogen curtain at the ends. Wafer travel from cassette to cassette on a heated chain track. The gases are injected from a showerhead above the wafers. The substrate can be fed continuously through the system, and large diameter wafers are easily handled. The schematic diagram of an atmospheric pressure chemical vapor deposition process is shown in the fig 2.3

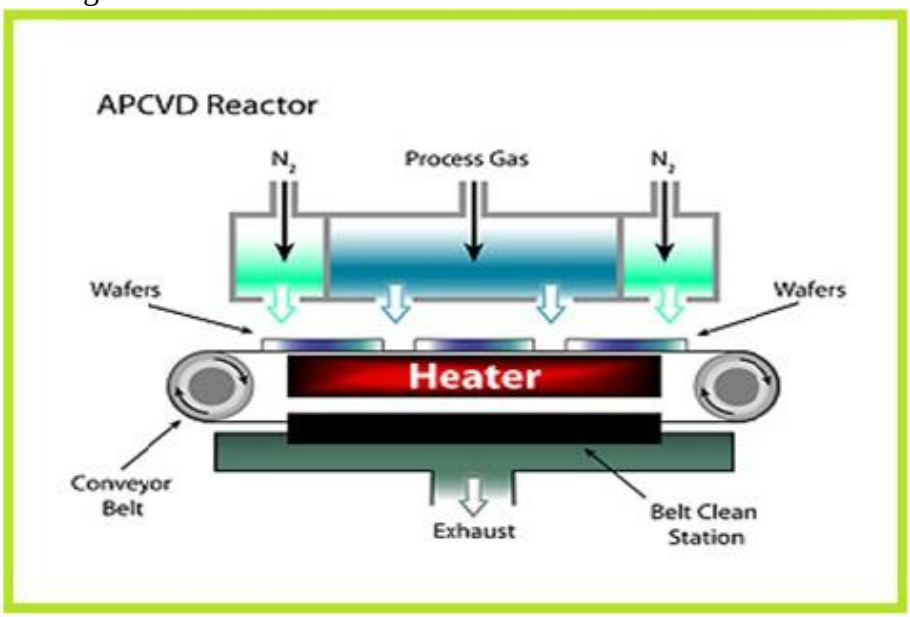


Fig2.3. schematic diagram of an AP CVD

A disadvantage with this type of reactor is that high gas flow rates are required. Temperature may vary from 240 °C to 450 °C. Adding sufficient amount of N2 or another inert gas can control particle formation in the gas phase. But there is also a problem with deposition that occurs at the gas injectors. Even if the growth rate of these particles is low, after a number of

wafers the particles will become large enough to fall on the wafer surface. To avoid this problem, the showerhead may be segmented so as to keep the reactant gasses separated until they are injected into the chamber.

Growth of silicon nitride thin film

Low-pressure chemical vapor deposition (LPCVD) method was adopted for the growth of Si_3N_4 film. A layer of Si_3N_4 film is deposited on the pre-cleaned silicon substrate by simultaneous introduction of dichlorosilane (SiH_2Cl_2) and ammonia (NH_3) into the reaction chamber. The deposition temperature and working pressure were 800 °C and 240 mTorr, respectively.

Chapter 3

3. Characterization Techniques

In order to known the structure, composition, morphology, topography and other various properties of the prepared sample characterization of the sample is necessary. There are many characterization techniques that can give information about the sample. To study the compositional details about the samples generally x-ray diffraction, energy dispersive x-ray spectroscopy, x-ray photoelectron spectroscopy, Auger electron spectroscopy, secondary ion mass spectroscopy, Rutherford back scattering spectroscopy. For the study of morphology of the sample scanning electron microscopy, transmission electron microscopy, atomic force microscopy, scanning tunnelling microscopy are the techniques performed. There are many other techniques also to detect other properties of sample.

In this project work composition and morphology of the samples are detected by using x-ray diffraction techniques and scanning electron microscopy respectively.

3.1 X-ray Diffraction (XRD)

X-ray diffraction is a no-destructive technique that gives detailed information about the chemical composition and crystallographic structure of natural and manufactured materials. X-ray diffraction is used for phase identification of a crystalline material. By this technique the average spacing between the atoms, orientation of the single crystal, size and shape of the crystalline are determined.

For the X-rays to yield useful information about the structure, the wavelength of the incident X-rays should be of the same order of magnitude as the interatomic spacing in the crystal structure. The dominant effect that occurs when an incident beam of monochromatic X-rays interacts with a target material is scattering of those X-rays from atoms within the target material.

The relationship describing the angle at which a beam of X-ray particular wavelength diffracts from a crystalline surface was discovered by The English physicist W.H Bragg and is known as Braggs law

$$n\lambda=2d \sin \theta$$

d = distance between lattice plane

λ = wavelength of X-ray

θ = angle of incidence with lattice plane

n = integer

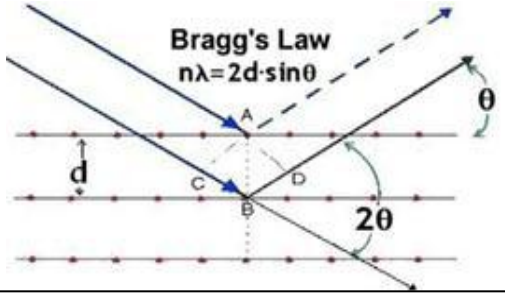


Fig.3.1. X-ray Diffraction for Bragg's condition

X-ray diffraction is based on constructive interference of a crystalline sample and monochromatic X-rays. These X-rays are generated by a cathode ray tube, filtered to produce monochromatic radiation, collimated to concentrate, and directed toward the sample. The interaction of the incident rays with the sample produces constructive interference when conditions satisfy Bragg's Law (nλ=2d sin θ). This law relates the wavelength of electromagnetic radiation to the diffraction angle and the lattice spacing in a crystalline sample. These diffracted X-rays are then detected, processed and counted.

Some applications are:

(1) Differentiation between crystalline and amorphous materials

(2) Determination of the structure of crystalline material

(3) Identification of crystalline phases and measurement of the relative proportions

(4) Measurement of various kinds of order and disorder, and imperfections in crystals.

3.2 Scanning Electron Microscopy (SEM)

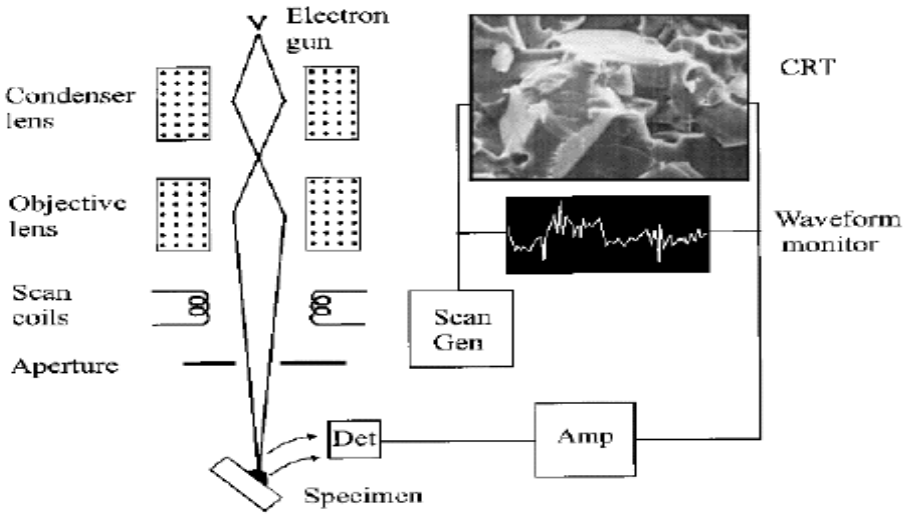


Fig3.2. schematic Diagram of scanning electron miscrope

Scanning electron microscopy uses a focused electron probe to extract structure and chemical composition point by point from a region of interest of sample. The electron beam is generally scanned in a raster scan pattern and the beam's position is combined with the detected signal is to produce an image.

In SEM, an electron beam is thermionically emitted from an electron gun fitted with a tungsten filament cathode, shown in the fig3.2. The electron beam which typically has an energy ranging from 0.2 keV is focused by one or two condenser lenses to a spot about 0.4 nm to 5 nm in diameter. The beam passes through pairs of scanning coils or pairs of deflector plates in the electron column, typically in the final lens, which deflect the beam in x and y axes so that it scan in a raster fashion over a rectangular area of the sample surface.

In SEM the surface of a material utilizes signals of two types, secondary and back scattered electrons. Secondary electrons are a result of the inelastic collision and scattering of incident electrons with specimen electrons. They are generally characterized by occurring energy of less than 50 eV. Backscattered electrons are a result of an elastic collision and scattering between incident electrons and specimen nuclei or electrons. Backscattered electrons can be generated further from the surface of the material and help to resolve topographical contrast and atomic number contrast with a resolution of greater than 1 μ.

SEM can achieve resolution better than 1 nanometer. Specimen can be observed in high vacuum, low vacuum and in environmental Scanning electron microscopy specimens can be observed in wet conditions.

3.3. Capacitance-Voltage Measurement (C-V)

C-V (capacitance-voltage) measurements are used in studying gate-oxide quality in detail. These measurements are made on a two-terminal device called a MOS capacitor, which is basically a MOSFET without a source and drain. From the C-V data many MOS device parameters, such as oxide thickness flatland voltage, threshold voltage, etc., can be extracted.

For the study of the samples, electrical contacts were made using silver paste on the two faces of each sample. The structure is made similar to a MIS capacitor .The area of the silver paste electrode is approximately circular and its diameter is about 2 mm. C-V measurement was performed using Agilent LCR meter by applying a DC bias

C-V measurements in a semiconductor device are made by using two simultaneous voltage sources.(1) An applied AC voltage signal, (2) DC voltage that is swept in time, shown in the fig3.3.

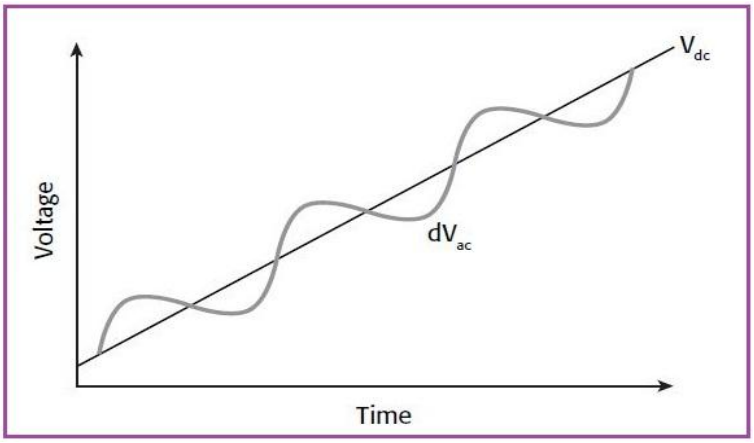


Fig.3.3. voltage versus swept

The capacitance measurement can be performed at a given depth in the device due to the AC voltage bias, which provides the small signal bias. The capacitance of MOS capacitor changes with an applied DC voltage .As a result, the modes of operation of the MOS capacitor changes as a function as a function of the applied voltage. If a DC voltage is applied to the gate, it causes the device to pass through accumulation, depletion, and inversion regions, which are shown in the fig.3.3.1.

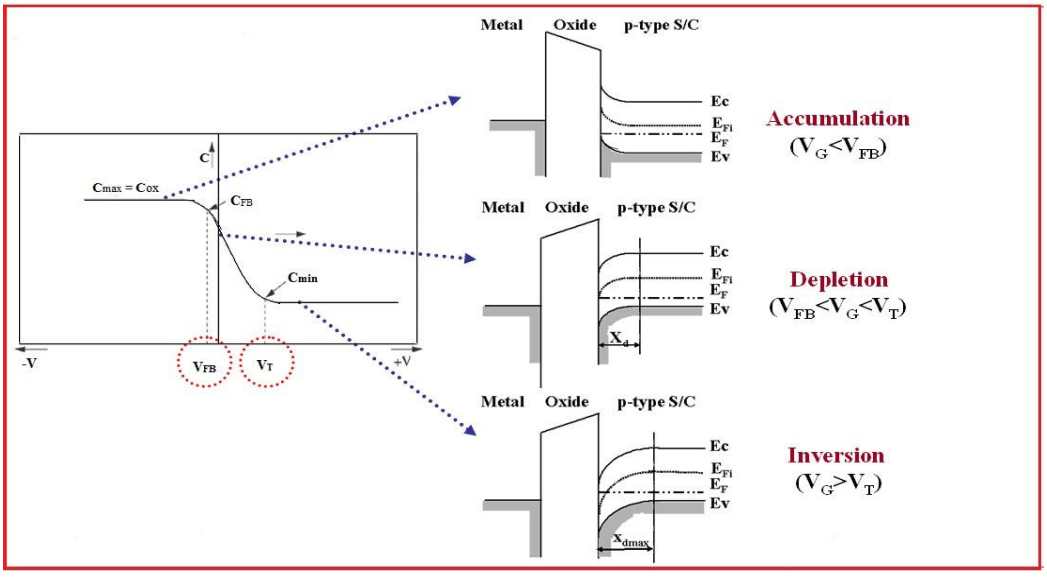


Fig3.3.1 capacitance-voltage curve for P-type semiconductor showing different regions such as accumulation, depletion, and inversion

4.3.1 Accumulation region

A p-type semiconductor has holes, or majority carriers, in the valance band, with no voltage applied. More holes will appear in the valance band at the oxide-semiconductor interface when a negative voltage is applied between the metal gate oxide and semiconductor. This is because the negative charge of the metal causes an equal net positive charge to accumulate at the interface between the oxide and semiconductor. In p-type semiconductor, this state is called accumulation.

4.3.2 Depletion Region

The majority carriers are replaced from the semiconductor-oxide interface when a positive voltage is applied between the gate and semiconductor. The surface of the semiconductor is depleted of majority carriers so this state of semiconductor is called depletion. It can no longer contain or conduct charge so this area of semiconductor acts as dielectric. In this effect it becomes an insulator

4.3.3 Inversion Region

If the gate voltage of p-type MOS-C increases beyond the threshold voltage then dynamic carrier generation and recombination move toward net carrier generation so the positive gate voltage generates electron-hole pairs and attracts electrons towards the gate. These minority carriers accumulate at the substrate to oxide because the oxide is a good insulator. The carrier polarity inverted so the accumulated minority carrier layer is called the inversion layer.

Chapter 4

4. Results and Discussions

4.1 X-ray diffraction (XRD)

Fig. 4.1 shows the X-ray diffraction pattern of grown sample at different annealing temperature. In each case similar nature of the curves are observed. The sharp prominent peak corresponds to the (400) orientation of crystalline silicon substrates, whereas the weak peak corresponding to (200) orientation of silicon substrate. The absence any other peak confirms the amorphous nature of Si_3N_4 film. The amorphous phase of Si_3N_4 depicts the absence of grain in the grown film. The presence of grain boundaries usually provides a path for the transport of charge carriers which is not seen here.

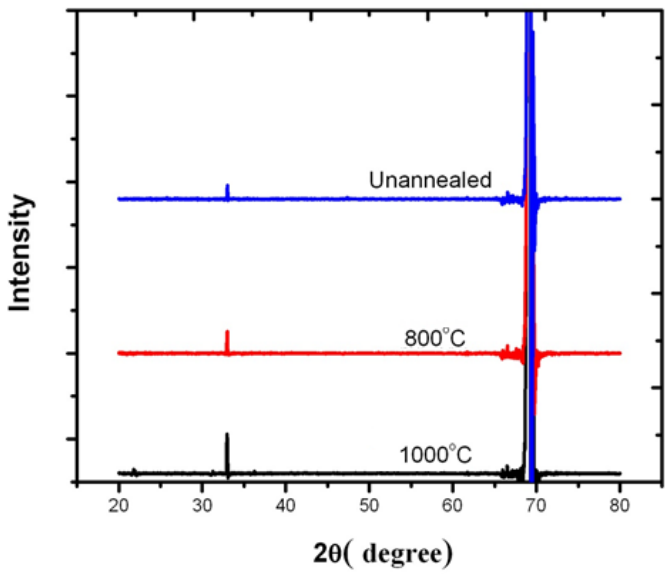
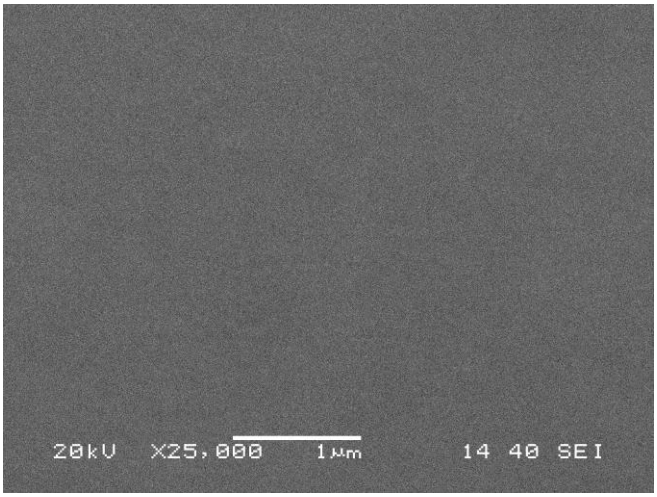


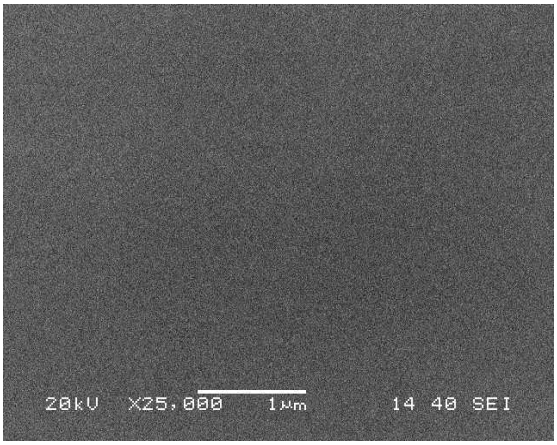
Fig. 4.1 XRD plot of Si_3N_4 unannealed sample and annealed at 800 ^oC, 1000 ^oC

4.2 Scanning Electron Microscope (SEM)

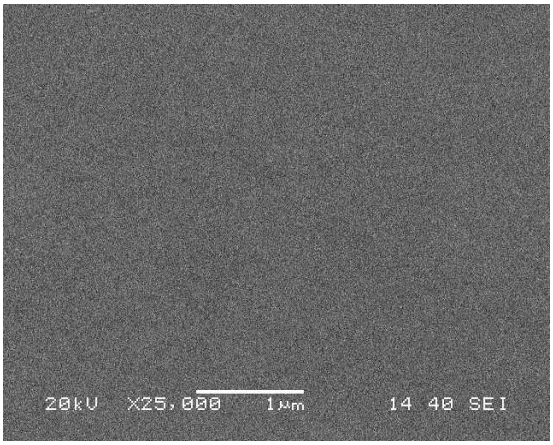
Fig.4.2 shows the SEM images Si_3N_4 of (100-200 nm). The morphology is uniform and homogeneous without any surface modulation. There is no formation of particulates and grains during thermal oxidation, which gives rise to an amorphous phase with smoother surface.



Silicon Nitride unannealed



Silicon Nitride 800 ^{0}C



Silicon Nitride 1000 ^{0}C

Fig. 4.2 SEM images of Si_3N_4 samples annealed in 800 ^{o}C, 1000 ^{o}C and unannealed

4.3 capacitance-voltage measurement

Three regions namely accumulation, depletion and inversion are clearly observed from C-V plot (Fig. 4.3) Maximum Capacitance is obtained in the accumulation region and the type of silicon substrate is p-type. The C-V curves shifted towards zero voltage with increase in annealing temperature, which shows the reduction in bulk charge densities. This may be due to the annihilation of defects, during annealing. In addition, the stretch out of the C-V curve is more for unannealed sample and decreases with annealing, which depicts the decrease in interface trapped density. The interface trapped density decreases due to the reduction of dangling bonds or unsaturated bonds at the thin film/semiconductor interface

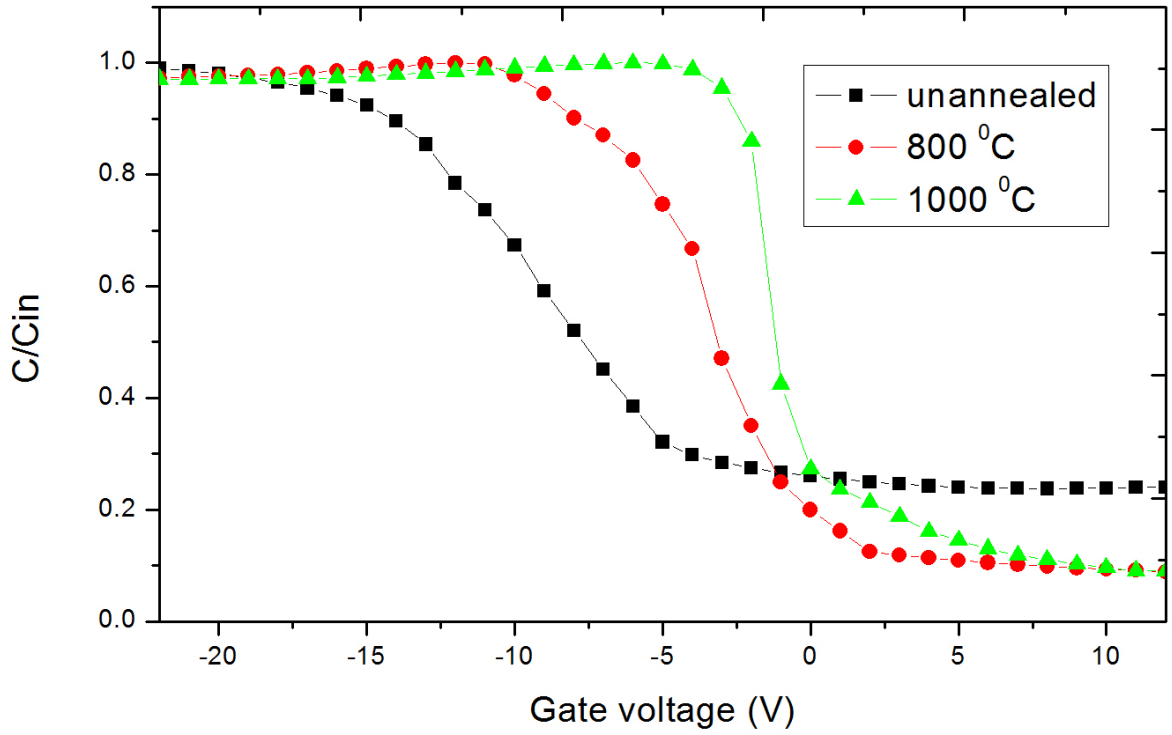


Fig. 4.3 C-V plot of Si_3N_4 unannealed sample and annealed at 800 ^oC, 1000 ^oC

Chapter-5

5.1. Conclusion

Si_3N_4 thin films were prepared on p-type silicon substrates using chemical vapor deposition method. Three Si_3N_4 samples were taken. One was not annealed while the rest two were annealed at different temperatures. The average film thickness was found to be around 250 nm. Two Si_3N_4 samples were annealed at 800 ^oC and 1000 ^oC in a furnace in the presence of N_2. The morphological characterizations of the samples are done using XRD and SEM. In addition electrical properties of the thin films are evaluated by using C-V technique. XRD and SEM confirmed its amorphous nature. The stretch out of the C-V curve is more for unannealed sample. The stretch out of the curve decreases with annealing, which depicts the decrease in interface trapped density

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