Digital Pulse Width Modulation Generation Using 8051 for DC DC Buck Converter

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Digital Pulse Width Modulation Generation Using 8051 for DC DC Buck Converter

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by

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NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA

CERTIFICATE

This is to certify that the report entitled, '**Digital Pulse Width Modulation (DPWM) Generation Using 8051 for DC-DC Buck Converter** ' submitted by **Gajanan S Shirnewar** to the Department of Electrical Engineering, National Institute Of Technology, Rourkela, India, during the academic session 2012-2013 for the award of the degree of **Master of Technology** in **"Control & Automation"** specialization, is a bona-fide record of work carried by him under our supervision and guidance. The thesis has fulfilled all the requirements as per the regulations of this institute and in our opinion reached the standard for submission.

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Declaration

I, **Gajanan S Shirnewar**, declare that:

1. The work contained in this report is original and has been done by me under the guidance of my supervisors Dr. Susovon Samanta & Dr. Supratim Gupta
2. The work has not been submitted to any other Institute for any degree or diploma.
3. I have followed the guidelines provided by the institute in preparing the report.
4. I have conformed to the norms and guidelines given in the Ethical Code of Conduct of the Institute.
5. Whenever I have used materials (data, theoretical analysis, figures and text) from other sources, I have given due credit to them by citing them in the text of the report and giving their details in the references.

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Finally, I dedicate this thesis to my family: my dear father, my dearest mother who supported me morally despite the distance that separates us. I thank them from the bottom of my heart for their motivation, inspiration, love they always give me. Without their support nothing would have been possible. I am greatly indebted to them for everything that I am.

Abstract

DC-DC converters with digital control techniques gained popularity due to their high efficiency, low power consumption, higher immunity to environmental changes such as temperature and aging of components,, ability to interface with digital systems, ease of programmability and to implement sophisticated control schemes. Their applications include portable electronic devices such as cellular phones and laptop computers and others.

The research on digital control of DC-DC converters is mainly focused on two areas. One is the methods to generate digital PWM (DPWM) signals to meet the output voltage requirement precisely. Various techniques have been developed to meet the requirement of output voltage and at the same time it is also necessary to get more resolution to increase precision. The other is to develop new control methods that can utilize the advantages of the digital controller so as to improve the dynamic performance of the switching power converters.

The objective of this thesis is to study current techniques of DPWM generation and to develop new techniques using 8051 for low cost implementation. In this thesis a new way is proposed for PWM generation, which uses the Timers and Interrupts of 8051. Motivation behind selecting 8051 microcontroller is its low cost and ease of programming, despite its disadvantages, like low clock frequency (33 MHz for 89C51RD2, which in internally divided by 12), no inbuilt ADC or DAC. Initially different techniques are validated in NI Multisim environment and also the proposed method is validated on the same platform for a dc-dc buck converter. This thesis also compares the designed new approach with the delay line method of DPWM generation with simulation result. The delay line method is also implemented in 8051 for comparison with the new designed method.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

The electronics industry is going to see a phenomenal growth in the near future, with the rising technological advancements. The digital technology revolution has enabled the industry to earn profit from the growing interaction of digital applications like CD Players, DVD Players / Recorders, hi-fi systems, home theatre, in-car entertainment systems, portable digital audio, mobile phones, pagers, PDAs, laptops, televisions and video recorders. With these technological advancements, the global consumer electronics industry generated billions of revenue. These devices require different operating voltages and currents as per their specifications and application. For that a voltage regulator is needed to automatically maintain the regulation for specific product. This voltage regulation can be done by the two following methods,

1) Linear Regulator
2) Switching Regulator

1.1.1. Linear Regulators

The resistance of the regulator varies in accordance with the load resulting in a constant output voltage. The regulating device is made to act like a variable resistor, continuously adjusting a voltage divider network to regulate output voltage, and continually dissipating the difference between the input and regulated voltages as waste heat. Simple linear regulators may only contain a Zener diode and a series resistor; more complicated regulators include separate stages of voltage reference, error amplifier and power pass element. Fig 1.1 shows typical diagram of linear regulator. Despite easiness of linear regulator, the key problem is its efficiency.

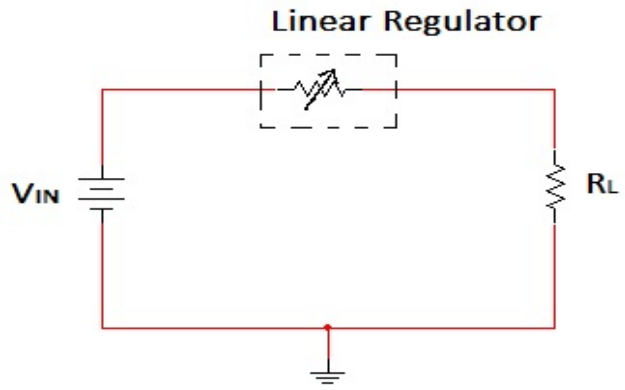


Fig. 1.1 Linear Regulator

1.1.2 Switching Regulators

The switching regulators are increasing in popularity because they offer the advantages of higher power conversion efficiency and increased design flexibility. A switching regulator works by taking small portion of energy, part by part, from the input voltage source, and moving them to the output. This is accomplished with the help of an electrical switch and a controller which regulates the rate at which energy is transferred to the output hence they called "switching regulator".

The energy losses involved in moving portion of energy around in this way are relatively small, and the result is that a switching regulator can typically have 85% efficiency. Since their efficiency is less dependent on input voltage, they can power useful loads from higher voltage sources.

Fig. 1.2 schematic diagram shows a very basic switching regulator called buck converter. The output voltage of buck converter is less than the input voltage and is used to step down the input voltage at desired level. Here the regulation is done by using simple switches (with ideally no on resistance or very low on resistance). These switches goes ON and OFF at a fixed rate called as switching frequency, to keep the output at desired level. The output of DC-DC buck converter is given as

$$V_{OUT} = V_{IN} * \frac{T_{ON}}{T_{SW}} \qquad \ldots\ldots\ldots \qquad (1.1)$$

Where, T_{ON} = is on time or duty cycle of the PWM signal

T_{SW} = is period of PWM signal

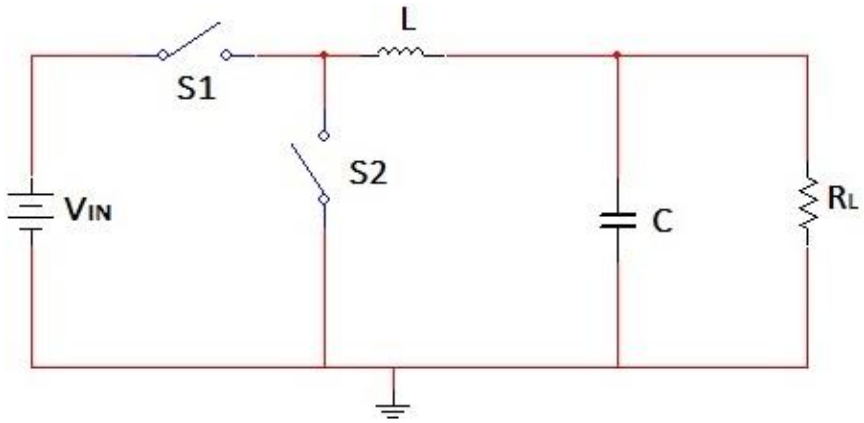


Fig 1.2 Basic schematic of buck converter

It can be seen from equation (1), the output of DC-DC buck converter is function of T_{ON}, for a fixed input voltage at fixed switching frequency. The output maximum voltage can be equal to V_{IN} if T_{ON} is same as T_{SW} i.e. at 100% duty cycle, hence the output can be controlled by controlling the width of PWM signal to the switches of DC-DC converter.

1.2 Digital Controllers

The primary advantages of digital control over analog control are higher immunity to environmental changes such as temperature and aging of components, increased flexibility by changing the software, more advanced control techniques and reduced number of components. As a result of the dramatic scaling of digital technology, digital power management controllers could offer reduced power and die area in to implement them, hence digital controller require reduced size. Certainly, digital controllers also have some technical limitations. Most significantly, there is delay associated with the sampling process and discrete-time computation. Another issue associated with digital controller implementations is the possibility of undesirable non-linear system behavior. Fig 1.3 shows the block diagram of digitally controlled DC-DC converter operating in Voltage Mode Control.

1.3 Objective

In this thesis different types of generation techniques for PWM are studied. The main objective of this thesis is to realize low cost and efficient implementation of DPWM

generation, exploiting various function modules of microcontroller. This is achieved by implementing a very

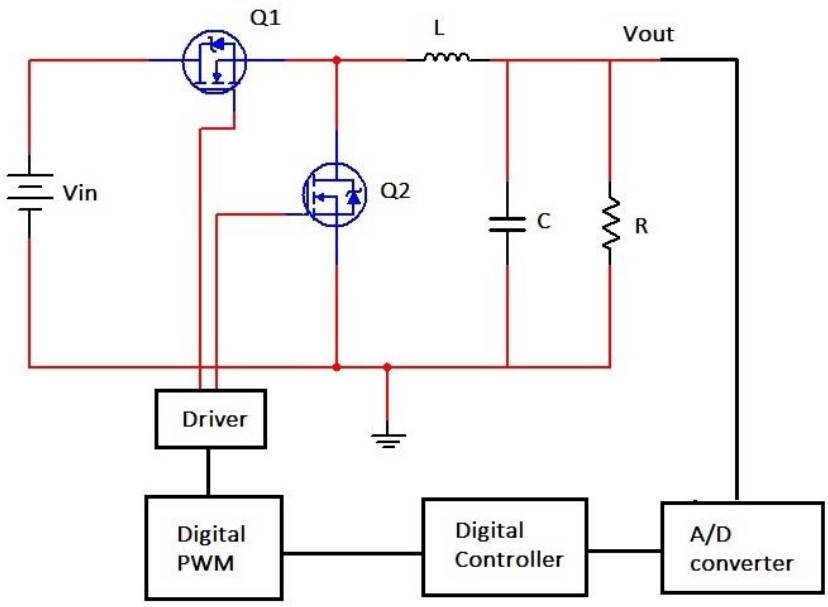


Fig 1.3 Block diagram of digitally controlled Buck converter

new logic in 8051, which has very basic structure of microcontrollers and the cost is also low. This thesis is also meant to compare the designed method with the existed methods to checks its efficiency and performances.

1.4 Thesis Structure

In order to analyze and check the performance of DPWM generation techniques, for a DC-DC converter the proper design of power stage parameters of DC-DC buck converter are necessary. Chapter 2 discusses designing of parameters viz. L, C, R of DC-DC buck converter.

Chapter 3 presents the basic principle of Pulse Width Modulation (PWM). It also discusses present techniques of PWM generation in analog as well as digital domain. In this chapter the basics of microcontroller and its way of exploitation for PWM generation also included.

Chapter 4 gives simulation results of the designed PWM generation technique. The simulation results are obtained for DC-DC buck converter whose L, C, R are designed in Chapter

2. Chapter 4 also covers the comparison of two PWM generated techniques on 8051 platform, for DC-DC buck converter.

At last Chapter 5 contains conclusion to the thesis. Scope of future work extending the study further is suggested in this chapter.

CHAPTER 2

POWER STAGE DESIGN

This chapter explains the formulation of power stage for a buck converter. It also explains the relation of the ripple current and the ripple voltage with inductor L, capacitor C. The section helps in selection of MOSFET.

2.1 Basic Configuration of a Buck Converter

Figure 2.1 shows the basic configuration of a buck converter with two Metal Oxide Semiconductor Field Effect Transistors **(**MOSFETs), which act as switches. This type of buck converter is called synchronous buck converter. Some converters have low side MOSFET (which is connected to ground) replaced by a diode, this type of converter is called as a synchronous buck converter.

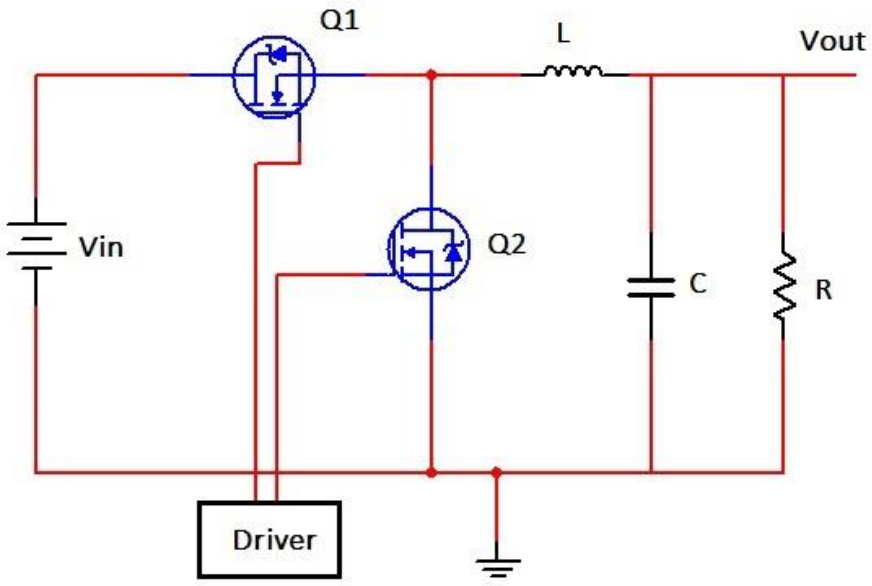


Figure 2.1 Basic configuration of a buck converter with two MOSFETs

To calculate the power stage component values following, following parameters are necessary,

1. Input voltage: V_{IN}
2. Nominal output voltage: V_{OUT}
3. Maximum output current: I_{OUT} (max)

From fig 2.1 it can be inferred that, the LC output filter is acting like a element that receives a voltage square wave at its input (the switching node, indicated in Figure 2.1 with an arrow), and produces a constant voltage at its output (the regulated output voltage V_{OUT}) by filtering the square wave that is presented at its input.

2.2 Selecting the Inductor

The property of an inductor is to resist the change in current passing through it. In buck converter, MOSFETs switches at high speed. Hence current will be discontinuous at output of switches, but inductor over wits this problem. In the ON state an electric current flows in the circuit and energy is stored in the inductor (charging). As soon as the switch is turned off, the inductor produces magnetic fluxes and releases the stored energy. At steady state condition**,** the average current in the inductor I_L is equal to the output current I_{OUT}.

Figure 2.2 represents the inductor current vs. time in CCM (Continuous Conduction Mode, i.e. the inductor is never fully discharged and its current never reaches zero). As can be seen, the inductor current is not constant, but varies around I_{OUT} between a maximum and a minimum value, whose difference ΔI_L is the peak-to-peak inductor current ripple.\

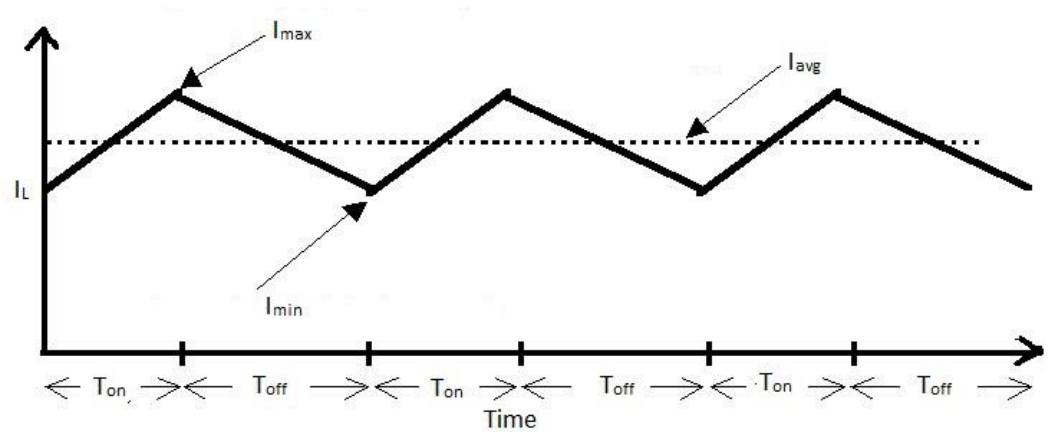


Fig 2.2 inductor current vs. time in CCM

The first step to select the power inductor is to define an acceptable inductor current ripple ΔI_L at the application level. From there, the inductance value can be calculated as follows:

$$L = \frac{(V_{IN} - V_{OUT}) * V_{OUT}}{V_{IN} * F_{SW} * \Delta I_L} \quad \ldots\ldots\ldots (2.1)$$

Where

- V_{IN}: converter's input voltage (in V)
- V_{OUT}: converter's output voltage (in V)
- F_{SW}: converter's switching frequency (in Hz)
- L: inductance (in H)
- ΔI_L: peak-to-peak inductor current ripple (in A)

As established from the formula above, larger values of L allow smaller values of ΔI_L , which results in lower output voltage ripple (see next section, "Selecting the Capacitor"), better efficiency, and better EMC behavior, but slower load transient response. Therefore, selecting the right inductance is a trade-off between the different factors. Choosing ΔI_L to be between 20% and 40% of I_{OUT} is typically a viable choice [4].

When selecting a power inductor from one of the various manufacturers, the inductance is not the only parameter to consider. Another important parameter is the saturation current I_{SAT} of the inductor, which should never be exceeded in the application. Operating the inductor above I_{SAT} would cause a significant inductance loss and a steep increase of the inductor current during the charging phase.

2.3 Selecting the Capacitor

The function of the capacitor is to keep a constant output voltage and limit voltage at the output. Both the ESR (equivalent series resistance) and capacitance have an influence on the output voltage. The best practice is to use low-ESR capacitors to minimize the ripple on the output voltage.

For a certain peak-to-peak output voltage ripple ($\Delta V_{OUT,\ RIPPLE}$), the required maximum ESR of the output capacitor can be calculated by using the following equation [5]

$$ESR = \frac{\Delta V_{OUT,RIPPLE}}{\Delta I_L} \qquad \text{..... (2.2)}$$

where, ΔI_L is the inductor current ripple and the minimum output capacitance can be estimated with the following equation [5]

$$C_{OUT} = \frac{L * \left(I_{L,\ MAX}\right)^2}{\left(V_{OUT} + \Delta V_{OUT,\ OVERSHOOT}\right)^2 - V_{OUT}{}^2} \qquad \text{..... (2.3)}$$

where $\Delta V_{OUT,\ OVERSHOOT}$ is the maximum voltage overshoot allowed on the output, and $I_{L,\ MAX}$ is the maximum inductor current.

Due to the internal ESR, this RMS current produces power dissipation and a temperature increase of the capacitor itself. Since excessive temperature negatively affects the reliability and the lifetime of a capacitor, an output capacitor with an adequate current rating should be selected.

To achieve better output voltage filtering, low-ESR capacitors are required. Ceramic capacitors offer very low ESR.

2.4 Selecting the MOSFET

Figure 2.1 shows the power stage of DC- DC Converter. The MOSFET Q1 High Side MOSFET, Q2 is the Low Side MOSFET. Basically both MOSFETs have to withstand the input voltage. The MOSFETs also have to have a capability to handle additional voltage spikes caused by parasitic inductances. The maximum current seen by both MOSFETs is the output current plus 50 % of the ripple current. Since both MOSFETs are switched dynamically their power dissipation results partly out of the static losses contributed by the on resistance and the current and partly out of the switching losses [6]. The MOSFET should be chosen which satisfy above criteria the voltage and power rating of MOSFETs can be obtained from its datasheet.

Once the power and voltage rating criteria is satisfied and the operating conditions of the system have been determined (load current, frequency, Vout, etc.), the choices for the power MOSFET are as the following:

1. The value of $R_{DS\ (on)}$ .The lower the value, the less dissipation and the better the power stage will work.
2. Heat Sink. If space is available, external heat sinks can achieve the same results as a lower $R_{DS\ (on)}$ at a lower cost.
3. The rise and fall time for MOSFET. By the thumb rule, the time required to on & off a MOSFET, should be 100 times less than the switching period of the power stage.
4. The shoot through immunity. The lower the Qgd/Qgs ratio in the low-side MOSFET, the more robust the synchronous buck will be to dV/dt shoot-through. A ratio of < 1 is a good indicator.

2.5 Selecting the ADC

The ADC converts analog signal in to digital data. These days many advanced microcontroller like PIC, Arduino comes with inbuilt ADC, but the basic microcontroller like 8051 does not have inbuilt ADC. So, the selection of ADC for these types of microcontrollers plays very important role in the performance of the whole system. Following things must be considered while opting for an ADC

2.5.1 Resolution

The resolution of the ADC is defined as the number of discrete values it can produce for the analog values. The number of discrete values available, or "levels", is a power of two, since they are stored in binary form. For example, an ADC with a resolution of 8 bits can encode an analog input to one in 256 different levels, since $2^8 = 256$.

Resolution can also be defined electrically. The minimum change in voltage required to change in the output level is called the least significant bit (LSB) voltage. The resolution *Q* of the ADC is equal to this voltage. Voltage resolution of an ADC is equal to its reference voltage divided by the number of discrete values:

$$V = \frac{V_{range}}{2^M - 1} \quad \ldots\ldots 2.4$$

where M is the ADC's resolution in bits and V_{range} is the full scale voltage range given by

$$V_{range} = V_{refHi} - V_{refLo} \quad \ldots\ldots 2.5$$

where V_{RefHi} and V_{RefLow} are the upper and lower extremes, respectively, of the voltages that can be coded.

Hence, we can say that the higher resolution gives less error in the digital equivalent representation. The resolution can affect the performance of the system by producing quantization noise.

2.5.2 Conversion Time

This is very crucial factor while selecting an ADC, the conversion time is the time required to convert the analog value at the input in to its digital equivalence. The ADC with low conversion time is desirable for higher speed of operation. The speed of conversion for an ADC should match with speed of operation of microcontroller. If the speed of conversion is high than speed of operation of microcontroller, the data packets will be lost. If the speed of operation is higher than the speed of conversion, the waiting time for microcontroller will increase. Consequently it will affect the overall performance of the system.

Chapter 3

Pulse Width Modulation Techniques

Digital controllers for DC-DC converters have been verified as having many advantages as compared to the analog controllers. A high resolution digital pulse-width modulator (DPWM) is required to achieve precise output voltage regulation and eliminate errors to the quantization effects of the ADC and the DPWM. In recent years, several methods are proposed for PWM generation as explained in [1]. This chapter discusses the basic principle of PWM and cover all from very elementary method to the proposed method of PWM.

3.1 Pulse Width Modulation

Pulse-width modulation (PWM) is a commonly used technique for controlling power to inertial electrical devices, made practical by modern electronic power switches.

The average value of voltage (and current) fed to the load is controlled by turning the switch between supply and load on and off at a fast pace. The longer the switch is on compared to the off periods, the higher the power supplied to the load is. The term duty cycle describes the proportion of 'on' time to the regular interval or 'period' of time; a low duty cycle corresponds to low power, because the power is off for most of the time. Duty cycle is expressed in percent, 100% being fully on.

The main advantage of PWM is that power loss in the switching devices is very low. When a switch is off there is practically no current, and when it is on, there is almost no voltage drop across the switch. Power loss, being the product of voltage and current, is thus in both cases close to zero. PWM also works well with digital controls, which, because of their on/off nature, can easily set the needed duty cycle.

The average value is given as

$$y_{(avg)} = \frac{1}{T}\int_0^T f(t)\ \mathrm{dt}$$

If we consider a pulse waveform with a low value y_{min}, a high value y_{max} and a duty cycle D

$$y_{(avg)} = \frac{1}{T}\left(\int_0^{D.T} f(t)\ dt + \int_{D.T}^{T} f(t)\ dt\right) \quad \text{..... (3.1)}$$

$$y_{(avg)} = D^* y_{max} + (1-D)\, y_{min} \quad \text{.....(3.2)}$$

If $y_{min} = 0$ then $y_{(avg)} = D^* y_{max}$ .....(3.3)

hence average value of the signal is directly dependent on the duty cycle D.

The simplest way to generate a PWM signal is the interceptive method, which requires only a sawtooth or a triangle waveform (easily generated using a simple oscillator) and a comparator. When the value of the reference signal (the red sine wave in figure 1) is more than the modulation waveform (blue), the PWM signal (magenta) is in the high state, otherwise it is in the low state as shown in fig 3.1

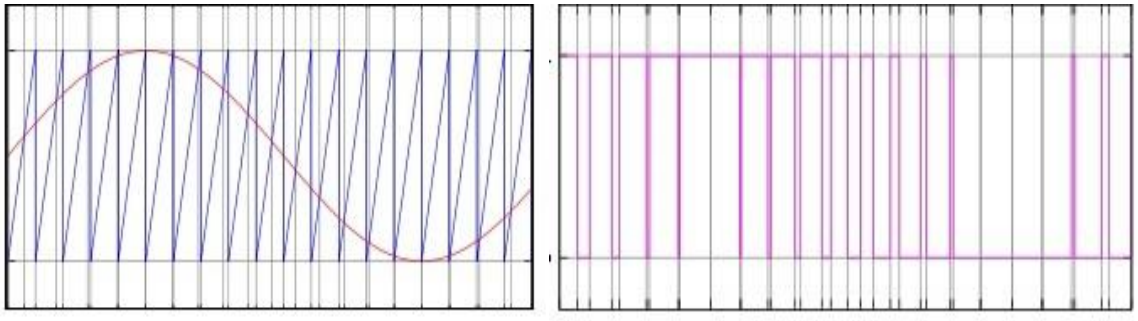


Fig. 3.1: A simple method to generate the PWM pulse train corresponding to a given signal is the interceptive PWM: the signal (here the red sine wave) is compared with a saw tooth waveform (blue). When the latter is less than the former, the PWM signal (magenta) is in high state (1). Otherwise it is in the low state (0).

3.2 PWM Generation

3.2.1 Analog Implementation

In the standard analogue trailing-edge pulse width modulation, an analog input signal is compared to a given carrier to provide amplitude to time domain conversion, as shown in figure below. The usual particular case of a linear ramp ("saw-tooth") as the carrier results in a linear relationship between the input signal and the output pulse width

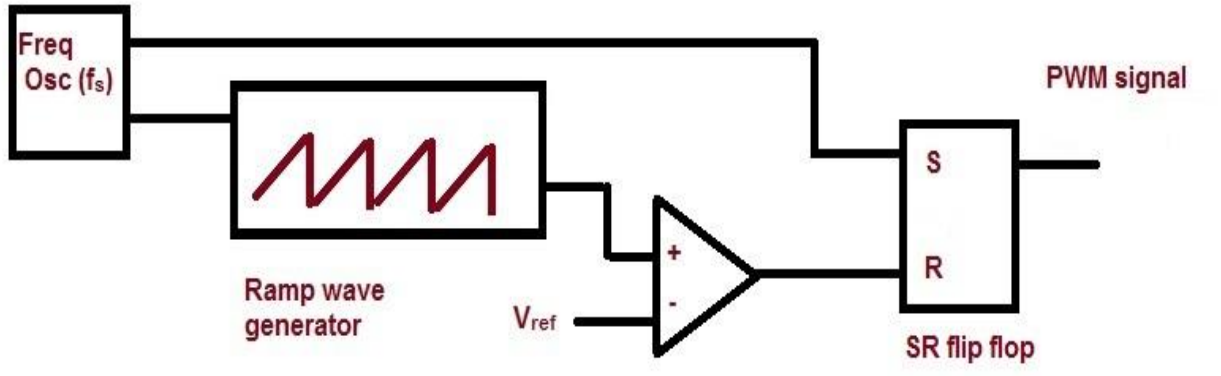


Fig.3.2 Conceptual block diagram of an analog PWM.

3.2.2 Digital Implementation

3.2.2.1 Counter- comparator based technique:

The first reported method for implementing a DPWM is based on the direct digital emulation of the ramp waveform by means of a fast-clocked counter, which is loaded by the input digital code at the beginning of the cycle, and thus generating a time-varying digital code following a sawtooth, signal that is compared with zero by a digital zero detector. This counter-based DPWM closely follows the general block diagram of Fig. 3.3. An excellent linearity is achieved in the digital to time domain conversion through the use of a clock to divide the time p*eri*od T_{SW} = 1/ F_{SW} & for an n-bit DPWM. For a high switching frequency F_{SW} and a high DPWM resolution n, the need for the very high frequency clock is the main disadvantage of this approach.

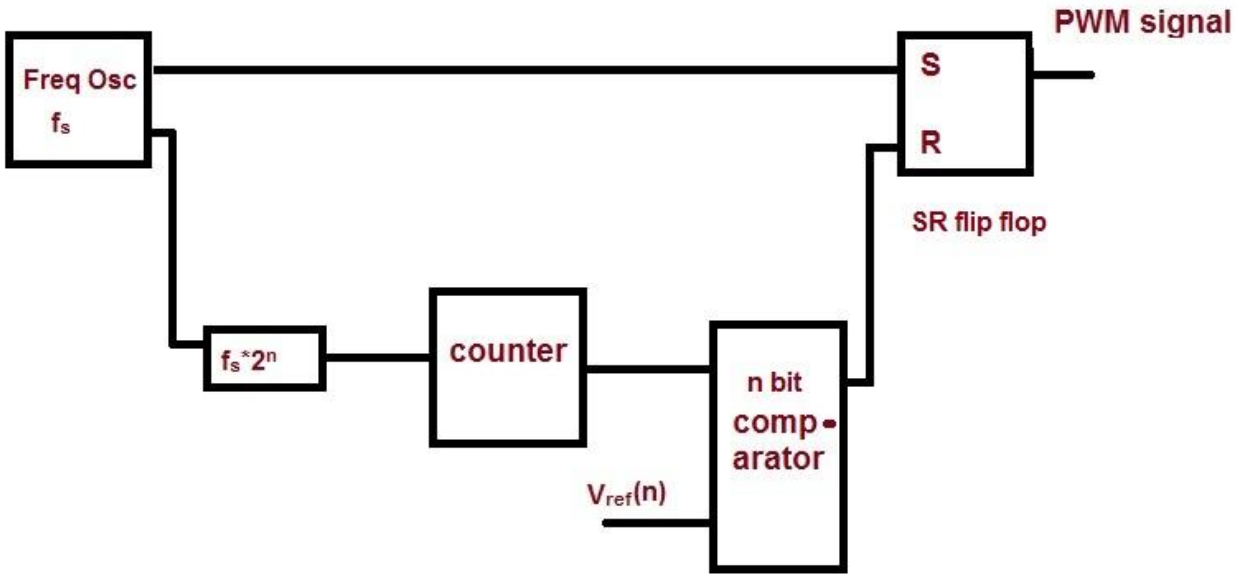
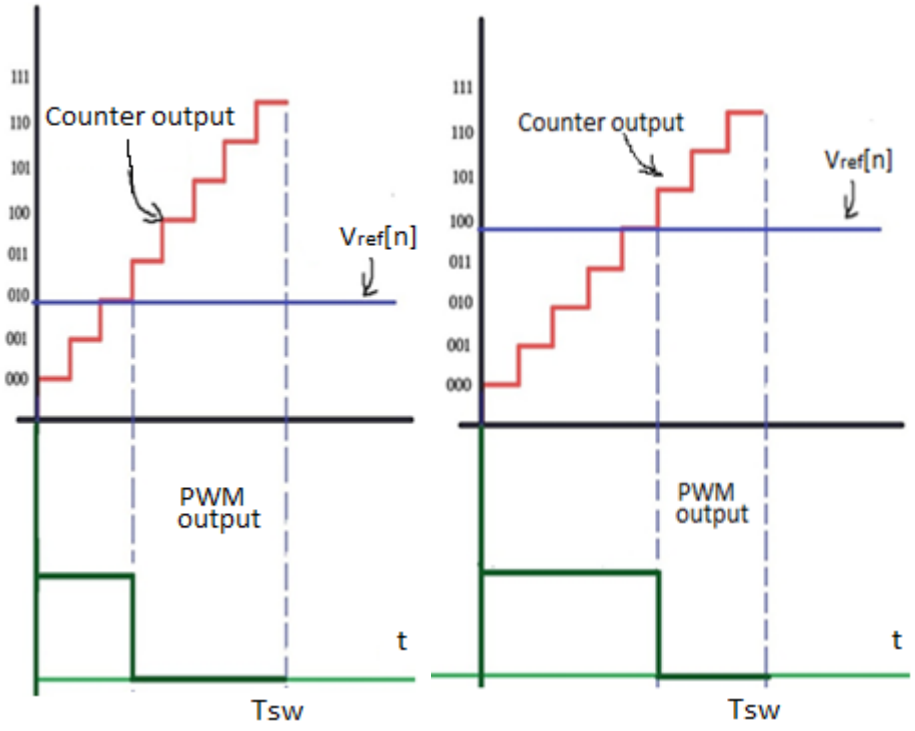


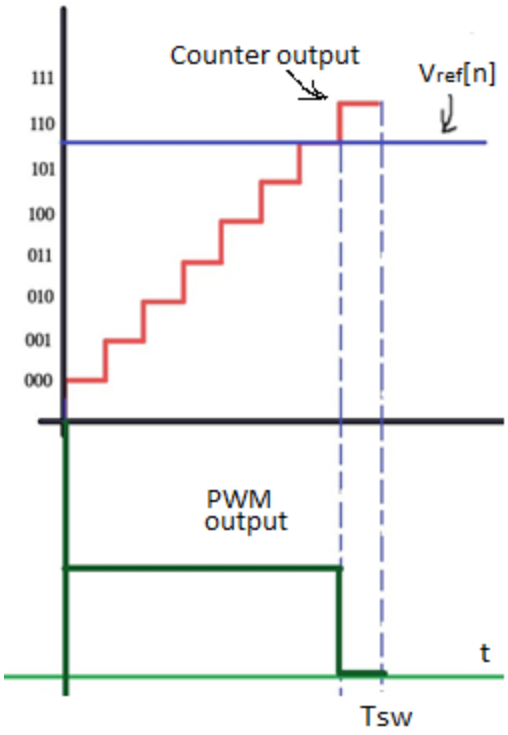
Fig.3.3 Conceptual block diagram of a digital PWM

The input output relation can be explained as follows with an example. Consider a 3 bit operation, which means all the digital signals are represented and arithmetic operations for them are done using 3 bits and if any arithmetic operation results need more than 3 bits, they are either discarded or stored in other variable. Hence, higher number bit representation gives better resolution consequently less quantization error. Fig 3.4 illustrates the operation of PWM generation using this counter comparator method. The output of SR flip-flop is set high at the starting of each cycle of switching frequency. The comparator continuously compares the output from the counter with the 3 bit reference value of the voltage. Whenever, the counter values goes above the reference value the comparator makes his carry signal high at the output. This signal triggers the SR flip-flop to reset its output. In fig. 3.4, the output results are drawn shows the variation in the width of pulse with respect to the error generated by the 3 bit comparator. As it can be seen from the waveforms generated by the counter, the counter needs to clock at frequency $F_{SW}*2^n$, n is 3 here. That is equal to 8 times the switching frequency F_{SW}. Hence, if we increase the number of bits for high resolution the switching frequency requirement for counter increases exponentially, so this method is not desirable to achieve high resolution.

The figures in the below are drawn for illustration purpose, the simulation gave the same results but for better understanding of operation, the waveforms are drawn using drawing tool application in Microsoft's operating system. The figures show the output PWM waveform for different reference value.



(a) (b)



(c)

Fig. 3.4 Illustration of operation for PWM generation using Counter Comparator Method

3.2.2.2 Delay Line based Technique:

The second approach is called as Delay line method, it circumvents the high-frequency clock problem of the counter-based DPWM is based on a tapped delay line, as depicted in Fig 4. This circuit takes advantage of the linear propagation of a given pulse from a reference clock *clk* through the delay cells connected in cascade, to select a given pulse width quantized as a function of the selected number of cells. This selection can he obtained from the digital input code by means of a 2^n to 1 multiplexer driven by the digital input code *d*. The multiplexer selects the signal that resets the output PWM signal, thus performing the function of selecting one of the time slots generated by the delay-line time quantizer. The delay line in Fig 3.3 operates in the sense that the switching frequency F_{SW} is imposed by an external oscillator, while the total delay of the line should he designed in order for the maximum delay to match the switching period. As the semiconductor material properties (and therefore the cell delay td) vary with process and temperature, this condition cannot be satisfied at all process or temperature corners.

Consequently, the executed duty cycle D_{exe} is not always the same as the duty cycle command D_{comd} presented by the input digital signal.

One of the disadvantages of the delay line based approach is the nonlinearity in the digital to time domain conversion, which has its origin in the cell delay mismatch due to process variations across the length of the delay line and any extra mismatched delay in the path of delay cell output to the reset terminal of the flip-flop. The most important disadvantage for this architecture is the large size required by the multiplexer in charge of gating the desired delay line tap to the flip-flop. A power and area efficient solution can be implemented by considering a hybrid counter/delay-line based design, trading-off multiplexer area versus counter clock frequency. In the hybrid approach, the two cases reported so far employ either the counter with the most significant hits to provide a coarse pulse width and the finer pulse width being generated by the delay line selected by the least significant bits, or vice versa. This method

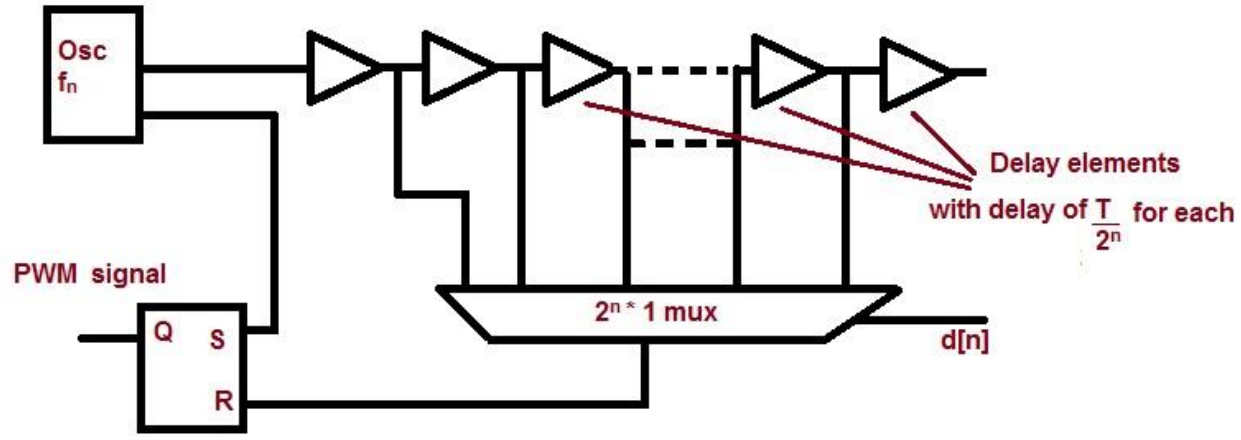
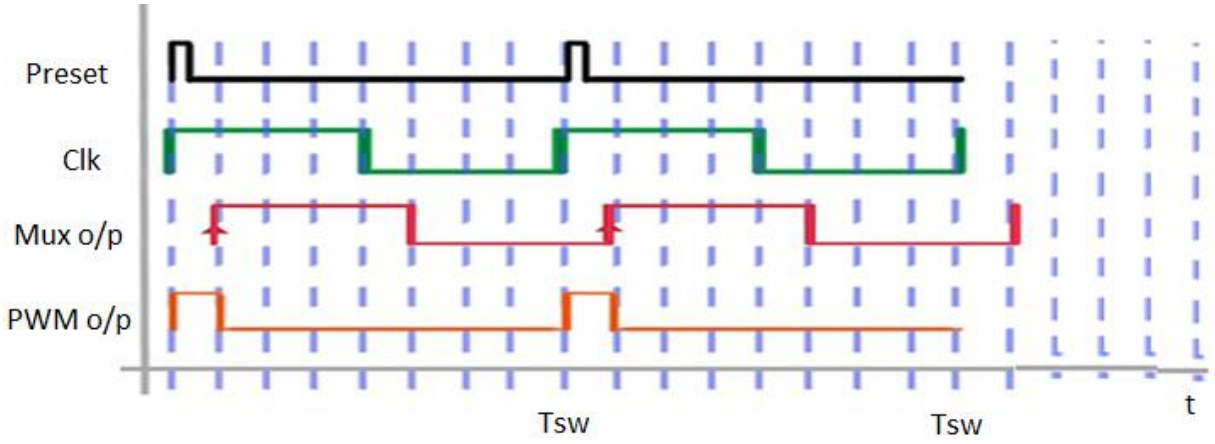


Fig.3.5 Delay-line based digital pulse width modulator (DPWM) architecture

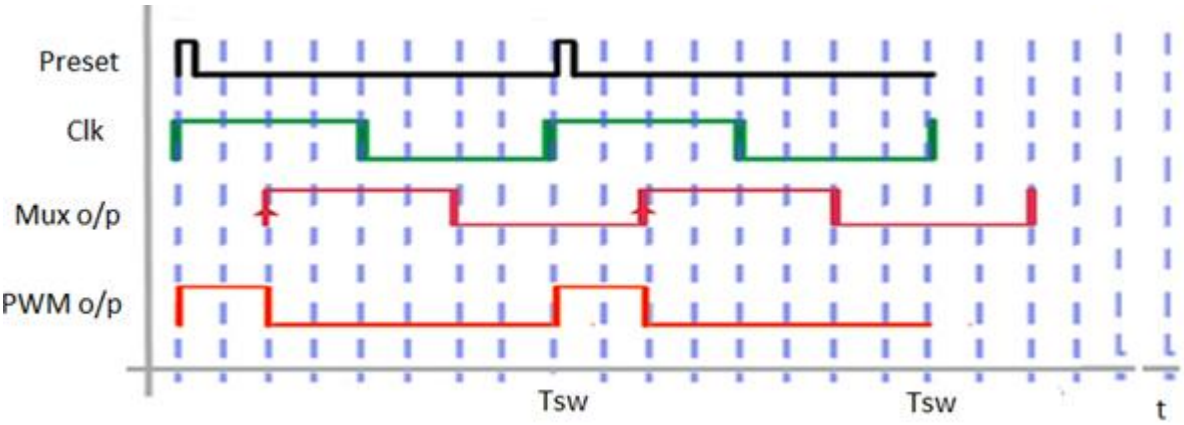
circumvents the problem of high frequency requirement. But this method has other disadvantages like the requirement of more hardware as the resolution of increases and hence more delay time is introduced in the control loop which results in slow transient response and reduced bandwidth.

The description for PWM generation using this method can be explained through Fig 3.6. This method uses N number of delay elements where N is equal to 2^n and n is the number of bits, a 2^n*1 mux and a flip- flop. The output of each delay element is get delayed by $T/2^n$, where T is total period of switching cycle. At starting each switching cycle, the output of SR flip-flop is set

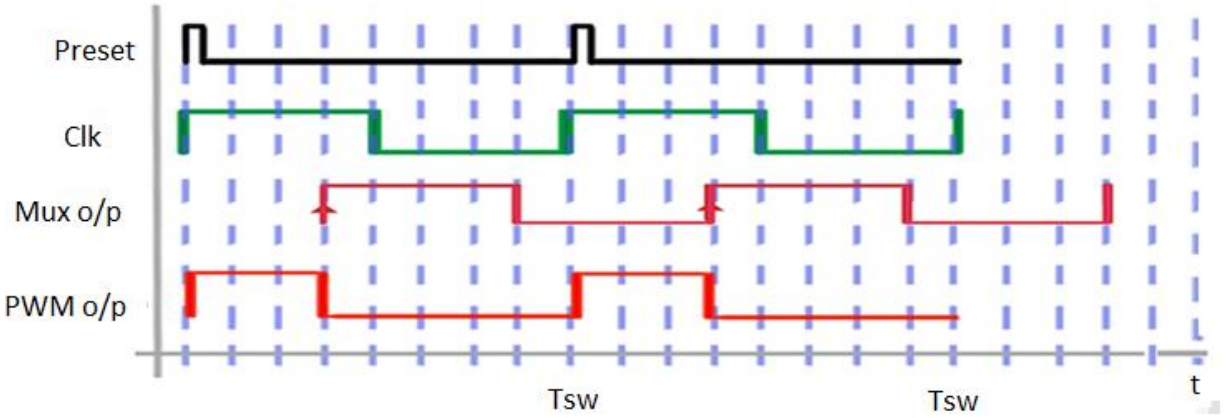
to high, depending on the error d[n] the mux taps one of the delay elements and reset the output of flip-flop. If the error value is high the mux select the more delayed element and the output will be reset lately. In this method the high frequency requirement is circumvented but this method need more number of delay element for higher resolution. The figures in Fig 3.6 are drawn for illustration purpose, the simulation gave the same results but for better understanding of operation, the waveforms are drawn using drawing tool application in Microsoft's operating system. The figures show the output PWM waveform for different reference value. The error is increasing from Fig. 3.6 (a) to 3.6 (d) linearly.



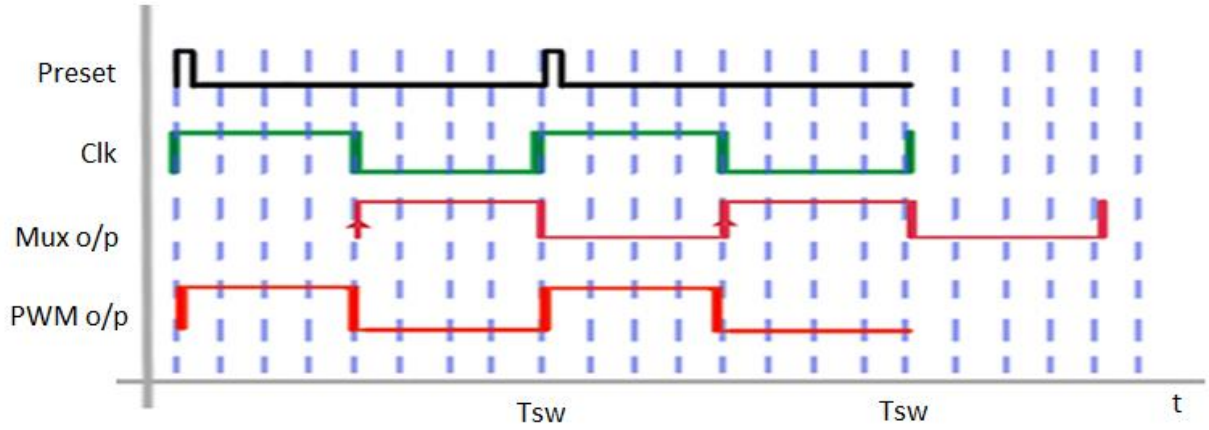
(a)



(b)



(c)



(d)

Fig. 3.6 Illustration of PWM generation using Delay Line Method

3.3 Microcontroller based Technique:

3.3.1 Microcontroller:

The microcontroller incorporates all the features that are found in microprocessor. The microcontroller has built in ROM, RAM, Input Output ports, Serial Port, timers, interrupts and clock circuit. A microcontroller is an entire computer manufactured on a single chip. Microcontrollers are usually dedicated devices embedded within an application. For example, microcontrollers are used as engine controllers in automobiles and as exposure and focus controllers in cameras. In order to serve these applications, they have a high concentration of on-chip facilities such as serial ports, parallel input output ports, timers, counters, interrupt control,

analog-to-digital converters, random access memory, read only memory, etc. The I/O, memory, and on-chip peripherals of a microcontroller are selected depending on the specifics of the target application. Since microcontrollers are powerful digital processors, the degree of control and programmability they provide significantly enhances the effectiveness of the application. The 8051 is the first microcontroller of the MCS-51 family introduced by Intel Corporation at the end of the 1970s. The 8051 family with its many enhanced members enjoys the largest market share, estimated to be about 40% among the various microcontroller architectures. The microcontroller has on chip peripheral devices. Microcontroller can be classified on the basis of their bits processed like 8bit MC, 16bit MC. 8 bit microcontroller, means it can read, write and process 8 bit data. Fig 3.4 shows a functional block of the internal operation of an 8051 microcomputer. The internal components of the chip are shown within the broken line box [10].

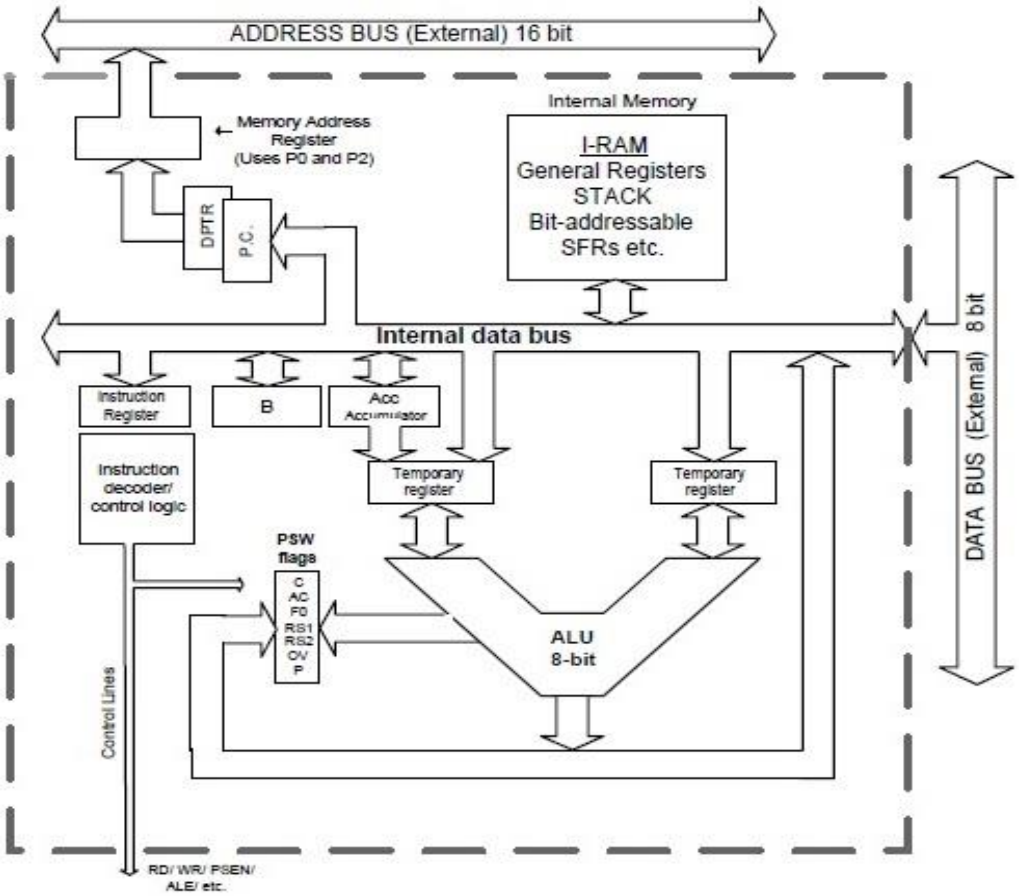


Fig. 3.7 Functional block diagram of 8051 microcontroller

The programming approaches for generating PWM signals are explained below.

1) Sequential approach
2) Time multiplexed approach

3.3.2 Sequential approach

In this approach microcontroller core processor monitors the timing generation for "ON" and "OFF" status. The algorithm and flowchart for this approach is explained below. Flowchart given below shows the algorithm used in this approach. The program flow is sequential and processor of 8051 is engaged in the time slot generation for PWM signal. The input to this program is the digitized error signal generated from the plant. Digital version of the error signal is generated from the A to D converter used prior to this system.

The program can be explained as the input in the form of 8 bits is obtained from the plant and then $T_{on,}$ T_{off} timing values are calculated depending on the error. These timing values are fed to timer of the 8051 controller and the processor of the 8051 monitors these values and make the PWM output from the 8051 high and low representing "ON" and "OFF" status of the pin. The algorithm for this method is in flowchart of fig 3.5. Drawbacks of this method are the processor is engaged in the time slot generation which can be done on other way and hence this method is not efficient.

3.3.3 Time multiplexed approach:

For this approach the concept of interrupts is exploited. Interrupts are explained as follows.

Interrupt: An interrupt causes a temporary diversion of program execution in a similar sense to a program subroutine call, but an interrupt is triggered by some event, external to the currently operating program. We say the interrupt event occurs asynchronously to the currently operating program as it is not necessary to know in advance when the interrupt event is going to occur. There are total six interrupt sources for the 8051 listed as follows [11]:

Interrupt	Flag	Vector address
System RESET	RST	0000h
External interrupt 0	**IE0**	**0003h**
Timer/counter 0	TF0	000Bh
External interrupt 1	**IE1**	**0013h**
Timer/counter 1	TF1	001Bh
Serial port	RI or TI	0023h

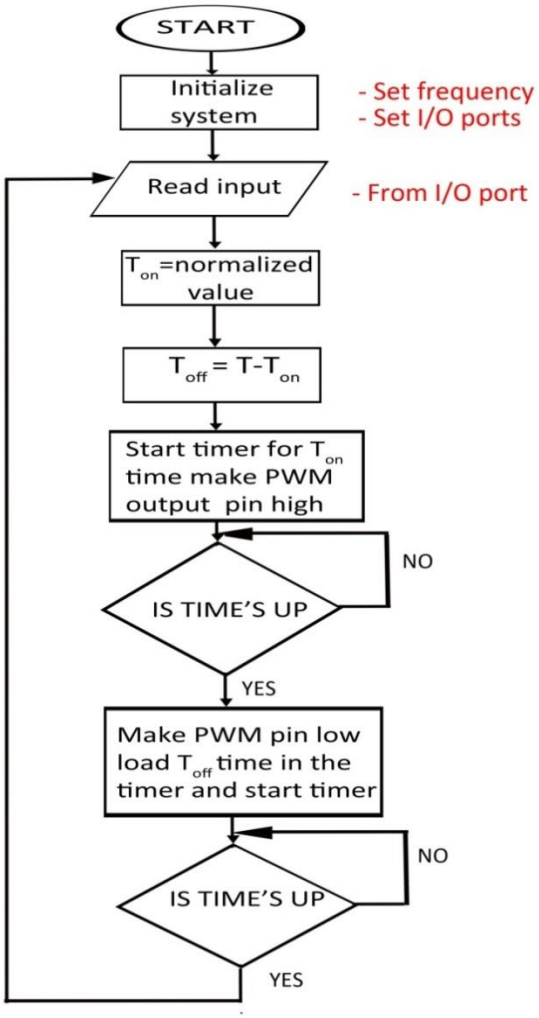


Fig.3.8 Flowchart for sequential approach

The time multiplexed approach is the proposed approach in for PWM generation in this thesis. This approach uses timer and external interrupt of 8051. These interrupts will produce an interfere to current process and make the processor to respond it. To respond the interrupt the microcontroller executes an interrupt handler program which is also called as Interrupt Service

Routine (ISR). At this location the respective instructions are saved which will be executed when the processor transfers the program control here.

Here at the ISR of timer 0, instructions for toggling the status of PWM output depending on T_{on} and T_{off} are saved and at the ISR of external interrupts a small program is written to update the T_{on} and $T_{off.}$ The flowchart which is given below will explain the algorithm in detail.

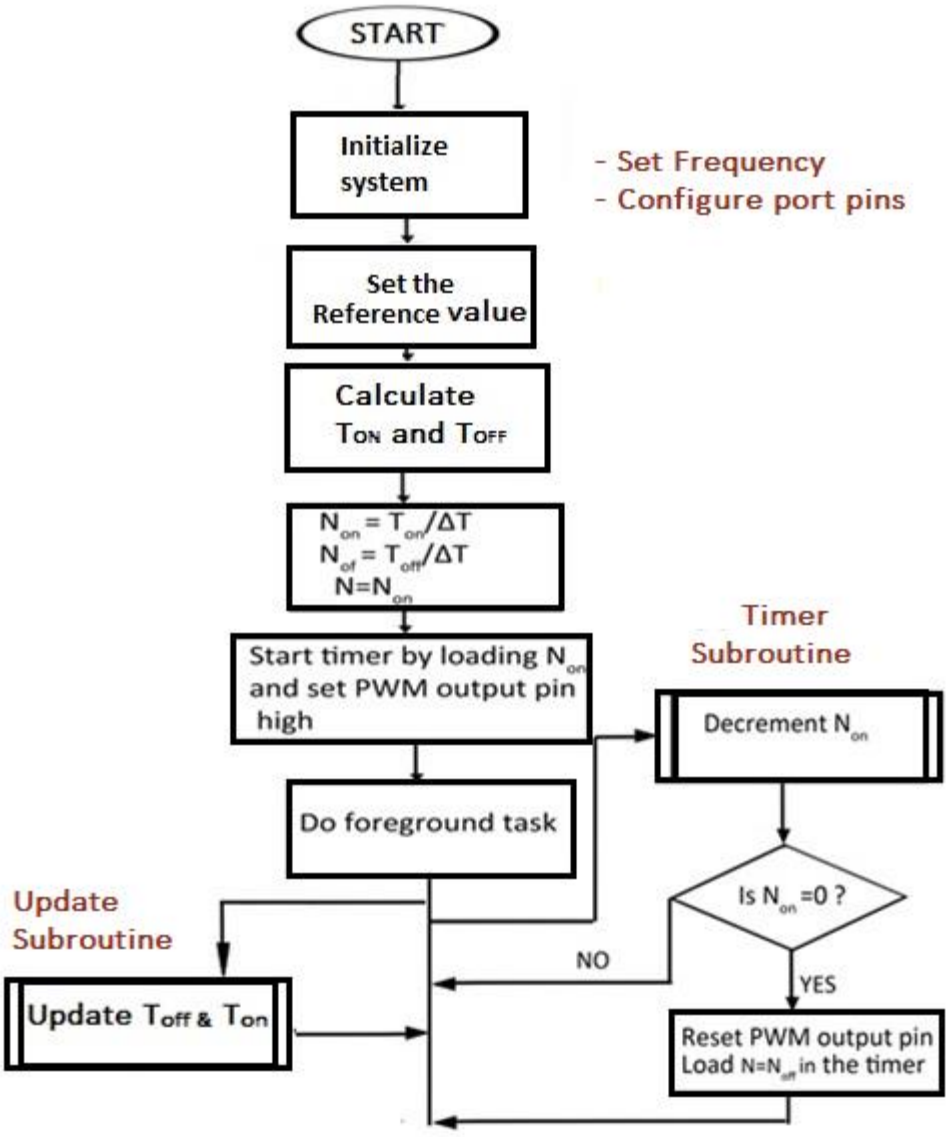


Fig. 3.9 Flowchart for time multiplexed approach

3.3.4 Delay Line approach:

As previously stated in section 3.2.2, delay line method came into picture to circumvent the drawbacks of counter comparator method. Delay line method used for high speed requirement. Main disadvantage of delay line method is that the variation in delays of each element due to variation in semiconductor properties caused by change in temperature.

In this approach the logic of Delay line is implanted through program in 8051 microcontroller. The objective is to validate the proposed method in section 3.3.3 with this method.

CHAPTER 4

RESULTS

This chapter gives the results of the proposed approach also comparison with the delay line method.

4.1 Simulation Results for Proposed Approach:

The proposed method for PWM generation is fully based on programming the microcontroller. The algorithm of this program is explained in section 3.3.3 of chapter 3. The simulation of DC- DC buck converter is done in NI Multisim environment. Multisim was originally created by a company named Electronics Workbench, which is now a division of National Instruments. Multisim includes microcontroller simulation (formerly known as Multi MCU), as well as integrated import and export features to the Printed Circuit Board layout software in the suite, NI Ultiboard. It is very easy to use schematic capture and easily simulates various analog and digital circuits. It is also widely used in academia and industry for circuit's education, electronic schematic design and SPICE simulation. For writing the programs of microcontroller the Keil software is used. Keil provides a broad range of development tools like ANSI C compiler, macro assemblers, debuggers and simulators, linkers, IDE, library managers, real-time operating systems and evaluation boards for 8051, 251, ARM, and XC16x/C16x/ST10 families. The hex file produced from the Keil is dumped in to microcontroller using the Multisim.

The switching frequency generated for PWM signal from 8051 microcontroller is 5 KHz. Using this value as F_{SW} and with the help of formulae in chapter two, the power stage parameter calculation is done. The values of L, C used and other parameters for simulations are as follows, V_{IN} = 5 volts, V_{OUT}= 2.5 volts, R_L = 1ohm, L = 100 μ H and C= 1000μ F,

The simulation diagram is shown in fig 4.1 the block label indicates their functionality. For above values of power stage parameters the voltage waveform at the load resistance of buck converter is shown in fig 4.3 with dotted line. Fig 4.4 shows variation at the output voltage due to step load change with dotted line. The step load is applied at 10msec.

4.2 Simulation Results for Delay Line Approach:

To validate performance of proposed approach, delay line method is implemented in 8051 microcontroller and simulated for the same power stage parameters as obtained in section 4.1. For simulation of this approach NI Multisim is used. Fig 4.2 gives the block diagram for this method.

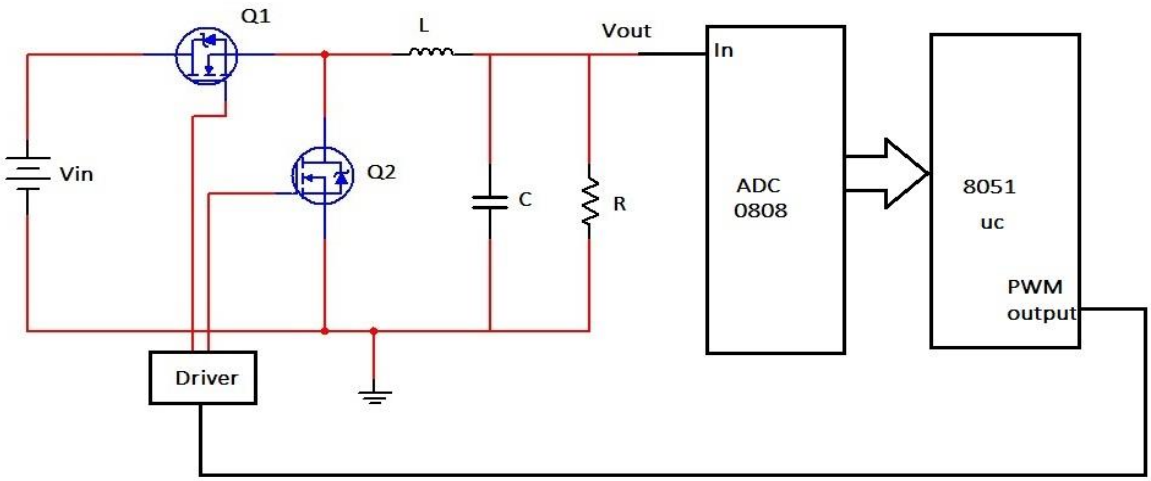


Fig 4.1 Simulation diagram for proposed approach

The voltage waveform at the load resistance of buck converter is shown in fig 4.3 with solid line. Fig 4.4 shows variation at the output voltage due to step load change with solid line. The step load is applied at 10msec.

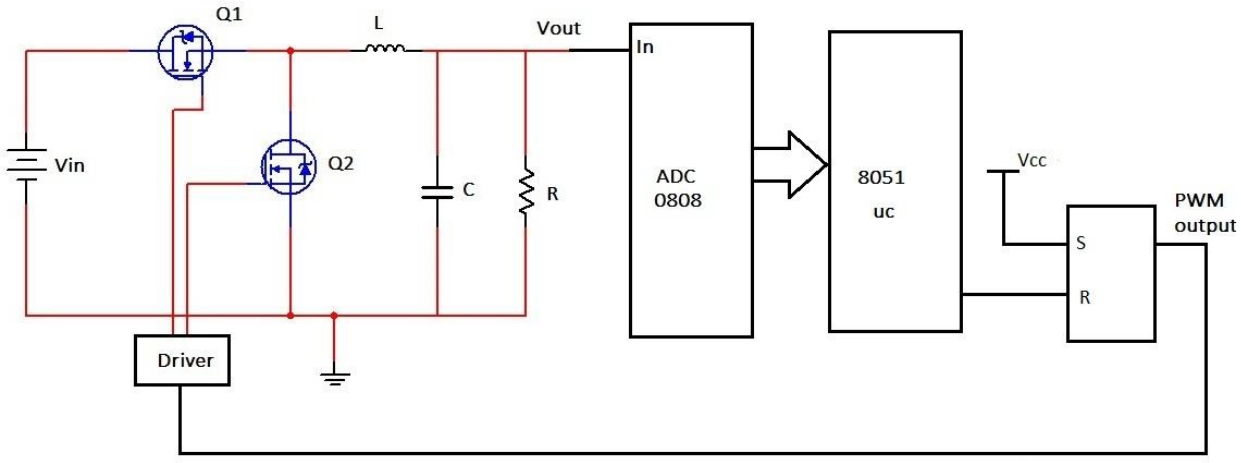


Fig 4.2 Simulation diagram for delay line approach

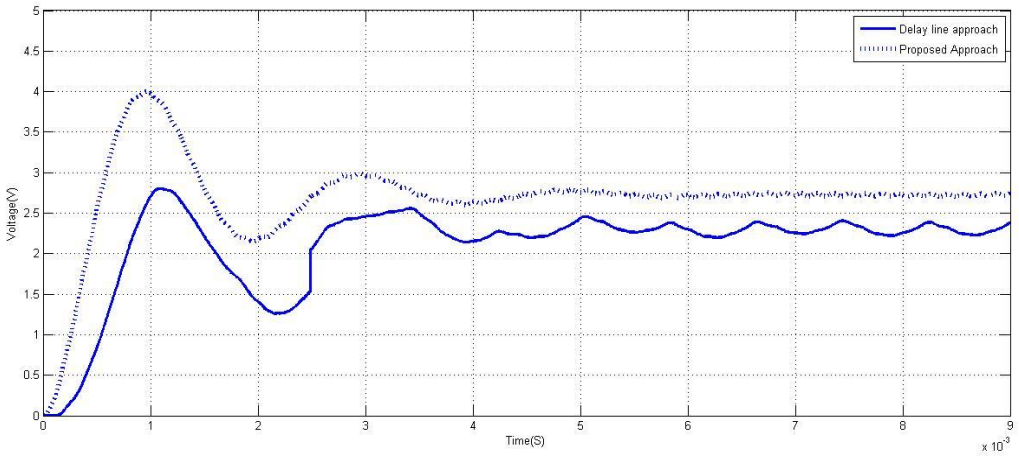


Fig 4.3 Voltage responses at load of buck converter

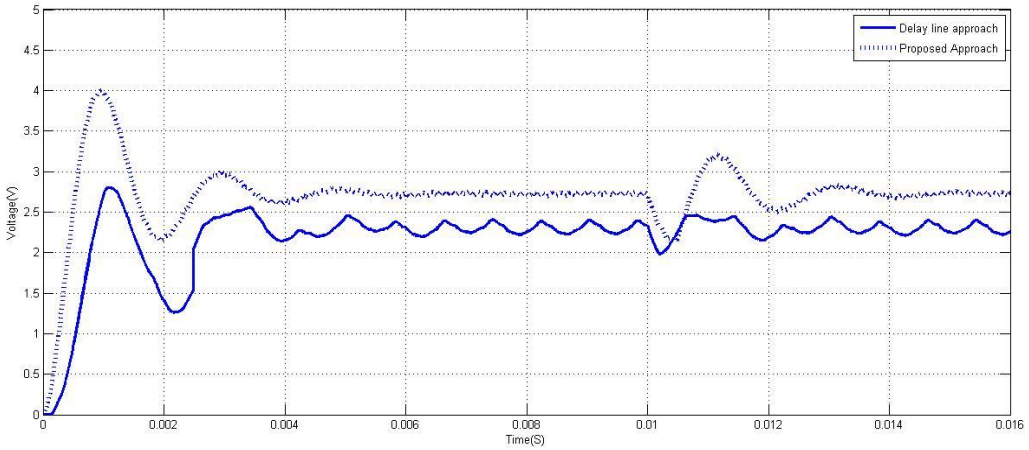


Fig 4.4 Voltage responses for step load change load of buck converter

4.3 Simulation Results for Different Set voltages:

As the digital controller implemented for PWM generation, it has the power of reprogrammability. So changing the program code we can change the desired or reference voltage of buck converter. The waveform in Fig. 4.5- 4.10 shows the effect of changing the set value of buck converter. The respective PWM waveform and inductor current waveforms are also shown in these figures.

Vset = 2 V

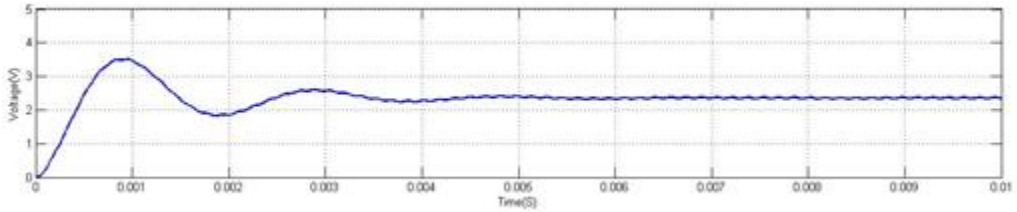


Fig 4.5 (a)

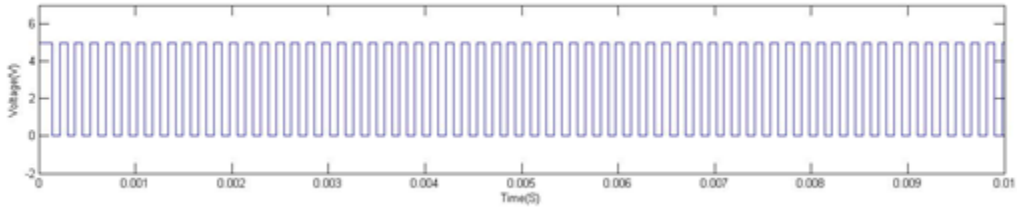


Fig 4.5 (b)

Fig. 4.5 (a) Voltage waveforms form the buck converter for Vset = 2 V

(b) Corresponding PWM waveforms form microcontroller

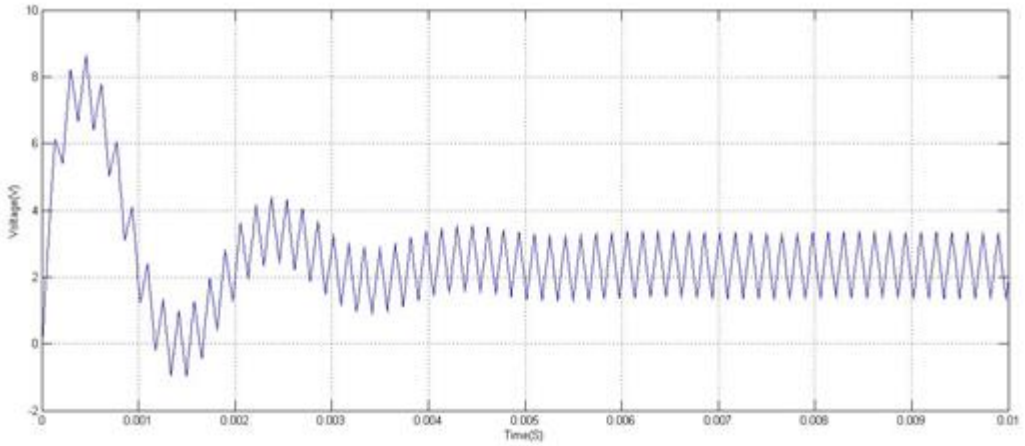


Fig. 4.6 Inductor current waveforms form the buck converter for Vset = 2 V

Vset = 2.5 V

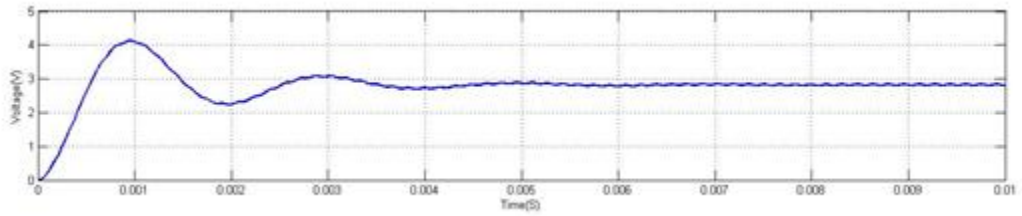


Fig 4.7 (a)

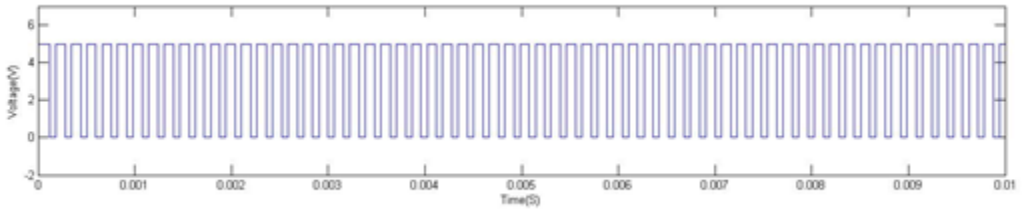


Fig 4.7 (b)

Fig. 4.7 (a) Voltage waveforms form the buck converter for Vset = 2.5 V

(b) Corresponding PWM waveforms form microcontroller

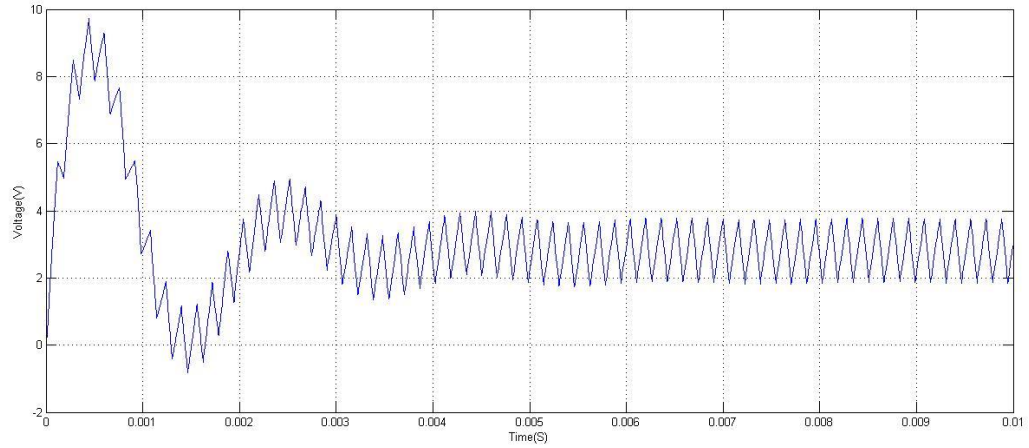


Fig. 4.8 Inductor current waveforms form the buck converter for Vset = 2.5 V

Vset = 3 V

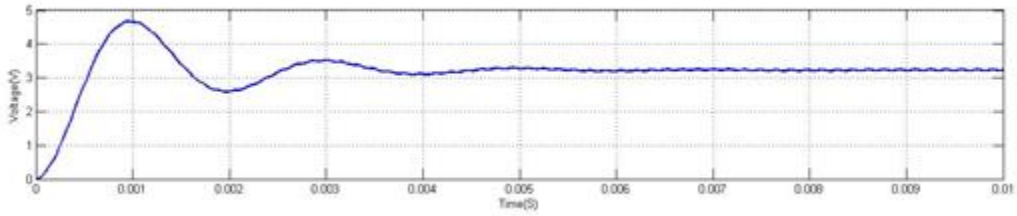


Fig. 4.9 (a)

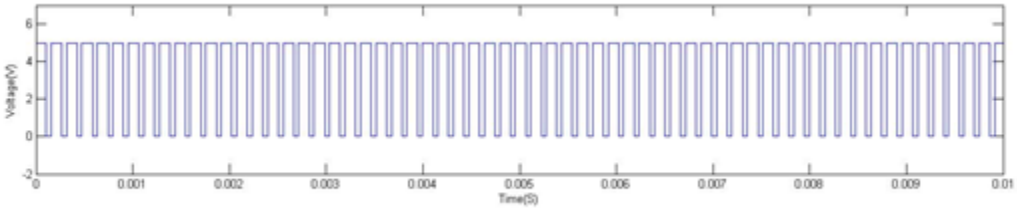


Fig. 4.9 (b)

Fig. 4.9 (a) Voltage waveforms form the buck converter for Vset = 3 V
(b) Corresponding PWM waveforms form microcontroller

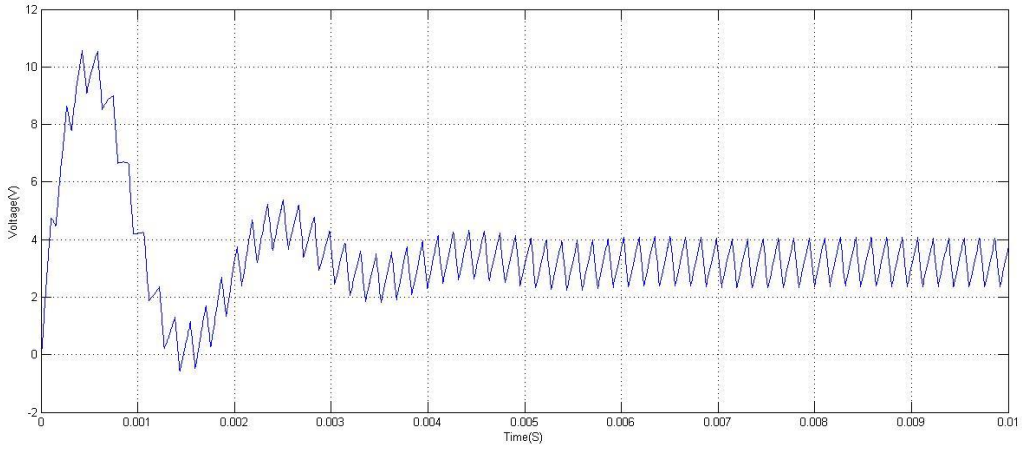


Fig. 4.10 Inductor current waveforms form the buck converter for Vset = 3 V

Chapter 5

Conclusions

In this work different PWM architecture are studied and implemented. The first method i.e. counter comparator method of DPWM provides good linearity in digital to time domain conversion and fail to provide high resolution. The counter also requires high very clock frequency i.e. $F_{SW}*2^n$, where F_{SW} is switching frequency and *n* number bits.

The drawbacks of counter comparator methods are circumvented in delay line method. But this delay line method requires more hardware and the number of delay elements increase with increase in the number of bits. One more disadvantage of this method is, the temperature effect on the semiconductor devices. As the semiconductor material properties and therefore the cell delay td vary with process and temperature. Consequently, the executed duty cycle D_{exe} is not always the same as the duty cycle command D_{comd} presented by the input digital signal.

The proposed approach eliminates drawbacks of counter comparator method and delay line method. It provides good linearity between the digital to time domain conversion. The switching frequency can be increased by increasing the clock frequency of the microcontroller. The proposed method produces quantization error due to the ADC resolution and the slots of timer used in microcontroller. These errors can be reduced by increasing the resolution of ADC and clock frequency of the microcontroller.

5.1 Future work

The proposed method does not incorporate any controller like PI, PID, though the problem of saturation is taken care by the program. Hence the immediate future work would be to use a suitable controller for efficient controlling and make the system more stable.

As the proposed method uses basic 8051 architecture, there is limitation on the speed of operation consequently there is limitation on the high frequency PWM generation. This can be circumvented by using high speed microcontroller or even using the FPGAs for PWM generation.

References

[1] Asif Syed, Ershad Ahmed and Dragan MaksimoviC, Eduard Alarcon "Digital Pulse Width Modulator Architectures", *351h Annual IEEE Power Electronics Specialirls Conference* Aachen, Germany, 2004.

[2] Santa Concepcion Huerta, Angel de Castro, Oscar Garcia, and Jose A. Cobos "FPGA-Based Digital Pulsewidth Modulator With Time Resolution Under 2 ns*", IEEE Transaction on Power Electronics Vol. 23 No.6,* pp. 3135-3142, *November 2008*

[3] Soon H. Kwon Ick Choy and K. H. Kim H. S. Mok, "A New Direct Digital PWM Technique for Microprocessor-Based PWM Inverters" ", *Power Electronics Specialists Conference, 1996. PESC '96* Vol. 2 pp.: 1300 – 1304.

[4] Brigitte Hauke "Basic Calculation of a Buck Converter's Power Stage" *an Application Report December 2011–Revised August 2012*.

[5] Giuseppe Maimone "Selecting L and C Components in the Power Stage of the MC34700 Switching Regulators" *Freescale Semiconductor* Application Note.

[6] Jens Ejury, V2.0 "The Selection of MOSFETs for DC-DC-Converters" *Infineon technologies*, Application Note.

[7] Y. Choi, N. Chang, and T. Kim, "DC-DC converter-aware power management for battery-operated embedded systems," in *Proc. ACM/IEEE Des. Autom. Conf.*, 2005, pp. 895–900.

[8] E. T. Moore and T. G. Wilson "Basic Considerations for DC to DC Conversion Networks" *IEEE transaction on Magnetics, Vol. Mag-2, No -3 pp. 620-624 Sept. 1996*

[9] Luca Corradini, , and Paolo Mattavelli " Modeling of Multisampled Pulse Width Modulators for Digitally Controlled DC–DC Converters" *IEEE transaction on Power Electronics, Vol. 23, No. 4, pp.1839-1847* JULY 2008 .

[10] Kenneth J. Ayala "The 8051 microcontroller architecture, programming and application" *2nd Edition, Penram International Publishers (India),* pp. 11 -98, *1996.*

[11] Raj Kamal " Embedded Systems - Architecture, Programming and Design", 2nd Edition McGraw-Hill Publication, Chapter 5, 2008

[12] Wang Xichuan, Zhang ting, Deng Huan "The Design of a Developed PWM DC-DC Converter" *Proceedings of HDP'07*

[13] Yoichi Ishizuka, Yosuke Asako, Masao Ueno and Hirofumi Matsuo "A Design of a Low-Delay DPWM Control Circuit for DC-DC Converter", *29th International Telecommunications Energy Conference, 2007. INTELEC 2007.*

[14] Yan-Fei Liu, Eric Meyer, and Xiaodong Liu "Recent Developments in Digital Control Strategies for DC/DC Switching Power Converters" *IEEE transaction on Power Electronics, VOL. 24, NO. 11, pp. 2567- 2578 NOVEMBER 2009*

[15] R. R. Boudreaux, R. M. Nelms, and John Y. Hung "Simulation and Modeling of a DC-DC Converter Controlled by an 8 bit Microcontroller" *Applied Power Electronics Conference and Exposition, 1997. APEC '97*

[16] Chester Simpson "Linear and Switching Voltage Regulator Fundamentals" *Power Management Applications 2008*

[18] Simone Buso "Digital control of switching mode power supplies" *University of Padova – ITALY UNICAMP - August 2011*