National Institute of Technology

Rourkela

ATLAS SIMULATION BASED STUDY OF RECESSED SOURCE/DRAIN SOI MOSFETS

A thesis submitted in partial fulfillment of the requirements for the degree of Bachelor of Technology in Electronics & Communication Engineering

BY:

GOURI SANKAR SAHOO — ROLL NO-109EC0235

MANORANJAN BEHERA — ROLL NO-109EI0318

Under supervision of:

- PROF. PRAMOD KUMAR TIWARI

Department of Electronics & Communication Engineering

NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA

ODISHA, INDIA – 769 008

CERTIFICATE

This is to certify that the thesis titled "*ATLAS SIMULATION BASED STUDY OF RECESSED SOURCE/DRAIN SOI MOSFETs*" submitted to the National Institute of Technology, Rourkela by Mr. Gouri Sankar Sahoo, Roll No. 109EC0235 and Mr. Manoranjan Behera,Roll No.109EI0318 for the award of the degree of Bachelor of Technology in Electronics & Communication Engineering, is a bona fide record of research work carried out by them under my supervision and guidance.

The candidates have fulfilled all the prescribed requirements.

The thesis, which is based on candidate's own work, has not been submitted elsewhere for a degree/diploma.

In my opinion, the thesis is of standard required for the award of a Bachelor of Technology degree in Electronics & Communication Engineering.

To the best of my knowledge, they bear extremely good moral character and decent behavior.

Prof. P.K Tiwari

Department of Electronics & Communication Engineering

National Institute of Technology

Rourkela-769 008 (INDIA)

ACKOWLEDGEMENT

We are extremely grateful towards prof. Pramod Kumar Tiwari for his priceless advice and instructions. We would also like to extend our hearty gratitude towards Mr. Gopi Krishna,P.H.D scholar and Mr. Santanu Sarangi ,P.H.D scholar for their extended support and assistance in completing this paper.

TABLE OF CONTENTS PAGE NO.

ABSTRACT

Front gate and back gate threshold voltage, potential distributions and sub threshold swing of recessed source/drain ultra-thin body silicon on insulator MOSFETs are simulated and analyzed in a vivid manner with extreme meticulousness. Analysis and comparative study of the electrical characteristics of Re s/d UTB SOI MOSFETs with that of conventional FD SOI MOSFETs has been done. Structures of conventional SOI MOSFET and Re s/d MOSFETs is simulated with the help of software like ATLAS. The Re S/D has several advantages over conventional UTB MOSFETs with elevated S/D structure. We observe that values of drain current comes out to be higher for recessed s/d SOI MOSFETs

Chapter1:INTRODUCTION

Initial structure of MOSFET was at first proposed and patented by Lilienfeld and Heil in the year 1930, but was not successfully demonstrated until year 1960. The main technological problems were the control and reduction of the surface states at the interface between the oxide and the semiconductor .Initially it was only possible to deplete an existing n-type channel by applying a negative voltage to the gate. Such devices have a conducting channel between source and drain even when no gate voltage is applied and are called **"depletion-mode"** devices. A reduction of the surface states enabled the fabrication of devices which do not have a conducting channel unless a positive voltage is applied. Such devices are referred to as **"enhancement-mode"** devices. The electrons at the oxide-semiconductor interface are concentrated in a thin (~10 nm thick) "inversion" layer. By now, most MOSFETs are "enhancement-mode" devices.

MOSFET stands for metal oxide field effect transistor. MOSFET Field effect transistor is a unipolar transistor, which acts as a voltage-controlled current device and is a device in which current at two electrodes drain and source is controlled by the action of an electric field at another electrode gate having in-between semiconductor and metal very a thin metal oxide layer .MOSFET comprises of 4 parts namely source (S), gate (G), drain (D), and body (B) terminals. The body (or substrate) of the MOSFET often is connected to the source terminal, making it a three-terminal device. Because these two terminals are normally connected to each other (short-circuited) internally, only three terminals appear in electrical diagrams.

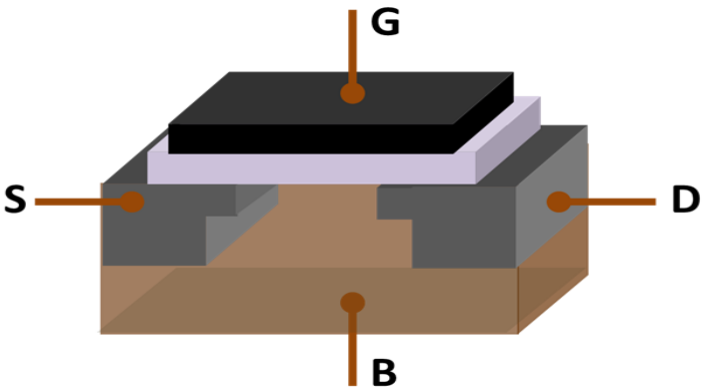
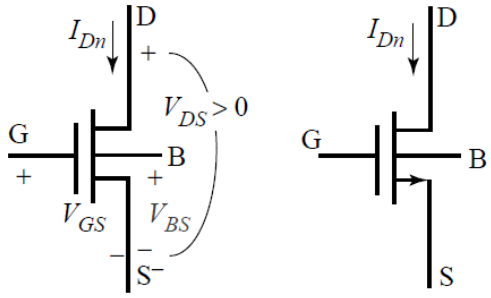


FIGURE 1.1.1

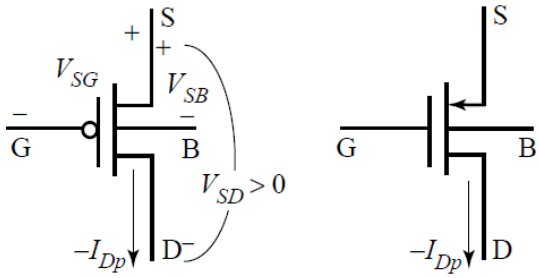
Two complementary devices:-

- ✓ n-channel device (n-MOSFET) on p-Si substrate(uses electron inversion layer)
- ✓ p-channel device (p-MOSFET) on n-Si substrate(uses hole inversion layer)



(a) n-channel MOSFET

FIGURE 1.1.2



(b) p-channel MOSFET

FIGURE 1.1.3

TYPES OF MODES IN A MOSFET

In *enhancement mode* MOSFETs, a voltage drop occurs across the oxide and hence induces a conducting channel between the source and drain contacts *via* the field effect. The term "enhancement mode" refers to the increase of conductivity with increase in oxide field that adds carriers to the channel, also referred to as the *inversion layer*. The channel can contain electrons (called an nMOSFET or nMOS), or holes (called a pMOSFET or pMOS), opposite in type to the substrate, so nMOS is made with a p-type substrate, and pMOS with an n-type substrate.

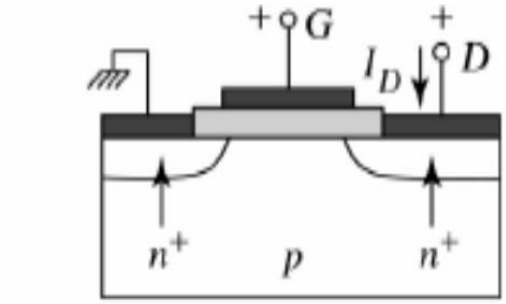


Fig 1.1.4 n-channel enhancement MOSFET

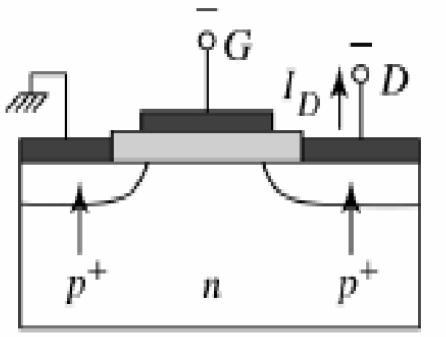


Fig1.1.5 p-channel enhancement MOSFET

When VGS = 0, the n-channel is very thin and channel width enhances with +VGS There are a pair of small n-type regions just under the drain & source electrodes. If apply a +ve voltage to gate, will push away the 'holes' inside the p-type substrate and attracts the moveable electrons in the n-type regions under the source & drain electrodes. Increasing the +ve gate voltage pushes the p-type holes further away and enlarges the thickness of the created channel. As a result increases the amount of current which can go from source to drain this is why this kind of transistor is called an enhancement mode MOSFET.

Three operational modes

A. Cut-off mode:

• $V_{GS} < V_T$, $V_{GD} < V_T$ with $V_{DS} > 0$.whereV_T –Threshold voltage of the device. According to the basic threshold model, the transistor is turned off, and there is no conduction between drain and source.so Id=0.

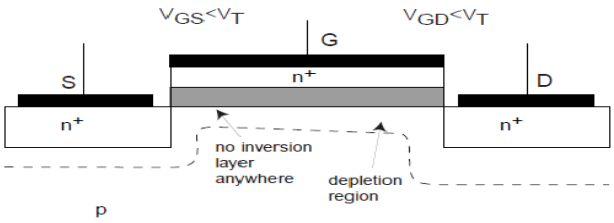


FIGURE 1.1.6

B.Linear or Triode regime:

• $V_{GS} > V_T$, $V_{GD} > V_T$, with $V_{DS} > 0$.

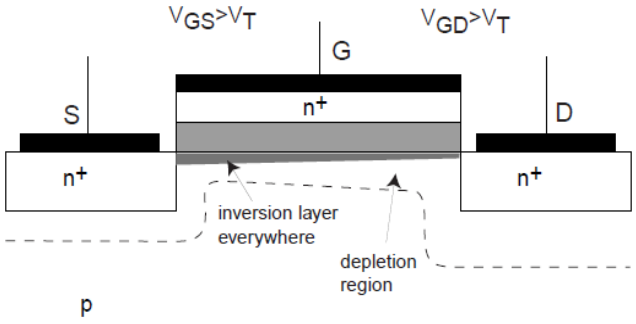


FIGURE 1.1.7

The transistor is turned on, and a channel has been created which allows current to flow between the drain and the source. The MOSFET operates like a resistor, controlled by the gate voltage relative to both the source and drain voltages. The current from drain to source is modeled as:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

Where μ_n is the charge-carrier effective mobility, W is the gate width, L is the gate length and C_{ox} is the gate oxide capacitance per unit area. The transition from the exponential sub threshold region to the triode region is not as sharp as the equations suggest.

C. Saturation Mode:

• $V_{GS} > V_T$, $V_{GD} < V_T$ ($V_{DS} > 0$).

ID independent of VDS: ID = IDsat

The drain voltage is higher than the gate voltage, the electrons spread out, and conduction is not through a narrow channel but through a broader, two- or three-dimensional current distribution extending away from the interface and deeper in the substrate. The onset of this region is also known as **pinch-off** to indicate the lack of channel region near the drain. The drain current is now weakly dependent upon drain voltage and controlled primarily by the gate–source voltage, and modeled approximately as:

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{th})^2\,(1 + \lambda(V_{DS} - V_{DSsat}))\,.$$

The additional factor involving λ, the channel-length modulation parameter, models current dependence on drain voltage due to the Early Effect or channel. According to this equation, a key design parameter, the MOSFET transconductance is:

$$g_m = \frac{2I_D}{V_{GS} - V_{th}} = \frac{2I_D}{V_{ov}},$$

where the combination $V_{ov} = V_{GS} - V_{th}$ is called the Overdrive voltage and where $V_{DSsat} = V_{GS} - V_{th}$ accounts for a small discontinuity in I_D which would otherwise appear at the transition between the triode and saturation regions.

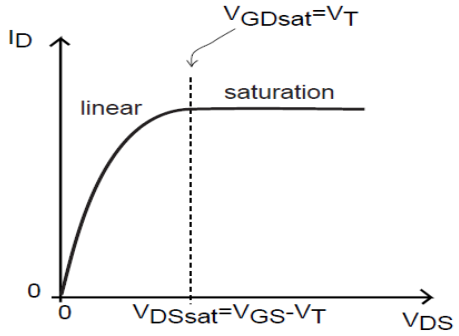


FIGURE 1.1.8

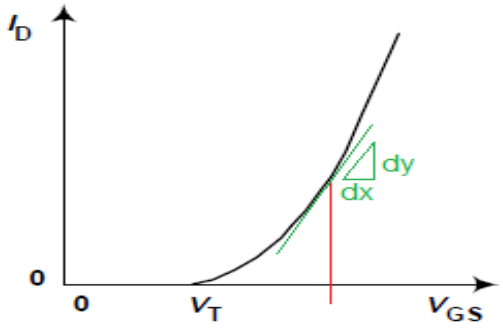


FIGURE 1.1.9

Key dependencies:
• V_{DS} increases -----→ ID increases (higher lateral electric field)
• V_{GS} increases ------→ ID increases (higher electron concentration)
• L increases -----→ ID decreases (lower lateral electric field)
• W increases -------→ ID increases (wider conduction channel)

DISADVANTAGES OF CONVENTIONAL MOSFETS

As the continuous down scaling of MOSFET device is required to increase the device speed and packaging density, but it degrades the device performance in terms of short channel effect and leakage current .To continue the scaling process there is need of device structure that provide better performance in deep submicron regime. Due to reduction in the channel length scaling, threshold voltage is decreasing that increasing the leakage current and short channel effects. First of all was excessive heating effect produced in the circuits. Furthermore they showed a large number of short channel effects which badly affected the performance. Scaling trend in CMOS approaching physical limits prompts the need for alternative device. With the technology scaling the MOSFET's channel length is reduced .as the channel length approaches the source-body and drain body depletion widths ,the charge in the channel due to these parasitic diodes become comparable to the depletion charge due to MOSFET gate-body voltage rendering the gate and body terminals to be less effective.

Some short channel effects are explained below:-
In particular five different short-channel effects can be distinguished:
1. Drain-induced barrier lowering
2. Surface scattering
3. Velocity saturation
4. Impact ionization
5. Hot electrons

➢ DIBL(Drain Induced Barrier Lowering)

Drain induced barrier lowering is a short channel effect in MOSFETs referring originally to a reduction of threshold voltage of the transistor at higher drain voltages. In a classic planar field-effect transistor with a long channel, the bottleneck in channel formation occurs far enough from the drain contact that it is electrostatically shielded from the drain by the combination of the substrate and gate, and so classically the threshold voltage was independent of drain voltage. The combined charge in the depletion region of the device and that in the channel of the device is balanced by three electrode charges: the gate, the source and the drain. As drain voltage is increased, the depletion region of the p-n junction between the drain and body increases in size and extends under the gate, so the drain assumes a greater portion of the burden of balancing depletion region charge, leaving a smaller burden for the gate. As a result, the charge present on the gate retains charge balance by attracting more carriers into the channel, an effect equivalent to lowering the threshold voltage of the device.

In effect, the channel becomes more attractive for electrons. In other words, the potential energy barrier for electrons in the channel is lowered. Hence the term "barrier lowering" is used to describe these phenomena. As channel length is reduced, the effects of DIBL in the subthreshold region (weak inversion) show up initially as a simple translation of the subthreshold current vs. gate bias curve with change in drain-voltage, which can be modeled as a simple change in threshold voltage with drain bias.

DIBL also affects the current vs. drain bias curve in the active mode, causing the current to increase with drain bias, lowering the MOSFET output resistance. This increase is additional to the normal channel length modulation effect on output resistance, and cannot always be modeled as a threshold adjustment.

➢ Surface scattering

As the channel length becomes smaller due to the lateral extension of the depletion layer into the channel region, the longitudinal electric field component increases, and the surface mobility becomes field-dependent. Since the carrier transport in a MOSFET is confined within the narrow inversion layer, and the surface scattering (that is the collisions suffered by the electrons that are accelerated toward the interface by E_x) causes reduction of the mobility, the electrons move with great difficulty parallel to the interface, so that the average surface mobility, even for small values of E_x, is about half as much as that of the bulk mobility.

➢ Velocity saturation

The performance short-channel devices are also affected by velocity saturation, which reduces the transconductance in the saturation mode. At low E_y, the electron drift velocity V_{de} in the channel varies linearly with the electric field intensity. Note that the drain current is limited by velocity saturation instead of pinchoff. This occurs in short channel devices when the dimensions are scaled without lowering the bias voltages.

➢ Impact ionization

Another undesirable short-channel effect, especially in NMOS, occurs due to the high velocity of electrons in presence of high longitudinal fields that can generate electron-hole (e-h) pairs by impact ionization, that is, by impacting on silicon atoms and ionizing them. It happens as follow: normally, most of the electrons are attracted by the drain, while the holes enter the substrate to form part of the parasitic substrate current. Moreover, the region between the source and the drain can act like the base of an npn transistor, with the source playing the role of the emitter and the drain that of the collector. If the aforementioned holes are collected by the source, and the corresponding hole current creates a voltage drop in the substrate material of the order of 6V, the normally reversed-biased substrate-source pn junction will conduct appreciably. Then electrons can be injected from the source to the substrate, similar to the injection of electrons from the emitter to the base. They can gain enough energy as they travel toward the drain to create new eh pairs. The situation can worsen if some electrons generated due to high fields escape the drain field to travel into the substrate, thereby affecting other devices on a chip.

➢ Hot electrons

Another problem, related to high electric fields, is caused by so-called hot electrons. These high energy electrons can enter the oxide, where they can be trapped, giving rise to oxide charging that can accumulate with time and degrade the device performance by increasing V_T and affect adversely the gate's control on the drain current.

Due to the above mentioned limitations in conventional MOSFETs we moved on to the next structure i.e. conventional SOI MOSFET.

1.2)SOI MOSFET

(A) SOI MOSFET stands for silicon on insulator MOSFETs.In such structures a semiconductor layer e.g. silicon, germanium is formed above an insulator layer which may be a buried oxide layer formed on a semiconductor substrate.

Types of SOI MOSFET:

- **Partially Depleted (PD)**
- **Fully Depleted (FD) SOI MOSFETs**

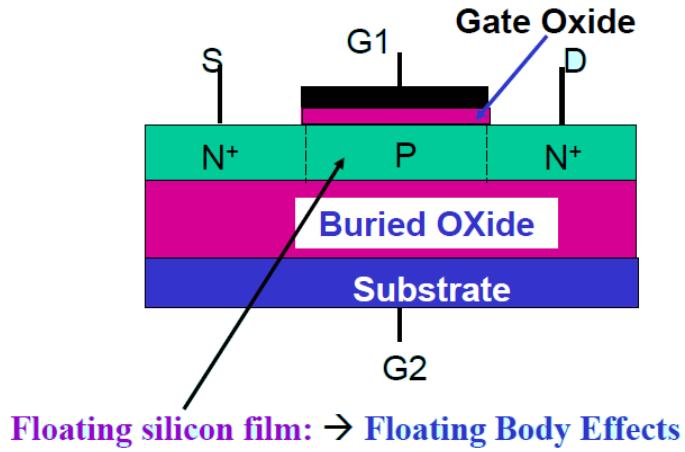


FIGURE 1.2.1 SOI MOSFET STRUCTURE

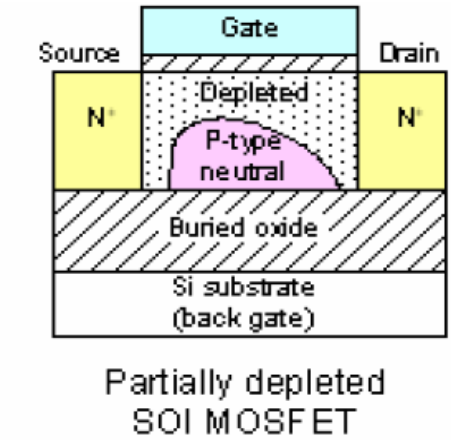


FIGURE 1.2.2

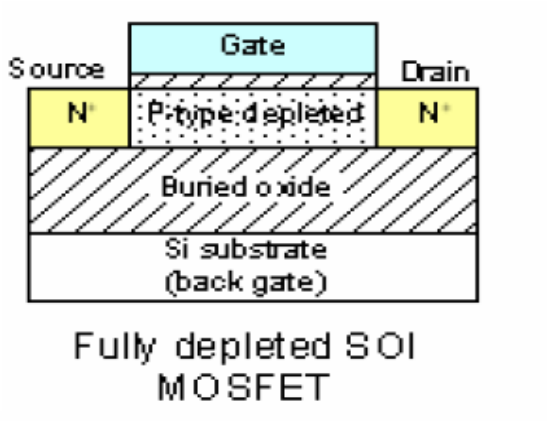
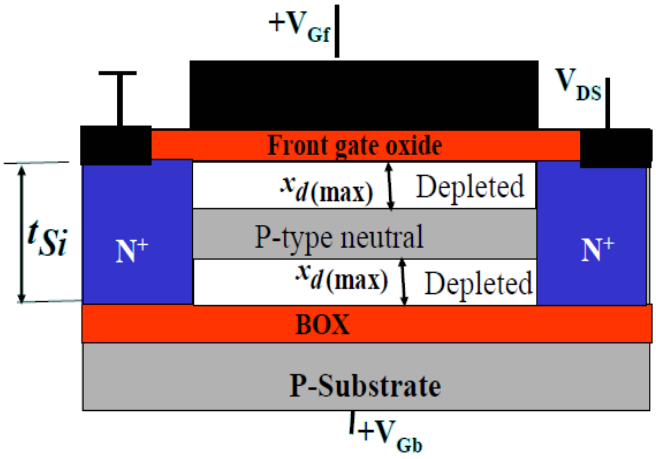


FIGURE1.2.3

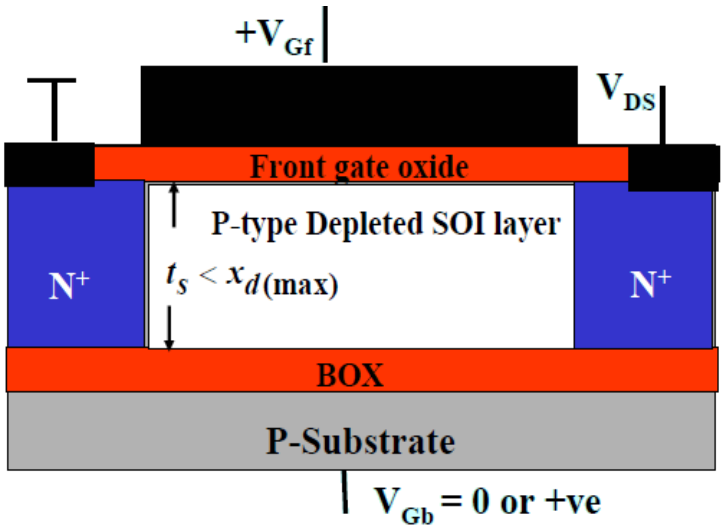
PARTIALLY DEPLETED SOI MOSFETS



The basic device equations of PD SOI MOSFETs are the same as for bulk devices, except of course from the complications arising from the floating body (FBE).

IN THIS CASE tsi<$2X_{d(max)}$)

FULLY DEPLETED SOI MOSFETS



In FDSOI case, the front and back channels are electro-statically coupled during device operation. This electrostatic coupling makes the front channel FD device parameters dependent on the back gate Voltage, including drain current, threshold voltage, sub-threshold slope etc.

ENERGY BAND DIAGRAMS OF PD AND FD SOI MOSFETS

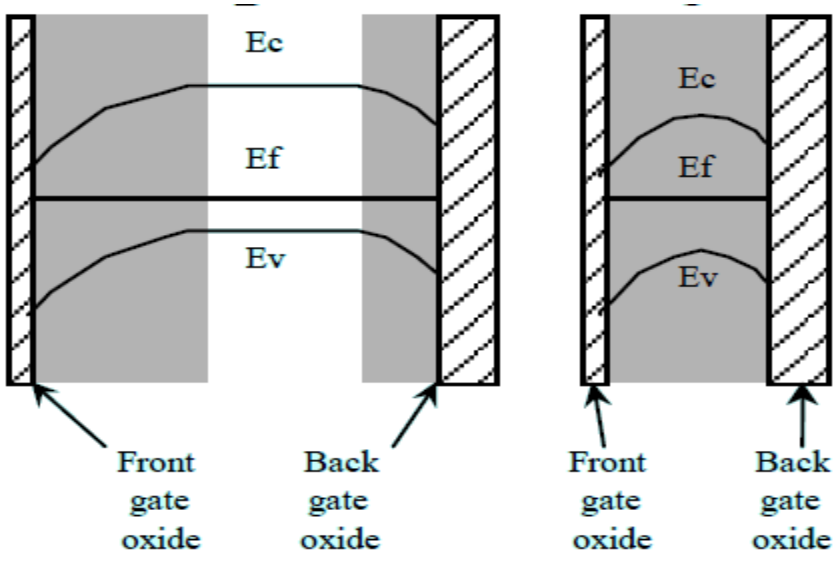
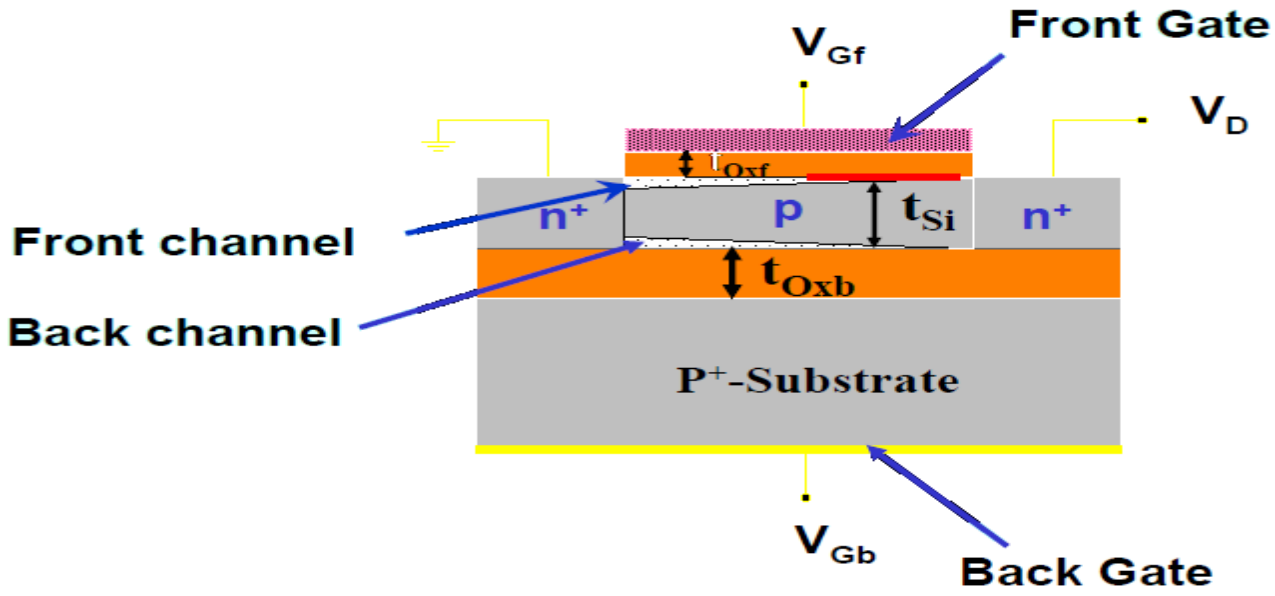


FIGURE 1.2.4

(Shaded regions are depleted)

FD SOI Device operation and Threshold Voltage analysis



LIMITATIONS OF CONVENTIONAL SOI MOSFETS

SOI-MOSFETs comes with many device related fabrication problems .Those are- Kink effect, Lattice heating and Subthreshold slope etc. The kink effect is characterized by the appearance kink in the output characteristics of an SOI-MOSFET. The kink appears above a certain drain voltage. SOI-MOSFETs are thermally insulated from the substrate by the buried insulator. SOI MOSFET's are thermally insulated from the substrate by the buried insulator. This arises because device is thermally insulated from the substrate by a buried oxide layer. Leads to substantial elevation in temperature which affects the output. This effect is called as Lattice heating.

Hence Recessed source /drain SOI was needed to reduce above limitations.

1.3)RECESSED SOURCE/DRAIN UTB SOI MOSFETS

Planar SOI MOSFETs show short channel effects that reduce or has detrimental effects on the electrical characteristics; hence with the advent of fully depleted utb SOI MOSFET with buried insulator underneath greater control has been achieved over these short channel effects. The major problem of short channel utb SOI MOSFETs is that they show high series resistance characteristics caused by ultra-thin source and drain regions .FD UTB SOI MOSFET with recessed s/d overcomes this problem by increasing source or drain thickness which is achieved by extending source/drain regions deeper into the buried oxide.

In comparison with the standard SOI MOSFETs, the special property of the ReS/D SOI MOSFETs is the coupling of the back-side of the silicon-body to the source and drain through the buried insulator. Additionally, these structures still exhibit substrate coupling in the direction perpendicular to wafer surface.
We derive a general expression for the front-gate surface potential distribution at the gate-oxide to- silicon-body interface and the back-gate surface potential distribution at the buried-oxide-to-silicon-body interface, that are fundamental for the modeling of SOI MOS devices. These expressions are then used to describe the surface threshold voltage of the Re S/D UTB SOI MOSFETs related to the front-gate and to analyze threshold voltage dependence on various device parameters, such as channel length, gate-oxide thickness, silicon-body, thickness, channel doping, and thickness of the source/drain extensions in the buried-oxide.

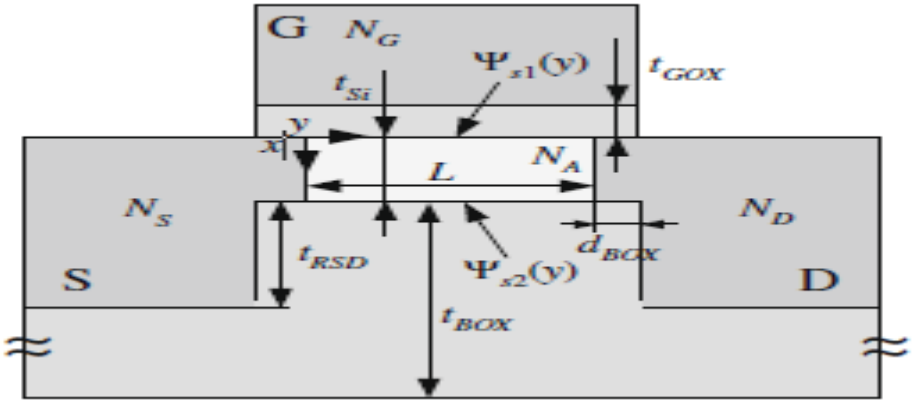


FIGURE 1.3.1

The characteristics of SOI-MOSFET can be studied by varying thickness of either silicon layer or oxide layer and the effect of change in threshold voltage values. Different characteristics curve between voltage and current, capacitance and voltage and thickness in silicon layer. The advantages of using SOI-MOSFET device to remove high parasitic capacitance values and latch effect thereby improving performance.

Chapter 2:SIMULATION METHOD USING ATLAS

All 3-D programs in ATLAS supports structures defined on 3D prismatic meshes. Structures may have arbitrary geometries in two dimensions and consist of multiple slices in the third dimension .There are two methods for creating a 3D structure that can be used with ATLAS. One way is through the command syntax of ATLAS. Another way is through an interface to DEVEDIT3D.

ATLAS Syntax for 3D Structure Generation

Mesh generation.

Conventionally, slices are made perpendicular to the Z axis. The mesh is triangular in XY but rectangular in XZ or YZ planes.

Region, Electrode, and Doping definition

To Define a Structure" also covers the definition of 2D regions, electrodes and doping profiles. To extend the regions into 3D, use the Z.MIN and Z.MAX parameters. For example:

```
REGION NUM=2 MATERIAL=Silicon X.MIN=0 X.MAX=1 Y.MIN=0 Y.MAX=1 Z.MIN=0 Z.MAX=1
ELECTRODE NAME=gate X.MIN=0 X.MAX=1 Y.MIN=0 Y.MAX=1 Z.MIN=0 Z.MAX=1
DOPING GAUSS N.TYPE CONC=1E20 JUNC=0.2 Z.MIN=0.0 Z.MAX=1.0
```

For 2D regions or electrodes defined with the command language, geometry is limited to rectangular shapes. Similarly, in 3D regions and electrodes are composed of rectangular parallelepipeds.

DevEdit3D Interface

DEVEDIT3D is a graphical tool that allows you to draw 3D device structures and create 3D meshes. It can also read 2D structures from ATHENA and extend them into 3D. These structures can be saved from DEVEDIT3D as structure files for ATLAS. Also, save a command file when using DEVEDIT3D. This file is used to recreate the 3D structure inside DEVEDIT3D, which is important, since DEVEDIT3Ddoesn't read in 3D structure files. ATLAS can read structures generated by DEVEDIT3D using the command:

```
MESH INF=<filename>
```

The program is able to distinguish automatically between 2D and 3D meshes read in using this command. Models and material parameters are chosen in 3-D in common with other 2-D modules using the MODELS, IMPACT, MATERIAL, MOBILITY, INTERFACE, and CONTACT statements.

The models available in 3D device simulation programs are

Mobility

- Table for 300K (CONMOB)
- Thomas (ANALYTIC)
- Arora's Model (ARORA)
- Klaassen's Model (KLAASSEN)
- Lombardi's Model (CVT)
- Yamaguchi Model (YAMA)
- Parallel Field Dependence (FLDMOB)
- Parallel Field Dependence with negative differential mobility (FLDMOB EVSATMOD=1)

Recombination

- Shockley Read Hall (SRH)
- Concentration dependent lifetime SRH (CONSRH)
- Klaassen's concentration dependent lifetime SRH (KLASRH)
- Auger (AUGER)
- Klaassen's concentration dependent Auger recombination model (KLAAUG)
- Optical Recombination (OPTR)
- Bulk and interface traps (TRAP, INTTRAP)
- Continuous defect states (DEFECT)

Generation

- Selberherr Impact Ionization (IMPACT SELB)
- Crowell Impact Ionization (IMPACT CROWELL)
- Hot Electron Injection (HEI)
- Fowler Nordheim Tunneling (FNORD)
- Single Event Upset (SINGLEEVENTUPSET)

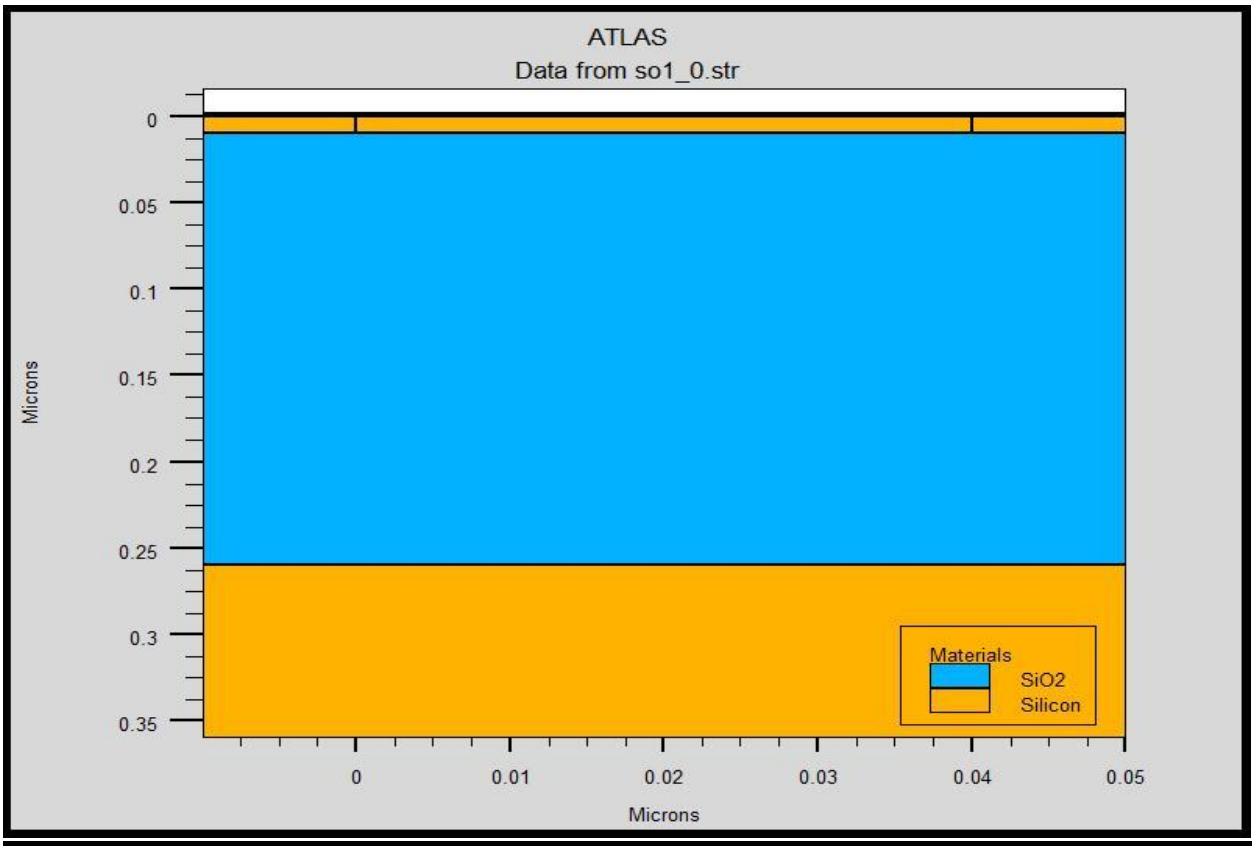
Carrier Statistics

- Boltzmann (default)
- Fermi (FERMI)
- Band Gap Narrowing (BGN)

•Incomplete Ionization (INCOMPLETE)
•Quantum Mechanical Effects (QUANTUM)

Chapter3:RESULTS AND DISCUSSIONS

3.1)Simulated Structure of conventional SOI MOSFET with channel length 40nm



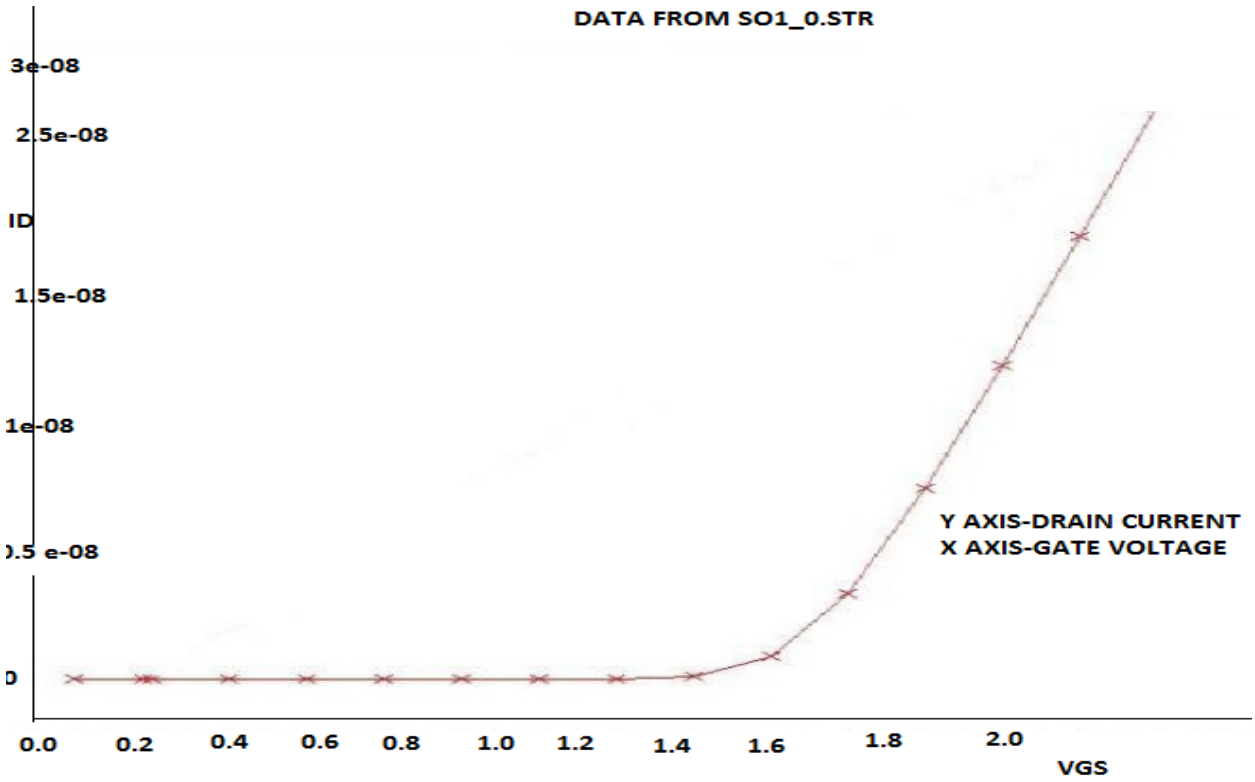
ANALYSIS

Region 1-silicon dioxide layer of 2nm at the top of source, drain and gate
Region 2-gate region of length 40 nm and width 10 nm
Region 3- buried oxide or sio2 layer of length 60nm and width 250nm
Region 4-substrate of si below insulator of length 60nm and width 100nm
Region 5-source region of length 10 nm and width 10nm
Region 6-drain region of length 10nm and width 10 nm
Hence by dividing the above structure into specific regions, we have been able to design the structure adequately. The box region is made up of sio2.and substrate is made up of silicon.
The doping concentration in region2---uniform, p-type $2x10^{17}$

The doping concentration in region 4------uniform, p-type, $2x10^{17}$
The doping concentration in region 5------uniform, n-type, 10^{20}
The doping concentration in region 6------uniform, n-type, 10^{20}

ELECTRICAL CHARACTERISTICS OF THE ABOVE GENERATED STRUCTURE

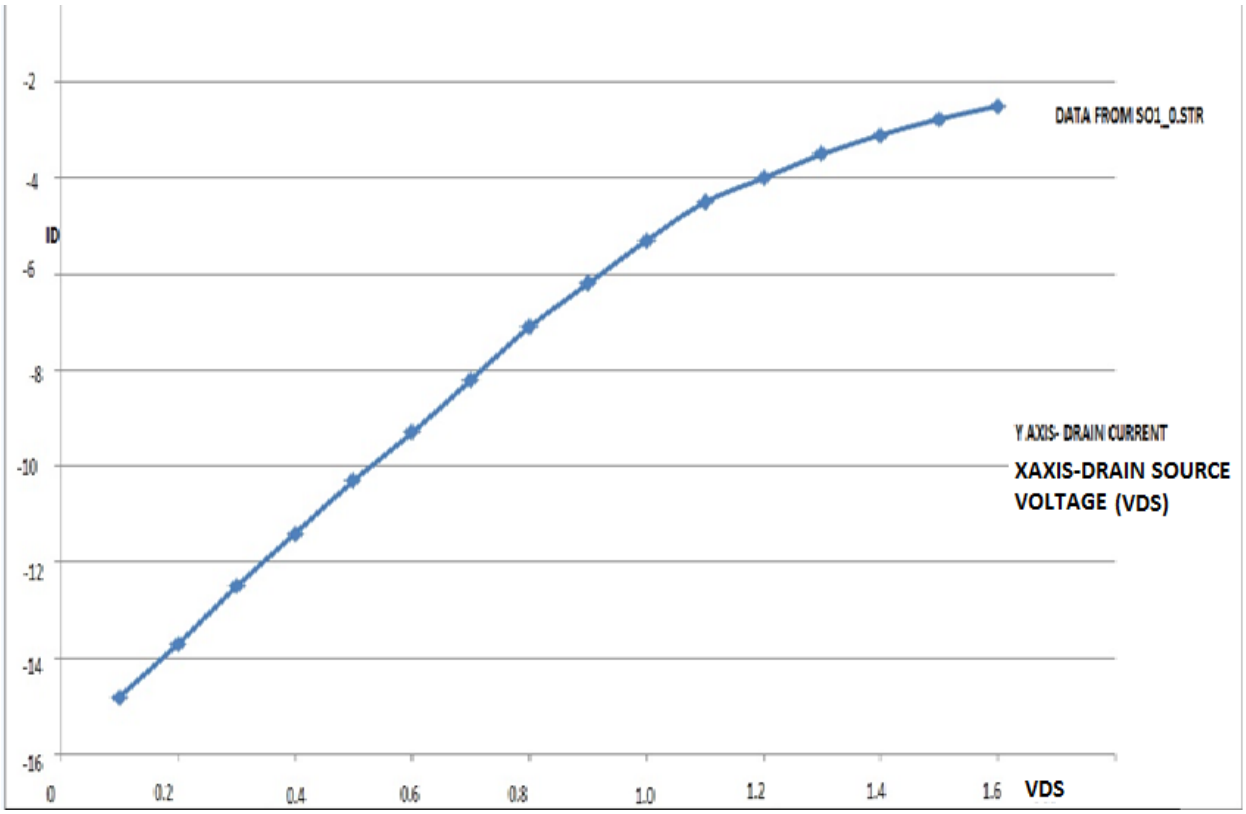
3.2)ID V/S V_{GS} CURVES (FIGURE 5(A).2)



ANALYSIS

The curve between drain current v/s gate voltage was plotted by taking a constant Vds=0.5v.different values of drain currents were obtained for different values of gate bias voltage. The above characteristics were obtained as shown in the above curve

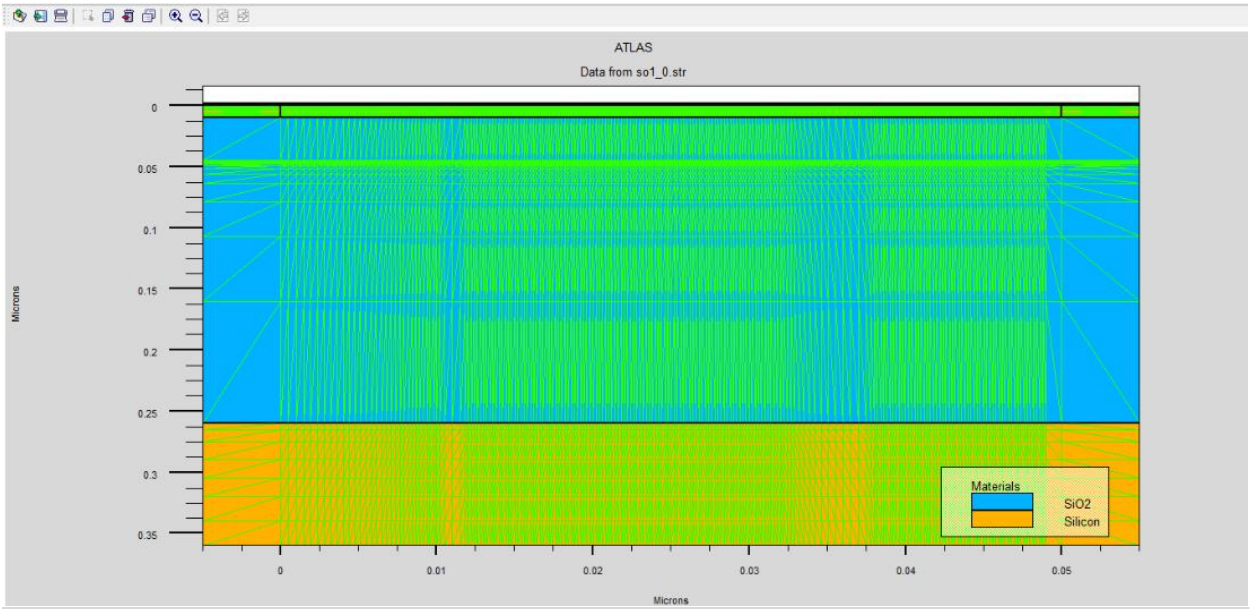
3.3)ID V/S VDS CURVE

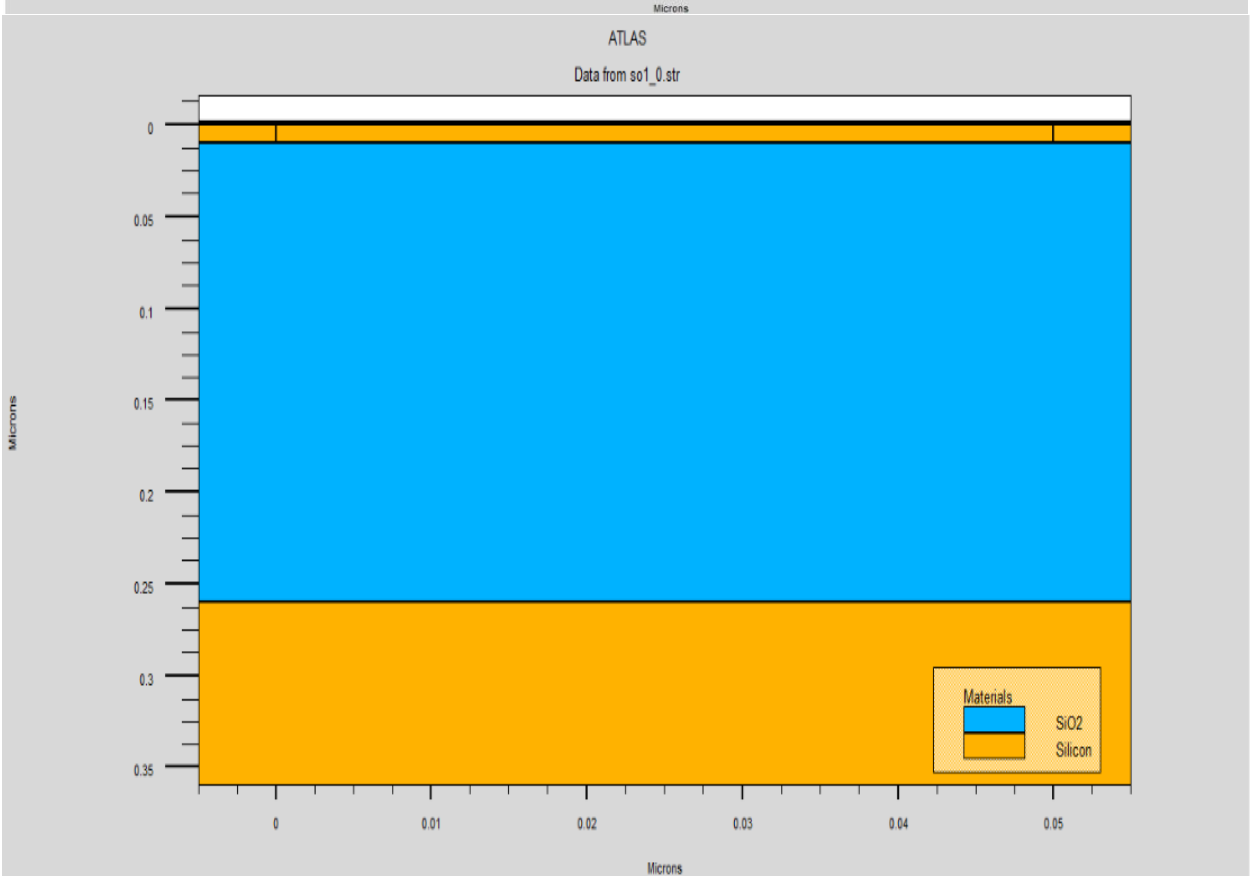


ANALYSIS

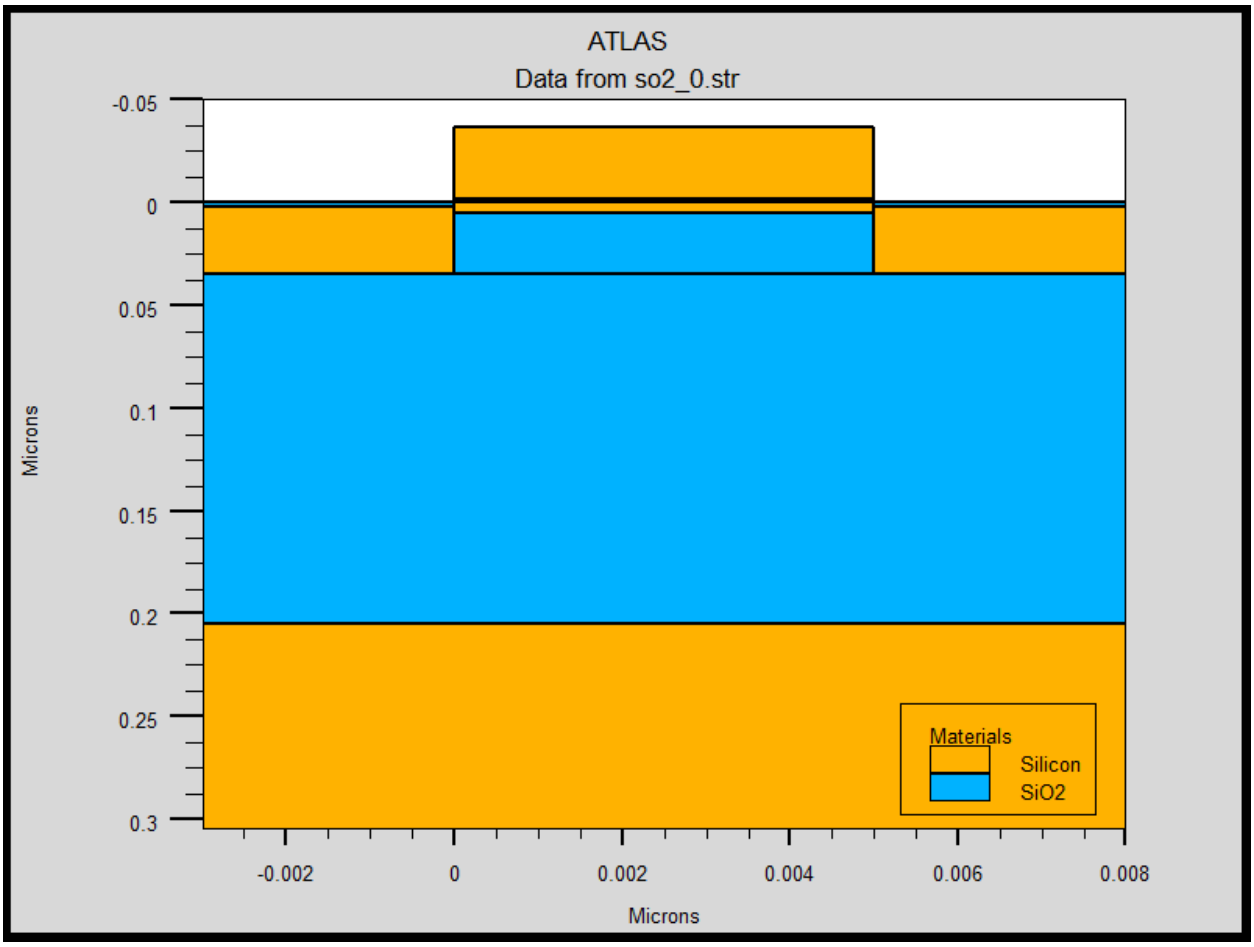
The curve between drain current and drain voltage was obtained for a constant value of gate voltage i.e. v_{gs}=0.5v different values of drain current i.e. id values were obtained for different values of drain source voltage. Hence the corresponding curve was plot using the data obtained from atlas software. In recessed source/drain utb SOI MOSFET the drain and source regions are extended into buried oxide region as a result increasing the area of cross section keeping length constant .we know R=ρ.L/A, as A increases with l and ρ remaining constant so R value also decreases .Rseries of the aforementioned structure is summation of Rsource, Rdrain and Rgate . Rsource and Rdrain decreases so overall Rseries also decreases. From ohm's law V=I.R.R decreases hence resulting in greater values of drain current for the same values of drain source voltages as in FDSOI MOSFETs.

Simulated structure of conventional SOI MOSFET with channel length 50nm





3.4)Simulated structure of Recessed source /drain SOI MOSFET with channel length 5nm



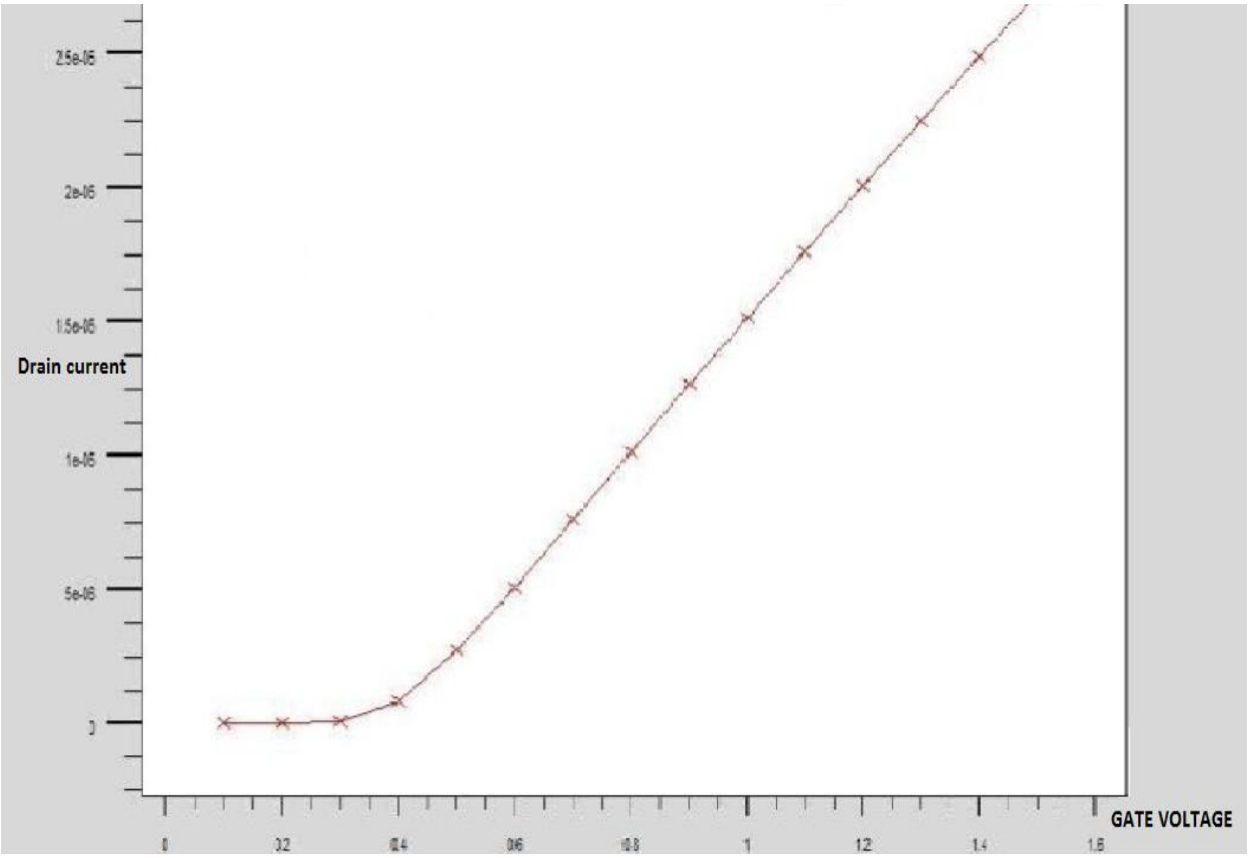
ANALYSIS

Region 1 refers to gate having width 35nm and length 5nm.
Region 3 refers to source having width 35nm and length 3nm
Region 4 refers to drain having width 35nm and length 3nm.
Region 5 refers to a silicon channel width 5nm and length 5nm
Region 6 and 7 refers to buried oxide layer.
In this structure we call it as recessed source/drain as because the source and drain have got extended into buried oxide region by 30nm.

Region 8 refers to the substrate having width 100nm and length 11nm.
trsd=30nm tbox=200nm dbox=0 tgox=2nm tsi=5nm

ELECTRICAL CHARACTERISTICS OF RECESSED SOURCE/DRAIN UTB SOI MOSFETS

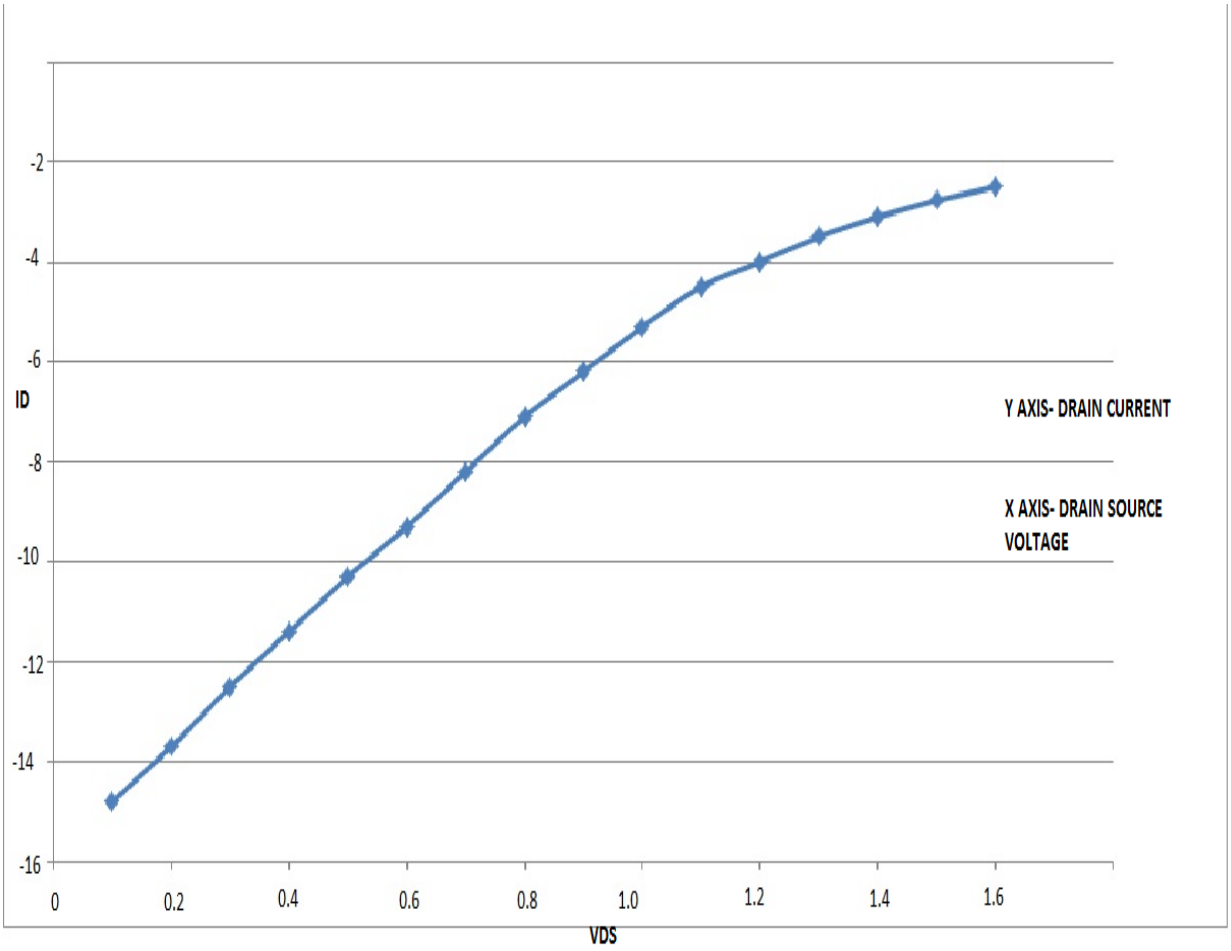
3.5)ID VS VGS CURVE.



ANALYSIS

The curve between drain current vs gate voltage was plotted by taking a constant vds=0.5v.Different values of drain currents were obtained for different values of gate bias voltage. So the above characteristics were obtained as shown in the above curve.

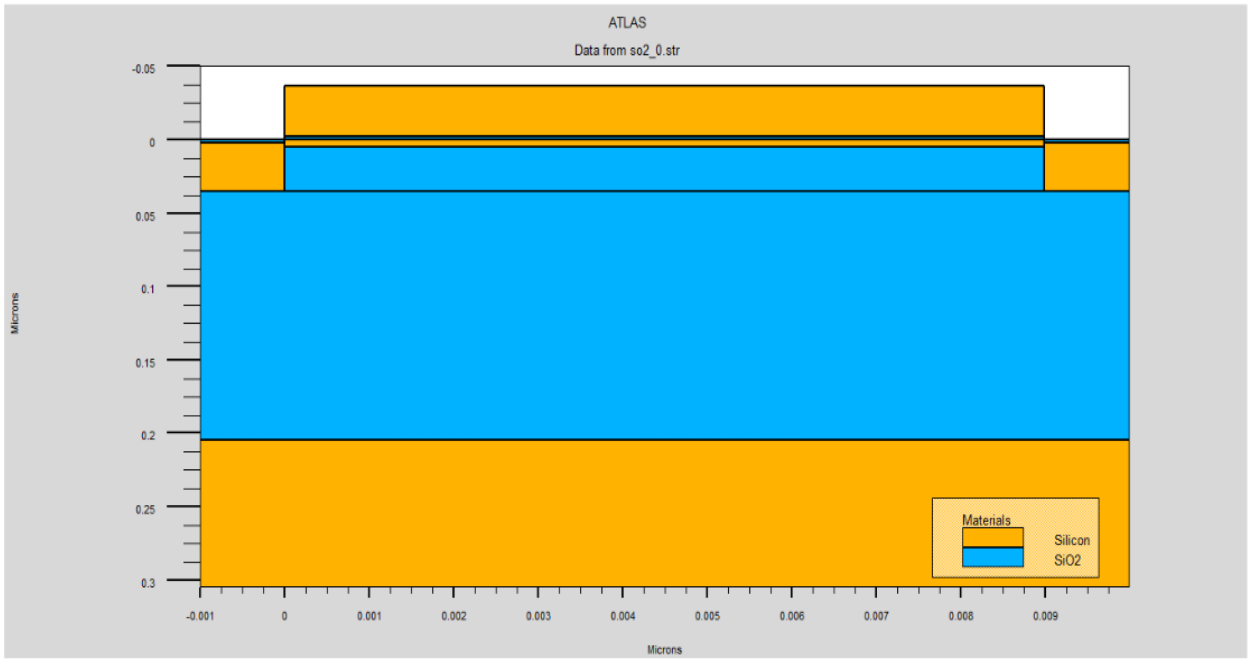
3.6)ID VS VDS CURVE

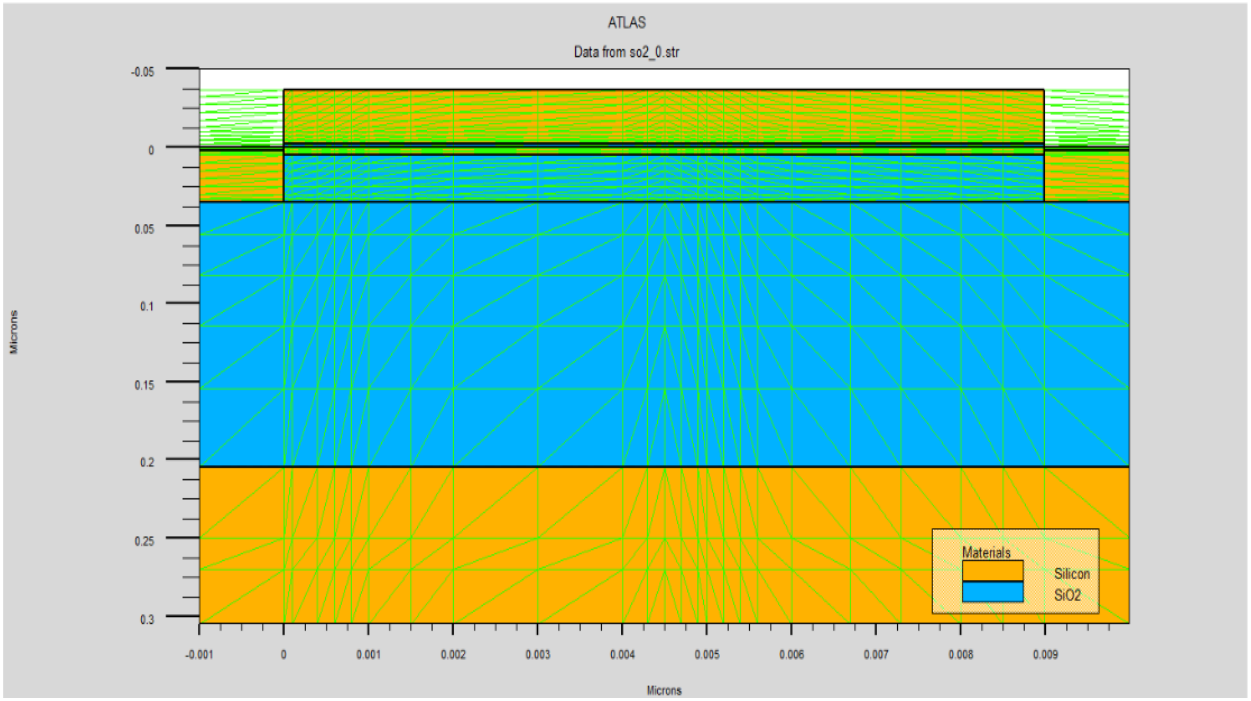


ANALYSIS

The curve between drain current and drain voltage was obtained for a constant value of gate voltage i.e. v_{gs}=0.5v different values of drain current i.e. id values were obtained for different values of drain source voltage .Hence the corresponding curve was plot using the data obtained from atlas software.

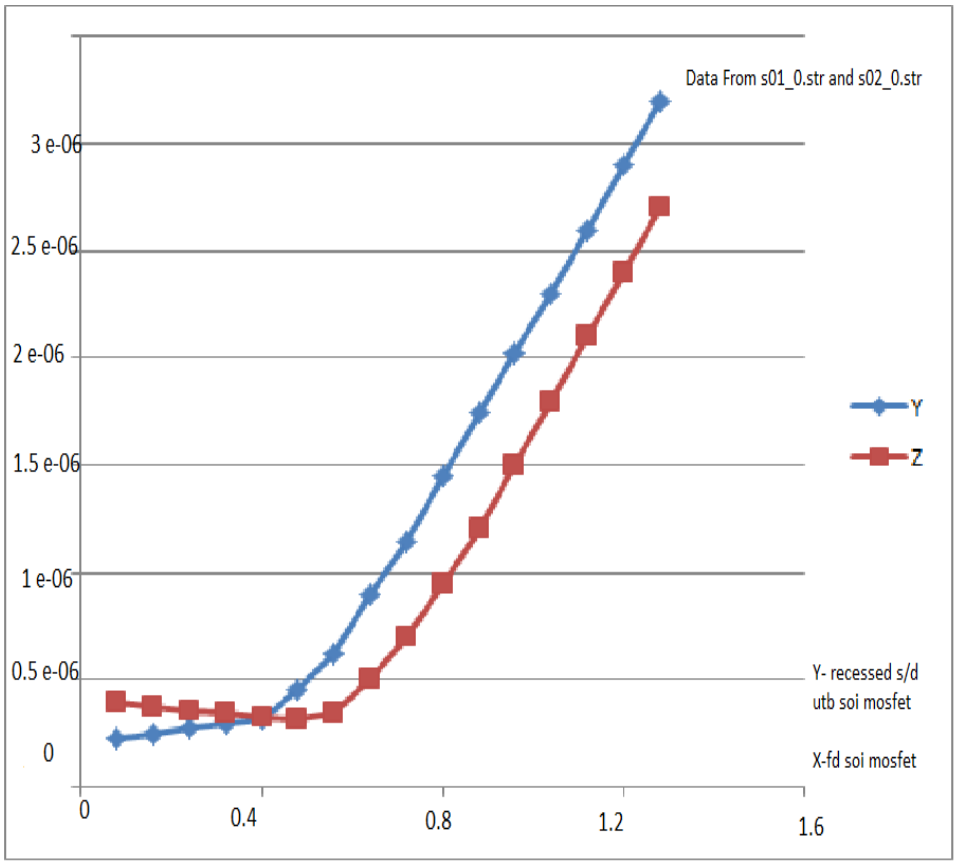
Simulated structure of Recessed source/drain SOI MOSFET with channel length 9nm





3.7)COMPARITATIVE STUDY OF ELECTRICAL CHARACTERISTICS OF FDSOI MOSFET AND RECESSED SOURCE/DRAIN UTB SOI MOSFET

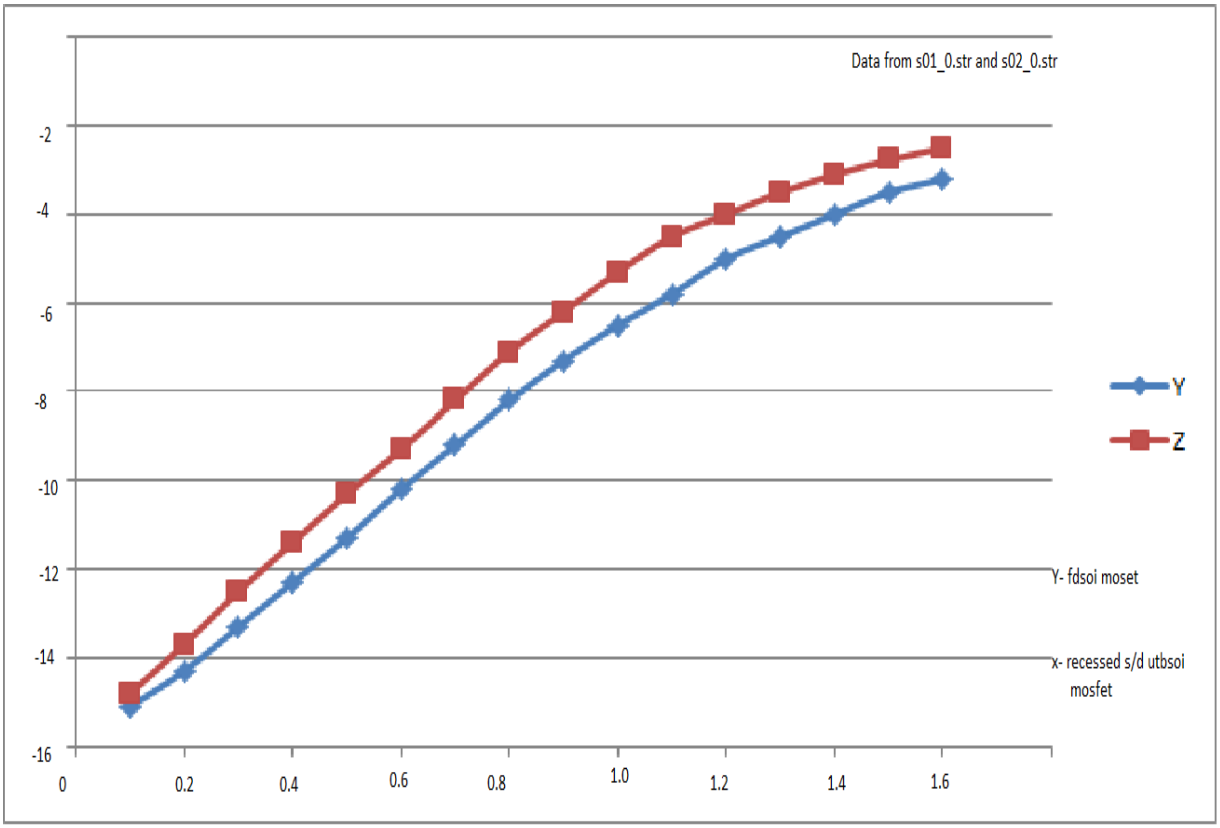
DIFFERENCE BETWEEN I_D AND V_{GS} CURVES



ANALYSIS

In recessed source/drain utb SOI MOSFET the drain and source regions are extended into buried oxide region as a result increasing the area of cross section keeping length constant .we know R=ρ.L/A, as A increases with L and ρ remaining constant so R value also decreases. R_{series} of the aforementioned structure is summation of R_{source}, R_{drain} and R_{gate} . R_{source} and R_{drain} decreases so overall R_{series} also decreases. From ohm's law V=I.R.R decreases hence resulting in greater values of current for the same values of gate voltages as in FDSOI MOSFETs.

3.8)DIFFERENCE BETWEEN I_D VS V_{DS} CURVES



ANALYSIS

In recessed source/drain utb SOI MOSFET the drain and source regions are extended into buried oxide region as a result increasing the area of cross section keeping length constant .we know R=ρ.l/A, as A increases with l and ρ remaining constant so R value also decreases.R_{series} of the aforementioned structure is summation of R_{source}, R_{drain} and R_{gate} . R_{source} and R_{drain} decreases so overall R_{series} also decreases. From ohm's law V=I.R.R decreases hence resulting in greater values of drain current for the same values of drain source voltages as in FDSOI MOSFETs.

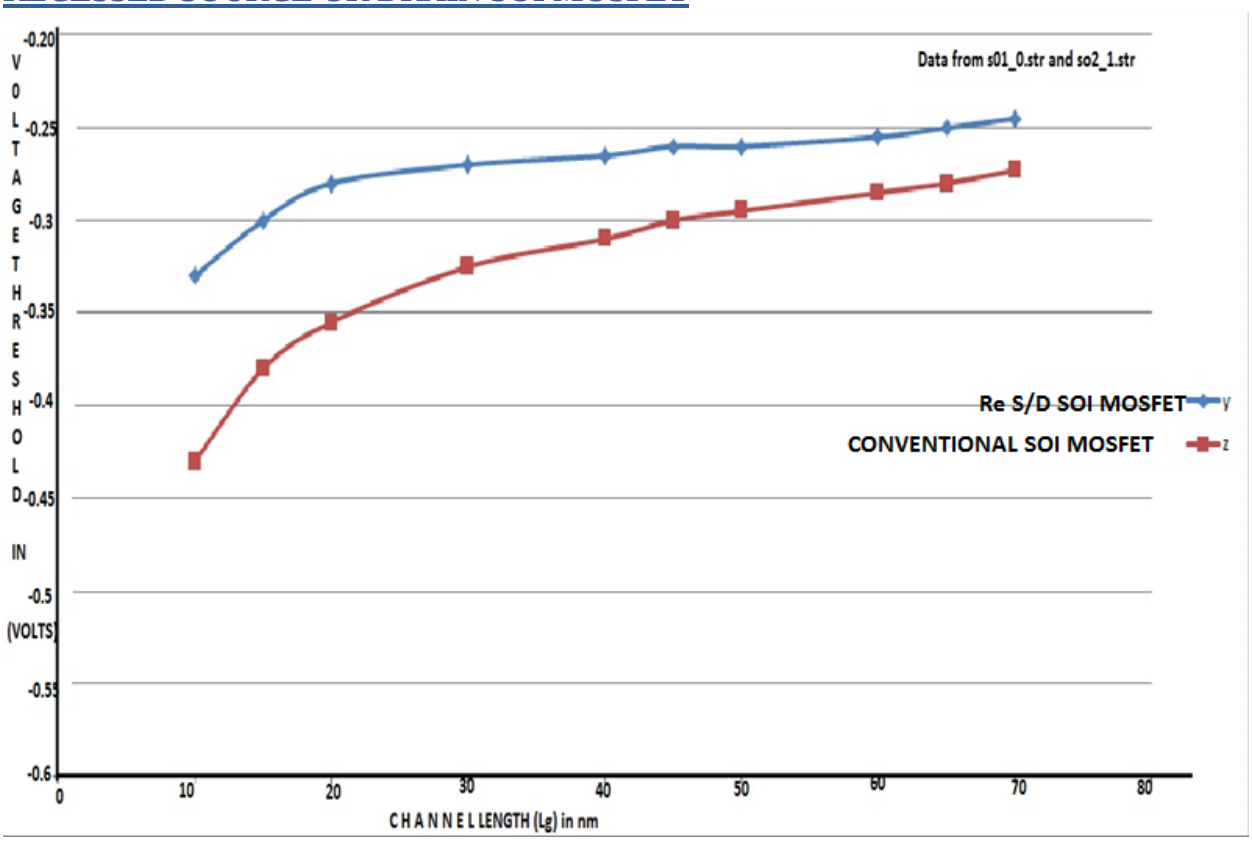
3.9)THRESHOLD VOLTAGE OF RECESSED SOURCE/DRAIN SOI MOSFETS

Threshold voltage is the value of the gate voltage for which the minimum surface potential equals the value of $2\psi_b$, where $\psi_b = (kT/q)\ln(N_A/ni)$ is the difference between the extrinsic Fermi level in the channel region and the intrinsic Fermi level .In the case of the Re S/D UTB SOI MOSFETs, the inversion channel can be formed at the back-interface of the channel region while the front interface is still depleted ,due to its coupling with the n+ source and drain regions. Therefore, the threshold value is defined in a more general manner as the gate voltage V_G at which the larger of the minimum front-gate surface potential $\psi_{s1(y = ymin,s1)}$ and the minimum of the back-gate surface
Potential $\psi_{s2(y = ymin,s2)}$ equals $2\psi_b$.

$$V_{th} = V_G\big|_{\max\left[\Psi_{s1}(y=y_{min,s1}),\Psi_{s2}(y=y_{min,s2})\right]=2\Psi_b}$$

Solving this we obtain values for threshold voltage.

COMPARISION BETWEEN VOLTAGE THRESHOLDS OF FDSOI MOSFET AND RECESSED SOURCE OR DRAIN SOI MOSFET



ANALYSIS

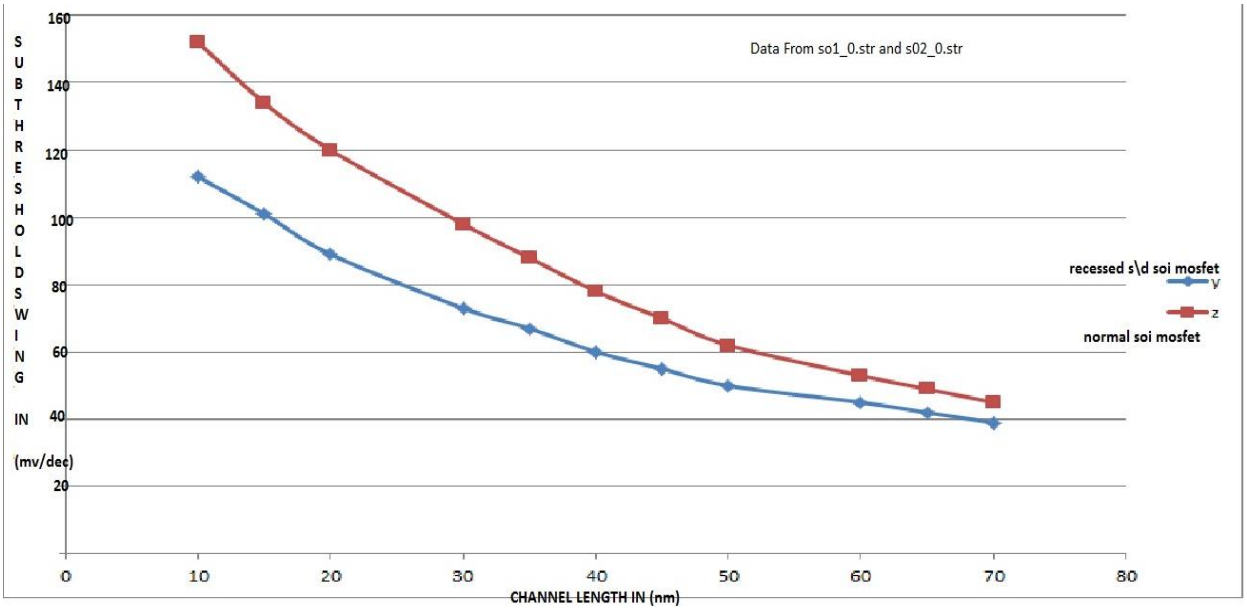
Dependence of the threshold voltage on device parameters such as gate-oxide thickness, silicon-body doping, silicon-body thickness, buried-oxide thickness, and thickness of the source/drain extensions in the buried-oxide .With the reduction of gate-oxide thickness t_{GOX}, the threshold voltage increases and the short-channel immunity significantly improves. By decreasing gate-oxide thickness, C_{GOX} is increased and the front-gate has the predominant control of the channel potential over the complete body thickness and the back-gate surface potential is also predominantly controlled by the front-gate rather than the back-gate (source and drain). The increase in silicon-body doping concentration N_A induces the threshold voltage shift to more positive values and the threshold voltage roll-off becomes smaller due to the reduced drain-field penetration inside the channel. In the case of thinner silicon-body .the back-gate surface potential is again influenced more by the front-gate and thus, the short-channel immunity improves and the threshold voltage increases. As the buried-oxide thickness t_{BOX} is reduced, Vth increases, but the short-channel immunity is slightly decreased since relatively larger portion of the gate bias is now expended over the buried-oxide as can be seen from the capacitance ratios in body factors for the both front-side and back-side inversion .

The change in thickness of the source/drain extensions in the buried-oxide t_{RSD} has little influence on the threshold voltage allowing significant freedom in the design of the source/drain extensions in the buried-oxide region with respect to the threshold voltage. In the case of zero source/drain extensions in the buried-oxide ($t_{RSD} = 0$), the device structure becomes the conventional UTB SOI MOSFET. The value of the recessed source/drain buried-oxide capacitance is now calculated from the relation with $\theta=\pi$, which accounts for the lateral component of electric field inside the buried-oxide. The comparison of the Vth for two Re S/D SOI devices with different depth of their recessed regions as well as conventional UTB SOIMOSFET in proves the accuracy of our model and its applicability to the UTB SOI MOSFETs ($t_{RSD} = 0$).

3.10)SUBTHRESHOLD SWING

The sub-threshold swing $S = \partial V_G / \partial \log_{10} I_D$ in a MOSFET may *decrease* significantly as gate length L_G is reduced before increasing catastrophically when L_G becomes so short that punch through current flows. The effect is largest in devices with lightly doped substrates, deep source/drain junctions, and heavy threshold adjust implants operated at high drain bias. An explanation for the effect is provided in terms of sharing of the depletion region charge between gate and drain.

COMPARISION BETWEEN VOLTAGE THRESHOLDS OF FDSOI MOSFET AND RECESSED SOURCE OR DRAIN SOI MOSFET



ANALYSIS

From the above curve it is quite evident that the sub threshold swing of recessed source/drain in millivolts per decade will be lesser in comparison to that of FD SOI MOSFETs for the same changes in channel length.

FUTURE SCOPE

Furthermore we can also do the physical modeling of SOI MOSFETs. To master the design technologies for achieving competitive systems with increasing functionality, performance and complexity, without compromising on reliability, energy consumption and costs of such systems; it is necessary to develop new design and architecture paradigms both for emerging device and their integration at large scale. Integration at high density is a big challenge, as different types of Nanotubes and materials are to be considered so that they comply with the planar technology which is still the basis of CMOS ICs for the future decade. The era beyond CMOS is yet close to start. If some efforts are being made to maintain the advanced CMOS technology, it cannot go beyond few decades. Hence emerging devices should be considered in order to comply with technology developments in the near and far future. Engineered devices and materials will stretch the roadmap for few decades. Lot of researches are being done to design and implement reliable and durable HDIC

APPENDIX

1.Software modeling for FDSOI MOSFETwith channel length equals to 40nm

```
go atlas
mesh space.mult=1.0
X.mesh loc=-0.01 spac=0.05
x.mesh loc=0.00 spac=0.0005
x.mesh loc=0.01 spac=0.0002
x.mesh loc=0.011 spac=0.0005
x.mesh loc=0.012 spac=0.0002
x.mesh loc=0.015 spac=0.0002
x.mesh loc=0.016 spac=0.0002
x.mesh loc=0.018 spac=0.0002
x.mesh loc=0.020 spac=0.0002
x.mesh loc=0.022 spac=0.0002
x.mesh loc=0.024 spac=0.0002
x.mesh loc=0.026 spac=0.0002
x.mesh loc=0.028 spac=0.0002
x.mesh loc=0.032 spac=0.0002
x.mesh loc=0.036 spac=0.0005
x.mesh loc=0.037 spac=0.0005
x.mesh loc=0.038 spac=0.0002
x.mesh loc=0.04 spac=0.05
x.mesh loc=0.042 spac=0.02
x.mesh loc=0.043 spac=0.02
y.mesh loc=0.045 spac=0.02
y.mesh loc=0.047 spac=0.02
x.mesh loc=0.048 spac=0.02
x.mesh loc=0.049 spac=0.02
x.mesh loc=0.05 spac=0.05

y.mesh loc=-0.002 spac=0.02
y.mesh loc=0.00 spac=0.02
y.mesh loc=0.001 spac=0.02
y.mesh loc=0.0012 spac=0.02
y.mesh loc=0.0013 spac=0.02
y.mesh loc=0.0014 spac=0.02
y.mesh loc=0.0025 spac=0.02
y.mesh loc=0.0026 spac=0.02
y.mesh loc=0.0037 spac=0.02
y.mesh loc=0.0038 spac=0.02
y.mesh loc=0.0049 spac=0.02
y.mesh loc=0.0055 spac=0.02
y.mesh loc=0.0064 spac=0.02
y.mesh loc=0.0072 spac=0.02
y.mesh loc=0.0080 spac=0.02
y.mesh loc=0.0088 spac=0.02
y.mesh loc=0.0096 spac=0.02
y.mesh loc=0.0099 spac=0.02
y.mesh loc=0.01 spac=0.05
y.mesh loc=0.26 spac=0.10
y.mesh loc=0.265 spac=0.02
y.mesh loc=0.275 spac=0.02
```

```
y.mesh loc=0.29 spac=0.02
y.mesh loc=0.32 spac=0.02
y.mesh loc=0.34 spac=0.02
y.mesh loc=0.36 spac=0.10

region number=1 x.min=-0.01 x.max=0.05  y.min=-0.002 y.max=0.00 SiO2
region number=2 x.min=0.00 x.max=0.04  y.min=0.00 y.max=0.01    silicon
region number=3 x.min=-0.01 x.max=0.05  y.min=0.01 y.max=0.26     SiO2
region number=4 x.min=-0.01 x.max=0.05  y.min=0.26 y.max=0.36    silicon
region number=5 x.min=-0.01 x.max=0.00  y.min=0.00 y.max=0.01    silicon
region number=6 x.min=0.04 x.max=0.05  y.min=0.00 y.max=0.01   silicon

electrode name=source number=5 x.min=-0.01 x.max=0.00 y.min=0.00 y.max=0.01 neutral
electrode name=drain  number=6 x.min=0.04 x.max=0.05 y.min=0.00 y.max=0.01 neutral
electrode name=gate   number=1 x.min=0.00 x.max=0.04 y.min=-0.002 y.max=-0.002 neutral

doping uniform conc=1e17 p.type reg=2
doping uniform conc=1e17 p.type reg=4
doping uniform conc=1e20 n.type reg=5
doping uniform conc=1e20 n.type reg=6

save outf = so1_0.str

tonyplot so1_0.str -set so1_0.set

contact name=drain
contact name=source
contact name=gate workfunction=4.7
contact name=substrate


models       conmob srh auger bgn fldmob print

solve init

method       newton    trap
log         outf=so1_1.log
solve        prev
solve        vgate=-0.02
solve        vdrain=0.5
solve        vdrain=0.01

solve       vgate=0.1 vstep=0.1 name=gate vfinal=1.5
tonyplot    so1_1.log -set so1_1.set


quit
```

2. SOFTWARE CODING TO GENERATE FDSOI MOSFET WITH CHANNEL LENGTH EQUALS TO 50nm

```
go atlas
mesh space.mult=1.0
X.mesh loc=-0.0 spac=0.05
x.mesh loc=0.00 spac=0.0005
x.mesh loc=0.01 spac=0.0002
x.mesh loc=0.011 spac=0.0005
x.mesh loc=0.012 spac=0.0002
x.mesh loc=0.015 spac=0.000205
x.mesh loc=0.016 spac=0.0002
x.mesh loc=0.018 spac=0.0002
x.mesh loc=0.020 spac=0.0002
x.mesh loc=0.022 spac=0.0002
x.mesh loc=0.024 spac=0.0002
x.mesh loc=0.026 spac=0.0002
x.mesh loc=0.028 spac=0.0002
x.mesh loc=0.032 spac=0.0002
x.mesh loc=0.036 spac=0.0005
x.mesh loc=0.037 spac=0.0005
x.mesh loc=0.038 spac=0.0002
x.mesh loc=0.042 spac=0.0002
x.mesh loc=0.043 spac=0.0002
y.mesh loc=0.045 spac=0.0002
y.mesh loc=0.047 spac=0.0002
x.mesh loc=0.048 spac=0.0002
x.mesh loc=0.049 spac=0.0002
x.mesh loc=0.05 spac=0.05
x.mesh loc=0.055 spac=0.05

y.mesh loc=-0.002 spac=0.02
y.mesh loc=0.00 spac=0.02
y.mesh loc=0.001 spac=0.02
y.mesh loc=0.0012 spac=0.02
y.mesh loc=0.0013 spac=0.02
y.mesh loc=0.0014 spac=0.02
y.mesh loc=0.0025 spac=0.02
y.mesh loc=0.0026 spac=0.02
y.mesh loc=0.0037 spac=0.02
y.mesh loc=0.0038 spac=0.02
y.mesh loc=0.0049 spac=0.02
y.mesh loc=0.0055 spac=0.02
y.mesh loc=0.0064 spac=0.02
y.mesh loc=0.0072 spac=0.02
y.mesh loc=0.0080 spac=0.02
y.mesh loc=0.0088 spac=0.02
y.mesh loc=0.0096 spac=0.02
y.mesh loc=0.0099 spac=0.02
y.mesh loc=0.01 spac=0.05
y.mesh loc=0.26 spac=0.10
y.mesh loc=0.265 spac=0.02
y.mesh loc=0.275 spac=0.02
y.mesh loc=0.29 spac=0.02
```

```
y.mesh loc=0.32 spac=0.02
y.mesh loc=0.34 spac=0.02
y.mesh loc=0.36 spac=0.10

region number=1 x.min=-0.005 x.max=0.055  y.min=-0.002 y.max=0.00 SiO2
region number=2 x.min=0.00 x.max=0.05  y.min=0.00 y.max=0.01    silicon
region number=3 x.min=-0.005 x.max=0.055  y.min=0.01 y.max=0.26     SiO2
region number=4 x.min=-0.005 x.max=0.055  y.min=0.26 y.max=0.36    silicon
region number=5 x.min=-0.005 x.max=0.00  y.min=0.00 y.max=0.01    silicon
region number=6 x.min=0.05 x.max=0.055  y.min=0.00 y.max=0.01   silicon

electrode name=source number=5 x.min=-0.005 x.max=0.00 y.min=0.00 y.max=0.01 neutral
electrode name=drain  number=6 x.min=0.05 x.max=0.055 y.min=0.00 y.max=0.01 neutral
electrode name=gate   number=2 x.min=0.00 x.max=0.05 y.min=-0.002 y.max=-0.002 neutral

doping uniform conc=1e17 p.type reg=2
doping uniform conc=1e17 p.type reg=4
doping uniform conc=1e20 n.type reg=5
doping uniform conc=1e20 n.type reg=6

save outf = so1_0.str

tonyplot so1_0.str -set so1_0.set

contact name=drain
contact name=source
contact name=gate workfunction=4.7
contact name=substrate


models       conmob srh auger bgn fldmob print

solve init

method       newton    trap
log         outf=so1_1.log
solve        prev
solve        vgate=-0.02
solve        vdrain=0.5
solve        vdrain=0.01

solve       vgate=0.1 vstep=0.1 name=gate vfinal=1.5
tonyplot    so1_1.log -set so1_1.set


quit
```

3.SOFTWARE CODE FOR RECESSED S/D SOI MOSFET with channel length 5nm

```
go atlas
        mesh space.mult=1.0

        x.mesh loc=-0.003   spac=0.05
        x.mesh loc=-0.0025   spac=0.05
        x.mesh loc=-0.0020   spac=0.02
        x.mesh loc=-0.0010  spac=0.02
        x.mesh loc=-0.0008   spac=0.02
        x.mesh loc=-0.0006   spac=0.02
        x.mesh loc=-0.0005   spac=0.02
        x.mesh loc=-0.0003   spac=0.02
        x.mesh loc=-0.0001   spac=0.02
        x.mesh loc=0.00     spac=0.05
        x.mesh loc=0.0001    spac=0.02
        x.mesh loc=0.0004    spac=0.02
        x.mesh loc=0.0006    spac=0.02
        x.mesh loc= 0.0008   spac=0.02
        x.mesh loc=0.001    spac=0.02
        x.mesh loc=0.0015    spac=0.02
        x.mesh loc=0.002    spac=0.02
        x.mesh loc=0.003   spac=0.02
        x.mesh loc=0.004   spac=0.02
        x.mesh loc=0.0043    spac=0.02
        x.mesh loc=0.0045    spac=0.02
        x.mesh loc=0.0047    spac=0.02
        x.mesh loc=0.0049    spac=0.02
        x.mesh loc=0.005    spac=0.02
        x.mesh loc=0.0052    spac=0.02
        x.mesh loc=0.0054    spac=0.02
        x.mesh loc=0.0056    spac=0.02
        x.mesh loc=0.006    spac=0.02
        x.mesh loc=0.0067    spac=0.02
        x.mesh loc=0.0073    spac=0.02
        x.mesh loc=0.008



        y.mesh loc=-0.037    spac=0.02
        y.mesh loc=-0.032    spac=0.02
        y.mesh loc= -0.027   spac=0.02
        y.mesh loc=-0.022    spac=0.02
        y.mesh loc=-0.017    spac=0.02
        y.mesh loc=-0.013    spac=0.02
        y.mesh loc=-0.010   spac=0.02
        y.mesh loc=-0.007   spac=0.02
        y.mesh loc=-0.005    spac=0.02
        y.mesh loc=-0.004   spac=0.02
        y.mesh loc=-0.002    spac=0.02
        y.mesh loc=0.00    spac=0.05
        y.mesh loc=0.001   spac=0.05
        y.mesh loc=0.002    spac=0.02
        y.mesh loc=0.003    spac=0.02
        y.mesh loc=0.004    spac=0.02
        y.mesh loc=0.005    spac=0.02
```

```
y.mesh loc=0.010    spac=0.05
y.mesh loc=0.015    spac=0.05
y.mesh loc=0.020    spac=0.05
y.mesh loc=0.025    spac=0.05
y.mesh loc=0.030    spac=0.05
y.mesh loc=0.033    spac=0.02
y.mesh loc=0.035    spac=0.02
y.mesh loc=0.205    spac=0.05
y.mesh loc=0.25    spac=0.05
y.mesh loc=0.27    spac=0.5
y.mesh loc=0.305    spac=0.5


region number=1 x.min=0.00   x.max=0.005    y.min=-0.037    y.max=-0.002 silicon

region number=2 x.min=0.00   x.max=0.005    y.min=-0.002    y.max=0.00   SiO2

region number=3 x.min=-0.003   x.max=0.00    y.min= 0.00   y.max= 0.035  silicon

region number=4 x.min=0.005   x.max=0.008    y.min=0.00    y.max=0.035   silicon

region number=5 x.min=0.00   x.max=0.005    y.min=0.00    y.max=0.005   silicon

region number=6 x.min=0.00   x.max=0.005    y.min=0.005    y.max= 0.035  SiO2

region number=7 x.min=-0.003   x.max=0.008    y.min=0.035    y.max=0.205  SiO2

region number=8 x.min=-0.003   x.max=0.008    y.min=0.205    y.max= 0.305   silicon

region number=9 x.min=-0.003   x.max=0.00    y.min=0.00    y.max=0.002   SiO2

region number=10 x.min=0.00   x.max=0.005    y.min=-0.037    y.max=-0.038  SiO2

region number=11 x.min=0.005   x.max=0.008    y.min=0.00    y.max= 0.002   SiO2


electrode name=gate number=1 x.min=0.00  x.max=0.005  y.min=-0.037  y.max=-0.02      neutral

electrode   name=source   number=3   x.min=-0.003     x.max=0.00     y.min=0.00     y.max=0.035
neutral

electrode name=drain number=4 x.min=0.005  x.max=0.008  y.min=0.00  y.max=0.035      neutral


doping uniform conc=10e20    n-type reg=1

doping uniform conc=10e20    p-type reg=3

doping uniform conc=10e20    p-type reg=4

doping uniform conc=10e15    p-type reg=5
```

```
doping uniform conc=10e15    n-type reg=8



save outf=so2_0.str
tonyplot so2_0.str - set so2_0.set

contact name=drain
contact name=source
contact name=gate workfunction=4.7
contact name=substrate


models       conmob srh auger bgn fldmob print

solve init

method       newton    trap

log         outf=so2_1.log master

solve        prev
solve        vgate=0.02
solve        vdrain=0.01
solve        vsource=0.01

solve       vgate=0.1 vstep=0.1 name=gate vfinal=1.5

tonyplot    so2_1.log -set so2_1.set
quit
```

4.SOFTWARE CODING FOR RECESSED SOURCE/DRAIN UTB SOI MOSFET WITH CHANNEL LENGTH=9nm

```
go atlas
mesh space.mult=1.0

x.mesh loc=-0.001   spac=0.05
x.mesh loc=0.00     spac=0.05
x.mesh loc=0.0001    spac=0.02
x.mesh loc=0.0004    spac=0.02
x.mesh loc=0.0006    spac=0.02
x.mesh loc= 0.0008   spac=0.02
x.mesh loc=0.001    spac=0.02
x.mesh loc=0.0015    spac=0.02
x.mesh loc=0.002    spac=0.02
x.mesh loc=0.003   spac=0.02
x.mesh loc=0.004   spac=0.02
x.mesh loc=0.0043    spac=0.02
x.mesh loc=0.0045    spac=0.02
x.mesh loc=0.0047    spac=0.02
x.mesh loc=0.0049    spac=0.02
x.mesh loc=0.005    spac=0.02
x.mesh loc=0.0052    spac=0.02
x.mesh loc=0.0054    spac=0.02
x.mesh loc=0.0056    spac=0.02
x.mesh loc=0.006    spac=0.02
x.mesh loc=0.0067    spac=0.02
x.mesh loc=0.0073    spac=0.02
x.mesh loc=0.008    spac=0.02
x.mesh loc=0.0085     spac=0.05
x.mesh loc=0.09

y.mesh loc=-0.037    spac=0.02
y.mesh loc=-0.032    spac=0.02
y.mesh loc= -0.027   spac=0.02
y.mesh loc=-0.022    spac=0.02
y.mesh loc=-0.017    spac=0.02
y.mesh loc=-0.013    spac=0.02
y.mesh loc=-0.010   spac=0.02
y.mesh loc=-0.007   spac=0.02
y.mesh loc=-0.005    spac=0.02
y.mesh loc=-0.004   spac=0.02
y.mesh loc=-0.002    spac=0.02
y.mesh loc=0.00    spac=0.05
y.mesh loc=0.001   spac=0.05
y.mesh loc=0.002    spac=0.02
y.mesh loc=0.003    spac=0.02
y.mesh loc=0.004    spac=0.02
y.mesh loc=0.005    spac=0.02
y.mesh loc=0.010    spac=0.05
y.mesh loc=0.015    spac=0.05
y.mesh loc=0.020    spac=0.05
y.mesh loc=0.025    spac=0.05
y.mesh loc=0.030    spac=0.05
y.mesh loc=0.033    spac=0.02
```

```
y.mesh loc=0.035    spac=0.02
y.mesh loc=0.205    spac=0.05
y.mesh loc=0.25    spac=0.05
y.mesh loc=0.27    spac=0.5
y.mesh loc=0.305    spac=0.5


region number=1 x.min=0.00   x.max=0.009    y.min=-0.037    y.max=-0.002 silicon

region number=2 x.min=0.00   x.max=0.009    y.min=-0.002    y.max=0.00   SiO2

region number=3 x.min=-0.001   x.max=0.00    y.min= 0.00   y.max= 0.035  silicon

region number=4 x.min=0.009   x.max=0.010    y.min=0.00    y.max=0.035   silicon

region number=5 x.min=0.00   x.max=0.009    y.min=0.00    y.max=0.005   silicon

region number=6 x.min=0.00   x.max=0.009    y.min=0.005    y.max= 0.035  SiO2

region number=7 x.min=-0.001   x.max=0.010    y.min=0.035    y.max=0.205  SiO2

region number=8 x.min=-0.001   x.max=0.010    y.min=0.205    y.max= 0.305   silicon

region number=9 x.min=-0.001   x.max=0.00    y.min=0.00    y.max=0.002   SiO2

region number=10 x.min=0.00   x.max=0.009    y.min=-0.037    y.max=-0.038  SiO2

region number=11 x.min=0.009   x.max=0.010    y.min=0.00    y.max= 0.002   SiO2



electrode name=gate number=1 x.min=0.00  x.max=0.009  y.min=-0.037  y.max=-0.02      neutral

electrode name=source number=3 x.min=-0.001    x.max=0.00    y.min=0.00    y.max=0.035
neutral

electrode name=drain number=4 x.min=0.009  x.max=0.010  y.min=0.00  y.max=0.035      neutral



doping uniform conc=10e20    n-type reg=1

doping uniform conc=10e20    p-type reg=3

doping uniform conc=10e20    p-type reg=4

doping uniform conc=10e15    p-type reg=5

doping uniform conc=10e15    n-type reg=8
```

```
save outf=so2_0.str
tonyplot so2_0.str - set so2_0.set

contact name=drain
contact name=source
contact name=gate workfunction=4.7
contact name=substrate


models       conmob srh auger bgn fldmob print

solve init

method       newton    trap

log         outf=so2_1.log master

solve        prev
solve        vgate=0.02
solve        vdrain=0.01
solve        vsource=0.01

solve       vgate=0.1 vstep=0.1 name=gate vfinal=1.5

tonyplot    so2_1.log -set so2_1.set
quit
```

CONCLUSION

In the above analysis we found that the electrical characteristics and performance of a general MOSFET is hugely affected by short channel effects like DIBL(Drain Induced Barrier Lowering) . The main design parameter of the ReS/D structure is the depth of the ReS/D region and S/D underlap dimension between the deep S/D and the thin silicon channel. It is desirable to place the deep source drain closer together around the gate edge to reduce the series resistance due to the thin body. The drawback for placing the deep S/D closer together is the increased susceptibility to SCE as the electric field from the deep source drain is more easily coupled to the center of the channel. On the other hand, there is no limitation imposed by the spacer on the side of the poly silicon gate as in the raised S/D structure, therefore a reduction of 25.6% miller capacitance is achieved with careful simulation.

Through experimental measurement, the ReS/D has several advantages over conventional UTB MOSFETs with elevated S/D structure, including lower series resistance and reduced Miller capacitor. A minor draw back in the ReS/D structure is the slightly worse DIBL effect, which can be minimized by careful design. Furthermore we observe that values of drain current comes out to be higher for recessed s/d SOI MOSFETs so we can conclude that the electrical characteristics of Re S/D is definitely better in comparison to that of conventional UTB SOI MOSFETs.

REFERENCES

- **[1] J.PColinge ,Tyndall National Institute,"The New Generation of SOI MOSFET",Romanian journal of information ,science and technology,11,number1,2008,3-15**
- **[2].B.Svilicic ,V.jovanovic,T.suligoj ,"Analytical models of front and back gate potential distribution and threshold voltage for recessed source/drain utb SOI MOSFETs",Solid state electronics,53(2009),540-547**
- **[3]W. Jeamsaksiri, M. Jurczak, L. Grau, D. Linten, E. Augendre, M. De Potter, R. Rooyackers, P.Wambacq, and G. Badenes, "Gate-source-drain architecture impact on DC and RF performance of sub-100-nm elevated source/drain NMOS transistors," *Electron Devices*, vol. 50, no. 3, pp.610–617, Mar. 2003**
- **[4] P. Ranade, H. Takeuchi, V. Subramanian, and T.-J. King, "A novel elevated source/drain PMOSFET formed by Ge-B/Si intermixing," *IEEE Electron Device Lett.*, vol. 23, pp. 218–220, Apr. 2002.**