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An Analytical Model for the Threshold Voltage of Short-Channel Double-Material-Gate (DMG) MOSFETs with a Strained-Silicon (s-Si) Channel on Silicon-Germanium (SiGe) Substrates

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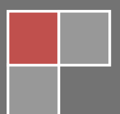

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A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF

MASTER OF TECHNOLOGY
IN
VLSI DESIGN AND EMBEDDED SYSTEMS

By:
SHIV BHUSHAN
Roll No. 211EC2100

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY
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Under the guidance of
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
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ROURKELA, ORISSA, INDIA

2013

Dedicated

To

My Father and My Late Mother

DEPARTMENT OF ELECTRONICS AND
COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA
ORISSA, INDIA-769008

CERTIFICATE

This is to certify that the Thesis Report entitled "**An Analytical Model for the Threshold Voltage of Short-Channel Double-Material-Gate (DMG) MOSFETs with a Strained-Silicon (s-Si) Channel on Silicon-Germanium (SiGe) Substrates**", submitted by **Mr. SHIV BHUSHAN bearing roll no. 211EC2100** in partial fulfilment of the requirements for the award of **Master of Technology in Electronics and Communication Engineering** with specialization in "**VLSI Design and Embedded Systems**" during session 2011-2013 at National Institute of Technology, Rourkela is an authentic work carried out by him under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other university/institute for the award of any Degree or Diploma.

Place: Rourkela

Date: 24TH May, 2013

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ABSTRACT

As the silicon CMOS technology move into the sub-20nm regime, manufacturing limits and fundamental curb the traditional scaling of transistors. Modernization in device structures and materials will be needed for continued transistor miniaturization and equivalent performance improvements. Device dimensions are approaching their scaling limit giving rise to undesirable effects like short channel effects, gate leakage current, drain induced barrier lowering (DIBL) etc. Strained-silicon devices have been receiving enormous attention owing to their potential for achieving higher channel mobility and drive current enhancement and compatibility with conventional silicon processing. Dual-Material Gate (DMG) structure offers an alternative way of simultaneous SCE suppression and improved device performance by careful control of the material workfunction and length of the laterally cascaded gate materials. The aim of project is to study the short-channel double-material-gate (DMG) strained-silicon ($s-Si$) on silicon-germanium ($Si_{1-X}Ge_X$) MOSFET and develop analytical models for the same.

In this novel work, an analytical threshold voltage model is developed for a short-channel double-material-gate (DMG) strained-silicon ($s-Si$) on silicon-germanium ($Si_{1-X}Ge_X$) MOSFET structure. The proposed threshold voltage model is based on the so called virtual-cathode potential formulation. The virtual-cathode potential is taken as minimum channel potential along the transverse direction of the channel and is derived from two-dimensional (2D) potential distribution of channel region. The 2D channel potential is formulated by solving the 2D Poisson's equation with suitable boundary conditions in both the strained-Si layer and relaxed $Si_{1-X}Ge_X$ layer. The effects of a number of device parameters like the Ge mole fraction, Si film thickness and gate-length ratio have been considered on threshold voltage. Further, the drain induced barrier lowering (DIBL) has also been analyzed for gate-length ratio and amount of strain variations and also, the sub threshold swing is also analyzed for the device with different parameter variation. The model is used to investigate the excellent immunity against SCE offered by the DMG structure. The validity of the present 2D analytical model is verified with ATLAS^{TM}, a 2D device simulator from Silvaco Inc.

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Shiv Bhushan

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CHAPTER 1

Introduction

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Chapter 1

1 INTRODUCTION

1.1 Scaling: A Historical Perspective

The twentieth century marked the beginning of an era in industrial electronics, automation, information sharing and technology. Communication technology multiplied in leaps and bounds. In no point in human history, the human race was ever been connected as it is today. Miniaturization of computer and hand held gadgets with every possible applications; be it audio, video, high speed communication; revolutionized the world of interconnectivity and entertainment. It's all attributed to the high speed ultra small sized, low power semiconductor devices, sensors, all new materials and their implementation through VLSI design.

It all begins with the perception of Lilienfeld of Insulated Gate Field Effect Transistor in 1925 which bore the potential to replace the vacuum tube technology with small sized semiconductor transistor technology [1]. The first practical demonstration took place in 1960 by Kahng and Atilla [2] in the form of the Silicon-based Metal Oxide Semiconductor Field Effect Transistor (MOSFET). In 1958, Jack Kilby at Texes Instruments conceived the idea of the Integrated Circuits (IC) and Robert Noyce from the Fairchild Corp. fabricated the first IC (a S-R flip flop) as shown in Fig. 1 [3]. It then came in 1959 when Richard Feynman delivered his notable speech, "There is plenty of room at the bottom", acknowledging the high performance achievement of the materials at the reduced dimensions [4]. Another visionary prophecy from Gordon Moore, then with Fairchild Corp. and co-founder of Intel, states that, "The number of transistors on integrated circuits doubles approximately every two years". This prophecy has been accurate for more than 3 decades as shown in Fig. 2. The year 1962 saw the growth of the first logic family, the TTL [3]. Intel introduced the first microprocessor in 1972 which used more than 2000 PMOS transistors. Following the

Moore's law the transistor count increased exponentially [5]. Then next few microprocessors used the NMOS technology which was routed out soon due to heavy dynamic power consumption with the increased number of transistor per chip. Then with the advent of the CMOS technology which consumed the least power, scaling technology sailed from the small scale integration (SSI) to Very Large Scale Integration (VLSI) and now spearheading towards the nanotechnology.

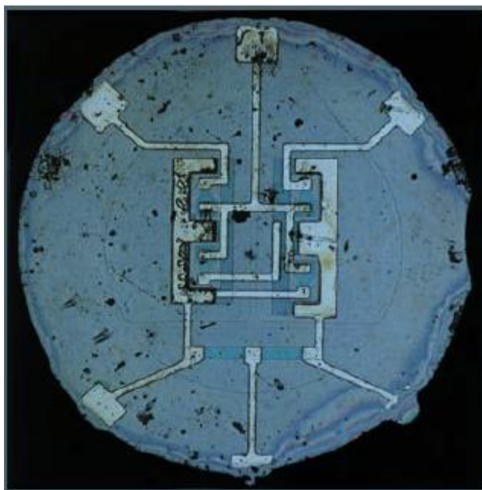

Fig. 1 First IC fabricated by Jay Last's developmentgroup at Fairchild Corp. **[4]**

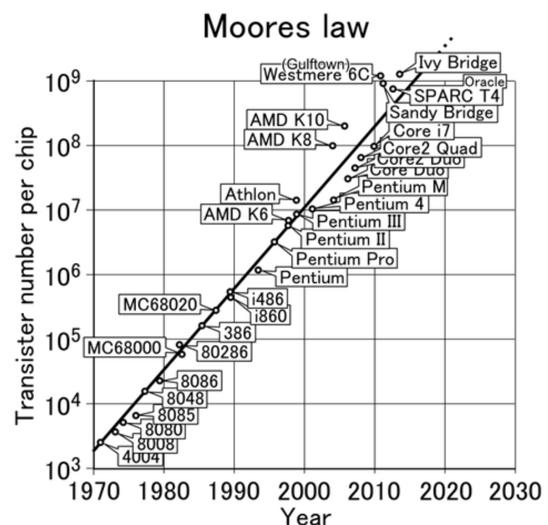

Fig. 2 Transistor Integration on Chip displaying Moore's Law. **[5]**

Another basic advantage that CMOS technology provides is the presence of definite scaling laws. The International Technology Roadmap for Semiconductor (ITRS) has laid a roadmap to direct this scaling in terms of power consumption and cost incurred. As evident from the ITRS 2010 in Fig. 3, the year 2013 with technology node 22nm is project to have physical channel length of 10nm and less. The latest Itanium-7 quad core GPU processor contains more 1.1 billion transistors in a 160 mm² chip area and Intel 32 nm SRAM wafer (1 Tb) has about 800 billion transistors [6]. Device engineers throughout the world have made this wonder come true through a magic named "Scaling". Scaling is defined as controlled modification of the device dimensions such that it acquires lesser chip area while maintaining the long channel characteristic and performance. Dennarad and fellow workers

proposed the scaling approach in 1972 [7]. Scaling not only reduces the device dimensions rendering to a higher packing density but it also leads to significant dynamic power saving through lesser voltages. The scaling approach stated that both the lateral and vertical dimensions of the transistor should be scaled by the same scaling factor in order to avoid the SCEs and ensure good electrostatic control when fabricating the smaller devices, and by the same scaling factor, the supply voltage should be reduced and substrate doping concentration should be increased.

Today's monolithic Integrated Circuits (ICs) use the MOSFET as a basic switching element for digital logic applications and as an amplifier for analog applications. This has resulted in chips that are significantly faster and have greater complexity in every generation while continually bringing down the cost per transistor.

1.2 Scaling Problems

Integration of billions of transistors on a chip has been possible due to the possibility to pattern every smaller feature on silicon through optical lithography. As optical lithography enters the sub-wavelength regime, light diffraction and interference from sub wavelength pattern feature causes image disorder. Therefore, patterning becomes difficult without adopting resolution enhancement techniques.

The ITRS's most recent projection provides some insight as to current market drivers. Fig. 4 illustrates that the power consumption trend versus power requirements is creating the "Power Gap" akin to the "Design Gap" that the industry dealt with a decade ago. This gap is creating a need to manage power at all levels of abstraction and majorly at the device level.

The power consumption is approximated by [8]

$$P_{diss} = P_D + P_S = \alpha f C_L V_{DD}^2 + V_{DD}\left(I_{leakage} + I_{th} 10^{-\frac{V_{th}}{s}} \right) \quad (1)$$

where P_D is the dynamic power dissipation, P_S is the static power dissipation, α is the activity factor, C_L is the load capacitance, V_{DD} is the supply voltage, $I_{leakage}$ is the total leakage current, I_{th} is the threshold current, V_{th} is the threshold voltage and s is the subthreshold swing. The power consumption is lowered through lower V_{DD}, $I_{leakage}$ and s; and higher V_{th}.

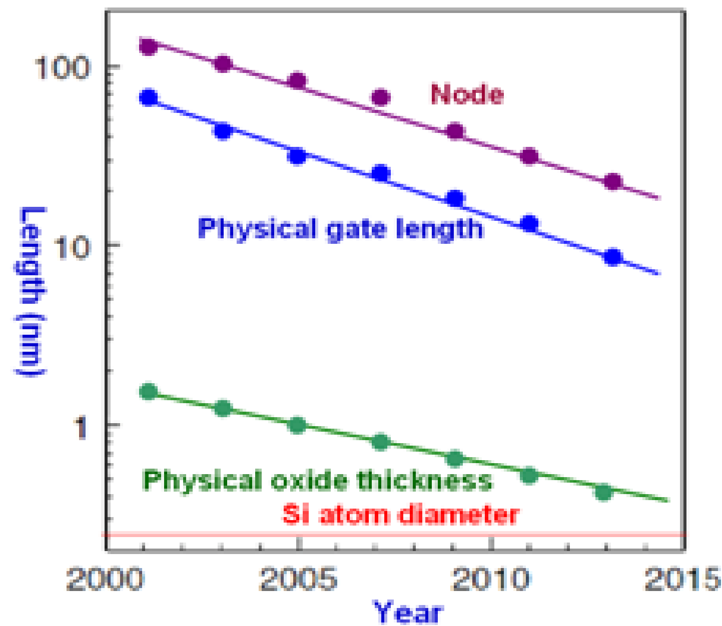

Fig. 3 Shrinking gate length with of scaling. years (Courtesy: ITRS 2010)

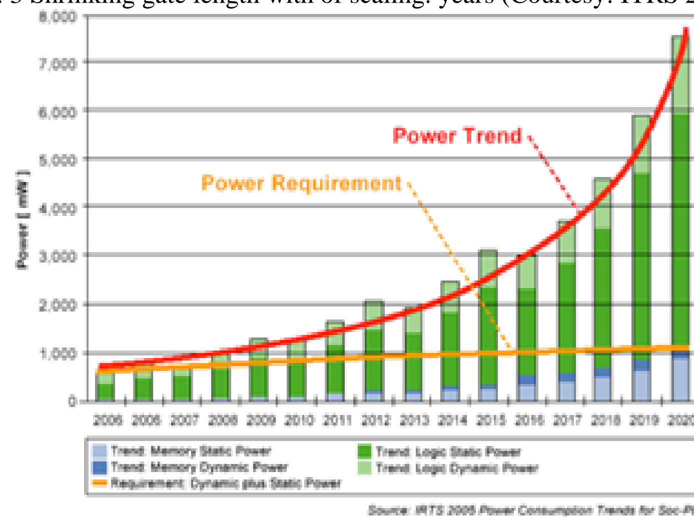

Fig. 4 Power Consumption trends with years of scaling. (Courtesy: ITRS 2005)

Thus V_{DD} and V_{th} are in conflict for which the gate oxide needs to be scaled tremendously which in turn increases gate tunnelling leakages. Also, higher substrate doping

is must to check the short channel effects (SCEs) but again this diminishes the current drive due to increased scattering. To trade-off between the power consumption, SCE and the lower current, is the need of the hour which the conventional MOSFETs fails to achieve. This gives way to creation of alternative device structures and architectures to continue further CMOS scaling.

Let's have a physical insight into the problems due to scaling. MOSFET scaling alters both lateral and vertical device dimensions.

1.2.1 Vertical Scaling

1.2.1.1 Polysilicon Depletion Effect

With vertical scaling, the effective oxide thickness increases, resulting in the degradation of the gate capacitance and transconductance. One of the factor responsible for this is scaling of the oxide whereas the other being thick polysilicon depletion layer when the device is operated at inversion. This depletion region cannot be further reduced due to doping limitations due to the solid solubility of silicon ($\sim 10^{19}$-10^{20} cm^{-3}). The effect also leads to a threshold voltage shift, which gets more pronounced at low polysilicon gate doping densities. Thus, the technology node predicts the use of metal gates to avoid this challenge.

1.2.1.2 Quantum effects

Scaling the oxide leads to strong surface electric field near the silicon/oxide interface creating a potential well and leading to quantum confinement of the inversion carriers, giving rise to discrete sub-bands for motion in the direction perpendicular to the interface and shifting the peak of the inversion charge centroid away from the interface. At inversion, the peak of the inversion carrier concentration peak is located around 1.2 nm away from interface in silicon. The confinement decreases the inversion charge density at a given bias, increases the effective oxide thickness and increases the threshold voltage.

1.2.1.3 Gate Tunnelling

With the diminishing gate oxide thickness, static power dissipation increases and the major contributor is the Gate Tunnelling. The tunnelling may take place through mechanisms like the direct tunnelling or the Fowler Nordheim tunnelling. Use of high-k dielectric materials (viz. HfO_2, $HfSiO_4$, and Si_3N_4) are employed to check gate tunnelling.

1.2.2 Lateral Scaling

1.2.2.1 Threshold voltage roll-off and DIBL

As the lateral dimensions are scaled, the S/D channel p-n junction depletion width becomes significant in comparison to the channel length leading to loss of gate control over the channel. The channel barrier reduces tremendously with increasing scaled channel which is manifested as threshold voltage roll off or a sharp fall of the threshold voltage with a scaled channel length.

The V_{th} roll-off is more dramatic when the drain bias is high. This is expected, since an increase in drain voltage leads to further penetration of the drain-induced field into the channel of the transistor, reducing the lateral potential barrier that is typically controlled by the gate. This effect is termed drain induced barrier lowering (DIBL). V_{th} lowering due to DIBL can be qualitatively explained by a semi-empirical 'charge sharing' model which considers the splitting of the depletion charge under the gate into two parts – one controlled by the gate, the other controlled by the source and drain. This introduces a correction of the maximum depletion charge controlled by the gate which determines the threshold voltage.

$$V_{th} = V_{FB} + 2\phi_f - \frac{Q'_d}{C_{ox}}$$

(2)

where, $Q'_d = Q_d - \Delta Q$ (3)

$Q'_d, Q_d, \Delta Q$ represents the depletion charge under gate control, the total depletion charge and depletion charge under drain control.

1.2.2.2 Hot Carrier Effect

Hot-carrier (HC) degradation affects reliability, increases SCE and causes long-term instability, manifested by a threshold voltage decrease and sub-threshold drive current increase. The high electric field near the drain creates hot carriers which are injected into the oxide with enough energy to create defect states (traps) in the oxide near the silicon/oxide interface. It is found that only hot electrons having energy of 0.6eV larger than the Si-SiO2 conduction band discontinuity can cause SiO_2 degradation in n-channel MOSFETs. The degradation is attributed to the breaking of the ≡SiH bond at the interface.

1.2.2.3 Mobility Degradation

Following the rules of scaling, for a planar bulk MOSFET, continuous scaling requires continuous increase in the channel doping (N_a). This is because it is desired to have a lower junction electric field in the channel region. Also higher doping ensures non-overlap of the source and drain depletion in the channel. But a serious effect of mobility degradation due to the impurity scattering comes in play with higher amount of channel doping. Also the threshold voltage variations take place due to random dopant fluctuations inside the channel.

1.3 Technology Boosters: Solution to Scaling

1.3.1 Gate Engineering Techniques

1.3.1.1 High-k dielectric

High-k/metal gates were introduced into mass production in 2007 by Intel in the 45 nm CMOS technology generation. This is the first time that traditional oxides or oxynitrides have been replaced in gate stacks, to enable continuous scaling of the EOT.

1.3.1.2 Metal Gate

Initially, poly-Si/high-k combination gate stack was considered as a route to improving gate leakage. However theoretical studies and experimental data show mobility degradation compared to the use of metal gates. Depending on the gate dielectric, the work function varies due to differing band alignments.

1.3.1.3 Multiple Gate

A potential candidate to continue the MOSFET scaling further is the fully-depleted silicon-on-insulator (FDSOI) MOSFET. Rigorous research of the FD SOI MOSFETs revels that this transistor possesses higher transconductance, lower threshold voltage roll-off and steeper subthreshold slope compare to the bulk MOSFET. In the FDSOI MOSFETs, the front gate parasitic junction (source/drain to channel) capacitances reduces resulting in higher switching speeds. The presence of the buried oxide (BOX) further removes drawbacks like leakage current, threshold voltage roll off, higher sub-threshold slope and body effect. However, due to the ultra thin source and drain regions, FD SOI MOSFETs possess large series resistance which leads to the poor current drive capability of the device despite having excellent short-channel characteristics. To prevent the encroachment of electric field lines from the drain on the channel region, special gate structures can be used as shown in Fig. 16. Such "multiple"-gate devices include double-gate transistors, triple-gate devices such as the quantum wire, the FinFET and Δ-channel SOI MOSFET, and quadruple-gate devices such as the gate-all-around device, the DELTA transistor, and vertical pillar MOSFETs. In a fully depleted SOI (FDSOI) device, most of the field lines propagate through the buried oxide (BOX) before reaching the channel region. Short-channel effects can be reduced in FDSOI MOSFETs by using a thin buried oxide and an underlying ground plane. This approach, however, has the inconvenience of increased junction capacitance and body effect. A much more efficient device configuration is obtained by using the double-gate transistor structure. Multi-gate

MOSFETs realized on thin films are the most promising devices for the ultimate integration of MOS structures due to the volume inversion or volume accumulation in the thin layer (for enhancement- and depletion-type devices, respectively), leading to an increase of the number and the mobility of electrons and holes as well as driving current (additional gain in performance in a loaded environment), optimum subthreshold swing and the best control of short channel effects and off-state current, which is the main challenge for future nanodevices due to the power consumption crisis and the need to develop green/sustainable ICs.

1.3.2 Channel Engineering Techniques

1.3.2.1 Shallow S/D Junction

Lowering the source/drain junction depths (especially near the gate edge, where the source/drain regions are called 'extensions') reduces the drain coupling to the source barrier. However, as the source/drain junction depths get shallow, their doping must be increased so as to keep the sheet resistance constant. Solid solubility of dopants puts an upper limit (~10^{20} cm^{-3}) on the doping density. Therefore, further reduction in 13 junction depth causes an increase in the series resistance encountered in accessing the channel. Also, from a technological point of view, it becomes difficult to form ultra shallow junctions that remain abrupt after the annealing steps needed to activate the dopants and achieve low resistivity [8]. The formation of abrupt S-D junctions also leads to an increase in the band-to-band tunneling leakage component. All these factors degrade the overall transistor performance.

1.3.2.2 Halo Doping

To overcome the SCEs, various channel engineering techniques like double-halo (DH) and single-halo (SH) or lateral asymmetric channel (LAC) devices have been proposed. In the subthreshold region, although the halo doping is found to improve the device performance parameters for analog applications (such as gm/Id, output resistance and intrinsic gain) in

general, the improvement is significant in the LAC devices. Halo doping led to a higher drive current in the saturation region. The halo device pinch–off region occurs in the halo implant region, since that region is closest to the drain and has a threshold voltage higher than the uniformly doped region.

1.3.2.3 Strain

To maintain a lower junction electric field in the channel and non-overlap of the source and drain depletion in the channel, doping becomes imperative. But a serious effect of mobility degradation due to the impurity scattering comes in play with higher amount of channel doping. Also the threshold voltage variations take place due to random dopant fluctuations inside the channel. The mobility of the charge carriers is enhanced through a concept known as the strain technology. To sum it all the benefits of strain, it results in a modified lattice constant of the material; second a modified energy band structure to trap carriers through well formation and finally an enhanced mobility. By increasing the Ge concentration of the relaxed $Si_{1-X}Ge_X$ substrate, the amount of biaxial strain and therefore higher magnitude of the mobility enhancement can be achieved. Literature had confirmed a mobility enhancement factor of 2.3 for a 30% Ge concentration [9].

1.3.2.3 Multi-Material Gate

One of the prominent means to get rid of hot carrier effect (HCE) is using cascaded gate structure consisting of two or more metals of different work functions. This structure is commonly known as Double-Material-Gate (DMG) structure as proposed in 1999 by Long *et al.*[10] or Triple-Material-Gate (TMG) as proposed by Razavi *et al*[11]. The metal gates are so cascaded that the gate near the source is a metal (M_1) with higher work-function and the drain side metal (M_2) is of relatively lower workfunction. As a result of this, the electron velocity and the lateral electric field along the channel increases sharply at the interface of the

two gate material which further results in the increased gate transport efficiency. Li Jin *et al.* described how reduction of the HCE may be achieved by decreasing the control gate to screen gate ratio in a DMG strained-Si on insulator MOSFET [11]. Further, the structure creates a step-like surface potential profile in the channel and thereby ensures screening of the minimum potential point from drain voltage variations. The metal gate M_1 is thus rightfully known as the *Control Gate* (L_1) and the metal M_2 as the *Screen Gate* (L_2).

1.4 Physics of Strain

When a layer of a crystal is grown over another layer, a strain is developed in the upper layer due to the mismatch of the lattice constants of the two layers. This is used to achieve the high speeds without scaling down the devices. In order to achieve the biaxial strain in the Si channel a $Si_{1-X}Ge_X$ virtual substrate is used. Here is germanium is chosen because of its compatibility with the Si technology and its slightly larger lattice constant [11]. The lattice constant of both material is given below:

Silicon = 5.431 Å

Germanium = 5.657 Å

Epitaxial growth of Si on relaxed SiGe substrate results in strained-Si layers due to the larger lattice constants of Ge. Fig. 5 shows the basic strain generation methodology. When a layer of $Si_{1-X}Ge_X$ is deposited by epitaxial growth on top of a bulk Si wafer. The atoms of SiGe substrate will initially line up with the Si wafer and be under compressive strain and as the depth of the $Si_{1-X}Ge_X$ layer increases it will begin to relax. The most commonly used way of relaxing this $Si_{1-X}Ge_X$ layer is to grade the Ge content. After the formation of critical thickness it become energetically favourable for the lattice to relax [11] and where the atoms do not line up due to the difference in atomic spacing misfit dislocations

are formed. While it is preferred to have a large number of defects in the graded layer of substrate to raise the relaxation [11], the problem is that on interaction with each other the misfit dislocations form threading dislocations which can move to the surface.

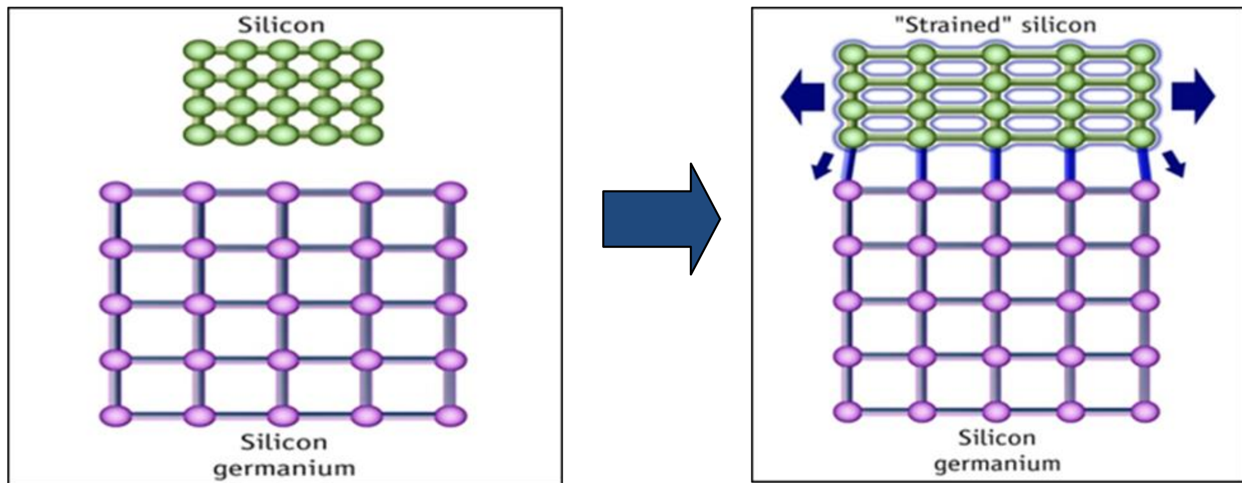

Fig. 5 The basic methodology to generate strain in the channel

This causes major problems for device performance. In order to try and reduce the number of threading dislocations point defects (PD) in the form of vacancies (absence of atoms) or interstitials (additional atoms) are often intentionally introduced. These condense on {111} planes forming dislocation loops. High numbers of point defects should promote dislocation climbing therefore annihilating threading dislocations creating a smooth surface morphology and low defect density [11].

Generally dislocations are not mobile at room temperatures and so only become debilitating when a wafer undergoes a high temperature process, Dislocations then travel across the wafer destroying the device.

Once a graded $Si_{1-X}Ge_X$ layer is deposited a uniform layer of $Si_{0.8}Ge_{0.2}$ would then be grown for ~1µm allowing a high Ge content to be achieved on the surface, with a high degree of misfit strain relaxation but without introducing a crippling number of threading dislocations.

H or He implantation has been tried as a way of restricting dislocations to areas below the upper surface [11] but the most commonly used method these days in a Chemical Mechanical Polishing (CMP) process performed between the graded and uniform SiGe layers.

1.4.1 Energy Band of Biaxial Strained Silicon

The fig. 6 shows the energy orbitals of the unstrained silicon. Each energy level of silicon is composed of six equal energy lobes in three dimensions [11].

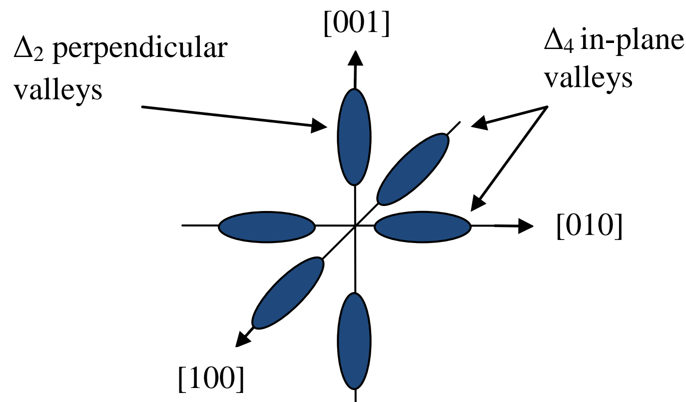

Fig. 6 Energy orbital's of unstrained silicon

These are named as two perpendicular Δ_2 states and four Δ_4 states parallel to the plane. Electrons are scattered between these bands through a process known as inter-band scattering. Similar splitting is observed between the heavy and light hole bands in the valence band. By altering the band structure at the channel the carrier mobility significantly increases. The alteration in the band structure in the channel layer of silicon provides a lower effective mass and also suppresses intervalley scattering, which is a prime cause of enhancement of the drive current and carrier mobility. The mobility becomes roughly twice that of a conventional Si substrate MOSFETs [12]. The strain induced in the silicon channel causes the splitting of conduction bands and it is totally depends on the type of strain induced. The below fig. 7 shows the energy orbital's of compressive and tensile strain in the silicon channel. For every 10% Ge in SiGe substrate layer, the Si energy bands split by 67meV [thesis_andi_mc].

When a stress is applied in silicon channel, the Δ_4 states Δ_2 and states are split up into higher and lower energy states. This band alteration in channel gives an alternate lower site for electrons to occupy, i.e. Δ_2. The change in the energy valleys causes repopulation of the electrons in the lower mass valleys. Electrons preferentially fill the lower energy bands, therefore tensile strain is more beneficial for nMOS devices as it leaves only the lower energy 2 fold degenerate levels, for inter-band scattering to occur between by presenting fewer possible final states for the carriers to scatter into. As a result electrons can travel further through the lattice before scattering. The effective mass of electrons in the lower energy states is less than the higher states. Due to this variation in energy states, the electron mobility increases. Besides of this, the inter-valley phonon scattering between the upper and lower states is suppressed due to the strain induced larger energy difference.

Mathematically the carrier mobility is described the given equation

$$\mu = \frac{q\tau}{m^*} \tag{4}$$

where, $\frac{1}{\tau}$ is the scattering rate and m^* is the conductivity effective mass.

The mobility of carrier is directly related to the velocity ‘v’ and the applied external electric field ‘E’, as given by

$$v = \mu E \tag{5}$$

By the above given relation, we can say that the carrier the velocity increasing with the increase in carrier mobility, which is directly proportional to the drain current and the switching speed of the device. Strain has less of an effect on holes than electrons with only a

38meV split for every 10% Ge in the substrate [12]. When strain is applied the similar splitting is observed between the heavy hole and light hole bands in the valence band.

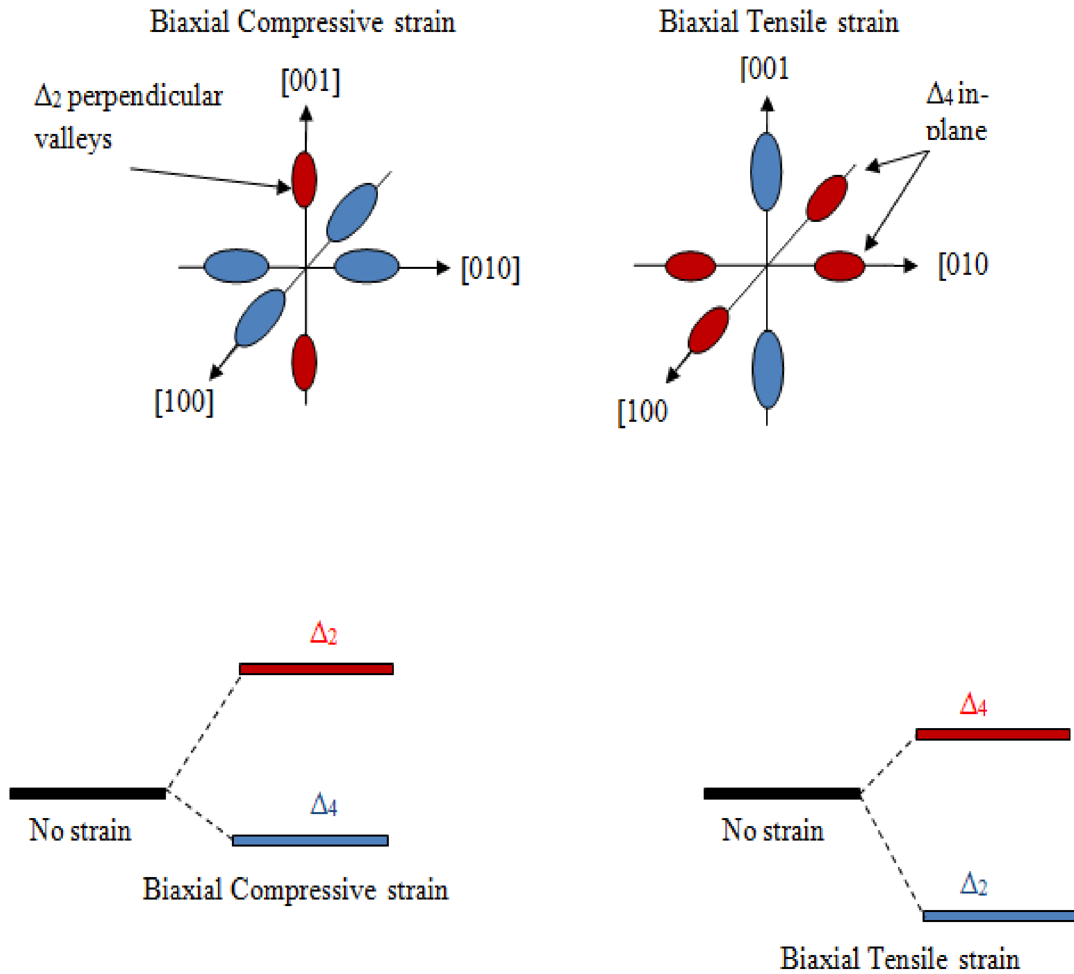

Fig. 7 Energy orbital's under compressive and tensile strain, and the effect on the energy levels that represent the orbitals.

The fig. 8 shows the holes splitting in the valence band. The valence band made up of three bands given as heavy-hole, light-hole and split-orbit bands.[12], as shown fig. 8. Application of strain results in high band warping. When the strain is applied, the valence band energy states get split up into heavy-hole and light-hole bands. The holes now occupy the low energy states, which reduces their effective mass. This increases mobility under strain.

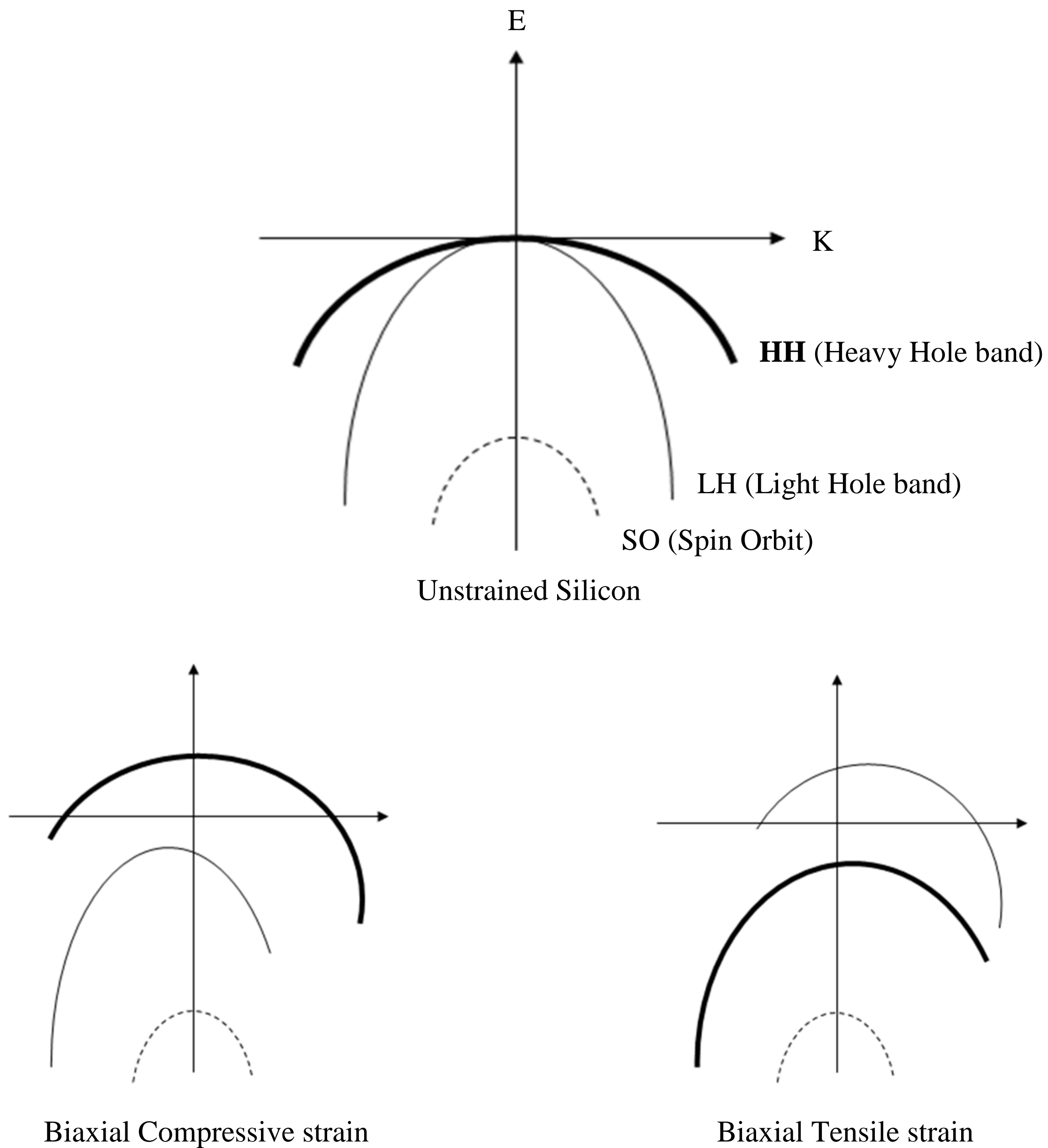

Fig. 8 Light Hole and Heavy Hole band splitting of the Silicon valence bands under strain [12].

1.4. 2 Effect of Strain on Band Structure

Basically there are two types of band alignments in the lattice, commonly known as type Ⅰ and type Ⅱ alignments [12]. When a thin film of larger lattice constant epitaxial layer, e.g. SiGe, is grown over a substrate with a smaller lattice constant (e.g. silicon), the film preserve the in-plane lattice constant of the substrate and so this under a biaxial compressive strain. This is known as the type Ⅰ band alignment where around all the band alteration occurs in the

valence band only and with very less band alteration in the conduction band. This type of structure is suitable for hole confinement and is a basic order for p-MOSFETs. When, a smaller lattice constant silicon epitaxial layer grown over a larger lattice constant relaxed-SiGe substrate it will be under biaxial tension. This is commonly known as type II band alignment and this type of structure has many advantages over the more common type I band alignment. In type II band alignment, a large band alteration is obtained in both the valence bands and conduction band, relative to the relaxed-SiGe substrate [12]. This type of structure allows both hole and electron confinements, making it suitable for both p-type and n-type devices for strained-Si/SiGe based CMOS technology. Strained silicon is used to increase n-type and p-type MOSFET drive currents by 10% and 25%, respectively [12].

1.4. 3 The Modified Band Structure of Silicon Due to Strain

Fig. 9 displays the change in silicon energy band structure because of strain in the silicon channel. The device simulator model library of ATLAS™, thus, has been modified according to the effects of strain on Si band structure. The effects of strain on Si band structure can be modeled as [13]

$$(\Delta E_C)_{s-Si} = 0.57X \tag{6}$$

$$(\Delta E_g)_{s-Si} = 0.40X \tag{7}$$

$$V_T \ln\left(\frac{N_{v,Si}}{N_{v,s-Si}}\right) = V_T \ln\left(\frac{m^*_{h,Si}}{m^*_{h,s-Si}}\right)^{\frac{3}{2}} \approx 0.075X \tag{8}$$

where, $(\Delta E_c)_{s-Si}$ is the increase in electron affinity of silicon due to strain; $(\Delta E_g)_{s-Si}$ is the decrease in the band gap of silicon due to strain; V_T is the thermal voltage ; $N_{v,Si}$ and $N_{v,s-Si}$ are the density of states in the valence band in unstrained and strained-silicon; $m^*_{h,Si}$ and

$m^*_{h,s-Si}$ are the hole density of states (DOS) effective masses in unstrained and strained silicon, respectively.

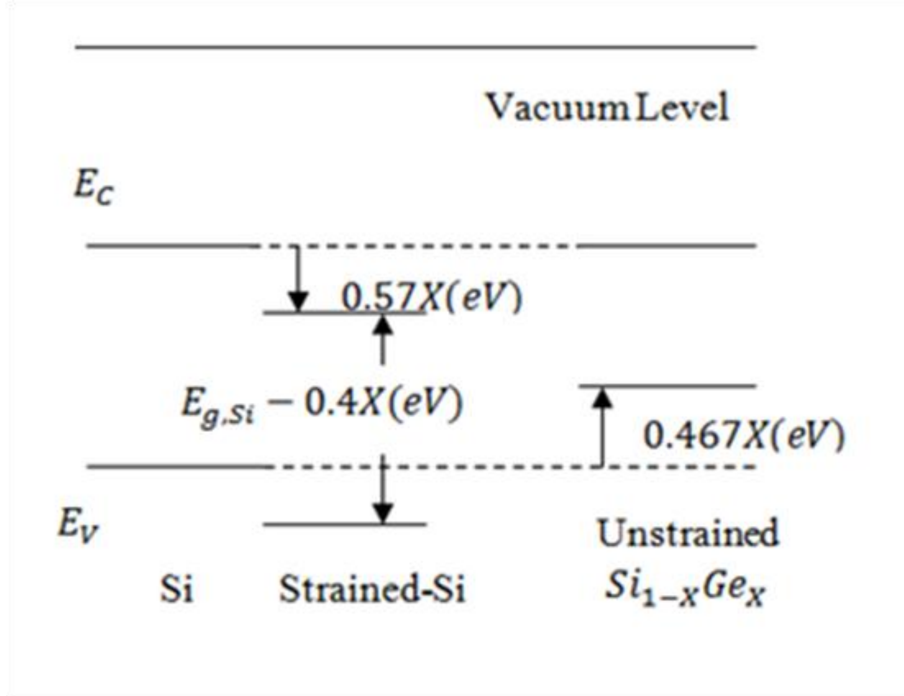

Fig. 9 Alternation of Band structure due to strain in $s-Si$ on $Si_{1-X}Ge_X$ substrate [14].

It should be noted that whole lump of Eq. (3) is a result of $(\phi_{f,Si} - E_{v,Si}) - (\phi_{f,s-Si} - E_{v,s-Si})$ [15], where $(\phi_{f,Si} - E_{v,Si})$ is the difference of Fermi energy level and valance band energy level of unstrained silicon and $(\phi_{f,s-Si} - E_{v,s-Si})$ is the difference of Fermi energy level and valance band energy level of strained Si; $\phi_{f,Si}$, $E_{v,Si}$, $\phi_{f,s-Si}$ and $E_{v,s-Si}$ are Fermi level of unstrained Si; valance band energy level of unstrained Si, Fermi level of strained Si and valance band energy level of strained Si respectively.

The energy band parameters for $Si_{1-X}Ge_X$ substrate have been estimated as follows [13]

$$(\Delta E_g)_{SiGe} = 0.467X \qquad (9)$$

$$N_{v,SiGe} = (0.6x + 1.04(1 - X)) \times 10^{19}\text{cm}^{-3} \quad (10)$$

$$\varepsilon_{SiGe} = 11.8 + 4.2\text{X} \quad (11)$$

where, $(\Delta E_g)_{SiGe}$ is the decrease in the band gap of $\text{Si}_{1-X}\text{Ge}_X$; $N_{v,SiGe}$ the density of states in the valence band of the relaxed $\text{Si}_{1-X}\text{Ge}_X$ film and ε_{SiGe} is the permittivity of the $\text{Si}_{1-X}\text{Ge}_X$.

1.4. 4 Change in MOSFET Parameter Due to Strain

The effect of strain on front-channel flat-band voltage can be modeled as

$$(V_{FB,f})_{s-Si} = (V_{FB,f})_{Si} + \Delta V_{FB,f} \quad (12)$$

where, $(V_{FB,f})_{Si} = \varphi_M - \phi_{(Si)}$ (13)

$$\Delta V_{FB,f} = -\frac{(\Delta E_C)_{s-Si}}{q} - \frac{(\Delta E_g)_{s-Si}}{q} - V_T \ln \frac{N_{V,Si}}{N_{V,s-Si}} \quad (14)$$

φ_M and q are the metal work function and electronic charge of the silicon, respectively; $(V_{FB,f})_{Si}$ represents the flat band voltage for a bulk MOSFET; $(V_{FB,f})_{s-Si}$ represents the flat band voltage for the strained bulk MOSFET and $\Delta V_{FB,f}$ represents the amount of change in the bulk flat band voltage due to strain.

$$\phi_{(Si)} = \frac{\chi_{Si}}{q} + \frac{E_{g,Si}}{2q} + \phi_{f,Si} \quad (15)$$

$$\phi_{f,Si} = V_T \ln\left(\frac{N_a}{n_{i,\text{Si}}}\right) \quad (16)$$

where, $\phi_{(Si)}$ is the unstrained Si work function; χ_{Si} is electron affinity of the silicon; $E_{g,Si}$ is

the band gap of unstrained Si; $\phi_{f,Si}$ is the Fermi potential in unstrained Si; N_a is the body doping concentration; and $n_{i,Si}$ is the intrinsic carrier concentration in unstrained Si.

The built-in voltage across the source-body and drain-body junctions in the strained-Si thin film is also affected by strain as

$$V_{bi,s-Si} = V_{bi,Si} + (\Delta V_{bi})_{s-Si} \tag{17}$$

Where,

$$V_{bi,Si} = \frac{E_{g,Si}}{2q} + \phi_{f,Si} \tag{18}$$

$$(\Delta V_{bi})_{s-Si} = \frac{-(\Delta E_g)_{s-Si}}{q} - V_T \ln \frac{N_{V,Si}}{N_{V,s-Si}} \tag{19}$$

Where, $V_{bi,Si}$ is the unstrained Si built in potential and $(\Delta V_{bi})_{s-Si}$ is the change in built in potential due to strain in the strained channel and source (drain) interface.

The built-in voltage across the source-body and drain-body junctions in the relaxed $Si_{1-X}Ge_X$ substrate can be written as,

$$V_{bi,SiGe} = V_{bi,Si} + (\Delta V_{bi})_{SiGe} \tag{20}$$

$$V_{bi,Si} = \frac{E_{g,Si}}{2q} + \phi_{f,Si} \tag{21}$$

$$(\Delta V_{bi})_{SiGe} = \frac{-(\Delta E_g)_{SiGe}}{q} - V_T \ln \frac{N_{V,Si}}{N_{V,s-Si}} \tag{22}$$

where, $(\Delta V_{bi})_{SiGe}$ is the change in built potential due to strain in $Si_{1-X}Ge_X$ substrate and source (drain) interface.

1.4. 5 Concept of Dual Material Gate MOSFET

In 1999, Long et. al. [10] proposed a new gate structure called the Double Material Gate (DMG)-MOSFET. Unlike the asymmetric structures employing doping engineering in which the channel field distribution is continuous, gate-material engineering with different workfunctions introduces a field discontinuity along the channel, resulting in simultaneous transport enhancement and suppressed SCEs.

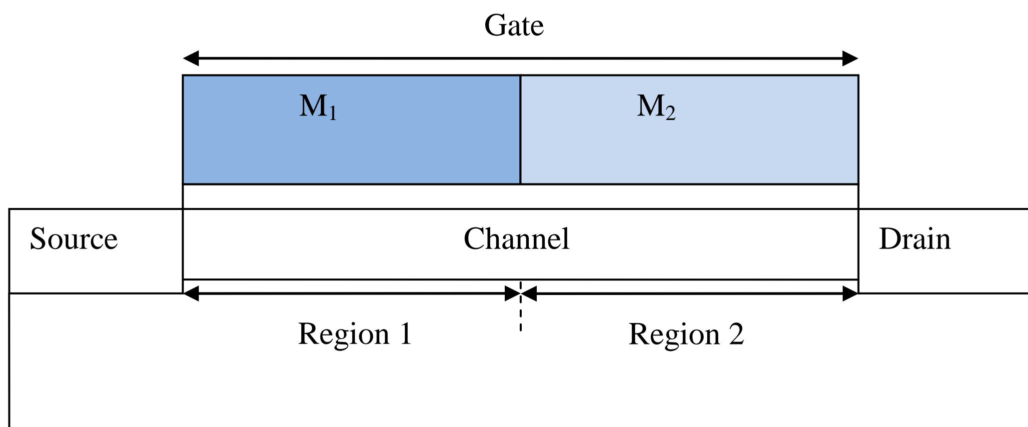

Fig. 10 Basic DMG MOSFETStructure

The fig. 10 show the basic structure of DMG Mosfet. The two gate metals are so cascaded that the gate near the source is a metal (M_1) with higher work-function and the drain side metal (M_2) is of relatively lower workfunction. As a result of this, the electron velocity and the lateral electric field along the channel increases sharply at the interface of the two gate material which further results in the increased gate transport efficiency [16]. Li Jin *et al.* described how reduction of the HCE may be achieved by decreasing the control gate to screen gate ratio in a DMG strained-Si on insulator MOSFET [17]. Further, the structure creates a step-like surface potential profile in the channel and thereby ensures screening of the minimum potential point from drain voltage variations. The metal gate M_1 is thus rightfully known as the *Control Gate* and the metal M_2 as the *Screen Gate*. Fabrication

techniques for DMG CMOS [20- 23] structure are reported in literature. DMG CMOS device with gate length of 55nm is already fabricated [21]. So, considering the development of the process technology over the years, the 30nm DMG MOSFET can also be fabricated in near future.

1.5 Thesis Objectives

The main objectives of this thesis is to develop a novel structure, which is useful in minimization of short channel (SCE) and drain induced barrier lowering (DIBL) effects, with the enhancement of carrier mobility. This work covers the complete analysis of strain and the double material gate concept. In this work, a subthreshold analysis of Double-Material-Gate (DMG) strained silicon on Silicon Germanium substrate is carried out. A two dimensional surface potential and threshold model are developed by using two dimensional Poisson's equation with suitable boundary conditions in both the strained-Si layer and relaxed $Si_{1-X}Ge_X$ layer. The sub threshold swing and current are also formulated. The variations in the surface potential, threshold voltage, subthreshold swing and current are carried out with different combination of the device parameters. Especially the effect of germanium concentration i.e. mole fraction of Ge is shown for different electrical parameter of device. The analysis has been carried out with the help of simulation results by a commercially available two dimensional (2D) ATLAS device simulators

1.6 Motivation

The Silicon-based Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has become one of the most important device in the semiconductor industry after the first practical demonstration in 1960. Today's monoliththic Integrated Circuits (ICs) use the MOSFET as a basic switching element for an amplifier for analog applications and digital logic circuit applications. While the basic structure of the MOSFET has remained unchanged.

But accordance with Moore's Law the physical size has been continually scaled by a factor of two every 2-3 years [18]. A conventional exponential scaling based on the reduction of feature size obviously cannot continue forever. The practical constraints as well as the fundamental curb the performance of the conventional bulk Si MOSFET. The need to enhance the drive currents while scaling of the transistor physical size and decreasing supply voltage, has been associated with an exponential increase in the static, off-state leakage of the device .While the active power density on the chip has steadily increased with gate length scaling, the static power density has grown at a much faster rate. The active power occurs due to the dissipative switching of charge between the transistor supply/ground and gates terminals during logic switching. The static or standby power, also known as sub-threshold power, is dissipated even in the absence of any switching operation. The mobility of the carrier in device is also degraded with the scaling of physical size of the device. Once the scaling of the conventional bulk Si MOSFET starts slowing down, the insertion of performance boosters, like novel materials and non- classical device structures, will become necessary to continue to improve performance.

The past several years have witnessed rapid growth in the study of strained silicon due to its potential ability to improve the performance of very large scale integrated (VLSI) circuits independent of geometric scaling. Strain improves MOSFET drive currents by fundamentally altering the band structure of the channel and can therefore enhance performance even at aggressively scaled channel lengths. This is the non classical way to improve the scaling limit of the device. With the generation of strain in the channel, the mobility and the velocity is increased by a factor of 2.3 for the 30% of germanium concentration in the SiGe substrate. The double material gate structure provide high immunity to short channel effects and drain induced barrier lowering effect.

1.7 Scope of Thesis

The scope of thesis is organized as follows:

- **Chapter 1: Introduction**

This chapter describes the theoretical background of strain mosfet and also it covers the complete description of the physics related to strain. This chapter also analyze the effect of strain on the band structure of silicon and also the effect of strain on the Mosfet parameters. This chapter provide a brief description of double material gate Mosfet.

- **Chapter 2: Literature Review**

This chapter describes the complete details of two dimensional (2D) ATLAS device simulator models used to simulate different types of the physical MOSFET structure.

- **Chapter 3: Simulation Methodology**

This chapter reports the simulation results of the misaligned effects of gate engineered double-gate (DG) MOSFETs along with some analysis.

- **Chapter 4: Surface Potential and Threshold Voltage Modeling**

This chapter, contains the modeling of surface potential and threshold voltage of the double material Strained-Si on SiGe MOSFET. The model has been compared with 2D simulations and the results with varying device parameters have been discussed.

- **Chapter 5: Conclusion**

This chapter contains the conclusion of the complete work.

CHAPTER 2

LITERATURE REVIEW

Early Work

Fabrication

Chapter 2

2 LITERATURE REVIEW

2.1 Early Work

The influence of strain on the mobility of intrinsic silicon was first observed in 1954 by C.S Smith [19]. The origin of strained Si film grown on relaxed SiGe can be traced to the 1980s [19]. While strain effects were not largely exploited, it was in the early 1990s that the strain was once again revived at Massachusetts Institute of Technology (MIT), USA on process-induced and biaxial strain. In 1992, the first n-channel MOSFET with a strained Si channel exhibiting a 70% higher mobility was demonstrated [19]. The commercial adoption of strain technology was followed in 90 nm technology node by all major semiconductor companies like AMD, Integrated Electronics (Intel) and International business machines (IBM). While IBM and AMD adopted strained-Si with their silicon on insulator (SOI) technology, Intel went ahead with strained Si on bulk Si MOSFET.

In year 2005, W. Zhang and J. G. Fossum [20] have shows the shift in threshold voltage in biaxially strained Si on $Si_{1-X}Ge_{X}$ CMOS devices. This is demonstrated by the shift in 2-D energy sub-bands and modified effective conduction and valance band densities of states. This increased electron affinity and band gap narrowing in the s-Si layer were found to be predominant components of these phenomena, which is generally less sensitive to the modified DOS effects. The general modeling, for both n-channel and p-channel s-Si devices, gives important physical insights on how the strain shifts the 2-D. subband energies, and how the varied threshold surface potential and the shifted flat-band voltage.

In year 2006, M. J. Kumar et al. [21] have reported a compact threshold voltage model for the single-layer FD-SSOI MOSFETs and demonstrated the effect of various device

parameters such as strain, channel length, strained-silicon thin-film doping, s-Si thin-film thickness and gate work function. This article shows that there is a significant drop in threshold voltage with decreasing channel length and increasing strain. The increase in strain, i.e., equivalent Ge content, enhances the performance of SSOI MOSFETs in terms of improved transconductance and speed because of an increase in the carrier mobility. However, as demonstrated by our results, there are undesirable side effects with increasing equivalent Ge content such as a roll off in V_{th}, which may affect the device characteristics and performance significantly.

In year 2007, M. J. Kumar et al[13] have first time examined the impact of various device parameters like strain (concentration of Ge in SiGe substrate), gate length, S/D junction depths, substrate (body) doping, strained silicon thin-film thickness and gate work function on the threshold voltage of strained-Si on $Si_{1-X}Ge_X$ MOSFET. There is a significant drop in threshold voltage with increasing strain in relaxed $Si_{1-X}Ge_X$ substrate and decreasing channel length. The increase in mole fraction of Ge, enhances the performance of MOSFETs in terms of transconductance and speed because of an increase in the carrier mobility. In the Same year V.Venkataraman [22], have also demonstrated fully depleted strained-Si on SGOI MOSFETs. This article also shows that there is significant increase in mobility due to strain.

In year 2010, A. Chaudry have submitted a review of strained silicon technology. The uniaxial and biaxial structures proposed by both industry and academia via literature and patents have been reviewed. The main structures under biaxial category are relaxed SiGe, graded SiGe, strained SOI, SGOI and other various hetero-structures help in providing improved performance. It also demonstrated that the biaxial strain solution provided by SSOI as the key material for solving the integration issues raised at channel length of 45nm and below. In the same year, Li Jin et al also submitted an article that shown, the high-*k* region on the oxide layer reduces DIBL and SCE. The scaling capability of the proposed structure is

compared to the conventional s-Si MOSFET, which demonstrate the improved Subthreshold behavior of the Gate Stack strained Si MOSFET over conventional strained Si MOSFET.

In year 2012, S. Bhushan et al [23] have demonstrated a surface potential model for interface trapped positive and negative charge. This article also demonstrated that the SCE is increase with increase in the magnitude of positive charge. One more finding was that increasing strain in the silicon channel suppresses short-channel effect (DIBL) and enhances the carrier mobility. Thus the concept of strain can be used to curb the SCE in sub 50nm technology and is an effective means of channel engineering.

In year 2004, A. Chaudhry demonstrated fully depleted DMG SOI MOSFET and shown its potential integration in the current CMOS technology [24]. The unique features of the DMG that are not easily available in the conventional SOI devices include: V_{th} roll-up, reduced DIBL, simultaneous transconductance enhancement and SCE suppression. They can be controlled by an alternative way of gate material engineering.

In year 2010, Li Jin et al [17] model for surface potential and threshold voltage, the paper has examined the effectiveness of DMG structure in fully depleted SSOI MOSFETs to suppress SCE. The demonstrated result show that the introduction of the novel device leads to the suppression of SCE due to a step-function in the channel potential profile. The shift in surface channel potential minimum position is negligible with increasing drain bias. This article also shows electric field in the channel at the drain end is reduced, which improves HCE. This also demonstrate that the DMG SSOI MOSFET gives rise to a desirable threshold voltage roll-off with decreasing channel length and improves the carrier transport efficiency.

2.2 Fabrication

In year 2001 Zhi-Yuan Cheng et al. [25] have demonstrated long-channel strained-Si MOSFETs fabricated in SGOI with a high Ge content of 25%. The SGOI substrates were

fabricated by a new wafer bonding and etch back method, utilizing 20% SiGe in the graded buffer layer as a natural etch stop. The measured electron mobility for s-Si n-MOSFETs fabricated on SGOI is significantly higher than both the universal mobility and that of co-processed bulk Si MOSFETs. In comprision with the SIMOX process, where the high annealing temperature limits the Ge content to a low level so this new SGOI process has a low thermal budget and thus is compatible with a wide range of Ge contents in $Si_{1-X}Ge_X$ layer.

In year 2003, K. Misty et al [26] Uniaxial strained silicon has been implemented in a high volume of manufacturing 90nm logic technology for the first time, with impressive performance results and improved power scaling of device. NMOS transistors employ a tensile capping layer to induce strain and improve NMOS drive current by 10%. PMOS transistors employ selective SiGe heteroepitaxy to generate uniaxial compressive strain in the channel.

T. Tezuka et al [27], demonstrate the steps to produce a strain silicon MOSFETs. In order to obtain a tensile strain in the channel a layer of strained Si channel layer is pseudomorphically grown over a relaxed SiGe on insulator (SGOI) substrate.

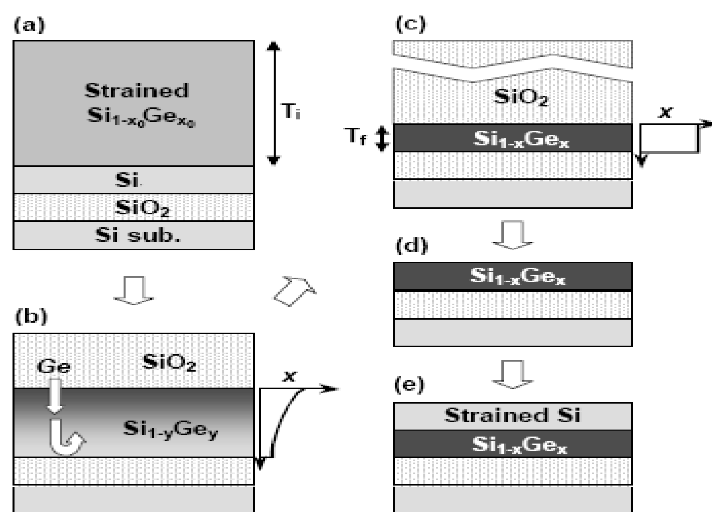

Fig. 11 Fabrication procedure of a SGOI substrate and a strained Si layer on it by the Ge condensation technique [27]

This is having a larger lattice constant than that of Si. SIMOX and wafer bonding techniques are use to fabricate SGOI substrates. The basic fabrication methodology is shown in above diagram.

In year 2006, P.F. Hsu et al [28] fabricated a dual material gate for a short channel device having channel length of 55nm. For the fabrication of short channel dual material gate MOSFETs they uses TaC and M_oN_x technology. Superior carrier mobility was achieved by optimizing the interface quality using hydroxyl rich base oxide (HRBO). The impact of dielectric crystallization on device characteristics is also reported for the first time. The excellent threshold voltage control, high mobility performance and its integration with strain-Si module demonstrate that this metal/high-*k* technology is promising for future CMOS applications.

CHAPTER 3

SIMULATION METHODOLOGY

Introduction

ATLAS Input and Output

The Order of ATLAS Commands

Define a Structure through the Command Language

Defining Material Parameter and Models

Numerical Method Selection

Solution Specification

Parameter Extraction

Chapter 3

3 SIMULATION METHODOLOGY

3.1 Introduction

ATLAS enables device technology engineers to simulate the thermal, optical and electrical behavior of semiconductor devices [29]. Atlas provides a physics-based, modular, easy to use and extensible platform to analyze AC, DC, and time domain responses for all semiconductor based technologies in 2 and 3 dimensions. ATLAS is designed to be used in conjunction with the virtual wafer fab (VWF) interactive tools. VWF include DECKBUILD, TONYPLOT, DEVEDIT, OPTIMIZER and MASKVIEWS. DECKBUILD contribute an interactive run time domain. TONYPLOT provides scientific visualization capabilities. DEVEDIT is an associated tool for structure, mesh specification and refinement. MASKVIEWS is an IC Layout Editor. The OPTIMIZER provides black box optimization across multiple simulators. ATLAS can be used as one of the simulators within the VWF automation tools. VWF makes it convenient to perform highly automated simulation-based experimentation. VWF is used in a way that reflects experimental research and development procedures using split lots. It therefore links simulation very closely to technology development and resulting in the significantly increased benefits from simulation use.

ATLAS is a physically based device simulator [29]. Physically based device simulators predict the electrical characteristics which are associated with specified physical structures and bias conditions. This is obtaining by approximating the operation of a device onto a two or three dimensional grid, the number of grid points called nodes. By using a set of differential equations which is obtained from Maxwell's laws apply onto this node to

simulate the transport of carriers within a structure. This means that the electrical performance of a device can now be modeled in AC, DC or transient modes of operation.

Physically based simulation has become very important for two reasons. First it is almost always much cheaper and quicker than performing experiments and second is it provides information that is impossible or difficult to measure. The drawbacks of physically based simulation are that all the relevant physics must be incorporated into a simulator and the numerical procedures must be implemented to solve the equations which are associated with this.

In ATLAS, specify device simulation problems by defining the following:

- The physical structure which to be simulated.
- The physical models to be used for simulation.
- The bias conditions which electrical characteristics are to be simulated.

3.2 ATLAS Input and Output

Fig. 12 shows the flow of input and output of the ATLAS. Most ATLAS simulations has two input files. The first input file is a text file which contains commands for ATLAS to execute [29].

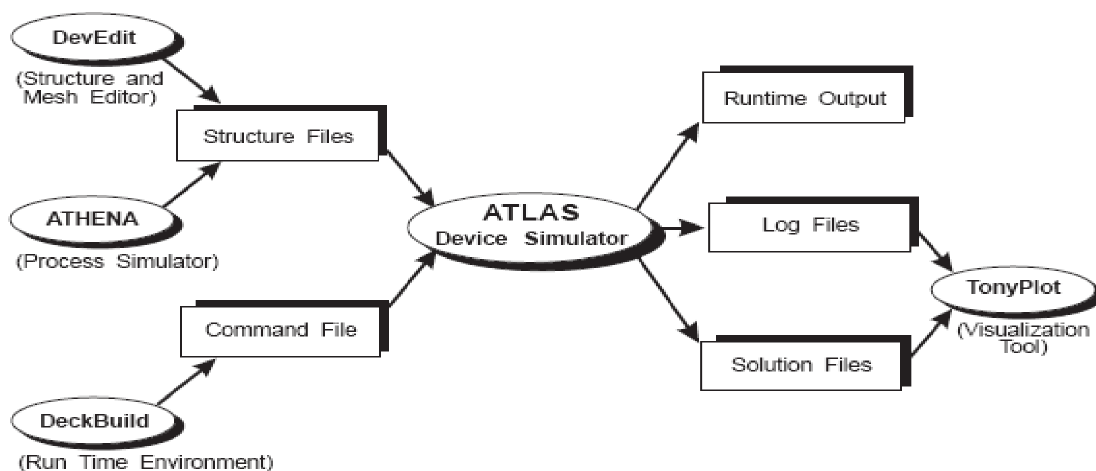

Fig. 12 Input and Output Flow of ATLAS [29]

The second input file is a structure file which specifies the structure that will be simulated.

ATLAS produces three types of output files.voltages and currents from the device analysis. Third type of output file is solution file which stores 2D and 3D data relating to the values of solution variables within the device at a given bias point.

3.3 The Order of ATLAS Commands

The order in which statements occur in an ATLAS input file is essential [29]. There are five groups of statements that must occur in the correct order. The required five essential groups are given below. Failure to do so usually causes an error message to appear which could lead to incorrect operation or termination of the program.

Group		Specification
1. Structure Specification	————	Mesh Region Electrode Doping
2. Material Model Specification	————	Material Models Contacts Interface
3. Numerical Method Selection	————	Method
4. Solution Specification	————	LOG SOLVE LOAD SAVE
5. Result Analysis	————	Extract Tony Plot

The correct order of statements in the mesh definition, structural definition, and solution specification is also essential. Improper order may cause incorrect operation and may cause the termination of the program and simulation will be stop.

3.4 Define a Structure through the Command Language

To define a device through the ATLAS command language, first of all define a mesh. This mesh or grid covers the physical simulation domain. Mesh is described by a series of vertical and horizontal lines and the spacing between them. Regions within this mesh are allocated to different materials as required to construct the device. After the regions are defined the electrodes location is specified. Final step is to specify the doping in each region.

3.4.1 The Initial Mesh Specification

The first statement to define the Mesh [29]. It must be written as follows

MESH SPACE.MULT=<VALUE>

The above statement is followed by X.MESH and Y.MESH.

X.MESH LOCATION=<VALUE> SPACING=<VALUE>

.

Y.MESH LOCATION=<VALUE> SPACING=<VALUE>

The SPACE.MULT parameter value is used as a scaling factor for the mesh obtained by the X.MESH and Y.MESH statements, default value is 1. Values less than 1 will create a globally finer mesh for increased accuracy. Values greater than 1 will create a globally coarser mesh for fast simulation. The X.MESH and Y.MESH statements are used to specify the locations in microns of horizontal and vertical lines, respectively. Together with the horizontal or vertical spacing associated with that line. At least two mesh lines must be described for each direction. The X.MESH and Y.MESH statements must be listed in the order of increasing x and y. Negative and positive values of x and y are allowed.

3.4.2 Specifying Regions and Materials

After the mesh is specification, every part of device must be assigned with a material type. This is process is completed with REGION statements [29].

REGION number=<integer> <material type> <position parameters>

Region numbers must start from region 1 and are increased for each subsequent region statement. The position parameters are described in microns using X.MIN, X.MAX, Y.MIN and Y.MAX parameters.

3.4.3 Specifying Electrodes

After the specification of region and material the next is to specify the electrode that contact to semiconductor material. ELECTRODE statement is used for this specification [29].

ELECTRODE NAME=<electrode name> <position parameters>

3.4.4 Specifying Doping

Doping of different regions is the next step of structure specification.

DOPING <distribution type> <dopant type> <position parameters>

Analytical doping profiles can have uniform or Gaussian pattern. Analytical distribution are specified with the DOPING statement.

DOPING UNIFORM CONCENTRATION=1E16 N.TYPE REGION=1

DOPING GAUSSIAN CONCENTRATION=1E18 CHARACTERISTIC=0.05 P.TYPE \
X.LEFT=0.0 X.RIGHT=1.0 PEAK=0.1

The first DOPING statement specifies a uniform n-type doping density of 10^{16} cm^{-3} in the region. The second DOPING statement specifies a p-type Gaussian profile with a peak concentration of $10^{18}cm^{-3}$, statement describe that the peak doping is located along a line from x = 0 to x = 1 microns [29].

3.5 Defining Material Parameter and Models

Once the mesh, geometry, and doping profiles are defined, now the next step is to modify the characteristics of electrodes, change the default material parameters, and choose which physical models ATLAS will use during the device simulation. These actions are

accomplished using the CONTACT, MATERIAL, and MODELS statements respectively [29].

3.5.1 Specifying Contact Characteristics

An electrode in contact with semiconductor material is assumed by default to be ohmic. If a work function is defined the electrode is treated as a Schottky contact. The CONTACT statement is used to specify the metal work function of one or more electrodes. The NAME parameter is used to identify which electrode will have its properties modified. The WORKFUNCTION parameter sets the work function of the electrode. The below given method is used to assign work function to an electrode [29].

CONTACT NAME=gate WORKFUNCTION=4.8

In ATLAS, t is possible to tie two or more contact together so that voltages on both contacts are equal. This is useful for many technologies for example dual material gate Mosfet. If the electrodes are defined with different names the following syntax can be used to link the voltages applied to the two electrodes.

CONTACT NAME=base1 COMMON=base

Here, the electrode, base1, will be linked to the electrode, base. The applied 0.1V on base will then appear on base1.

3.5.2 Specifying Material Properties

All materials are split into three classes: conductors, semiconductors and insulators. Each class of material requires a different set of parameters to be specified. For semiconductors, these properties include band gap, electron affinity, density of states and saturation velocities. There are default parameters for material properties used in device simulation for many materials [29]. The MATERIAL statement allows, specifying values for these basic parameters as per the different material is used. Mentioned values can apply to a specified

material or a specified region. The given syntax shows the method to specify the parameter value to the material.

MATERIAL MATERIAL=Silicon MUN=1100 EG300=1.12

The given statement sets the low field electron mobility and band gap in all silicon regions in the device. The material properties are defined by region then the region is mentioned using the REGION or NAME parameters in the MATERIAL statement.

3.5.3 Specifying Physical Model

Physical models are mentioned using the IMPACT and MODELS statements. Parameters for these models emerge on many statements along with: MODELS, IMPACT, MOBILITY, and MATERIAL. The physical models can be classified into five classes: mobility, recombination, impact ionization, carrier statistics, and tunnelling. All models are specified with the MODELS statement while the impact ionization is specified with IMPACT statement as the syntax shown below.

MODELS CONMOB SRH FLDMOB FERMIDIRAC

The above syntax specifies the standard concentration dependent mobility, Shockley-Read-Hall recombination with fixed carrier lifetimes, parallel field mobility, and Fermi Dirac statistics. ATLAS also provides an easy method for selecting the correct models for various technologies. The PRINT parameter lists to the run time output the parameters and models, which is used during the simulation of device. This allows verifying the material and models parameters. It is highly recommend that the PRINT parameter must include in the MODEL statement.

3.6 Numerical Method Selection

The semiconductor device problems can be solved by several different numerical methods. Numerical methods are specified in the METHOD statements of the input file.

There are basically three types of solution techniques [29]:

- Decoupled (GUMMEL),
- Fully coupled (NEWTON)
- BLOCK

The GUMMEL method will solve for each unknown while keeping the other variables constant the process is repeating until a stable solution is achieved. The GUMMEL method is generally useful where the equations of the system is weakly coupled, but has only linear convergence.

The NEWTON method solves the total system of unknowns together. The NEWTON method may spend extra time solving for quantities which are essentially weakly coupled or constant. NEWTON also requires a more accurate initial guess to the problem to obtain convergence.

The isothermal drift diffusion model requires the solution of three equations for potential, hole concentration and electron concentration. This method is highly recommended for all simulations with floating regions such as SOI transistors. ATLAS can solve both hole and electron continuity equations or it can be only one or may be none. This choice can be select by using the CARRIERS parameter.

3.7 Solution Specification

ATLAS can be used to obtain DC, AC small signal, and transient solutions. Generally, voltages are defined on each of the electrodes in the device. ATLAS then calculates the current through each electrode. ATLAS also calculates internal quantities such as electric fields and carrier concentrations for the device [29].

3.7.1 DC Solution

In DC solutions, the SOLVE statement is used to specify the voltage on all electrode.

For example:

solve vdrain=0.005

The statement solves a single bias point with 0.005V on the drain electrode.

3.7.2 Sweeping the Bias

In most of applications, a sweep of one or more electrodes is usually required. A ramped bias is used because the basic DC stepping is inconvenient. The below given syntax is used to show the variation in drain voltage from 0.0V to 2.0V with 0.05V steps with a fixed gate voltage of 0.01V.

solve vfgate=0.01

solve vdrain =0.0 vstep=0.05 vfinal=0.2 name=drain.

3.7.3 The Initial Solution

The initial guess for potential and carrier concentrations must be made from the doping profile when no previous solutions exist. This is why the initial solution must be performed at the zero bias (or thermal equilibrium) condition. This is specified by the given syntax:

SOLVE INIT

3.7.4 Log Files

Log files use to store the terminal characteristics which are calculated by ATLAS. These are voltages and current for each electrode in DC simulations. In AC simulations, the small the conductance, capacitances, and signal frequency are saved In transient simulations, the time is saved. The given syntax is used:

LOG OUTF=<FILE NAME.log>

Log files contain only the terminal characteristics. They are typically viewed in TONYPLOT. DECKBUILD is used for parameter extraction of log files data. Log files cannot be loaded

into ATLAS to re-initialize the simulation.

3.7.5 Solve statement

The DeckBuild Solve menu can be used generate SOLVE statements. The menu has a spreadsheet style entry. To access this menu, select the **Command/Solutions/Solve...** button in DECKBUILD.

3.7.6 Save Statement

To generate a structure file, use the OUTFILE parameter of either the SOLVE or SAVE statements. The given syntax is used to save the file.

SAVE OUTF=<File Name.str>

3.8 Parameter Extraction

The EXTRACT command is available within the DECKBUILD environment. It allows extract the device parameters. This command has a flexible syntax which allows making specific EXTRACT routines. EXTRACT operates on the previous solved structure file. By default the EXTRACT uses the currently open log file. To override this default action provides the name of a file to be used by EXTRACT command before the extraction routine. The syntax is given for extraction:

EXTRACT NAME="<filename>"

A typical example of using EXTRACT is the extraction of the threshold voltage of an MOS transistor.

Table 1 Device Parameter Used For Simulation

Parameters	**Value**
Mole Fraction	0-40%
Source /Drain doping (N_d)	$2X10^{20}$ cm^{-3}
Channel doping (N_a)	10^{18}cm^{-3}
Oxide thickness (t_{ox})	2 nm
Channel Length (L)	30 nm
Silicon film thickness (t_{si})	10 nm
Gate Metal work-function (M_1)	4.71 eV
Gate Metal work-function (M_2)	4.6 eV , 4.4 eV , 4.2 eV

Table 2 Modified parameter values of silicon due to strain (x)

Parameter	$X = 0$	$X = 0.1$	$X = 0.2$	$X = 0.3$
E_g300 (eV)	1.08	1.04	1.00	0.96
N_c300 (cm^{-3})	2.80 x10^{19}	2.25 x10^{19}	1.98 x10^{19}	1.95 x10^{19}
N_V300 (cm^{-3})	1.04x10^{19}	7.80 x10^{18}	5.85 x10^{18}	4.39 x10^{18}
Permittivity	11.8	11.8	11.8	11.8
Mobility (cm^2/V.sec)	1400	1800	2250	2305
Affinity (eV)	4.17	4.23	4.28	4.34
n_i (cm^{-3})	1.45 x10^{10}	2.44 x10^{10}	4.29 x10^{10}	7.99 x10^{10}

CHAPTER 4

SURFACE POTENTIAL AND THRESHOLD VOLTAGE FORMULATION

Introduction

Surface Potential Modeling

Threshold Voltage Modeling

Drain Induced Barrier Lowering (DIBL) Modeling

Results and Discussion

Chapter 4

4 SURFACE POTENTIAL AND THRESHOLD VOLTAGE FORMULATION

4.1 Introduction

In this work, the concept of Double-Material-Gate (DMG) is incorporated in strained-silicon ($s-Si$) on silicon-germanium ($Si_{1-X}Ge_X$) MOSFET in order to overcome HCE and other SCEs in strained-Si MOSFET. An analytical 2D surface potential model and thereby a threshold voltage model is also developed for the proposed device. For this purpose, the 2D Poisson's equation is solved in strained-Si and relaxed $Si_{1-X}Ge_X$ using the appropriate boundary conditions along with the parabolic approximation of the channel potential profile. An extensive analysis was carried out on the surface potential and threshold voltage by various device parameters like strain, oxide and silicon thickness, gate length ratio and gate metal variations. Also, the DIBL effect on the device is well analyzed. Fig. 13 shows the cross-section of a short channel DMG strained-Si on $Si_{1-X}Ge_X$ MOSFET along with the depletion region of the device.

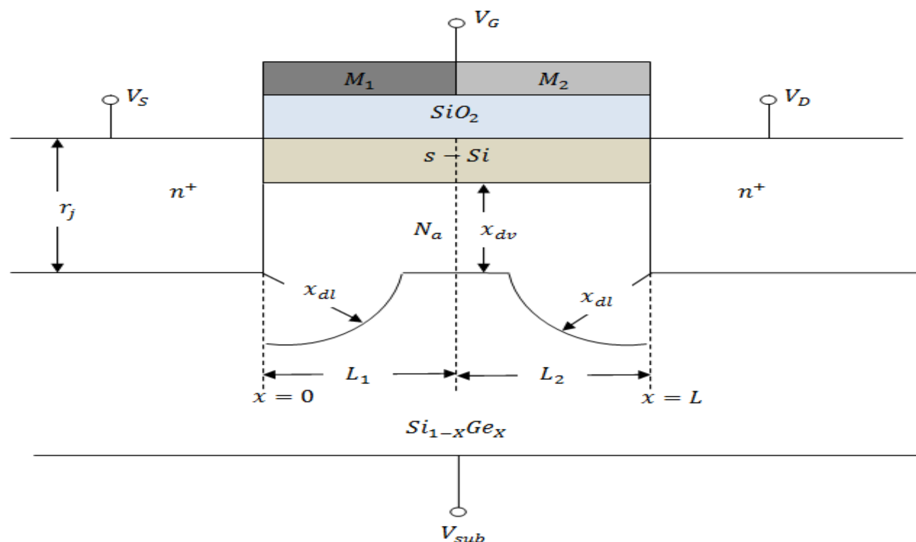

Fig. 13 Cross sectional view of DMG MOSFET with $s-Si$ channel on $Si_{1-X}Ge_X$ Substrates

Device dimensions, doping and other parameters are defined in Table1. As shown in Fig. 13, the depletion region under the gate is non-uniform caused by the lateral source-body and drain-body depletion widths x_{dl}. In such a case, the development of an analytical model through the exact solution of the 2D Poisson equation will be highly challenging and would require employment of numerical methods and iterations. To develop a simple analytical solution, device structure of Fig. 2(a) is altered into a box type approximation of the depletion region as shown in Fig. 2 (b) consisting of a uniform depletion thickness of x_d and a uniform doping density of $N_{a,eff}$.

Fig. 14 Box approximation of the depletion region of DMG MOSFET with $s-Si$ channel on $Si_{1-X}Ge_X$ substrate

M. J. Kumar et al. [13] have used some geometric approximations to find the effective channel doping and the depletion thickness of the channel in the MOSFET. Following the

same approach, the effective doping concentration due to the box approximation can be written as

$$N_{a,eff} = N_a \left[1 - \left(\left(1 + \frac{2x_{dv}}{r_j} \right)^{\frac{1}{2}} - 1 \right) \frac{r_j}{L} \right] \tag{23}$$

where,

$$x_{dv} = \sqrt{\frac{2\varepsilon_{SiGe}(\phi_{th} - V_{sub})}{qN_a}} \tag{24}$$

$$\phi_{th} = 2\phi_{f,Si} + \Delta\phi_{(s-Si)} \tag{25}$$

$$\Delta\phi_{(s-Si)} = \frac{-(\Delta E_g)_{s-Si}}{q} - V_T \ln \frac{N_{V,Si}}{N_{V,s-Si}} \tag{26}$$

where, x_{dv} is vertical depletion widths; ϕ_{th} is that value of surface potential at which the inversion charge density in the strained-Si device is same as that in the unstrained-Si at threshold; $\Delta\phi_{(s-Si)}$ is change in unstrained Si workfunction due to strain and V_{sub} is substrate bias voltage.

The depletion region thickness is given as

$$x_d \cong \frac{2x_{dl}\left(r_j + \frac{\pi}{4} x_{dl} \right) + (L - 2x_{dl}) x_{dv}}{L} \qquad \text{for} \quad L \geq 2x_{dl} \tag{27}$$

and

$$x_d \cong r_j + \left(x_{dl}^2 - \frac{L^2}{4} \right)^{\frac{1}{2}} + \frac{\theta}{2} x_{dl} \qquad \text{for} \quad L \leq 2x_{dl} \tag{28}$$

where,

$$\theta = \sin^{-1}\left(\frac{L}{2x_{dl}}\right) \tag{29}$$

$$x_{dl} = \sqrt{\frac{2\varepsilon_{SiGe} V_{bi,SiGe}}{qN_a}} \tag{30}$$

where, x_{dl} is the lateral depletion widths; r_j is the source and drain depth and L is total channel length.

Considering all the above approximations, the modified device structure is shown in Fig. 2 (b). As shown, the depletion region is divided into four regions represented by regions 1 and 3 under metal M_1 and regions 2 and 4 under metal M_2. Regions 1 and 2 represent the s-Si layer whereas regions 3 and 4 represent the relaxed $Si_{1-X}Ge_X$ layer.

4.1 Surface Potential Modeling

To find out the potential distribution $\phi_i(x, y)$ in the channel region, the following 2D Poisson's equations have been solved in all the four regions of strained-Si and the relaxed $Si_{1-X}Ge_X$ layers.

$$\frac{\partial^2 \phi_i(x, y)}{\partial x^2} + \frac{\partial^2 \phi_i(x, y)}{\partial y^2} = \frac{qN_{a,eff}}{\varepsilon_{Si}} \quad \text{with } i = 1,2 \tag{31}$$

$$\frac{\partial^2 \phi_i(x, y)}{\partial x^2} + \frac{\partial^2 \phi_i(x, y)}{\partial y^2} = \frac{qN_{a,eff}}{\varepsilon_{SiGe}} \quad \text{with } i = 3,4. \tag{32}$$

For the s−Si layer the y co-ordinate points downwards whereas for $Si_{1-X}Ge_X$ layer, y-coordinate is considered at y' pointing upwards as shown in fig. 14. The subscript i in the Eq. (31) and Eq. (32) denotes the respective channel regions as i takes the numerical values

1, 2 3 and 4; $N_{a,eff}$ is the effective body doping concentration; q is the electronic charge; ε_{Si} and ε_{SiGe} are the permittivity of strained-Si film and relaxed $Si_{1-X}Ge_X$. The potential distributions in all the four regions are approximated by parabolic polynomials as [30]

$$\phi_i(x,y) = \phi_{si}(x) + C_{i1}(x)y + C_{i2}(x)y^2 \quad i = 1,2 \tag{33}$$

$$\phi_i(x,y') = V_{sub} + C_{i1}(x)y' + C_{i2}(x)y'^2 \quad i = 3,4 \tag{34}$$

Here, $\phi_{si}(x)$ is the surface potential at $SiO_2/s-Si$ interface under both metals M_1 and M_2. The coefficients C_i are the functions of x only. V_{sub} is the substrate bias usually taken to be zero [13]. The continuity of potential and electric field across the interface of regions 1 and 2 are:

$$\phi_1(L_1,0) = \phi_2(L_1,0) \tag{35}$$

$$\phi_3(L_1,0) = \phi_4(L_1,0) \tag{36}$$

$$\left[\frac{\partial\phi_1(x,y)}{\partial x}\right]_{x=L_1} = \left[\frac{\partial\phi_2(x,y)}{\partial x}\right]_{x=L_1} \tag{37}$$

$$\left[\frac{\partial\phi_3(x,y')}{\partial x}\right]_{x=L_1} = \left[\frac{\partial\phi_4(x,y')}{\partial x}\right]_{x=L_1} \tag{38}$$

The electric flux at SiO_2/s-Si interface should be continuous in both regions 1 and 2:

$$\left[\frac{\partial\phi_1(x,y)}{\partial y}\right]_{y=0} = \frac{\varepsilon_f}{\varepsilon_{Si}}\frac{\phi_{s1}(x) - V_{g1}}{t_f} \tag{39}$$

$$\left[\frac{\partial\phi_2(x,y)}{\partial y}\right]_{y=0} = \frac{\varepsilon_f}{\varepsilon_{Si}}\frac{\phi_{s1}(x) - V_{g2}}{t_f} \tag{40}$$

where ε_f the permittivity of the SiO_2, t_f is the thickness of front gate oxide.

$$V_{g1} = V_{gs} - (V_{FB1,f})_{s-Si} \text{ where } (V_{FB1,f})_{s-Si} = \varphi_{M1} - \phi_{(Si)} \tag{41}$$

$$V_{g2} = V_{gs} - (V_{FB2,f})_{s-Si} \text{ where } (V_{FB2,f})_{s-Si} = \varphi_{M2} - \phi_{(Si)} \tag{42}$$

where, V_{gs} as the gate to source voltage; V_{g1} and V_{g2} are the effective gate voltage of control gate and the screen gate at the $\mathrm{s-Si/SiO_2}$ interface; $(V_{FB1,f})_{s-Si}$ is the flat-band voltage for control gate and $(V_{FB2,f})_{s-Si}$ is the flat-band voltage for screen gate. φ_{M1} and φ_{M2} represents the metal work functions of the control gate and the screen gate.

Electric field at the bottom edge of depletion region (in regions 3 and 4) is zero and can be written as

$$\left[\frac{\partial \phi_3(x, y')}{\partial y'}\right]_{y'=0} = 0 \tag{43}$$

$$\left[\frac{\partial \phi_4(x, y')}{\partial y'}\right]_{y'=0} = 0 \tag{44}$$

The potential and electric field at the $\mathrm{s-Si/Si_{1-X}Ge_X}$ interface should be equal and continuous, respectively, as

$$\phi_1(x, t_{Si}) = \phi_3(x, t_{SiGe}) \tag{45}$$

$$\left[\frac{\partial \phi_1(x, y)}{\partial y}\right]_{y=t_{Si}} = -\frac{\varepsilon_{SiGe}}{\varepsilon_{Si}}\left[\frac{\partial \phi_3(x, y')}{\partial y'}\right]_{y'=t_{SiGe}} \tag{46}$$

$$\phi_2(x, t_{Si}) = \phi_4(x, t_{SiGe}) \tag{47}$$

$$\left[\frac{\partial \phi_2(x, y)}{\partial y}\right]_{y=t_{Si}} = -\frac{\varepsilon_{SiGe}}{\varepsilon_{Si}}\left[\frac{\partial \phi_4(x, y')}{\partial y'}\right]_{y'=t_{SiGe}} \tag{48}$$

The potentials at the source and drain end can be given by

$$\phi_1(0,0) = V_{bi,s-Si} \tag{49}$$

$$\phi_2(0,L) = V_{bi,s-Si} + V_{ds} \tag{50}$$

$$\phi_3(0,0) = V_{bi,SiGe} \tag{51}$$

$$\phi_4(0,L) = V_{bi,SiGe} + V_{ds} \tag{52}$$

where, V_{ds} is drain-to-source voltage.

The coefficients $C_{i1}(x)$ and $C_{i2}(x)$ appeared in Eq. (33) and Eq. (34) has been obtained by using the boundary conditions from Eq. (35) to Eq. (52):

$$C_{11}(x) = \frac{C_f}{\varepsilon_{Si}}(\phi_{s1}(x) - V_{g1}) \tag{53}$$

$$C_{12}(x) = -\frac{1}{2(C_{SiGe} + C_{Si})t_{Si}^2}\left[\phi_{s1}(x)\frac{\left(C_f C_{Si} + 2C_{Si}C_{SiGe} + 2C_f C_{SiGe}\right)}{C_{Si}} - 2\phi_{s3}(x)C_{SiGe} - \frac{(2C_f C_{SiGe} + C_f C_{Si})}{C_{Si}}V_{g1}\right] \tag{54}$$

$$C_{21}(x) = \frac{C_f}{\varepsilon_{Si}}(\phi_{s2}(x) - V_{g2}) \tag{55}$$

$$C_{22}(x) = -\frac{1}{2(C_{SiGe} + C_{Si})t_{Si}^2}\left[\phi_{s2}(x)\frac{\left(C_f C_{Si} + 2C_{Si}C_{SiGe} + 2C_f C_{SiGe}\right)}{C_{Si}} - 2\phi_{s4}(x)C_{SiGe} - \frac{(2C_f C_{SiGe} + C_f C_{Si})}{C_{Si}}V_{g2}\right] \tag{56}$$

$$C_{31}(x) = 0 \tag{57}$$

$$C_{32}(x) = -\frac{C_{Si}}{2(C_{SiGe} + C_{Si})t_{SiGe}^2}\left[2\phi_{s3}(x) - \frac{(2C_{Si} + C_f)}{C_{Si}}\phi_{s1}(x) + \frac{C_f}{C_{Si}}V_{g1}\right] \tag{58}$$

$$C_{41}(x) = 0 \tag{59}$$

$$C_{42}(x) = -\frac{C_{Si}}{2(C_{SiGe} + C_{Si})t_{SiGe}^2}\left[2\phi_{s4}(x) - \frac{(2C_{Si} + C_f)}{C_{Si}}\phi_{s2}(x) + \frac{C_f}{C_{Si}}V_{g2}\right] \tag{60}$$

where, $C_f = \frac{\varepsilon_{ox}}{t_f}, C_{Si} = \frac{\varepsilon_{Si}}{t_{Si}}, C_{SiGe} = \frac{\varepsilon_{SiGe}}{t_{SiGe}}$ are front gate oxide, strained-Si, relaxed $Si_{1-X}Ge_X$ layer capacitances respectively.

Utilizing Eq. (33), Eq. (34) and boundary conditions of Eq. (35) - Eq. (52) into Eq. (31) and Eq. (32), one dimensional differential equation for surface potential, $\phi_{si}(x)$, can be written as

$$\frac{\partial^2 \phi_{si}(x)}{\partial x^2} - P\phi_{si}(x) = Q_i \tag{61}$$

where, $P = \frac{\alpha_1\alpha_2 - \beta_1\beta_2}{\alpha_1 + \alpha_2}$ (62)

$$Q_1 = \frac{\alpha_2\gamma_1 + \beta_1\gamma_3}{\alpha_1 + \alpha_2} \tag{63}$$

$$Q_2 = \frac{\alpha_2\gamma_2 + \beta_1\gamma_4}{\alpha_1 + \alpha_2} \tag{64}$$

$$\alpha_1 = \alpha_2 = \frac{2C_{SiGe}C_{Si} + 2C_f C_{SiGe} + C_f C_{Si}}{C_{Si}(C_{SiGe} + C_{Si})t_{Si}^2} \tag{65}$$

$$\beta_1 = \beta_2 = \frac{2C_{SiGe}}{(C_{SiGe} + C_{si})t_{si}^2} \tag{66}$$

$$\gamma_1 = \frac{qN_a}{\varepsilon_{Si}} - \frac{C_f(2C_{Sige} + C_{Si})V_{g1}}{C_{Si}(C_{Sige} + C_{Si})t_{Si}^2} \tag{67}$$

$$\gamma_2 = \frac{qN_a}{\varepsilon_{Si}} - \frac{C_f(2C_{SiGe} + C_{Si})V_{g2}}{C_{Si}(C_{SiGe} + C_{Si})t_{Si}^2} \tag{68}$$

$$\alpha_3 = \alpha_4 = \frac{2C_{Si}}{(C_{SiGe} + C_{Si})t_{SiGe}^2} \tag{69}$$

$$\beta_3 = \beta_4 = \frac{2C_{Si} + C_f}{(C_{SiGe} + C_{Si})t_{SiGe}^2} \tag{70}$$

$$\gamma_3 = \frac{qN_a}{\varepsilon_{SiGe}} + \frac{C_f C_{SiGe} V_{g1}}{C_{SiGe}(C_{SiGe} + C_{Si})t_{SiGe}^2} \tag{71}$$

$$\gamma_4 = \frac{qN_a}{\varepsilon_{SiGe}} + \frac{C_f C_{SiGe} V_{g2}}{C_{SiGe}(C_{SiGe} + C_{Si})t_{SiGe}^2} \tag{72}$$

Solution of Eq. (61) yields following expression for surface potential, $\phi_{si}(x)$ [31]

$$\phi_{s1} = \frac{\psi_{d1}\sinh(\lambda x) - \psi_{s1}\sinh(\lambda(x - L_1))}{\sinh(\lambda L_1)} - \sigma_1 \tag{73}$$

$$\phi_{s2} = \frac{\psi_{d2}\sinh(\lambda(x - L_1)) - \psi_{s2}\sinh(\lambda(x - L))}{\sinh(\lambda L_2)} - \sigma_2 \tag{74}$$

$$\lambda = \sqrt{P} \tag{75}$$

$$\sigma_i = \frac{Q_i}{P} \tag{70}$$

$$\psi_{s1} = V_{bi,\text{s-Si}} + \sigma_1 \tag{76}$$

$$\psi_{d2} = V_{bi,\text{s-Si}} + V_{ds} + \sigma_2 \tag{77}$$

$$\psi_{d1} = V_p + \sigma_1 \tag{78}$$

$$\psi_{s2} = V_p + \sigma_2 \tag{79}$$

$$V_p = \frac{\psi_{d2}\cos ech(\lambda L_1) + \psi_{s1}\cos ech(\lambda L_1) - \sigma_1\coth(\lambda L_1) - \sigma_2\coth(\lambda L_2)}{\coth(\lambda L_1) + \coth(\lambda L_2)} \tag{80}$$

where, $\psi_{s1}, \psi_{s2}, \psi_{d1}, \psi_{d2}, \sigma_1$ and σ_2 are the constants and λ is the characteristic length associated with the surface potential.

The position $x_{\min}$ of the so called virtual cathode (the minimum surface potential) lies under the control gate [24] is estimated by solving $\left(\frac{\partial \phi_{s1}(x)}{\partial x}\right)_{x=x_{\min}} = 0$ and is determined as

$$x_{\min} = \frac{1}{2\alpha}\ln\left(\frac{b_1}{a_1}\right) \tag{81}$$

where, $a_1 = \frac{-1}{2\sinh(\lambda L_1)}\left[\psi_{s1}e^{-\lambda L_1} - \psi_{d1}\right]$ (82)

and

$$b_1 = \frac{-1}{2\sinh(\lambda L_1)}\left[-e^{\lambda L_1}\psi_{s1} + \psi_{d1}\right] \tag{83}$$

Now, the minimum surface potential or virtual cathode potential, $\phi_{s1,\min}$ under the control gate region can be obtained by putting Eq. (81) into Eq. (73) as

$$\phi_{s1,\min} = 2\sqrt{a_1 b_1} - \sigma_1 \tag{84}$$

4.2 Threshold Voltage Modeling

For an unstrained-Si MOSFET, the threshold voltage V_{th} is defined as that value of the gate voltage V_{gs} at which a conduction channel is induced under the gate oxide. Therefore, in a conventional unstrained-Si MOSFET, the threshold voltage is taken to be that value of the gate–source voltage at which the virtual cathode potential equals twice the difference between the extrinsic Fermi level in the bulk and the intrinsic Fermi level of silicon (i.e. $\phi_{s,\min} = 2\phi_{f,Si}$ where, $\phi_{s,\min}$ is minimum surface potential) [32].

For the DMG strained-Si on $Si_{1-X}Ge_X$ MOSFET, the threshold condition is modified as in [20]

$$\phi_{s1,\min} = 2\phi_{f,Si} + \Delta\phi_{(s-Si)} = \phi_{th} \tag{85}$$

Hence, we can determine the value of the threshold voltage (V_{th}) by substituting Eq. (84) into Eq. (85) and solving for $V_{gs} = V_{th}$ as

$$V_{th} = \frac{-\eta + \sqrt{\eta^2 - 4\mathrm{P}\xi}}{2\mathrm{P}} \tag{86}$$

$$\mathrm{P} = V_1 V_2 - n^2 \tag{87}$$

$$\eta = U_2 V_1 + U_1 V_2 - 2nl \tag{88}$$

$$\xi = U_1 U_2 - l^2 \tag{89}$$

$$U_1 = \frac{(V_{P11} + m_1 - (V_{bi,s-Si} + m_1)\exp(-\lambda L_1))}{\sinh(\lambda L_1)} \tag{90}$$

$$V_1 = \frac{(V_{P12} + n(1 - \exp(-\lambda L_1))}{\sinh(\lambda L_1)} \tag{91}$$

$$U_2 = \frac{(V_{bi,s-Si} + m_1)\exp(\lambda L_1) - (V_{P11} + m_1)}{\sinh(\lambda L_1)} \tag{92}$$

$$V_2 = \frac{n(\exp(\lambda L_1) - 1) - V_{P12}}{\sinh(\lambda L_1)} \tag{93}$$

$$l = \phi_{th} + m_1 \tag{94}$$

$$V_{P11} = \frac{1}{U_3}\begin{bmatrix} \left(\cos ech(\lambda L_1) - \coth(\lambda L_1)\right)m_1 + \left(\cos ech(\lambda L_2) - \coth(\lambda L_2)\right)m_2 \\ + \cos ech(\lambda L_1)V_{bi,s-Si} + (V_{bi,s-Si} + V_{ds})\cos ech(\lambda L_2) \end{bmatrix} \tag{95}$$

$$V_{P12} = \frac{n}{U_3}\left[\cos ech(\lambda L_1) + \cos ech(\lambda L_2) - \coth(\lambda L_2) - \coth(\lambda L_1)\right] \tag{96}$$

$$U_3 = \coth(\lambda L_1) + \coth(\lambda L_2) \tag{97}$$

$$m_1 = \frac{\alpha_2 A_1 + \beta_1 C_1}{\alpha^2 - \beta^2} \tag{98}$$

$$m_2 = \frac{\alpha_2 A_2 + \beta_1 C_2}{\alpha^2 - \beta^2} \tag{99}$$

$$n = \frac{\beta_1 D - \alpha_2 B}{\alpha^2 - \beta^2} \tag{100}$$

$$B = \frac{C_f(2C_{SiGe} + C_{Si})}{C_{Si}(C_{SiGe} + C_{Si})t_{Si}^2} \tag{101}$$

$$D = \frac{C_f}{(C_{SiGe} + C_{Si})t_{SiGe}^2} \tag{102}$$

$$A_1 = \frac{qN_a}{\varepsilon_{Si}} + \frac{C_f(2C_{SiGe} + C_{Si})(V_{FB1,f})_{s-Si}}{C_{Si}(C_{SiGe} + C_{Si})t_{Si}^2} \tag{103}$$

$$A_2 = \frac{qN_a}{\varepsilon_{Si}} + \frac{C_f(2C_{SiGe} + C_{Si})(V_{FB2,f})_{s-Si}}{C_{Si}(C_{SiGe} + C_{Si})t_{Si}^2} \tag{104}$$

$$C_1 = \frac{qN_a}{\varepsilon_{SiGe}} - \frac{C_f(V_{FB1,f})_{s-Si}}{(C_{SiGe} + C_{Si})t_{SiGe}^2} \tag{105}$$

$$C_2 = \frac{qN_a}{\varepsilon_{SiGe}} - \frac{C_f(V_{FB2,f})_{s-Si}}{(C_{SiGe} + C_{Si})t_{SiGe}^2} \tag{106}$$

4.3 Drain Induced Barrier Lowering (DIBL) Modeling

Drain induced barrier lowering (DIBL) is a short-channel effect in MOSFETs causing a reduction of threshold voltage V_{th} of the transistor at the higher drain voltages. DIBL also affects the current of MOSFETs the current is increase with the increase in drain bias voltage due to this the output resistance the MOSFET is reduced.

In practice, DIBL can be formulated as follows [33]:

$$DIBL = \frac{V_{Th}(high) - V_{Th}(low)}{V(high) - V(low)} \tag{107}$$

Where $V_{Th}(high)$ is the threshold voltage measured at a higher drain voltage and $V_{Th}(low)$ is the threshold voltage measured at a very low drain voltage, generally in the range of 0.05 V or 0.1 V. $V(high)$ is the higher supply(drain) voltage and $V(low)$ is the low supply(drain). The units of DIBL are mV/V.

4.4 Results and Discussion

In this section, results obtained from theoretical models of surface potential and threshold voltage are compared with the numerical simulation results. Fig. 15 shows the surface potential profiles for single-material-gate (SMG) $s-Si$ and DMG $s-Si$ on $Si_{1-X}Ge_X$ MOSFETs structures. For the DMG structure, the screen gate workfunction is varied keeping the control gate workfunction same for all the cases. As the screen gate work function decreases, the minimum surface potential increases, reducing the source-channel barrier height and thereby decreasing the threshold voltage. Also, as the screen gate work function decreases the minimum surface potential shifts towards the source-side which then increasingly becomes immune to the drain voltage changes (i.e. lower drain induced barrier lowering (DIBL)). So, for $\varphi_{M2} = 4.2$ eV, the source-channel barrier height is minimum but is

highly immune to DIBL when compared to SMG structure. For $\varphi_{M2} = 4.6\,\text{eV}$, the barrier height is more compared to the case when φ_{M2} was $4.2\,\text{eV}$ but device is susceptible to DIBL.

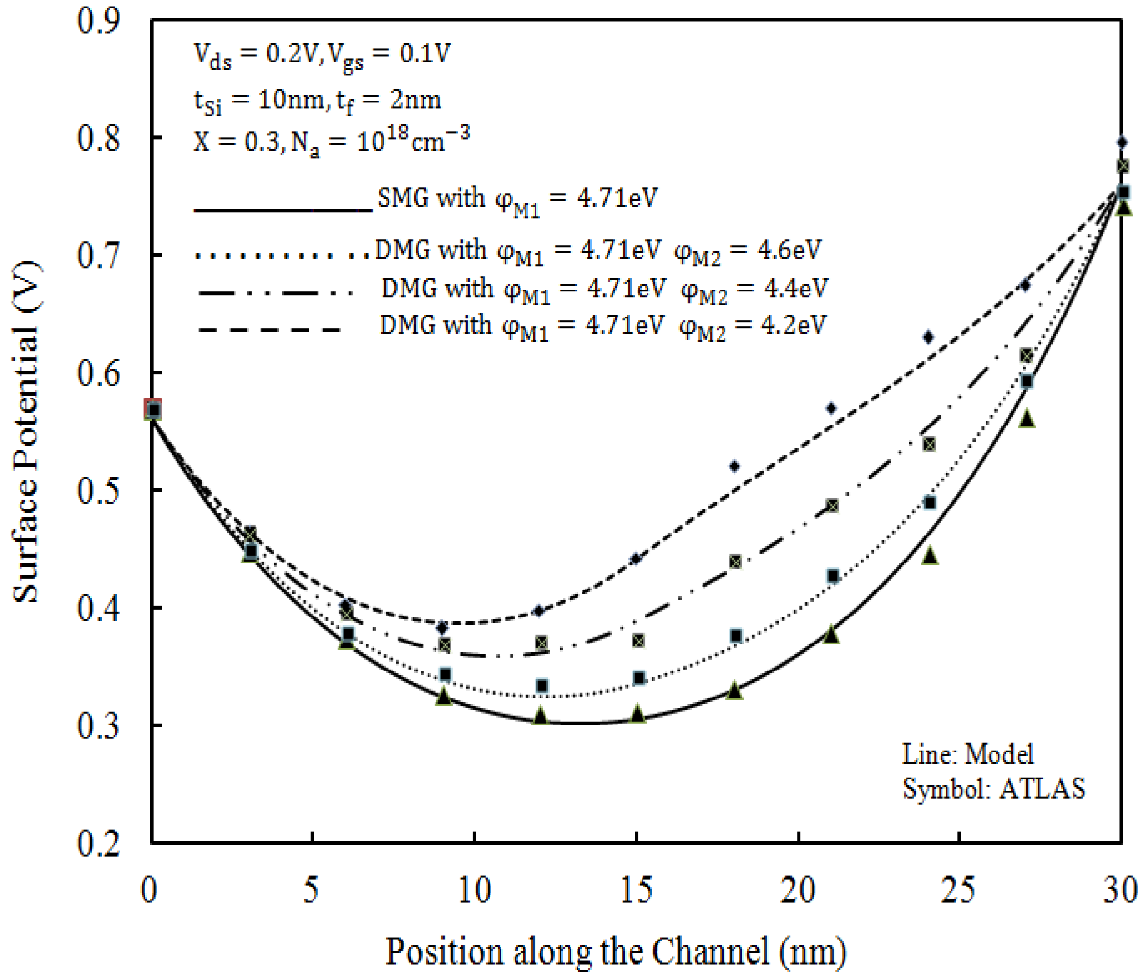

Fig. 15 Comparison of surface potential of Single Material Gate (SMG), and DMG (with different metal work function) strained MOSFETS against position along the channel length

Fig. 16 shows surface potential variations along the channel length (L) for different control-to-screen gate length ratios ($L_1 : L_2$). The step profile in the surface potential of the DMG $s\text{-}Si$ on $Si_{1-X}Ge_X$ MOSFET enhances the immunity of the device against undesired variations in the drain-to-source voltage (V_{ds}) by screening it effectively. It is observed that as

the screen gate length increases, the minimum surface potential increases leading to decrease in the channel barrier height. Also, the minimum surface potential point shifts towards the source side decreasing the influence of the drain on it. In other words, the device with equal control and screen gate length will be the optimized device in terms of V_{ds} immunity and barrier height.

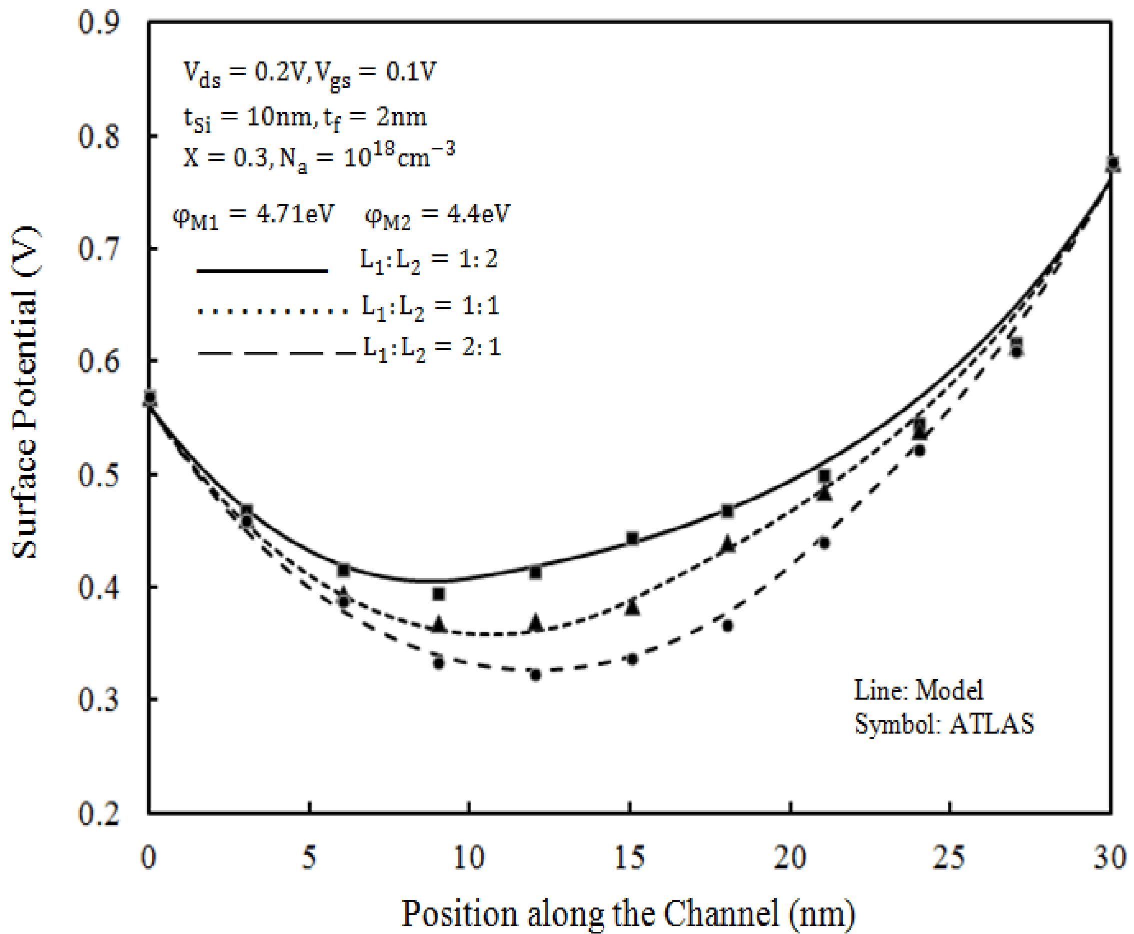

Fig. 16 Comparison of surface potential of DMG strained MOSFET against position along the channel length for different gate length ratios.

Li Jin *et. al* [17] showed that as L_2 increases, the point of peak electric field in the channel shifts toward the source end causing more uniformity of the electric field in the channel and improving carrier drift velocity and device speed. The increased carrier transport efficiency with decreasing L_1 causes lower HCE and improved DIBL.

Fig. 17 shows the channel potential variation along the channel length for different values of V_{ds} and Ge mole fraction (X). For a fixed amount of mole fraction, the minimum potential rises with the rise in V_{ds} showing the drain influence over it at a short channel length.

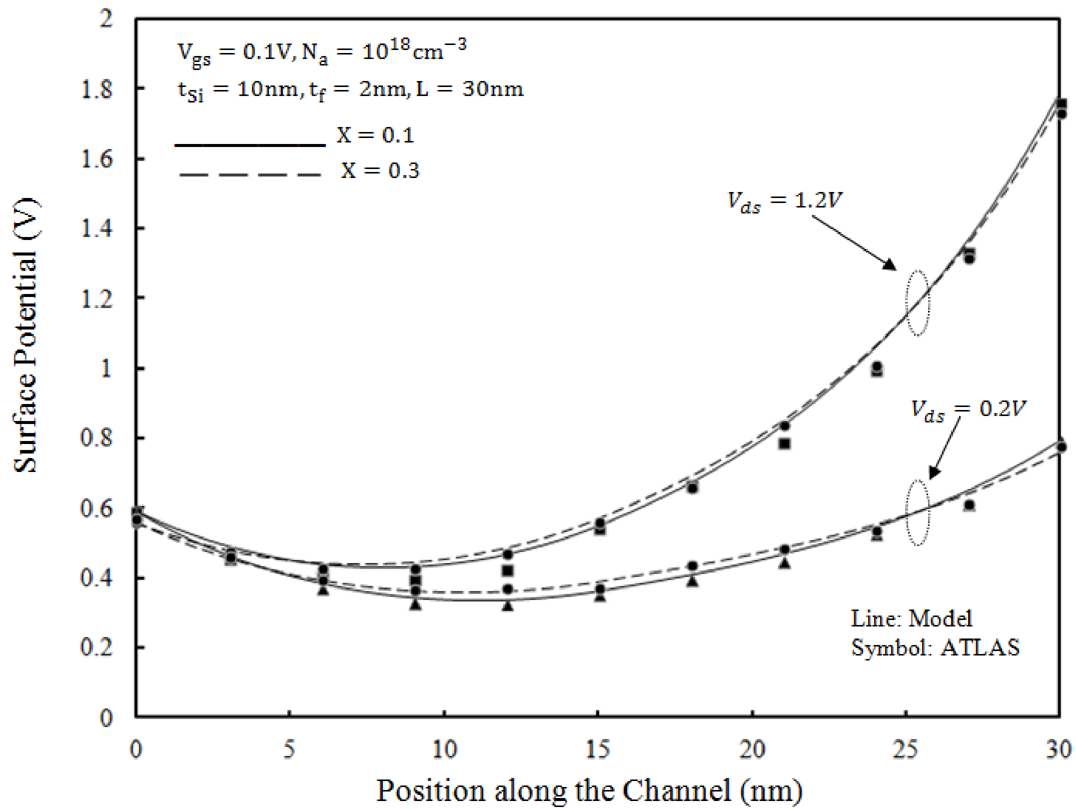

Fig. 17 Surface potential variation along the channel length for fixed gate length ratios for different Ge mole fractions X and for different V_{ds}

Fig. 18 shows the threshold voltage variations against different gate length for different values of Ge mole fraction. As evident from the curves, the magnitude of the threshold voltage decreases due to with increasing Ge content (X) because of decrease in flatband voltage, decrease in source-body/ drain-body built-in potential barrier and earlier onset of inversion due to decrease in ϕ_{th}. Now for the sub 75 nm channel length, the threshold falls steeply displaying the short channel behaviour. This is due to the charge sharing in the gate-S/D and also the built-in potential barrier lowering of the source-body/drain-body due to

significant overlap of the lateral source-body and drain-body depletion regions (x_{dl} as in Fig. 13) at such short channel lengths.

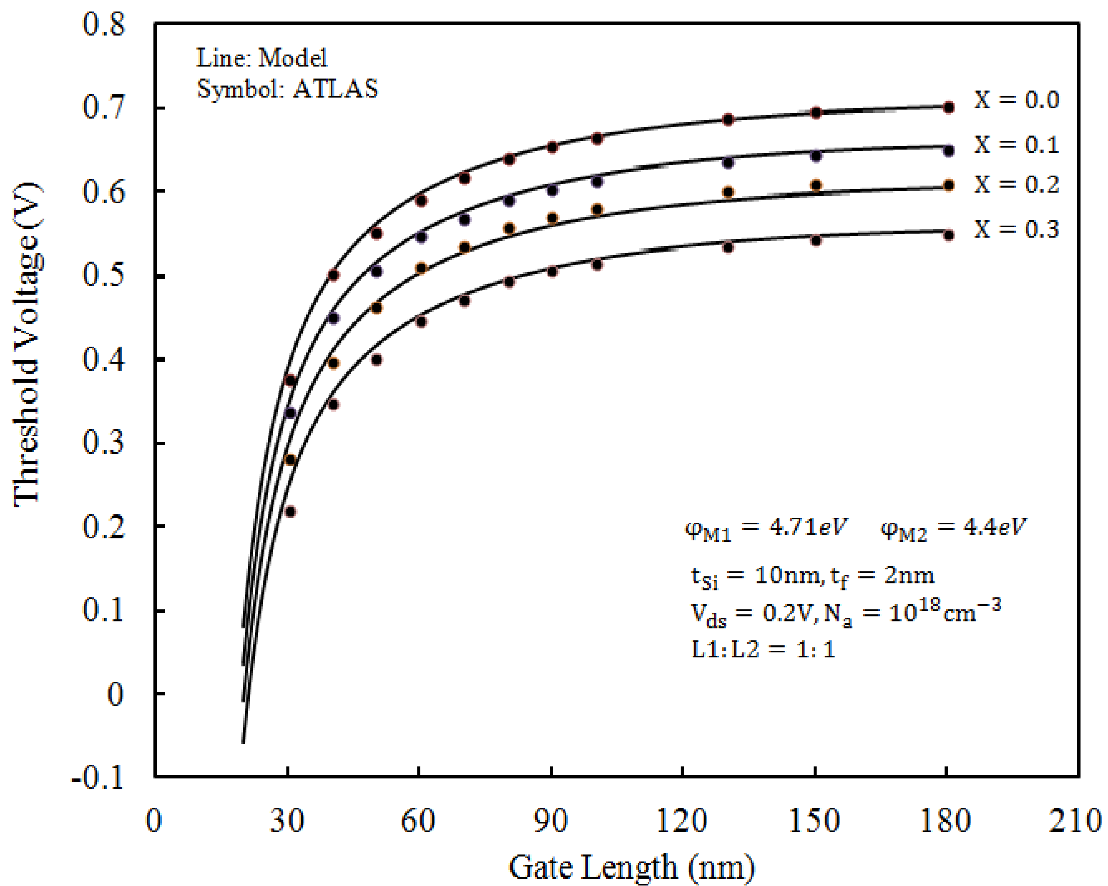

Fig. 18 Threshold voltage against device channel length for different Ge mole fraction X in the $Si_{1-X}Ge_X$ layer

Fig. 19 shows the threshold voltage variation against channel length for different gate length ratios ($L_1 : L_2$) and Ge mole fractions (X). It is observed that the threshold voltage is higher for the higher control gate length. This may be due to the higher channel barrier height for higher gate length ratio $(L_1 : L_2 = 2:1)$ as predicted in the Fig. 17. Further, the roll-off in the threshold curve is higher for the smaller gate length ratio of the device. This is attributed to the fact that the control gate loses its control over the channel at smaller length ratios. At smaller gate length ratio, the channel barrier height gets reduced giving rise to greater short channel effects.

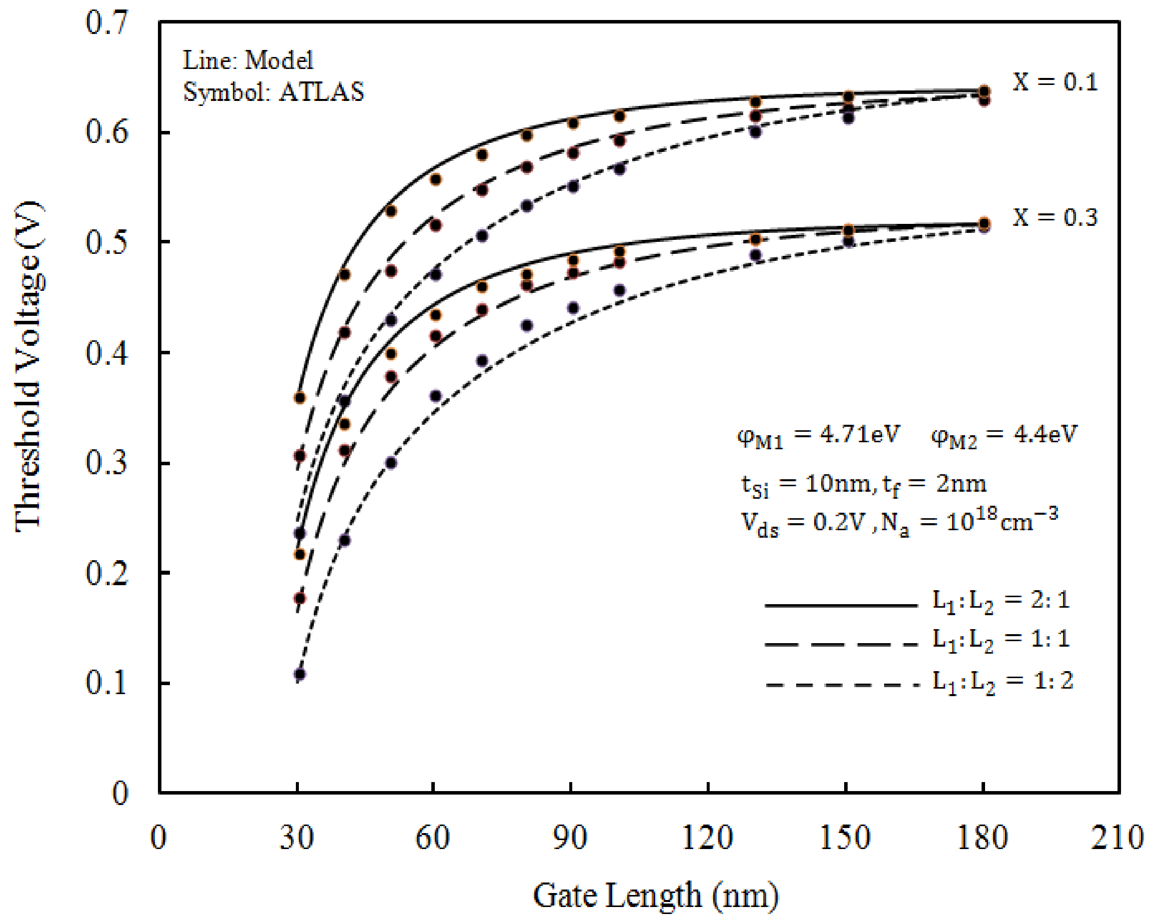

Fig. 19 Threshold voltage against device channel length (L) with different gate length ratios ($L_1 : L_2$) for different Ge mole fraction (X) in the $Si_{1-X}Ge_X$ layer

The only advantage in reducing the gate length ratio is in DIBL as discussed later. In addition, the decrease in the threshold voltage is observed with increasing strain (X) which is already discussed in Fig. 19.

Fig. 20 shows the threshold voltage variations with Ge mole fraction variations at different Si film thickness. As seen from the diagram, the threshold voltage is lower for higher strain at the same gate length. It is observed that the threshold voltage reduces considerably in a linear manner with increasing strain.

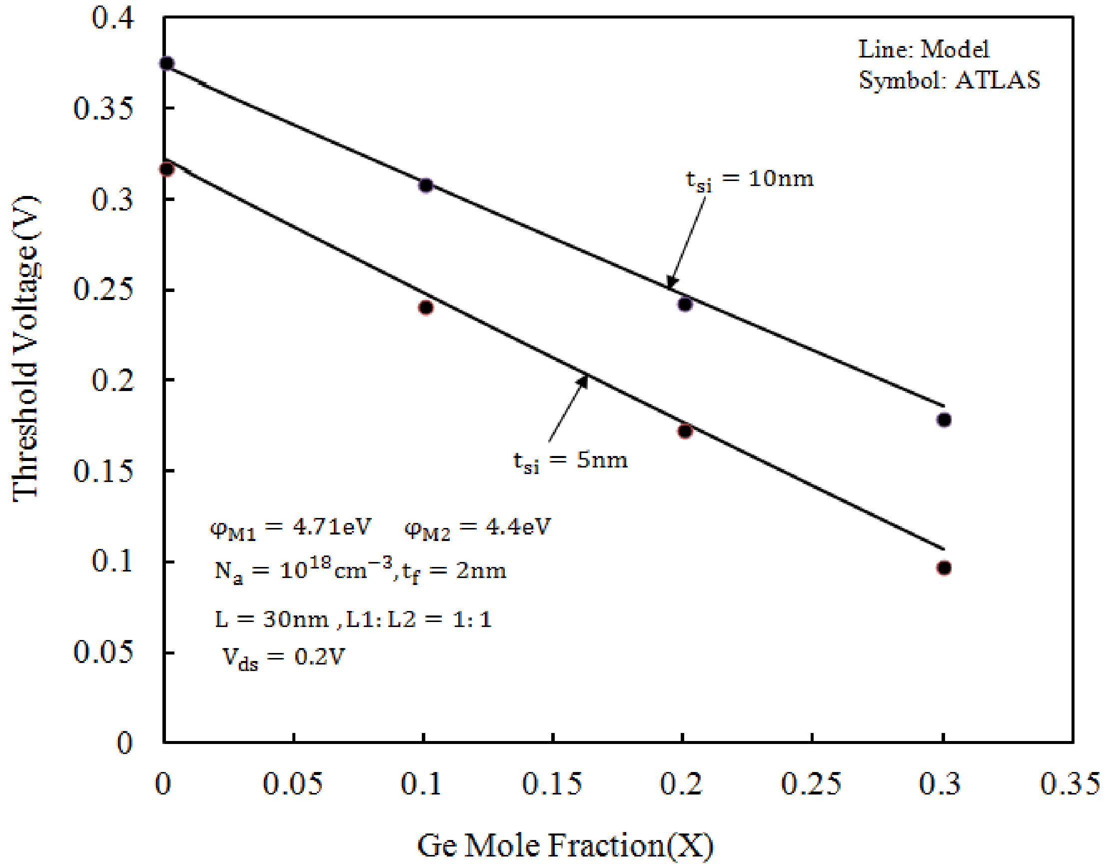

Fig. 20 Threshold voltage against Ge mole fraction (X) in the $Si_{1-X}Ge_X$ layer for different strained silicon layer thickness (t_{Si})

Fig. 21 shows the variation of the DIBL with gate length for different gate length ratios. The DIBL for a short-channel s−Si on $Si_{1-X}Ge_X$ MOSFET is computed as the difference between the linear (V_{ds} = 0.2 V) and saturation (V_{ds} = 1.2 V) threshold voltages [12]. The threshold voltage is extracted from simulated $I_D - V_{gs}$ curve as mentioned in simulation method and model section of the present manuscript. It is observed that the DIBL is negligible for longer channel lengths (above 100 nm), but is significant for smaller channel lengths (below 60–70 nm). As seen from the Fig. 21, the DIBL increases sharply as the length of the control gate increases. This may be attributed to the shift of the minimum surface potential point towards the drain side when the length of control gate increases for fixed channel length as shown in Fig. 16. It should be noted that if the surface potential point is more close to the drain side,

the source channel barrier height will have strong affinity with drain voltage and hence more DIBL will be observed in the device.

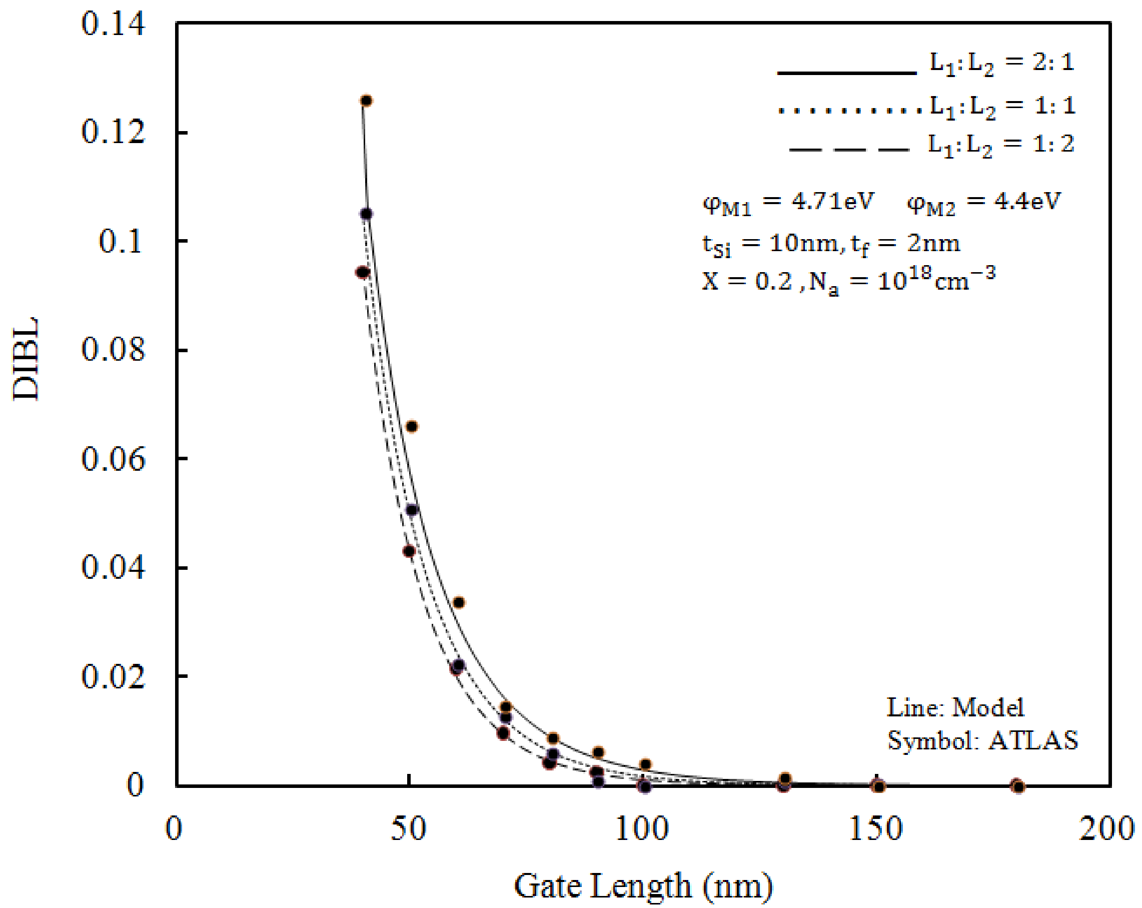

Fig. 21 Drain induced barrier lowering (DIBL) against device channel length (L) for different gate length ratios $(L_1 : L_2)$.

CHAPTER 5

CONCLUSIONS

Chapter 5

5 CONCLUSIONS

The developed 2-D analytical model for surface potential and threshold voltage analyses the effectiveness of DMG structure in an $s-Si$ on $Si_{1-X}Ge_X$ substrate to suppress the hot carrier effects (HCEs) and drain induced barrier lowering (DIBL). The suppression of HCE and DIBL by the introduction of the dual material gate is attributed to the creation of a step-function in the channel potential profile which is verified by the simulations. An extensive analysis of the impact of numerous device parameters on the threshold voltage has been carried out. It may be concluded that the depreciation in the threshold voltage with increasing strain is improved by increasing the length of control gate for the given channel length and increasing the $s-Si$ thickness. Also, modifying the Ge mole fraction and the gate length ratio, DIBL can be controlled effectively. The derived 2-D analytical model is found to be in excellent agreement with the simulation results obtained from ATLAS™ from Silvaco. The developed model may prove to a useful tool to optimize the desired performance of the device parameters.

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