A Rigorous Simulation Based Study of Gate Misalignment Effects in Gate Engineered Double-Gate (DG) MOSFETs

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF

MASTER OF TECHNOLOGY
IN
VLSI DESIGN AND EMBEDDED SYSTEMS

By:
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY
ROURKELA, ORISSA, INDIA
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CERTIFICATE

This is to certify that the Thesis Report entitled "**A Rigorous Simulation Based Study of Gate Misalignment Effects in Gate Engineered Double-Gate (DG) MOSFETs**", submitted by **Mr. SANTUNU SARANGI bearing roll no. 211EC2111** in partial fulfilment of the requirements for the award of **Master of Technology in Electronics and Communication Engineering** with specialization in "**VLSI Design and Embedded Systems**" during session 2011-2013 at National Institute of Technology, Rourkela is an authentic work carried out by him under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other university/institute for the award of any Degree or Diploma.

Place: Rourkela

Date: 3rd June, 2013

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This thesis is dedicated to

the living memories of my father Late Brundaban Sarangi

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ACRONYMS

CGAA: Cylindrical Gate-All-Around

CLM: Channel Length Modulation

CMOS: Complementary Metal Oxide Semiconductor

DG: Double Gate

DIBL: Drain Induced Barrier Lowering

DMDG: Dual Material Double Gate

DSM: Drain Side Misalignment

FDSOI: Fully Depleted Silicon On Insulator

GAA: Gate All Around

HCE: Hot Carrier Effect

IC: Integrated Circuit

ITRS: International Technology Roadmap for Semiconductor

LAC: Lateral Asymmetric Channel

MISFET: Metal Insulator Semiconductor Field Effect Transistor

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

RF: Radio Frequency

SCE: Short Channel Effect

SMDG: Single Material Double Gate

SEMOI: Semiconductor On Insulator

SOI: Silicon-on-Insulator

SSM: Source Side Misalignment

TMDG: Triple Material Double Gate

TTL: Transistor Transistor Logic

UTC: Ultra Thin Channel

VLSI: Very Large Scale Integration

ABSTRACT

Currently, the expansion of VLSI industry is primarily focussed on the way to the efficiency of semiconductor devices which in turn is extremely dependent on the advancement in the CMOS technology. As the scaling down of device dimensions are being aggressive, carrier mobility reduced due to dopant fluctuation, gate tunnelling effect increases and p-n junction leakage current increases. More precise and novel device structures are required to be developed for satisfying the above requirements. These needs have led to development of alternative technology. The double-gate (DG) Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFETs) are the front runner among the sub-100 nm devices because, both front and back gate of DG MOSFETs control the channel region simultaneously and these are also well suited for ultra-low-voltage operation due to the inherent suppression of short channel effects (SCEs), reduced drain-induced barrier lowering (DIBL), excellent scalability and un-doped body doping. However, alignment between the front and back gate is an issue of concern during fabrication because its influences are baleful for device performance. Further, the issue of alignment between front and back gates assumes greater seriousness for gate engineered DG MOSFETs, like double material double gate (DMDG) or triple material double gate (TMDG) MOSFETs for improving the device performance.

In this work, a numerical simulation based study on the effects of gate misalignment between the front and the back gate for gate engineered double-gate (DG) Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFETs) has been presented. A comparative study of electrical characteristics and its effects on device performance between single material double gate (SMDG), double material double gate (DMDG) and triple material double gate (TMDG) MOSFETs have been investigated qualitatively. Both source side misalignment (SSM) and drain side misalignment (DSM) of different lengths in the back gate have been considered to investigate the effects of gate misalignment on device performance. In this context, an extensive simulation has been performed by a commercially available two-dimensional (2D) device simulator (ATLAS^{TM}, SILVACO Int.) to figure out the impacts of misalignment on device characteristics like surface potential, threshold voltage, drain-induced-barrier lowering (DIBL), subthreshold swing, subthreshold current, maximum drain current, transconductance and output conductance.

Chapter 1

1 INTRODUCTION

1.1 MOSFET and its scaling: A Historical Perspective

Over the past thirty years, the growth of microelectronics, automation, information sharing, signal processing has strongly dependent on very large scale integrated circuit (VLSI) industry. Advancement of computer and fascinating gadgets with every possible applications; be it audio, video, any type of game or high speed communication; revolutionized the world of interconnectivity and entertainment. It's all credited to the high speed ultra small sized, low power semiconductor devices, sensors, all new materials and their implementation through VLSI design.

It all starts with the insight of Lilienfeld of Insulated Gate Field Effect Transistor in 1925 which bore the potential to substitute the vacuum tube technology with small sized semiconductor transistor technology [1]. The first practical exhibition took place in 1960 by Kahng and Atilla [2] in the form of the Silicon-based Metal Oxide Semiconductor Field Effect Transistor (MOSFET). In 1958, Jack Kilby at Texes Instruments conceived the idea of the Integrated Circuits (IC) and Robert Noyce from the Fairchild Corp. fabricated the first IC (a S-R flip flop) as shown in Fig. 1.1[3]. It then came in 1959 when Richard Feynman delivered his notable speech, "There is plenty of room at the bottom", acknowledging the high performance accomplishment of the materials at the reduced dimensions [4]. Another visionary prophecy from Gordon Moore, then with Fairchild Corp. and co-founder of Intel, states that, "The number of transistors on integrated circuits doubles approximately every two years". This prophecy has been accurate for more than 3 decades as shown in Fig. 1.2. The year 1962 saw the growth of the first logic family, the TTL [3]. Intel introduced the first microprocessor in 1972 which used more than 2000 PMOS transistors. Following the Moore's law the transistor count increased exponentially [3]. Then next few microprocessors used the NMOS technology which was routed out soon due to heavy dynamic power consumption with the increased number of transistor per chip. Then with the advent of the CMOS technology which consumed the least power, scaling technology sailed from the small scale integration (SSI) to Very Large Scale Integration (VLSI) and now spearheading towards the nanotechnology.

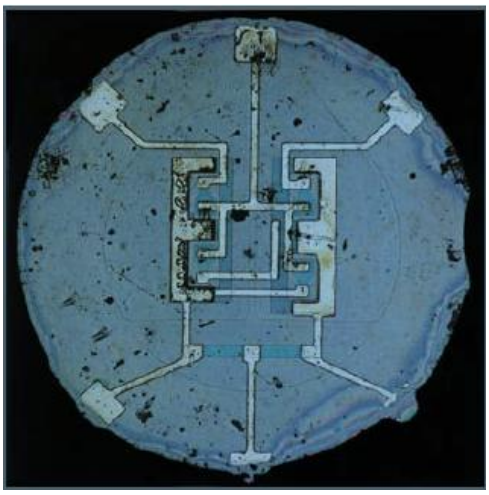

Figure 1.1.1: First IC fabricated by Jay Last's development group at Fairchild Corp. [4]

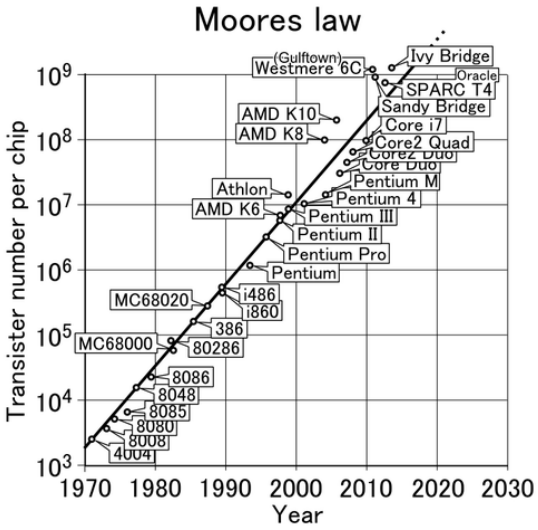

Figure 1.1.2: Transistor Integration on Chip displaying Moore's Law. [5]

1.2 Overview of MOSFETs

The metal oxide semiconductor field effect transistor (MOSFET), the heart of integrated circuits is generally used for the purpose of switching and amplifying electronic signals. Though the MOSFET is recognized as four-terminal device with source (S), drain (D), gate (G), and body (B) terminals [6], the body (or substrate) of the MOSFET frequently attached to the source terminal, making it a three-terminal device. Because these two terminals are normally coupled to each other inside, only three terminals appear in electrical diagrams. Till now, MOSFET is the most universal transistor in both analog and digital circuits, even if the bipolar junction transistor was at one time much more recognizable.

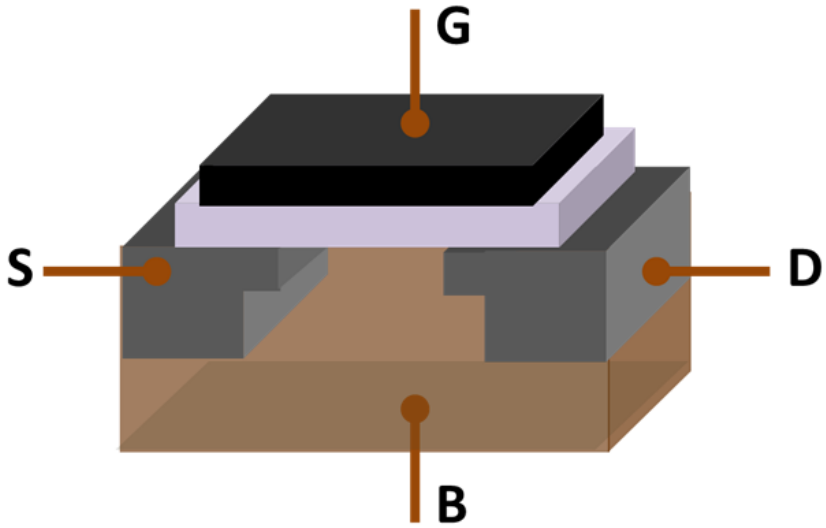

Figure 1.2.1: Cross sectional view of conventional bulk MOSFET [7]

In enhancement mode MOSFETs, a voltage drop across the oxide induces a conducting channel between the source and drain contacts due to the field effect. The name enhancement mode refers to enhance of conductivity with increase in oxide field that attract carriers to the channel, also known as the inversion layer. The channel can include electrons (for n-type MOSFET), or holes (for p-type MOSFET), reverse in nature to the substrate, so n-type MOSFET is prepared with a p-type substrate, and p-type MOSFET with an n-type substrate. In the rare used depletion mode MOSFET, the channel contains of carriers in a surface layer of reverse type to the substrate, and conductivity is degrades by application of a field that removes carriers from this surface layer [8].

The gate metal in the MOSFET is now a misinterpretation because the formerly metal gate material is now often a sheet of poly-silicon. Until the mid of 1970s Aluminium had been the gate material, when poly-silicon became foremost, due to its capability to form self aligned gates. Metallic gates are regaining recognition, since it is hard to increase the speed of operation of devices without using metal gates. Similarly, the oxide in the name can be a misinterpretation, as different dielectric materials are used with the aim of obtaining strong channels with applied smaller voltages.

1.3 MOSFET operation

1.3.1 Metal Oxide Semiconductor structure

The conventional metal oxide semiconductor (MOS) structure is obtained by growing a layer of silicon dioxide (SiO_2) on top of a silicon substrate and depositing a layer of metal or polycrystalline silicon. As the silicon dioxide is a dielectric substance, its structure is alike to a planar capacitor; with one of the electrodes is semiconductor. When a voltage is applied to a MOS structure, it modifies the sharing of charges in the semiconductor. If we consider a p-type semiconductor, a positive voltage, V_{GS}, from gate to substrate creates a depletion layer by forcing the positively charged holes away from the insulator- semiconductor interface, leaving uncovered a carrier-free region of immobile, negatively charged acceptor ions. If gate to source voltage is sufficient, a high concentration of negative charge carriers forms in an inversion layer situated in a thin layer next to the interface between the semiconductor and the insulator. Unlike the MOSFET structure, where the inversion layer electrons are supplied speedily from the source to drain, in the MOS capacitor they are created much more slowly by thermal generation through carrier generation and recombination in the depletion region. Usually, the gate voltage at which the concentrations of electrons in the inversion layer are the same as the concentrations of holes in the body is called the threshold voltage. When the gate to source exceeds the threshold voltage, it is known as overdrive voltage.

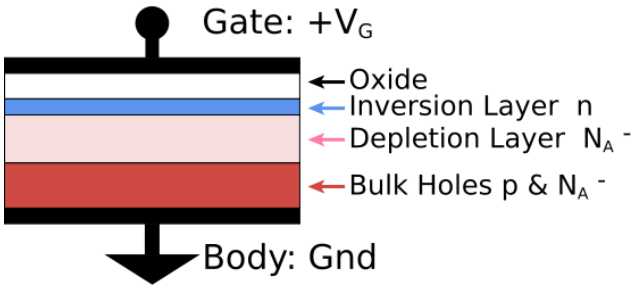

Figure 1.3.1: Metal-oxide-semiconductor structures on p-type silicon [7]

1.3.2 MOSFET structure and channel formation

A MOSFET is based on the modulation of charge concentration by a MOS capacitance between a substrate electrode and a gate electrode located above the silicon substrate and insulated from all other device regions by a gate dielectric sheet which in the case of a MOSFET is a silicon dioxide. If dielectrics other than silicon dioxide are employed the device may be referred to as a metal-insulator-semiconductor FET (MISFET).

If the MOSFET is an n-channel MOSFET, then the source and drain are 'n+' regions and the substrate is a 'p' region. If the MOSFET is a p-channel MOSFET, then the source and drain are 'p+' regions and the body is a 'n' region. The source is so named because it is the source of the charge carriers (electrons for n-channel, holes for p-channel) that flow through the channel; similarly, the drain is where the charge carriers leave the channel.

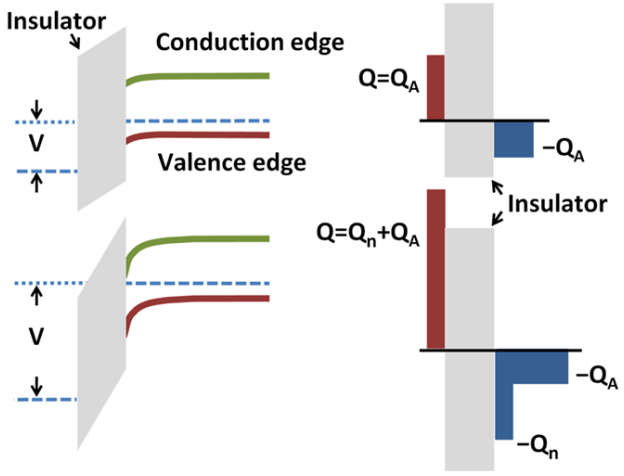

Figure 1.3.2: Channel formation in n-channel MOSFET [7]

In a semiconductor the occupancy of the energy bands is set by the position of the Fermi level relative to the semiconductor energy band edges. As described above, and shown in the fig. 1.6, with sufficient gate voltage, the valence band edge is driven far from the Fermi level, and holes from the body are driven away from the gate. At larger gate bias still, near the semiconductor surface the conduction band edge is brought close to the Fermi level, populating the surface with electrons in an inversion layer or n-channel at the interface between the p region and the oxide. This conducting channel extends between the source and the drain, and current is conducted through it when a voltage is applied between the two electrodes. Increasing the voltage on the gate leads to a higher electron density in the inversion layer and therefore increases the current flow between the source and drain.

For gate voltages less than the threshold value, the channel is lightly populated, and a very minute subthreshold leakage current can flow between the source and the drain. When a negative gate to source voltage (positive source to gate) is applied, it creates a p-channel at the surface of the oxide and semiconductor, equivalent to the n-channel case, but with reverse polarities of charges and voltages. When a voltage less negative than the threshold value (a

negative voltage for p-channel) is applied between gate and source, the channel disappears and only a very small subthreshold current can flow between the source and the drain.

The device may contain Silicon on Insulator (SOI) device in which a buried oxide (BOX) is formed under a thin semiconductor layer. If the channel region between the BOX region and gate dielectric is very thin, then very thin channel region is known to as an ultrathin channel (UTC) region with the source and drain regions formed on either side thereof above the thin semiconductor layer. Other way, the device may comprise a semiconductor on insulator (SEMOI) device in which semiconductors other than silicon are employed.

1.4 MOSFET scaling

Over the past thirty years, the MOSFET has constantly been scaled down in dimension; typical MOSFET channel lengths were once quite a few micrometres, but recent integrated circuits are incorporating MOSFETs with channel lengths of tens of nanometres. Robert Dennard's work on scaling theory was essential in recognising that this ongoing reduction was possible. Intel began manufacture of a process featuring a 32 nm feature size (with the channel being even shorter) in late 2009. The semiconductor industry maintains a "roadmap", the ITRS [9], which sets the pace for MOSFET growth. Historically, the difficulties with decreasing the size of the MOSFET have been connected with the semiconductor device fabrication process, the need to use very low voltages, and with inferior electrical performance necessitating circuit reshape and innovation

One more basic benefit that CMOS technology provides is the presence of certain scaling laws. The International Technology Roadmap for Semiconductor (ITRS) has laid a roadmap to direct this scaling in terms of power consumption and cost incurred. As obvious from the ITRS 2010 in Fig. 1.6.1, the year 2013 with technology node 22nm is planning to have physical channel length of 10nm and less. The latest Itanium-7 quad core GPU processor contains more 1.1 billion transistors in a 160 mm^2 chip area and Intel 32 nm SRAM wafer (1 Tb) has about 800 billion transistors [10]. Device engineers all over the world have made this speculate come true through a magic named “Scaling”. Scaling is defined as controlled change of structural and electrical properties such that it acquires smaller chip area while maintaining the long channel characteristic and performance. Dennarad and fellow workers suggested the scaling approach in 1972 [11].Scaling not only decreases the device dimensions making to a higher packing density but it also leads to major dynamic power reduction through lesser voltages. The scaling come up to stated that both the horizontal and

vertical dimensions of the transistor should be scaled by the same scaling factor in order to avoid the SCEs and ensure good electrostatic control when fabricating the smaller devices, and by the same scaling factor, the supply voltage should be reduced and substrate doping concentration should be increased.

1.5 Reasons for MOSFET scaling

Smaller MOSFETs are attractive for a number of reasons. The main reason to build transistors smaller is to group more and more devices in a given chip area. This results in a chip with the same functionality in a lesser area, or chips with more functionality in the identical area. As fabrication costs for a semiconductor wafer are relatively fixed, the cost per integrated circuits is mostly related to the number of chips that can be produced per wafer. Hence, smaller ICs allow more chips per wafer, decreasing the price per chip. In fact, over the past 30 years the number of transistors per chip has been doubled every 2–3 years once a new technology node is introduced. For example the number of MOSFETs in a microprocessor fabricated in a 45 nm technology can well be twice as many as in a 65 nm chip. This doubling of transistor density was first experiented by Gordon Moore in 1965 and is commonly referred to as Moore's law [12].

It is also usual that smaller transistors switch more rapidly. For example, one approach to dimension reduction is a scaling of the MOSFET that requires all device sizes to decrease proportionally. The major device dimensions are the channel length, channel width, and oxide thickness. When they are scaled down by the same factor, the transistor channel resistance does not modify, while gate capacitance is cut by that factor. Hence, the RC delay of the transistor scales with a similar factor.

While this has been conventionally the case for the older technologies, for the state-of-the-art MOSFETs reduction of the transistor dimensions does not necessarily transform to higher chip speed because the delay due to interconnections is more significant.

1.6 Scaling problems

Manufacturing MOSFETs with much smaller channel lengths than a micrometre is a big challenge, and the difficulties of semiconductor device fabrication are always a warning factor in advancing integrated circuit technology. In recent years, the small dimension of the MOSFET, under a few tens of nanometres, has created operational troubles.

Integration of billions of transistors on a chip has been realizable due to the possibility to pattern every smaller feature on silicon through optical lithography. As optical lithography enters the sub-wavelength regime, light diffraction and interference from sub wavelength pattern feature causes image disorder. Therefore, patterning becomes difficult without adopting resolution enhancement techniques.

The ITRS's most recent projection provides some insight as to current market drivers. Fig. 4 illustrates that the power consumption trend versus power requirements is creating the "Power Gap" akin to the "Design Gap" that the industry dealt with a decade ago. This gap is creating a need to manage power at all levels of abstraction and majorly at the device level.

The power consumption is approximated by [8]

$$P_{diss} = P_D + P_S = \alpha f C_L V_{DD}^2 + V_{DD}\left(I_{leakage} + I_{th} 10^{-\frac{V_{th}}{s}} \right) \tag{1.1}$$

where P_D is the dynamic power dissipation, P_S is the static power dissipation, α is the activity factor, C_L is the load capacitance, V_{DD} is the supply voltage, $I_{leakage}$ is the total leakagecurrent, I_{th} is the threshold current, V_{th} is the threshold voltage and s is the subthreshold swing. The power consumption is lowered through lower V_{DD}, $I_{leakage}$ and s; and higher V_{th}.

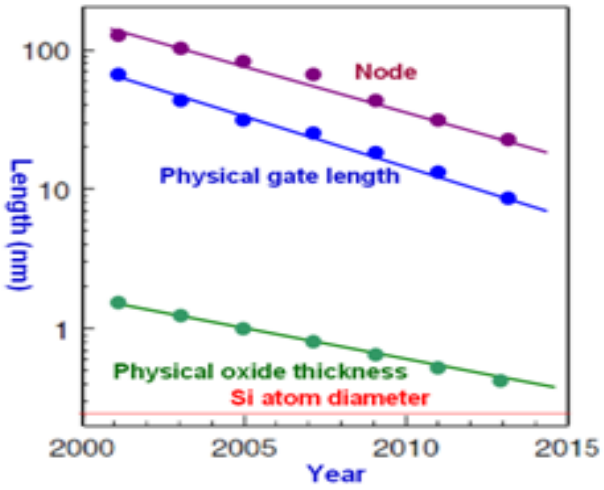

Figure 1.6.1: Shrinking gate length with of scaling. (Courtesy: ITRS 2010)

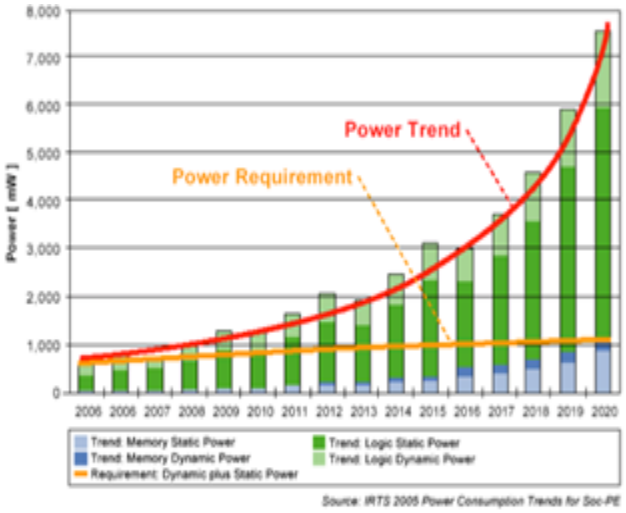

Figure 1.6.2: Power Consumption trends with years of scaling. (Courtesy: ITRS 2005)

Thus V_{DD} and V_{th} are in conflict for which the gate oxide needs to be scaled tremendously which in turn increases gate tunnelling leakages. Also, higher substrate doping is must to check the short channel effects (SCEs) but again this diminishes the current drive due to increased scattering. To trade-off between the power consumption, SCE and the lower current, is the need of the hour which the conventional MOSFETs fails to achieve. This gives way to creation of alternative device structures and architectures to continue further CMOS scaling.

1.6.1 Higher subthreshold conduction

As MOSFET geometries minimize, the voltage that can be applied to the gate must be reduced to preserve reliability. To preserve performance, the threshold voltage of the MOSFET has to be decreased as well. As threshold voltage is reduced, the transistor cannot be turn-on from complete turn-off with the less voltage swing available; the circuit design is conciliation between strong current in the ‘on’ case and less current in the off case and the application find out whether to favour one over the other. Subthreshold leakage (including subthreshold current conduction, gate-oxide leakage current and reverse biased junction leakage), which was mistreated in the past, now can consume upwards of half of the total power consumption of recent high-performance VLSI chips [13,14,15].

1.6.2 Increased gate-oxide leakage

The gate oxide, which acts as insulator between the gate and channel, should be prepared as thin as possible to enhance the channel conductivity and performance when the transistor is on and to lessen subthreshold leakage when the transistor is off. However, with recent gate oxides with a thickness of around 1.2 nm the quantum mechanical phenomenon of electron tunnelling occurs between the gate and channel, leading to more power consumption.

Silicon dioxide has conventionally been used as the gate insulator. Silicon dioxide however has a retiring dielectric constant. Raising the dielectric constant of the gate dielectric permits a thicker layer while keeping a high capacitance. All else equal, a higher dielectric thickness decreases the quantum tunnelling current through the dielectric between the gate and the channel. Insulators that have a higher dielectric constant than silicon dioxide, such as hafnium based silicates and zirconium based oxides are being used to lessen the gate leakage from the sub-micrometer technology node onwards.

On the other hand, the barrier height of the current gate insulator is an significant consideration; the difference in conduction band energy between the semiconductor and the dielectric (and the corresponding difference in valence band energy) also increases leakage current level. For the conventional gate oxide, silicon dioxide, the previous barrier is approximately 8 eV. For many other dielectrics the value is considerably lower, tending to increase the tunnelling current, somewhat opposing the benefits of higher dielectric constant. The extreme gate-source voltage is calculated by the strength of the electric field able to be sustained by the gate dielectric before significant leakage occurs. Since the insulating dielectric is made thinner, the electric field magnitude within it goes high for a constant voltage. This requires using lower voltages with the thinner dielectric.

1.6.3 Increased junction leakage

To make devices smaller, junction design has become more complex, forcing to higher doping levels, shallower junctions, halo doping etc.[16,17] all to reduce drain induced barrier lowering (DIBL) . To remain these complicated junctions in place, the annealing steps previously used to take away damage and electrically active defects must be partial. Higher doping is also related with thinner depletion layers and more recombination centres that result in enhanced leakage current, even with no lattice damage.

1.6.4 Lower output resistance

For analog functions, good gain requires high MOSFET output resistance, which is to say, the MOSFET current should vary only a little with the applied drain-to-source voltage. As devices are made smaller, the influence of the drain competes more successfully with that of the gate due to the growing closeness of these two electrodes, increasing the sensitivity of the MOSFET current to the drain voltage. To counter the resulting decrease in output resistance, circuits are made more complicated, either by requiring more devices, for example the cascode and cascade amplifiers, or by feedback circuitry using operational amplifiers, for example a circuit like that in the adjacent figure.

1.6.5 Lower transconductance

The transconductance of the MOSFET decides its gain and is directly proportional to hole or electron mobility depending on device type, for low drain voltages. As MOSFET dimension is decreased, the fields in the channel improve and the dopant impurity levels increases. Both changes decrease the carrier mobility, and thus the transconductance. As channel lengths are decreased with no proportional reduction in drain voltage, increasing the electric field in the channel, the result is limiting the current, velocity saturation of the carriers, and the transconductance.

1.6.6 Interconnect capacitance

Conventionally, switching time was roughly proportional to the gate capacitance of MOSFETs. On the other hand, with transistors becoming smaller and number of transistors being located on the chip, interconnect capacitance (the capacitance of the metal-layer connections between different parts of the chip) is becoming a great percentage of capacitance [18, 19]. Signals have to pass through the interconnection, which leads to amplified delay and degrade performances.

1.6.7 Heat production

The increasing density of MOSFETs on an integrated circuit makes difficulties of substantial localized heat generation that can hurt circuit operation. Circuits work more slowly at high temperatures, and have decreased constancy and shorter lifetimes. Cooling devices and methods and heat sinks are now necessary for many integrated circuits including microprocessors.

Power MOSFETs are at danger of thermal runaway. As their on-state resistance increases with temperature, if the load is approximately a constant-current load then the power loss increases correspondingly, generating extra heat. When the heat sink is not intelligent to remain the temperature low enough, the junction temperature may increase rapidly and uncontrollably, resulting in devastation of the device.

1.6.8 Process variations

With MOSFETs becoming smaller, the number of atoms in the silicon that create many of the transistor's properties is becoming fewer, with the result that control of dopant numbers and placement is more random. During chip manufacturing, random process variations affect all transistor dimensions: length, width, junction depths, oxide thickness *etc.*, and become a greater percentage of overall transistor size as the transistor shrinks. The transistor characteristics become less certain, more statistical. The random nature of manufacture means we do not know which particular example MOSFETs actually will end up in a particular instance of the circuit. This uncertainty forces a less optimal design because the design must work for a great variety of possible component MOSFETs [20].

1.6.9 Modeling challenges

Modern ICs are computer-simulated with the aim of obtaining working circuits from the very first manufactured lot. As devices are miniaturized, the difficulty of the processing makes it hard to predict exactly what the ultimate devices look like, and modelling of physical processes becomes more challenging as well. In addition, microscopic variations in structure due simply to the probabilistic nature of atomic processes require statistical predictions. These factors combine to make adequate simulation and "right the first time" manufacture difficult.

To minimize the difficulties of small size bulk MOSFETs, Researchers and engineers discover several alternative device structures, by which the technology can further scaled down with a improved performance. These are, double gate (DG) MOSFETs, Strained MOSFETs, gate all around (GAA) MOSFETs etc. Double gate MOSFET is one of the improved device structure for reducing short channel effects.

1.7 Technology Boosters: Solution to Scaling

1.7.1 Channel Engineering Techniques

Shallow S/D Junction

Lowering the source/drain junction depths (especially near the gate edge, where the source/drain regions are called ‘extensions’) reduces the drain coupling to the source barrier. However, as the source/drain junction depths get shallow, their doping must be increased so as to keep the sheet resistance constant. Solid solubility of dopants puts an upper limit (~10^{20} cm^{-3}) on the doping density. Therefore, further reduction in 13 junction depth causes an increase in the series resistance encountered in accessing the channel. Also, from a technological point of view, it becomes difficult to form ultra shallow junctions that remain abrupt after the annealing steps needed to activate the dopants and achieve low resistivity [21]. The formation of abrupt S-D junctions also leads to an increase in the band-to-band tunneling leakage component. All these factors degrade the overall transistor performance.

Halo Doping

To overcome the SCEs, various channel engineering techniques like double-halo (DH) and single-halo (SH) or lateral asymmetric channel (LAC) devices have been proposed. In the subthreshold region, although the halo doping is found to improve the device performance parameters for analog applications (such as gm/Id, output resistance and intrinsic gain) in general, the improvement is significant in the LAC devices. Halo doping led to a higher drive current in the saturation region. The halo device pinch–off region occurs in the halo implant region, since that region is closest to the drain and has a threshold voltage higher than the uniformly doped region.

Strain

To maintain a lower junction electric field in the channel and non-overlap of the source and drain depletion in the channel, doping becomes imperative. But a serious effect of mobility degradation due to the impurity scattering comes in play with higher amount of channel doping. Also the threshold voltage variations take place due to random dopant fluctuations inside the channel. The mobility of the charge carriers is enhanced through a concept known as the strain technology. To sum it all the benefits of strain, it results in a modified lattice constant of the material; second a modified energy band structure to trap carriers through well formation and finally an enhanced mobility. By increasing the Ge concentration of the relaxed Si1-XGeX substrate, the amount of biaxial strain and therefore higher magnitude of the mobility enhancement can be achieved. Literature had confirmed a mobility enhancement factor of 2.3 for a 30% Ge concentration.

1.7.2 Gate Engineering Techniques

High-k dielectric

High-k/metal gates were introduced into mass production in 2007 by Intel in the 45 nm CMOS technology generation. This is the first time that traditional oxides or oxynitrides have been replaced in gate stacks, to enable continuous scaling of the EOT.

Metal Gate

Initially, poly-Si/high-k combination gate stack was considered as a route to improving gate leakage. However theoretical studies and experimental data show mobility degradation compared to the use of metal gates. Depending on the gate dielectric, the work function varies due to differing band alignments.

Multi-Material Gate

One of the prominent means to get rid of hot carrier effect (HCE) is using cascaded gate structure consisting of two or more metals of different work functions. This structure is commonly known as Double-Material-Gate (DMG) structure as proposed in 1999 by Long *et al.* [22] or Triple-Material-Gate (TMG) in 2008 proposed by Razavi *et al.*[23]. The metal gates are so cascaded that the gate near the drain is a metal (M_2) with lower work-function and the source side metal (M_1) is of relatively higher workfunction. As a result of this, the electron velocity and the lateral electric field along the channel increases sharply at the interface of the two gate material which further results in the increased gate transport efficiency. Li Jin *et al.* described how reduction of the HCE may be achieved by decreasing the control gate to screen gate ratio in a DMG strained-Si on insulator MOSFET [24]. Further, the structure creates a step-like surface potential profile in the channel and thereby ensures screening of the minimum potential point from drain voltage variations. The metal gate M_2 is thus rightfully known as the *Screen Gate* (L_2) and the metal M_1 as the *Control Gate* (L_1).

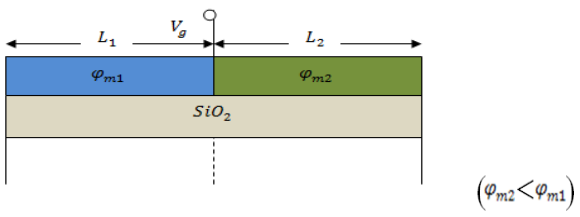

Figure 1.7.1: The dual metal gate structure

Multiple Gate

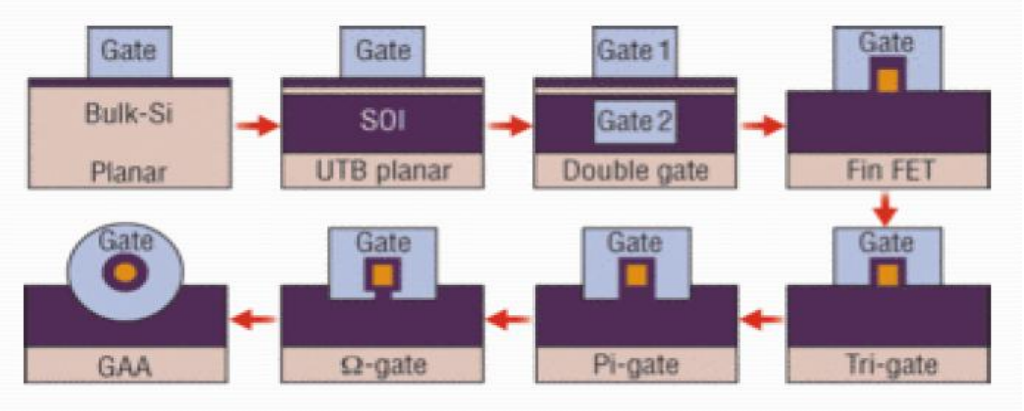

Figure 1.7.2: Progress of the MOSFET Technology through multiple-gates ([])

A potential candidate to continue the MOSFET scaling further is the fully-depleted silicon-on-insulator (FDSOI) MOSFET. Rigorous research of the FD SOI MOSFETs revels that this transistor possesses higher transconductance, lower threshold voltage roll-off and steeper subthreshold slope compare to the bulk MOSFET. In the FDSOI MOSFETs, the front gate parasitic junction (source/drain to channel) capacitances reduces resulting in higher switching speeds. The presence of the buried oxide (BOX) further removes drawbacks like leakage current, threshold voltage roll off, higher sub-threshold slopeand body effect. However, due to the ultra thin source and drain regions, FD SOI MOSFETs possess large series resistance which leads to the poor current drive capability of the device despite having excellent short-channel characteristics. To prevent the encroachment of electric field lines from the drain on the channel region, special gate structures can be used as shown in Fig. 16. Such "multiple"-gate devices include double-gate transistors, triple-gate devices such as the quantum wire, the FinFET and Δ-channel SOI MOSFET, and quadruple-gate devices such as the gate-all-around device, the DELTA transistor, and vertical pillar MOSFETs [25]. In a fully depleted SOI (FDSOI) device, most of the field lines propagate through the buried oxide (BOX) before reaching the channel region. Short-channel effects can be reduced in FDSOI MOSFETs by using a thin buried oxide and an underlying ground plane. This approach, however, has the inconvenience of increased junction capacitance and body effect. A much more efficient device configuration is obtained by using the double-gate transistor structure. Multi-gate MOSFETs realized on thin films are the most promising devices for the ultimate integration of MOS structures due to the volume inversion or volume accumulation in the thin layer (for enhancement- and depletion-type devices, respectively), leading to an increase

of the number and the mobility of electrons and holes as well as driving current (additional gain in performance in a loaded environment), optimum subthreshold swing and the best control of short channel effects and off-state current, which is the main challenge for future nanodevices due to the power consumption crisis and the need to develop green/sustainable ICs.

The triple-gate MOSFETs have made the advent of 22nm technology node feasible at industrial scale in 2011 [26, 27, 28]. One among various multi-gate structures, triple-gate MOSFET enjoys the silicon channel engaged from three sides giving enhanced on-current and reduced off-current. As the MOS dimension has attained its physical limit, the scaling beyond 22nm node is thus an insuperable task. The improvement in device performance, however, are believed to be continued in the company of multi-gate MOSFETs as they employ third dimension offering superb gate control over channel from several sides. The degree of gate controllability increases further with the quadruple-gate, the Omega/Pi-gate and the gate-all-around (GAA) structures respectively with better combinations of performance and energy efficiency [25]. As far as the characteristics lengths of the device structures are concerned, the gate-all-around MOSFETs offer the lowest characteristic length and hence the highest capability to be scaled for a given gate oxide thickness [16]. This capability gets coupled with the highest current drive per unit silicon area and demonstrates strong confinement of the electric field owing to the gate surrounding the channel.

1.8 Thesis Objectives

The main objectives of this thesis are to understand the structure design of gate engineered DG MOSFETs along with its back gate misalignment, while comparing them with single material double gate (SMDG) MOSFET, to investigate the device performance of SMDG, DMDG and TMDG MOSFETs in terms of device physics and misalignment effects. The analysis has been carried out with the help of simulation results by a commercially available two dimensional (2D) ATLAS device simulators.

1.9 Motivation

As conventional single gate MOSFETs are unable to perform well in less channel dimensions, because of short channel effects, high leakage currents and less control over threshold voltages, double gate MOSFETs gives the promise to the industry to take away the burden somehow. Again double gate MOSFETs enhancing their performances by using dual

material gate with different work function both in top and bottom of the device instead a single material gate. Furthermore to reduce hot carrier effect (HCEs) and channel length modulation (CLM) triple material double gate (TMDG) MOSFET come up to the field of research. But the misalignment effects between the top and bottom gate of the MOSFETs during fabrication degrades the performances of the device. So how it affects the performances on device parameters, whether the device is useful or not in this condition or if the device will perform well without any demerit then how much should be the optimal misalignment length. To give the answer of those above problem a thorough analysis is required about all the device characteristics.

1.10 Thesis Outline

Following the introduction, the rest of the thesis is organized as follows:

Chapter 2: This chapter describes the theoretical background and history of double-gate (DG) MOSFETs along with gate engineering technique. Details of gate misalignment effects at both drain side and source side are presented.

Chapter 3: This chapter describes the complete details of two dimensional (2D) ATLAS device simulator models used to simulate different types of the physical MOSFET structure.

Chapter 4: This chapter describes the complete details of the device structure and its simulation using the appropriate simulation model and numerical methods

Chapter 5: This chapter reports the simulation results of the misaligned effects of gate engineered double-gate (DG) MOSFETs along with some analysis.

Chapter 6: This chapter will conclude on the results from all the simulations. Discussions and analysis are included in this section. There is, also, a discussion on the suggestion for future work.

Chapter 2

2 LITERATURE REVIEW

2.1 Double gate MOSFETs

The double-gate (DG) MOSFET is one of the most promising architectures for scaling CMOS devices down to nanometre size [29], since they allow a significant reduction of the short-channel effects (SCEs), such as threshold voltage roll-off, drain-induced barrier lowering (DIBL), and subthreshold slope degradation [30,31,32], compared to planar single-gate MOSFETs. Moreover, in DG MOSFETs, the ultrathin channel material is preferred to be undoped. The absence of dopant atoms in the channel material eliminates adverse effects, such as mobility degradation [33] and random microscopic fluctuations of dopant atoms, which can lead to unwanted dispersion in the device characteristics [34]. Because of these advantages, a simple analytic threshold-voltage model for undoped DG MOSFETs is highly desirable in order to facilitate the design of such nanoscale devices

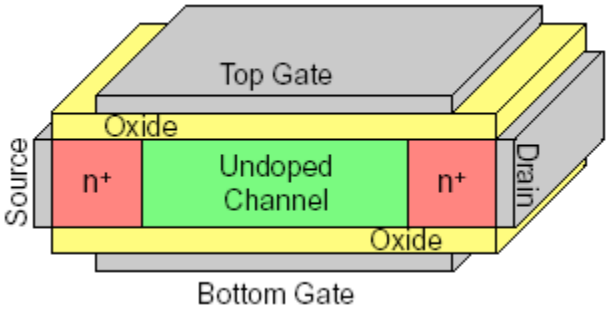

Figure 2.1.1: General double gate MOSFET structure

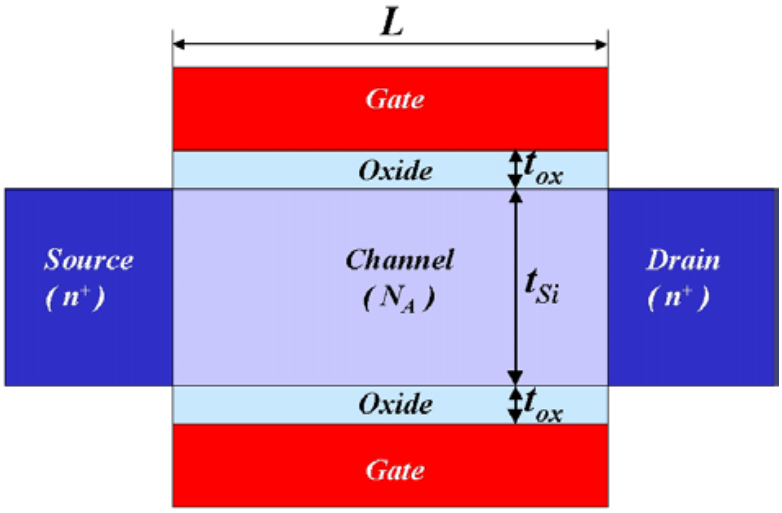

Figure 2.1.2: Cross-sectional view of double gate MOSFET structure

Double-gate MOSFET has two gates simultaneously controlling the charge in the thin silicon body layer, allowing for two channels for current flow. Because the silicon film is thin, a direct charge coupling exists between the front and back gate invariably [35], influencing the terminal characteristics of the device

General DGT Operation

The device can be operated in several ways [36].The voltage applied on the gate terminals controls the electric field, determining the amount of current flow through the channel. The most common mode of operation is to switch both gates simultaneously. Another mode is to switch only one gate and apply a bias to the second gate (this is called “ground plane” (GP) or “back-gate” (BG))

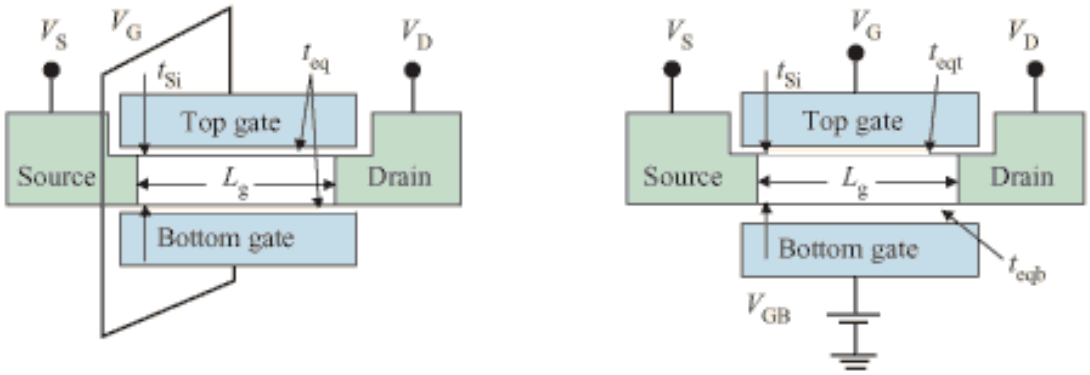

Figure 2.1.3: Operation of double gate MOSFET with ground plane and back gate mode

(1) Front channel alone conducting, the back channel being either depleted or accumulated.

(2) Both channels conducting, both or either of the channels being in weak or strong inversion.

The current-voltage characteristics of the device with the front channel in strong inversion and the back channel either in accumulation or in depletion has been modelled analytically [37,38,39] Since silicon films are thin, the electrical properties of MOSFETs fabricated are inherently influenced by the charge coupling between the front and back gates. Due to extremely small device dimensions, low voltage operation will be mandatory where the low threshold voltage is required [40].

2.2 Gate engineered DG MOSFETs

Gate engineering of the MOSFET means, the total gate material of the MOSFET is engineered or divided into two materials or three materials. If the total material length is the combination of two different materials having different metal work function, then the MOSFET structure is known as dual material gate (DMG) MOSFET structure. Similarly, if the total gate material length is the combination of three different materials having different metal work function, then the MOSFET structure is known as triple material gate (TMG) MOSFET structure. In double gate structure the gate engineering technique is applied both the top and the bottom gate. For two metals the structure is known as dual material double gate (DMDG) MOSFET and for three materials the structure is known as triple material double gate (TMDG) MOSFET.

The technique of Gate engineering such as dual metal gate (DMG) MOSFET has been anticipated in which the structure has two gates with different work functions [8-13].DMG MOSFET, in which two dissimilar materials having different work functions are combined together to shape a single gate of a bulk MOSFET. In the DMG structure, the work function of the gate material (M1) close to source is chosen higher than the one close to drain end (M2) for n-channel MOSFETs. As a result, the electron velocity and electric field along the channel abruptly increases near the boundary of the two gate materials which results in improved gate transport efficiency. This shows that the threshold voltage under gate material M1 is higher than that of under gate material M2.When the drain voltage exceeds the drain saturation voltage, the excess voltage is absorbed by gate metal M2 preventing the drain field from penetrating into the channel. This step potential is thus responsible for lower sub

threshold leakage current, reduced DIBL effects and increased output resistance in DMG MOSFETS. This so called gate work-function engineering allows the DMG devices to have same threshold voltage for a reduced doping concentration in the channel region, resulting in better immunity to mobility degradation and hence higher transconductance [41].

2.3 Advantages of DG MOSFETs

i. reduction of ioff.
ii. undoped channel eliminates intrinsic
iii. parameter fluctuations and minimizes
iv. impurity scattering.
v. double gate allows for higher current drive capability
vi. better control of short channel effects.

2.4 Challenges of DG MOSFETs

i. Control of threshold voltage.
ii. Fabrication of the DG-FET is difficult.
iii. Alignment of both gates is hard to achieve,
iv. Misaligned gates result in extra capacitance and loss of current drive.

2.5 Gate misalignment of DG MOSFETs

Misalignment between top and bottom Gate of the DG MOSFETs are the most common possibility during fabrication. Because of misalignment some part of the channel has only one gate and behaves as a single gate conventional bulk MOSFET. Furthermore due to the absent of electric field, the electrostatic control over the gate reduces and the channel resistance increases, therefore drive current decreases. The misalignment can be happened either side of the device; i.e. drain side or source side. If the gate shifted towards source side then it is called as drain side misalignment (DSM) and if the gate shifted towards drain side then it is called as source side misalignment (SSM). The amount of length shifted either side called as misalignment length m_a.

2.6 Effect of misalignment: past works

The VLSI industry has been developing by leaps and bounds in the past few decades since its inception and it is solely credited to the continuous dimensional scaling of MOSFETs. The most straightforward advantages of MOSFET scaling are higher packing density, low dynamic power dissipation and improvement of speed [42]. Further, the stringent down scaling of complementary metal-oxide-semiconductor (CMOS) technology are highly responsible for the radio frequency (RF) performance metrics such as cut-off frequency, maximum oscillation frequency, and minimum noise figure [43]. On the other hand, the rigorous scaling of conventional bulk MOSFETs has given rise to many maligning problems, such as reduced gate control over the channel leading to drain induced barrier lowering (DIBL) and increasing short-channel effects (SCEs) such as threshold voltage roll-off and subthreshold swing. The SCEs lead to increase in off state leakage current thereby degrading I_{on}/I_{off} ratio, which results in a severe trade-off between the circuit speed and the stand-by power [44]. Therefore, the elimination of SCEs, while MOSFET scaling is of utmost concern.

To diminish the deleterious presence of SCEs, some of the most effective ways are reduction of gate oxide thickness (t_{ox}) which increases gate capacitance and improves the electrostatic control of the gate over the channel and an increase of the channel doping concentration (N_a) which minimizes the junction electric field entering into the channel region [45]. As the scaling has reached its limit, it is no longer suitable to decrease the gate oxide thickness and increasing channel doping. Because the thin gate oxide causes tunnelling of carriers from channel to gate which increases the stand-by power and degrades the device performance severely [46], whereas higher channel doping (N_a) results in mobility degradation [47,48], and fluctuation in threshold voltage [49,50,51].

Double-Gate (DG) MOSFET structure, a non-classical CMOS, overcomes these obstacles competently [52]. However, below channel length of $100\,\text{nm}$, the DG MOSFET structure with some modification is required to lessen the drain control on device characteristics [43]. Among various techniques, being employed in the DG MOSFETs, gate engineering is the most promising technique in which the gate is made up of two different metals of different work function, commonly known as Double-Material Gate (DMG) structure [53,54,55]. In this structure, the two gate metals are such that the work-function of the metal gate near the source (M_1) is higher than that of the drain side metal (M_2). The discontinuity in the work-

functions results in a step-like surface potential profile below the metal interface ensuring the screening of the minimum surface potential from the drain voltage variations. The metal gate M_2 is thus rightfully known as the *Screen Gate* and the metal M_1 as the *Control Gate*.

Reddy *et al.* [55] adopted this technique to propose double-material double-gate (DMDG) MOSFETs for achieving the benefits of both DG and DMG structures. The observable advantages in this structure are the decrease in peak electric field near the drain-body junction, increase in drain breakdown voltage, reduction in drain conductance, improvement in transconductance and threshold voltage roll-up.

Razavi *et al.* [56] further confirmed the superiority of the triple-material double gate (TMDG) MOSFET over the DMDG MOSFET structure in terms of both short-channel effects and hot-carrier effects. A triple-material gate structure provides further improvement as it possesses two step-shapes in the surface potential profile to screen the effect of the drain on device channel in a much efficient way. The simulation results show that the SCEs such as drain-induced barrier lowering (DIBL), hot-carrier effects (HCE) and channel length modulation (CLM) decreases significantly as compared with single-material double gate (SMDG) and DMDG counterparts. Later on, Tiwari *et al.* [57] reported that a better HCEs, increased barrier height and reduced threshold voltage roll-off can be achieved in TMDG structure compared to DMDG structure.

Although gate engineered DG MOSFETs are believed to spearhead the sub-100 nm regime of MOS technology, yet an inherent difficulty lies in aligning the front gate over the back gate during fabrication. Further, the problems related to the gate misalignment become more severe with DMDG and TMDG MOSFET structures owing to a possible process variation. The misalignment produces gate to source/drain overlap capacitance and results in loss of current drive [58]. The deteriorated performance of the MOSFETs gets reflected in terms of higher threshold voltage roll-off, lower drain current and lower transconductance. The problem of misalignment, thus, has been studied widely and reported in the conventional as well as the double material DG MOSFETs.

In 2003, Wong *et al.* [59] studied the effects gate misalignment of the subthreshold characteristics of sub-100nm DG-MOSFETs. They confirm that gates alignment in DG-MOSFETs becomes more and more difficult as devices are scaling down in non-self-aligned double gate processes. The results show that gate misalignment effects are not as serious as

generally expected and 60 to 80% misalignment is considered to be tolerable in some circuit applications.

For the first time in 2004, E. C. Sun and J. B. Kuo [60] analysed the gate misalignment effect on the threshold voltage of double-gate ultrathin fully depleted silicon-on-insulator nMOS devices using a compact modelling. They also consider the fringing electric field effect to predict the accurate behaviour of the threshold voltage.

In 2005, C. Yin and C. H. Chan [61] investigated the Source/Drain Asymmetric Effects Due to Gate Misalignment in Planar Double-Gate MOSFETs both by experimental data and simulation results. They found that, the overlap region at drain side can reduces DIBL, while the overlap region at source side decreases drain side capacitance and gate leakage current. They also confirm that the circuit will works without any degradation with a optimal misalignment length of 20% of total gate length.

In 2008, A. Kranti and G. A. Armstrong [62] studied in his research that, 25% back gate misalignment can be tolerated without any significant degradation in cut-off frequency and intrinsic voltage gain for ultra low voltage analog and radio frequency (RF) applications.

In 2009, Sharma *et al.* [63] analysed the gate misalignment effects on device characteristics for a dual material double gate SOI n-MOSFET. In this study the threshold voltage consistently increases as the source side misalignment increases and threshold voltage decreases for drain side misalignment. Furthermore, with the increase in misalignment length towards source side, drain current and transconductance consistently decrease, similar to SMDG devices, whereas for the drain side misalignment, it shows an ambiguous behaviour.

In 2012, Valin *et al.*[64] investigate the gate misalignment effects in a 10-nm double-gate SOI MOSFET with a 2-D Monte Carlo simulator, by accounting quantum effects. They found that an improvement of current, when the gate misalignment length is more in source side and reduction of channel control when drain side misalignment is more.

When misalignment creeps into the TMDG structure, advance knowledge of the effects and their severity on the threshold voltage, drain current, transconductance and other device parameter become a prerequisite to the fabrication. This thesis presents a detailed analysis of the same for various amounts of misalignment at the source and the drain end. Besides this,

different parameters of TMDG MOSFET structures are also compared with respective counterparts of DMDG and SMDG.

Chapter 3

3 SIMULATION METHODOLOGY

3.1 Introduction

Mostly for device simulation purpose atlas device simulator are used. ATLAS is a very powerful tool gives common capabilities for physically-based two (2D) and three-dimensional (3D) simulation of semiconductor devices. ATLAS is intended to be used in conjunction with the vwf interactive tools.The vwf interactive tools, which include DECKBUILD, TONYPLOT, DEVEDIT, MASKVIEWS, and OPTIMIZER.

3.2 Structure Definition

The structure of a device can be defined in three different ways for use in ATLAS.

I. The first type is to read an existing structure from a file. The structure is created either by an earlier ATLAS run or another program such as ATHENA or DEVEDIT. A MESH statement loads in the mesh, geometry, electrode positions, and doping of the structure. For example:

   MESH INFILE=<filename>

II. The second type is to use the **Automatic Interface** feature from DECKBUILD to transfer the input structure from ATHENA or DEVEDIT.

III. The third way is create a structure by using the ATLAS command language.

3.2.1 Using The Command Language To Define A Structure

Steps to define a device through the ATLAS command language

I. The first step is a mesh definition, in which the mesh or grid covers all the physical simulation area.

II. The mesh is specified by a series of horizontal and vertical lines and the spacing between them.

III. Regions within the mesh are assigned to different materials as required to construct the device. For example, the specification of a MOS device requires the specification of silicon and silicon dioxide regions.

IV. After the regions are defined, the location of electrodes is specified.

V. The final step is to specify the doping in each region.

To define a structure using command language, the following four sub-sections must be specified in the proper sequence as listed.

Specifying the initial mesh

There are three statements for specifying a initial mesh:

I. Mesh statement

To specify a mesh the first statement must be:

MESH SPACE.MULT=<VALUE>

This is followed by a series of X.MESH and Y.MESH statements.

X.MESH LOCATION=<VALUE> SPACING=<VALUE>

Y.MESH LOCATION=<VALUE> SPACING=<VALUE>

The SPACE.MULT parameter value is used as a scaling factor for the mesh created by the X.MESH and Y.MESH statements. The default value is 1. Values greater than 1 will create a globally coarser mesh for fast simulation. Values less than 1 will create a globally finer mesh for increased accuracy. The X.MESH and Y.MESH statements are used to define the locations in microns of vertical and horizontal lines, respectively, together with the vertical or horizontal spacing associated with that line.

II. Elimination statement

After completion of initial meshing, one can remove grid lines in specified regions. This is typically done in regions of the device where a coarse grid is expected to be enough such as the substrate. The elimination of grid lines is complete using the ELIMINATE statement. The ELIMINATE statement take away every second mesh line in the particular direction from within a specified rectangle. For example, the statement:

ELIMINATE COLUMNS X.MIN=0 X.MAX=4 Y.MIN=0.0 Y.MAX=3

Eliminates every second vertical grid line within the rectangle bounded by x=0, x=4, y=0 and y=3 microns.

III. Region statement

Once the mesh is specified, every part of it must be assigned a material type. This is done with REGION statements. For example:

REGION number=<integer> <material_type> <position parameters>

Region numbers must start at 1 and are increased for each subsequent region statement. Maximum 200 different regions can be defined in ATLAS. A large number of materials are existing. If a composition-dependent material type is specified, the x and y composition fractions can also be defined in the REGION statement.

IV. Position statement

The position parameters are specified in microns using the X.MIN, X.MAX, Y.MIN, and Y.MAX parameters. If the position parameters of a new statement overlap those of a previous REGION statement, the overlapped area is assigned as the material type of the new region.

Specifying Electrodes

Once the regions and materials have specified, at least one electrode should be define that will contacts a semiconductor material. This is accomplished with the ELECTRODE statement. For example:

ELECTRODE NAME=<electrode name> <position_parameters>

The maximum number of electrodes that can be specified is 50. More than one electrode statements may have the same electrode name. Nodes that are associated with the same electrode name are treated as being electrically connected.

Specifying Doping

For specifying the doping DOPING statement is used in ATLAS. For example:

DOPING <distribution_type> <dopant_type> <position_parameters>

Analytical Doping Profiles

Analytical doping profiles are two types; i.e uniform or Gaussian forms.

I. Uniform doping profile

The parameters defining the analytical distribution are specified in the DOPING statement

DOPING UNIFORM CONCENTRATION=1E16 N.TYPE REGION=1

The above doping statement gives a uniform n-type doping density of 10^{16} cm^{-3} in the region that was previously labelled as region #1. The position parameters: X.MIN, X.MAX, Y.MIN, and Y.MAX can be used instead of a region number.

II. Gaussian doping profile

The parameters defining the analytical distribution are specified in the DOPING statement

DOPING GAUSSIAN CONCENTRATION=1E18 CHARACTERISTIC=0.05 P.TYPE \
X.LEFT=0.0 X.RIGHT=1.0 PEAK=0.1

The above doping statement givesa a p-type Gaussian profile with a peak concentration of $10^{18}cm^{-3}$. This statement specifies that the peak doping is located along a line from x = 0 to x = 1 microns. If a Gaussian profile is being added to an area that was already defined with the opposite dopant type, you can use the JUNCTION parameter to specify the position of the junction depth instead of specifying the standard deviation using the CHARACTERISTIC parameter

3.3 Defining material parameters and models

Once the mesh, geometry, and doping profiles are completed, one can change the characteristics of electrodes, change the default material parameters, and decide which physical models ATLAS will use during the device simulation. These behaviours are finished using the CONTACT, MATERIAL, and MODELS statements respectively. Impact ionization models can be enabled using the IMPACT statement. Interface properties are set by using the INTERFACE statement.

3.3.1 Specifying Contact Characteristics

Work function for Gates or Schottky Contacts

The contact between electrode and semiconductor material is assumed by default as ohmic. If a work function is specified, the electrode behaves as a Schottky contact. The CONTACT statement is used to define the metal work function of one or more electrodes. The NAME parameter is used to identify which electrode will have its properties modified.

The WORKFUNCTION parameter sets the work function of the electrode. For example, the statement:

CONTACT NAME=gate WORKFUNCTION=4.8

The work function of the gate electrode sets to 4.8eV. The work functions of several commonly used contact materials may be specified using the name of the material. Work functions for ALUMINUM, N.POLYSILICON, P.POLYSILICON, TUNGSTEN, and TU.DISILICIDE can be specified in this way. The following statement sets the work function for an n-type polysilicon gate contact.

CONTACT NAME=gate N.POLYSILICON

The CONTACT statement can also be used to define barrier and dipole lowering of the Schottky barrier height. Barrier lowering is enabled by specifying the BARRIER parameter, while dipole lowering is specified using the ALPHA parameter. For example, the statement:

CONTACT NAME=anode WORKFUNCTION=4.9 BARRIER ALPHA=1.0e-7

The work function of anode Schottky contact sets to 4.9eV enables barrier lowering and fixes coefficient of the dipole lowering to 1 nm.

Setting Current Boundary Conditions

To alter an electrode from voltage control to current control, CONTACT statement is also used. For simulating devices Current controlled electrodes are useful, where the current is highly responsive to voltage.

The statement for current boundary conditions is:

CONTACT NAME=drain CURRENT

Here, changes the drain electrode to current control. The NEWTON or BLOCK solution methods are necessary for all simulations with a current boundary condition.

Defining External Resistors, Capacitors, or Inductors

Lumped resistance, capacitance, and inductance connected to an electrode can be specified using the RESISTANCE, CAPACITANCE, and INDUCTANCE parameters in the CONTACT statement. For example, the statement:

CONTACT NAME=drain RESISTANCE=50.0 CAPACITANCE=20e-12 INDUCTANCE=1e-6

The above statement specifies a parallel resistor and capacitor of 50 ohms and 20 pF respectively in series with a 1 μH inductor. Note that in 2D simulations, these passive element values are scaled by the width in the third dimension. Since in 2D ATLAS assumes a 1μm width, the resistance becomes 50 Ω-μm.

Distributed contact resistance for an electrode can be specified using the CON.RESIST parameter. For example, the statement:

CONTACT NAME=source CON.RESISTANCE=0.01

The above statement specifies that the source contact has a distributed resistance of 0.01 Ωcm^2.

Floating Contacts

For specifying a floating electrode the CONTACT statement is also used. There are completely two different situations where floating electrodes are significant. The first condition is for floating gate electrodes used in EEPROM and other programmable devices. The second condition is the contacts with the semiconductor materials such as floating field plates in high power devices.

Floating gates are enabled by defining the parameter FLOATING on the CONTACT statement. For example, the statement:

CONTACT NAME=fgate FLOATING

The above statement gives that the electrode named fgate will be floating and that charge boundary conditions will apply.

For direct contacts to the semiconductor, the FLOATING parameter cannot be used. This type of floating electrode is best simulated by defining current boundary conditions on the CONTACT statement. For example, the statement:

CONTACT NAME=drain CURRENT

The above statement gives current boundary conditions for the electrode named drain. On subsequent SOLVE statements, the drain current boundary condition will default to zero current, therefore floating the contact.

Shorting Two Contacts Together

It is feasible in ATLAS to short two or more contact together so that voltages on both contacts are same. This is useful for many technologies for example dual gate MOSFETs. There are some methods for achieving this depending on how the structure was originally defined.

If the structure is specified using ATLAS syntax, one can have number of ELECTRODE statements with the same NAME parameter specifying different locations inside the device structure. In this case, the areas specified to be electrodes will be considered as having the similar applied voltage. A single current will come into view combining the current through both ELECTRODE areas.

Making an Open Circuit Contact

It is often necessary to carry out a simulation with an open circuit on one of the specified electrodes. There are three distinct methods to create an open circuit contact.

I. The first means is to totally removing an electrode from the structure file.
II. The second way is to add an tremendously large lumped resistance. For example, 2000 Ω onto the contact to be made open circuit.
III. The third means is to switch the boundary conditions on the contact to be creating open circuit from voltage controlled to current controlled and then defining a very negligible current through that electrode.

The above methods are possible but if a floating region is generated within the structure, then numerical convergence may have some problem. So the second method is better because it gives better convergence.

3.3.2 Specifying Material Properties

Semiconductor, Insulator, or Conductor

All materials are divided into three classes: semiconductors, insulators and conductors. Each class requires a distinct set of parameters to be defined. For semiconductors, these properties include band gap, electron affinity, saturation velocities and density of states. There are the general parameters used in simulations of devices for many materials.

Setting Parameters

The MATERIAL statement permits to specify user defined values for these general parameters. For example, the statement:

MATERIAL MATERIAL=Silicon EG300=1.12 MUN=1100

The above statement gives the band gap value of 1.12 eV and low field electron mobility of 1100 cm^2/v-s in all silicon regions in the device. If the material properties are defined by region, the region is specified using the REGION or NAME parameters in the MATERIAL statement. For example, the statement:

MATERIAL REGION=2 TAUN0=2e-7 TAUP0=1e-5

The above statement gives the electron and hole Shockley-Read-Hall recombination lifetimes for region number two. If the name, base, has been specified using the NAME parameter in the REGION statement, then the statement:

MATERIAL NAME=base NC300=3e19

The above statement gives the conduction band density of states at 300 K for the region named base.

Heterojunction Materials

The heterojunction material properties can also be customized with the MATERIAL statement. In addition to the usual material parameters, composition dependent material parameters can be specified. These include composition dependent band parameters, dielectric constants, saturation velocities, and so on.

For heterojunction material systems, the bandgap difference between the materials is divided between conduction and valence bands. The ALIGN parameter specifies the fraction of this difference that is applied to the conduction band edge. This determines the electron and hole barrier height and overrides any electron affinity specification. For example, the statement:

MATERIAL MATERIAL=InGaAs ALIGN=0.35

MATERIAL MATERIAL=InP ALIGN=0.35

The above statement specifies that 35% of the band gap difference between InGaAs and InP is given to the conduction band and 65% is given to the valence band. For example, if the

band gap difference (Eg) for this material system is 0.6 eV, then the conduction band barrier height is 0.210 eV and the valence band barrier height is 0.390 eV.

Specifying Interface Properties

The statement for INTERFACE is used to specify the interface charge density and surface recombination velocity at interfaces between semiconductors and insulators. For example, the statement:

INTERFACE QF=3e10

Give that all interfaces between semiconductors and insulators have a fixed charge of $3x10^{10}cm^{-2}$. In many cases, the interested interface is limited to a specific region. This can be done with the X.MIN, X.MAX, Y.MIN, and Y.MAX parameters on the INTERFACE statement. These parameters specify a rectangle, where the interface properties be valid. For example, the statement:

INTERFACE QF=3e10 X.MIN=1.0 X.MAX=2 Y.MIN=0.0 Y.MAX=0.5

limits the interface charge to the semiconductor-insulator boundary within the specified rectangle. In addition to fixed charge, surface recombination velocity and thermionic emission are enabled and defined with the INTERFACE statement.

Chapter 4

4 DEVICE STRUCTURE & SIMULATION

4.1 The Device Structure

Figures 4.1 and 4.2 show the cross sectional view of the TMDG MOSFETs with drain side misalignment (DSM) and source side misalignment (SSM). The channel is assumed to be fully depleted (FD) at channel doping of N_a cm^{-3}, and the drain/source doping is N_d cm^{-3}. The channel length is L and misalignment length is m_a in either source or drain side. The silicon film of thickness t_{si} forms a sandwiched structure between the thin oxide (SiO_2) layers with a thickness of t_{ox}. M_1, M_2 and M_3 form the metal trio with decreasing order of work-function towards the drain terminal. Here, M_2 and M_3 form the screening gate whereas the M_1 serves as the control gate. The lengths of control gate and screen gates are L_1, L_2 and L_3 respectively and thus the total channel length is $L = L_1 + L_2 + L_3$. The source terminal is grounded and the gate and drain voltages are fixed at V_{gs} and V_{ds} respectively.

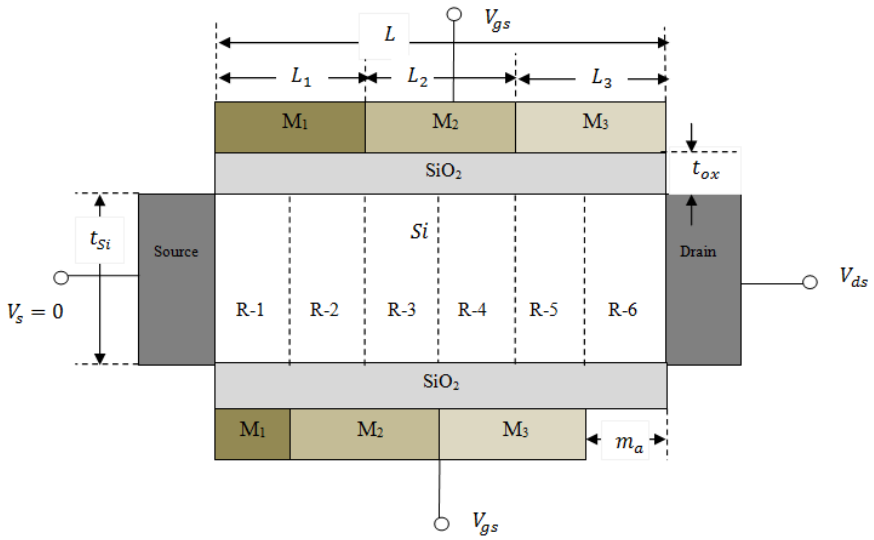

Figure 4.1.1: A schematic view of the TMDG MOSFET structure with drain side misalignment Length of control gate, first screen gate and second screen gate are taken as L_1, L_2 and L_3 respectively. t_{si} and t_{ox} are silicon channel thickness and gate oxide thickness respectively. m_a is the misalignment length between front and back gate at the drain end.

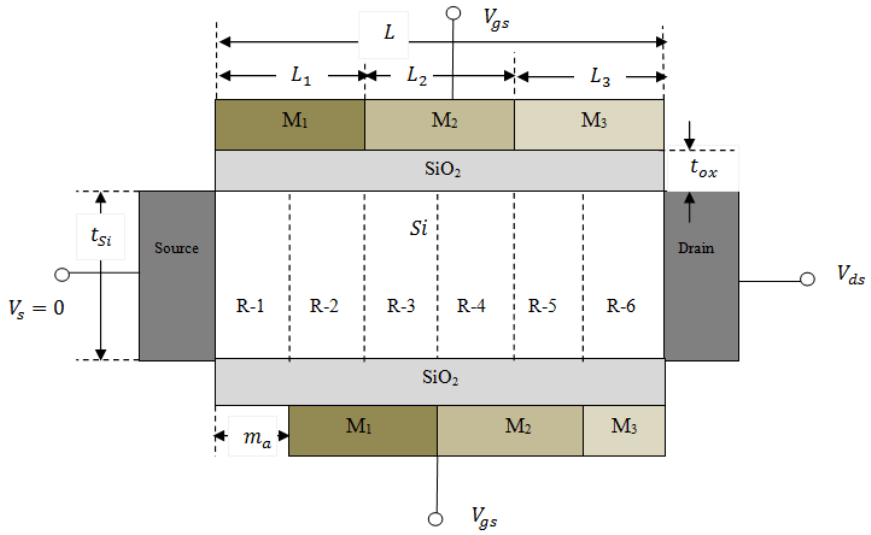

Figure 4.1.2: A schematic view of the TMDG MOSFET structure with source side misalignment Length of control gate, first screen gate and second screen gate are taken as L_1, L_2 and L_3 respectively. t_{si} and t_{ox} are silicon channel thickness and gate oxide thickness respectively. m_a is the misalignment length between front and back gate at the source end.

4.2 Model used for simulation

The numerical simulations have been carried out by a two-dimensional (2D) device simulator ATLAS^{TM} from Silvaco Int. [65], for obtaining surface potential profile and other device characteristics. The drift-diffusion model has been employed during simulation. For velocity saturation in high field, FLDMOB mobility model has been used in which the velocity saturation depends on the parallel electric field in the direction of current flow. Moreover, the CVT mobility model has also been used as it is a complete mobility model in which the mobility depends on doping density, temperature, parallel electric field and vertical electric field. The FERMI carrier statistical model is used to reduce carrier concentrations in heavily doped regions. The threshold voltage is calculated from drain-current gate-voltage curve by assuming the value of gate voltage for drain current, $I_d = \frac{W}{L} \times 10^{-7}$ A/μm (where, W and L are channel width and length respectively) [24]. DIBL is calculated as the difference of higher and lower threshold voltage upon difference of higher and lower drain voltages [21]. The source-body and the drain-body junctions are abrupt in nature. For SMDG MOSFET, the taken metal work-function of the front and back gates is $\phi_{M1} = 4.8\,\text{eV}$ (Au: Gold). DMDG MOSFET has metal work functions $\phi_{M1} = 4.8\,\text{eV}$ (Au: Gold) and $\phi_{M2} = 4.6\,\text{eV}$ (Mo: Molybdenum) for control and screen gates respectively. The TMDG MOSFET consists of

three different gates namely control gate, screen gate-1 and screen gate-2 with metal work functions $\phi_{M1} = 4.8\,\text{eV}$ (Au: Gold), $\phi_{M2} = 4.6\,\text{eV}$ (Mo: Molybdenum) and $\phi_{M3} = 4.4\,\text{eV}$ (W: Tungsten) respectively. The values of other parameters utilized in the simulation are mentioned in Table 4.2.1.

Table 4.2.1: Device parameters used for simulation

Parameters	**Value**
Source /Drain doping (N_d)	$10^{20}\,\text{cm}^{-3}$
Channel doping (N_a)	$10^{16}\,\text{cm}^{-3}$
Oxide thickness (t_{ox})	$2\,\text{nm}$
Channel Length (L)	$60\,\text{nm}$
Misalignment Length (m_a)	$0 - 30\,\text{nm}$
Silicon film thickness (t_{si})	$10\,\text{nm}$
Gate Metal work-function (M_1)	$4.8\,\text{eV}$
Gate Metal work-function (M_2)	$4.6\,\text{eV}$
Gate Metal work-function (M_3)	$4.4\,\text{eV}$

Chapter 5

5 RESULTS & DISCUSSIONS

5.1 Introduction

Here, all the simulation results and its discussion are briefly described. The effects of gate misalignment on device characteristics like, surface potential, threshold voltage, DIBL, subthreshold slope, subthreshold current, drain current, transconductance and output conductance have been analysed thoroughly.

5.2 Surface potential

Potential distributions along the channel length are plotted at both front and back Si/SiO_2 interfaces, named as front and back surface potential, respectively. Considering SSM and DSM with misalignment lengths of 10 nm, 20 nm and 30 nm, both front and back surface potentials for SMDG, DMDG and TMDG structures are shown in Figs. 3-8. In SMDG MOSFET case, the total channel length is divided into two regions due to misalignment named as region-1 (R-1) and region-2 (R-2). While considering DSM, the R-1 is called as a gate overlapped region, and contains both front gate and back gate with a work- function of 4.8eV, and the R-2 called as non-gate overlap region contains front gate with a work-function of 4.8 eV and back gate without any gate material. Similarly in the case of SSM, R-1 contains front gate with a work-function of 4.8 eV and back gate with absence of gate material whereas R-2 contains both front and back gates with a work-function of 4.8 eV . Fig. 3 shows the back surface potential profile at different misalignment lengths which depicts that the source channel-barrier height associated with back $Si\text{-}SiO_2$ interface increases with higher value of misalignment length for both SSM and DSM cases. This may be attributed to the absence of gate electric field, reduced electrostatic control and increase of series resistance in the non-overlapped gate region. Fig. 4 shows the front surface potential profile of SMDG structure with misalignment lengths of 10 nm, 20 nm and 30 nm. Though there is no region in the front gate, uncovered by gate metal, yet the source-channel barrier height along the front $Si\text{-}SiO_2$ interface increases with higher gate misalignment lengths. This is because in misalignment region the MOSFET is no longer a DG MOSFET, and it behaves as a simple thick film single gate bulk MOSFET requiring larger voltage for the channel

inversion. Comparison of Figs. 5.2.1 and 5.2.2 reveals that due to misalignment between front and back gates, SMDG MOSFET becomes asymmetric and both front and back surfaces have different threshold voltage. It is also found that the threshold voltage of SMDG MOSFET increases with increasing misalignment length. However, this threshold voltage may be associated with either front or back surface depending upon the fact that which surface is having higher source-channel barrier height.

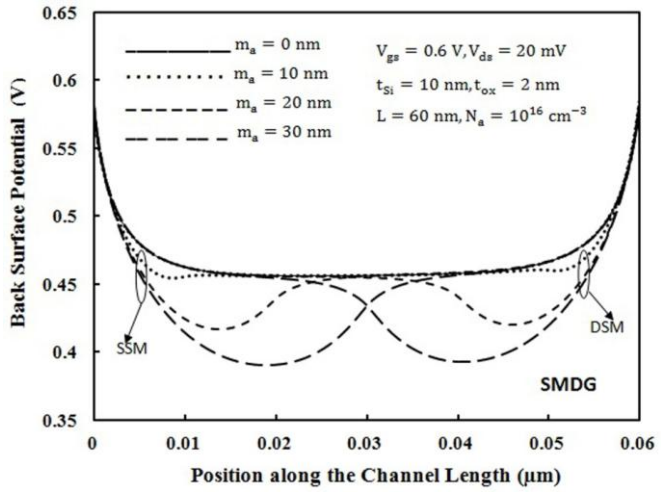

Figure 5.2.1: Variation of back surface potential with lateral direction of SMDG ($\phi_{M1} = 4.8\,\text{eV}$) MOSFET structure.

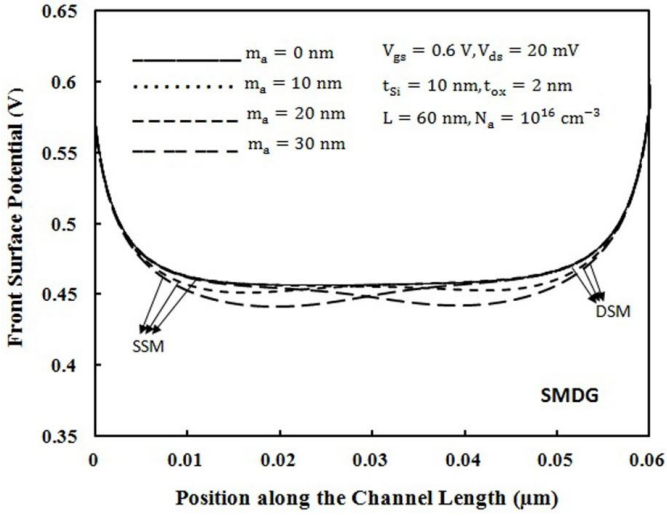

Figure 5.2.2: Variation of front surface potential with lateral direction of SMDG ($\phi_{M1} = 4.8\,\text{eV}$) MOSFET structure.

For the analysis of the DMDG MOSFET, the whole channel region is divided into four different regions named as R-1, R-2, R-3 and R-4 as illustrated in Table 5.2.1. The variation

of the back and front surface potential profile along the channel length direction in different regions are shown in Figs. 5.2.1 and 5.2.2 respectively. Table 5.2.2 manifests in detail the minimum surface potential and the position of the minimum surface potential for different misalignment cases which are shown in Figs. 5.2.3 and 5.2.4. It is also being revealed from Table III that the source-channel barrier height is under control of either front or back gate of DMDG MOSFET.

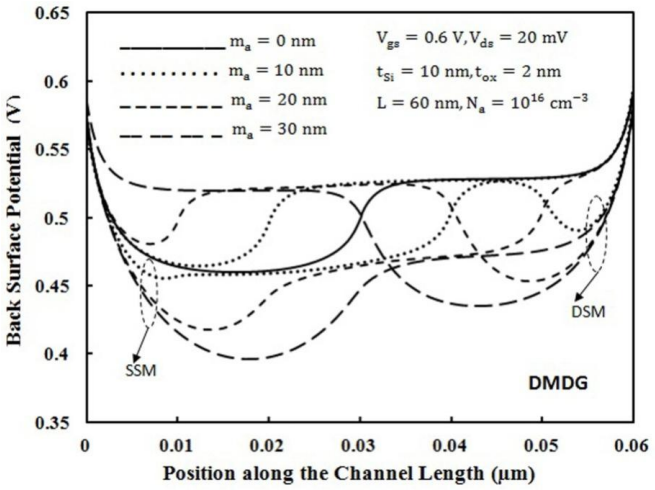

Figure 5.2.3: Variation of back surface potential with lateral direction of DMDG ($\phi_{M1} = 4.8\,\text{eV}$, $\phi_{M2} = 4.6\,\text{eV}$) MOSFET structure ($L_1 : L_2 = 1:1$).

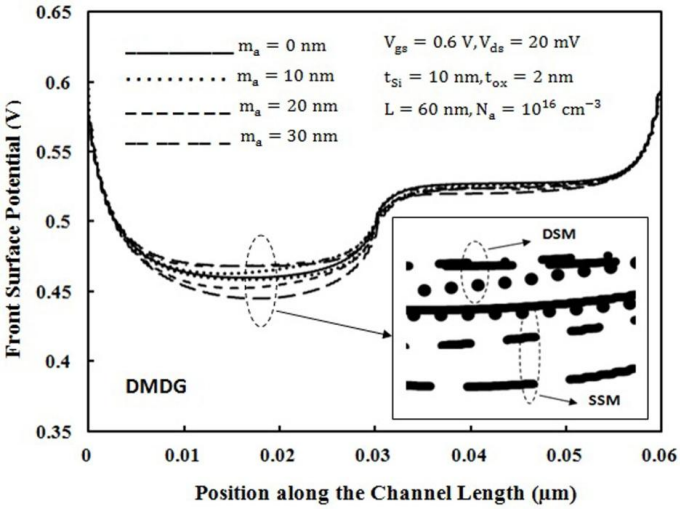

Figure 5.2.4: Variation of front surface potential with lateral direction of DMDG ($\phi_{M1} = 4.8\,\text{eV}$, $\phi_{M2} = 4.6\,\text{eV}$) MOSFET structure ($L_1 : L_2 = 1:1$).

Table 5.2.1: Region wise length of the channel and combinations of front-back gate metal work-functions at different misalignment lengths for DMDG MOSFET

Misalignment length (m_a)	Gate	Metal Work-function (eV) at Source Side Misalignment (SSM)				Metal Work-function (eV) at Drain Side Misalignment (DSM)			
		R-1[a]	R-2[b]	R-3[c]	R-4[d]	R-1[a]	R-2[b]	R-3[c]	R-4[d]
00 nm	Front	4.8	4.8	4.6	4.6	4.8	4.8	4.6	4.6
	Back	4.8	4.8	4.6	4.6	4.8	4.8	4.6	4.6
	Length (nm)	0-15	15-30	30-45	45-60	0-15	15-30	30-45	45-60
10 nm	Front	4.8	4.8	4.6	4.6	4.8	4.8	4.6	4.6
	Back	----	4.8	4.8	4.6	4.8	4.6	4.6	----
	Length (nm)	0-10	10-30	30-40	40-60	0-20	20-30	30-50	50-60
20 nm	Front	4.8	4.8	4.6	4.6	4.8	4.8	4.6	4.6
	Back	----	4.8	4.8	4.6	4.8	4.6	4.6	----
	Length (nm)	0-20	20-30	30-50	50-60	0-10	10-30	30-40	40-60
30 nm	Front	4.8	4.8	4.6	4.6	4.8	4.8	4.6	4.6
	Back	----	----	4.8	4.8	4.6	4.6	----	----
	Length (nm)	0-30	30-30	30-60	60-60	0-0	0-30	30-30	30-60

[a]Region 1, [b]Region 2, [c]Region 3, [d]Region 4

Table 5.2.2: Minimum surface potential, gate and region responsible for threshold voltage of DMDG MOSFET at different misalignment length

Misalignment Length (m_a)	Source Side Misalignment (SSM)			Drain Side Misalignment (DSM)		
	Min. Surface Potential Responsible for V_t[a]	Gate	Region	Min. Surface Potential Responsible for V_t[a]	Gate	Region
00 nm	0.45953 V	Any	R-2[b]	0.45953 V	Any	R-2[b]
10 nm	0.45857 V	Front	R-2[b]	0.46395 V	Back	R-2[b]
20 nm	0.45252 V	Front	R-1[c]	0.46796 V	Front	R-1[c]
30 nm	0.44513 V	Front	R-1[c]	0.46798 V	Front	R-1[c]

[a]Threshold voltage, [b]Region 2, [c]Region 1

Figures 5.2.5 and 5.2.6 show the back and front surface potential respectively, along the channel length direction for TMDG MOSFET structure with different misalignment cases. In this case, the total channel length is divided into six different regions from R-1 to R-6. Table IV gives the description about the misalignment length, number of regions, region length and region wise front and back gate material combinations. The conclusions drawn from Figs. 7 and 8 are summarized in Table V. Table V gives the detailed information about the minimum surface potential responsible for threshold voltage of TMDG MOSFET. It also informs about the position of minimum surface potential and the gate which is controlling the minimum surface potential.

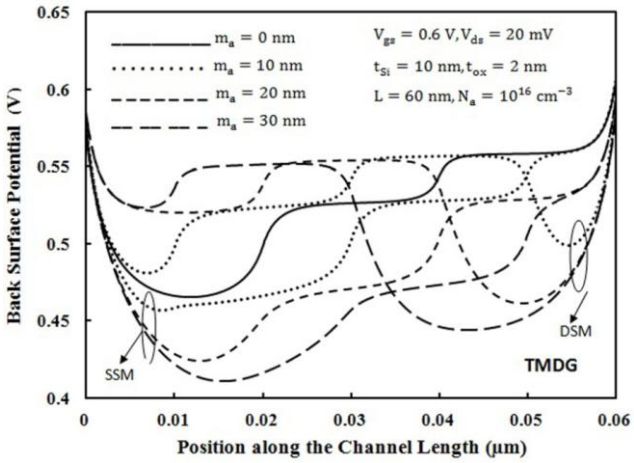

Figure 5.2.5: Variation of back surface potential with lateral direction of TMDG ($\phi_{M1} = 4.8\,\text{eV}$, $\phi_{M2} = 4.6\,\text{eV}$, $\phi_{M3} = 4.4\,\text{eV}$) MOSFET structure ($L_1 : L_2 : L_3 = 1:1:1$).

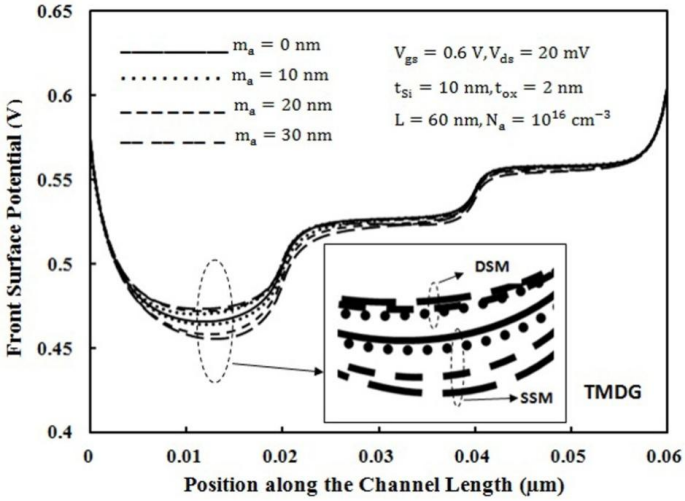

Figure 5.2.6: Variation of front surface potential with lateral direction of TMDG ($\phi_{M1} = 4.8\,\text{eV}$, $\phi_{M2} = 4.6\,\text{eV}$, $\phi_{M3} = 4.4\,\text{eV}$) MOSFET structure ($L_1 : L_2 : L_3 = 1:1:1$).

Table 5.2.3: Region wise front and back gate metal work-function combinations at different misalignment length for TMDG MOSFET structure

Misalignment length (m_a)	Gate	Metal Work-function (eV) at Source Side Misalignment (SSM)						Metal Work-function (eV) at Drain Side Misalignment (DSM)					
		R-1[a]	R-2[b]	R-3[c]	R-4[d]	R-5[e]	R-6[f]	R-1[a]	R-2[b]	R-3[c]	R-4[d]	R-5[e]	R-6[f]
00 nm	Front	4.8	4.8	4.6	4.6	4.4	4.4	4.8	4.8	4.6	4.6	4.4	4.4
	Back	4.8	4.8	4.6	4.6	4.4	4.4	4.8	4.8	4.6	4.6	4.4	4.4
10 nm	Front	4.8	4.8	4.6	4.6	4.4	4.4	4.8	4.8	4.6	4.6	4.4	4.4
	Back	----	4.8	4.8	4.6	4.6	4.4	4.8	4.6	4.6	4.4	4.4	----
20 nm	Front	4.8	4.8	4.6	4.6	4.4	4.4	4.8	4.8	4.6	4.6	4.4	4.4
	Back	----	----	4.8	4.8	4.6	4.6	4.6	4.6	4.4	4.4	----	----
30 nm	Front	4.8	4.8	4.6	4.6	4.4	4.4	4.8	4.8	4.6	4.6	4.4	4.4
	Back	----	----	----	4.8	4.8	4.6	4.6	4.4	4.4	----	----	----

[a]Region 1 (0-10 nm), [b]Region 2 (10-20 nm), [c]Region 3 (20-30 nm), [d]Region 4 (30-40 nm), [e]Region 5 (40-50 nm), [f]Region 6 (50-60 nm),

Table 5.2.4:The minimum surface potential responsible for threshold voltage of TMDG MOSFET at different misalignment length with the deciding gate and region

Misalignment Length (m_a)	Source Side Misalignment (SSM)			Drain Side Misalignment (DSM)		
	Min. Surface Potential Responsible for $V_t{}^a$	Gate responsible for $V_t{}^a$ determination	Minimum surface potential region	Min. Surface Potential Responsible for $V_t{}^a$	Gate responsible for $V_t{}^a$ determination	Minimum surface potential region
00 nm	0.46547 V	Any	R-2[b]	0.46547 V	Any	R-2[b]
10 nm	0.46350 V	Front	R-2[b]	0.48074 V	Back	R-1[c]
20 nm	0.45832 V	Front	R-2[b]	0.47149 V	Front	R-2[b]
30 nm	0.45521 V	Front	R-2[b]	0.47284 V	Front	R-2[b]

[a]Threshold voltage, [b]Region 2, [c]Region 1

5.3 Threshold voltage

The threshold voltage of a DG MOSFET is defined as the gate voltage when the electron densities in the front or the back channel, formed near front or back Si/SiO_2 interfaces, respectively, equals the doping density of the channel. It should be noted that the minima of front or back surface potential determines the threshold voltage of DG MOSFET. If minimum of front surface potential is more than that of back surface potential, the threshold voltage of DG MOSFET is determined by front channel and vice versa. In Fig. 5.3.1, threshold variation is shown against the gate misalignment for SMDG, DMDG and TMDG structures while taken value of drain to source voltage is $V_{ds} = 0.1\text{V}$. From Fig. 5.3.1, it is observed that without misalignment the SMDG MOSFET structure possesses the maximum threshold voltage compared with DMDG and TMDG MOSFETs. In SMDG MOSFET structure, the threshold voltage is almost constant as the misalignment increases at either ends. This may be attributed to the least variation of minimum front surface potential as shown in Fig. 5.2.2. The threshold voltage variation against gate misalignment in DMDG and TMDG structures gets complicated compared to the SMDG due to the various combinations of front and back gate materials. When misalignment occurs in a DMDG MOSFET [21], the device performance can be explained by dividing the channel into four different regions as discussed earlier. These regions can be regarded as four different devices connected in series, and the overall threshold voltage of the device is governed by the device with the maximum threshold voltage. While considering SSM, the threshold voltage is found to be increased as the misalignment increases. This is because the minimum front surface potential is always more than that of minimum back surface potential and hence source-channel barrier height corresponding to front gate is lower which is instrumental in determining the threshold voltage of DMDG MOSFET device. However, in DMDG MOSFET, threshold voltage decreases severely with drain side misalignment. In TMDG structure, the analysis of threshold voltage is same as that of DMDG structure. With gate misalignment, the minima of surface potential may occupy any region and accordingly threshold voltage of the device will be determined. Even in TMDG MOSFET, the threshold voltage is almost insensitive with source side misalignment. However, the threshold voltage is decreasing severely with the DSM and this degradation is more severe compared to the DMDG MOSFET case for the same channel length. This may be attributed to the more SCE which inherently comes in TMDG MOSFET structure. Fig. 5.3.2 shows the threshold voltage

of SMDG, DMDG, and TMDG structure at $V_{ds} = 1\text{V}$. Here the threshold voltage decreases with DSM for all three structures due to high drain to source voltage applied to the device. With SSM there are no significant variations in threshold voltage due to high drain to source voltage.

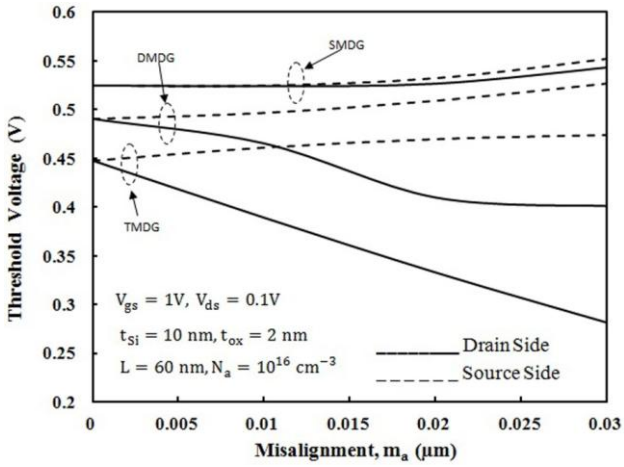

Figure 5.3.1: Threshold voltage variation with gate misalignment of SMDG ($\phi_{M1} = 4.8\text{ eV}$), DMDG ($\phi_{M1} = 4.8\text{ eV}, \phi_{M2} = 4.6\text{ eV}$), and TMDG ($\phi_{M1} = 4.8\text{ eV}, \phi 2 = 4.6\text{ eV}, \phi_{M3} = 4.4\text{ eV}$) MOSFET structures for $V_{ds} = 0.1\text{V}$

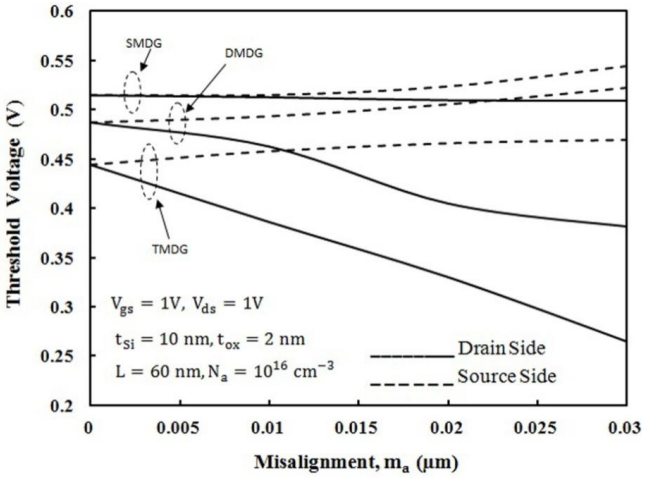

Figure 5.3.2: Threshold voltage variation with gate misalignment for SMDG ($\phi_{M1} = 4.8\text{ eV}$), DMDG ($\phi_{M1} = 4.8\text{ eV}, \phi_{M2} = 4.6\text{ eV}$) and TMDG ($\phi_{M1} = 4.8\text{ eV}, \phi_{M2} = 4.6\text{ eV}, \phi_{M3} = 4.4\text{ eV}$) MOSFET structures for $V_{ds} = 1\text{V}$

5.4 Drain induced barrier lowering (DIBL)

The short-channel effects in a MOSFET are mainly assumed to be comprised of DIBL, threshold voltage roll-off and subthreshold swing. DIBL is the most common short-channel

effect in MOSFETs specifying originally to a decrement of threshold voltage of the transistor at higher drain to source voltages. In a typical long channel planar field-effect transistor, the channel formation happens far enough from the drain contact that it is electro-statically shielded from the drain by the mixture of the substrate and gate, and so typically the threshold voltage was autonomous of drain voltage. When channel length of the device is small the drain is close enough to the source, and so a high drain voltage can open the bottleneck and turn on the transistor prematurely.

Barrier lowering enhances as channel length is decreased, even at zero applied drain-to-source bias, because the source and drain creates p-n junctions with the substrate, and so have related built-in depletion layers associated with them that become major partners in charge equilibrium at short channel lengths, even without any reverse bias given to enhance depletion widths.

Due to the reduction of channel length, the acts of DIBL in the subthreshold region (weak inversion) show up at first as a easy translation of the subthreshold current vs. gate bias plot with change in drain voltage, which can be modelled as a straightforward change in threshold voltage with drain bias. However, at smaller lengths the slope of the current vs. gate bias plot is decreased, that is, it wants a larger change in gate bias to effect the equal change in drain current. At very short lengths, the gate completely fails to turn off the device.

DIBL also harms the current vs. drain bias plot in the active mode, causing the current to enhance with drain bias, decreasing the MOSFET output resistance. This enhancememt is extra to the usual CLM effect on output resistance, and not possible to be modelled as a threshold adjustment.

In practice, DIBL can be calculated as follows:

$$DIBL = \frac{V_{Th}(high) - V_{Th}(low)}{V(high) - V(low)}$$

where $V_{Th}(high)$ is the threshold voltage measured at a supply voltage (the high drain voltage), and $V_{Th}(low)$ is the threshold voltage measured at a very low drain voltage, typically 0.05 V or 0.1 V. $V(high)$ is the supply voltage (the high drain voltage) and $V(low)$ is the low drain voltage (for a linear part of device I-V characteristics). Typical units of DIBL are mV/V.

Figure 5.4.1 shows the variation of DIBL with misalignment for SMDG, DMDG and TMDG structures. It is shown that DIBL variation is almost negligible with gate misalignment if the misalignment is taken at the source side. It is due to the fact that a minimum of surface potential is closer to the source side and drain has negligible control over the source channel barrier height. However, for drain side misalignment, TMDG MOSFET possesses the lowest DIBL compared to the DMDG and SMDG MOSFET structures. It is due to the fact that the TMDG MOSFET has two screen gates compared to the one screen gate of DMDG MOSFET and thus the minima of surface potential in TMDG MOSFET is screened effectively from the drain effects. Thus from Figs. 5.4.1 and 5.5.1, it may be concluded that SCE is more in TMDG MOSFET, and HCE is more in SMDG MOSFET and hence to optimize the performance of the DG MOS device, a trade-off must be made between SCEs and HCEs.

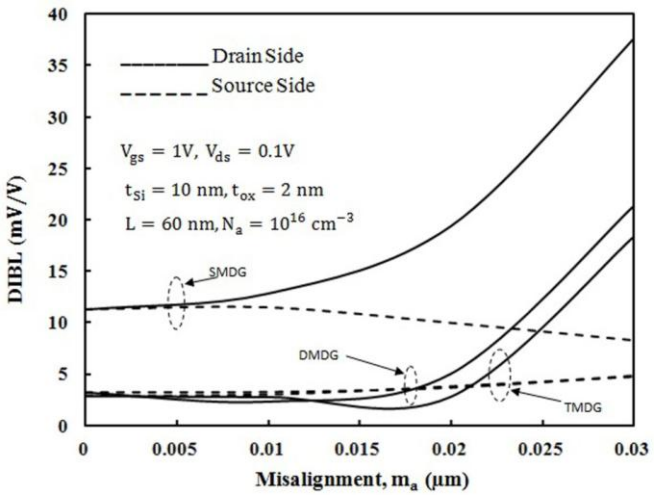

Figure 5.4.1: DIBL variation with gate misalignment of SMDG ($\phi_{M1} = 4.8$ eV), DMDG ($\phi_{M1} = 4.8$ eV , $\phi_{M2} = 4.6$ eV) and TMDG ($\phi_{M1} = 4.8$ eV , $\phi_{M2} = 4.6$ eV , $\phi_{M3} = 4.4$ eV) MOSFET structures.

5.5 Sub threshold slope

The sub threshold slope is a characteristic of a MOSFET's current-voltage plot. In the sub threshold region the drain current performance, though being controlled by the gate terminal - is analogous to the exponentially rising current of a forward biased diode. Hence a curve of logarithmic drain current versus gate voltage with drain, source, and bulk voltages constant will exhibit roughly linear behaviour in this MOSFET operating region. Its slope is known as sub threshold slope.

The sub threshold slope is strongly related to its reciprocal value called subthreshold swing S_{s-th} which is usually given as [66]:

$$S_{s-th} = \ln(10)\frac{kT}{q}\left(1+\frac{C_d}{C_{ox}}\right)$$

C_d = depletion layer capacitance, C_{ox} = gate-oxide capacitance.The typical value of Subthreshold swing at room temperature is $70\frac{mV}{dec}$.

A dec (decade) corresponds to a 10 times increase of the drain current I_d .A device characterized by sharp subthreshold slope exhibits a quicker transition between off (low current) and on (high current) states.

Fig. 5.5.1 shows the subthreshold slope variation with gate misalignment for SMDG, DMDG and TMDG structures. It is observed that for all three structures, the subthreshold swing increases for both SSM and DSM. In TMDG structure, the subthreshold swing is more than that of DMDG and SMDG counterparts and it can be well explained by the position and magnitude of the minimum of the surface potential.

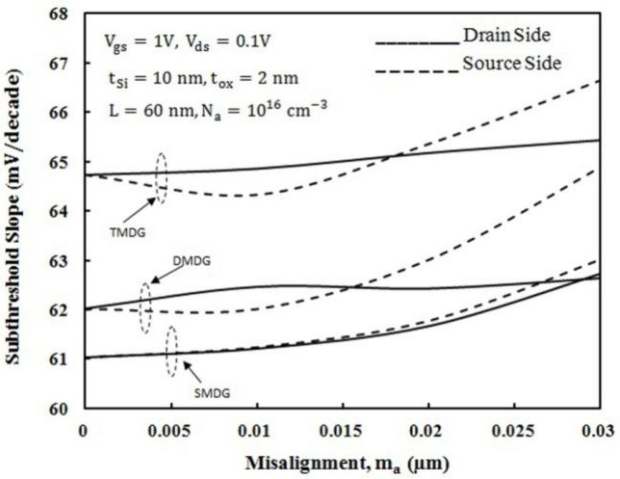

Figure 5.5.1: Subthreshold slope variation with gate misalignment SMDG ($\phi_{M1} = 4.8\,\text{eV}$), DMDG ($\phi_{M1} = 4.8\,\text{eV}, \phi_{M2} = 4.6\,\text{eV}$) and TMDG ($\phi_{M1} = 4.8\,\text{eV}, \phi_{M2} = 4.6\,\text{eV}, \phi_{M3} = 4.4\,\text{eV}$) MOSFET structures.

5.6 Sub threshold current

Subthreshold drain current or Subthreshold conduction or subthreshold leakage is the current which passes between the source and drain of a MOSFET when the transistor is in subthreshold regime, or weak-inversion condition, that is, for gate-to-source voltages less than the threshold voltage. The subthreshold region is frequently called as the weak inversion region. The terms for various degrees of inversion is described in Tsividis [67].

In circuits like digital, subthreshold current is generally considered as a parasitic leakage in a state that would preferably have no current. In ultra low power analog circuits, on the other hand, weak inversion is an competent operating region, and subthreshold is a valuable transistor mode around which circuit functions are intended [68].

In the past, the subthreshold current of transistors has been very less, but as the scaling of the transistors have been imposed, leakage from all sources has enhanced. For a particular technology generation with threshold voltage of 0.2 V, leakage can go beyond 50% of total power expenditure [69].

The cause for a rising significance of subthreshold conduction is that the supply voltage has repeatedly scaled down, both to decrease the dynamic power consumption of integrated circuits, and to remain electric fields inside small devices low, to uphold device consistency. The quantity of subthreshold conduction is set by the threshold voltage, which sits between the supply voltage and ground, and so has to be decreased along with the supply voltage. That reduction means small amount of gate voltage swing below threshold to turn-off the device, and as subthreshold current varies exponentially with gate voltage, it becomes more and more important as MOSFETs minimize in dimension [70].

Figures 5.6.1, 5.6.2 and 5.6.3 demonstrate the subthreshold current variation against the gate voltage, having DSM and SSM, for SMDG, DMDG and TMDG MOSFET structures respectively. Figure 5.6.1 depicts that in SMDG MOSFET structure, subthreshold current decreases with increase in misalignment at both source and drain ends of the device. The reason can be understood from Fig. 5.3.1 where the nature of V_t variation is shown against the misalignment. It can be said that increased V_t at higher misalignment leads subthreshold current to a reduced value. Figures 5.6.2 and 5.6.3 demonstrate that in both DMDG and TMDG MOSFET structures, subthreshold current decreases with increase in source side misalignment and increases with increase in drain side misalignment. This can also be explained from V_t variation against the misalignment which is shown in Fig. 9.

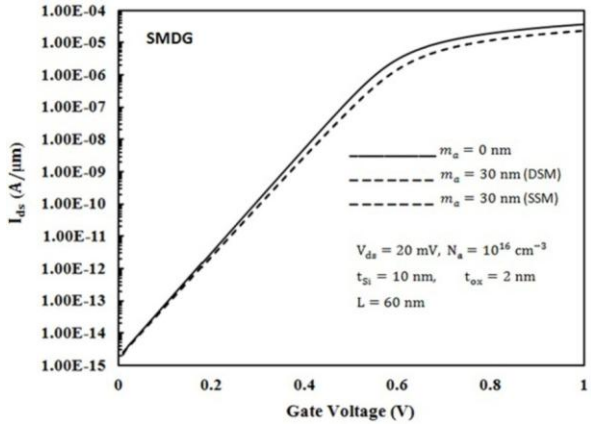

Figure 5.6.1: Subthreshold drain-current variation with gate voltage for SMDG ($\phi_{M1} = 4.8\,\text{eV}$) MOSFET structure.

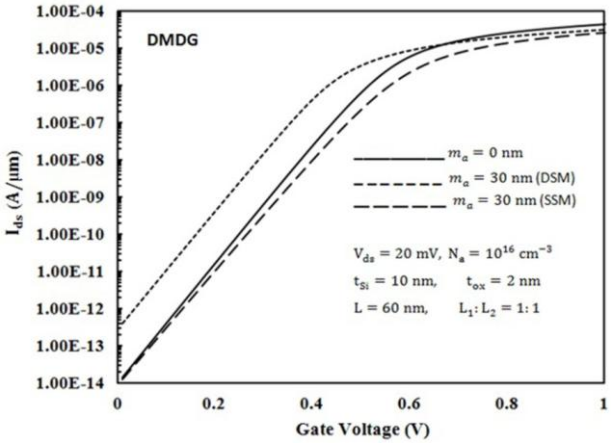

Figure 5.6.2: Subthreshold drain-current variation with gate voltage for DMDG ($\phi_{M1} = 4.8\,\text{eV}$ $\phi_{M2} = 4.6\,\text{eV}$) MOSFET structure ($L_1 : L_2 = 1:1$).

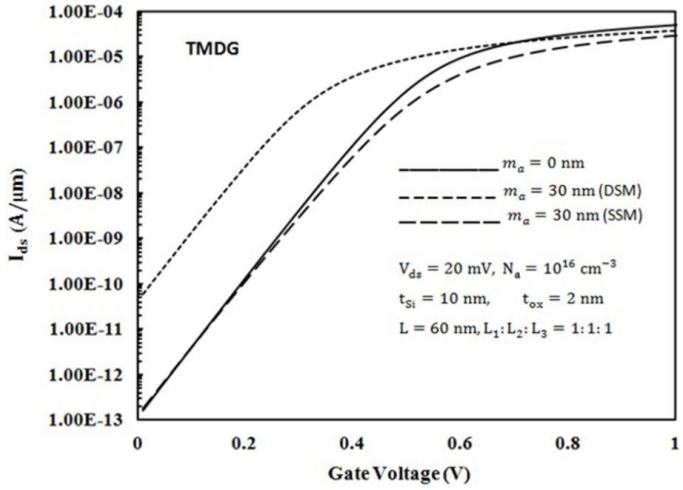

Figure 5.6.3: Subthreshold drain-current variation with gate voltage for TMDG ($\phi_{M1} = 4.8\,\text{eV}$ $\phi_{M2} = 4.6\,\text{eV}$ $\phi_{M3} = 4.4\,\text{eV}$) MOSFET structure ($L_1 : L_2 : L_3 = 1:1:1$) .

5.7 Maximum drain current

Figures 5.7.1 depicts maximum drain current and maximum transconductance variation with the gate misalignment in SMDG, DMDG and TMDG structures. It is observed that drain current decreases as misalignment increases. The maximum drain current is the highest for the TMDG structure on comparison with DMDG and SMDG MOSFET structures, when the misalignment length is zero (without misalignment).

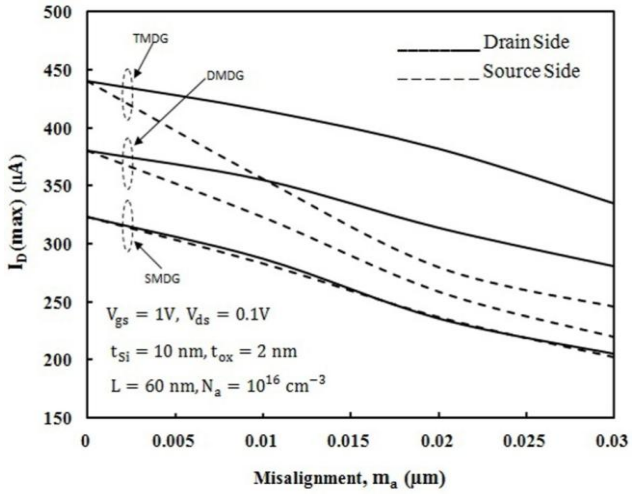

Figure 5.7.1: Maximum drain current ($I_D(\max)$) variation with gate misalignment for SMDG ($\phi_{M1} = 4.8\,\text{eV}$), DMDG ($\phi_{M1} = 4.8\,\text{eV}$, $\phi_{M2} = 4.6\,\text{eV}$) and TMDG ($\phi_{M1} = 4.8\,\text{eV}$, $\phi_{M2} = 4.6\,\text{eV}$, $\phi_{M3} = 4.4\,\text{eV}$) MOSFET structures.

5.8 Tranconductance

The transconductance of the MOSFET decides its gain and is proportional to hole or electron mobility (depending on device type), at least for low drain voltages. As MOSFET size is reduced, the fields in the channel increase and the dopant impurity levels increase. Both changes reduce the carrier mobility, and hence the transconductance. As channel lengths are reduced without proportional reduction in drain voltage, raising the electric field in the channel, the result is velocity saturation of the carriers, limiting the current and the transconductance.

Figure 5.8.1, depicts maximum transconductance variation with the gate misalignment in SMDG, DMDG and TMDG structures. It is observed that transconductance decreases as misalignment increases. The TMDG structure possesses the higher transconductance compared to DMDG and SMDG structures in the absence of any misalignment. As drain side misalignment increases, both maximum drain current and maximum transconductance decreases for all three structures. The reason is that the overall inversion charge density in non-overlap region gets reduced significantly in the absence of gate electric field. Thus the overall reduction in inversion charge density due to misalignment results in the reduction of both drain current and transconductance. With SSM the reduction of drain current and transconductance is more significant than DSM because the inversion charge density is less in SSM than the DSM.

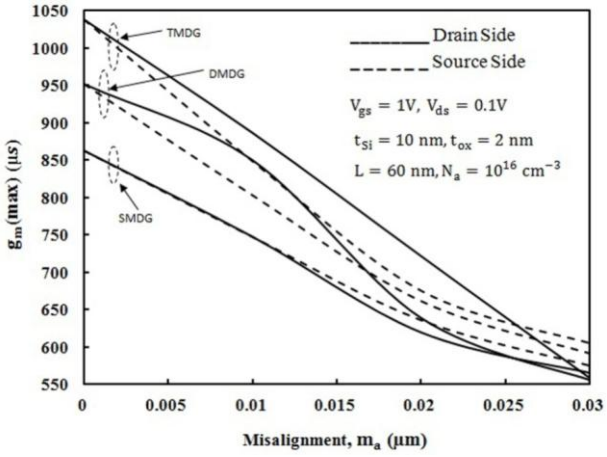

Figure 5.8.1: Maximum transconductance ($g_m(\max)$) variation with gate misalignment for SMDG ($\phi_{M1} = 4.8\,\text{eV}$), DMDG ($\phi_{M1} = 4.8\,\text{eV}, \phi_{M2} = 4.6\,\text{eV}$) and TMDG ($\phi_{M1} = 4.8\,\text{eV}, \phi_{M2} = 4.6\,\text{eV}, \phi_{M3} = 4.4\,\text{eV}$) MOSFET structures.

5.9 Output Conductance

Output conductance is one of the important parameters for accounting the channel length modulation in a device. It is defined as the change in drain current with respect to the change in drain voltage. Ideally, the value of output conductance at saturation should approach zero. Figs. 5.9.1-5.9.6 show the output conductance versus drain voltage of SMDG, DMDG and TMDG structures at different misalignments. It can be observed in each structure that the output conductance decreases consistently with increasing misalignment at the source end. However, the decrease in output conductance is inconsistent when misalignment increases at the drain end of the device. It is also observed that among TMDG, DMDG and SMDG MOSFET structures, the TMDG MOSFET structure possesses the highest output conductance.

Figure 5.9.1, depicts the output conductance of SMDG MOSFET when the misalignment occurs at the drain side. As the misalignment length increases the output conductance decreases gradually at very low drain voltage and its value is inconsistent at high drain voltages. It is seen that from the figure that, at high drain voltage or at saturation condition a non-zero output conductance is present due to gate misalignment and the value increases as the misalignment length increases.

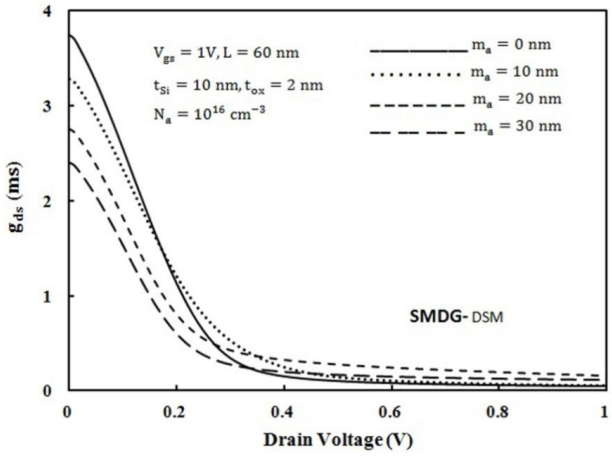

Figure 5.9.1: Output conductance (g_{ds}) variation with drain voltage for SMDG ($\phi_{M1} = 4.8\,\text{eV}$) MOSFET structure at drain side misalignment.

Figure 5.9.2, depicts the output conductance of SMDG MOSFET when the misalignment occurs at the source side. As the misalignment length increases the output conductance decreases gradually at very low drain voltage and its value is consistently decreases at high drain voltages. It is seen that from the figure that, at high drain voltage or at saturation

condition approximately a zero output conductance is present due to gate misalignment and the value decreases as the misalignment length increases.

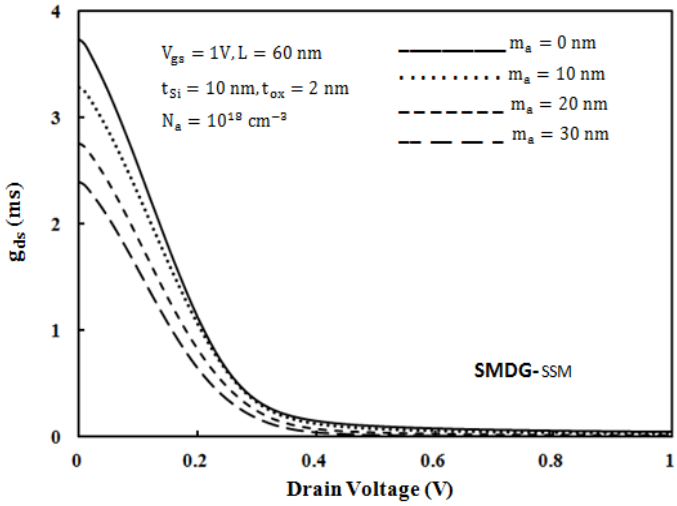

Figure 5.9.2: Output conductance (g_{ds}) variation with drain voltage for SMDG ($\phi_{M1} = 4.8\,\text{eV}$) MOSFET structure at source side misalignment.

Figure 5.9.3, depicts the output conductance of DMDG MOSFET when the misalignment occurs at the drain side. As the misalignment length increases the output conductance decreases gradually at very low drain voltage and its value is inconsistent at high drain voltages. It is seen that from the figure that, at high drain voltage or at saturation condition a non-zero output conductance is present due to gate misalignment and the value increases as the misalignment length increases.

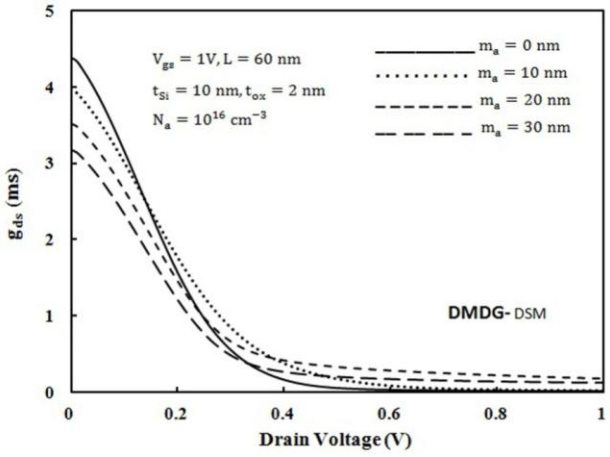

Figure 5.9.3: Output conductance (g_{ds}) variation with drain voltage for DMDG ($\phi_{M1} = 4.8\,\text{eV}$, $\phi_{M2} = 4.6\,\text{eV}$) MOSFET structure at drain side misalignment.

Figure 5.9.4, depicts the output conductance of DMDG MOSFET when the misalignment occurs at the source side. As the misalignment length increases the output conductance decreases gradually at very low drain voltage and its value decreases at high drain voltages. It is seen that from the figure that, at high drain voltage or at saturation condition a zero output conductance is present due to gate misalignment.

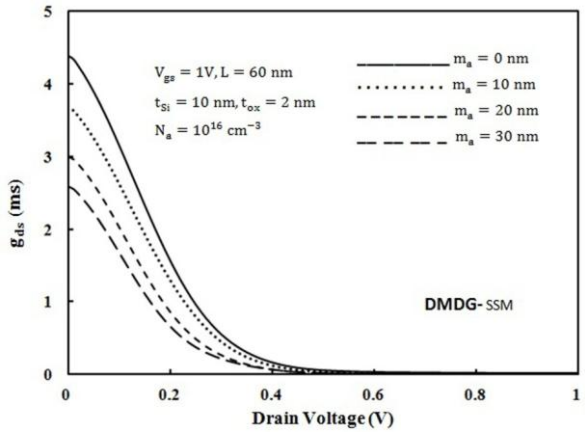

Figure 5.9.4Output conductance (g_{ds}) variation with drain voltage for DMDG ($\phi_{M1} = 4.8\,\text{eV}$, $\phi_{M2} = 4.6\,\text{eV}$) MOSFET structure at source side misalignment.

Figure 5.9.5, depicts the output conductance of TMDG MOSFET when the misalignment occurs at the drain side. As the misalignment length increases the output conductance decreases gradually at very low drain voltage and its value is inconsistent at high drain voltages. It is seen that from the figure that, at high drain voltage or at saturation condition a non-zero output conductance is present due to gate misalignment and the value increases as the misalignment length increases.

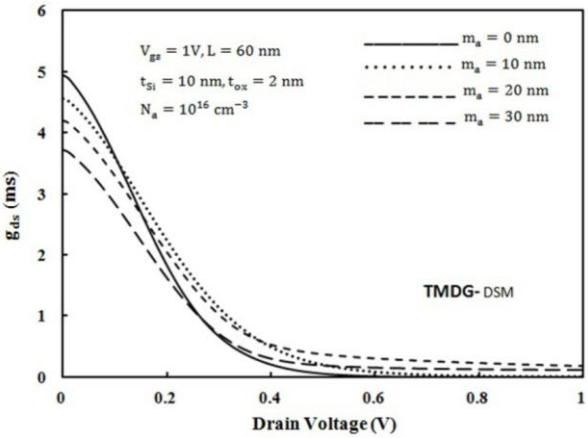

Figure 5.9.5: Output conductance (g_{ds}) variation with drain voltage for TMDG ($\phi_{M1} = 4.8\,\text{eV}$, $\phi_{M2} = 4.6\,\text{eV}$, $\phi_{M3} = 4.4\,\text{eV}$) MOSFET structure at drain side misalignment.

Figure 5.9.5, depicts the output conductance of TMDG MOSFET when the misalignment occurs at the source side. As the misalignment length increases the output conductance decreases gradually at very low drain voltage and its value decreases at high drain voltages. It is seen that from the figure that, at high drain voltage or at saturation condition a zero output conductance is present due to gate misalignment.

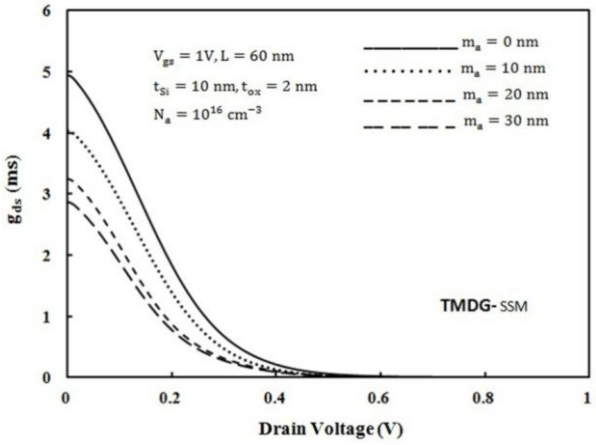

Figure 5.9.6: Output conductance (g_{ds}) variation with drain voltage for TMDG ($\phi_{M1} = 4.8\,\text{eV}$, $\phi_{M2} = 4.6\,\text{eV}$, $\phi_{M3} = 4.4\,\text{eV}$) MOSFET structure at source side misalignment.

Chapter 6

6 CONCLUSION

6.1 Performance Analysis

In the present work, the effects of gate misalignment have been investigated in the TMDG, DMDG and SMDG MOSFET structures by using a 2D ATLAS device simulator. The parameters which are investigated with source side misalignment (SSM) and drain side misalignment (DSM) are surface potential, threshold voltage, subthreshold swing, subthreshold current, drain induced barrier lowering (DIBL), maximum drain current, maximum transconductance and output conductance. It is found that for the given channel length, TMDG MOSFETs are highly prone to short-channel effects (SCEs) compared to the DMDG and SMDG MOSFET structures. Further, for the same channel length, TMDG MOSFET has the highest immunity against the DIBL effects. Furthermore, threshold voltage and DIBL decreases and increases, respectively when the misalignment at drain end increases. Due to misalignment, subthreshold slope is more in TMDG MOSFET compared to DMDG and SMDG MOSFETs which results in the degradation of subthreshold performance of the TMDG MOSFET. With source side misalignment, the output conductance decreases as misalignment increases and its value is almost negligible in saturation region of the operation. Similarly in the case of drain side misalignment output conductance decreases as misalignment increases for all three types of DG MOSFET structures, but in the saturation region its behaviour is inconsistent and possesses some finite value. In other words, we can say that the channel length modulation is more in drain side misalignment than the source side misalignment.

6.2 Scope of Future work

Here in this work, I have only investigate and analysed the dc device parameters with a extensive simulation. In future one can investigate the gate misalignment effects on analog and RF performance of the device. It is also possible to fabricate the device, and measuring the accuracy between the experimental data and the simulation results.

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