

**IMPROVED TECHNIQUES FOR HIGH
PERFORMANCE NOISE-TOLERANT DOMINO CMOS
LOGIC CIRCUITS**

A thesis submitted in partial fulfilment of the requirements for the
award of the degree of

Master of Technology

in

VLSI Design and Embedded Systems

by

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2010

CERTIFICATE

This is to certify that the thesis report entitled “**IMPROVED TECHNIQUES FOR HIGH PERFORMANCE NOISE-TOLERANT DOMINO CMOS LOGIC CIRCUITS**” submitted by **Srinivasa V S Sarma D, Roll No: 208EC214**, in partial fulfilment of the requirements for the award of the degree of Master of Technology with specialization in “**VLSI Design and Embedded Systems**” in **Electronics and Communication Engineering** at the **National Institute of Technology, Rourkela** is an authentic work under my supervision and guidance.

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ABSTRACT

[Key Words: Domino CMOS logic, CMOS technology scaling, speed, power consumption.]

Domino CMOS logic circuit family finds a wide variety of applications in microprocessors, digital signal processors, and dynamic memory due to their high speed and low device count. However, there are inevitable problems that degrade the noise immunity of this family; they are the inevitable leakage current and the charge sharing. Added to the drawbacks is the relatively large power consumption, especially if compared to the static complementary CMOS logic family. To make the matter worse, these drawbacks are more tactile with the scaling of CMOS technology.

In my thesis, An introduction to domino logic, The impact of CMOS technology scaling on the performance of domino CMOS logic, Three Phase Domino Logic Circuit, High-performance noise-tolerant circuit techniques for CMOS dynamic logic and other Domino logic techniques are studied and corresponding Domino logic techniques have been designed and simulated. Specifically, the need to decrease the dynamic power consumption forces the designer to use a lower power-supply voltage. This in turn necessitates the reduction of threshold voltage to maintain the performance with the associated increase in sub threshold leakage current. So, a properly sized PMOS keeper must be used to compensate for this leakage. It will be found that the speed, which is the major advantage of domino logic compared to other logic styles, will degrade with CMOS technology scaling due to the contention current of the keeper. To assure high performance in noise tolerant techniques, the inevitable effects like leakage currents and charge distribution have to be minimized.

In this thesis few modifications have also been made to already existing domino techniques and different Domino logic circuits are simulated in both Cadence virtuoso (implemented using GPDK090- library of 90nm technology) and Mentor graphics (implemented at different technologies like Tsmc 035.mod, Tsmc 025.mod, Tsmc 018.mod) environments. The performance parameters are also compared with other standard architectures of Domino logic.

CHAPTER 1

AN INTRODUCTION TO DOMINO LOGIC

1.1 CMOS and NMOS

By the late 1970s complementary metal oxide semiconductor (CMOS) started to become the process of choice for digital semiconductor designs. CMOS had originally been proposed by Frank Wanlass in 1963 as a low standby power technology, since CMOS logic gates dissipate almost no power when the inputs to the gate do not change. This follows as CMOS contains both PMOS field effect transistors (FETs), which can efficiently drive a high voltage, or logic one value, and NMOS transistors, which are good at driving a zero voltage. The presence of complementary transistors allows CMOS logic gates to be implemented so that the output voltage level is connected to the power or ground line, but not both. This ability to avoid contention ensures that if the inputs are not changing, then no power is dissipated. This was a major advantage of CMOS over the other manufacturing processes then available, which dissipated constant leakage or bias currents.

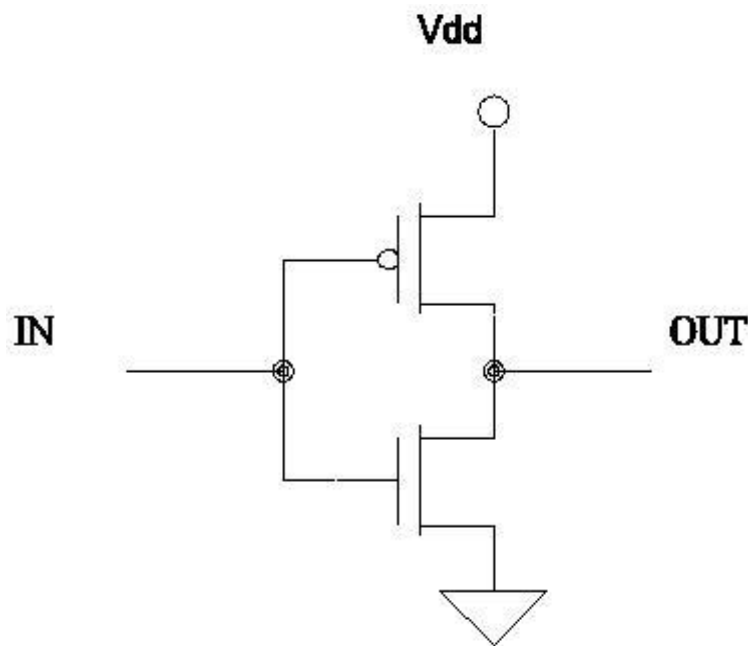


Fig. 1.1 A static CMOS Logic.

In Figure 1.2 the schematic representation of a CMOS static NAND logic gate is shown. The logic gate has two inputs A and B. A high logic value at inputs A and B turns on transistors MN1 and MN2, while turning off transistors MP1 and MP2. This causes the output Z to be low. When either input A or B is off, however, the path to the ground line is ruptured, with a path to the power supply (Vdd) being established. This causes Z to rise. While a NAND gate represents a simple function, it does show how contention between the power and ground supplies can be avoided in CMOS circuits. This lack of contention means that when the inputs to a CMOS circuit do not change, often called a standby or idle state, almost no power dissipation occurs, except for a small leakage current which flows through the transistors due to the imperfect manner in which a MOSFET acts as a switch due to the relentless scaling in the physical dimensions of CMOS processes, driven by the cost advantages of having a smaller silicon area for digital functions, MOS transistors have become less perfect switches, leading to greater leakage current.

The fact that CMOS logic would lead to substantial power savings was apparent to its inventor Frank Wanlass, who in 1963 attempted to prove the viability and technical advantages of CMOS with a monolithic implementation of the technology. When this proved infeasible, he proved the concept with discrete transistors. His CMOS implementations reduced standby power by six orders of magnitude over equivalent bipolar and PMOS implementations. While impressive, this advantage of CMOS would not prove decisive for many years. Early monolithic designs were very small, with the standby power consequently being very small as an absolute quantity. The inferior maturity of MOS transistors meant that in the 1960s, bipolar logic raced ahead of MOS transistors in applications. Transistor–transistor logic (TTL) and emitter-coupled logic (ECL) developed in 1962 and 1966, respectively, provided effective digital design techniques for bipolar transistors in the rapidly increasing semiconductor industry. The major user of CMOS in its early years was the watch industry, where battery life was a more important attribute than speed. Starting in the 1970s, MOS technology began to mature rapidly, with much of the early industrial development being driven by Intel. In 1971 Intel released the 4004, the world’s first microprocessor.

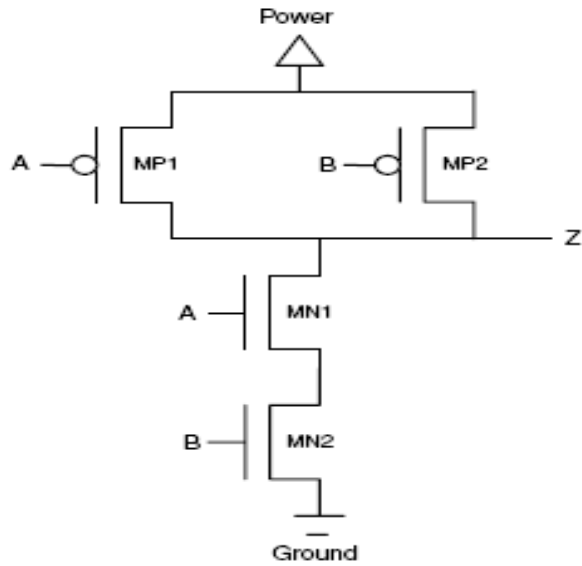


Fig. 1.2 A static CMOS two-input NAND cell.

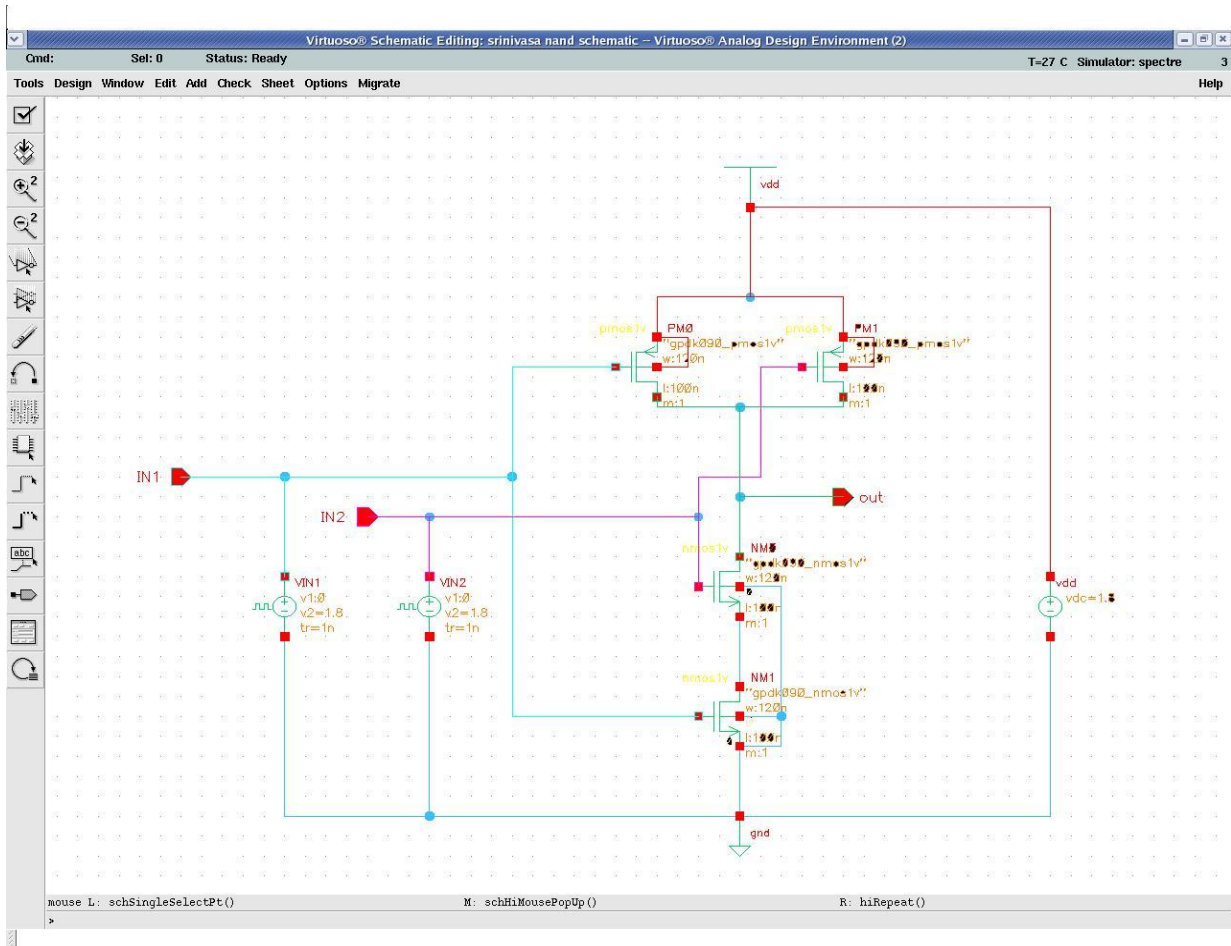


Fig. 1.3 A static CMOS two-input NAND cell implementation.

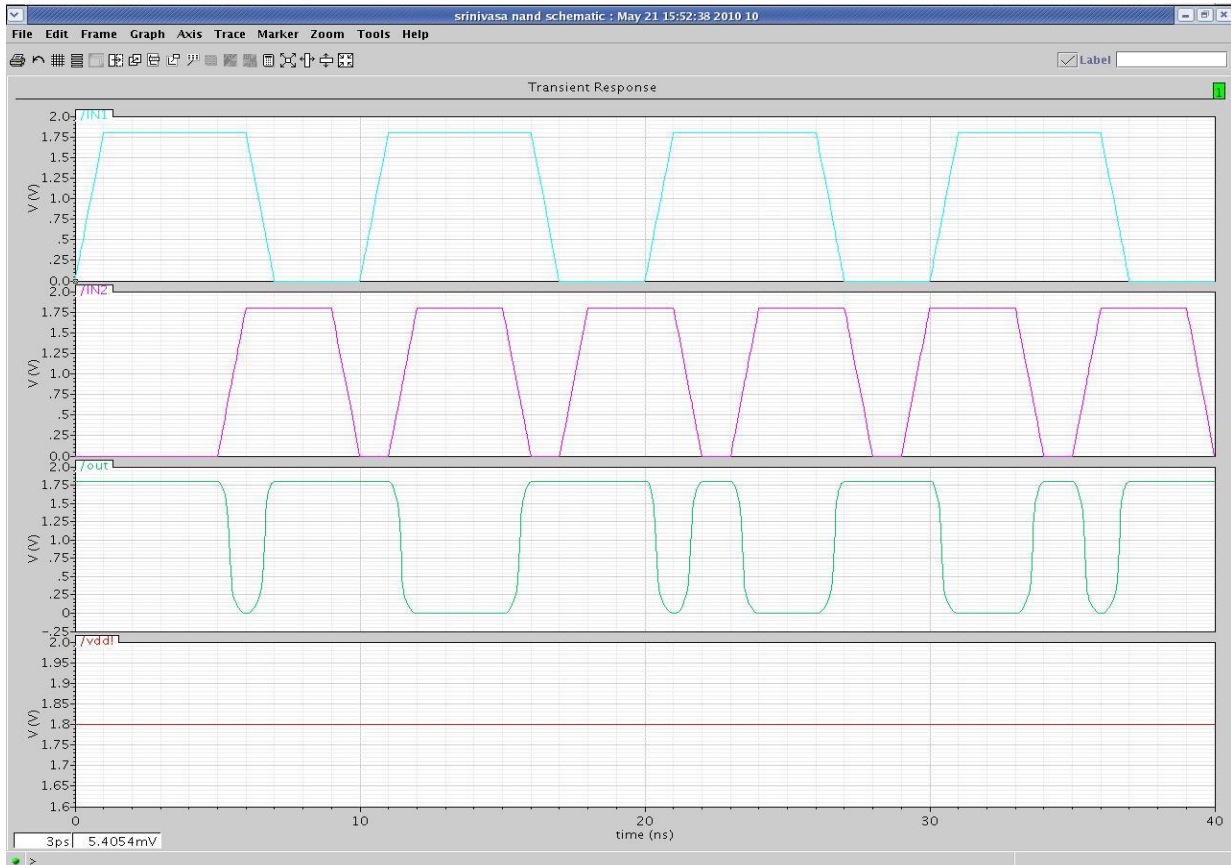


Fig. 1.4 A static CMOS two-input NAND cell simulation.

The 4004 was built using a 10 μm line width PMOS transistor and used 2300 transistors running at 108 kHz. In 1974 Intel released the 8-bit 8080, manufactured in a 6 μm NMOS process. The chip ran at 2MHz and had 6000 transistors. Yield and cost concerns at the time ensured manufacturers preferred to use a single type of MOS transistor. Since NMOS transistors were faster than PMOS ones, due to the higher mobility of electrons over holes, the move to an NMOS process was natural.

Advantages of CMOS Logic:

- (1) Robustness(less sensitive to noise).
- (2) Simple approach for implementing logic gates.
- (3) Easy to translate logic to FETs.
- (4) Good noise margins since FETs are in cut off & sizing not critical
- (5) No static power dissipation.
- (6) Low power consumption.

Disadvantages of CMOS Logic:

- (1) Complexity of circuits increases with increased Fan-in.
- (2) For N-input logic gate, 2N-transistors are required which results in significantly large implementation area.
- (3) Propagation delay of CMOS gates deteriorates rapidly as a function of Fan-in.

Fig. 1.5 shows the schematic implementation of a NAND gate using NMOS transistors only. The PMOS transistors MP1 and MP2 shown for the CMOS implementation in Fig. 1.2 are removed here and replaced by a resistor, R1. This conceptual resistor is actually implemented by a depletion mode NMOS transistor. The NMOS NAND gate output is at V_{dd}, or a logic one value, when either of the inputs, A or B, is low. When input A and input B are both high, the output is driven low. The current-driving ability of pull-down NMOS transistors must be much greater than that of the pull-up resistor. This ensures that the output can be driven to a low voltage at the cost of higher power dissipation. In addition to the standby power dissipation, NMOS circuits tend to be slower than equivalent CMOS circuits. This is due to the need for a weak pull-up resistor, which results in very slow low-to-high transitions. While these disadvantages may make NMOS appear to be unappealing, NMOS designs are more compact than CMOS circuits. Figure 1.5 uses only two transistors and a resistor, compared with the four transistors needed by a CMOS design. Since the pull-up resistor is implemented by another NMOS MOSFET, the NMOS design uses fewer transistors and a simpler process than the CMOS design. The need to move to CMOS therefore arose only when the integration level on integrated circuits (ICs) made the large standby power on the NMOS design unacceptable. For Intel this transition occurred in 1978, when the 8088/8086 family of microprocessors was introduced (the designs were almost identical to the 8088, having an 8-bit bus while the 8086 has a 16-bit bus). With 29,000 transistors and a clock rate of 5 to 10 MHz, the 8086 dissipated 1.5W. This exceeded the 1W per chip power limit for plastic packaging. Increases in integration levels meant that a 32-bit processor would dissipate 5 to 6W, leading to severe reliability problems. The CMOS version of the 8086, the 80C86, consumed only 250mW.

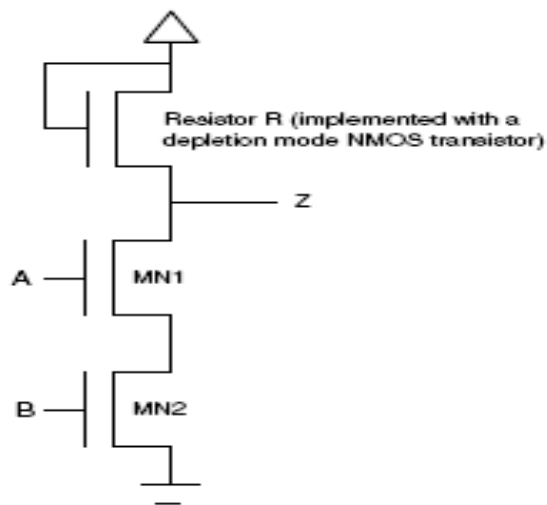


Fig. 1.5 A NMOS two-input NAND Logic.

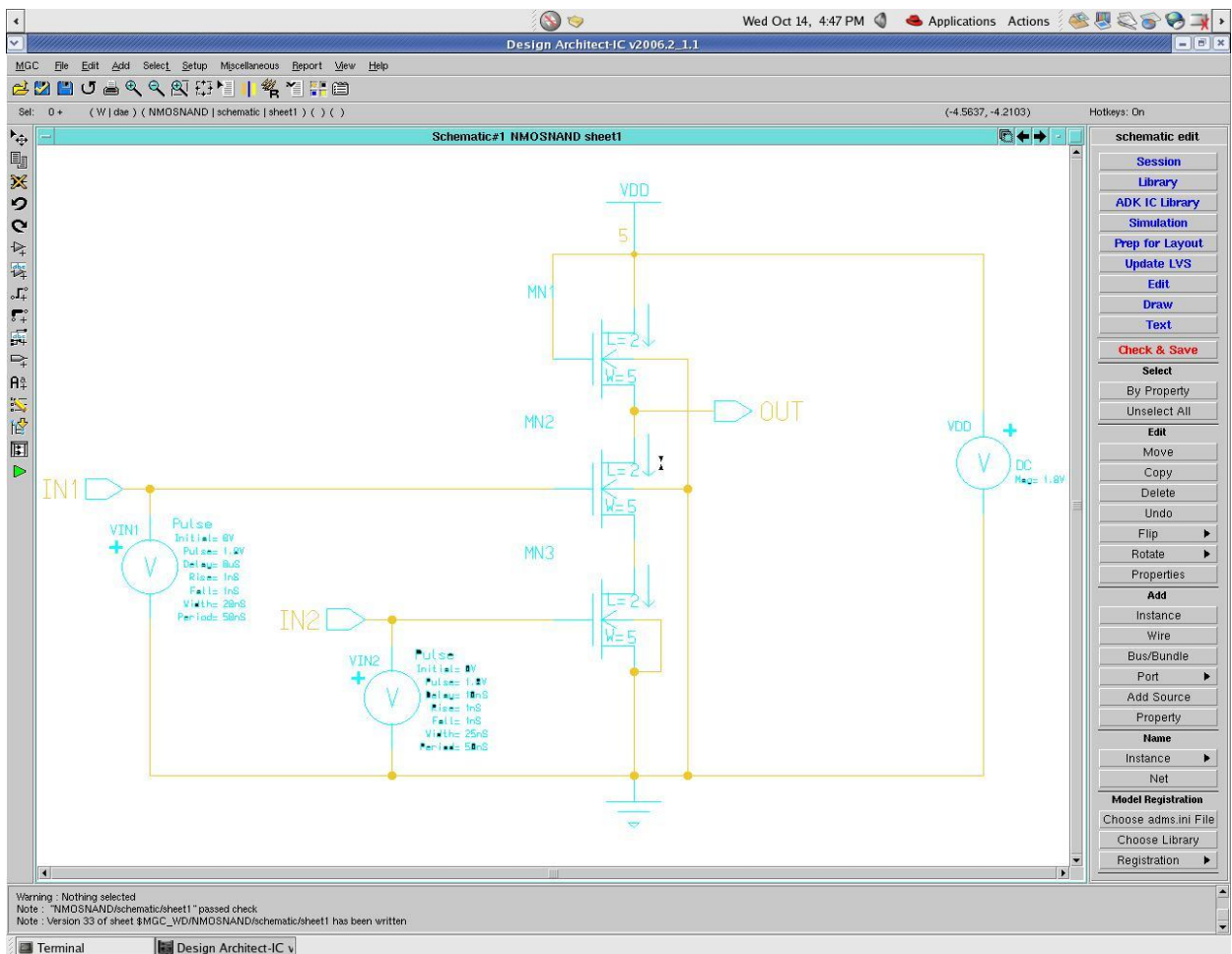


Fig. 1.6 A NMOS two-input NAND gate schematic implementation.

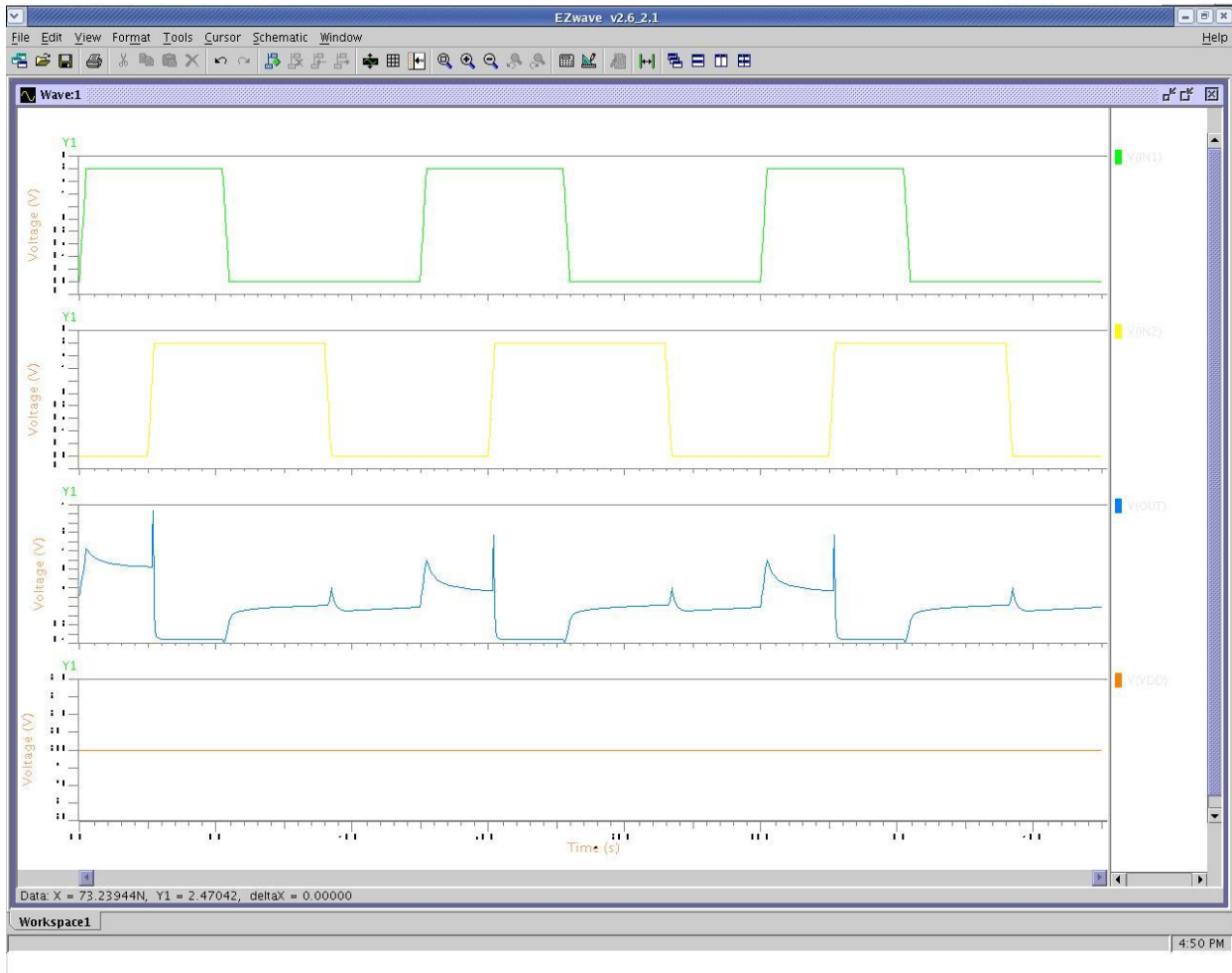


Fig. 1.7 A NMOS two-input NAND gate schematic simulation.

The ability of CMOS to reduce power dissipation with increasing integration meant that it rapidly emerged as the technology that could best utilize fabrication advances. It is an advantage that CMOS maintains till today with the overwhelming majority of digital IC designs in the world being manufactured in CMOS, and the increased convergence of systems onto chips leading CMOS to make strong inroads into analog and radio frequency (RF) designs.

As semiconductor manufacturing progressed, the largest challenge to the nascent industry was the ability to design and verify designs using the increasing number of transistors available. This need was met by the development of a new field of software, often closely tied to dedicated hardware in its early years, called electronic design automation (EDA). It may have been assumed that the emergence of ASIC design methodologies would displace

all other techniques for implementing digital CMOS logic. This has not happened, as many digital designs have specific needs that cannot be achieved by using standard ASIC techniques. In recent years the capabilities of ASIC tools have increased greatly.

The two most common benefits of custom design are

- (1) Its ability to optimize across the different levels of abstractions in the ASIC design framework and the opportunity it provides for using logic families other than standard static logic. The first of these advantages relates to the sequential approach that an ASIC design methodology uses, by which standard cell library development, logic synthesis, and physical design are broadly separate processes.
- (2) The second advantage of custom design is that it can utilize certain logic families, specifically dynamic logic, that automated design frameworks have not traditionally been able to support.

1.2 Different static logic styles

1.2.1 Pseudo N-MOS

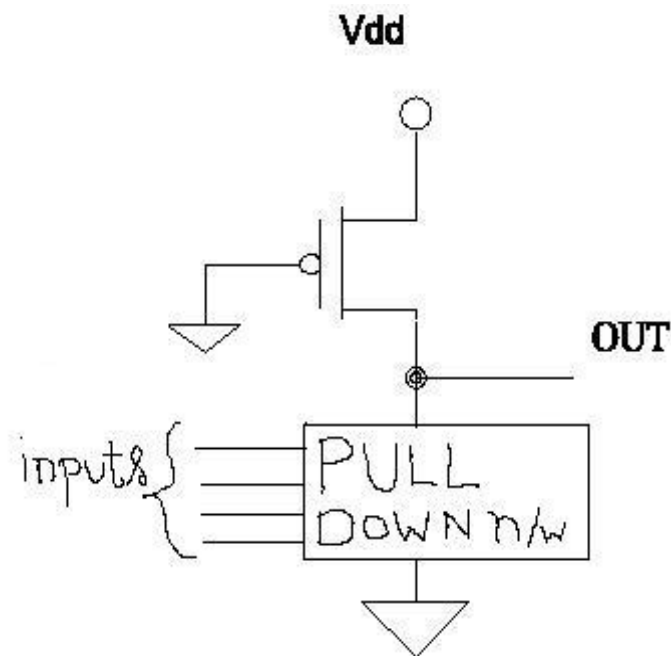


Fig. 1.8 Pseudo N-MOS Logic.

Advantages:

For N-input logic gate implementation, only (N+1) transistors are needed. This count is less when compared with Static CMOS Logic.

Disadvantages:

- (1) Noise Margin reduces.
- (2) Static power dissipation increases.

1.2.2 Differential Cascade Voltage Swing Logic

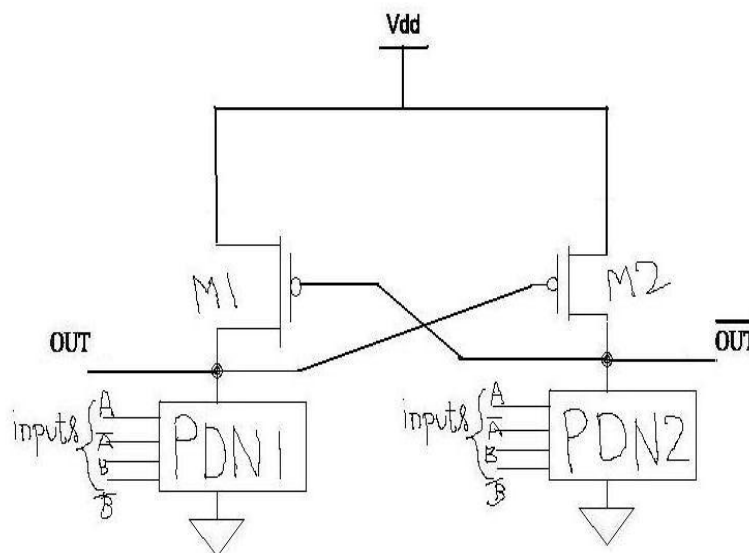


Fig. 1.9 Differential Cascade Voltage Swing Logic.

PDN 1 and PDN 2 are mutually exclusive, i.e. PDN2 = Complement of (PDN1)

Advantages:

- (1) Provides rail-to-rail swing.
- (2) Completely eliminates static currents, thus static power dissipation is eliminated.
- (3) A logic and its inverse can simultaneously be implemented.

Disadvantages:

- (1) Exhibits the problem of increased design complexity.
- (2) Power dissipation problem due to cross-over currents.

- (3) During the transition, there is a period of time when PMOS & PDN are turned 'ON' – simultaneously, producing a Short-Circuit path.

1.2.3 Pass Transistor Logic

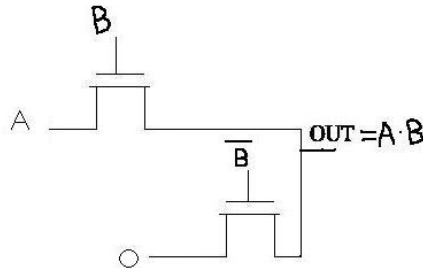


Fig. 1.10 Pass-transistor logic implementation of AND gate.

Advantages:

- (1) Reduces number of transistors required to implement logic by allowing the primary inputs to drive Gate, Source & Drain terminals of MOSFET.
- (2) The process of reducing the number of devices has the additional advantage of Lower-Capacitance.

Applications:

This logic is used in Multiplexers and Latches.

Note: PTL gates cannot be cascaded by connecting the output of a gate to the input of another Pass-transistor.

1.2.4 Differential / Complementary Pass Transistor Logic

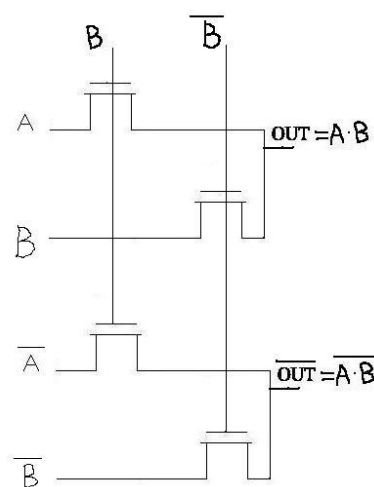


Fig. 1.11 Differential / Complementary Pass-transistor logic implementation of AND/NAND gate.

Advantages:

- (1) Complex gates such as XOR, XNOR and adders can be realized efficiently with small number of transistors.
- (2) This belongs to a class of Static gates, because the output nodes are always connected to either 'VDD' or 'Ground' through a low resistance path. This is an advantageous for Noise resilience.

Disadvantages:

- (1) Static power dissipation is present.
- (2) Reduced Noise Margins.

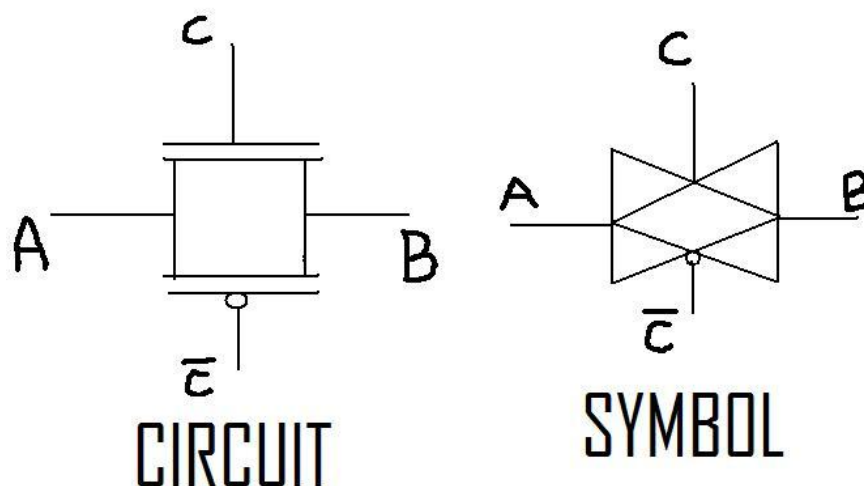
Remedy for drawbacks:

- (1) Using Level restoration circuit techniques.
- (2) Multiple threshold transistor techniques.
- (3) Implementing Transmission-Gate logic.

The most widely used technique to deal with Voltage-drop problems is Transmission-Gate logic.

• Transmission-Gate logic:

- It builds on the complementary properties of NMOS & PMOS transistors.
- Transmission gate combines the best of both device flavours by replacing an NMOS in parallel with a PMOS.



Where 'C' and complement of ('C') are control signals which are complement to each other

Fig. 1.12 Transmission-Gate logic.

Transmission-Gate acts as a Bi-directional switch controlled by gate control signal-‘C’.

(1) If C='1', then both the MOSFETs are 'ON', so they allow signal to pass through the gate.

Therefore $A=B$, if $C='1'$.

(2) If C='0', then both the MOSFETs are 'OFF', so then are in cut-off, Thus there is an open circuit between nodes A and B.

Advantages:

(1) It enables rail-to-rail swing although it requires 2-transistors & more control signals.

(2) Using Transmission gates, complex gates can be built very efficiently.

Fig. 1.13 shows the implementation of XOR gate using Transmission-Gate logic.

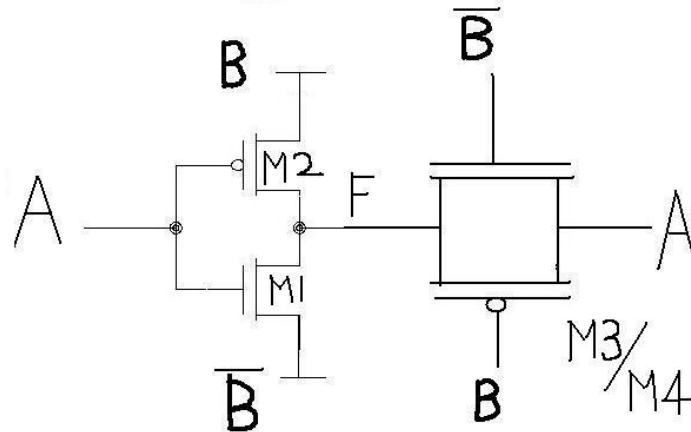


Fig. 1.13 Transmission-Gate XOR.

(1) If B='1', then transistors M1 & M2 act as inverters, while transmission gate M3/M4 is 'OFF'. Hence $F = [(\text{NOT}('A')) \text{AND} ('B')]$.

(2) If B='0', then transistors M1 & M2 are disabled and the transmission gate is operational.

Therefore $F = [('A') \text{AND} (\text{NOT}('B'))]$.

The combination of both leads to XOR function and regardless of the values of 'A' and 'B', node 'F' always has a connection to either 'VDD' or 'Ground' and thus is a Low-impedance node. When designing static-pass-transistor networks, it is essential to adhere to the low impedance rule under all circumstances.

1.3 Dynamic CMOS logic design

In IC's, Dynamic logic (Clocked logic) is a design methodology logic family in digital logic that was popular in 1970s. It can be distinguished from static logic in that it uses a clock signal in its implementation of Combinational logic circuits. The use of clock signal in Dynamic logic is to evaluate the combinational logic. The clock signal is also used in sequential circuits where it is used to synchronize the transitions in sequential logic circuits.

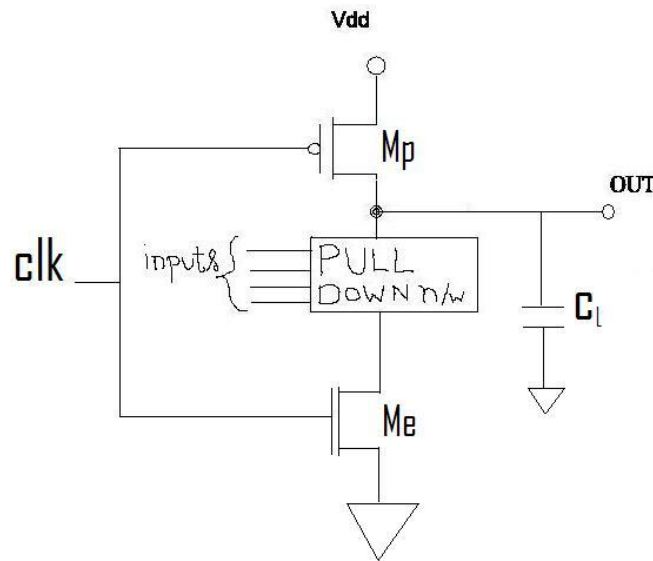


Fig. 1.14 Dynamic CMOS Logic.

When CLK is low

- (1) Evaluate M_e is off and precharge M_p is on
- (2) Output node is precharged to VDD, other nodes *may* precharge to $VDD - V_{th,n}$ depending on values of inputs

When CLK goes high

- (1) Evaluate M_e is on and precharge M_p is off
- (2) Output node may be discharged if inputs have configured a conducting path to GND, otherwise output node stays charged high.
- (3) Inputs must be stable before CLK goes high because once output has been discharged it won't go high again until next cycle
- (4) For same reason, noise/glitches on inputs cannot exceed M_e threshold, a much more stringent requirement than for static CMOS gates.

Advantages:

- (1) No static power consumption with addition of a clock input, it uses a sequence of
 - (a) Pre-charge
 - (b) Evaluation phases.
- (2) Increased speed and reduced implementation area.
- (3) This logic is twice as fast as the normal static CMOS logic since it uses only fast N-transistors in its evaluation phase.
- (4) It is amenable to transistor sizing optimizations.
- (5) Glitches (Dynamic Hazards) do not occur.

- **Glitches (Dynamic Hazards):**

The finite propagation delay from one logic block to next logic block causes spurious or abrupt transitions, which are known as Glitches. Gates have a non-zero propagation delay.

Drawbacks:

- (1) More power consumption because this logic greatly increases the number of transistors which are switching at any given time.
- (2) Problems will arise when cascading one gate to next gate.

Signal Integrity Issues in Dynamic Design:

There are several important considerations that must be taken into account if one wants Dynamic circuits to function properly.

They are

- (1) Charge leakage
- (2) Charge sharing
- (3) Capacitive coupling and
- (4) Clock feed through

Charge leakage and Charge sharing occur in Evaluation phase.

1.4 Domino logic circuits

It is a CMOS-based evolution of dynamic logic techniques which were based on either PMOS or NMOS transistors. To speed-up the circuits this logic was developed.

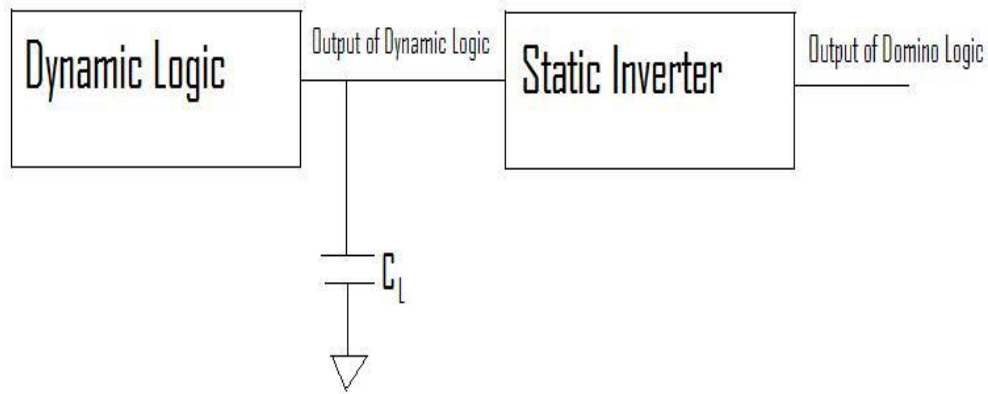


Fig. 1.15 Block diagram of Domino Logic.

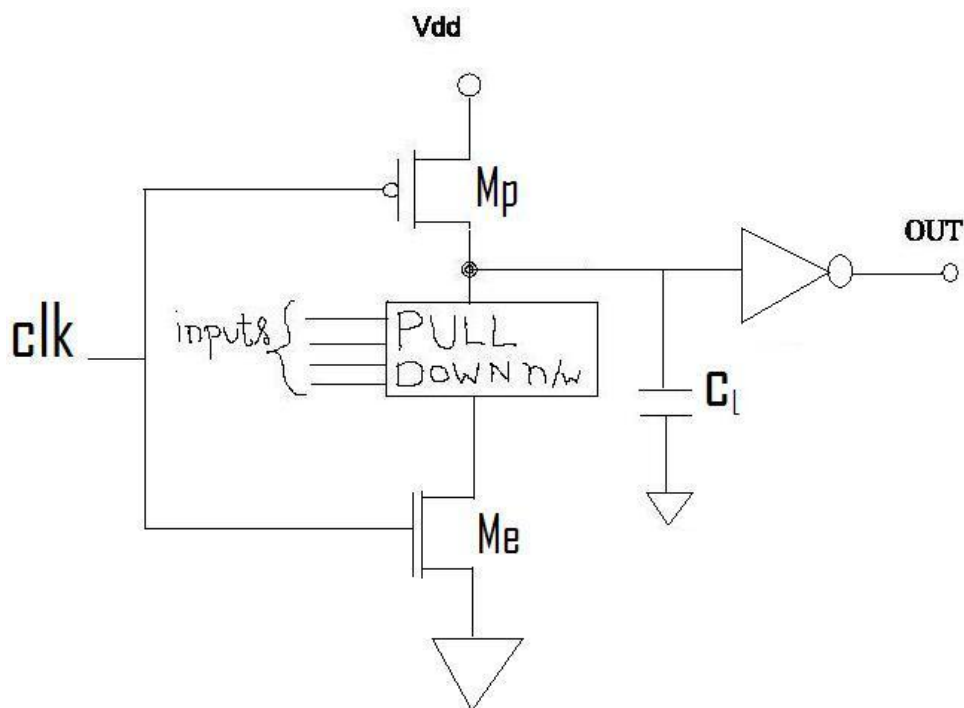


Fig. 1.16 Domino CMOS Logic.

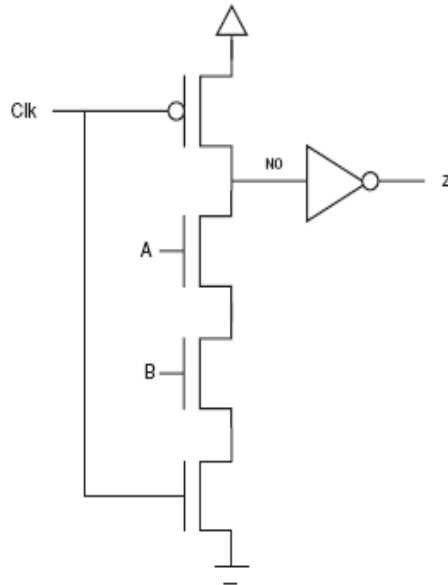


Fig. 1.17 A CMOS domino logic two-input AND gate.

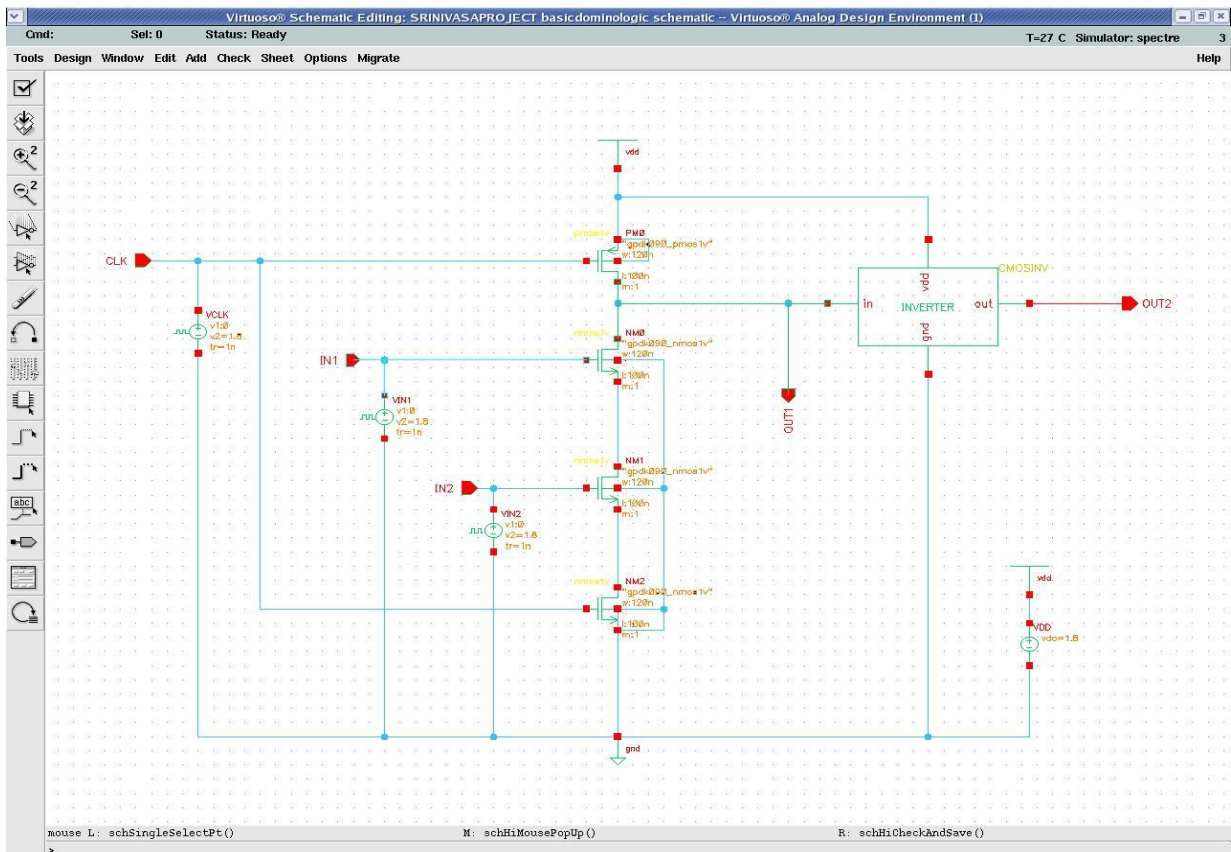


Fig. 1.18 A CMOS domino logic two-input AND gate schematic implementation.

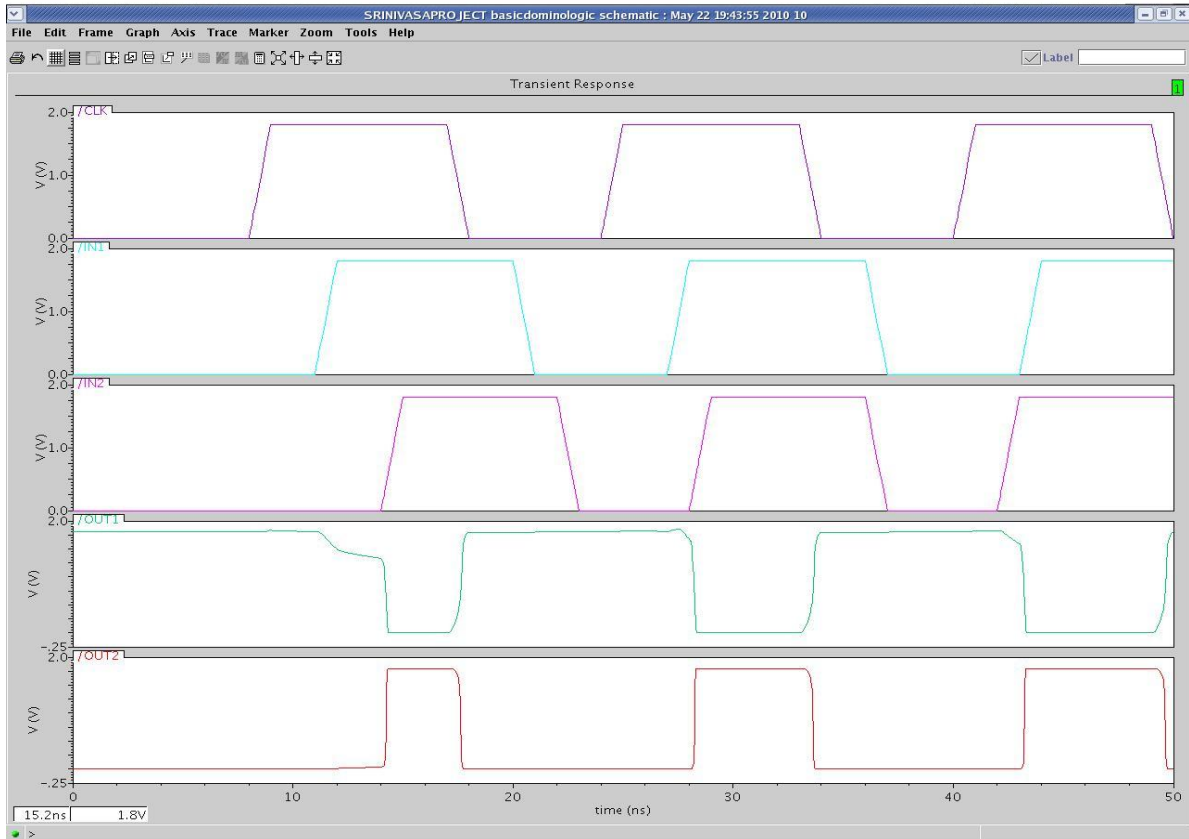


Fig. 1.19 A CMOS domino logic two-input AND gate schematic simulation.

The AND gate shown in Fig. 1.17 can be used to illustrate the functionality, the speed advantage, and also some of the challenges involved in using this logic family. In Fig. 1.17 it can be seen that the two functional inputs, A and B, are also attended by the clock signal, Clk. At first glance this may seem strange, since an AND gate should be a purely combinational circuit, which unlike latches and flip-flops does not require the presence of the clock signal. Domino logic is, however, a clocked logic family, which means that every single logic gate has a clock signal present. When the clock signal turns low, node N0 (which is called the evaluation or internal node or dynamic node) goes high, causing the output of the gate to go low. This represents the only mechanism for the gate output to go low once it has been driven high. The operating period of the cell when its input clock and output are low is called the precharge phase or cycle. The next phase, when the clock is high, is called the evaluate phase or cycle. During the evaluate phase the output of the domino AND cell can go high provided that both inputs A and B are high, which causes the evaluation node, N0, to be driven to a low value. The evaluate phase is the functional operating phase in domino cells, with the precharge phase enabling the next evaluate phase to occur. The appropriate application of the

clock signal ensures that the critical path in domino cells only traverses through cells in the evaluate phase. One of the advantages of domino logic over static logic can also be garnered from the schematic in Fig. 1.17. Since the domino cell only switches from a low to a high direction, there is no need for the inputs A and B to drive any pull-up PMOS transistors.

The lack of a PMOS transistor means that the effective transistor width that loads down a previous stage of logic, for a particular current drive, favours domino over static logic. This is critical since the key to high speed is ensuring that a speed advantage can be gained without loading down the cell greatly.

Advantages:

- (1) This logic allows rail-to-rail swing.
- (2) These Domino logic circuits have smaller areas than CMOS.
- (3) Parasitic capacitances are smaller so that higher operating speeds are possible.
- (4) Operation is free of Glitches as each gate can make only one transition.

Disadvantages:

- (1) Degradation of noise-immunity due to inevitable leakage current and charge sharing.
- (2) Large power consumption especially if compared to the static CMOS logic family.
- (3) Only non-inverting structures are possible because of the presence of inverting buffer.
- (4) Charge distribution may also be a problem.

CHAPTER 2

IMPACT OF TECHNOLOGY SCALING ON THE PERFORMANCE OF DOMINO CMOS LOGIC

2.1 Impact on power consumption

Power consumption is one of the most important constraints in the designing of any dynamic logic circuit. Domino CMOS logic circuit family finds a wide variety of applications in microprocessors, digital signal processors, and dynamic memory due to their high speed and low device count. However, there are inevitable problems that degrade the noise immunity of this family; they are the inevitable leakage current and the charge sharing. Added to the drawbacks is the relatively large power consumption, especially if compared to the static complementary CMOS logic family. To make the matter worse, these drawbacks are more tactile with the scaling of CMOS technology from one generation to the next. In this chapter, the impact of CMOS technology scaling on the performance of domino CMOS logic has been investigated.

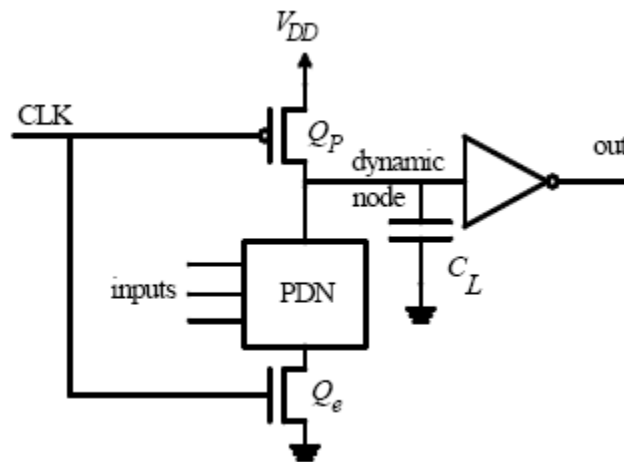


Fig. 2.1 Basic structure of domino-logic circuit.

A simple AND gate is designed using Domino-logic and it is simulated at different technologies.

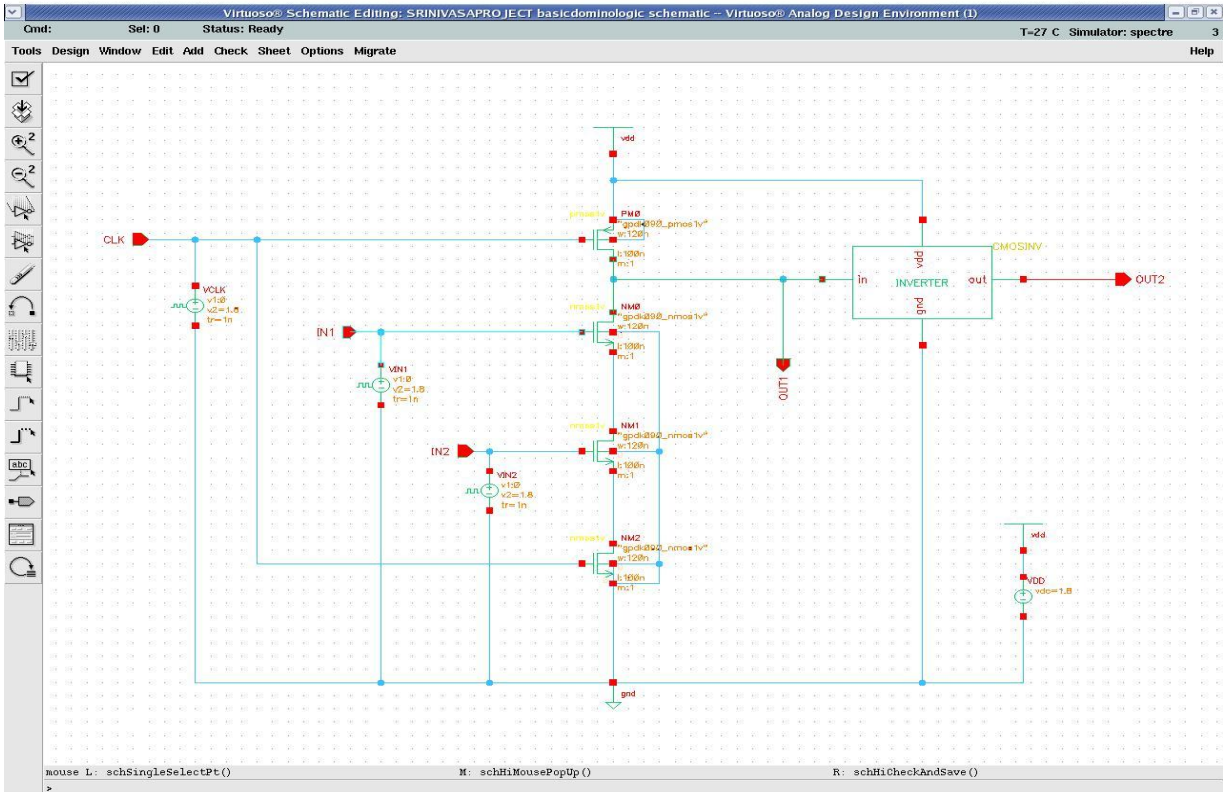


Fig. 2.2 Basic domino AND gate schematic implementation.

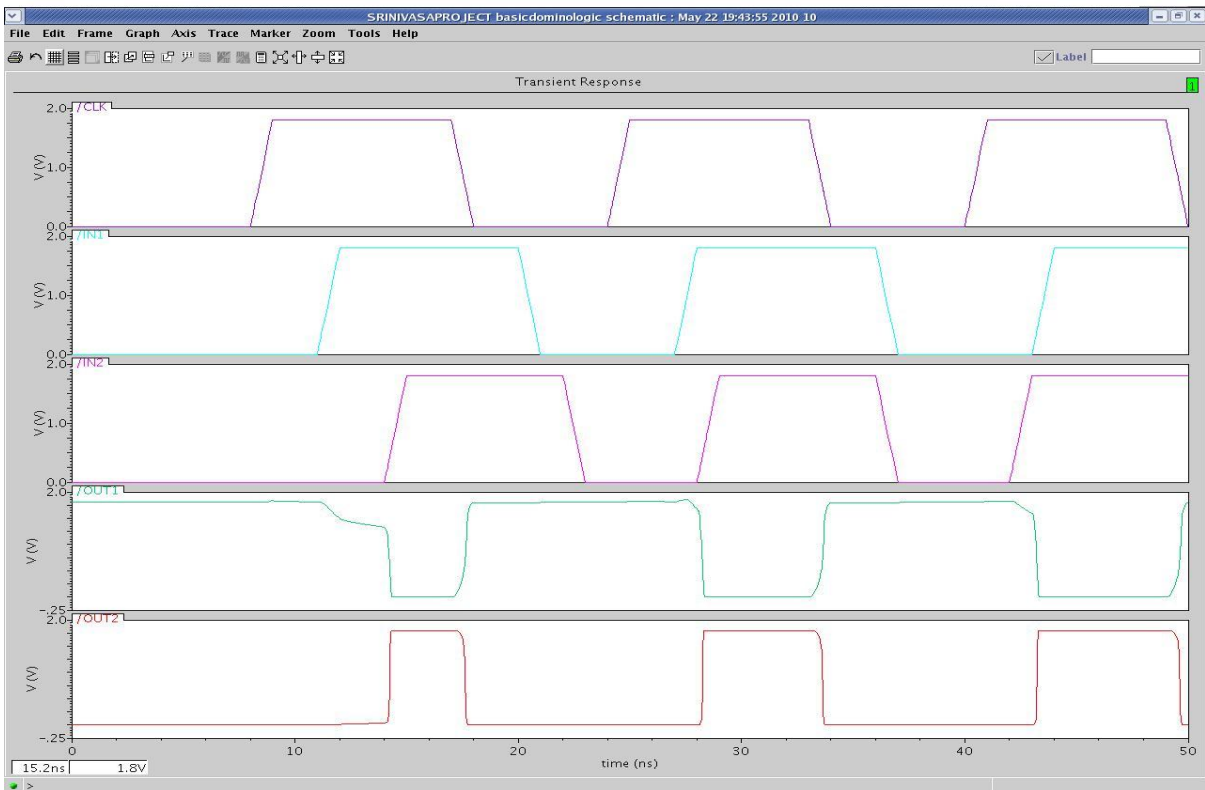


Fig. 2.3 Basic domino AND gate schematic simulation.

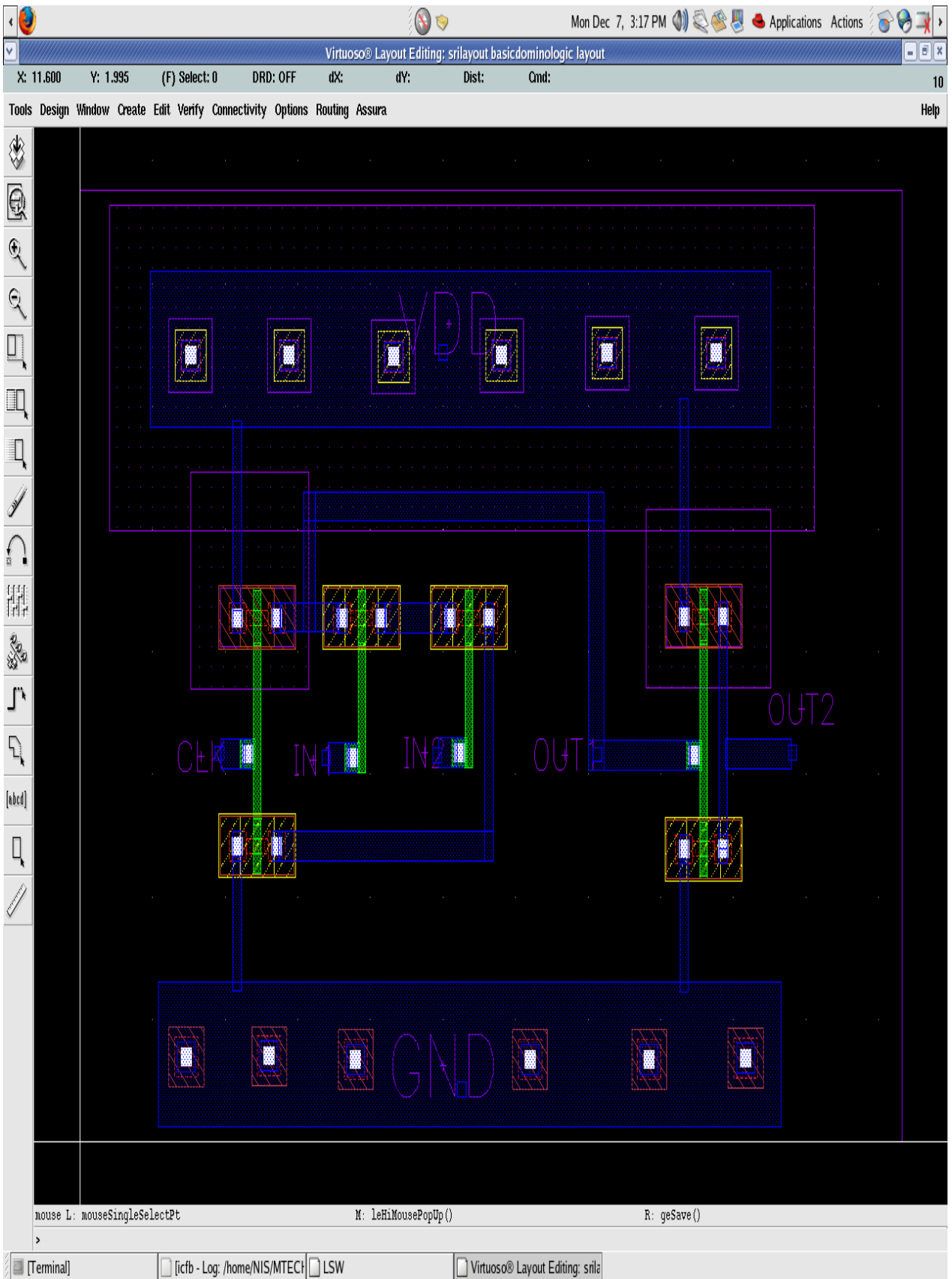


Fig. 2.4 Complete Layout of Basic domino AND gate Schematic.

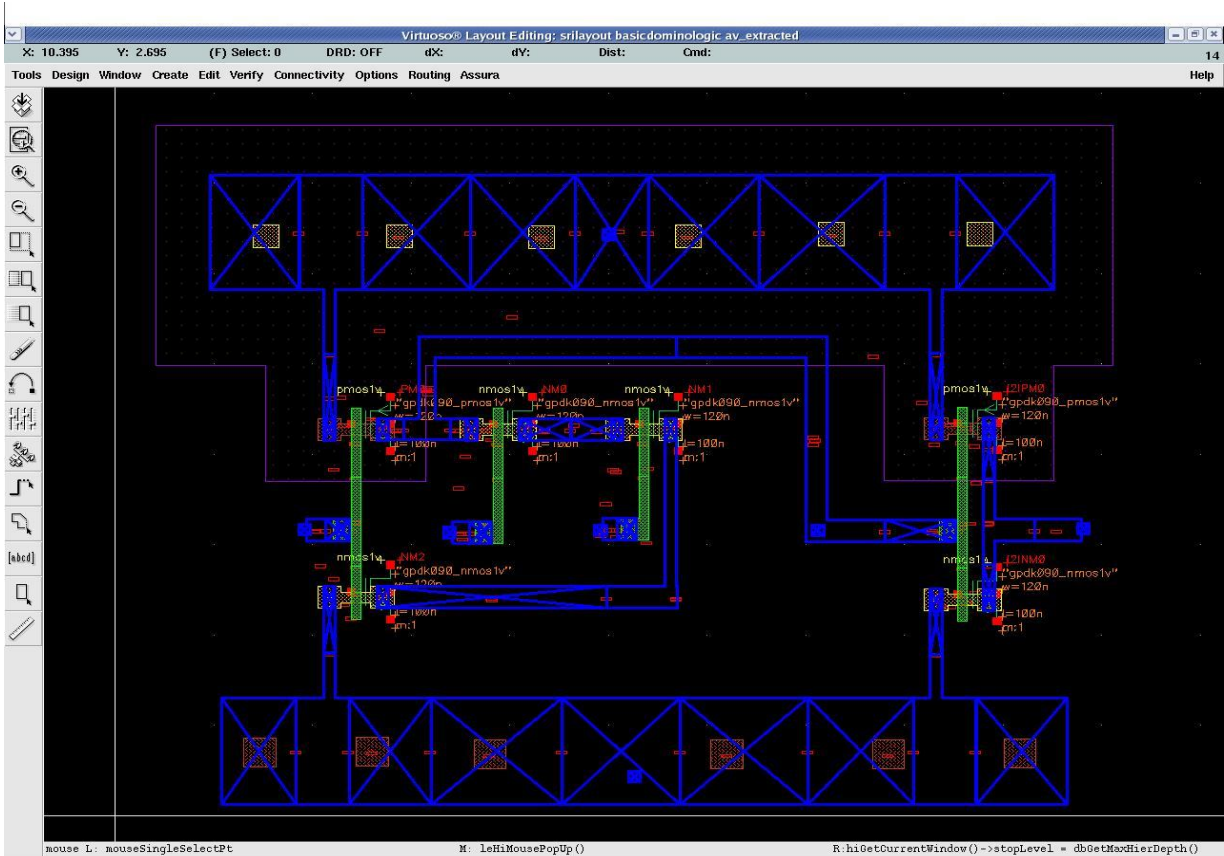


Fig. 2.5 Basic domino AND gate-Extraction of Layout.

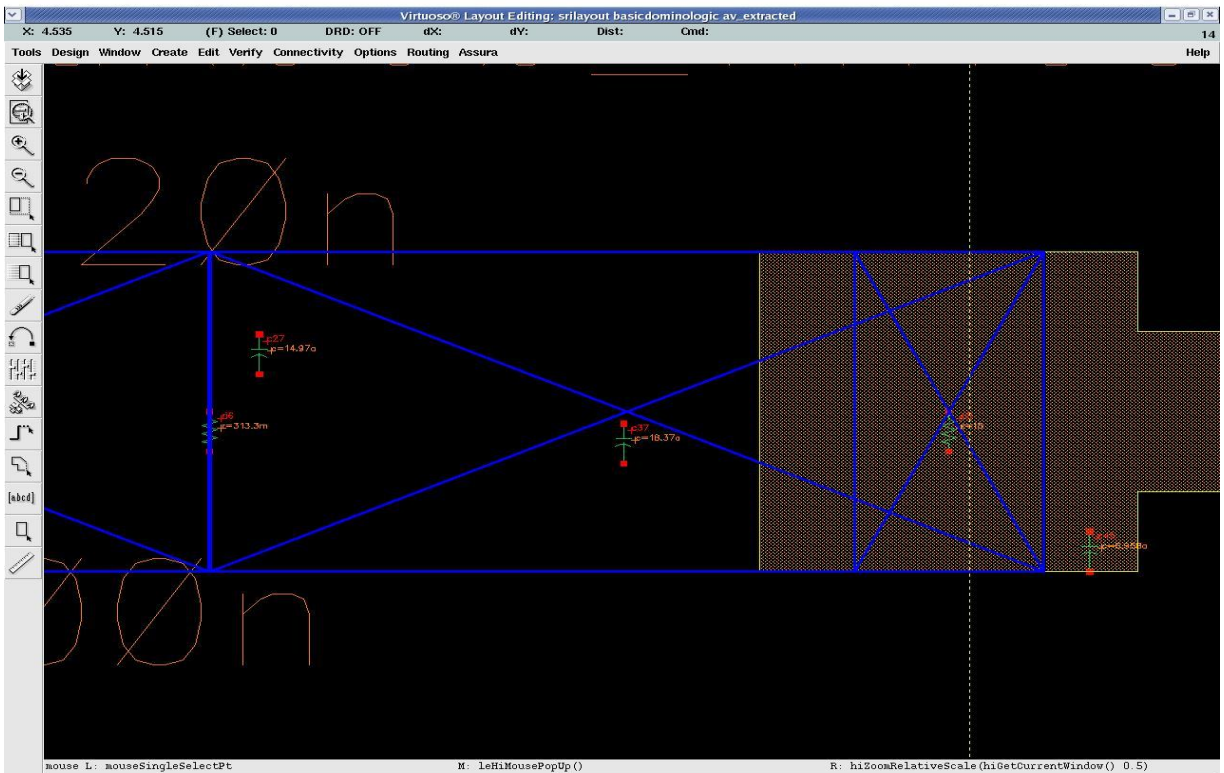


Fig. 2.6 Basic domino AND gate Extraction of Layout-Parasitic components.

After simulating this circuit at different technologies the following observations were made.

TABLE 2.1 Comparison of parameters with technology for Basic Domino AND Gate.

Technology	Power Dissipation (in Pico watts)	Vth(N)(inVolts)	Vth(P)(inVolts)
Tsmc 035.mod	3.375	0.549	-0.680
Tsmc 025.mod	11.663	0.365	-0.562
Tsmc 018.mod	14.538	0.372	-0.394
Ami 12.mod	3.260	0.607	-0.832
Ami 05.mod	3.276	0.708	-0.918

From the above table it is observed that with the down scaling of technology, more power is consumed. Specifically, the need to decrease the dynamic power consumption forces us to use a lower power-supply voltage. This in turn necessitates the reduction of threshold voltage to maintain the performance with the associated increase in sub threshold leakage current. So, a properly sized PMOS keeper must be used to compensate for this leakage. It will be found that the speed, which is the major advantage of domino logic compared to other logic styles, will degrade with CMOS technology scaling due to the contention current of the keeper.

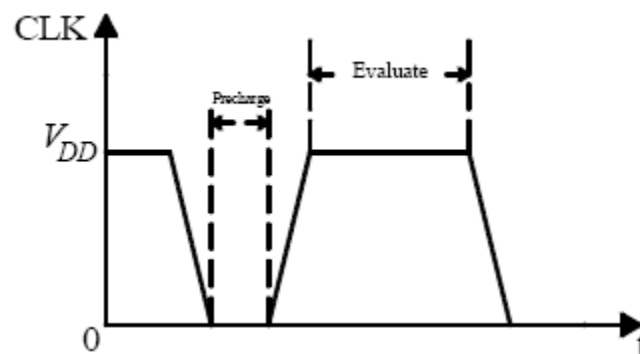


Fig. 2.7 CLK waveform to operate domino-logic circuit.

The basic dynamic domino logic gate is shown in Fig. 2.1. As shown in the Figure, it consists of a pull-down network (PDN) that realizes the desired logic function and there are two switches in series that are periodically operated by the clock signal, CLK whose waveform is shown in Fig. 2.7. CL denotes the total parasitic capacitance between the dynamic node and ground. When CLK is low, QP is turned on, and the circuit is in the precharge phase where the dynamic node charges to VDD . Also, during precharge, the inputs are allowed to change and settle to their proper values. Because Qe is off, no path to ground exists. When CLK is high, QP is off and Qe (known as the footer transistor) turns on, and the circuit is in the evaluation phase.

During the evaluation phase; there are two possibilities for the dynamic-node voltage. If the input combination is one that corresponds to a low output, the dynamic-node voltage must be maintained at the supply voltage, VDD . On the other hand, if the input combination is one that corresponds to a high output, the dynamic-node voltage must be discharged to ground through the conducting NMOS transistors of the PDN.

2.2 PMOS keeper to compensate charge lost

However, it has been assumed in the previous paragraph that there is no leakage of the charge stored on the dynamic node capacitor, CL . In practice, however, there are various sources of leakage during the evaluation phase even if the input combination does not allow discharging of CL . Among these sources are the sub threshold leakages current, the gate tunnelling current, and others. Leakage current is very small but finite. Due to concentration gradient between source and drain terminals of MOSFET, it flows. It is an inevitable problem in dynamic circuits. Also, the charge stored on CL may be shared with one of the drain capacitors associated with one of the NMOS transistors of the PDN for some of the input combinations. So, a PMOS keeper must be used as shown in Fig. 2.8 in order to replenish the charge lost from CL , thus maintaining the noise margin at an acceptable level. However, during the evaluation phase, if CL is to discharge through the PDN, the contention current from the keeper will slow down the discharging process. So, this keeper must be weak.

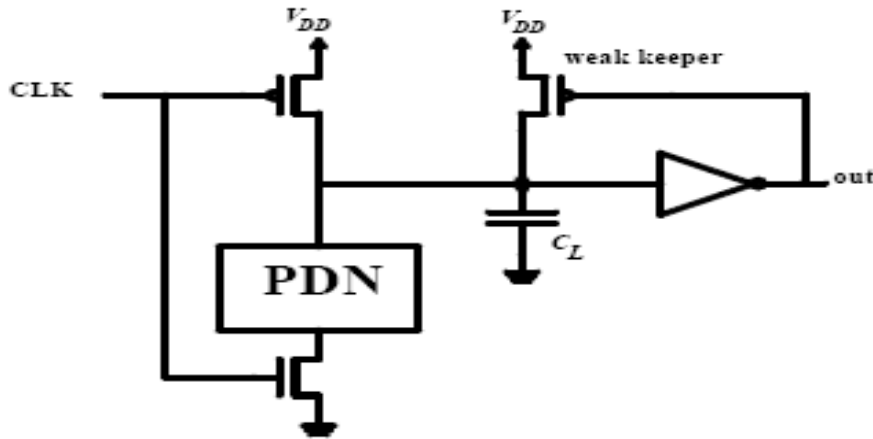


Fig. 2.8 Using a weak PMOS-keeper to replenish charge lost from the CL due to leakage.

It is obvious that the dynamic power consumption, PD , which is the dominant component of power consumption in digital VLSI circuits, is proportional to the square of the power-supply voltage, as evident from

$$P_d = Sfc_L V_{DD}^2 \quad (1)$$

where S is the switching activity factor, f is the switching rate, and CL is the load capacitance. So, reducing VDD has a dramatic effect on reducing the dynamic power consumption.

However, the delay will increase with reducing VDD as evident from the following Equation

$$t_d = \frac{C_L V_{DD}}{K(V_{DD} - V_{th})^\alpha} \quad (2)$$

where α is the velocity saturation index that takes a value of 2 for long-channel devices and a value of 1.3 for short channel devices and K is a parameter that depends on the CMOS technology. So, the threshold voltage needs to be decreased so that td will not be adversely affected by reducing VDD . This in turn leads to an exponential increase in I_{sub} . This forces the designer to use a larger than minimum-sized keeper in order to compensate for the relatively large leakage current. During the evaluation phase, if CL is to discharge to 0 V, then there are two possibilities. The first one is that the discharging of CL will slow down due to the keeper contention current. The second possibility is that CL will not discharge at all if the contention current is larger than the discharging current.

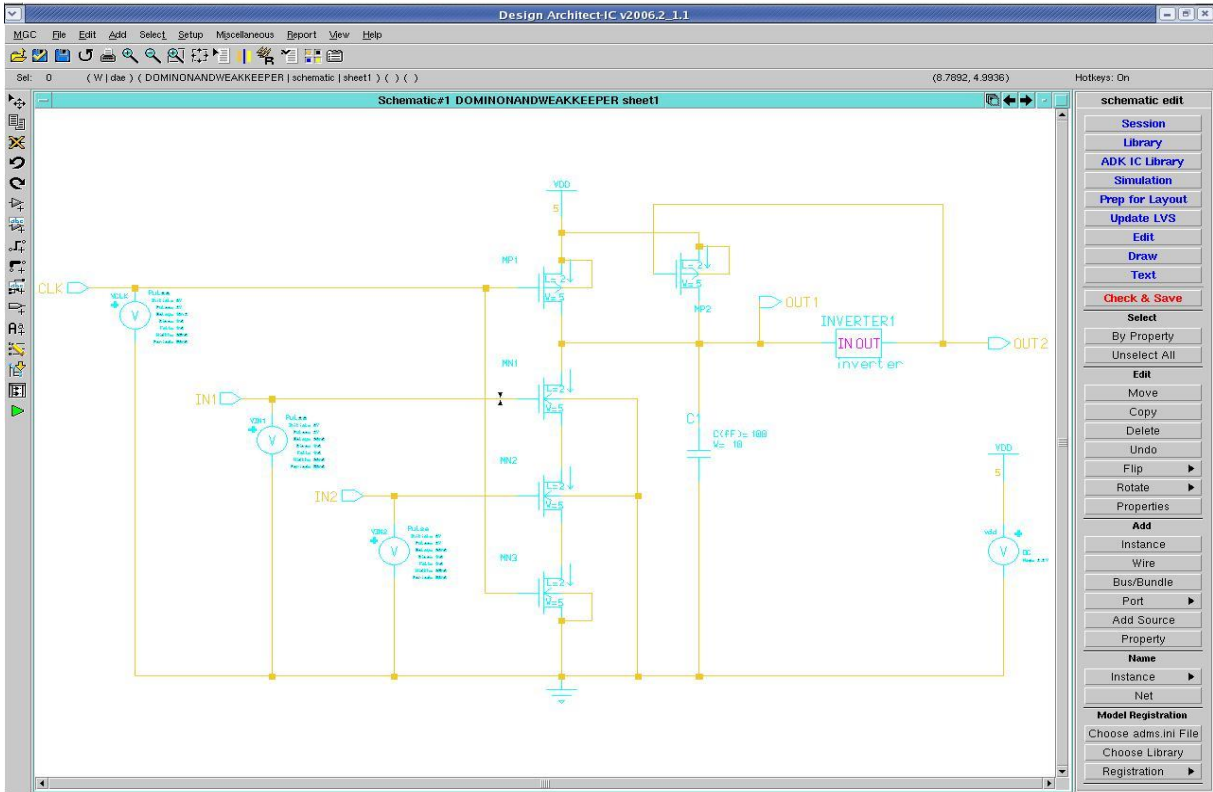


Fig. 2.9 Basic domino AND gate-using PMOS-keeper schematic implementation.

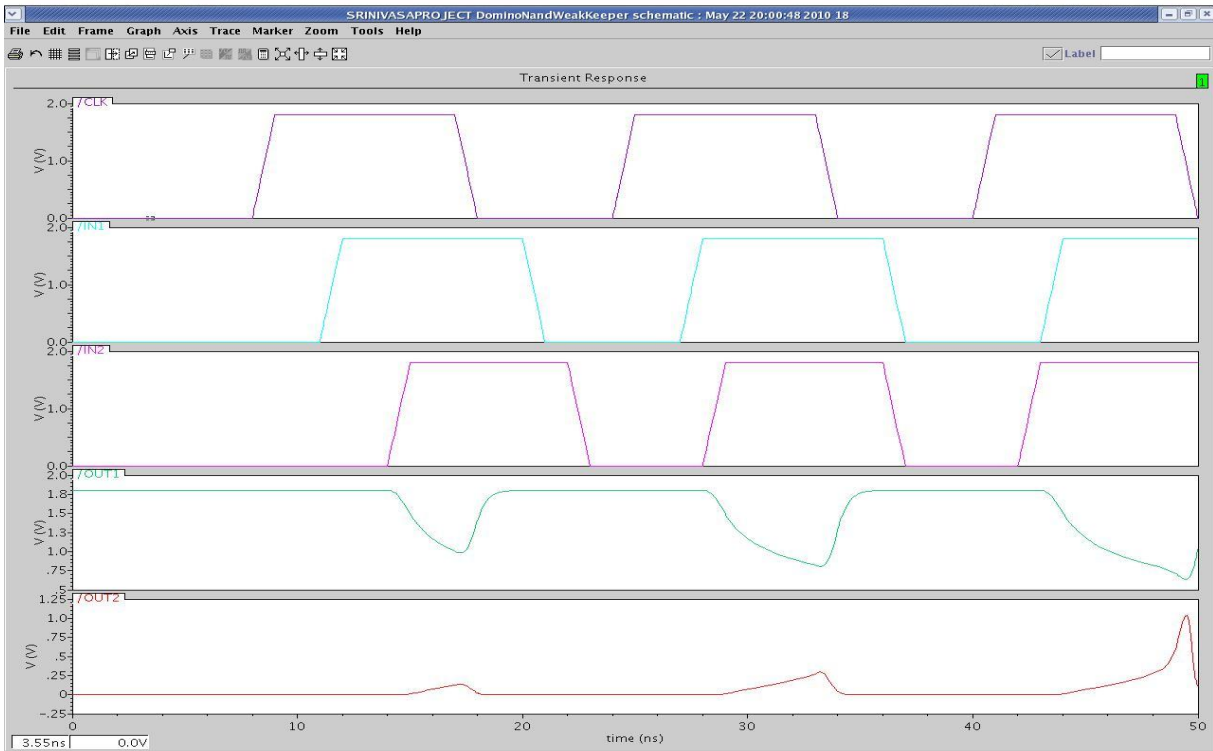


Fig. 2.10 Basic domino AND gate-using PMOS-keeper schematic simulation.

After simulating this circuit at different technologies the following observations were made.

TABLE 2.2 Comparison of parameters with technology for Basic Domino AND Gate using PMOS Keeper.

Technology	Power Dissipation (in Pico watts)	Vth(N)(inVolts)	Vth(P)(inVolts)
Tsmc 035.mod	22.086	0.549	-0.680
Tsmc 025.mod	38.682	0.365	-0.562
Tsmc 018.mod	60.856	0.372	-0.394
Ami 12.mod	21.896	0.607	-0.832
Ami 05.mod	21.880	0.708	-0.918

Conclusions from PMOS keeper circuit:

- (1) The need for reducing the dynamic power consumption necessitates the reduction of VDD . In order to maintain the performance, the threshold voltage must be reduced.
- (2) The reduction of the threshold voltage causes the sub threshold leakage current to increase exponentially, thus forcing us to use a larger than minimum-sized PMOS keeper. This, of course, increases the contention current of the keeper during the evaluation phase leading to slowing down the discharging process.
- (3) It can also be concluded that with scaling down the CMOS technology, domino CMOS logic will lose its fundamental advantage; the speed, especially if compared with other logic styles. This problem is imperative especially for applications that require the use of a relatively large number of NMOS transistors in parallel in the PDN with the subsequent increase in I_{sub} .

CHAPTER 3

THREE PHASE DOMINO LOGIC

3.1 Introduction

The speed and area advantage of domino logic circuits compared to static logic circuits makes them a favourite choice for the critical path of high performance processors. However they suffer from low noise margin. Noise is not scaling at the same rate as the supply voltage therefore new domino logic circuits are required to increase the noise margin. In this chapter a new domino circuit is introduced. The noise margin can also be increased with the less reduction in the gate speed.

The scaling trend of MOSFETs requires the supply voltage and the threshold voltage to be reduced. Scaling is required to reduce power and increase the speed. However as devices are scaled noise is becoming a more important issue. Noise is increasing because of higher switching speeds, capacitive/inductive noise coupling and fluctuation of device parameters.

Domino logic families are extensively used in high speed processors. They are faster than static logic families and consume less space on the silicon. However scaling requires lower threshold voltage which results in lower noise margin for domino logic families. Therefore domino logic circuits which have smaller noise margin compared to static logic circuits are more susceptible to noise for future generations. Thus noise margin needs to be increased, but the process of increasing noise margin will reduce gate speed. Therefore a novel technique is introduced to increase the noise margin of delayed domino logic circuits with a small impact on the speed. Using this circuit the charge sharing noise is limited and the crosstalk noise which is also one of the most important sources of noise in digital circuits can be controlled.

3.2 Noise Margin

Noise Margin (NM) of a circuit is defined as the maximum noise voltage that can be tolerated by the circuit. Two kinds of noise margin are defined:

- (1) Static noise-margin.
- (2) Dynamic noise-margin.

- (1) Static noise margin: The amount of DC noise voltage, which can be tolerated. Static noise margin is only a function of the noise voltage level.
- (2) Dynamic noise margin: The amount of noise voltage, which can be tolerated. It is a function of amplitude, shape and duration.

In static logic circuits the inputs affect the circuit at any time and the noise may have any duration. In worst-case it is assumed that a DC noise is on the input of the circuit, and therefore, the static noise margin is used to calculate the worst-case noise margin of static circuits.

Limiting the duration in which the logic is sensitive to the inputs, or in other words limiting the evaluation time, will result in a higher noise margin, because the noise has limited time to affect the output.

To be able to limit the evaluation time we must know

- (1) When are all of the inputs to a logic gate ready?
- (2) How much is the delay of the logic gate?

If the evaluation time is limited in a logic family then the duration in which the circuit is affected by the inputs is limited and as a result the noise duration is limited. In this case the dynamic noise margin should be used. The dynamic noise for this gate is shown in Fig. 3.1 which is a pulse with duration equal to the evaluation phase.

The proposed logic family should have three phases (Fig. 3.2). The first phase is the precharge phase. In this phase the input should not affect the output and the circuit gets ready for the evaluate phase to start. The evaluation phase begins when all of the inputs to that stage are ready. In this phase the output changes depending on the input and the logic performed in the circuit. This phase is the only phase that the circuit is affected by the inputs. Therefore noise may affect the output of the circuit only in this phase. After the evaluation phase the save phase begins. In this phase the evaluated value is saved for the next stages of the circuit. The circuit should be designed so that it is not affected by the inputs in the save phase. In the next section a new circuit is designed to implement the three required phases.

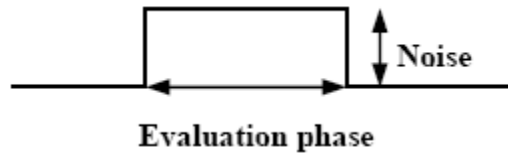


Fig. 3.1 Noise shape.

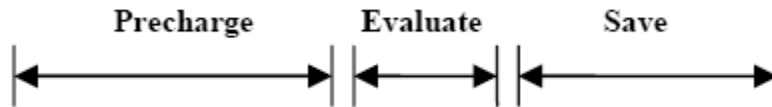


Fig. 3.2 Three phases of gate.

3.3 Implementing the Three Phase Domino (TP-Domino) logic

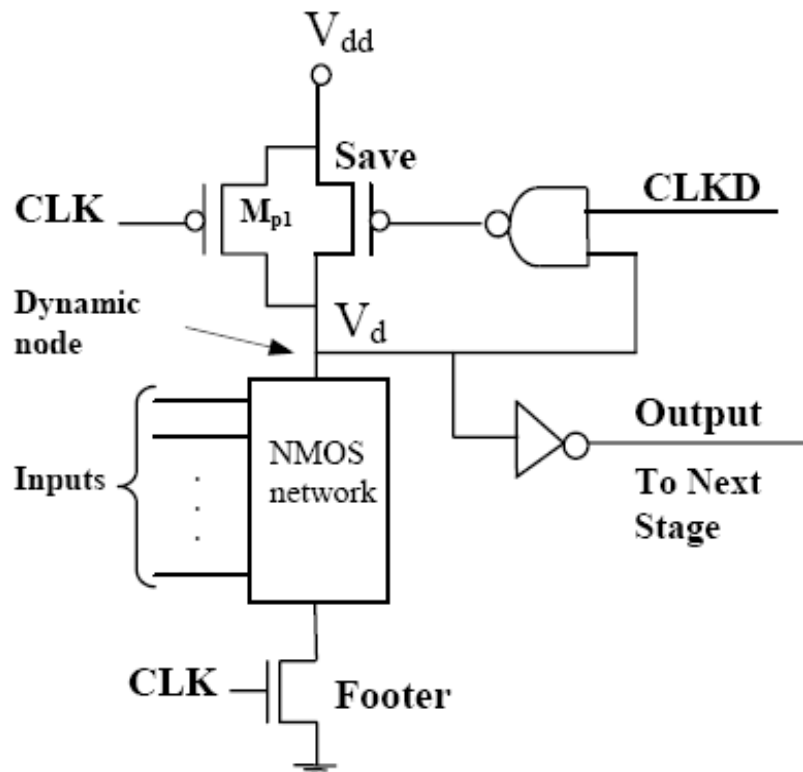


Fig. 3.3 Three phase Domino logic circuit.

There is a family of domino logic circuits named Clock- Delayed Domino (CD-Domino) logic in which, a clock signal is propagated in parallel to the logic network. Therefore the clock of each stage is the delayed form of the clock of the previous stage. In this logic family the evaluation starts by the rising edge of the clock for that stage. The clock delay of each gate is designed so that it arrives when all of the inputs to that gate are ready. By a small change in CD-Domino we are able to implement the three phases.

Fig. 3.3 shows the Three Phase Domino circuit. In this circuit CLKD is the delayed form of the CLK signal (Fig. 3.4), the Save PFET transistor is larger than the normal keeper transistors used in conventional domino gates and the NOT is changed by a NAND gate.

(1) During Precharge phase:

The footer transistor is off and Mp1 is on therefore the dynamic node is charged to Vdd which is the same as the precharge phase in CD-Domino. The footer transistor is off therefore the inputs have no affect on the dynamic node in this phase.

(2) During Evaluation phase:

The CLK signal changes to one turning off Mp1 and turning on the footer transistor. Therefore the evaluation is done depending on the inputs and the logic of the gate. The pull-down transistors can discharge the dynamic node very fast because both of the PFETs are off in this phase.

(3) During Save phase:

This phase starts when CLKD changes to Vdd. When CLKD changes to Vdd, the NAND acts as a NOT gate. Therefore if the dynamic node is discharged, the output of the NAND stays one and as a result the save transistor remains off. On the other hand if the dynamic node is not discharged the NAND output changes to zero which turns on the save transistor. Thus the dynamic node is connected to Vdd through the PFET save transistor. If the dynamic node is discharged the inputs can not affect the dynamic node voltage because it is not able to charge it again and if it is not discharged the save transistor is strong enough to keep the dynamic node voltage to be larger than the threshold voltage of the NAND gate. Therefore in either case the output of the gate does not change when the inputs change in the save phase.

The width of the noise pulse is determined by the evaluation time. The noise pulse causes the dynamic node to drop as shown in Fig. 3.5. This figure shows two cases. The first case is when the input is less than the low NM. In this case the output drops but the voltage drop is less than the high noise margin of the NAND gate. Therefore in the save phase, the save transistor restores the dynamic node to V_{dd}. In the second case the input is larger than the low NM. Therefore the voltage drop of the dynamic node is more than the high NM of the NAND gate and as a result it is not restored.

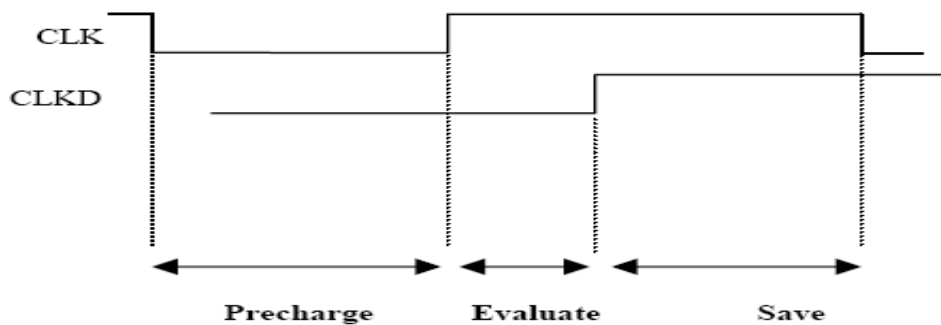
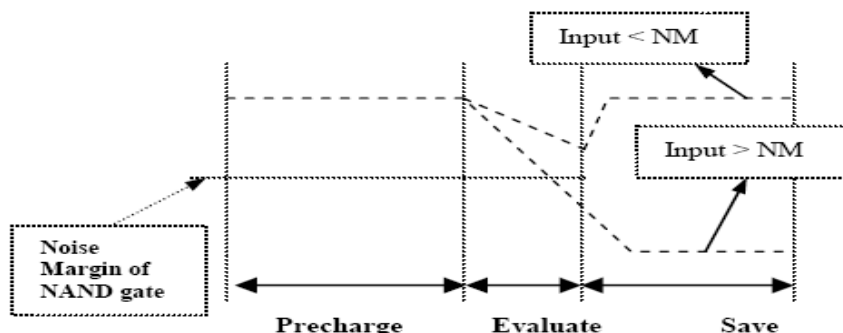


Fig. 3.4 Clock signals of Three phase Domino logic circuit.

The save transistor is off in the evaluate phase. Therefore in the evaluate phase it acts as a parasitic capacitance. On the other hand there is no keeper transistor which is used in normal clock delayed dynamic logic circuits. Therefore the delay compared to the delay of CD-domino may be either higher because of the added parasitic capacitors of the save transistor or lower because of omitting the keeper transistor.



**Fig. 3.5 Outputs for two different inputs,
1) Input < NM 2) Input > NM the input is one.**

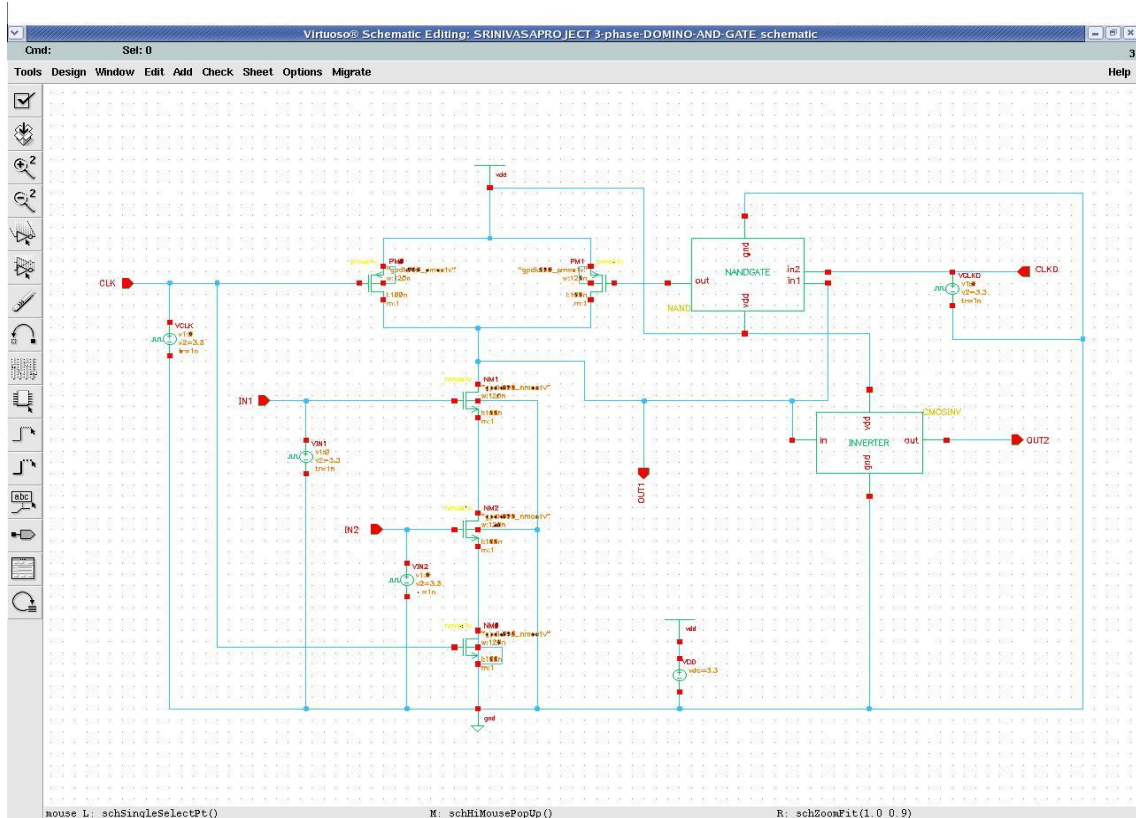


Fig. 3.6 Three phase Domino AND gate schematic implementation.

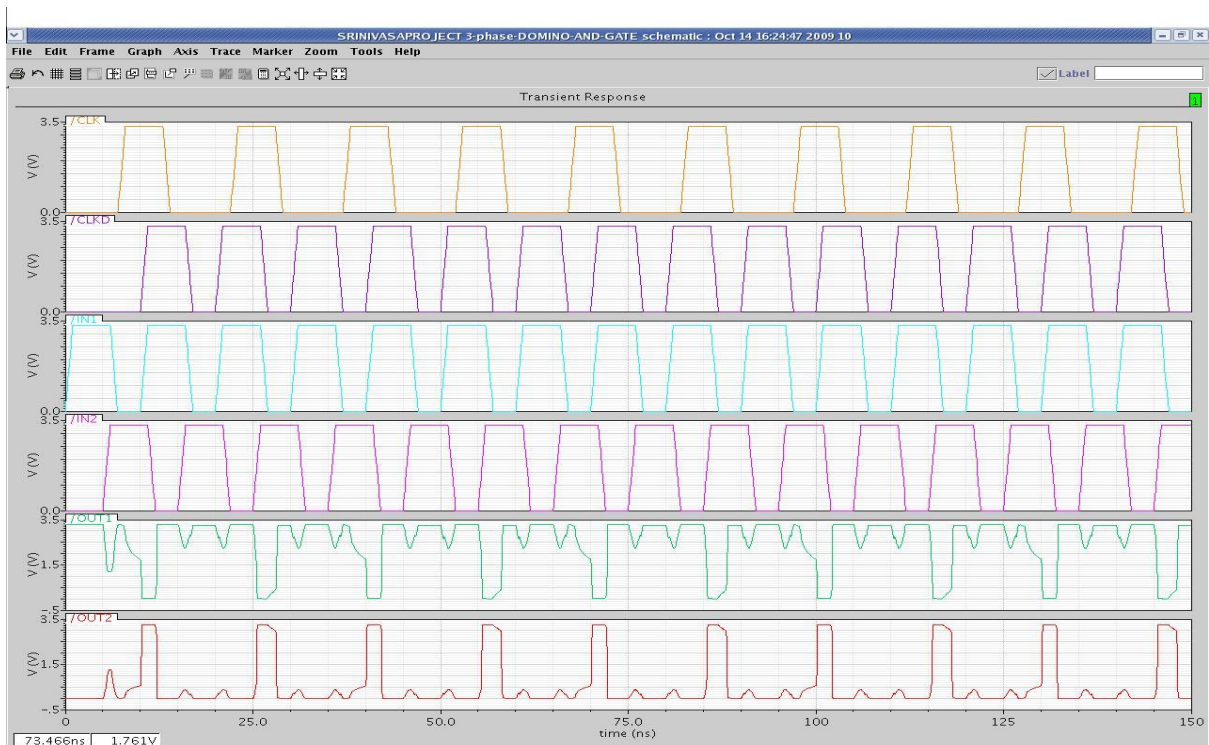


Fig. 3.7 Three phase Domino AND gate schematic simulation.

Observations from Simulation:

- (1) In Precharge phase Footer is 'OFF' and Mp1 is 'ON', thus dynamic node is charged to Vdd. Therefore inputs have no impact on output.
- (2) In Evaluation phase Footer is 'ON' and both Mp1 & SAVE transistor are 'OFF'. Since Footer can discharge dynamic node very fast, because Mp1 & SAVE transistor are 'OFF'.

Mp1 is clearly 'OFF' since CLK = '1' in evaluation phase.

But how is SAVE transistor also 'OFF'? (In Evaluation phase)

Since in Precharge mode dynamic node is charged to Vdd (say '1' logically) and is given to NAND gate through output. CLKD is delayed version of CLK. Therefore

CLKD in Evaluation mode = CLK in Precharge mode ('0').

⇒ CLKD = '0' and

⇒ dynamic node = Vdd (logic '1').

⇒ This Vdd is again given to NAND gate

⇒ Thus output of NAND gate = '1' and it is given as input to SAVE transistor (P-MOSFET)

⇒ Hence SAVE transistor is also 'OFF'

In this way both Mp1 & SAVE transistor are 'OFF'. In this mode SAVE transistor acts as a parasitic capacitance.

- (3) Save phase started when CLKD changed to Vdd (CLKD = Vdd). Here one input of NAND gate is always 'HIGH' (say '1' logically), hence NAND gate acts as a 'NOT' – gate.

In this phase the circuit operates as follows.

- (a) If dynamic node is discharged (say '0' logically) for all inputs are high to NMOS-PDN, then output of NAND gate is '1'. Thus SAVE transistor is 'OFF'.
- (b) If dynamic node is charged to Vdd (say '1' logically), then output of NAND gate is '0'. Thus SAVE transistor is 'ON'. This means dynamic node is connected to Vdd through SAVE transistor.

- (c) If dynamic node is discharged, then the inputs cannot affect the dynamic node voltage, because it is not able to charge it again.
- (d) If dynamic node is not discharged, then the SAVE transistor is strong enough to keep the dynamic node voltage to be larger than the threshold voltage of NAND gate.

Thus in SAVE mode inputs do not affect output. The value, which has been evaluated in 'Evaluation mode', remains same on output. It may be either '0' or '1'.

In Fig. 3.8 an input equal to V_{dd} is applied therefore in the evaluation phase the dynamic node drops to zero and the output of the circuit changes from zero to V_{dd} . The output of the NAND gate remains at V_{dd} , as a result the save transistor stays off.

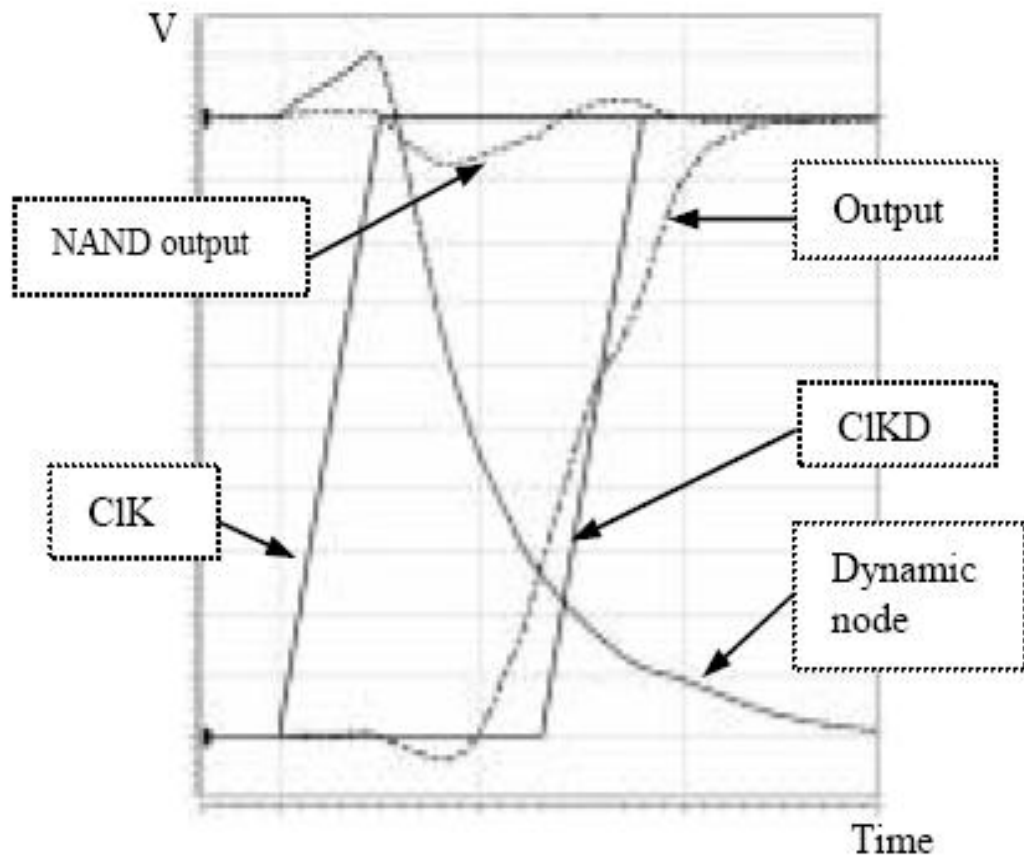


Fig. 3.8 Simulation outputs when input is 'ONE'.

In Fig. 3.9 shows the signals of the same gate when zero is applied to the input. In this case the dynamic node remains at Vdd and the output remains at zero. The output of the NAND gate changes from Vdd to zero which turns on the save transistor and as a result the dynamic node is connected to Vdd by the save transistor.

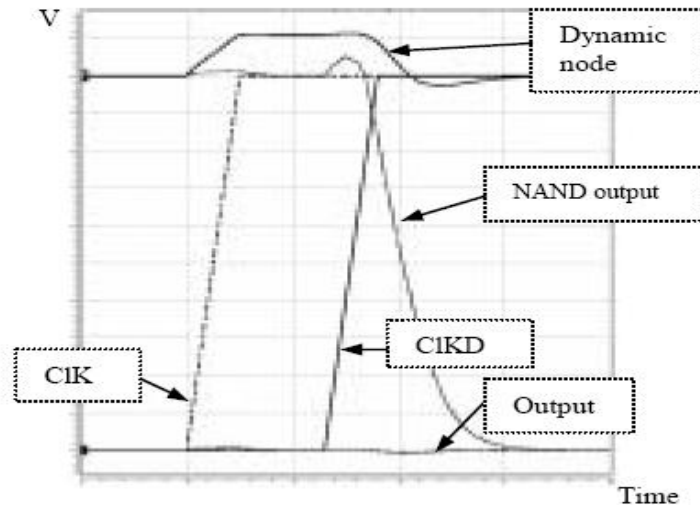


Fig. 3.9 Simulation outputs when input is 'ZERO'.

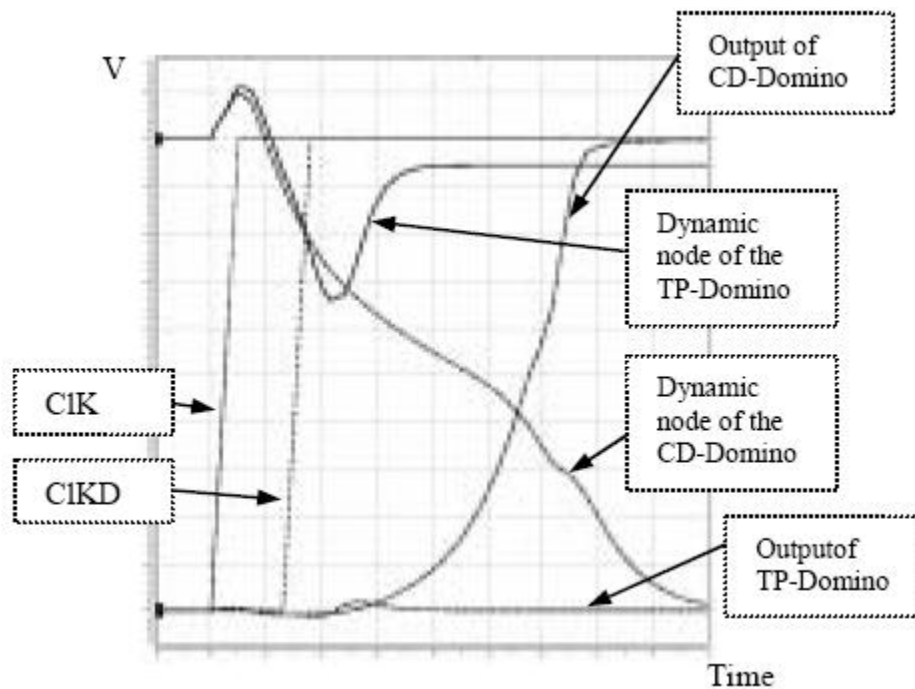


Fig. 3.10 Outputs of the Three-Phase Domino and clock delayed domino for an input noise.

Fig. 3.10 shows the output of a CD-Domino 3-input AND gate and the output of the TP-Domino 3-input AND gate when noise is applied in the input. As shown the dynamic node of the CD-Domino logic drops to zero but the output of the TP-Domino circuit is charged to V_{dd} when the save phase is turned on. In this case the output of the CD-Domino logic switches but the output of the TP-Domino logic remains at zero.

The noise margin of the circuit can be determined by the evaluation time and the noise margin of the NAND gate. Reducing the evaluation time increases the low noise margin and reduces the high noise margin and vice versa.

3.4 Sources of Noise

There are different sources of noise in deep submicron technology circuits. They are

- (1) Crosstalk,
- (2) Charge sharing,
- (3) Leakage current, and
- (4) Small variations of nominal supply voltage values.

(1) Crosstalk Noise:

Crosstalk noise occurs on a wire when the neighbouring wire switches. The switching wire is called the aggressor and the other one is called the victim wire. It occurs because of the capacitance coupling of the wires. Therefore this kind of noise occurs when the aggressor wire switches and therefore, it is not a random noise. In these kinds of circuits the output switches in the evaluation phase and it is only sensitive to the input in this phase. Therefore for each input wire the phase at which it is sensitive to noise is known and for each output wire the switching time is known. The crosstalk noise can be eliminated by not laying out the aggressor output wires and the victim input wires with overlapping evaluation phases. Even if the layout is done automatically, it can be easily implemented in the CAD tool. By using this technique the crosstalk noise which is the largest noise source can be easily eliminated for these kinds of circuits.

(2) Charge Sharing Noise:

Charge sharing noise happens because of sharing charge between the dynamic node and the parasitic capacitors within the gate. It reduces the charge on the dynamic node and as a result it reduces the dynamic node voltage. In Three Phase Domino logic circuits the inputs of each stage change when the circuit is in the precharge phase. At the precharge phase the dynamic node is connected to Vdd through Mp1 which is a large PFET transistor. Therefore the charge sharing noise is much smaller in TP-domino compared to other domino logic families.

(3) Leakage current:

Domino logic circuits are sensitive to leakage current. The leakage current of the NFET transistors discharges the charge on the dynamic node in the evaluation phase. A small keeper is used to prevent the dynamic node voltage from dropping. As transistors are scaled the leakage current is increased, therefore a small keeper might not be enough to keep the charge on the dynamic node. In the TP-Domino the time in which the dynamic node may be discharged by the leakage current of the NFET transistors is limited. In the precharge phase the dynamic node is connected to Vdd through Mp1 which is a large PFET transistor. Therefore the leakage current has no effect on the dynamic node charge in this phase. In the save phase if the dynamic node voltage is one it is connected to Vdd through the save transistor which also is a large transistor. Therefore the leakage current has no affect in the precharge and the save phase. It can only affect the dynamic node in the evaluation phase. The duration of the evaluate phase is comparable to the delay of the gate. The leakage current of a transistor is very small compared to the on current. Therefore the voltage drop caused by the leakage current during the evaluation phase is negligible. As a result no keeper transistor is needed in this kind of domino logic circuits.

Advantages:

- (1) Domino logic circuits are extensively used in the critical path of high performance processors.
- (2) Speed and area advantage of this family of logic circuits compared to static logic circuits makes them a favourite choice.
- (3) The Three-Phase circuit does not suffer from leakage current.
- (4) It is not sensitive to charge sharing noise which is an important source of noise in dynamic logic circuits.
- (5) The crosstalk noise which is the biggest source of noise can also be eliminated by applying some simple rules when laying out the wires.

Disadvantages:

- (1) Three phase Domino logic circuits suffer from their low noise margin.

CHAPTER 4

HIGH PERFORMANCE NOISE-TOLERANT CIRCUIT TECHNIQUES FOR CMOS DOMINO LOGIC

4.1 Introduction

Dynamic CMOS gates are widely exploited in high-performance designs because of their speed. However, they suffer from high noise sensitivity. The main reason for this is the sub-threshold leakage current flowing through the evaluation network. This problem becomes more and more severe with continuous scaling of the technology. A new circuit technique for increasing the noise tolerance of dynamic CMOS gates is designed. A comparison with previously reported schemes is presented. Simulations proved that, when 90 nm CMOS technology is used to realise wide fan-in gates, the proposed design technique can achieve the highest level of noise robustness.

Owing to the aggressive scaling down of the technology to the deep sub-micrometer regime, noise immunity is becoming a very important issue in the design of VLSI chips. The term 'noise' in digital integrated circuits generally refers to any possible event that may cause the voltage at a node to vary from its nominal value. There are different sources of noise in deep-submicron circuits. They are mostly related to crosstalk, small variations of the nominal supply voltage value, charge sharing and leakage current. The leakage current is the most critical, since in digital circuits it exponentially increases with the continuous shrinking of the MOS transistor dimensions. In fact, in order to limit dynamic energy consumption, the supply voltage is reduced in each new technology node. At the same time, the threshold voltage (V_{TH}) of the MOS transistor is scaled down to assure high performance. As a consequence, the sub-threshold leakage current continually increases, since it is exponentially dependent on $-V_{TH}$. Furthermore, the continuous reduction of the gate oxide thickness causes an exponential increase of the gate leakage current because of the enhanced tunnelling of the carriers through the oxide itself.

Together with the increase of transistor density, specific design styles have also been aggressively exploited in order to achieve high performance. Here, it is the case of the domino logic design style, which is faster than the static CMOS. Moreover, domino gates are more compact, especially when they have a wide fan-in. Wide fan-in domino gates are often employed in the critical path of high-performance chips, such as in general purpose microprocessors or digital signal processors. As an example, wide fan-in OR gates and MUXs are used in the design of high-performance register files.

Domino gates suffer from higher noise sensitivity than their static CMOS counterparts. This is because of their low switching threshold voltage, which is equal to the V_{TH} of the pull-down NMOS devices. Noise immunity has become a great concern, especially in the design of high fan-in gates. This is because of the high number of transistors and circuit branches, which cause more possible paths for gate and sub-threshold leakage currents.

Recently, several techniques have been proposed to reduce the leakage noise sensitivity of high fan-in footless domino gates. All the existing techniques improve the noise robustness of domino gates at a significant cost in terms of delay or energy consumption. Moreover, the degradation in speed and the increase in energy dissipation seem to become more and more troublesome with continuous technological progresses.

In this chapter, a new technique is proposed to increase the noise immunity of dynamic gates with minimal energy and delay penalties.

4.2 Different high-performance noise tolerant circuit techniques

4.2.1 Wide fan-in Domino OR gate-Footless scheme

In Fig. 4.1, a typical wide fan-in domino OR gate-footless scheme is depicted. The footless scheme is often exploited in high-performance circuits because the discharge of the dynamic node is faster and the capacitive load of the clock line is reduced. The operation of a domino gate is managed by the clock signal.

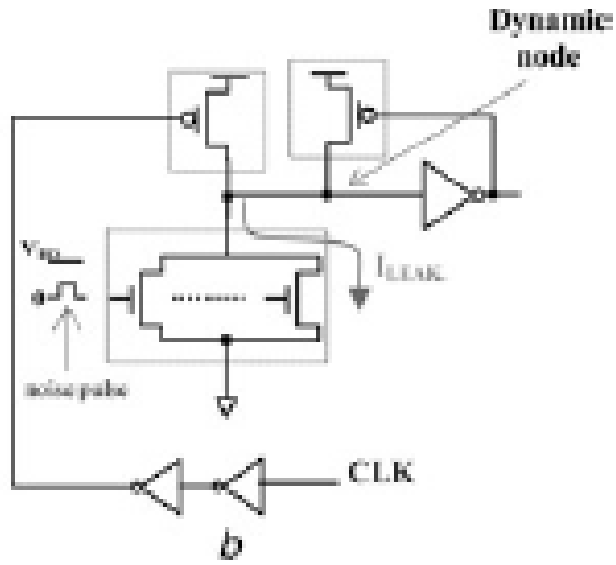


Fig. 4.1 Wide fan-in Domino OR gate-Footless scheme.

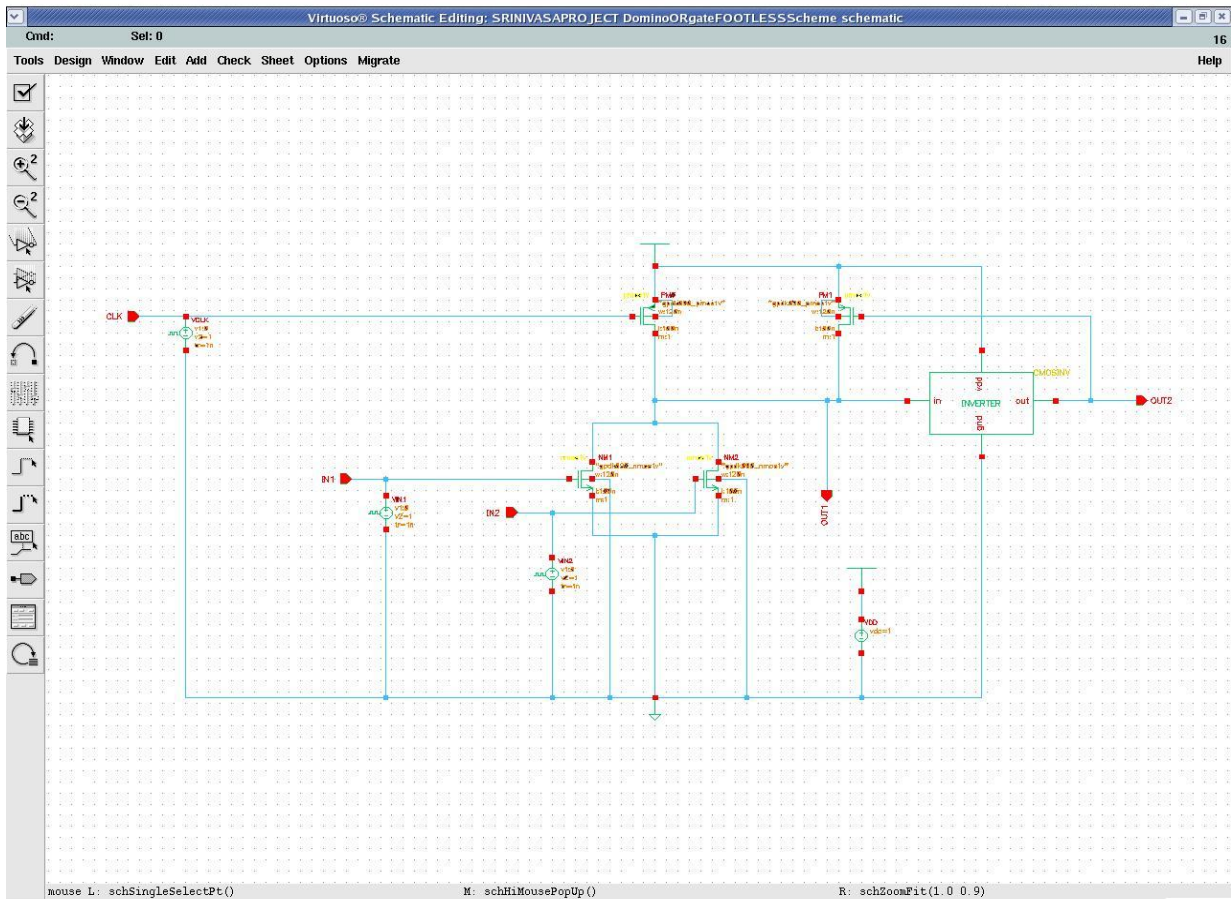


Fig. 4.2 Wide fan-in Domino OR gate-Footless schematic implementation.

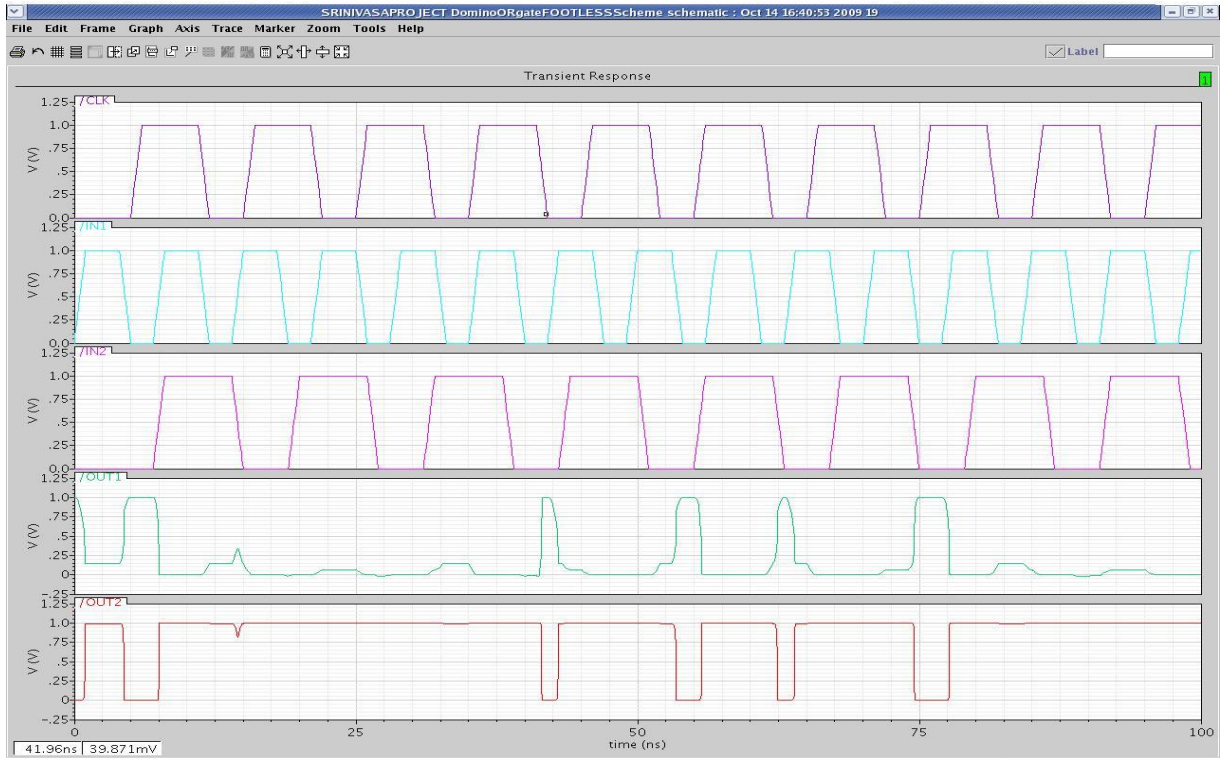


Fig. 4.3 Wide fan-in Domino OR gate-footless schematic simulation.



Fig. 4.4 Wide fan-in Domino OR gate-Footless schematic-Leakage current simulation.

During precharge (CLK = '0'):

The pre-charging PMOS charges the dynamic node up to vdd.

During Evaluation phase (CLK = '1'):

The dynamic node is no longer constantly connected to VDD through the pre-charge PMOS. Only the keeper provides a connection to VDD until OUT goes high. This event could be forced by the sub-threshold leakage currents. In fact, even with all the inputs low, the leakage currents flowing through the NMOS pull-down network (PDN) could discharge the dynamic node. This effect is enhanced if a noise voltage pulse occurs at one or more inputs (Fig. 4.1).

The noise voltage impulse causes two main effects.

- (1) First of all, the sub-threshold leakage current through the pull down NMOS transistor exponentially increases with the gate-to-source voltage (VGS) variation. As a result, the dynamic node is forced to be wrongly discharged.
- (2) The drain-to-gate voltage (VDG) decreases with VGS increasing, thus decrementing the drain-to-gate leakage current.

Unfortunately, the reduction of the gate leakage current is almost irrelevant if compared with the increase of the sub-threshold leakage current. In fact, the drain-to-gate leakage dependence on VDG is less remarkable than the impact of VGS on the sub-threshold leakage current. As a result, the presence of a noise impulse at one or more gate inputs enhances the discharging mechanism of the dynamic node.

Besides an input glitch, also a fluctuation of the voltage level of the ground network may cause a wrong discharge of the dynamic node during the evaluation phase. In fact, a negative voltage pulse occurring at the ground line would increase the VGS of the NMOS transistors inside the PDN. The sub-threshold current flowing from the dynamic node would be higher, thus enhancing the discharge of the dynamic node.

From the simulation result, the leakage current was found to be 25.49 n.a.

4.2.2 Wide fan-in Domino OR gate-Footed scheme

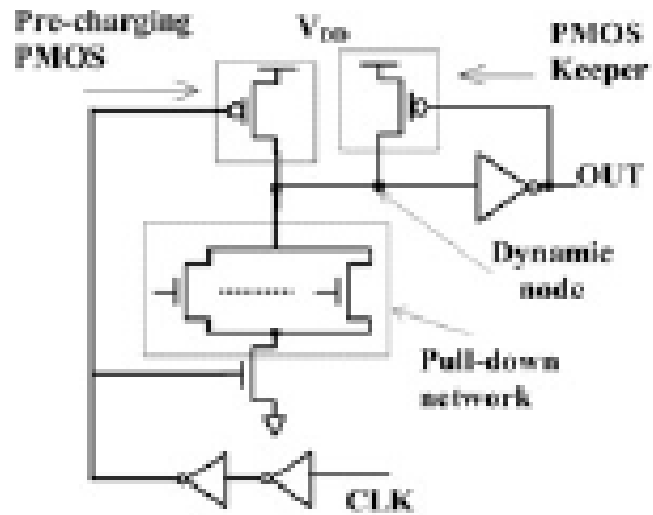


Fig. 4.5 Wide fan-in Domino OR gate-Footed scheme.

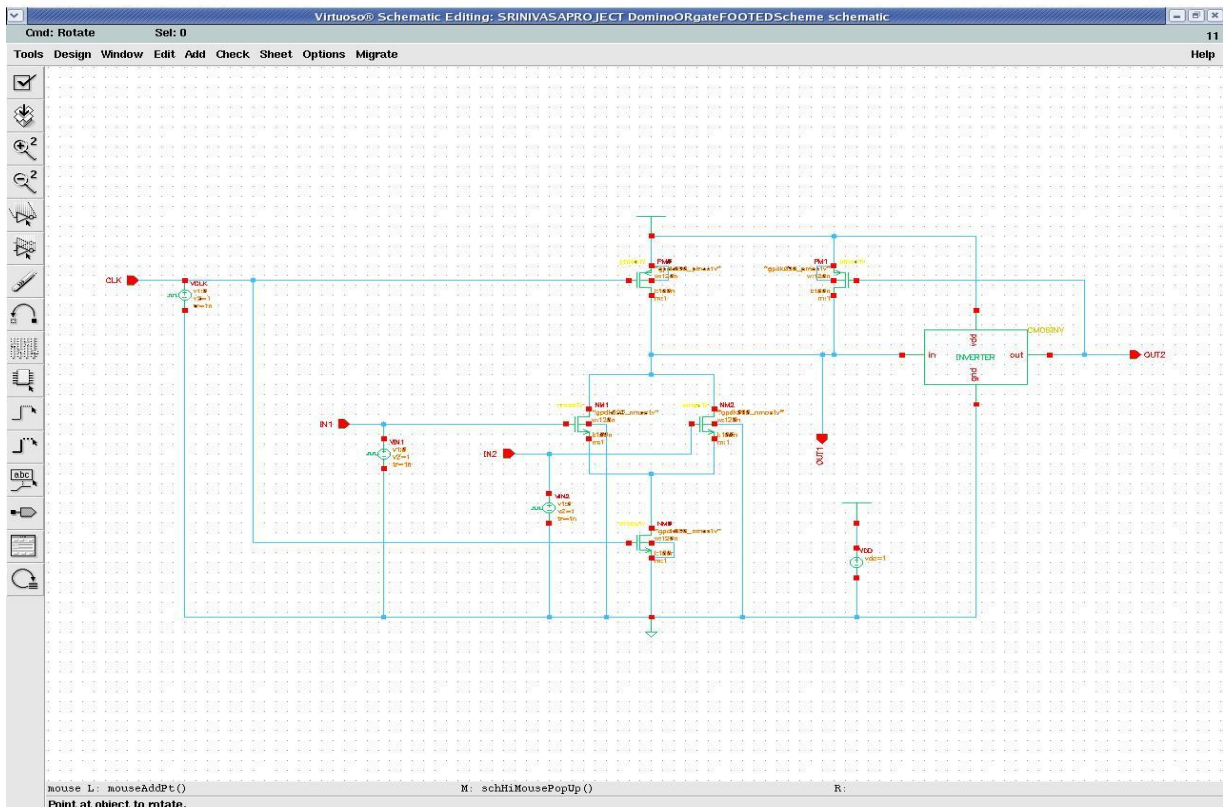


Fig. 4.6 Wide fan-in Domino OR gate-Footed schematic implementation.

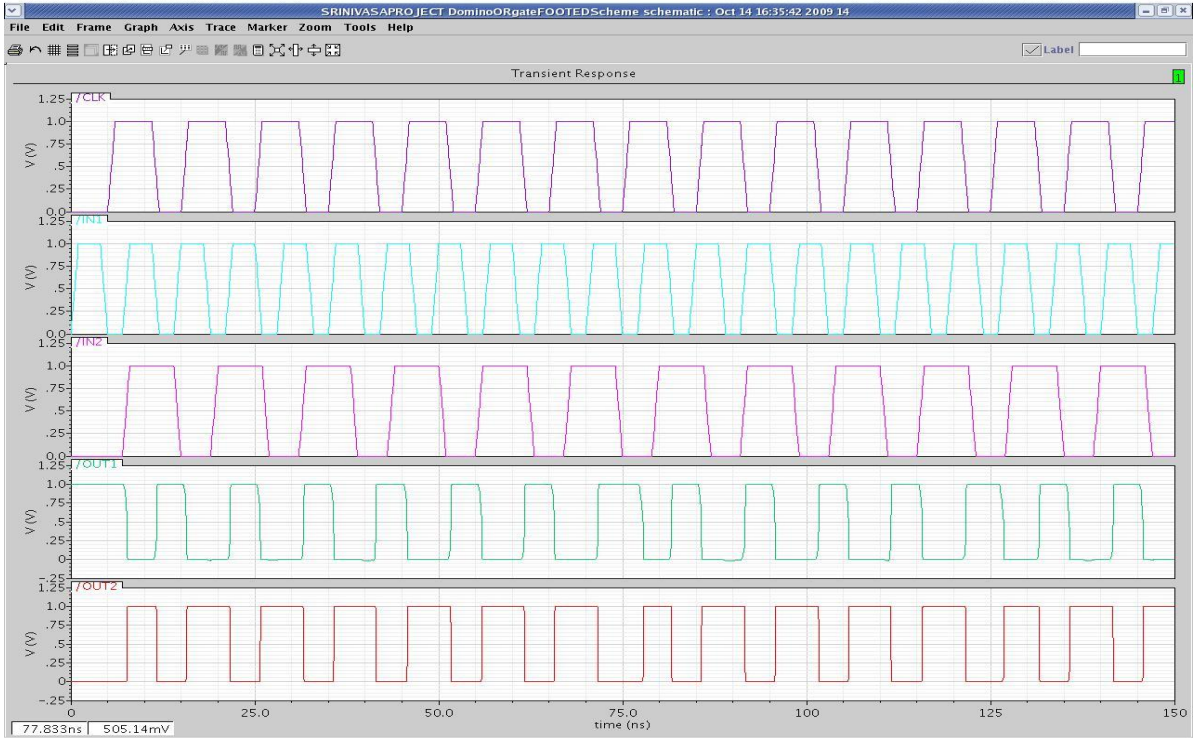


Fig. 4.7 Wide fan-in Domino OR gate-Footed schematic simulation.

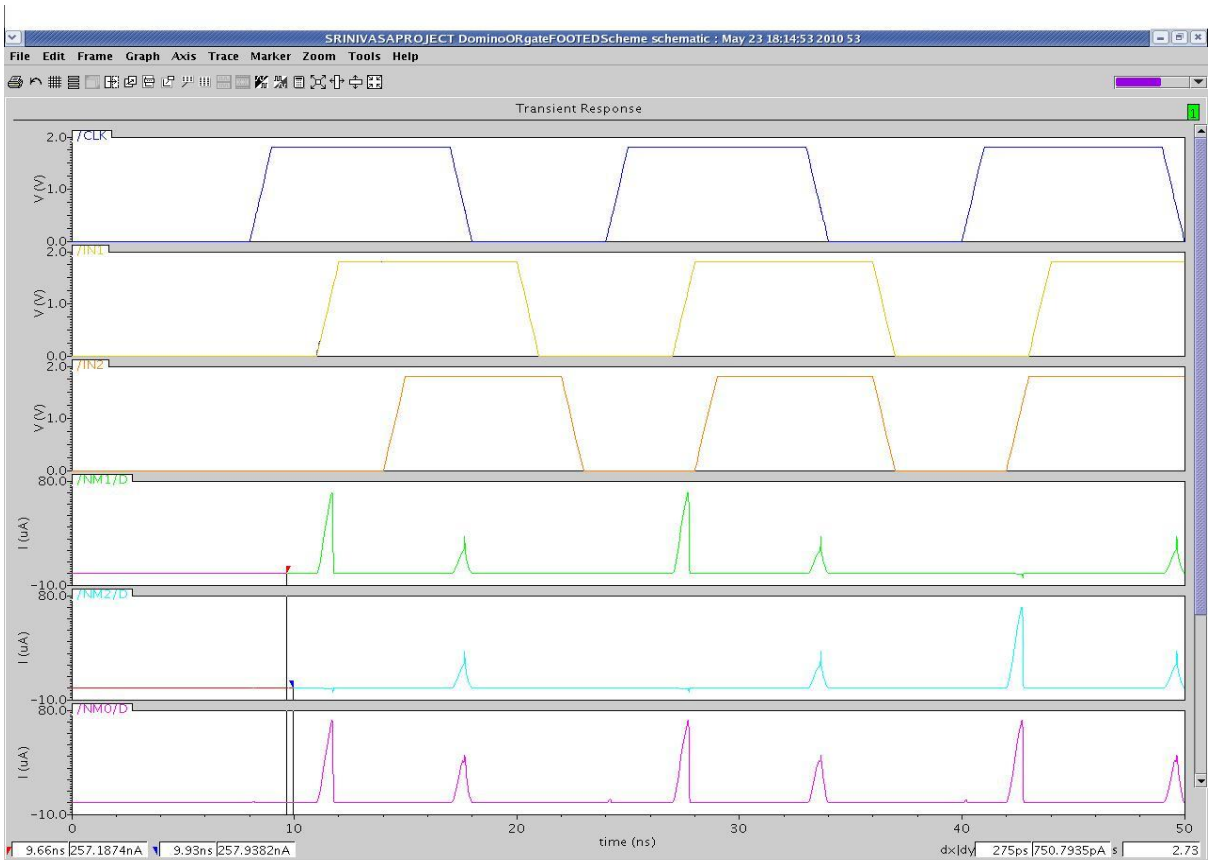


Fig. 4.8 Wide fan-in Domino OR gate-Footed schematic-Leakage current simulation.

In Wide fan-in Domino OR gate-footed schematic-Leakage current Simulation (Fig. 4.5) the leakage current was found to be 257 n.a.

4.2.3 Wide fan-in Domino OR gate-Diode footed scheme

In this section the existing noise-tolerant techniques effectively reduce the above described effects, either by

(1) reducing the sub-threshold leakage currents from the dynamic node,

Or

(2) providing greater charge restoration through the keeper transistor.

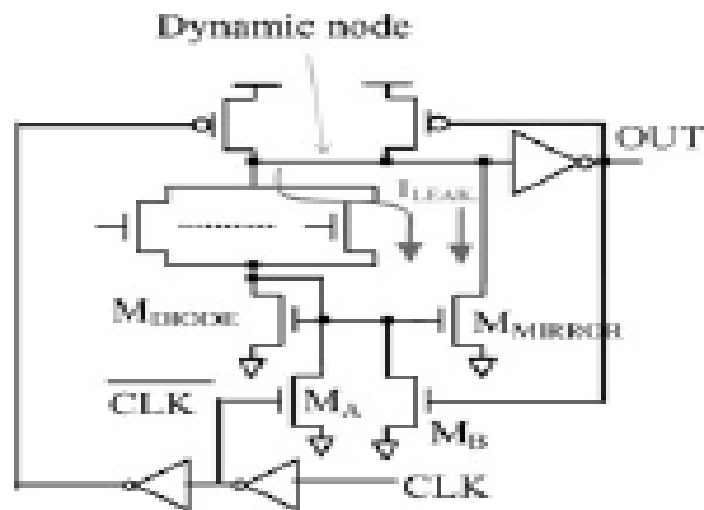


Fig. 4.9 Wide fan-in Domino OR gate-Diode footed schematic.

Fig. 4.9 depicts a wide domino OR gate based on the diode-footed scheme proposed.

- (1) The transistor MDIODE (diode-footer) limits the sub-threshold current during the evaluation phase exploiting the stack effect.
- (2) Owing to the leakage current of the evaluation network, a voltage drop is established across MDIODE.
- (3) This voltage drop makes the VGS voltage of the 'off' NMOS transistors in the evaluation network negative and, as a consequence, their sub-threshold leakage current exponentially decreases.

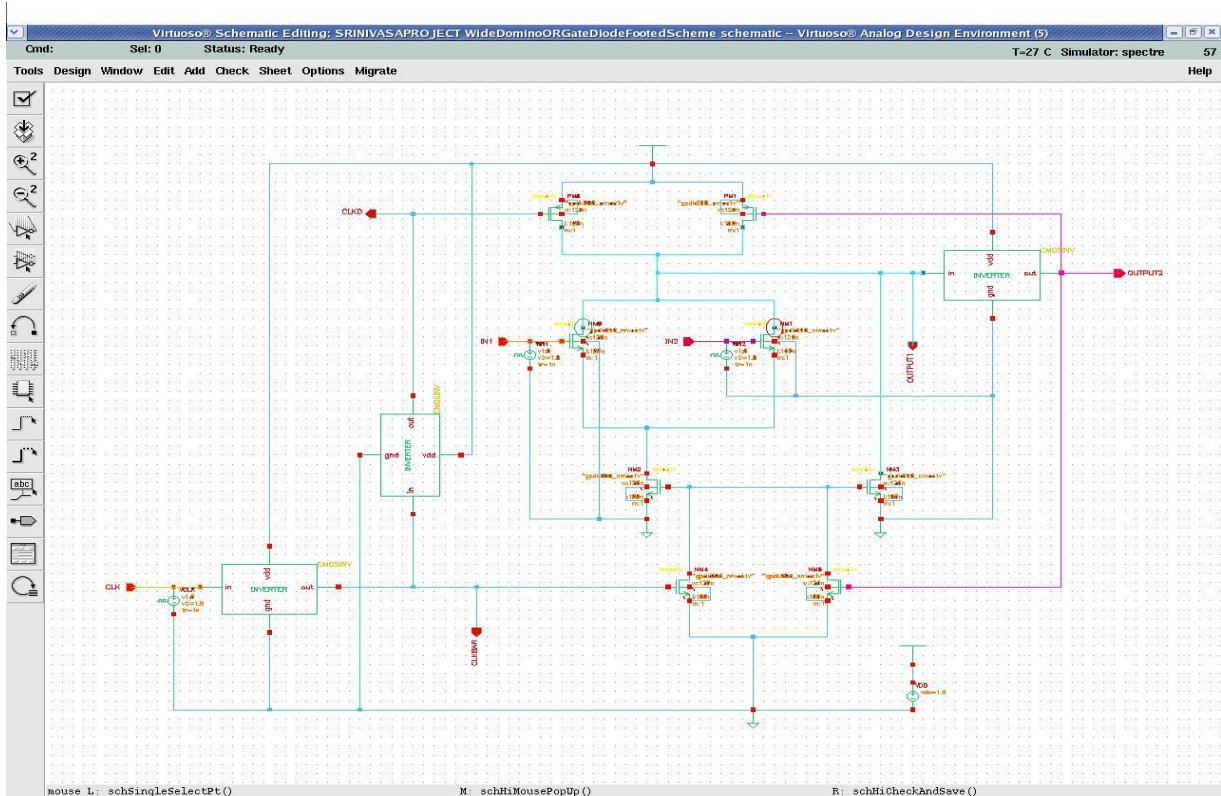


Fig. 4.10 Wide fan-in Domino OR gate-Diode footed schematic implementation.

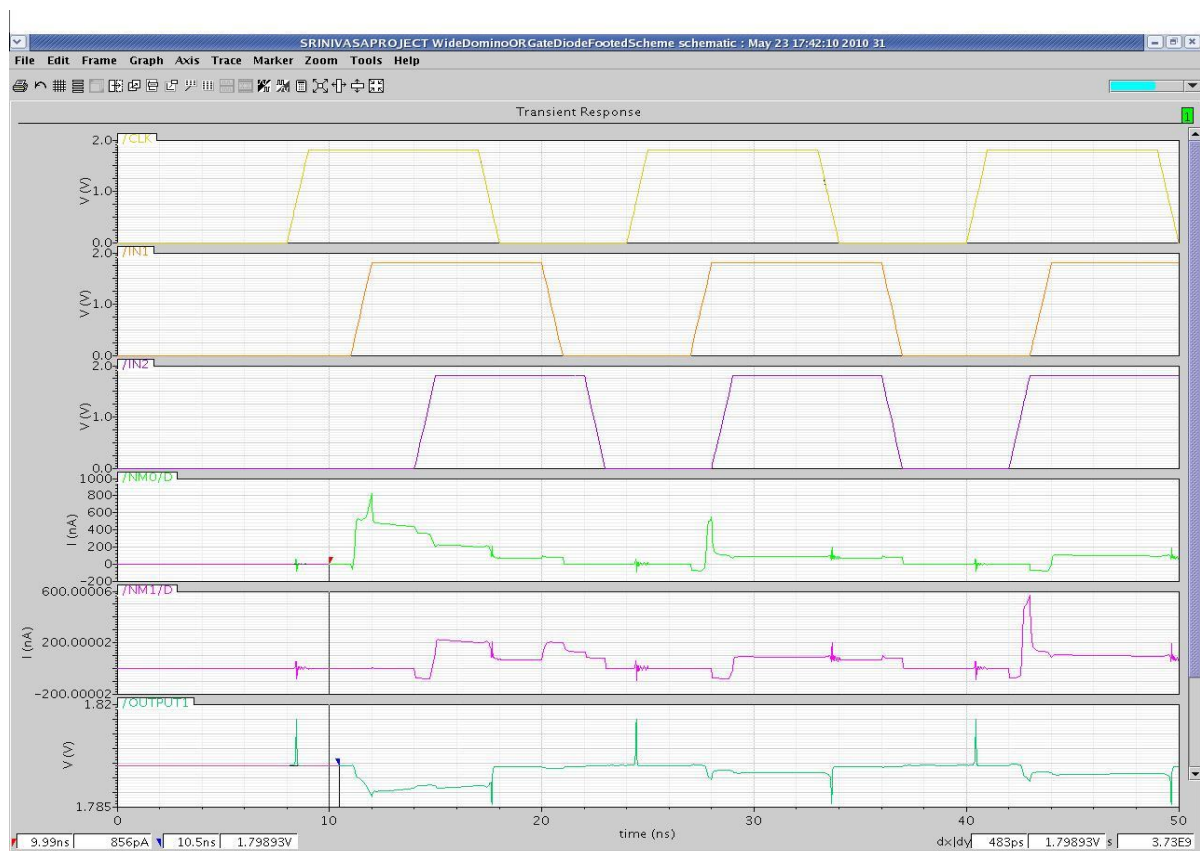


Fig. 4.11 Wide fan-in Domino OR gate-Diode footed schematic simulation.

From simulation results the Leakage current was found to be 856 p.a.

Advantages:

- (1) Sub-threshold leakage current exponentially decreases.
- (2) The mirror network composed of the transistors MA, MB and MMIRROR offers an alternative discharging path for the dynamic node and allows high performance to be reached.
- (3) By varying the dimension of MMIRROR, the gate delay and the noise sensitivity can be differently balanced.
- (4) Low area overhead.

Disadvantages:

- (1) The diode-connected NMOS increases the equivalent resistance of the evaluation path, thus making the gate slower.
- (2) High values of noise robustness achieved at the expense of the gate delay.

Why does gate become slower?

Since the diode connected NMOS increases the equivalent resistance of “evaluation” path.

To avoid gate noise sensitivity, the following technique is preferred.

4.2.4 Wide fan-in Domino OR gate-Replicated evaluation of PDN scheme

- (1) The gate noise sensitivity can be reduced by replicating the evaluation network, as depicted in Fig. 4.12.
- (2) The NMOS transistor MP aims to increase the voltage at the node between the two equal evaluation networks.
- (3) In this way, the VGS of the NMOS inside the upper evaluation network is reduced and the sub-threshold leakage current decreases.

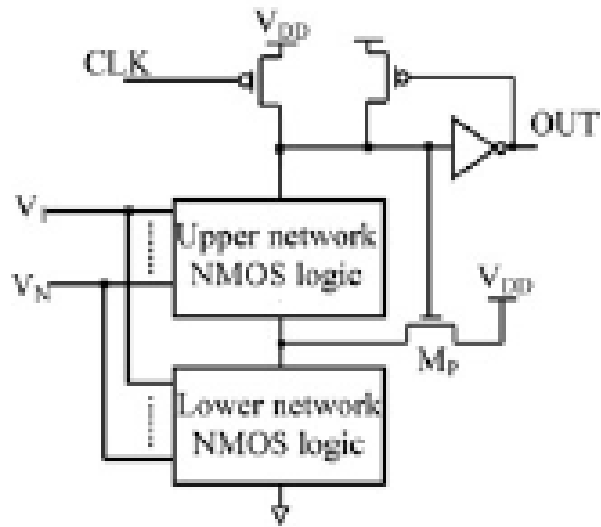


Fig. 4.12 Wide fan-in Domino OR gate-Replicated evaluation of PDN scheme.

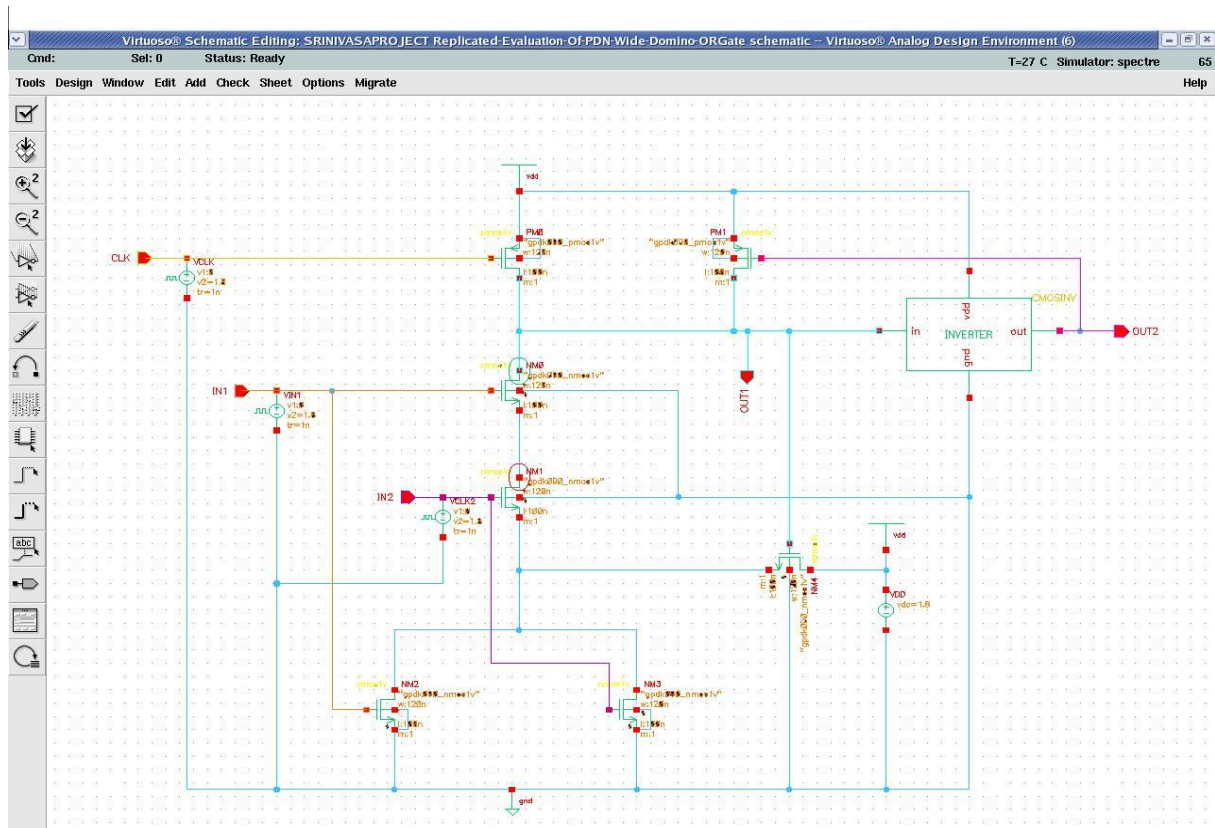


Fig. 4.13 Wide fan-in Domino OR gate-Replicated evaluation of PDN schematic implementation.

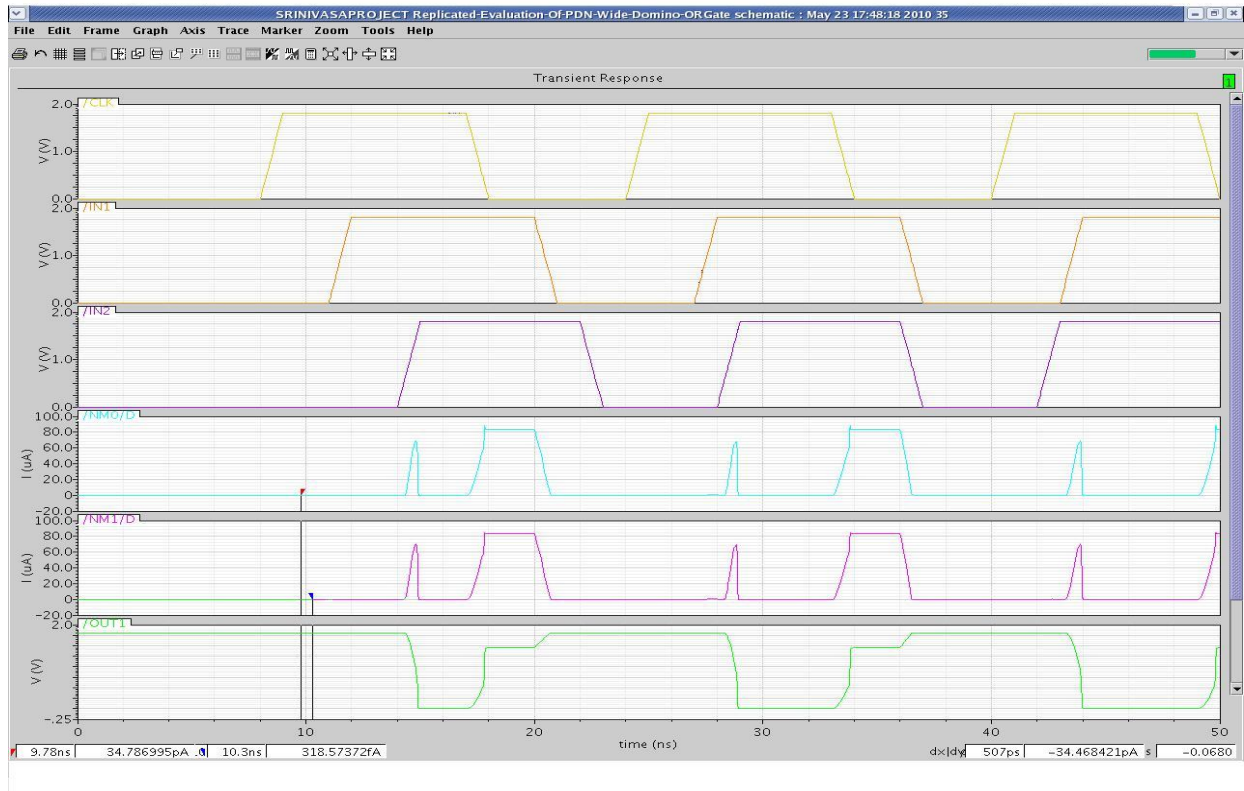


Fig. 4.14 Wide fan-in Domino OR gate-Replicated evaluation of PDN schematic simulation.

From the simulation results, the leakage current was found to be 34.7 p.a.

Advantages:

- (1) The gate noise sensitivity is reduced by replicating the evaluation network
- (2) The NMOS transistor MP aims to increase the voltage at the node between the two equal evaluation networks. In this way, the VGS of the NMOS inside the upper evaluation network is reduced and the sub-threshold leakage current decreases.
- (3) Both the occupied area and the gate delay are considerably compromised.

Disadvantages:

- (1) Owing to the presence of two evaluation networks connected in series, the capacitive load at each input is doubled.
- (2) This invalidates the classic advantages of a domino gate with respect to its static counterpart which has smaller capacitive loads of the input lines.

To avoid the capacitive loading problems, a new technique is preferred. Actually we need higher performance with smaller capacitive loads of input lines which we had in static counterpart logic.

4.2.5 Wide fan-in Domino OR gate-Dynamic node footed scheme

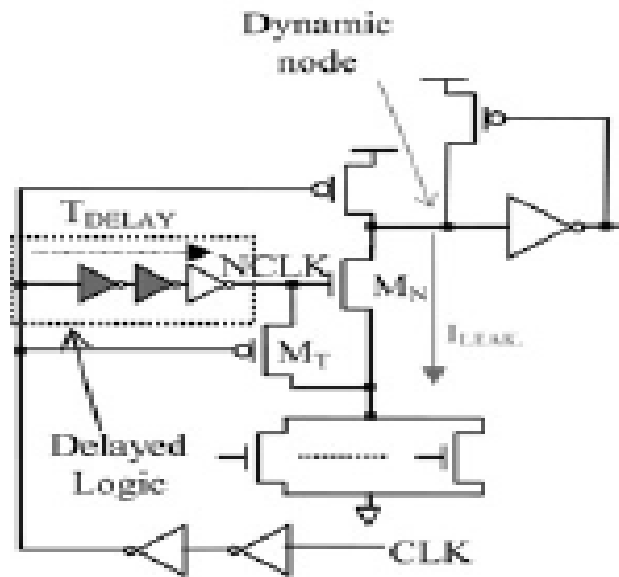


Fig. 4.15 Wide fan-in Domino OR gate Dynamic node footed schematic.

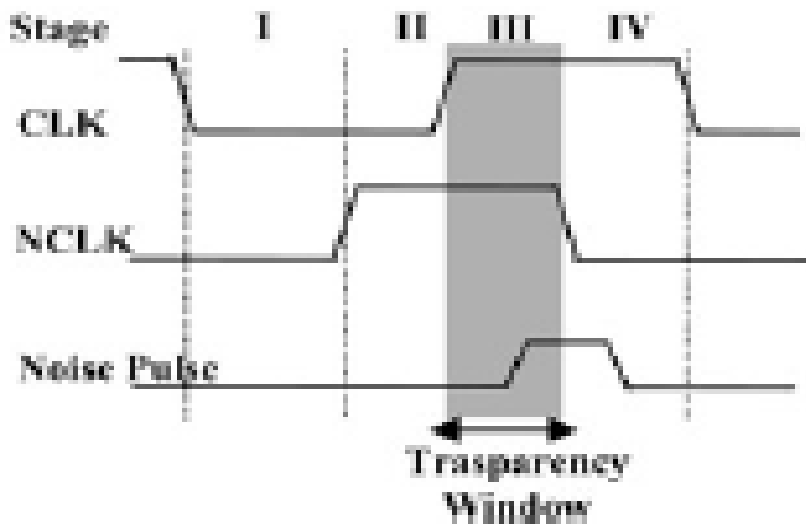


Fig. 4.16 Signal stages of Wide fan-in Domino OR gate-Dynamic node footed schematic.

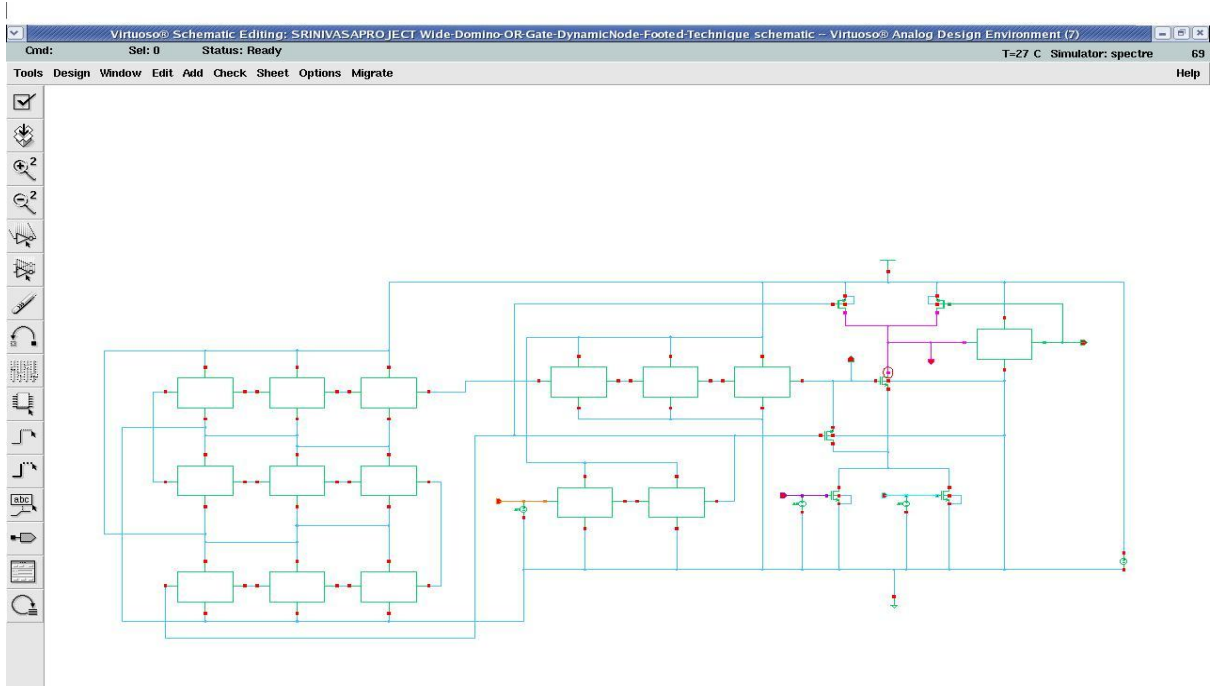


Fig. 4.17 Wide fan-in Domino OR gate-Dynamic node footed schematic implementation.

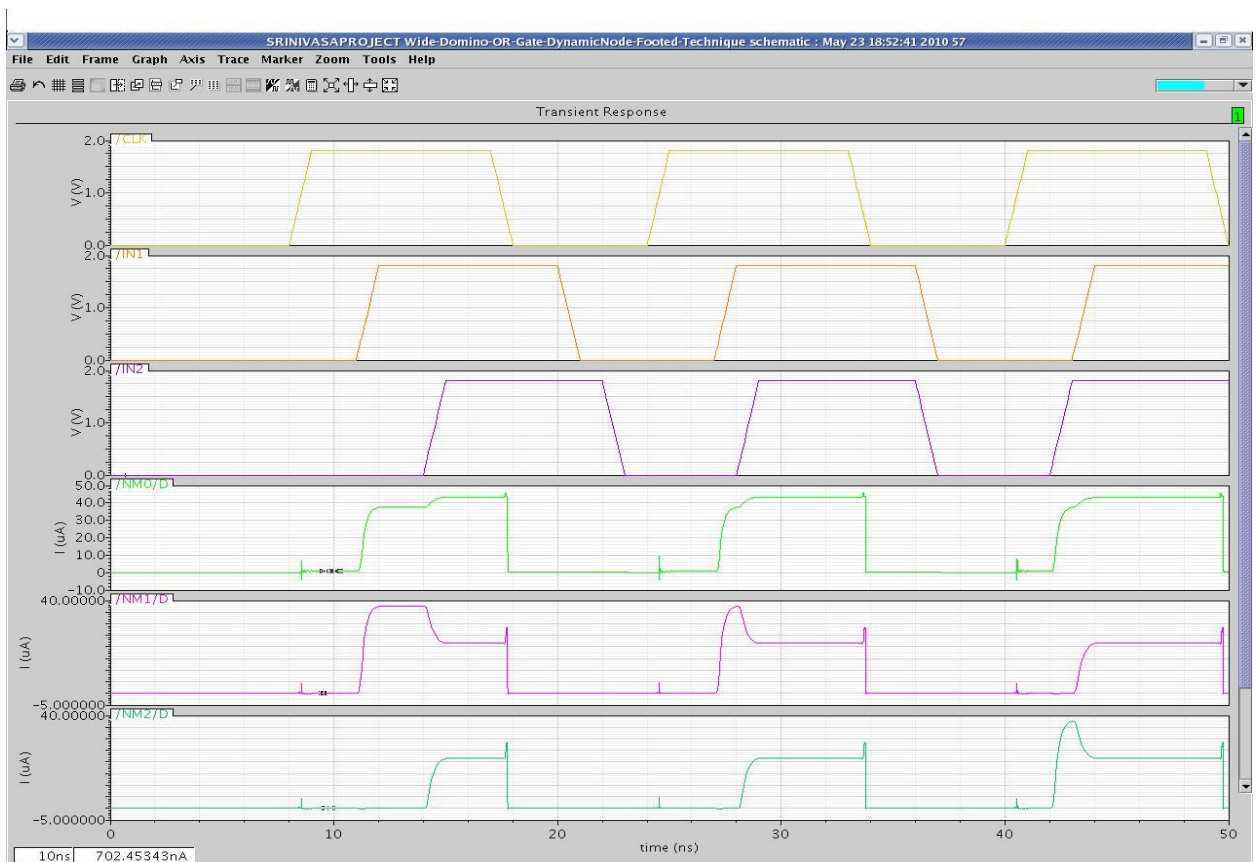


Fig. 4.18 Wide fan-in Domino OR gate-Dynamic node footed schematic-leakage current simulation.

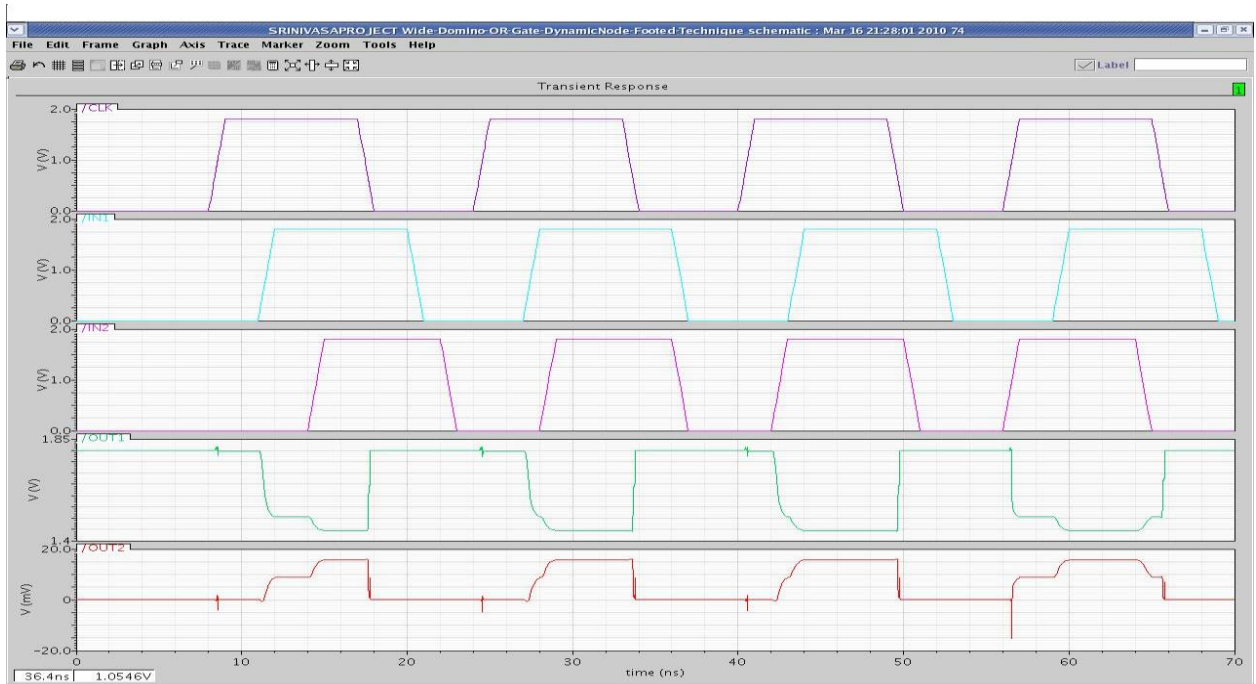


Fig. 4.19 Wide fan-in Domino OR gate-Dynamic node footed schematic simulation.

From the simulation result, the leakage current was found to be 702 n.a.

Advantages:

- (1) An NMOS transistor MN is inserted between the dynamic node and the PDN. Thus this technique will be referred to as the dynamic node-footed scheme.
- (2) Three static inverters and the PMOS transistor MT are exploited to properly turn MN on.
- (3) At the beginning of the evaluation phase, owing to the finite delay of the inverters-chain (TDELAY), both the CLK and NCLK signals are high. During this time (the “Transparency Window”), the gate can elaborate the input signals and the dynamic node can be eventually discharged.
- (4) After the time TDELAY is elapsed, NCLK becomes low and MN is turned off. In this condition, owing to the stack effect, the charge leakage from the dynamic node to ground is exponentially reduced and the noise immunity of the gate is increased.
- (5) Like the diode-footed technique, also the dynamic node-footed scheme leads to a very low area overhead.

Disadvantages:

(1) The increased capacitive load of the CLK line and the increased resistance of the discharging path for the dynamic node because of the presence of the extra transistor MN.

(2) Impact of T Delay:

Case (1): The longer the TDELAY, the wider the gate transparency window, the faster the gate and the lower the noise immunity.

Case (2): The smaller the TDELAY, the thicker the transparency window. This leads to a slower gate but also to greater noise robustness.

The three techniques described above (Fig. 4.9, Fig. 4.12, Fig. 4.15) reduce the leakage current flowing through the dynamic node by exploiting the stack effect. These approaches do not reduce the overall leakage current, but only the leakage current at the dynamic node that drives the final static inverter and is the critical node.

4.2.6 CLK delayed single keeper scheme

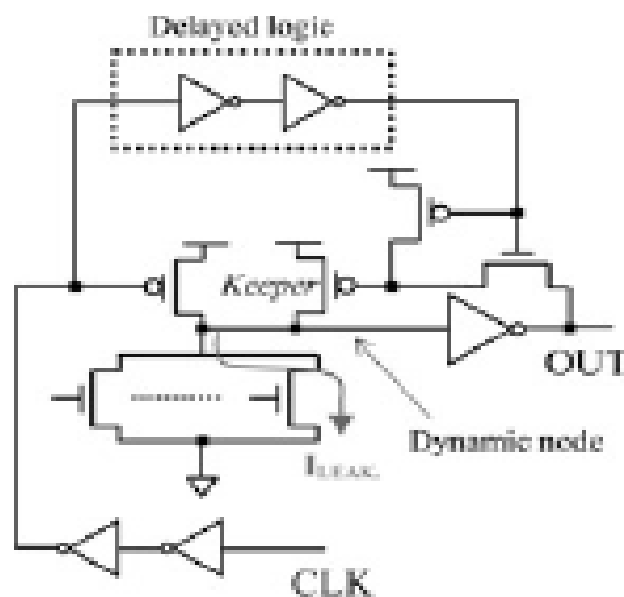


Fig. 4.20 CLK Delayed single keeper schematic.

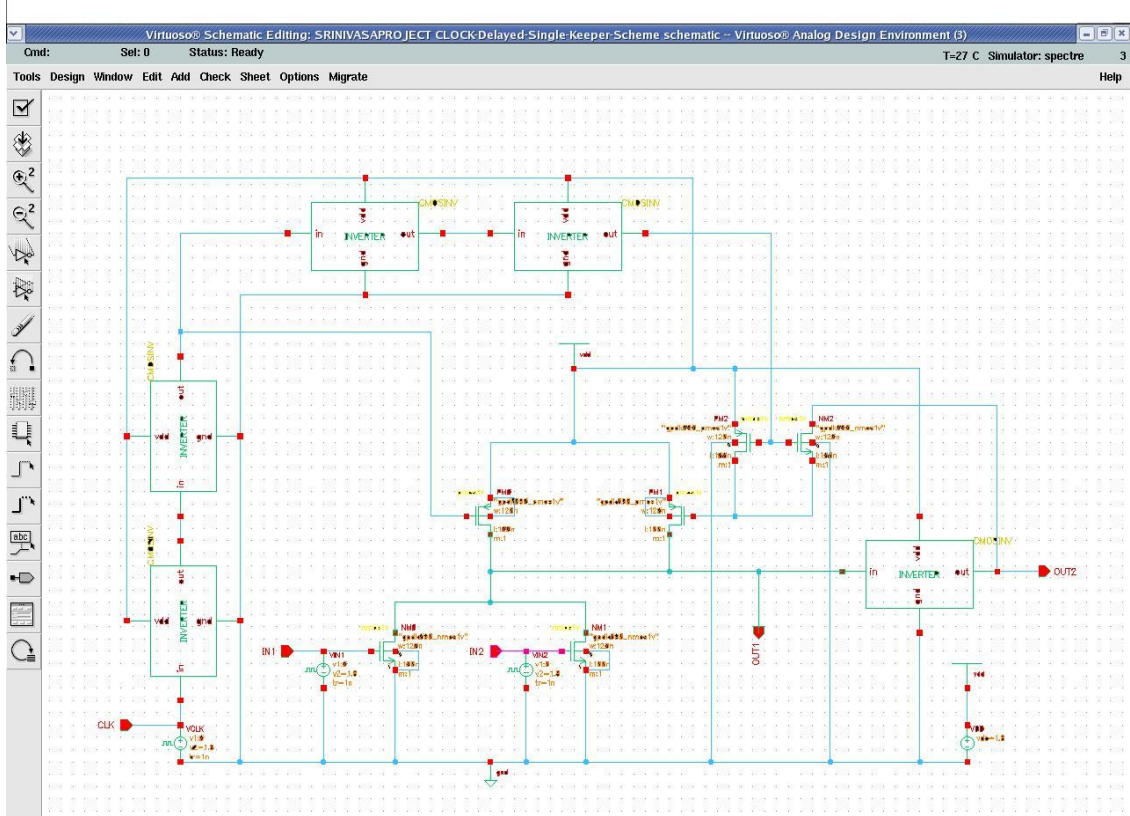


Fig. 4.21 CLK Delayed single keeper schematic implementation.

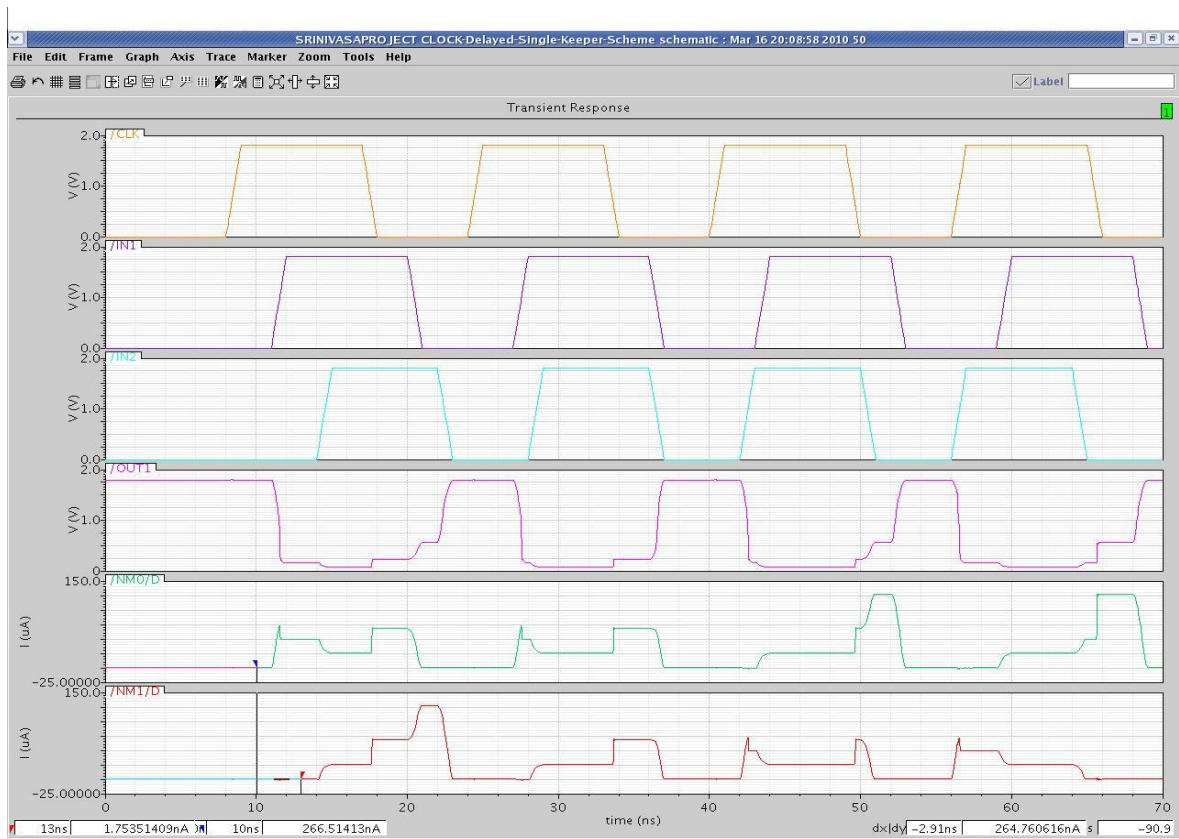


Fig. 4.22 CLK Delayed single keeper schematic simulation.

From the simulation result, the leakage current was found to be 266 n.a.

Advantage:

This technique is effective in reducing the noise sensitivity.

Disadvantage:

It leads to an increased capacitive load of the clock line because of the presence of the extra delayed logic.

4.2.7 Source Following Evaluation Gate

The so-called source following the evaluation gate (SFEG) technique, independently demonstrated and depicted in [Fig. 4.23](#).

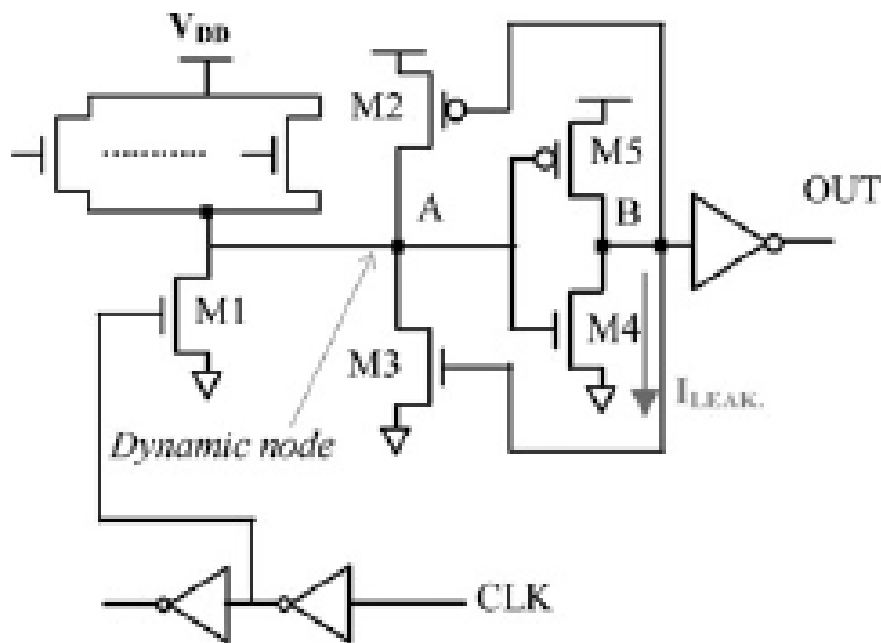


Fig. 4.23 Source Following Evaluation Gate schematic.

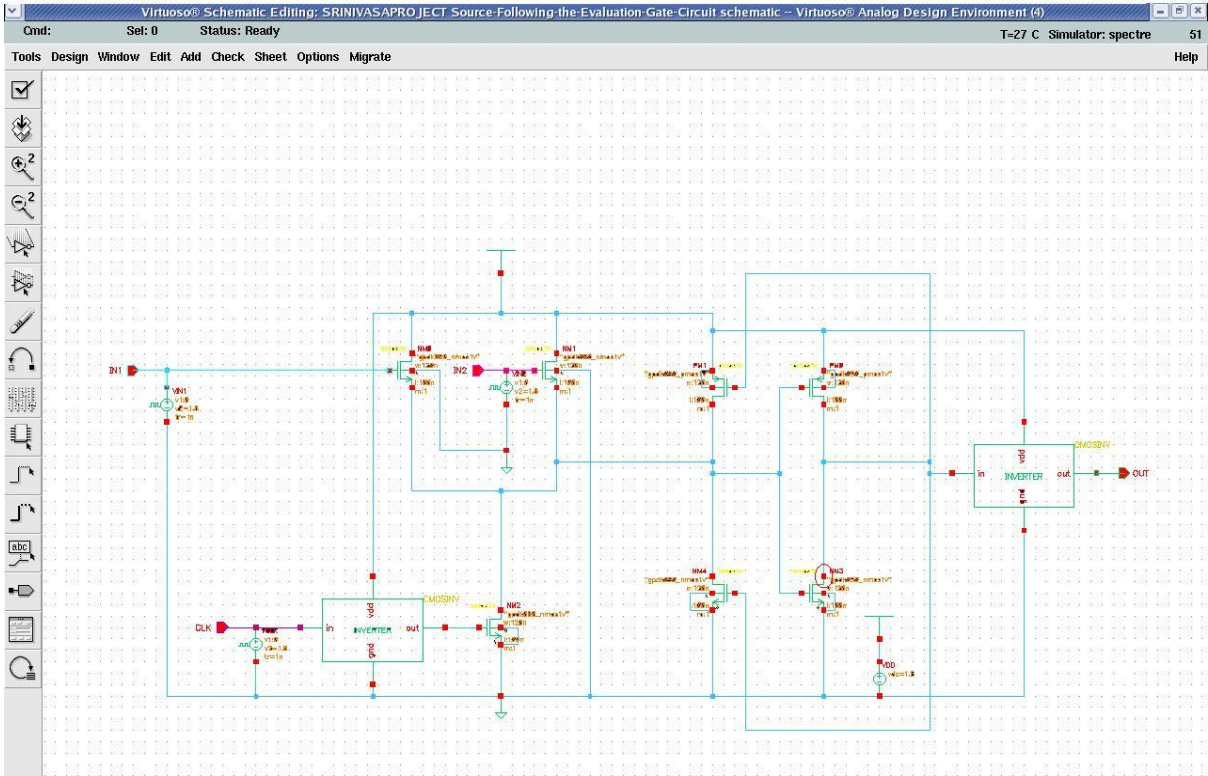


Fig. 4.24 Source Following Evaluation Gate schematic implementation.

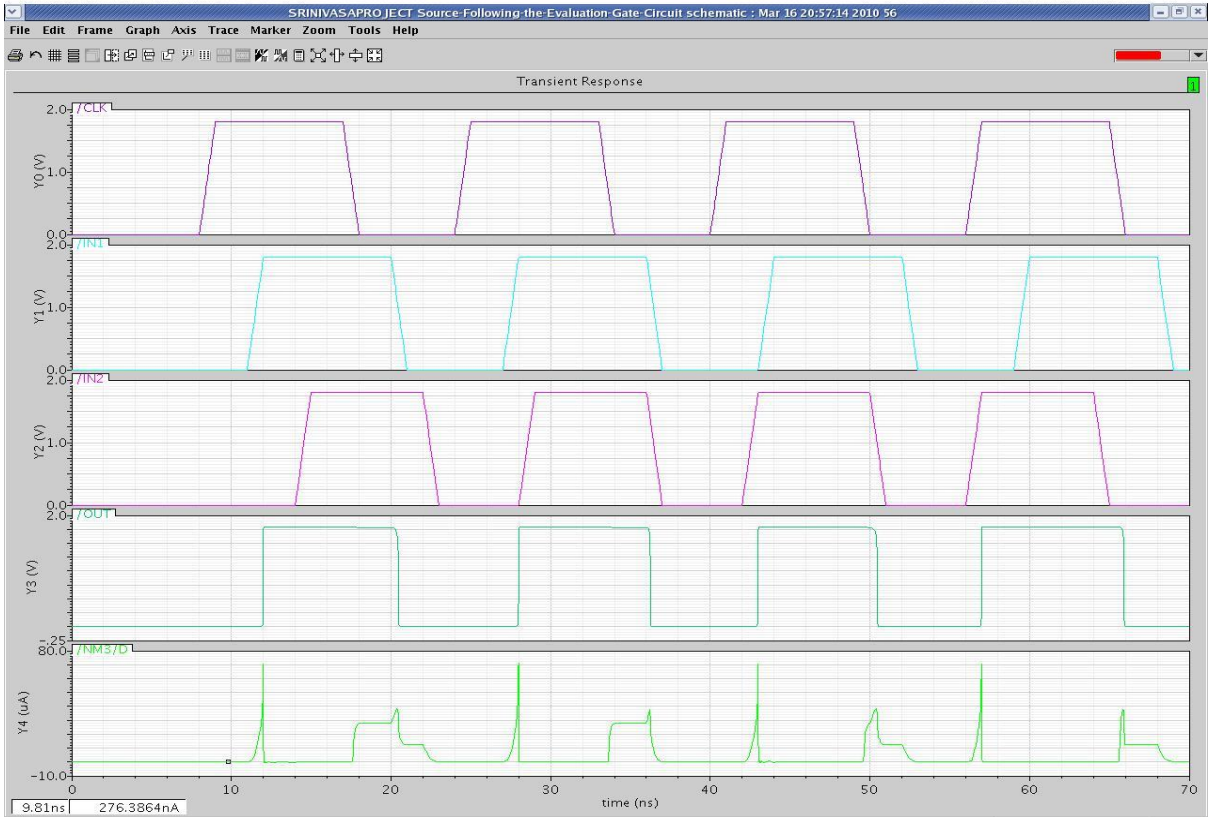


Fig. 4.25 Source Following Evaluation Gate schematic simulation.

From the simulation results the leakage current was found to be 276 n.a.

Advantages:

- (1) The noise immunity of the gate is increased by implementing the logic function by means of an NMOS pull-up network.
- (2) The leakage currents flowing through the evaluation network aim to charge the dynamic node (the node A). This event reduces the VGS of the NMOS transistors as a consequence the leakage currents are exponentially decreased.
- (3) The critical node driving the final static Inverter does not coincide with the dynamic node and thus, the critical node leakage current (I_{leak}) is only Because of the nmos (M4).

Disadvantages:

- (1) The NMOS pull-up network is able to charge the dynamic node only up to $V_{DD}-V_{TH}$ during an actual switching of the gate. The threshold voltage drop is compensated by the pull-up PMOS transistor M2.
- (2) However, the transistor M2 is not immediately turned on because of the finite delay of the feedback loop that drives M2 itself. For this reason, the short-circuit current, flowing through the path M4–M5 during the gate switching, causes an increased dynamic energy dissipation.

4.3 Improved high-performance noise tolerant circuit techniques

4.3.1 Improved Wide fan-in Domino OR gate-Footed scheme

This modified technique has been proposed to reduce the leakage noise sensitivity of high fan-in footed domino gates. All the existing techniques improve the noise robustness of domino gates at a significant cost in terms of delay or energy consumption.

To prove the efficiency of the proposed technique, the external NMOS transistor is inserted between the evaluation PDN network and footer transistor. The purpose is to reduce sub threshold leakage current that flows through evaluation PDN, thereby reducing the gate noise sensitivity.

The modified circuit is designed and simulated.

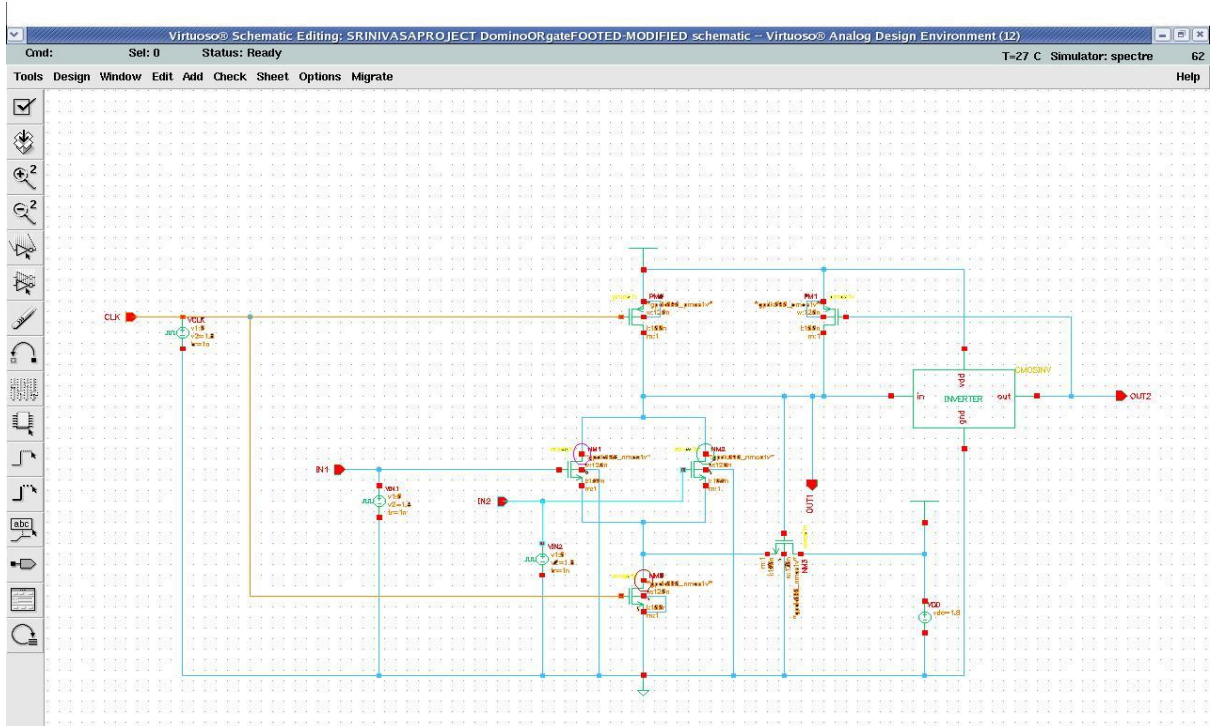


Fig. 4.26 Improved Wide fan-in Domino OR gate-Footed schematic implementation.

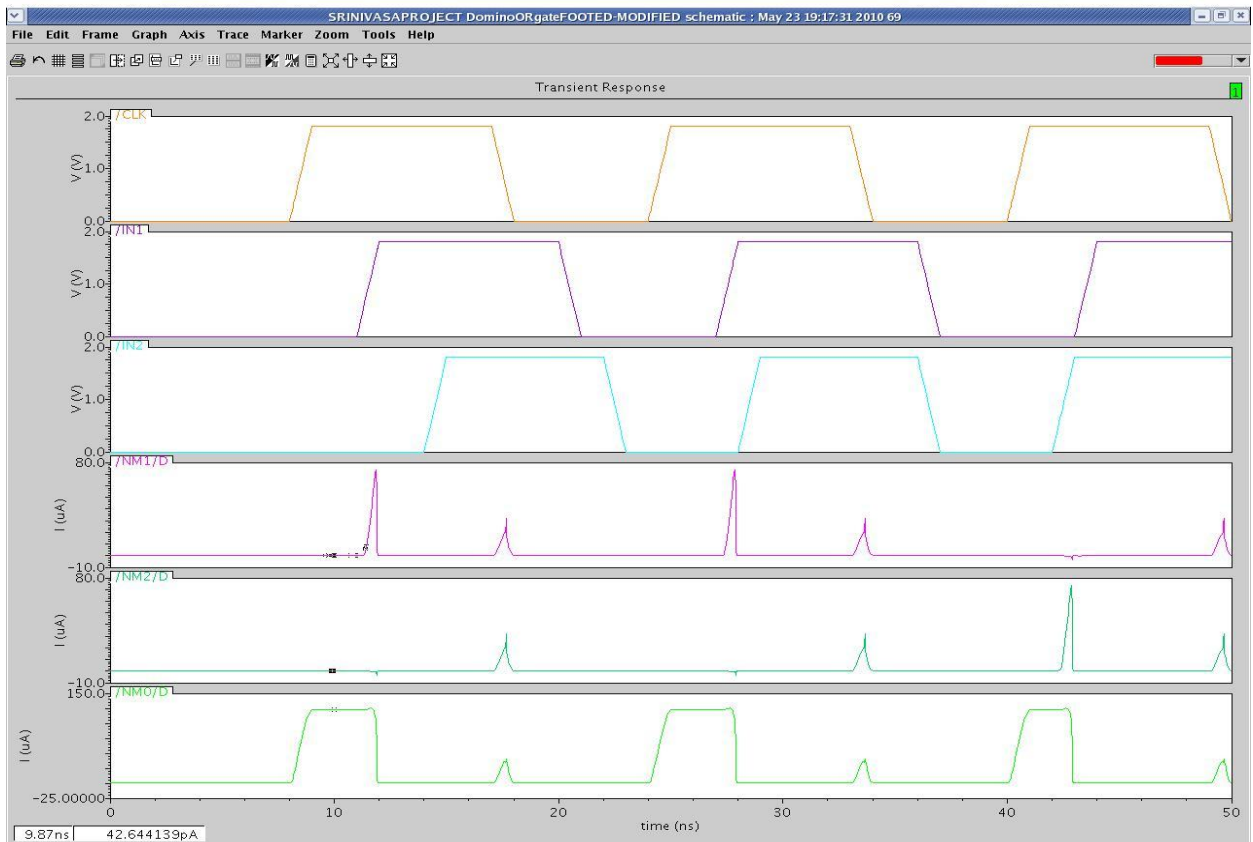


Fig. 4.27 Improved Wide fan-in Domino OR gate-Footed schematic simulation.

From the simulation result, the leakage current was found to be 42 p.a.

Advantages:

- (1) Leakage current is reduced considerably.

Disadvantages:

- (1) Though the leakage current through evaluation PDN is reduced, the current through footer is again increased, i.e. the leakage current through footer is 122 u.a.
- (2) Discharge of dynamic node is not so fast as previous technique (unmodified).

4.3.2 Modified Wide fan-in Domino OR gate-Footless scheme

Actually the same modified logic, which had been applied to footed technique, was applied to this technique also. The corresponding schematic implementation along with its simulation result is shown below.

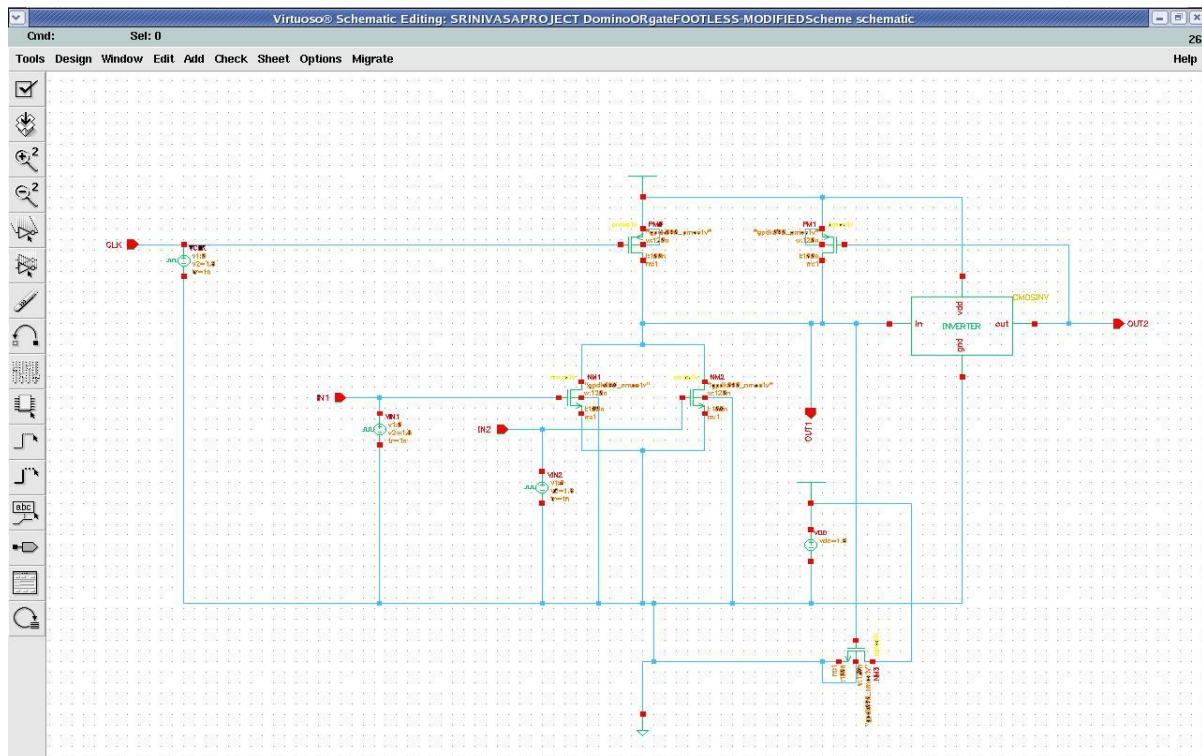


Fig. 4.28 Modified Wide fan-in Domino OR gate-Footless schematic implementation.

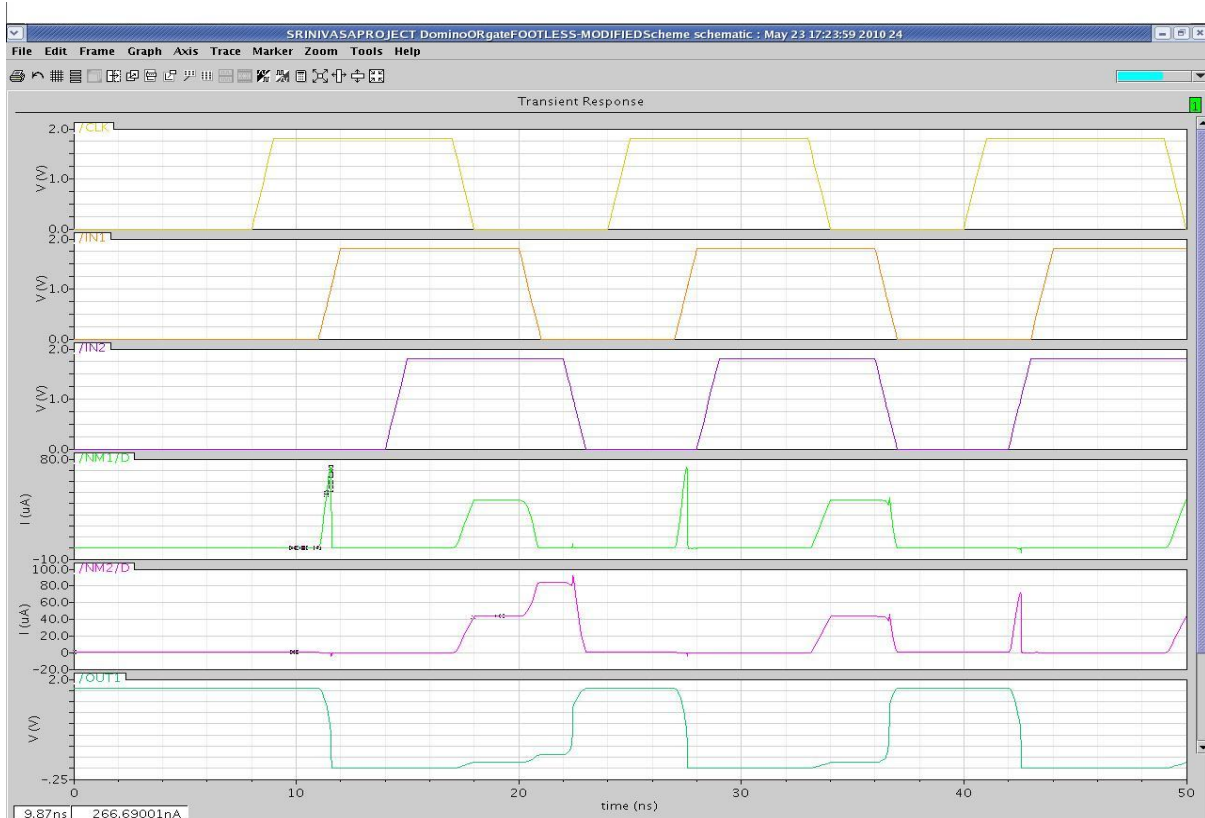


Fig. 4.29 Modified Wide fan-in Domino OR gate-Footless schematic simulation.

The modified version is not giving faithful results. Though the same modified logic is applied to this circuit also, it does not hold good in this case, since it does not possess footer transistor.

Thus the discharging of dynamic node is fast enough without modification. If any transistor is added to this PDN, then it reduces the sources potential, thereby increasing sub threshold leakage current.

From the simulation result, the leakage current was found to be 266.9 n.a.

Drawbacks:

- (1) Increased sub threshold leakage current.
- (2) The equivalent resistance of PDN network may increase.
- (3) Gate delay may be present.

Thus this modified network may be omitted.

4.3.3 Improved Wide fan-in Domino OR gate-Dynamic node footed scheme

To avoid the capacitive loading problems, we go for this modified new technique. The following modified circuit fulfils our requirements. In spite of having few drawbacks, as a whole its results are better than most other techniques.

Modifications made:

- (1) Reduction of the Transparency window (T delay) so that greater the noise robustness.
- (2) Insertion of NMOS transistor M_n between dynamic node and PDN.

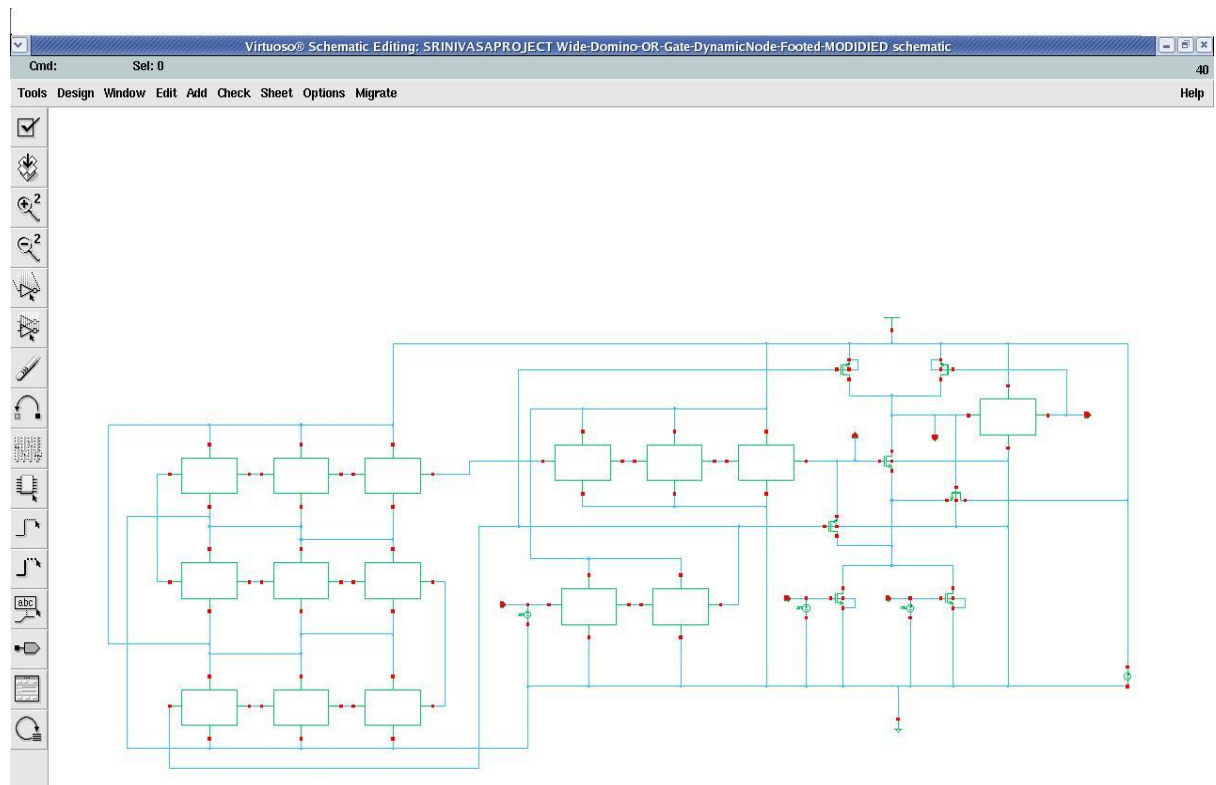


Fig. 4.30 Improved Wide fan-in Domino OR gate-Dynamic node footed schematic implementation.

This modified circuit is simulated and corresponding simulation result is shown below.

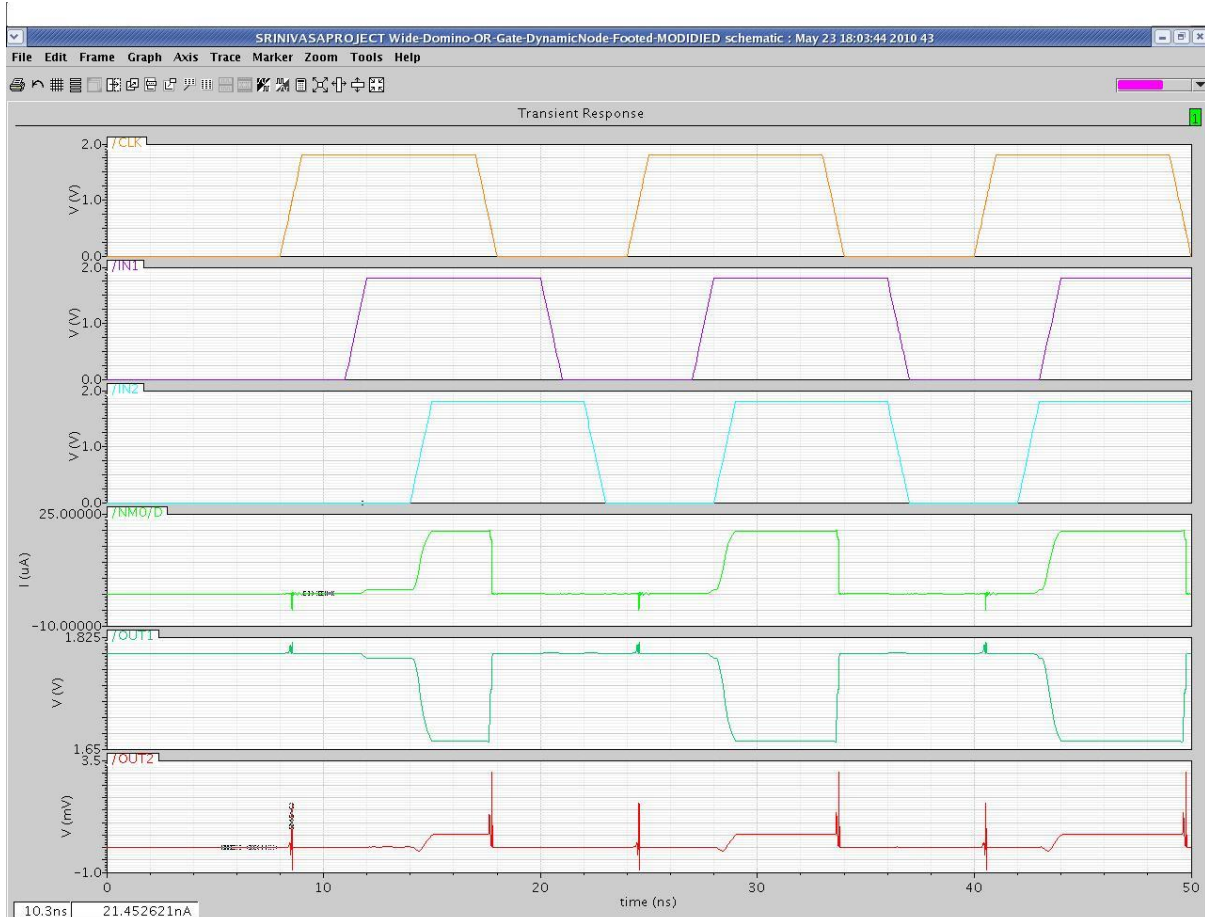


Fig. 4.31 Improved Wide fan-in Domino OR gate-Dynamic node footed schematic simulation.

From the simulation result, the leakage current was found to be 21.45 n.a.

Advantages:

- (1) High noise robustness.
- (2) Reduction of leakage current.
- (3) Low area over overhead.

Disadvantages:

- (1) Increased capacitive load of CLK line and increased resistance of discharging path of dynamic node due to presence of Mn and NMOS-externally inserted transistor.
- (2) Series of inverters, Mn, NMOS-externally inserted transistor all these cause dynamic energy dissipation, even output does not change.

TABLE 4.1 Leakage current comparisons among different techniques of Wide fan-in Domino OR gate.

Circuit technique	Leakage current
Foot-less	25.49 n.a
Footed	257 n.a
Diode-footed	856 p.a
Replicated evaluation of PDN	34.7 p.a
Dynamic node footed	702 n.a
CLK delayed	266 n.a
SFEG	276 n.a

TABLE 4.2 Leakage current comparisons between Unmodified & Improved techniques of Wide fan-in Domino OR gate.

Circuit technique	Leakage current	
	Un-modified	Improved
Footed	257 n.a	42 p.a
Footless	25.49 n.a	266.9 n.a
Dynamic node footed	702 n.a	21.45 n.a

CHAPTER 5

CONCLUSION

Domino CMOS logic circuit family finds a wide variety of applications in microprocessors, digital signal processors, and dynamic memory due to their high speed and low device count. Domino logic is a CMOS logic style obtained by adding a static inverter to the output of the basic dynamic gate circuit.

In this thesis, An introduction to domino logic, The impact of CMOS technology scaling on the performance of domino CMOS logic, Three Phase Domino Logic Circuit, High-performance noise-tolerant circuit techniques for CMOS dynamic logic and other Domino logic techniques are studied and corresponding Domino logic techniques have been designed & simulated. The results are studied. The advantages & disadvantages are also observed.

Advantages of Domino CMOS logic:

- (1) High speed
- (2) Low device count.

Disadvantages:

- (1) Degradation of Noise immunity.
- (2) Inevitable leakage currents.
- (3) Charge sharing.
- (4) Large power consumption.

In all those techniques the important effects like sub threshold leakage currents, threshold voltages, supply voltages, sources of noise, power consumptions, delays and area are considered. Few modifications have also been made to already existing domino techniques to get desired results. The improved techniques, though they suffer from few drawbacks, are giving better results compared with previous techniques.

Different Domino logic circuits are simulated in both Cadence virtuoso (implemented using GPDK090- library of 90nm technology) and Mentor graphics (implemented at different technologies like Tsmc 035.mod, Tsmc 025.mod, Tsmc 018.mod) environments. The performance parameters of improved techniques are also compared with other standard architectures of Domino logic.

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